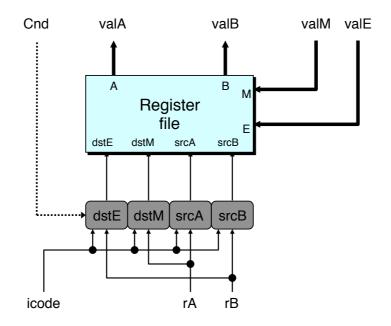
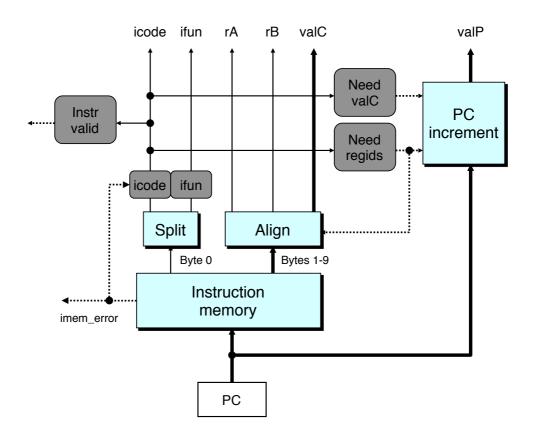


SEQ: hardware structure (defined in seq/seq-std.hcl)

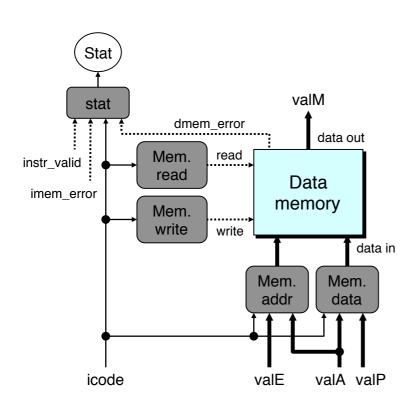
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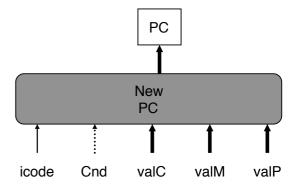


SEQ: decode and write-back stage



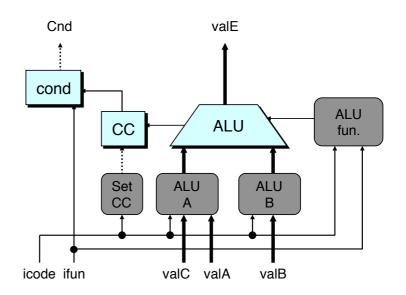
SEQ: fetch stage



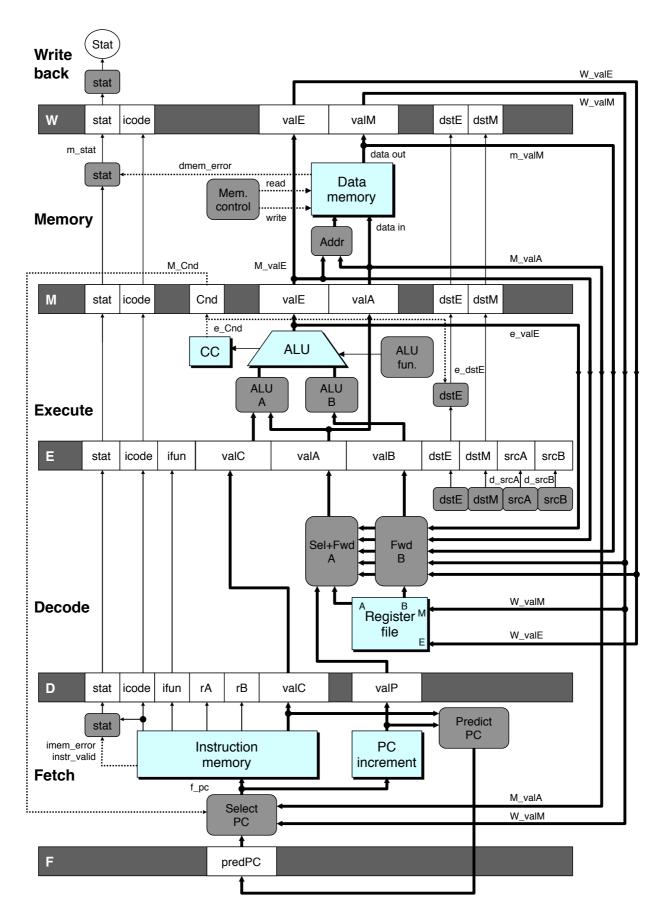


SEQ: PC update stage

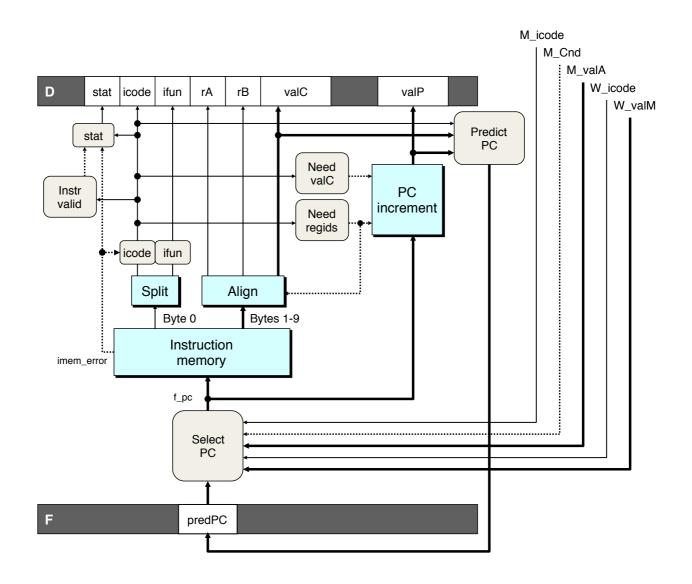
SEQ: memory state



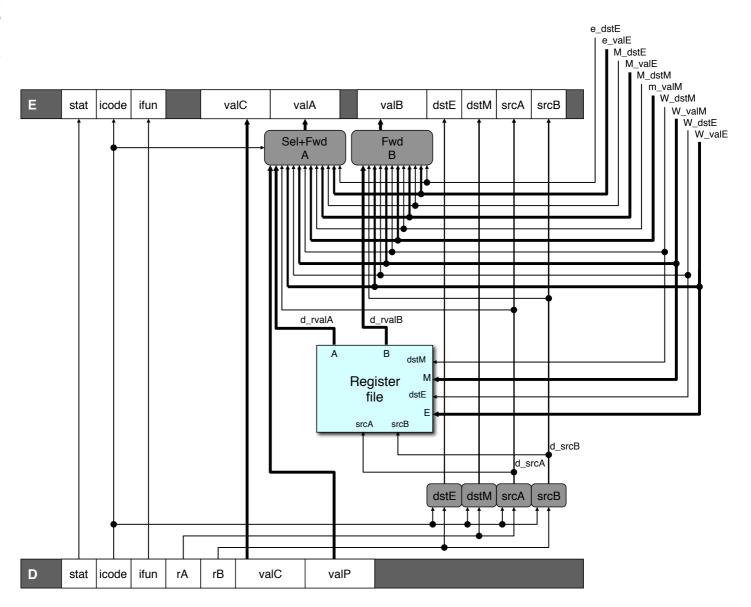
SEQ: execute state



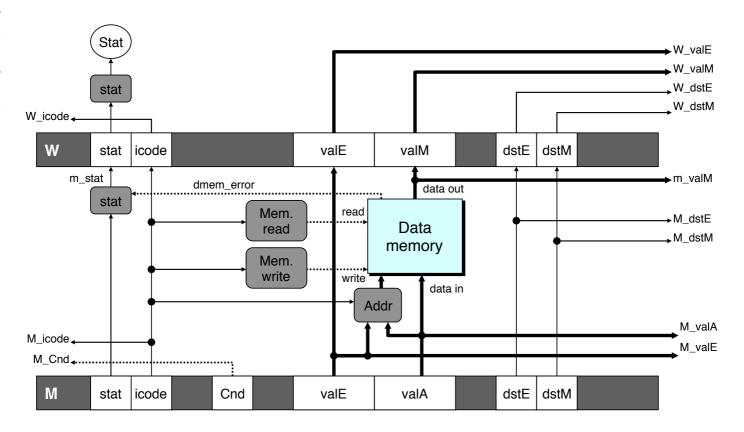
PIPE: hardware structure (defined in pipe/pipe-std.hcl)



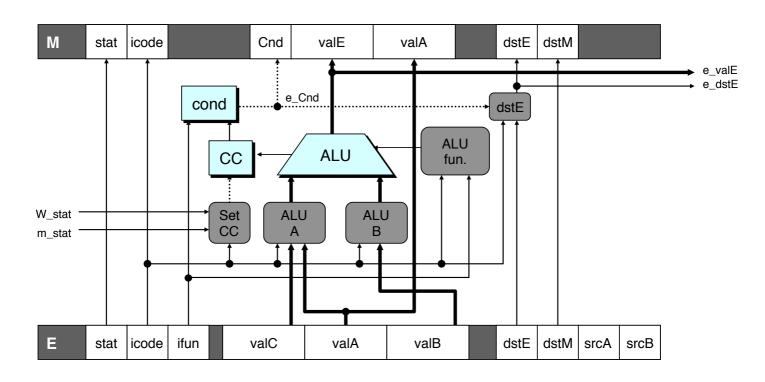
PIPE: PC selection and fetch logic



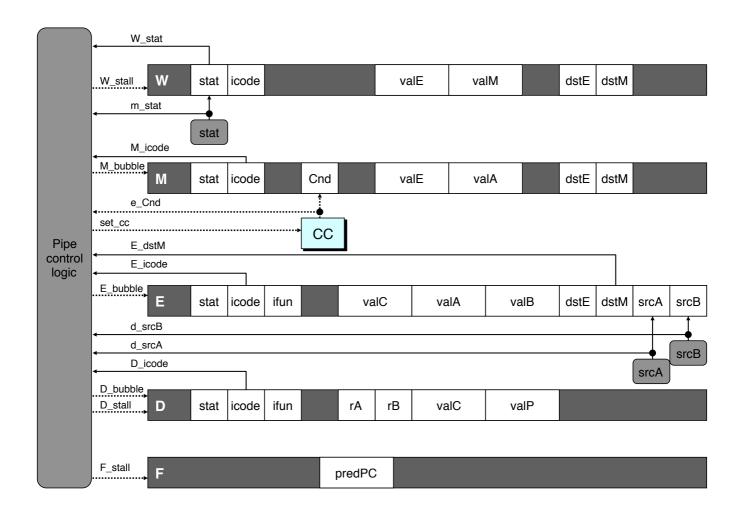
PIPE: decode and write-back stage logic



PIPE: memory stage logic



PIPE: execute stage logic



PIPE: pipeline control logic