REV	01

深圳市海量视界电子科技有限公司

SPECIFICATIONS

Model NO.	HL062CTIPS4lane
Customer	
TYPE	LCD MODULE，452(RGB) * 1280Pixels

■ **Preliminary Specification**

□ **Final Specification**

HLSJVision			**CUSTOMER**
PREPARED	**CHECKED**	**APPROVED**	**APPROVED**

RECORDS OF REVISION

REV.	DATE	Page	DESCRIPTION OF CHANGES
01	2025.3.24	All	FIRST ISSUE
02	2025.4.14	5	Update MECHANICAL DRAWING

CONTENT

1. GENERAL SPECIFICATION

1.1 Description

The HL062CTIPS4lane is a color active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD). This model is composed of a single 6.28 inches transmissive type main TFT-LCD panel. The resolution of the panel is 452 x1280 pixels and can display up to 16.7M color.

1.2 Feature

-Type for main TFT-LCD panel
-Structure COG+FPC+BL
-Full, Normal (Still), Partial, Sleep, Standby mode are available

1.3 Application

-Display terminals for cellular, industrial, medical or equivalent.

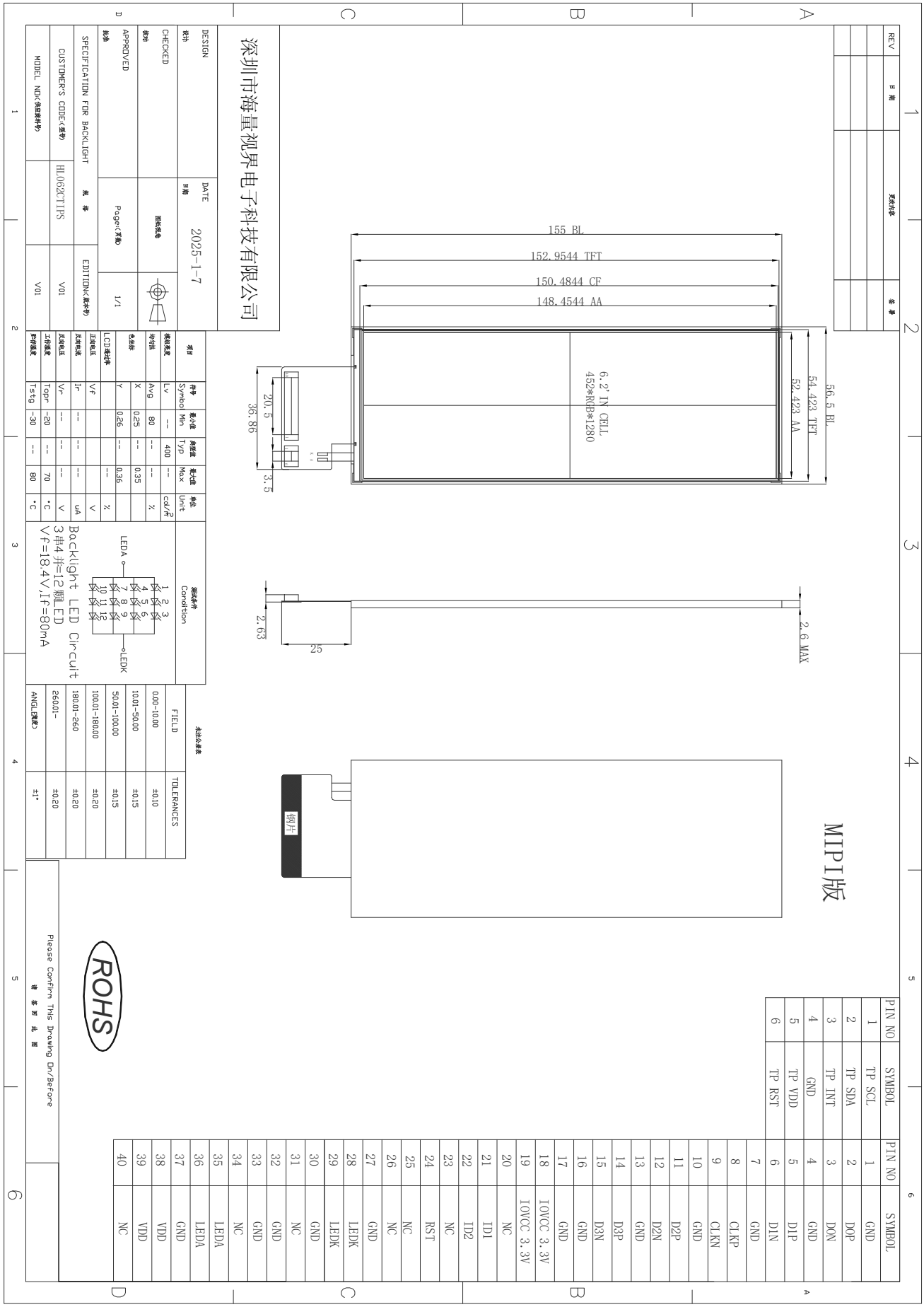
1.4 General Specification

Module:

No.	Item	Specification	Unit	Remark
1	LCD Size	6.2	inch	-
2	Panel Type	IPS	-	-
3	Resolution	452x (RGB) x 1280	pixel	-
4	Display Mode	Normally black	-	-
5	Display Number of Colors	16.7M	-	-
6	Viewing Direction	ALL	-	-
7	Contrast Ratio	1000	-	-
8	Luminance	400(TYP)	cd/m^2	Note
9	Module Size	56.5(W) x 155(H) x 2.6(T)	mm	Note
10	Active Area	52.423(W) x 148.454(H)		
11	Driver IC	AXS15260D	-	-
12	Driver IC RAM Size	RAMless	bit	-
13	Light Source	12LEDS,WHITE(18.4V,80mA)	-	-
14	Interface	MIPI-2/3/4lane	-	-
15	Operating Temperature	-20~70	℃	-
16	Storage Temperature	-30~80	℃	-

Note: Please refer to the mechanical drawing.

2.MECHANICAL DRAWING



PIN NO	SYMBOL
1	TP SCL
2	TP SDA
3	TP INT
4	GND
5	TP VDD
6	TP RST

PIN NO	SYMBOL
1	GND
2	D0P
3	D0N
4	GND
5	D1P
6	D1N
7	GND
8	CLKP
9	CLKN
10	GND
11	D2P
12	D2N
13	GND
14	D3P
15	D3N
16	GND
17	GND
18	IOVCC 3.3V
19	IOVCC 3.3V
20	NC
21	ID1
22	ID2
23	NC
24	RST
25	NC
26	NC
27	GND
28	LEDK
29	LEDK
30	GND
31	NC
32	GND
33	GND
34	NC
35	LEDA
36	LEDA
37	GND
38	VDD
39	VDD
40	NC

REV	日期	更改内容	备 考

DESIGN 设计		DATE 日期	2025-1-7
CHECKED 核对		图纸张数	
APPROVED 批准		Page(页数)	1/1
SPECIFICATION FOR BACKLIGHT 规 格		EDITION(版本号)	V01
CUSTOMER'S CODE(客号)	HL062CTIPS		
MODEL NO(客户型号)			V01

项目	符号 Symbol	最小值 Min	典型值 Typ	最大值 Max	单位 Unit
模组亮度	Lv	---	400	---	cd/㎡
均匀性	Avg	80	---	---	%
色坐标	X	0.25	---	0.35	
	Y	0.26	---	0.36	
LCD驱动IC					
正常电压	Vf			---	V
反向电流	Ir	---	---	---	uA
反向电压	Vr	---	---	---	V
工作温度	Topr	-20	---	70	°C
存储温度	Tstg	-30	---	80	°C

测试条件 Condition

Backlight LED Circuit
3串4并=12颗 LED
VF=18.4V,If=80mA

FIELD	TOLERANCES
0.00-10.00	±0.10
10.01-50.00	±0.15
50.01-100.00	±0.15
100.01-180.00	±0.20
180.01-260	±0.20
260.01-	±0.20
ANGLE(角度)	±1°

未注公差表

3.INTERFACE ASSIGNMENT

LCD PIN NO.	SYMBOL	FUNCTION DESCRIPTIONS
1	GND	Ground.
2	D0P	MIPI-DSI data Lane 0 positive-end input/output pin.
3	D0N	MIPI-DSI data Lane 0 negtive-end input/output pin.
4	GND	Ground.
5	D1P	MIPI-DSI data Lane 1 positive-end input pin.
6	D1N	MIPI-DSI data Lane 1 negtive-end input pin.
7	GND	Power supply for backlight (cathode).
8	CLKP	MIPI-DSI clock Lane positive-end input pin.
9	CLKN	MIPI-DSI clock Lane negative-end input pin.
10	GND	Ground.
11	D2P	MIPI-DSI data Lane 2 positive-end input pin.
12	D2N	MIPI-DSI data Lane 2 negtive-end input pin.
13	GND	Ground.
14	D3P	MIPI-DSI data Lane 3 positive-end input pin.
15	D3N	MIPI-DSI data Lane 3 negtive-end input pin.
16	GND	Ground.
17	GND	Ground.
18	IOVCC	Power supply to interface pins.
19	IOVCC	Power supply to interface pins.
20	NC	NC.
21	ID1	ID1 PIN.
22	ID2	ID2 PIN.
23	NC	NC.
24	RST	LCD reset pin.
25	NC	NC.
26	NC	NC.
27	GND	Ground.
28	LEDK	Power supply for backlight (cathode).
29	LEDK	Power supply for backlight (cathode).
30	GND	Ground.
31	NC	NC.
32	GND	Ground.

33	GND	Ground.
34	NC	NC.
35	LEDA	Power supply for backlight (anode).
36	LEDA	Power supply for backlight (anode).
37	GND	Ground.
38	VDD	Power Supply for Analog.
39	VDD	Power Supply for Analog.
40	NC	NC.

TP PIN NO.	SYMBOL	FUNCTION DESCRIPTIONS
1	TP_SCL	TP clock signal pin.
2	TP_SDA	TP serial data input pin.
3	TP_INT	External interrupt to the host for TP.
4	GND	Ground.
5	TP_VDD	Power Supply.
6	TP_RST	TP reset pin.

4. ELECTRICAL SPECIFICATION

4.1. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	VDD	Ta=25 ºC	-0.3	-	4.0	V
Power Supply for Digital IO	IOVCC	Ta=25 ºC	-0.3	-	4.0	V

Note: Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is applied.

4.2. TYPICAL OPERATION CONDITION

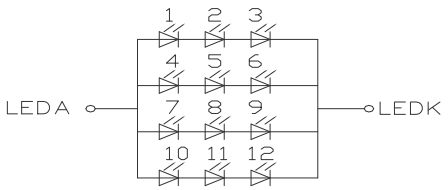
4.2.1 DC Characteristics

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	VDD	Ta=25 ºC	3.1	3.3	3.5	V
Power Supply for Digital IO	IOVCC	Ta=25 ºC	1.65	1.8	3.4	V
Input Signal “H” Level	VIH	-	0.7IOVCC	-	IOVCC	V
Input Signal “L” Level	VIL	-	0	-	0.3IOVCC	V
Output Signal “H” Level	VOH	IOH=-0.1mA	0.8IOVCC	-	IOVCC	V
Output Signal “L” Level	VOL	IOL=0.1mA	0	-	0.2IOVCC	V
Frame Frequency	fFRAME	-	\	60	\	Hz

Note: To prevent IC latch up or DC operation in LCD panel, the power on/off sequence should follow the driver IC specification.

4.3. BACKLIGHT SPECIFICATION

4.3.1 BACKLIGHT CIRCUIT

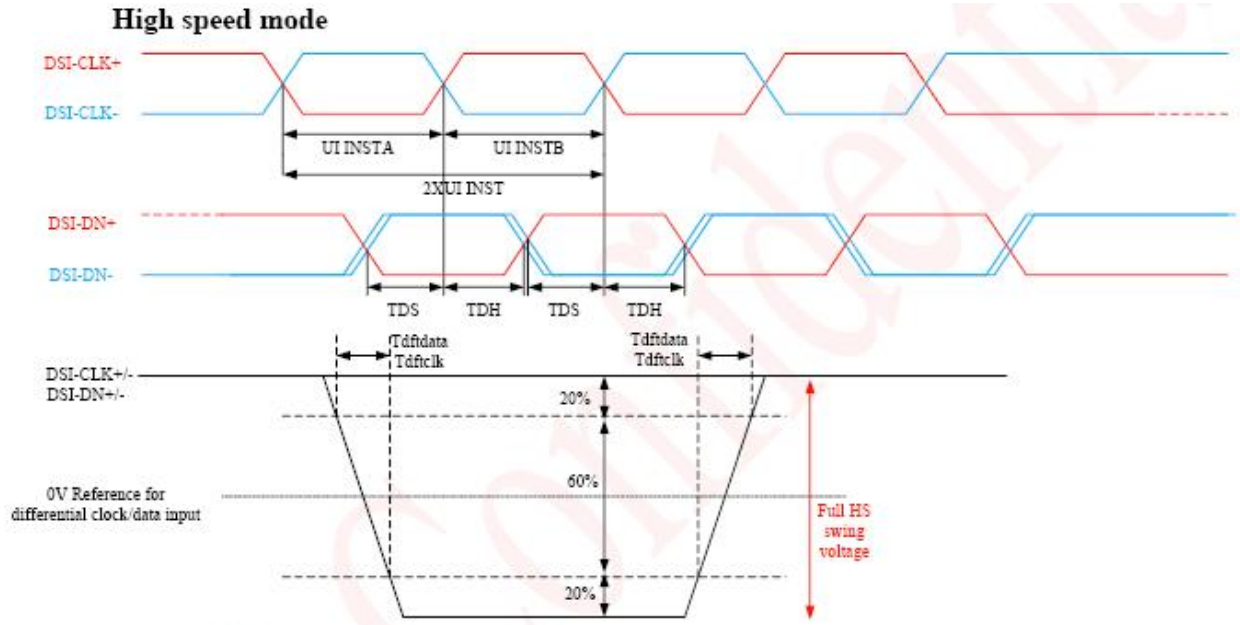


Backlight LED Circuit
3串4并=12颗LED
Vf=18.4V,If=80mA

4.3.2 ELECTRICAL CHARACTERISTICS (T=25℃)

PARAMETER	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
FORWARD VOLTAGE	VF	IF=80mA	\	18.4	\	V

4.4. INTERFACE TIMING CHARACTERISTICS



Parameter	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
DSI-CLK+/-	2xUI$_{INSTA}$	Double UI instantaneous	1.6		25	ns	
DSI-CLK+/-	UI$_{INSTA}$ UI$_{INSTB}$	UI instantaneous halfs	0.8		12.5	ns	UI=UI$_{INSTA}$=UI$_{INSTB}$
DSI-D0+/-	T$_{DS}$	Data to clock setup time	0.15	-		UI	
DSI-D0+/-	T$_{DH}$	Data to clock hold time	0.15	-		UI	

Figure: AC characteristics for MIPI-DSI High speed mode

Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP -11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP -11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T LPXD	-	2XT LPXD	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to driver LP-00 by display module	5XT LPXD	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to driver LP-00 after turnaround request - MPU	4XT LPXD	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

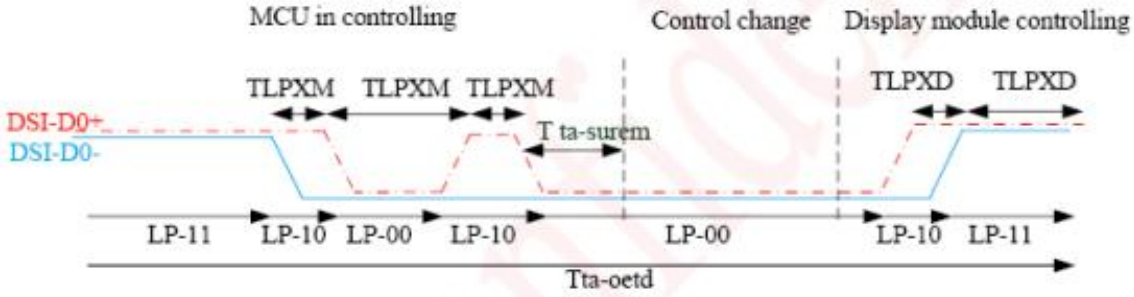


Figure: BTA from the MCU to the Display Module

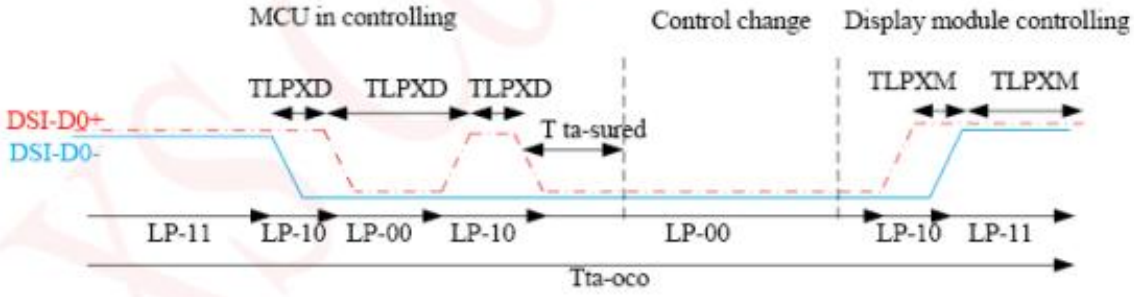


Figure: BTA from the Display Module to the MCU

Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to driver LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to driver HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to driver flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ Period to start of LP-11 state	-	-	105ns +12UI	ns

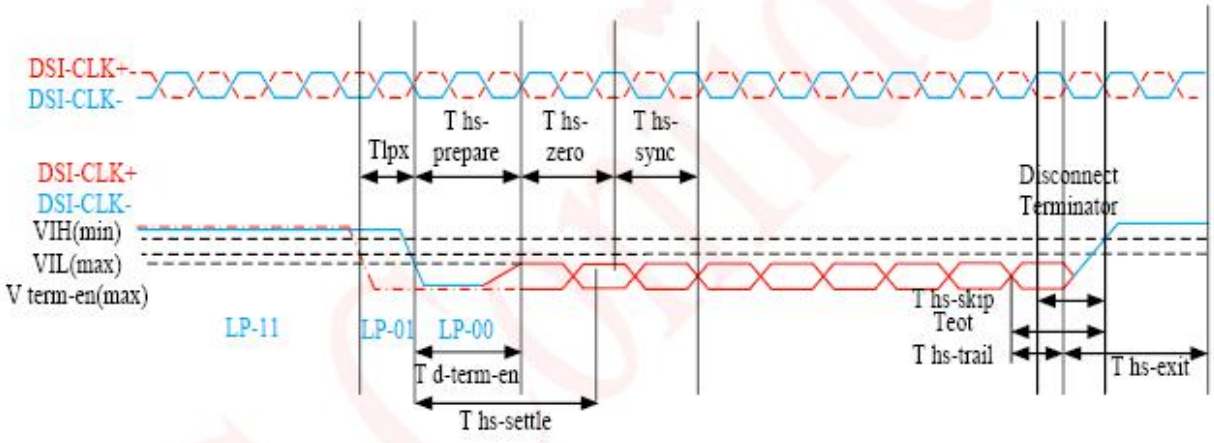
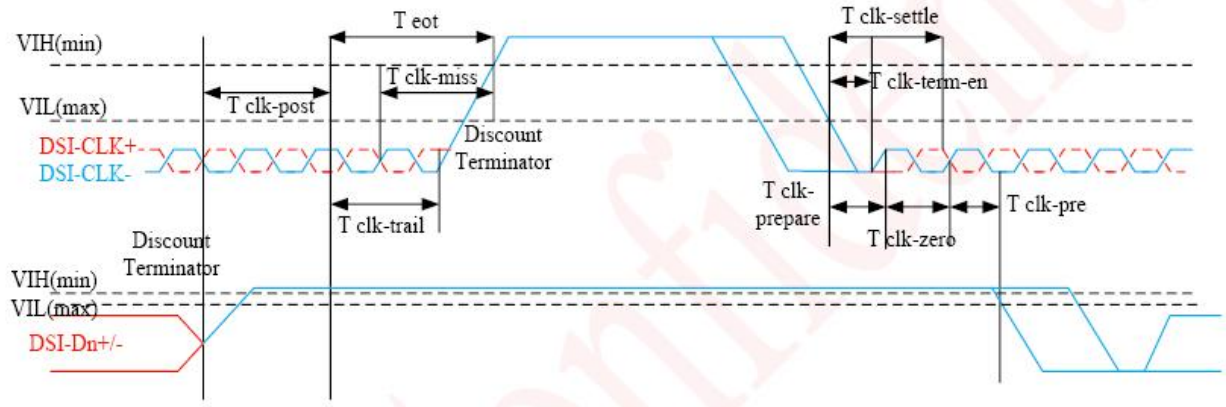


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lanehas transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be drivern prior to any associated Data Lanebeginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to driver LP-00 to prepare	38	-	95	ns
		for HS clock transmission				
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$+ time for lead HS-0 driver period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to driver HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ periodto start of LP-11 state	-	-	105ns + 12UI	ns



LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when

different combinations, what are listed below, are possible:

1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

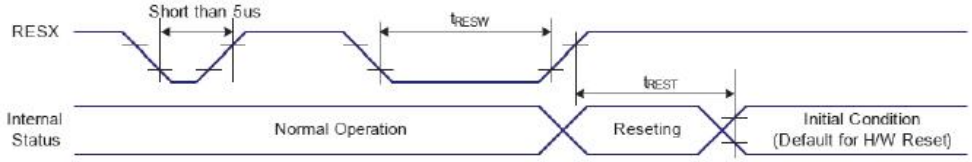
1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+52UI	-	60ns+52UI	-	60ns+52UI	-
BTA	100ns	-	100ns	-	100ns	-

4.5 RESET TIMING CHARACTERISTICS

4.5.1 LCD reset timing



Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	us
tREST	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

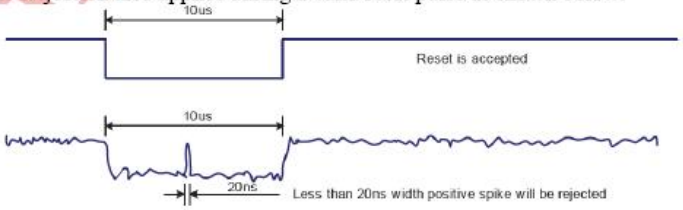
Note 1:Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2:During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3:During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

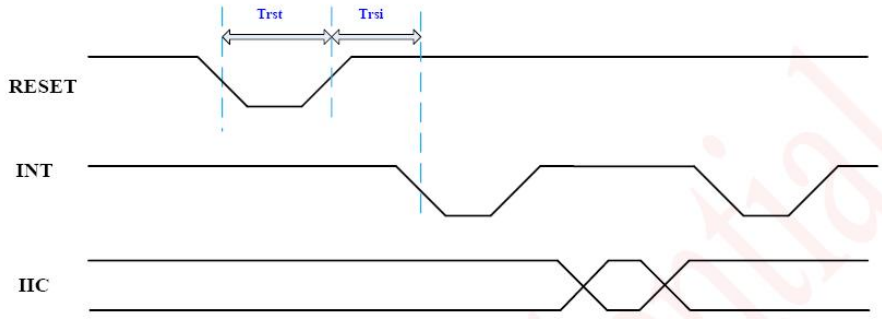
Note 4:Spike Rejection also applies during a valid reset pulse as shown below:



Note 5:It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

4.5.2 TP reset timing

Reset time must be enough to guarantee reliable reset.



Parameter	Description	Min	Max	Units
Trsi	Time of starting to report point after resetting	200	--	ms
Trst	Reset time	5	--	ms

5. OPTICAL CHARACTERISTICS

(T_a=+25ºC, VDD=3.3V, , IOVCC=+1.8V, I_B=80mA)

Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing Angle Range	Left	θ_L	CR≧10	-	85	-	degree	Note 1,2
	Right	θ_R		-	85	-		
	Top	Φ_T		-	85	-		
	Botto	Φ_B		-	85	-		
Response Time		T_{on} +T_{off}	Normal θ=Φ=0˚	-	30	-	ms	Note 2,3
Contrast Ratio		CR	Normal θ=Φ=0˚	-	1000	-	-	Note 2,4
Luminance		L	Normal θ=Φ=0˚	-	400	-	cd/m^2	Note 2,5
Color Chromaticity (CIE1931)	White	Wx	Normal θ=Φ=0˚	-	0.303	-	-	Note 2,6
		Wy		-	0.337	-		
	Red	Rx		-	0.632	-		
		Ry		-	0.335	-		
	Green	Gx		-	0.289	-		
		Gy		-	0.588	-		
	Blue	Bx		-	0.138	-		
		By		-	0.147	-		
Color Gamut		NTSC	CIE1931	-	60	-	%	-

Note 1: Definition of viewing angle range

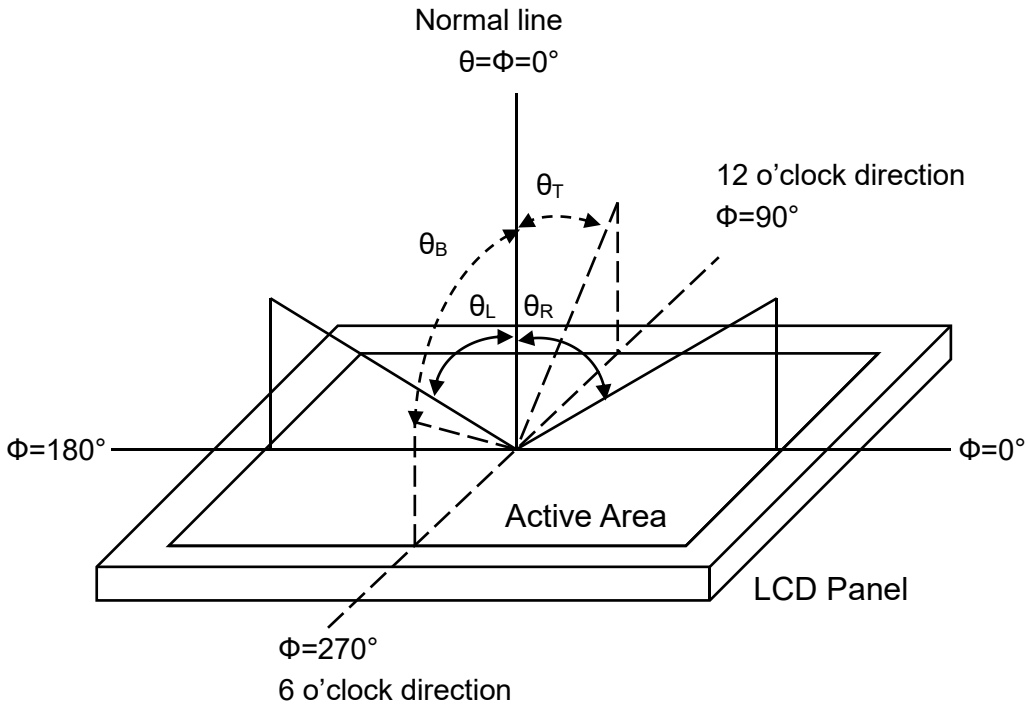


Fig. 1 Definition of viewing angle

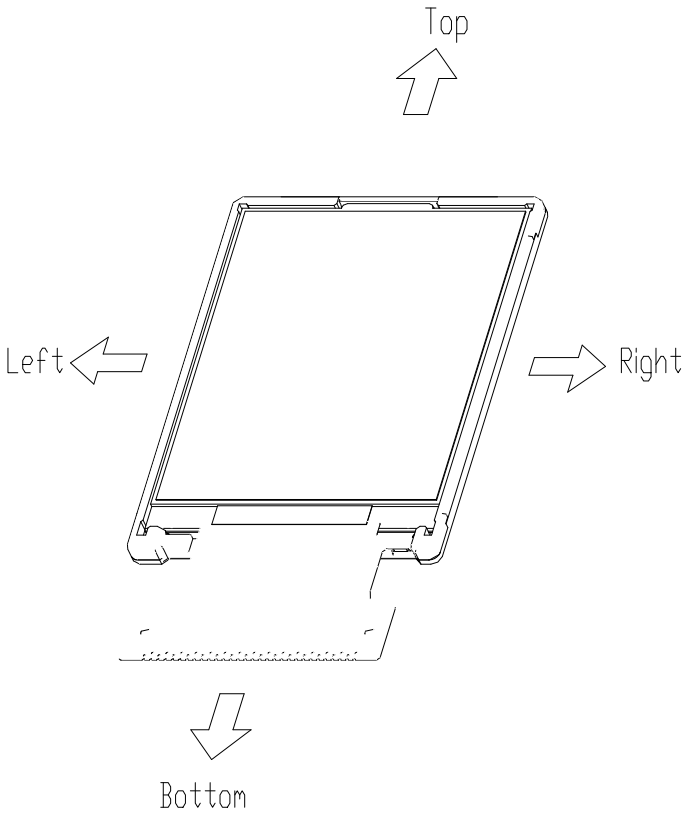


Fig. 2 Definition of viewing angle for display

Note 2: Definition of optical measurement system

The optical characteristics should be measured in a dark room with ambient temperature T_a=+25℃. The optical properties are measured at the center point of the LCD screen after 5 minutes operation. (Equipment: Photo detector TOPCON BM-5AS Field of view: 1°/Height: 500mm.)

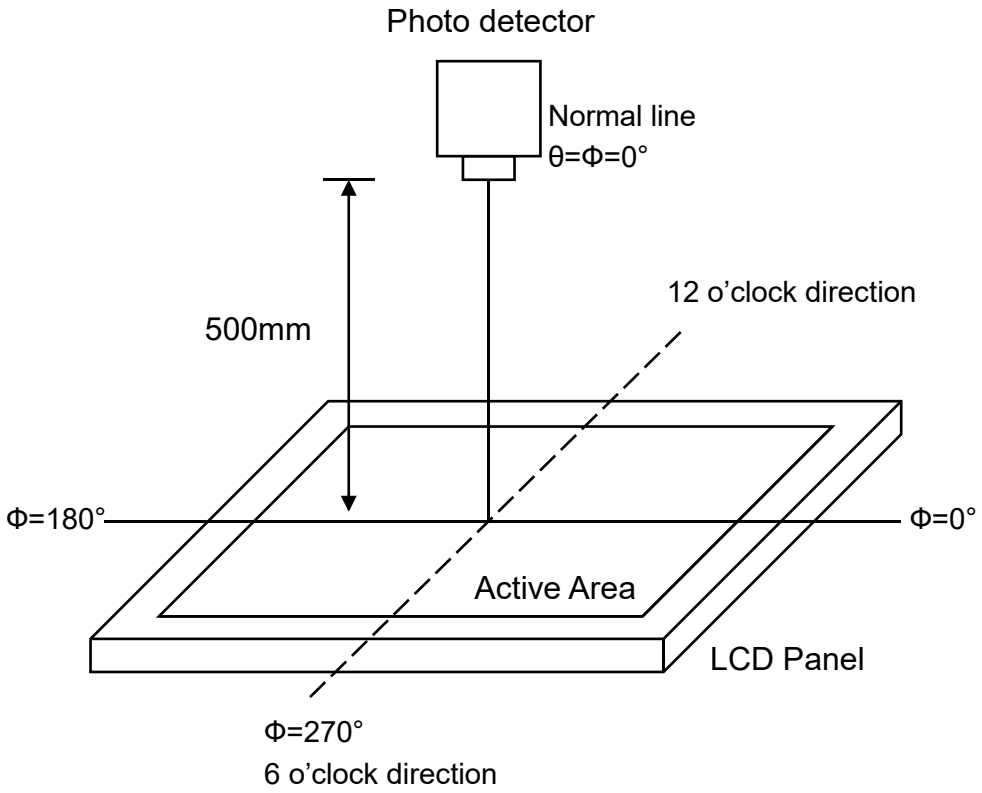


Fig. 3 Optical measurement system setup

Note 3: Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{on}) is the time between photo detector output intensity changed from 90% to 10%, and fall time (T_{off}) is the time between photo detector output intensity changed from 10% to 90%.

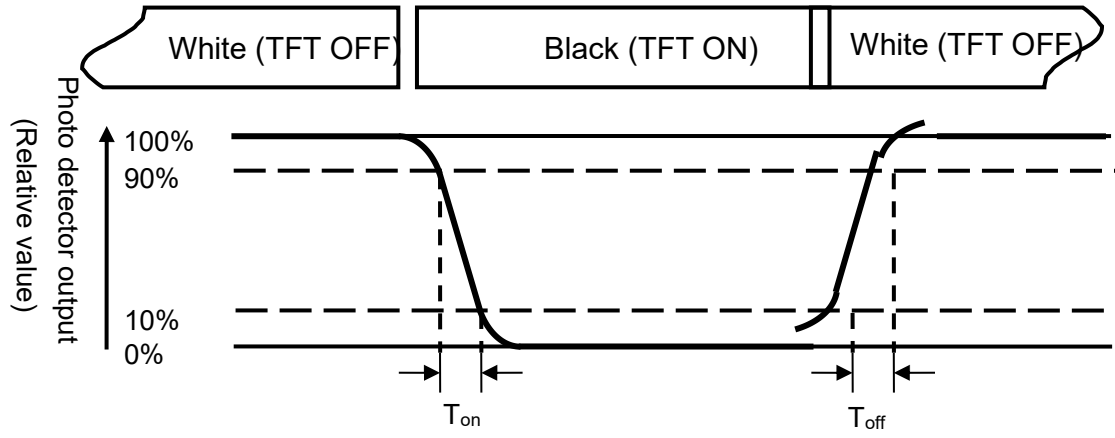


Fig. 4 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of luminance

Measured at the center area of the panel when LCD panel is driven at “white” state.

Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD when panel is driven at “White”, “Red”, “Green” and “Blue” state respectively.

Note 7: Definition of luminance uniformity

To test for uniformity, the tested area is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each circle as below.

$$\text{Luminance Uniformity } (U_L) = \frac{L_{min}}{L_{max}}$$

L-------Active area length W----- Active area width

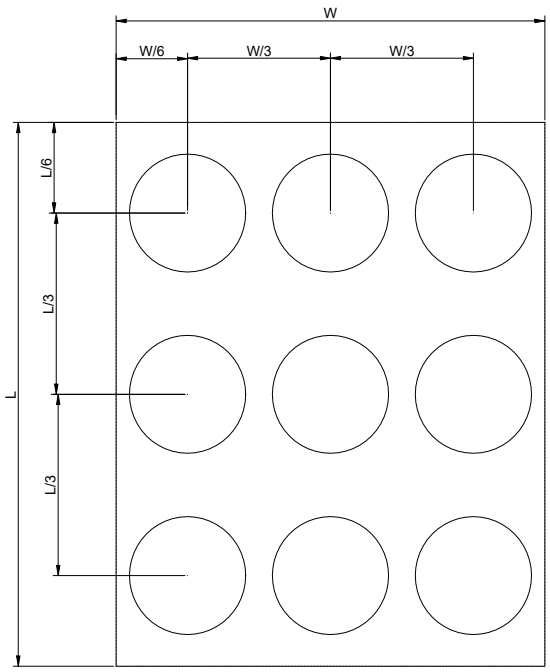


Fig. 5 Definition of luminance uniformity

L_{min} : The measured minimum luminance of all measurement position.

L_{max} : The measured maximum luminance of all measurement position.

6. PRECAUTIONS

6.1. HANDLING

6.1.1. Polarizer Cleaning, Petroleum ether (or N-hexane) is recommended for cleaning the front/rear polarizers and reflectors, acetone, toluene and ethanol are not allowed to avoid damaging the surface.

7.1.2. Body grounding, must wear Anti-ESD wrist strap while pick up LCDs.

7.1.3. FPC Soldering, less than 300℃/3S, solder must be grounding on grounding bench.

7.1.4. If use electric Screwdriver to do assembly, screwdriver must be grounding.

6.2. STORAGE

7.2.1. Keep in a sealed polyethylene bag.

7.2.2. Keep in a dark place.

7.2.3. Keep in temperature between 0°C and 35°C.

6.3. SAFETY

If liquid crystal leak out of a damaged glass cell, **DO NOT** put it in your mouth or touch eyes, if the liquid crystal touch your skin or clothes, please wash it off immediately using soap and water.

7. LIMITED WARRANTY

Unless otherwise agreed between Jingshengand customer, Jingsheng will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with JingshengLCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects over specs must be returned to Jingshengwithin 30 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of Jingshenglimited to repair and/or replacement on the terms set forth above. Jingshengshall not be responsible for any subsequent or consequential events.

7.1. RETURNING LCM UNDER WARRANTY – TERMS AND CONDITIONS

7.1.1. No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- Circuit modified in any way, including addition of components.

7.1.2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB’s eyelet, conductors and terminals.