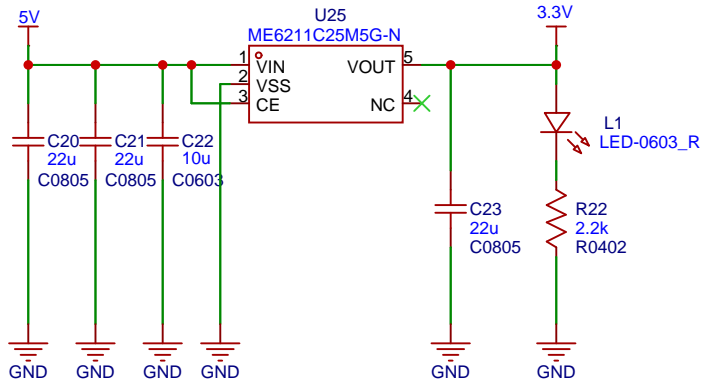


U34		U35	
1	GND	1	GND
2	N.C.	2	N.C.
3	N.C.	3	N.C.
4	N.C.	4	N.C.
5	VSA	5	VSA
6	OUT2	6	OUT2
7	N.C.	7	N.C.
8	VCP	8	VCP
9	H2	9	H2
10	H3	10	H3
11	H1	11	H1
12	DIAG	12	DIAG
13	SENSEA	13	SENSEA
14	RCOFF	14	RCPULSE
15	N.C.	15	N.C.
16	OUT1	16	OUT1
17	N.C.	17	N.C.
18	GND	18	GND
19	GND	19	GND
20	GND	20	GND
21	GND	21	GND
22	GND	22	GND
23	GND	23	GND
24	GND	24	GND
25	GND	25	GND
26	GND	26	GND
27	GND	27	GND
28	GND	28	GND
29	GND	29	GND
30	GND	30	GND
31	GND	31	GND
32	GND	32	GND
33	GND	33	GND
34	GND	34	GND
35	GND	35	GND
36	GND	36	GND
37	GND	37	GND

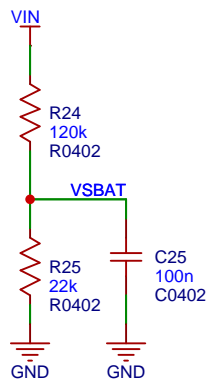
Schematic	UsingHalfBridgeController		Update Date	2025-01-26
			Create Date	2024-12-06
Page	Power		Part Number	JLCPCB-002
Drawn	EasyEDA	BLDC Driver_2025		
Reviewed	EasyEDA			
		VER	SIZE	PAGE 1 OF 3
EasyEDA		V0.1	A3	iOsnaaente

Regulador de tensão - LDO SOT89-3

Vin: 5V-18V Vout: 3.3V



Medição de VBat



Push buttons

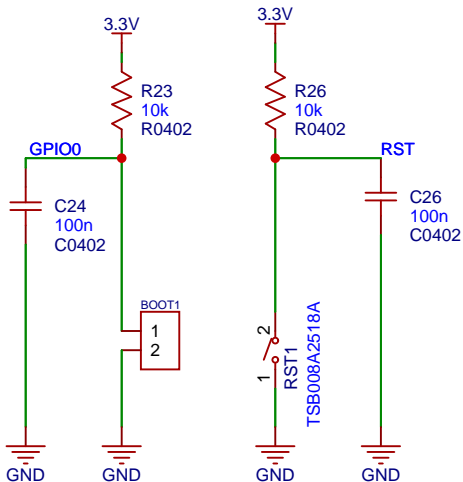


Table 2-11. Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
Default Configuration	1 (Pull-up)	0 (Pull-down)
SPI Boot (default)	1	Any value
Joint Download Boot ¹	0	0

¹ Joint Download Boot mode supports the following download methods:

- USB Download Boot:
 - USB-Serial-JTAG Download Boot
 - USB-OTG Download Boot
- UART Download Boot

2.6 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, voltage of flash memory, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins operate as regular IO pins.

The parameters controlled by the given strapping pins at chip reset are as follows:

- **Chip boot mode** – GPIO0 and GPIO46
- **VDD_SPI voltage** – GPIO45
- **ROM messages printing** – GPIO46
- **JTAG signal source** – GPIO3

GPIO0, GPIO45, and GPIO46 are connected to the chip's internal weak pull-up/pull-down resistors at chip reset. These resistors determine the default bit values of the strapping pins. Also, these resistors determine the bit values if the strapping pins are connected to an external high-impedance circuit.

Table 2-9. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Pull-up	1
GPIO3	Floating	–
GPIO45	Pull-down	0
GPIO46	Pull-down	0

Antena

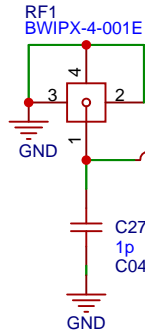
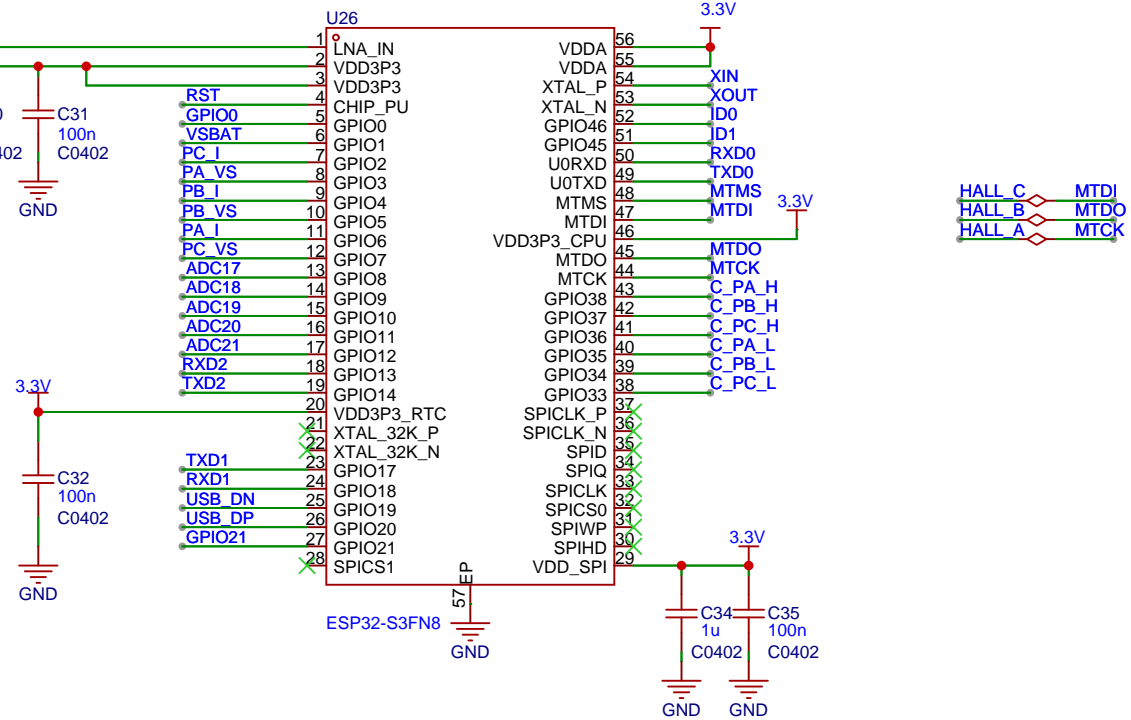


Table 39-6. SAR ADC Input Signals

Pin/Signal	Channel	ADC Selection
GPIO1	0	SAR ADC1
GPIO2	1	
GPIO3	2	
GPIO4	3	
GPIO5	4	
GPIO6	5	
GPIO7	6	
GPIO8	7	
GPIO9	8	
GPIO10	9	SAR ADC2
GPIO11	0	
GPIO12	1	
GPIO13	2	
GPIO14	3	
GPIO15	4	
GPIO16	5	
GPIO17	6	
GPIO18	7	
GPIO19	8	
GPIO20	9	
Internal voltage	n/a	

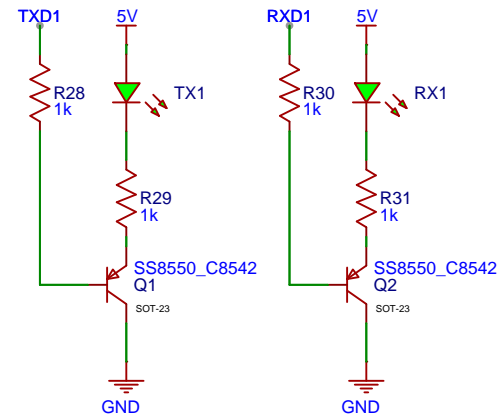
ESP32 S3



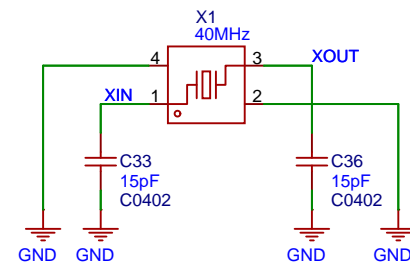
Leds ESP





Leds UART



Clock 40MHz



Schematic	UsingHalfBridgeController			Update Date	2024-12-16
				Create Date	2024-12-07
Page	Microcontroller			Part Number	JLPCPB-002
Drawn	EasyEDA	BLDC Driver_2025			
Reviewed	EasyEDA				
		VER	SIZE	PAGE	2 OF 3
		V0.1	A3	iOsnaaente	

Schematic	UsingHalfBridgeController			Update Date	2024-12-16	
				Create Date	2024-12-07	
Page	Connectors			Part Number	JLPCB-002	
Drawn	EasyEDA	BLDC Driver_2025				
Reviewed	EasyEDA					
		VER	SIZE	PAGE	3	OF 3
		V0.1	A3	iOsnaaente		