Prelab 2.
Please answer the following questions and hand in as your prelab for Lab 2.

1. What is the purpose of the NVIC peripheral?
   - 32 maskable interrupt channels (not including the sixteen Cortex®-M0 interrupt lines)
   - 4 programmable priority levels (2 bits of interrupt priority are used)
   - Low-latency exception and interrupt handling
   - Power management control
   - Implementation of System control registers
2. What is the difference between interrupt tail-chaining and nesting?

   Tail-chaining means that if there are multiple interrupts they will execute one right after the other and don't interrupt each other. Nesting interrupts give higher priority interrupts the opportunity to interrupt the lower priority interrupts.
3. In what file are the CMSIS libraries that control the NVIC?

   core_cm0.h
4. What is the purpose of the EXTI peripheral?
   - The extended interrupts and events controller (EXTI) manages the external and internal asynchronous events/interrupts and generates the event request to the CPU/Interrupt controller and a wake-up request to the Power manager.
   - It allows non-peripheral sources to trigger interrupts. While its typical use is to generate interrupts from the GPIO pins of the device, it may also monitor various internal signals such as the brownout protection circuitry (low-voltage shutdown).
5. What is the purpose of the SYSCFG pin multiplexers?
   - This register is used for specific configurations of memory and DMA requests remap and to control special I/O features
6. What file has the defined names for interrupt numbers?
   - stm32f072xb.h
7. What file has the Vector table implementation?
   - startup_stm32f072xb.s