2.2 — Postlab 2. Please answer the following questions and hand in as your postlab for Lab 2.

1. Why can’t you use both pins PA0 and PC0 for external interrupts at the same time?
   Because they are on the same multiplexor
2. What software priority level gives the highest priority? What level gives the lowest?
   Highest Priority = 0 Lowest Priority = 3
3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?
   Four 8-bit regions to set the priority of an interrupt. STM32F0 only has the uppermost two bits from these regions implemented.
4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.
   About 1.7 seconds
5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?
   If we do not clear the flags the interrupt will repeat continuously because the request never acknowledges as complete.

Submit your answers and any code files that you changed to the Lab 2 assignment.