



COMPUTER ORGANIZATION AND ARCHITECTURE

PROJECT CCCS217
SECTION [I1]

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PART 1: DIRECT MAPPING

RANEEM SAAD ALOMARI

A :

SET THE SIZE OF CACHE SO THAT DIRECT MAPPING HAS THE MAXIMUM HIT RATIO AND MINIMUM MISS RATIO?

AT CACHE SIZE 8 AND MEMORY SIZE 16 , WE REACH MAXIMUM HIT WITH %51 AND MINIMUM MISS %49.

B :

HOW CAN YOU INCREASE THE HIT RATIO IN CASE OF DIRECT MAPPING BY CHANGING SOME OF SIZE OF CACHES?

IT INCREASED AS THE SIZE OF THE CACHE CLOSED AS POSSIBLE TO THE MEMORY SIZE.

C:

SHOW THE PICTURES FROM THE SIMULATOR CONTAINING THE VALUES USED AND RESULTS OBTAINED. ALSO, GIVE REASONS WHY THE HIT RATIO INCREASES WHEN YOU CHANGE THE SIZE OF CACHES?



BECAUSE THE HIT/MISS RATIO IS DIRECTLY DEPENDENT ON THE CACHE SIZE IN OTHER WORDS IF THE CACHE SIZE IS CLOSE TO MEMORY SIZE THAT DECREASES THE NUMBER OF BLOCK OUT OF CACHE AND REQUIRES TO BE REPLACED WITH THE ONE IN THE CACHE THAT DEPENDENCY INCREASE THE HIT RATIO.

D:

EXPLAIN THE REASON FOR THE NUMBER OF BITS BEING USED FOR TAG AND FOR THE NUMBER OF BITS REQUIRED FOR RAM ADDRESS?

THE BIT USED IN THE TAG IS TO CLARIFY HIT OR MISS WHILE THE BITS REQUIRED TO RAM ADDRESS IS TO SPECIFY THE LOCATION OF THE DATA TO BE STORED.



PART 2: FULLY ASSOCIATIVE MAPPING

BEDOOR AYAD ALSULAMI

A :

SET THE SIZE OF CACHE SO THAT FULLY ASSOCIATIVE MAPPING HAS THE MAXIMUM HIT RATIO AND MINIMUM MISS RATIO?

THE MEMORY SIZE = 8

THE CACHE SIZE = 7

THE MAXIMUM HIT WAS 87% AND THE MINIMUM MISS WAS 13%.

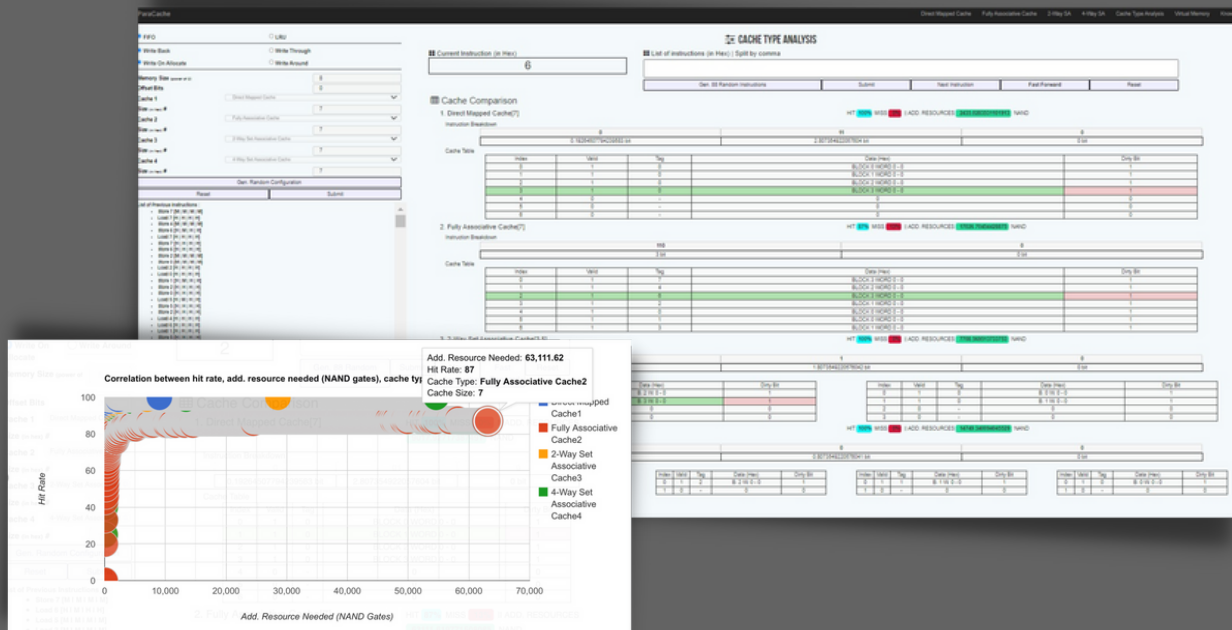
B :

HOW CAN YOU INCREASE THE HIT RATIO IN CASE OF FULLY ASSOCIATIVE MAPPING BY CHANGING SOME OF SIZE OF CACHES?

BY MAKING THE CACHE SIZE CLOSE TO MEMORY SIZE.

C:

SHOW THE PICTURES FROM THE SIMULATOR CONTAINING THE VALUES USED AND RESULTS OBTAINED. ALSO, GIVE REASONS WHY THE HIT RATIO INCREASES WHEN YOU CHANGE THE SIZE OF CACHES?



AS SHOWS INCREASING INTEREST AS THE HITS RATE INCREASES AS LONG AS THE CACHE SIZE IS INCREASING.

D:

EXPLAIN THE REASON FOR THE NUMBER OF BITS BEING USED FOR TAG AND FOR THE NUMBER OF BITS REQUIRED FOR RAM ADDRESS?

THE TAG STORED THE ADDRESS BITS WITH EACH LINE AND IT IS USED TO DECIDE WHETHER THE ADDRESS CURRENTLY BEING REQUESTED BY THE CPU IS BEING HELD IN THAT LINE OF THE CACHE, THE NUMBER OF BITS REQUIRED FOR THE RAM ADDRESS IS CALLED THE PHYSICAL ADDRESS WHICH IS A CODE. THE CPU (OR OTHER DEVICE) CAN USE THE CODE TO ACCESS THE CORRESPONDING MEMORY LOCATION.



PART 3: 4-WAY ASSOCIATIVE MAPPING

LAYAL SOUD HALWANI

A :

SET THE SIZE OF CACHE SO THAT 4-WAY ASSOCIATIVE MAPPING HAS THE MAXIMUM HIT RATIO AND MINIMUM MISS RATIO?

MEMORY SIZE = 4 , CACHE SIZE = 8
HIT RATIO 98% , MISS RATIO 2%
CACHE SIZE = 2 (ONE CACHE SIZE) * 4

B :

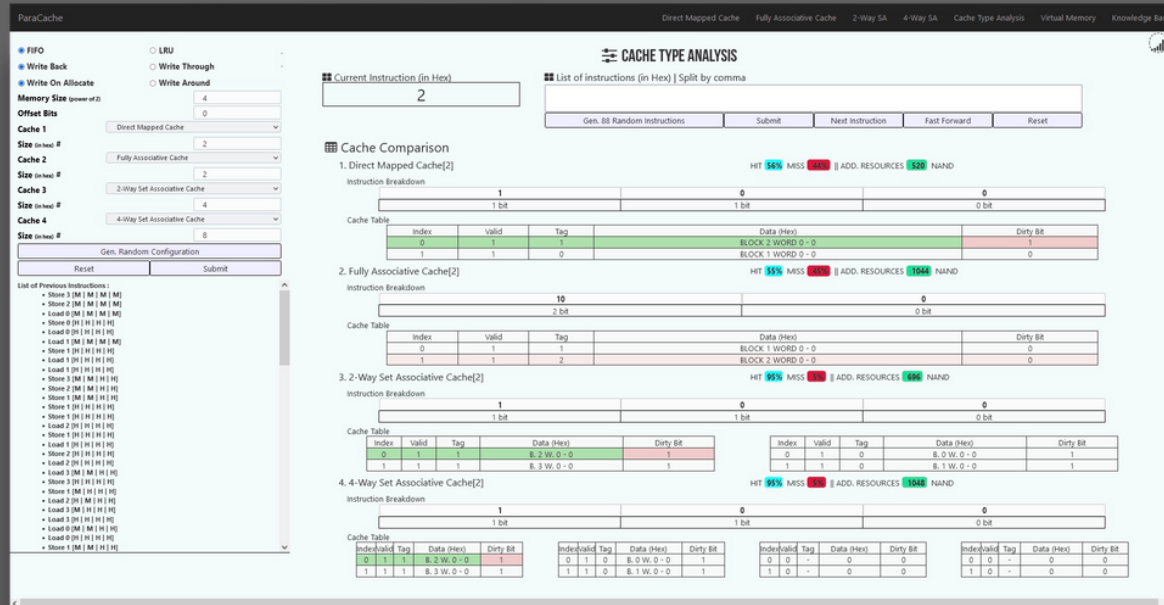
HOW CAN YOU INCREASE THE HIT RATIO IN CASE OF 4-WAY ASSOCIATIVE MAPPING BY CHANGING SOME OF SIZE OF CACHES?

WHEN THE CACHE SIZE IS CLOSER TO THE MEMORY SIZE THE HIT RATIO WILL BE INCREASED.

POSITIVE CORRELATION BETWEEN SIZE CACHE AND HIT RATIO, WHEN YOU INCREASE THE CACHE SIZE THE HIT RATIO WILL INCREASE.

C:

SHOW THE PICTURES FROM THE SIMULATOR CONTAINING THE VALUES USED AND RESULTS OBTAINED. ALSO, GIVE REASONS WHY THE HIT RATIO INCREASES WHEN YOU CHANGE THE SIZE OF CACHES?



THE HIT RATIO IS A CALCULATION OF CACHE HITS. THE RATE OF RECEIVED INFORMATION MATCHED THE INFORMATION IN THE CACHE.

INCREASING THE SIZE OF THE CACHE SHOULD ALLOW MORE INFORMATION TO BE STORED IN THE CACHE MEMORY.

WE CAN FIND MORE INFORMATION IN THE CACHE WHEN WE INCREASE THE CACHE SIZE, SO THE HIT RATIO WILL INCREASE.

D:

EXPLAIN THE REASON FOR THE NUMBER OF BITS BEING USED FOR TAG AND FOR THE NUMBER OF BITS REQUIRED FOR RAM ADDRESS?

- THE TAG IS HELPING US TO KNOW IF THE ADDRESS IS IN THE CACHE OR NOT. BY COMPARISON BETWEEN THE CACHE INDEX AND THE TAG. IF THE CACHE INDEX IDENTICAL WITH THE TAG , THAN THE ADDRESS IN THE CACHE (HIT). ELSE, (MISS) THE ADDRESS IN THE MAIN MEMORY (RAM).
- THE NUMBER OF BITS FOR RAM IS THE " **PHYSICAL ADDRESS** " , THAT WE NEED TO DETERMINE THE NUMBER OF BITS IN THE ADDRESS AND DISTRIBUTE IT TO 3 PARTS IN THIS WAY:
IN 4-WAY ASSOCIATIVE MAPPING : [TAG , SET , WORD] .