Name of Department:- Computer Science and Engineering

1. Subject Code: TCS 704 Course Title: **Advanced Computer Architecture**
2. Contact Hours: L: 3 T: - P: -
3. Semester: VII

4. Pre-requisite: TCS 404

5. Course Outcomes: After completion of the course students will be able to

1. Discuss the classes of computers, and new trends and developments in computer architecture
2. Study advanced performance enhancement techniques such as pipelines ,dynamic scheduling branch predictions, caches
3. Compare and contrast the modern computer architectures such as RISC, Scalar, and multi CPU systems
4. Critically evaluate the performance of different CPU architecture
5. Improve the performance of applications running on different cpu architectures.
6. Develop applications for high performance computing systems

6. Detailed Syllabus

UNIT	CONTENTS	Contact Hrs
Unit - I	Fundamentals: Computer Architecture and Technology Trends, Moore's Law, Classes of Parallelism and Parallel Architectures, Instruction Set Architecture: The Myopic View of Computer Architecture, Trends in Technology, Trends in Cost, Processor Speed, Cost, Power, Power Consumption, Fabrication Yield Performance Metrics and Evaluation: Measuring Performance, Benchmark Standards, Iron Law of Performance, Amdahl's Law, Lhadma's Law	**10**
Unit - II	Memory Hierarchy Design: Basics of Memory Hierarchy, Coherence and locality properties, Cache memory organizations, Cache Performance, Cache optimization techniques, Virtual Memory, Techniques for Fast Address Translation	**9**
Unit – III	Pipelining: What is pipelining, Basics of a RISC ISA, The classic five-stage pipeline for a RISC processor, Performance issues in pipelining, Pipeline Hazards	**10**
Unit – IV	Branches and Prediction: Branch Prediction, Direction Predictor, Hierarchical Predictors, If Conversion, Conditional Move Instruction Level Parallelism: Introduction, RAW and WAW, dependencies, Duplicating Register Values, ILP	**8**
Unit – V	Multiprocessor architecture: taxonomy of parallel architectures. Centralized shared-memory, Distributed shared-memory architecture, Message passing vs Shared Memory	**9**
	Total	**46**

Text/ Reference Books

1. John L. Hennessy, David A. Patterson, **"Computer Architecture:** A Quantitative Approach" 5th edition, Morgan Kaufmann
2. **"**by Kai Hwang **,"Advanced Computer Architecture"**, McGraw Hill Publishing