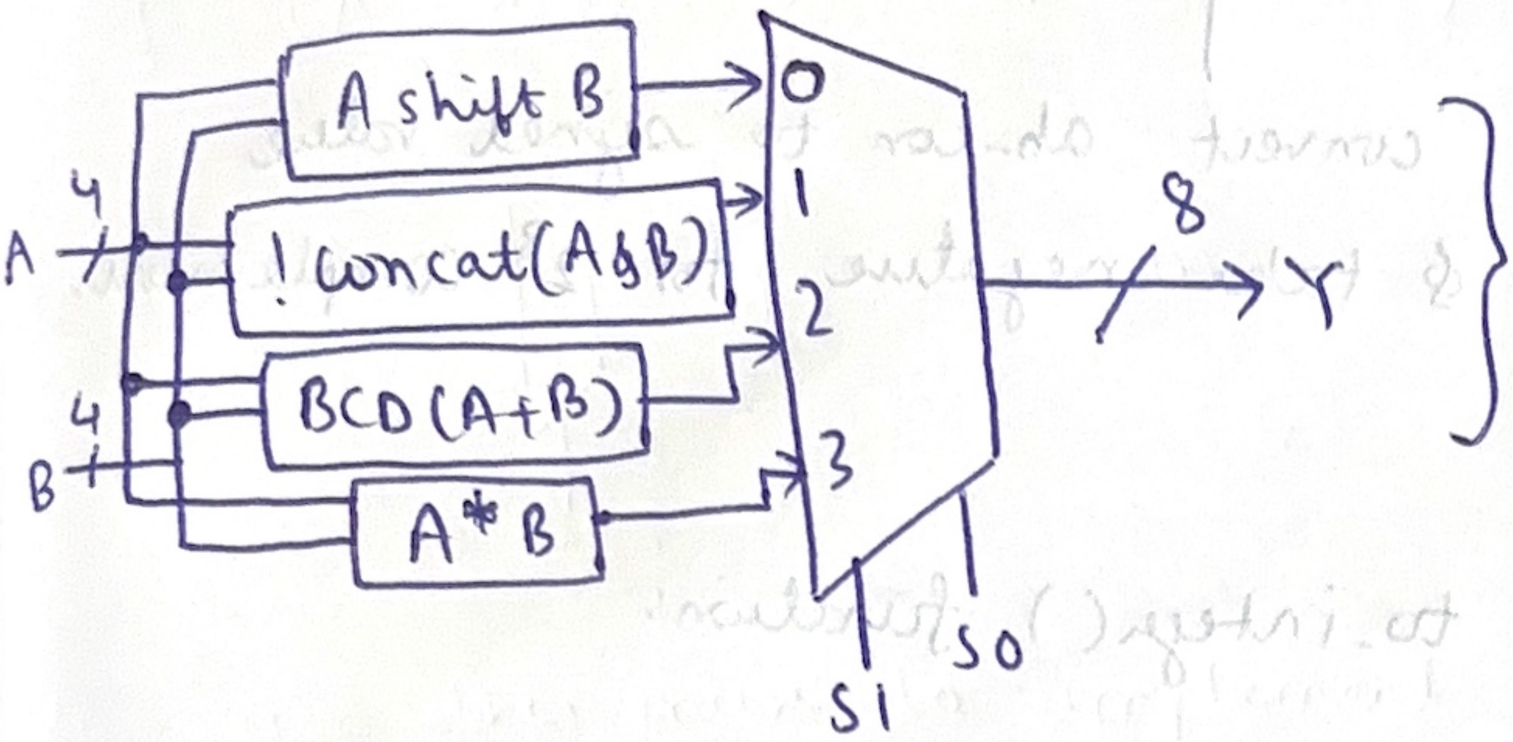
Problem - Lab 5 : 11/9/2025:

ALU:

The alu to be coded is given by:



we use behavioural modelling to implement this ALU.

i) Shift function:

The shift function takes in A, B as 2 std_logic_vectors of length 4 and returns a single logic vector. Hence the function definition header is:

→ function Shift(A, B : Std_logic_vector (3 down to 0)) return Std_logic_vector is

We then make a temporary A_extended variable that stretches A to 8 bits, ready to be shifted: The shift amount is first 3 bits of B:

→ variable shift_amount : integer := to_integer(unsigned B(2 downto 0)));

We write 2 if conditions: If B(3) = '0' then left shift and if B(3) = '1' we right shift the string. We store outcome in result vector:

→ if B(3) = '0' then
result = Std_logic_vector (shift_left (unsigned (A_extended), shift_amount)
elsif
B(3) = '1' then
result = std_logic_vector (shift_right (unsigned (A_extended), shift_amount)

ii) concatenate: we use inbuilt library functions.

ab_con = A & B;

Y <= std_logic_vector(-signed(ab_con))

↑ convert ab_con to signed value & take negative for 2's complement.

iii) BCD(A+B) value:

we calculate sum by to_integer() function:

sum := to_integer(unsigned(A)) + to_integer(unsigned(B));

ones_value := to_unsigned(sum mod 10, 4)

↑ take ones digit value

↳ 4 bit value stored

tens_value = to_unsigned(sum/10, 4)

↑ tens value ~~stored~~ calculated

↳ 4 bit value stored

Y <= std_logic_vector(tens_value & ones_value)

iv) Multiplication A*B:

Logic is that we go one by one through bits of B. If bit is 0 we ignore, but if it is 1 we shift A by that bit place index and add to product.

for i in 0 to 3 loop

if temp_B(i) = '1' then

prod := prod + shift_left(temp_A, i)

end if

end loop

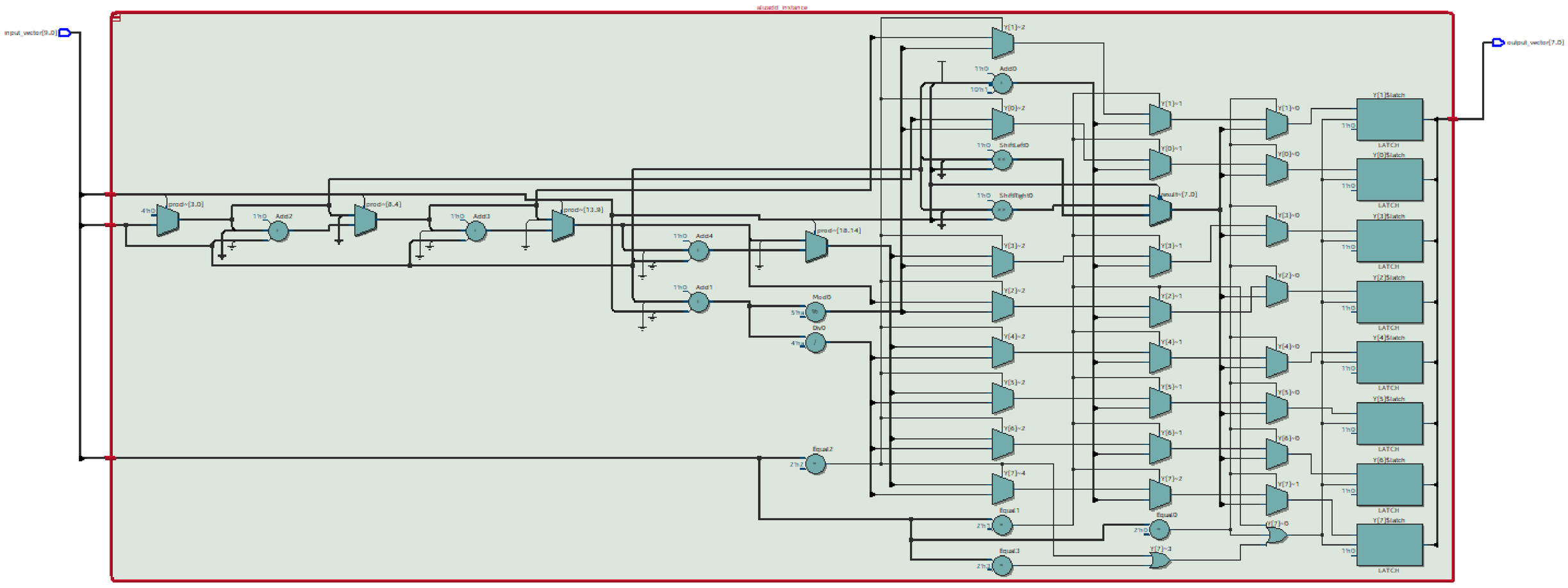
Y <= std_logic_vector(prod)

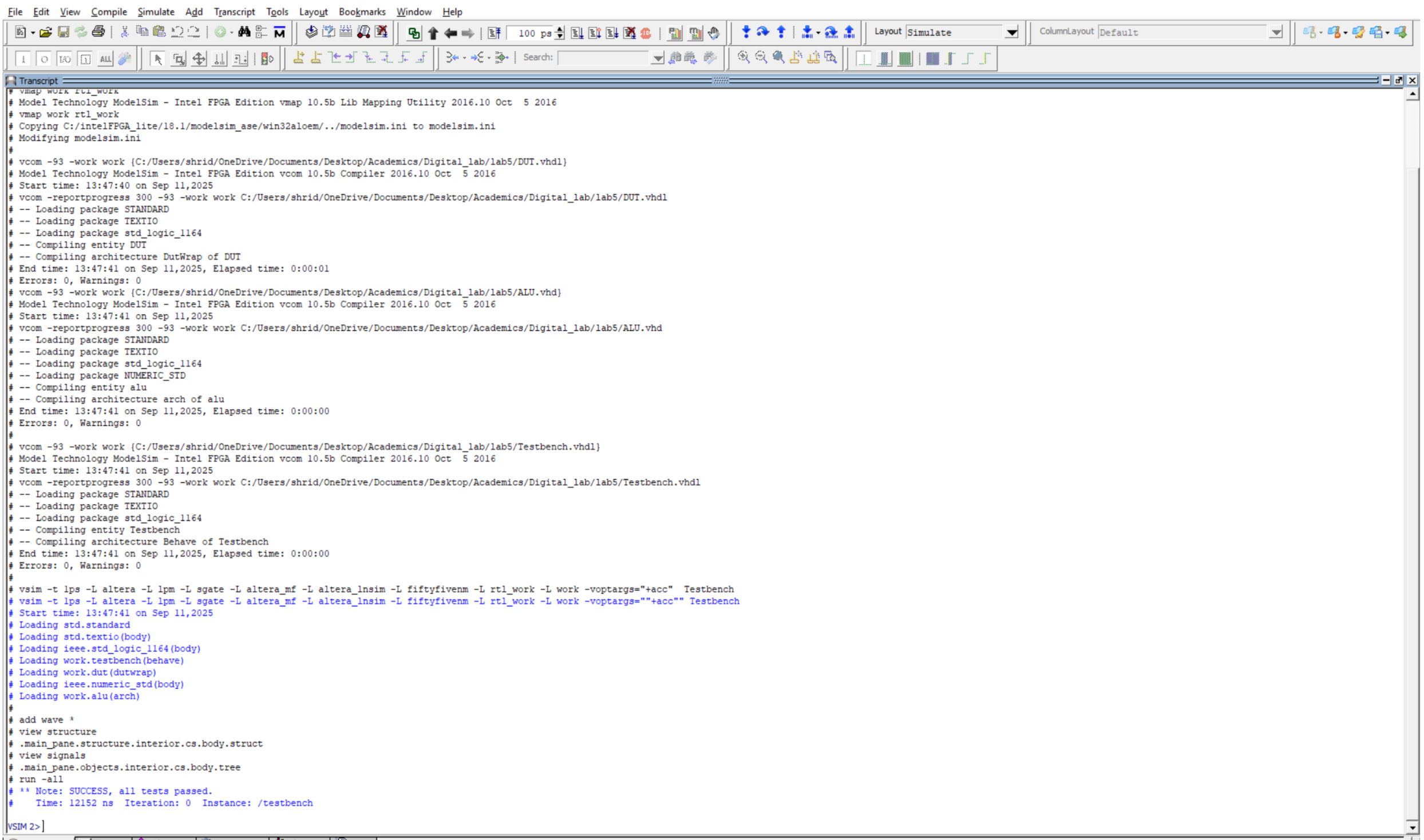
we can finally implement MUX behavior with a for-elsif block:

```
if S = "00" then:
    --shift function

if S == '01" then
    -- Concatenate & 2's complement

if S == "10" then
    -- Multiplication code
```


alu:inst1|alu:instance
input_vector[9..0]
output_vector[7..0]
prod<[3..0]
prod<[8..4]
prod<[13..9]
prod<[18..14]
Add2
Add3
Add4
Add1
Mod0
Div0
Equal2
Equal1
Equal0
Equal3
ShiftLeft0
ShiftRight0
result8<[7..0]
Y[1]$latch
Y[0]$latch
Y[3]$latch
Y[2]$latch
Y[4]$latch
Y[5]$latch
Y[6]$latch
Y[7]$latch
LATCH


File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Transcript
vmap work rtl_work
Model Technology ModelSim - Intel FPGA Edition vmap 10.5b Lib Mapping Utility 2016.10 Oct 5 2016
vmap work rtl_work
Copying C:/intelFPGA_lite/18.1/modelsim_ase/win32aloem/../modelsim.ini to modelsim.ini
Modifying modelsim.ini
#
vcom -93 -work work {C:/Users/shrid/OneDrive/Documents/Desktop/Academics/Digital_lab/lab5/DUT.vhdl}
Model Technology ModelSim - Intel FPGA Edition vcom 10.5b Compiler 2016.10 Oct 5 2016
Start time: 13:47:40 on Sep 11,2025
vcom -reportprogress 300 -93 -work work C:/Users/shrid/OneDrive/Documents/Desktop/Academics/Digital_lab/lab5/DUT.vhdl
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Compiling entity DUT
-- Compiling architecture DutWrap of DUT
End time: 13:47:41 on Sep 11,2025, Elapsed time: 0:00:01
Errors: 0, Warnings: 0
vcom -93 -work work {C:/Users/shrid/OneDrive/Documents/Desktop/Academics/Digital_lab/lab5/ALU.vhd}
Model Technology ModelSim - Intel FPGA Edition vcom 10.5b Compiler 2016.10 Oct 5 2016
Start time: 13:47:41 on Sep 11,2025
vcom -reportprogress 300 -93 -work work C:/Users/shrid/OneDrive/Documents/Desktop/Academics/Digital_lab/lab5/ALU.vhd
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package NUMERIC_STD
-- Compiling entity alu
-- Compiling architecture arch of alu
End time: 13:47:41 on Sep 11,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
#
vcom -93 -work work {C:/Users/shrid/OneDrive/Documents/Desktop/Academics/Digital_lab/lab5/Testbench.vhdl}
Model Technology ModelSim - Intel FPGA Edition vcom 10.5b Compiler 2016.10 Oct 5 2016
Start time: 13:47:41 on Sep 11,2025
vcom -reportprogress 300 -93 -work work C:/Users/shrid/OneDrive/Documents/Desktop/Academics/Digital_lab/lab5/Testbench.vhdl
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Compiling entity Testbench
-- Compiling architecture Behave of Testbench
End time: 13:47:41 on Sep 11,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
#
vsim -t lps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L fiftyfivenm -L rtl_work -L work -voptargs="+acc" Testbench
vsim -t lps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L fiftyfivenm -L rtl_work -L work -voptargs=""+acc"" Testbench
Start time: 13:47:41 on Sep 11,2025
Loading std.standard
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading work.testbench(behave)
Loading work.dut(dutwrap)
Loading ieee.numeric_std(body)
Loading work.alu(arch)
#
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
** Note: SUCCESS, all tests passed.
Time: 12152 ns Iteration: 0 Instance: /testbench
VSIM 2>
Transcript Wave Objects Processes Library sim
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
Msgs
/testbench/input_v...
/testbench/output_...
1111111111
11100001
Now
12152000 ps
Cursor 1
0 ps
2000000 ps
4000000 ps
6000000 ps
8000000 ps
10000000 ps
12000000 ps
Transcript Wave Objects Processes Library sim