



FLIP-FLOPS

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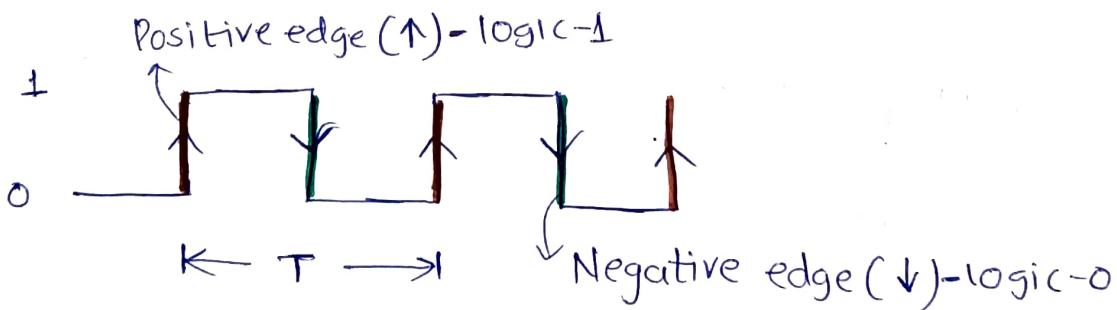
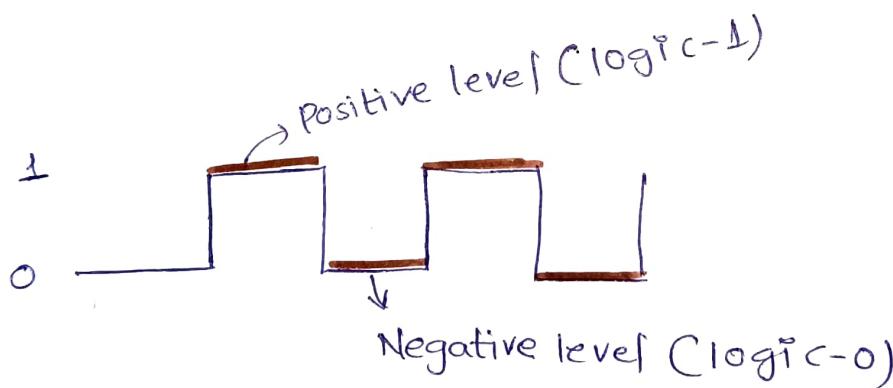
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Flip Flops :-

- FlipFlop is a single bit memory element (or) storage element.
- FlipFlop is a sequential circuit, and it is a edge triggered circuit.
 - 1) positive edge triggered FlipFlops (\uparrow)
 - 2) Negative edge triggered Flip flops (\downarrow)
- The difference between Latches and FlipFlops is,
 - Latches are level triggered.
 - FlipFlops are edge triggered.
- FlipFlop is also called as Bistable multi-vibrator.
- It has two stable states those are
 $0 \rightarrow \text{Low}$ & $1 \rightarrow \text{High}$



Types of FlipFlops:-

→ There are Four types of FlipFlops.

- 1) S-R Flip Flop.
- 2) D - Flip Flop.
- 3) JK Flip Flop.
- 4) T - Flip Flop.

1) S-R Flip Flop:-

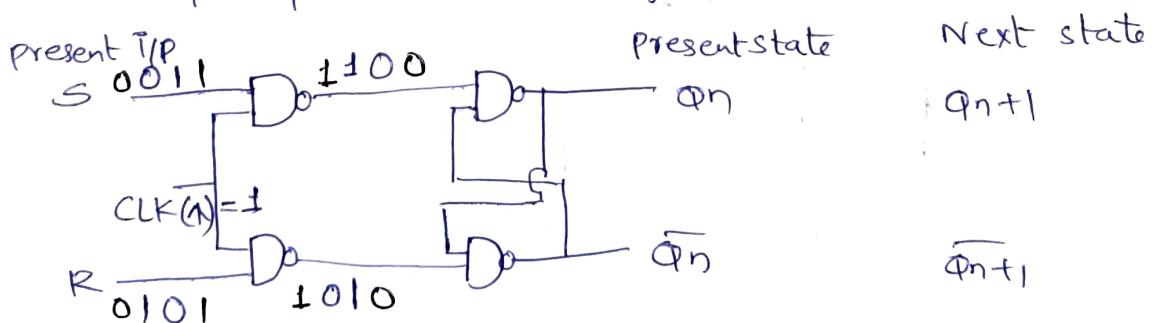
→ The SR Flip Flop is also called as Set, Reset Flip Flop.

- The Set indicates the output as logic-1
- The Reset indicates the output as logic-0.
- The SR Flip Flop can be designed using NAND gates and also using NOR gates
- The Following table shows the Truth Table of NAND gate.

→ If any one input is logic -0 then without referring another input the output is directly logic-1.

a	b	$y = \bar{a}b$
0	0	0
0	1	0
1	0	0
1	1	1

→ The Following fig shows SR - Flip Flop circuit diagram.



(2)

The operation of the SR Flip Flop can be explained in the following way:

Case-i :- $S=0; R=0; CLK=1$

$$\begin{aligned} Q_{n+1} &= \overline{1 \cdot \bar{Q}_n} = \bar{\bar{Q}_n} = Q_n \\ Q_{n+1} &= \overline{1 \cdot Q_n} = \bar{Q}_n = \bar{Q}_n \end{aligned} \quad \left. \begin{array}{l} \text{No-change state.} \\ \end{array} \right\}$$

Case-ii :- $S=0; R=1; CLK=1$

$$\begin{aligned} Q_{n+1} &= \overline{1 \cdot \bar{Q}_n} = \bar{\bar{Q}_n} = Q_n = 0 \\ Q_{n+1} &= \overline{0 \cdot Q_n} = \bar{Q}_n = 1 \quad \uparrow \end{aligned} \quad \left. \begin{array}{l} \text{Reset state.} \\ \end{array} \right\}$$

Case-iii :- $S=1; R=0; CLK=1$

$$\begin{aligned} Q_{n+1} &= \overline{0 \cdot \bar{Q}_n} = \bar{\bar{Q}_n} = 1 \\ Q_{n+1} &= \overline{1 \cdot 1} = \bar{1} = 0 \end{aligned} \quad \left. \begin{array}{l} \text{Set state} \\ \end{array} \right\}$$

Case-iv :- $S=1; R=1; CLK=1$

$$\begin{aligned} Q_{n+1} &= \overline{0 \cdot \bar{Q}_n} = \bar{\bar{Q}_n} = 1 \\ Q_{n+1} &= \overline{1 \cdot 0} = \bar{0} = 1 \end{aligned} \quad \left. \begin{array}{l} \text{Invalid state.} \\ \end{array} \right\}$$

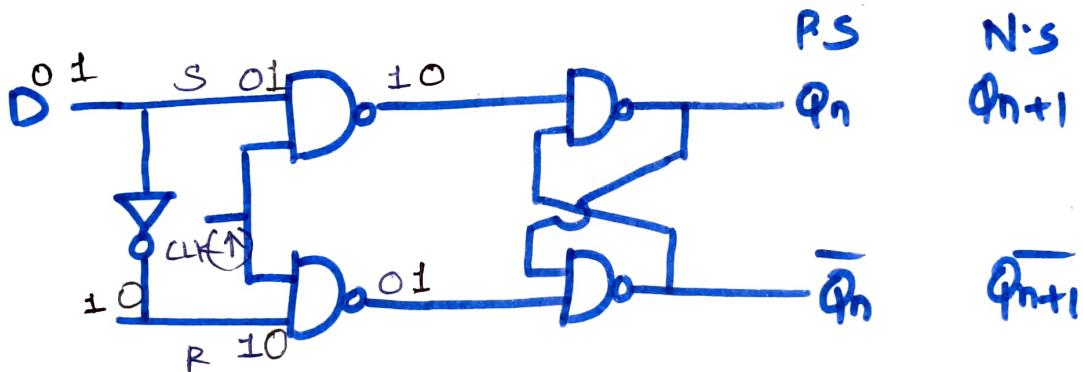
Truth Table of SR Flip Flop:-

S	R	P.S \bar{Q}_n	N.S Q_{n+1}
0	0	X	$\bar{Q}_n \rightarrow \text{NC}$
0	1	X	0 $\rightarrow \text{Reset}$
1	0	X	1 $\rightarrow \text{set}$
1	1	X	ID $\rightarrow \text{invalid}$

S	R	P.S \bar{Q}_n	N.S Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	ID
1	1	1	ID

2) D-FlipFlop:-

- The D-FlipFlop is a Data FlipFlop, it is also called as Delay FlipFlop (or) Transparent FlipFlop
- The output of the D-Flip Flop is same as input, but the difference is that Delay in the output with respect to input.
- The D-Flip Flop is used in the Registers
- The D-Flip Flop is obtained from the SR Flip Flop by shortcircuiting the S&R with an not gate
- The D-Flip Flop circuit is given below fig:-



The operation of the ~~D~~ FlipFlop can be explained in the following way.

Case :- 1

$$D = 0 \Rightarrow S = 0 \text{ & } R = 1 ; \text{ CLK} = 1$$

$$\begin{aligned} Q_{n+1} &= \overline{1 \cdot \bar{Q}_n} = \overline{\bar{Q}_n} = Q_n = 0 \\ Q_{n+1} &= \overline{Q_n \cdot 0} = \overline{0} = 1 \end{aligned} \quad \left. \begin{array}{l} \uparrow \\ \text{preset state.} \end{array} \right.$$

(3)

Case :- 2

$$D=1 \Rightarrow S=1 \& R=0; CLK=1$$

$$Q_{n+1} = \overline{0 \cdot \bar{Q}_n} = \overline{0} = 1 \quad \left. \right\} \text{set state.}$$

$$\bar{Q}_{n+1} = \overline{1 \cdot 1} = \overline{1} = 0 \quad \left. \right\}$$

Truth Table of D - Flip Flop :-

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Reset

Set

3) J-K Flip Flop :-

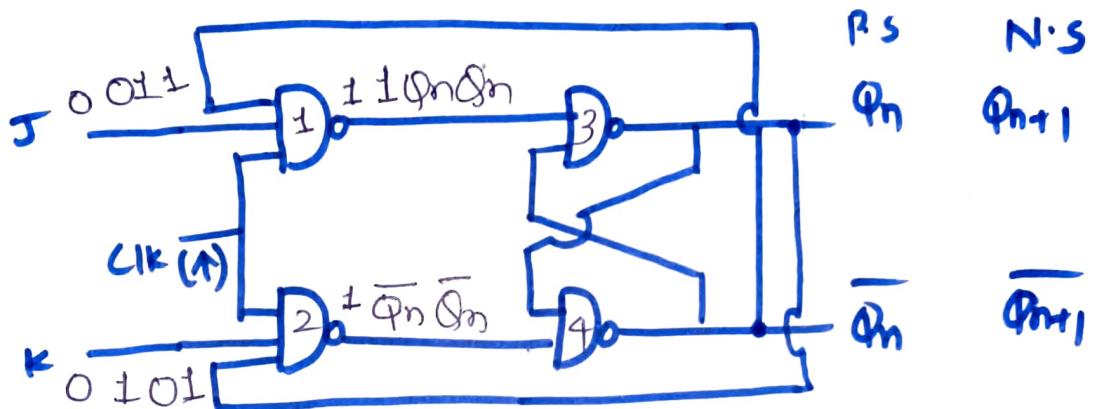
→ The JK Flip Flop was invented by the scientist Jack Kilby. so the name of JK Flip Flop is derived from the scientist name and it termed as the two inputs as J & K.

→ The JK Flip Flop can be obtained from the SR Flip Flop by feed back of Next state outputs as inputs to the present inputs

→ The JK Flip Flop is introduced to utilize the $S=1; R=1$ combination in the SR Flip Flop (Invalid state)

→ But in JK FlipFlop, that combination is utilized with one drawback, i.e., the output will suffer from multiple toggling. Hence, it is called as Race around condition.

→ The following Fig shows the circuit diagram of JK FlipFlop.



The operation of the JK FlipFlop is explained in the following way.

Case :- 1

$$J=0; K=0; CLK=1$$

$$\begin{aligned} Q_{n+1} &= \overline{1 \cdot \overline{Q}_n} = \overline{\overline{Q}_n} = Q_n \\ Q_{n+1} &= \overline{\overline{Q}_n \cdot 1} = \overline{\overline{Q}_n} \end{aligned} \quad \left. \right\} \text{No change state}$$

Case :- 2

$$J=0; K=1; CLK=1$$

$$\begin{aligned} Q_{n+1} &= \overline{1 \cdot \overline{Q}_n} = \overline{\overline{Q}_n} = \overline{Q_n} = 0 \\ Q_{n+1} &= \overline{\overline{Q}_n \cdot Q_n} = \overline{0} = 1 \end{aligned} \quad \left. \right\} \text{Reset state.}$$

Rough work gate - 2
 $\overline{1 \cdot 1 \cdot \overline{Q}_n} = \overline{Q_n}$

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Case :- 3

$$J=1; K=0; CLK=1$$

$$Q_{n+1} = \overline{Q_n \cdot \overline{Q_n}} = \overline{0} = 1 \Rightarrow \boxed{1}$$

$$\overline{Q_{n+1}} = \overline{1 \cdot \overline{Q_n}} = \overline{\overline{Q_n}} = Q_n = 0 \quad \boxed{\text{Set state.}}$$

Rough work of gate-1
 $1 \cdot 1 \cdot \overline{Q_n} = \overline{Q_n} = Q_n$

Case :- 4

$$J=1; K=1; CLK=1$$

Here firstly we need to find the $\overline{Q_{n+1}}$ to get the Toggle state. otherwise, if we find Q_{n+1} then it will give the Invalid output as $\underline{Q_{n+1} = \overline{Q_{n+1}} = 1}$

$$\overline{Q_{n+1}} = \overline{Q_n \cdot \overline{Q_n}} = \overline{0} = 1$$

$$Q_{n+1} = \overline{1 \cdot \overline{Q_n}} = \overline{Q_n} \quad (\text{Toggle})$$

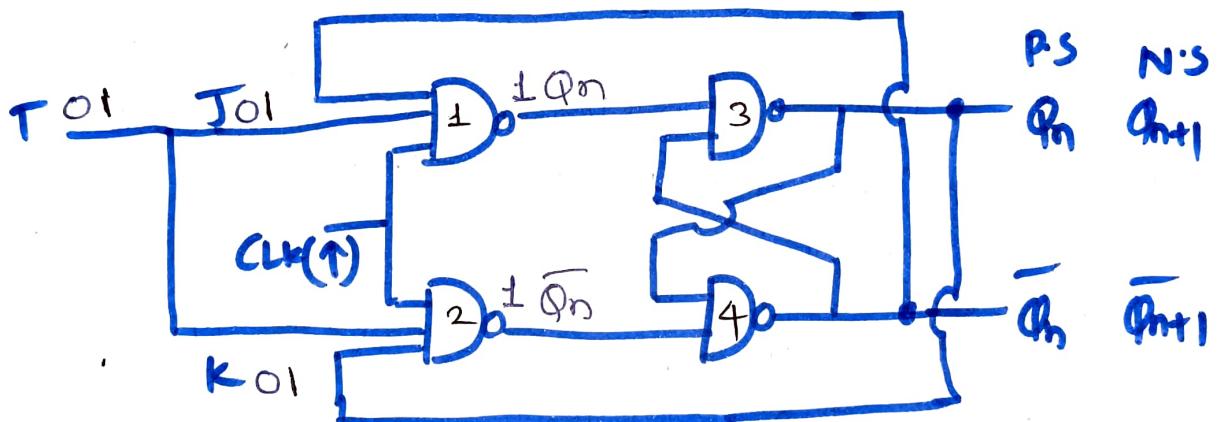
The Truth Table of JK FlipFlop is given below.

J	K	Q_n	Q_{n+1}	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset state
0	1	1	0	
1	0	0	1	Set state
1	0	1	1	
1	1	0	1	Toggle state
1	1	1	0	

Rough work
 $\underline{gate-1}$
 $1 \cdot 1 \cdot \overline{Q_n} = \overline{Q_n} = Q_n$
 $\underline{gate-2}$
 $1 \cdot 1 \cdot Q_n = \overline{Q_n}$

4) T-FlipFlop:-

- T-FlipFlop is a Toggle FlipFlop.
- The output of Toggle FlipFlop will change every time, hence it is called as Race-around condition.
- The Toggle FlipFlop is used in the design of counters.
- The Toggle FlipFlop can be obtained by short circuiting the J & K inputs of JK FlipFlop.
- The following Fig shows the circuit diagram of the T-FlipFlop



The operation of the T-FlipFlop is explained in the following way.

Case :- 1 $T=0 \Rightarrow J=0 ; K=0 ; CLK=1$

$$\begin{aligned} Q_{n+1} &= \overline{J \cdot Q_n} = \overline{Q_n} = Q_n \\ Q_{n+1} &= \overline{Q_n \cdot I} = \overline{Q_n} \end{aligned} \quad \left. \right\} \text{No change state.}$$

Case 2 $T=1 \Rightarrow J=1; K=1$

$$Q_{n+1} = \overline{Q_n Q_n} = \overline{0} = 1 \}$$

$$Q_{n+1} = \overline{1 \cdot Q_n} = \overline{Q_n} \quad \left. \begin{array}{l} \\ \end{array} \right\}$$

Toggle state.

Rough work gate-1

$$\overline{1 \cdot 1 \overline{Q_n}} = \overline{\overline{Q_n}} = Q_n$$

gate -2

$$\overline{1 \cdot 1 \cdot Q_n} = \overline{Q_n}$$

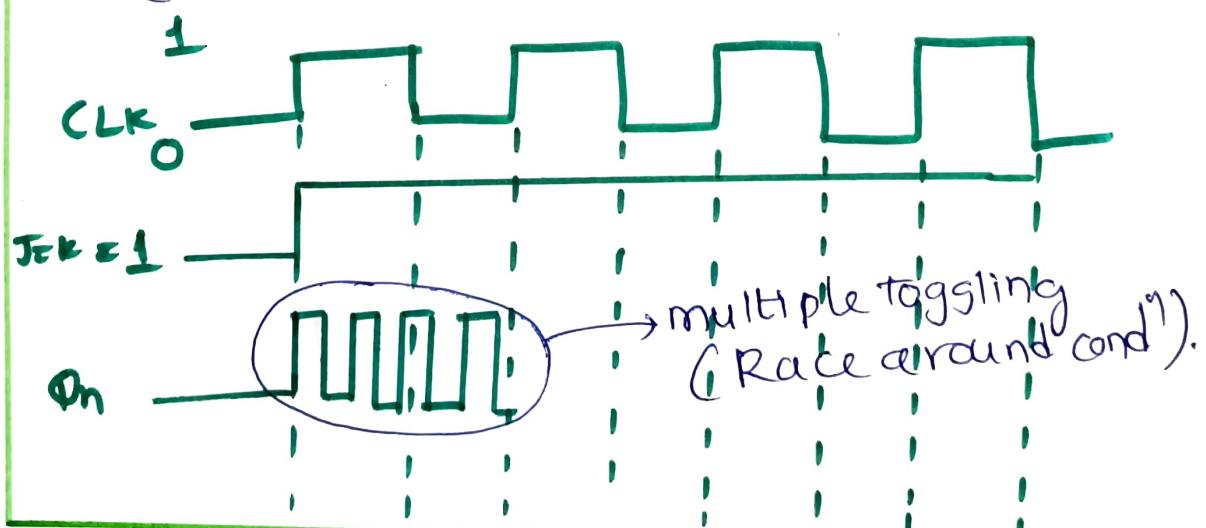
Truth Table of T- FF

T	Q_n	Q_{n+1}
0	0	0 } No change state
0	1	0 }
1	0	1 } Toggle state
1	1	0 $\overline{Q_n}$

(5)

Race around condition :-

- The Race around condition is a multiple toggling state. In case of the JK Flip Flop.
- The Race around condition is due to the feed back of Toggle outputs to the input state of Input J,K.
- The Race around condition is mainly occurs to the level triggered FlipFlops because the long duty cycle of the clock signal.
- In that long duty cycle of clock the output is fed to input side so the input will change accordingly and it causes the multiple toggling it is known as Race around condition.
- The Following Timing diagram shows the Race around Condition.



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The 'Race around condition can be avoided by the following methods

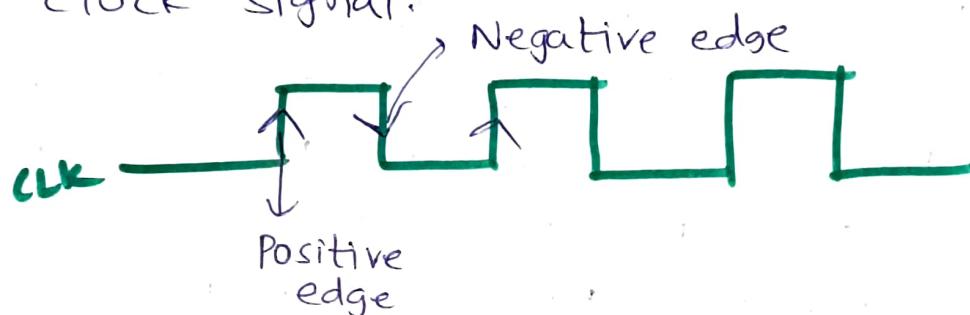
1) edge triggered Flip Flops.

2) JK Master slave Flip Flop.

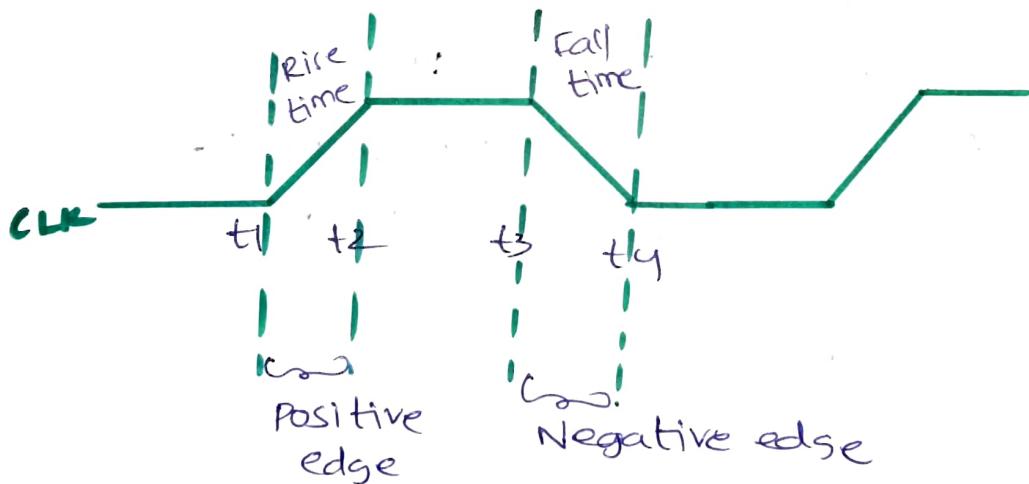
1) edge triggered Flip Flops:

→ The edge triggered Flip Flops can b- eliminate the Race around condition.

→ The following fig shows the ideal clock signal.



→ But the practical clock donot has the sharp cut-off edges.

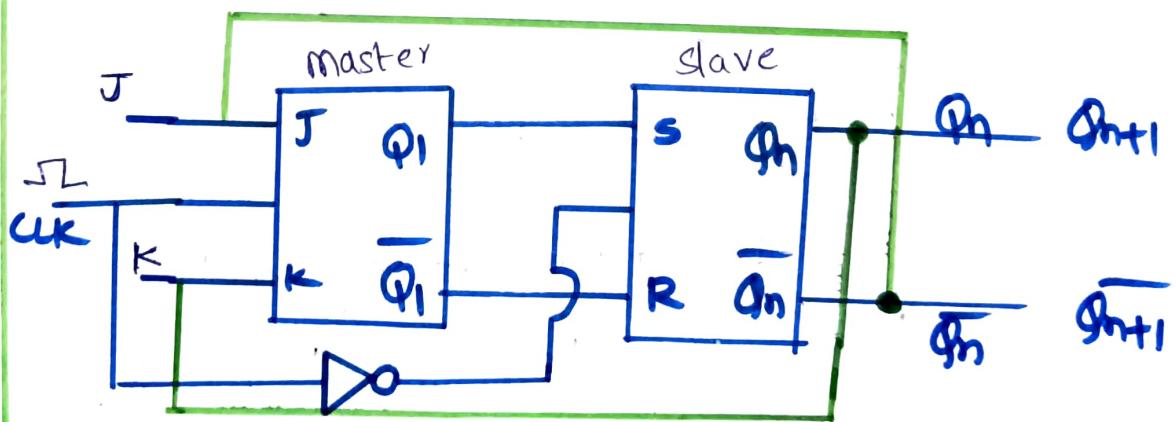


→ Due to the Rise time delay (or) Fall time delay, this edge triggered flip flop do not

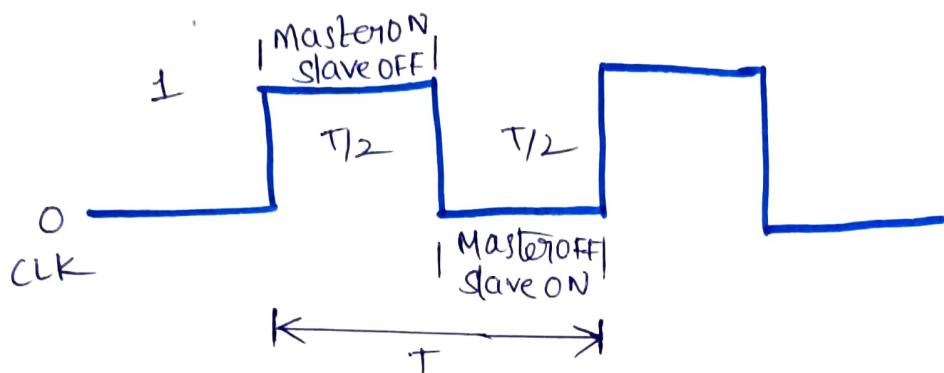
minimize the Race around condition to the minimal toggling.

2) JK Master slave Flip Flop

- JK Master slave Flip Flop consists of the level triggered Gated JK latch and Gated SR latch.
- The JK FF acts as Master and SR FF acts as slave
- Note:- The Gated latches with level triggered clock are also called FlipFlops.
- The clock in the Master slave is given as, normal clock for the Master and inverted clock for the Slave
- the Master will active for the positive level duty cycle of clock and the slave will active for the Negative level duty cycle of the clock.
- When the FF is ON state, it is called as Active state. and when the FF is OFF state then it is called as memory state.



→ The Following image predicts when the Master ON, OFF and slave ON, OFF.



The operation of the Master slave FlipFlop is given as follows.

Case-1 :- $J=0$; $K=0$; $CLK=1$ (Positive cycle)

Master - ON

Slave - OFF

The output of J,K are unchanged and slave -OFF the output of slave are no change

* $CLK=0$ (Negative cycle)

Master - OFF

slave - OFF

The output of SR is unchanged due to No change S,R inputs.

Case-2 :- $J=0$; $K=1$; $CLK=1$

Master - ON

$$Q_1 = 0 \rightarrow S$$

$$\bar{Q}_1 = 1 \rightarrow R$$

slave - OFF

$$S = 0 ; Q_n$$

$$R = 1 ; \bar{Q}_n$$

} No change

* $CLK = 0$

Master - OFF
Slave - ON

$Q_n = 0$
 $\bar{Q}_n = 1$

} Reset state

Case-3:- $J=1; K=0; CLK=1$

Master - ON

$Q_1 = 1 \rightarrow S$

$\bar{Q}_1 = 0 \rightarrow R$

slave - OFF

$S = 1 \quad Q_n$ } do not

$R = 0 \quad \bar{Q}_n$ } change

* $CLK = 0$

Master - OFF

Slave - ON

$Q_n = 1$
 $\bar{Q}_n = 0$

} set state

Case-4:- $J=1; K=1; CLK=1$

Master - ON

$Q_1 \quad \bar{Q}_1$ } Toggle $\xrightarrow[S]{R}$

Slave - OFF

$S \quad R$ } Toggle $Q_n \quad \bar{Q}_n$ } No
} change

* $CLK = 0$

Master - OFF

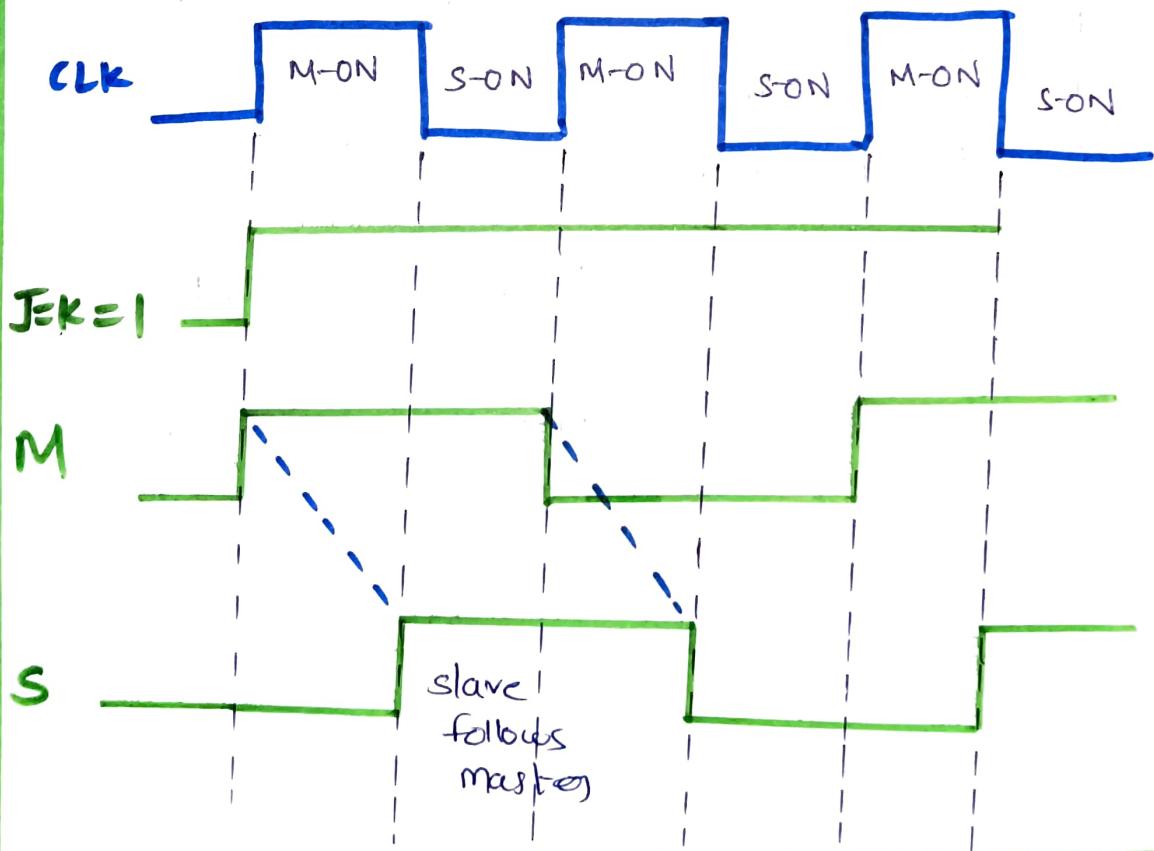
Slave - ON

Q_n } Toggles
 \bar{Q}_n

→ The output Q_n, \bar{Q}_n are also toggles but it will not toggle multiple times because the output is fed back to the input of JK Flip Flop and it is in OFF state due to $clock = 0$.

→ Hence by this we can avoid the Race around condition.

→ The Following Fig shows the timing diagram of the JK Master slave Flip Flop.



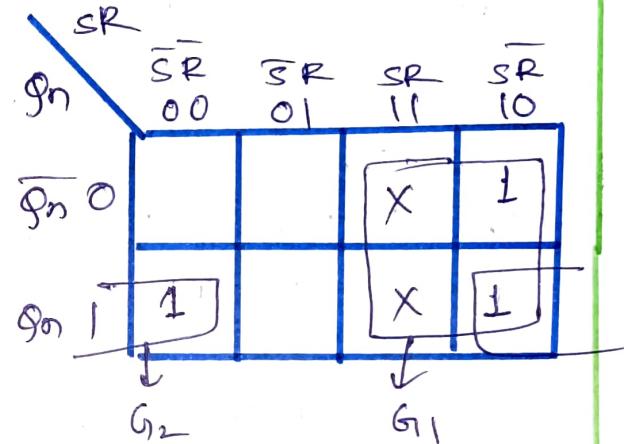
Characteristic eqⁿ and Excitation table of SR FF

characteristic eqⁿ defn:-

→ characteristic eqⁿ is a algebraic eqⁿ, it is represented in the combination of the present state and next state and present input-

$$\Rightarrow \text{Next state} = \text{present input} + \text{present state} \\ (\text{previous output})$$

S	R	PS Q_n	NS Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	ID(X)
1	1	1	ID(X)



$$G_1 = S ; G_2 = \bar{R}Q_n$$

$$\therefore Q_{n+1} = S + Q_n \bar{R}$$

↓

characteristic eqⁿ.

Excitation table defⁿ:

→ This table represents the input combination for the required outputs.

→ The excitation table and characteristic table both are used in the flip flop conversion.

characteristic table.

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	ID
1	1	1	ID

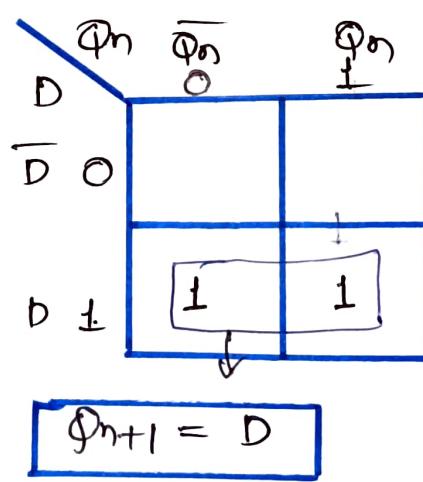
excitation table.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

characteristic eqⁿ and excitation table of DFF:-

characteristic eqⁿ:

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



Excitation Table of D-FF:-

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic eqⁿ and Excitation Table of JK FlipFlop:-

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Q_n	JK	$\bar{J}K$	JK	$\bar{J}K$
\bar{Q}_n	00	01	11	10
0			<u>1</u>	<u>1</u>
1		<u>1</u>		
				<u>1</u>

$$Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$$

$$Q_{n+1} = \bar{J}\bar{Q}_n + \bar{K}Q_n$$

Excitation Table of JK FF:-

characteristic eqⁿ

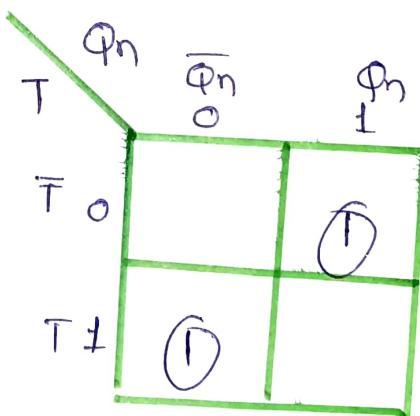
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

excitation Table .

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

characteristic eqⁿ and Excitation Table of T-FlipFlop :-

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



$$Q_{n+1} = T \bar{Q}_n + \bar{T} Q_n$$

Excitation Table of T-FF :-

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0