ENERGY-EFICIENT MEDIAN FILTER ON FPGA

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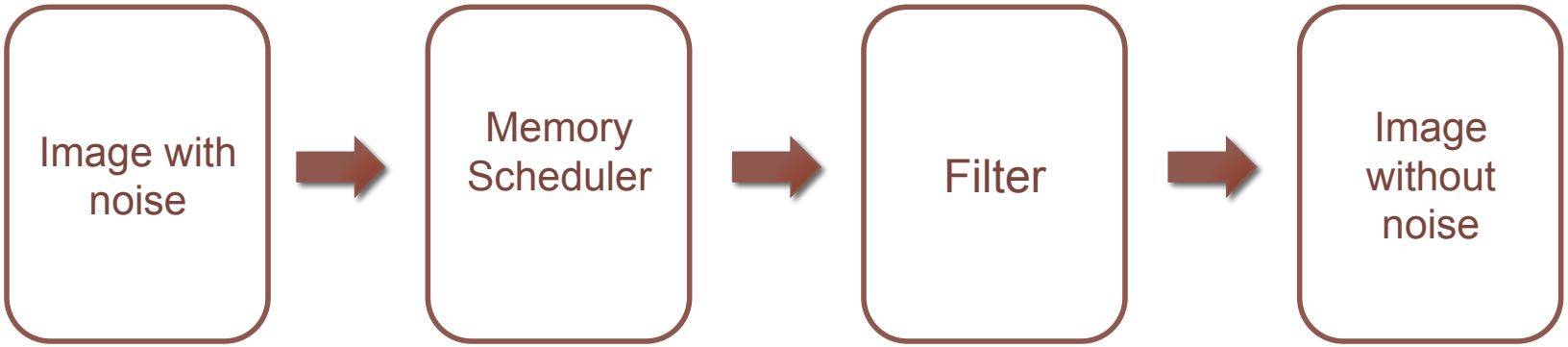
Median Filter

A nonlinear digital filtering technique,
often used to remove noise.



Memory Space

- Xilinx Spartan-6 LX16 FPGA contain 16Mbyte RAM (x16)
- Size of image from 1024x1024 pixels with 32bpp to 128x128 pixels with 8bpp.

Memory Scheduler

- Store the image data into memory parallel.
- Let B be the number of image pixels in one block and N is the length of the image. We will have N^2/B Blocks.
- For efficiency, we only active needed blocks, the rest remain deactivate.

Memory Scheduler

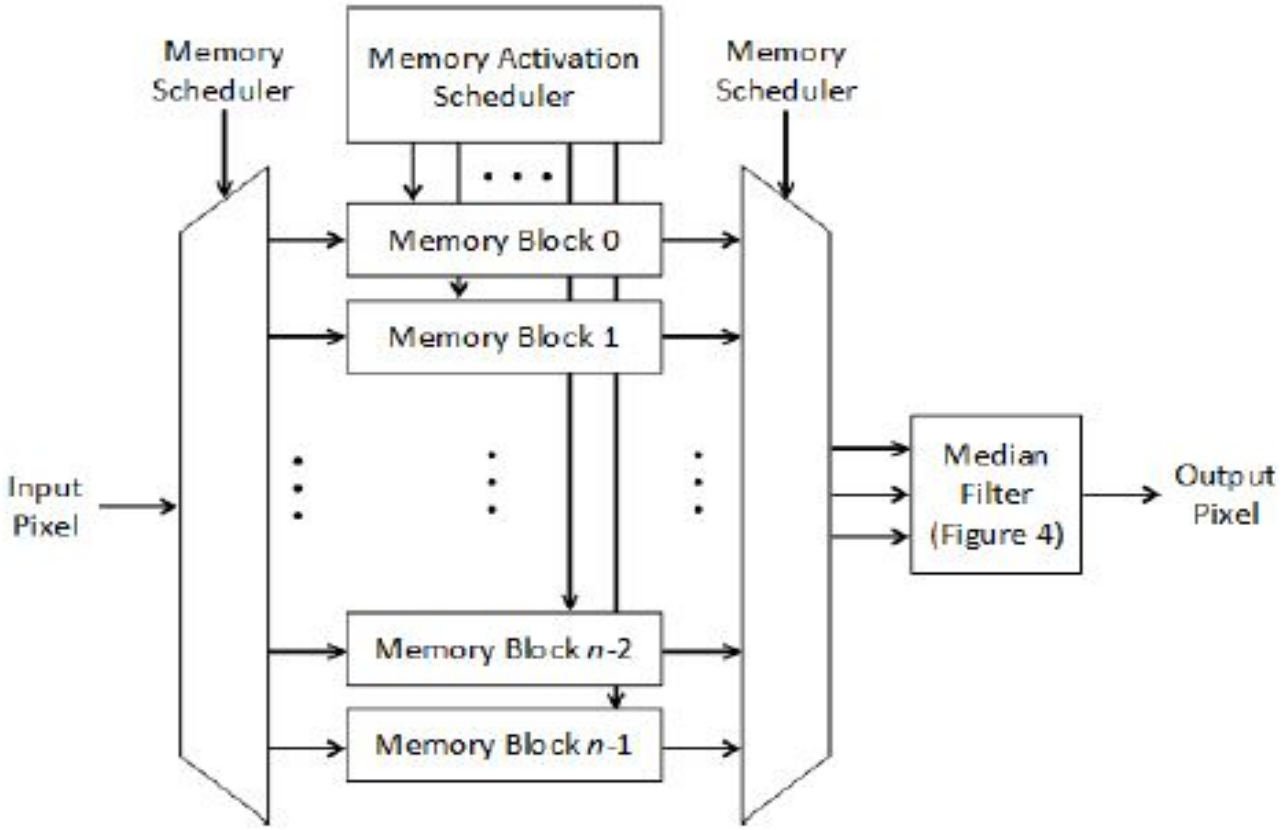


Fig. 1: High-level organization of our approach

Select with the Block

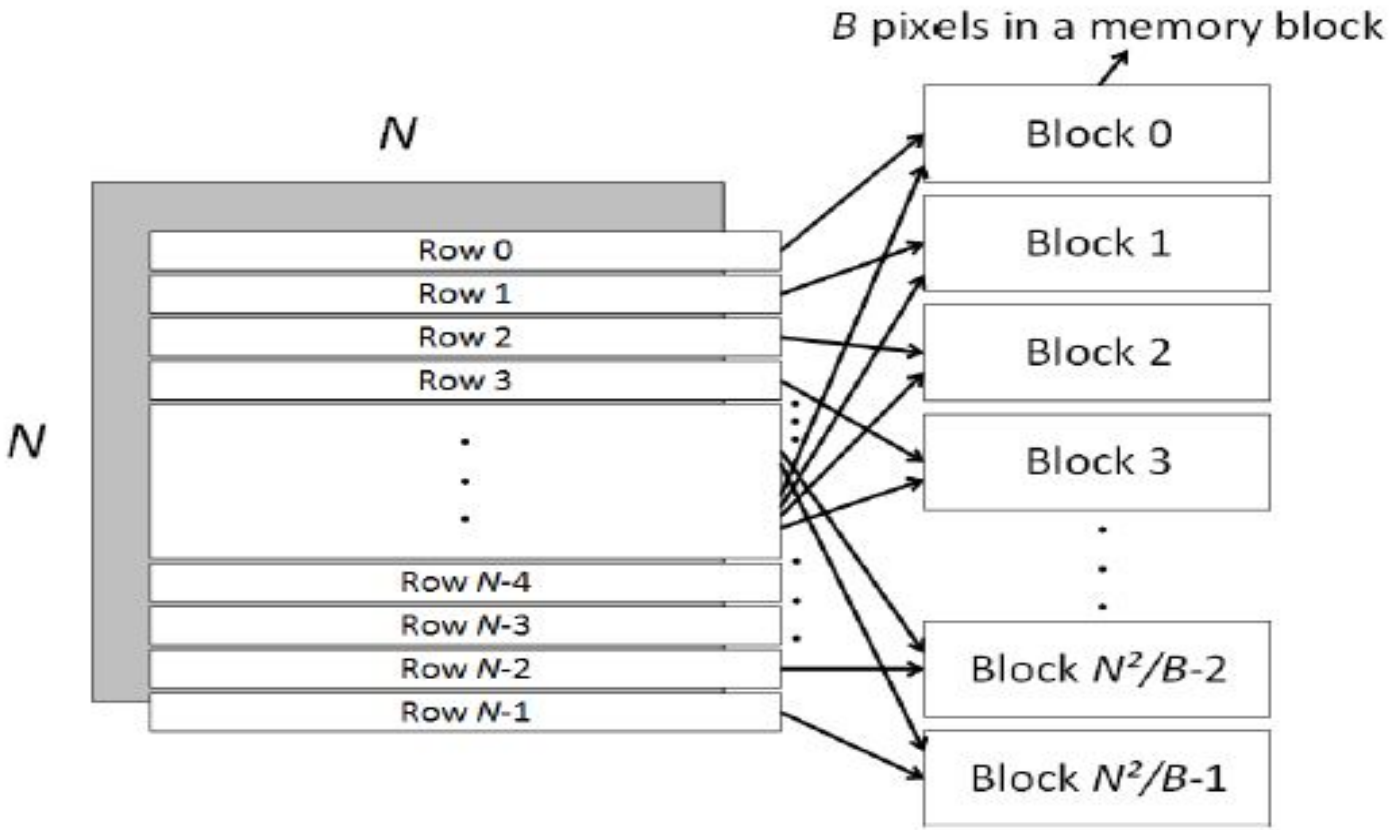
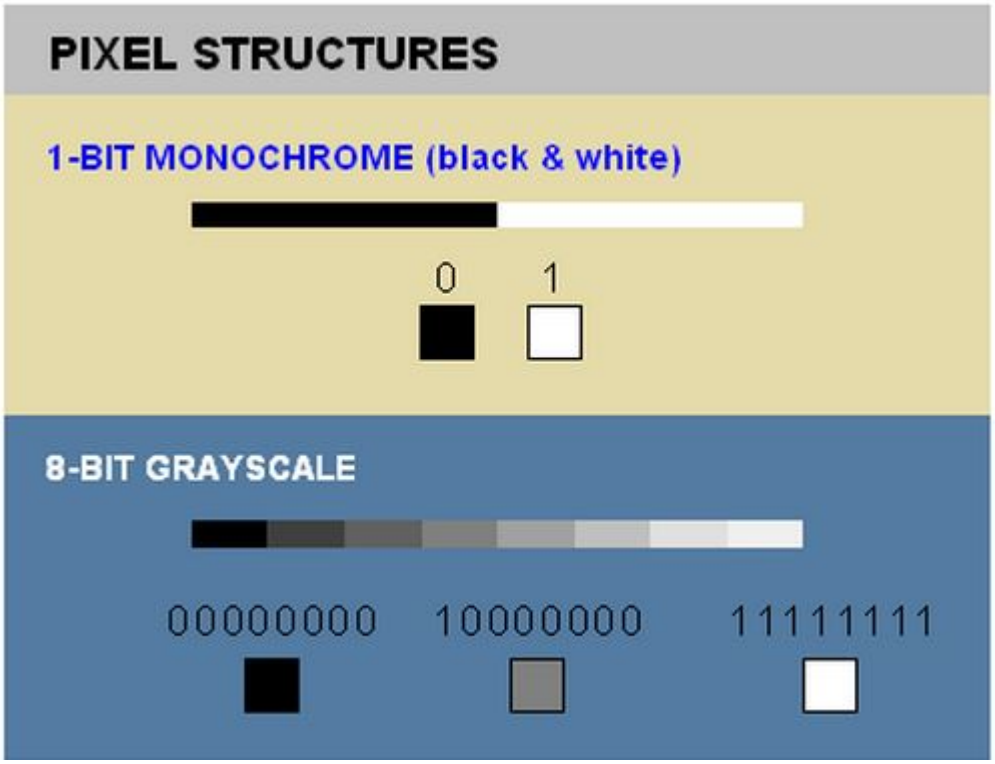
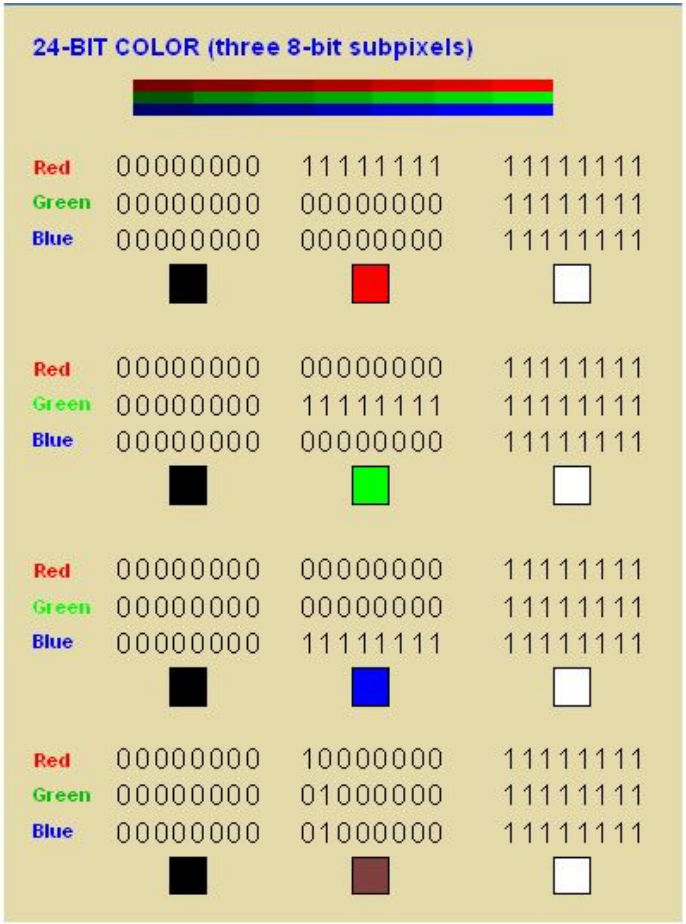


Fig. 7: Data layout

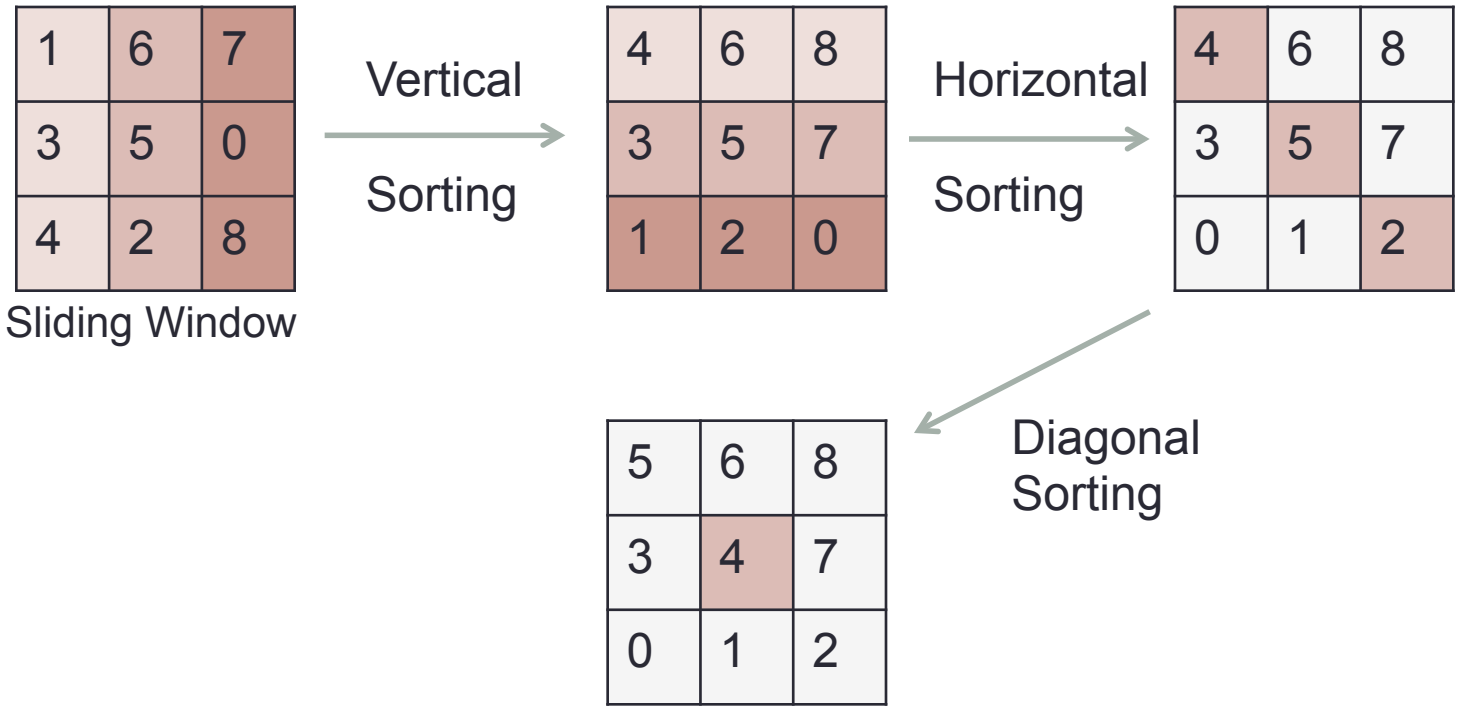
Pixel Structure



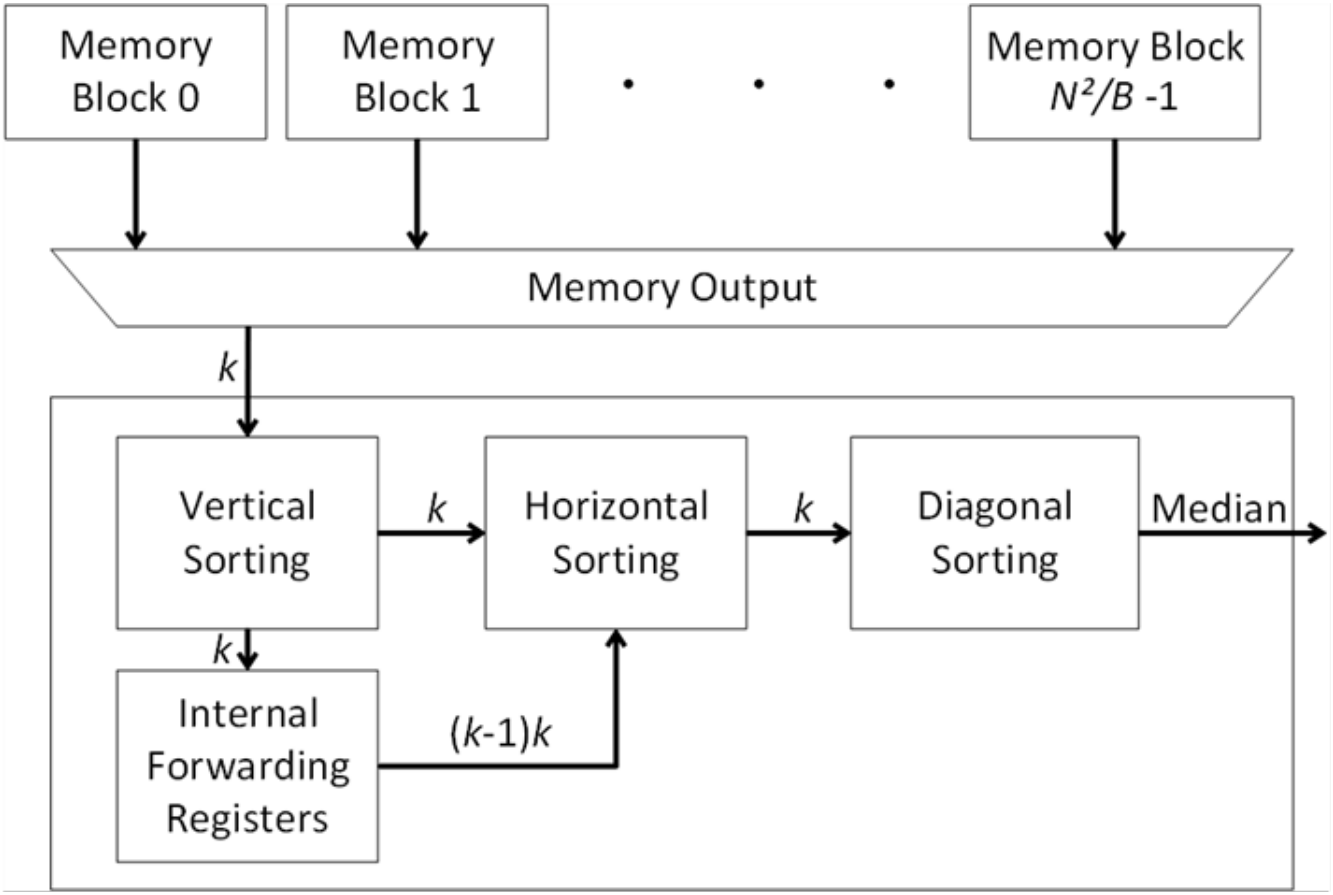
Pixel Structure



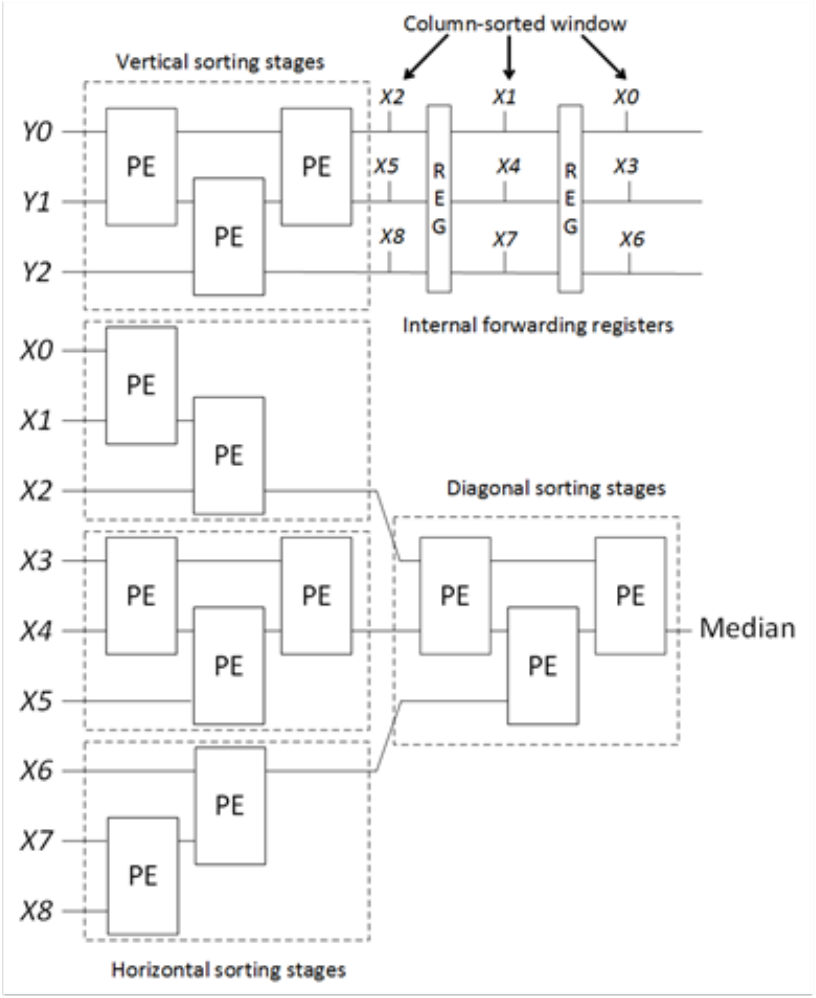
Algorithm in Median Filter



Filtering Procedure



Median Filter Architecture



Power Consumption Evaluation

- Dynamic power will use 20% toggle rates calculated from:
  Post-place and Route results
  Xilinx XPower Analyzer tool

- Image Sizes will be used:
  128x128, 256x256, 512x512
  1024x1024 with 8 to 32 bpp

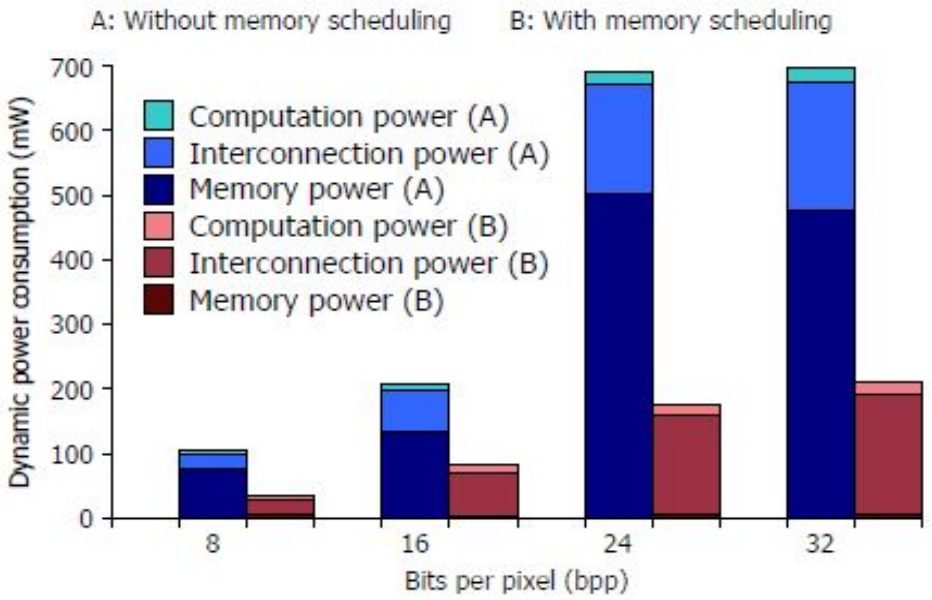
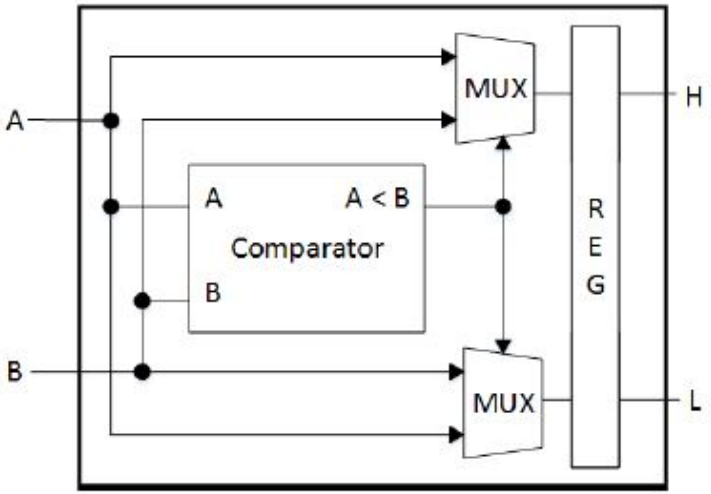


Fig. 10: Power profile of the architecture for a 512 x 512 image

Energy Efficiency

- To quantify we estimated the sustained energy efficiency
- Measured the peak energy efficiency using a minimal architecture for the processing element under ideal conditions.
- GOPS/s/W



Energy Efficiency

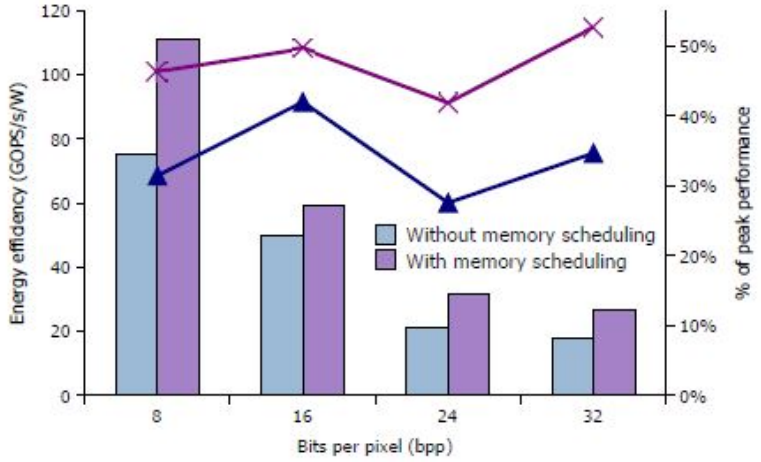


Fig. 11: Performance of a 128 x 128 image

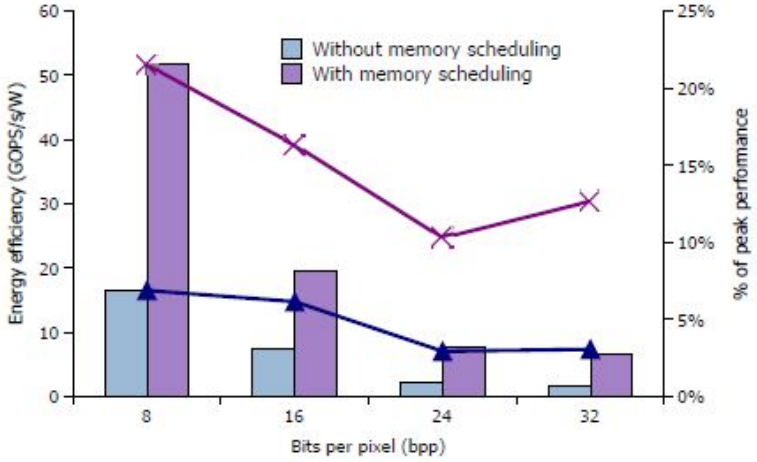
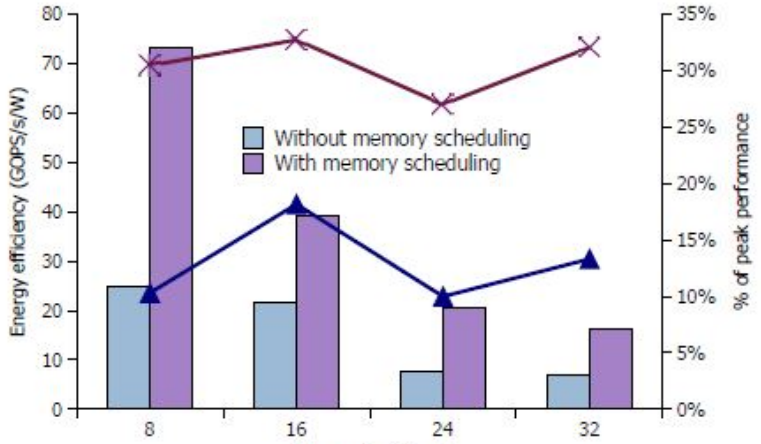
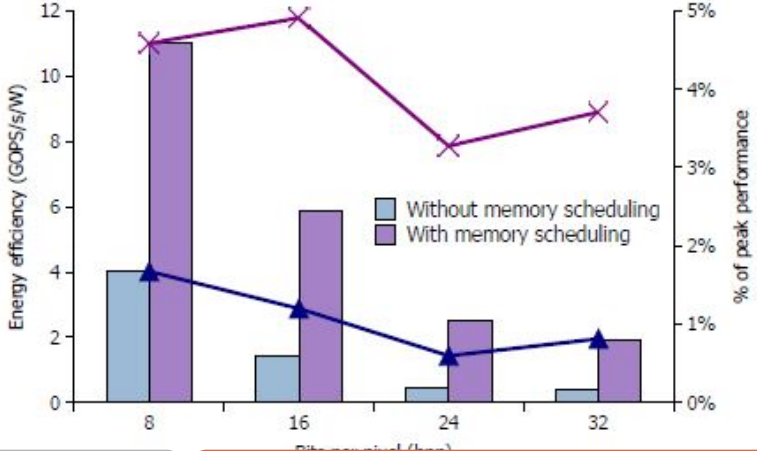


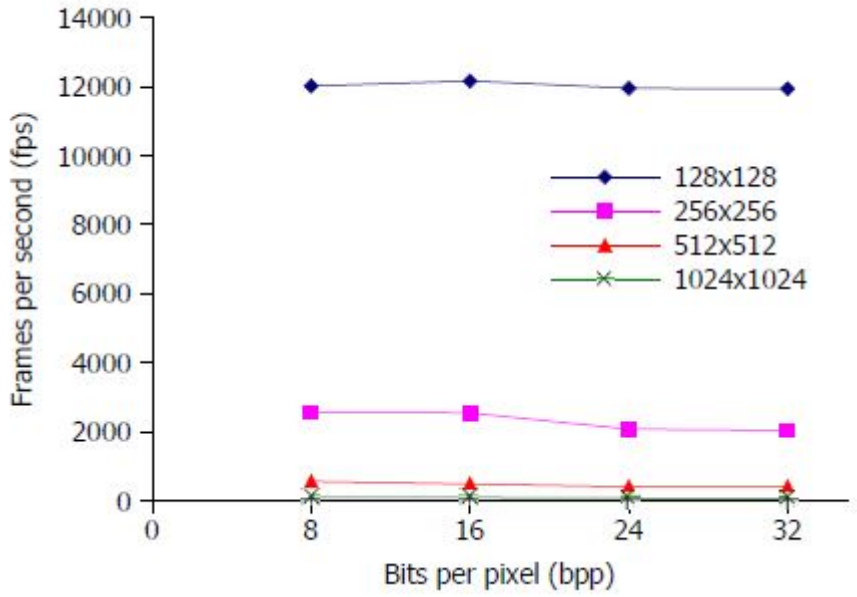
Fig. 13: Performance of a 512 x 512 image



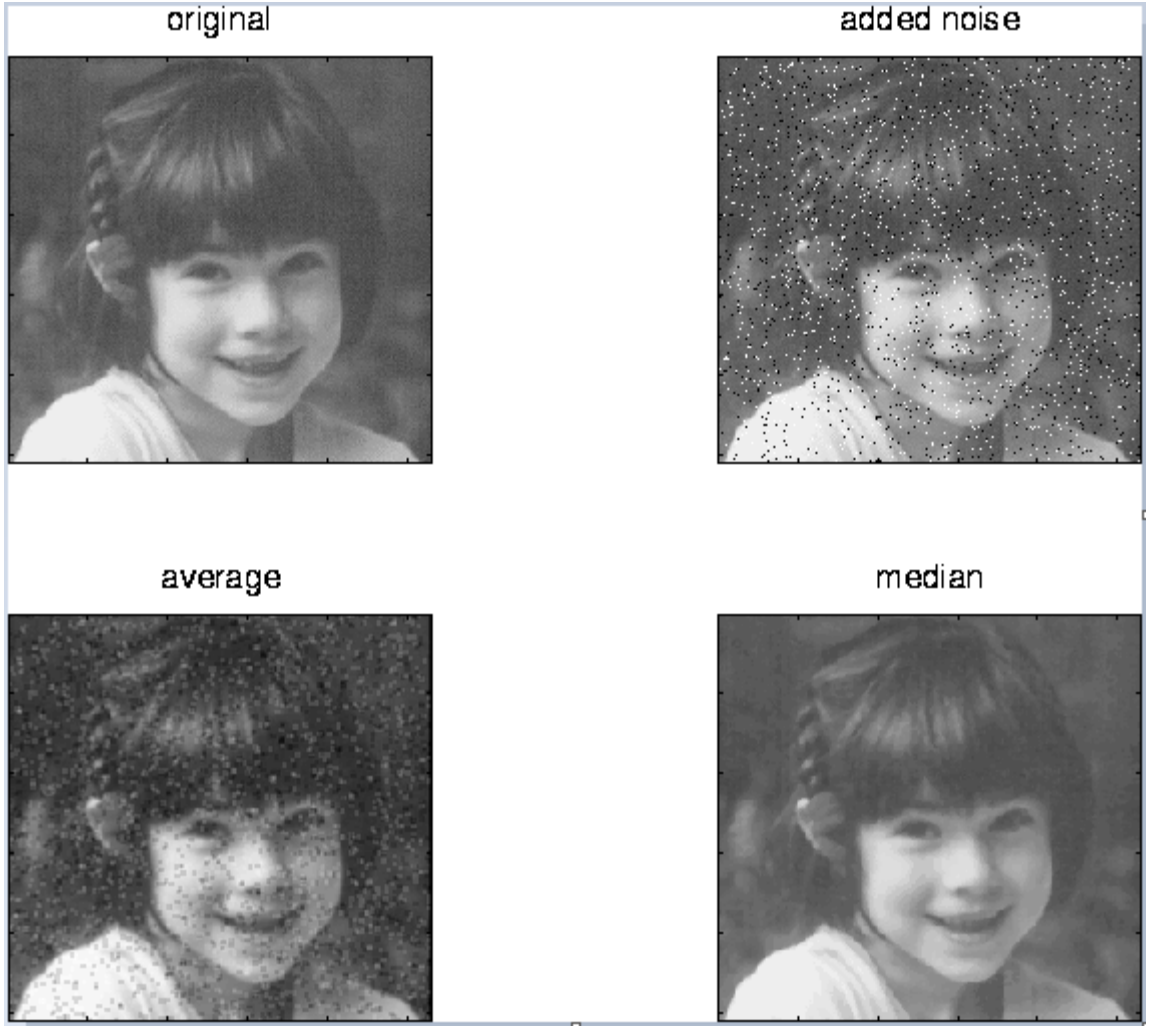


Throughput

- We define throughput as the frame rate or the number of frames per second.



Expected Result



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