Digital Design - CS/ECE/EEE F215

Design Assignment - Project Report

- Group Members (Group no. 42):

Name	**ID**
S. K. Anusri	**2018B5A70876G**
Asmita Limaye	2018B5A70881G
Arunabha Mukherjee	2018B5A70687G
Aman Jain	2018B5A70868G
Darshan Kothari	2018B5A70873G
Varun Singh	2018B5A70869G

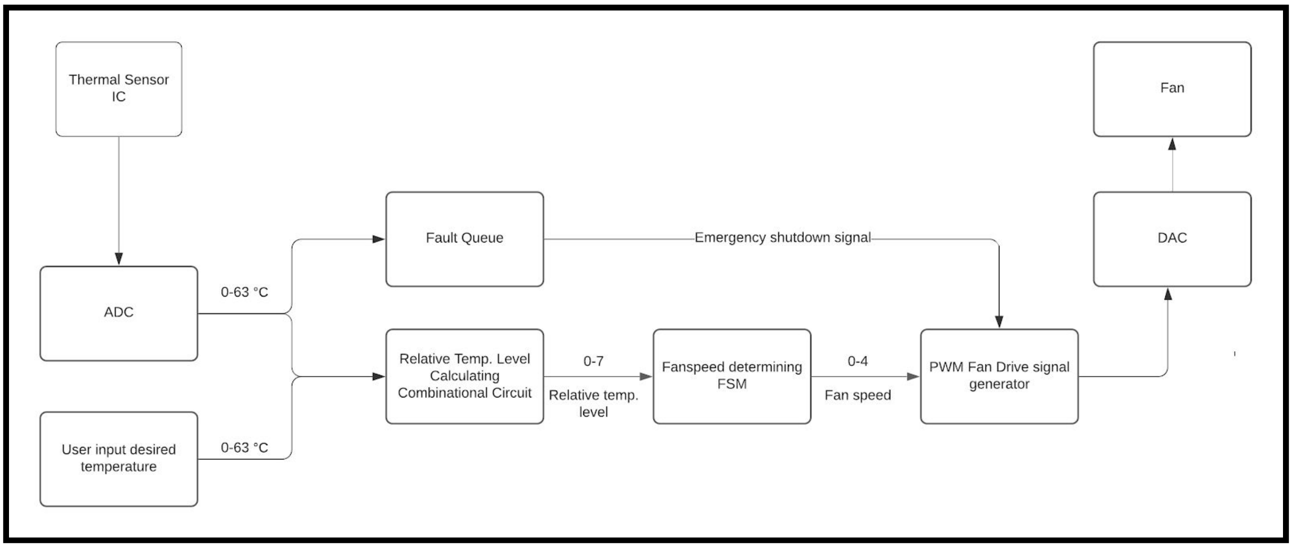
- Problem Statement 6:
  Design a system for cooling by using a fan with variable speeds and a temperature sensor that measures the ambient temperature. Assume that the fan has four variable speeds when switched ON. The temperature sensor can be assumed to have 4 levels above and 4 levels below the set temperature of the room.

Index

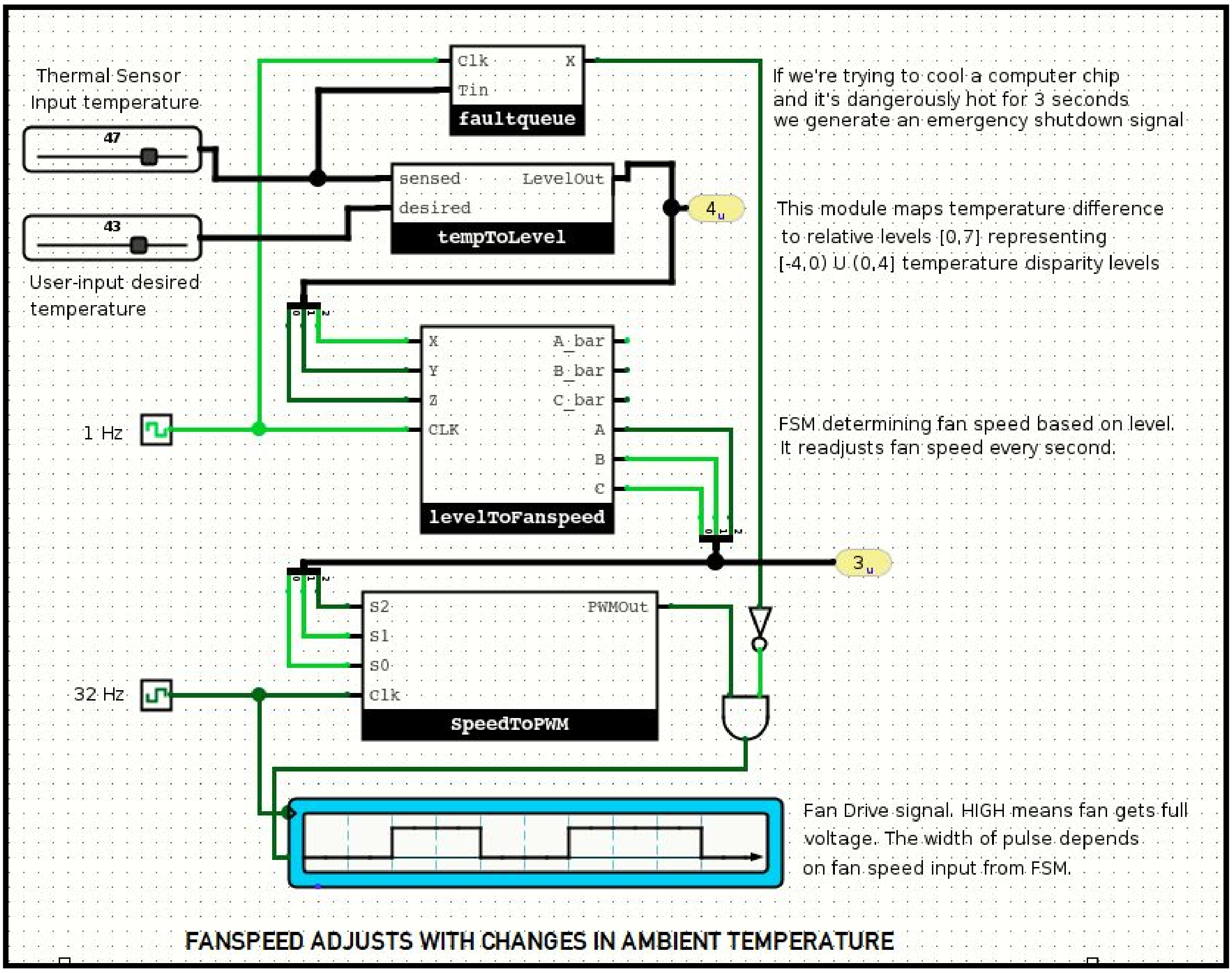
Top-Level Block Diagram

The top-level block diagram consists of the following blocks:

1. Thermal sensor input
2. Analog to Digital Converter (ADC)
3. Fault queue
4. Temperature to Relative Level combinational circuit
5. Relative Level to Fan Speed Finite State Machine
6. Fan Speed to Pulse Generator
7. Digital to Analog Converter (DAC)
8. Fan



The following diagram illustrates the 4 primary circuit blocks involved in our design :



Assumptions & Design Choices

1. Temperature range for operation: 0 °C to 63 °C. TTL 7400 series ICs function in this range.
2. 8 relative temperature levels - 4 above and 4 below the user set temperature - are used to determine fan speed.
3. The input(desired) temperature and the ambient(sensed) temperature have a range of 0-63 ℃.

Temperature Difference(Desired - Sensed)	**Level**	**Mapped to**
(-64, -48)	-4	0
[-48, -32)	-3	1
[-32, -16)	-2	2
[-16, 0)	-1	3
[0, 16)	+1	4
[16, 32)	+2	5
[32, 48)	+3	6
[48, 63]	+4	7

4. The encodings used for the relative temperature levels are given in the following table :

Relative Temperature Level	**Mapped to**	**Encoding**
-4	0	000
-3	1	001
-2	2	010
-1	3	011
+1	4	100

+2	5	101
+3	6	110
+4	7	111

5. In total 5 fan speed levels have been taken into consideration including the switched off state. The Fan speed levels/states and their respective encodings are given in the following table :

Fan Speed Level	State	Encoding
0 (switched off)	S_0	000
1	S_1	001
2	S_2	010
3	S_3	011
4 (maximum speed)	S_4	100
5	S_5	x (don't care)
6	S_6	x
7	S_7	x

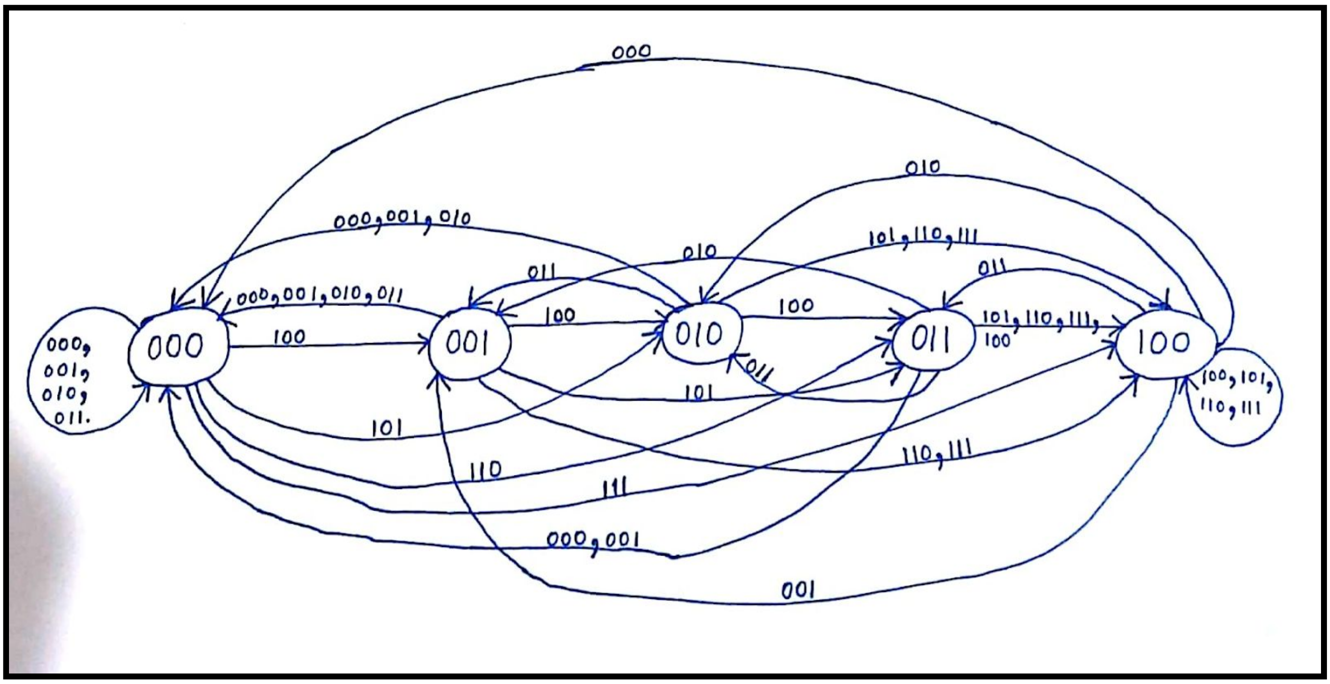
6. There are 4 variable fan speeds apart from the switched off state. We drive the fan with a "PWM Fan Drive Signal." It uses the relative width in a train of on-off pulses to control the speed.

7. The changes in temperature don't happen too quickly and the fan speed is readjusted every second.

8. The clock frequency we used for generating fan driving square pulses: 32 Hz.

State Diagram & State Table

Relative Temperature Level to Fan Speed FSM State Diagram:



The State Table below translates the given state diagram. 'ABC' denotes the state the FSM is in. The state table is implemented using three D flip flops namely A,B,C. XYZ denotes the temperature input level which ranges from 000 - 111 (corresponding to the -4 to +4 levels as stated in the question). The temperature levels are interpreted as the amount by which the fan speed level has to be increased or decreased to suit the required conditions. According to the given question the Fan has 4 speed levels apart from the switched off state. So three of the total eight states have been treated as don't care conditions.

Example of the mapping from relative temperature level to fan speed level :

Suppose the Fan is running at speed level 1 and the temperature input level is +3 (110), then the Fan speed level becomes 4 (1+3) in the next clock cycle. If the temperature input level was -1 (011), then the Fan speed level would have become 0 (1-1) in the next clock cycle.

STATE TABLE								
Present State(t)			Inputs			Next State(t+1)		
A	B	C	X	Y	Z	A	B	C
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0
0	0	0	0	1	0	0	0	0
0	0	0	0	1	1	0	0	0
0	0	0	1	0	0	0	0	1
0	0	0	1	0	1	0	1	0
0	0	0	1	1	0	0	1	1
0	0	0	1	1	1	1	0	0
0	0	1	0	0	0	0	0	0
0	0	1	0	0	1	0	0	0

0	0	1	0	1	0	0	0	0
0	0	1	0	1	1	0	0	0
0	0	1	1	0	0	0	1	0
0	0	1	1	0	1	0	1	1
0	0	1	1	1	0	1	0	0
0	0	1	1	1	1	1	0	0
0	1	0	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0
0	1	0	0	1	0	0	0	0
0	1	0	0	1	1	0	0	1
0	1	0	1	0	0	0	1	1
0	1	0	1	0	1	1	0	0
0	1	0	1	1	0	1	0	0

0	1	0	1	1	1	1	0	0
0	1	1	0	0	0	0	0	0
0	1	1	0	0	1	0	0	0
0	1	1	0	1	0	0	0	1
0	1	1	0	1	1	0	1	0
0	1	1	1	0	0	1	0	0
0	1	1	1	0	1	1	0	0
0	1	1	1	1	0	1	0	0
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	1
1	0	0	0	1	0	0	1	0
1	0	0	0	1	1	0	1	1

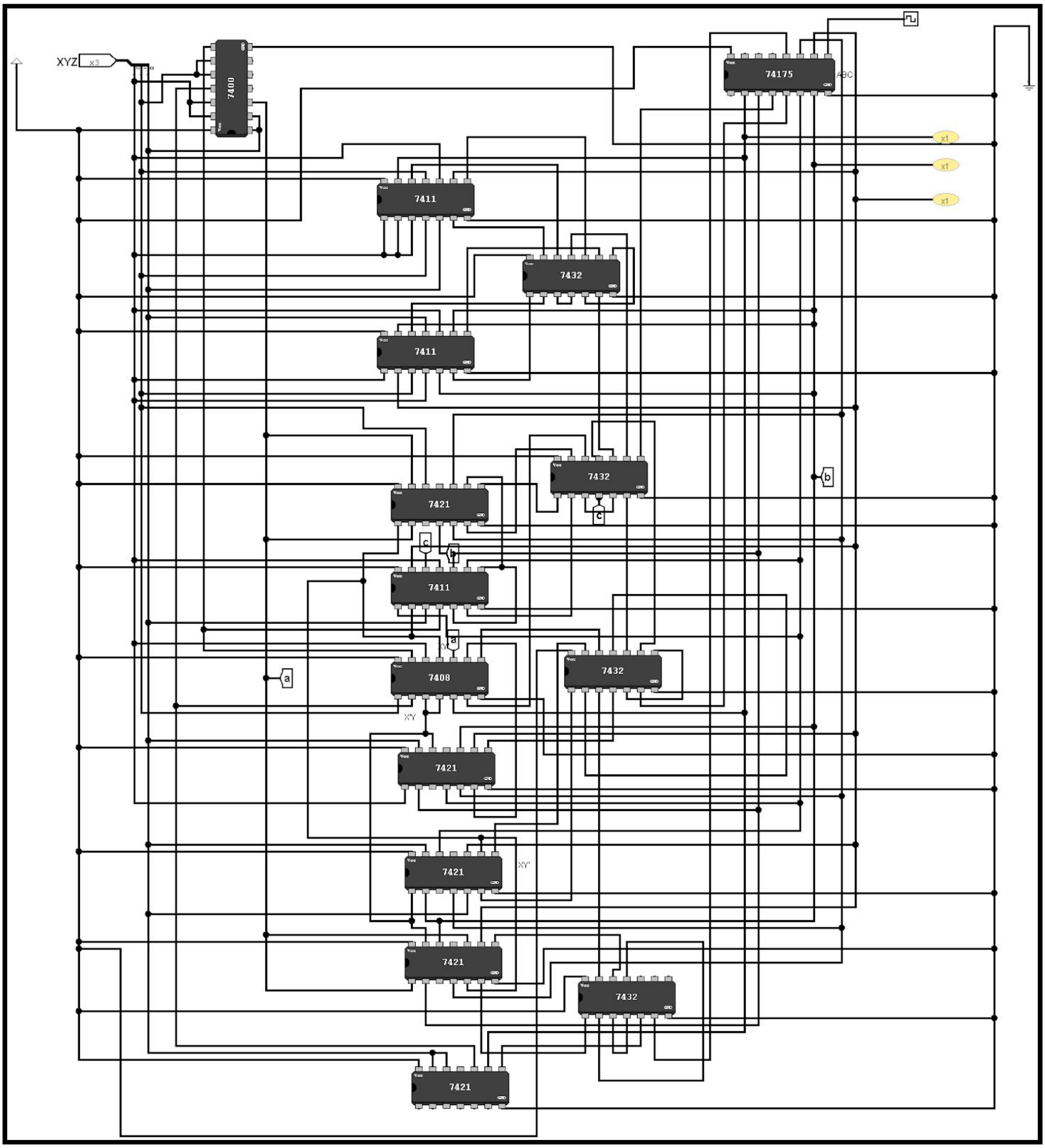
1	0	0	1	0	0	1	0	0
1	0	0	1	0	1	1	0	0
1	0	0	1	1	0	1	0	0
1	0	0	1	1	1	1	0	0
1	0	1	0	0	0	X	X	X
1	0	1	0	0	1	X	X	X
1	0	1	0	1	0	X	X	X
1	0	1	0	1	1	X	X	X
1	0	1	1	0	0	X	X	X
1	0	1	1	0	1	X	X	X
1	0	1	1	1	0	X	X	X
1	0	1	1	1	1	X	X	X
1	1	0	0	0	0	X	X	X

1	1	0	0	0	1	X	X	X
1	1	0	0	1	0	X	X	X
1	1	0	0	1	1	X	X	X
1	1	0	1	0	0	X	X	X
1	1	0	1	0	1	X	X	X
1	1	0	1	1	0	X	X	X
1	1	0	1	1	1	X	X	X
1	1	1	0	0	0	X	X	X
1	1	1	0	0	1	X	X	X
1	1	1	0	1	0	X	X	X
1	1	1	0	1	1	X	X	X
1	1	1	1	0	0	X	X	X
1	1	1	1	0	1	X	X	X

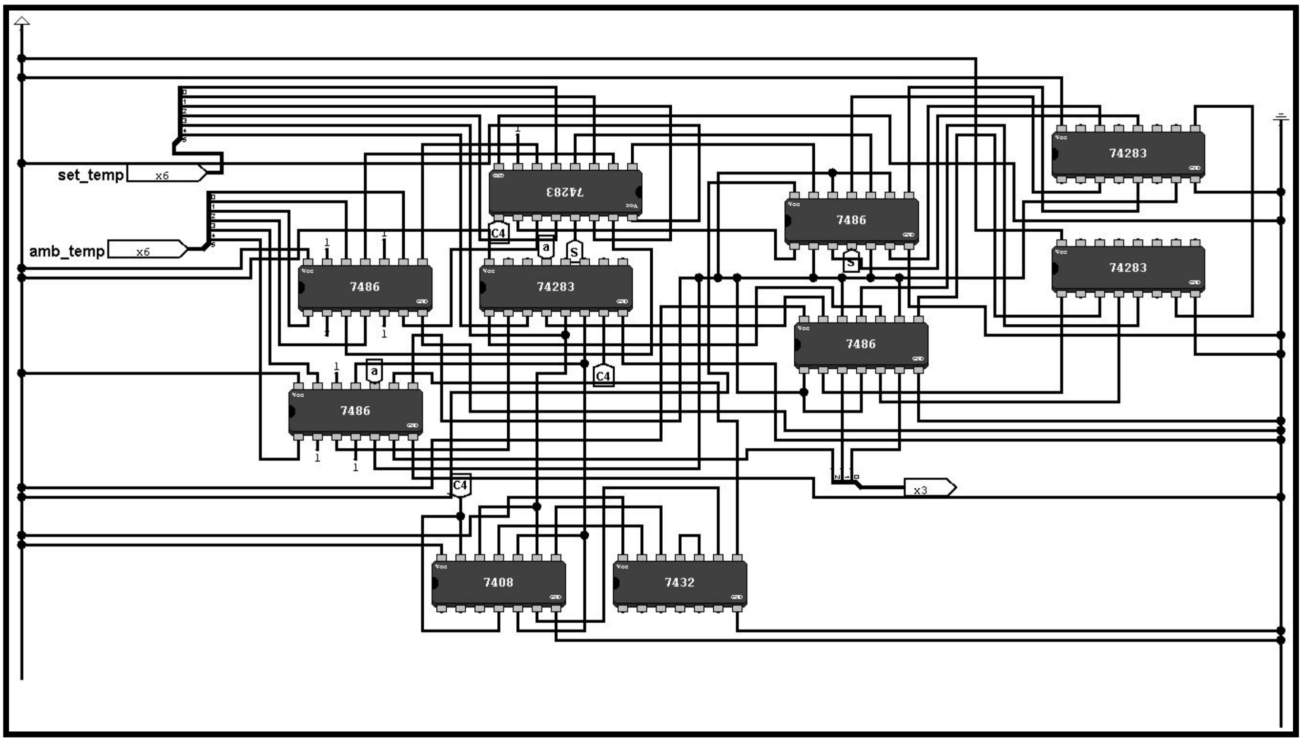
1	1	1	1	1	0	X	X	X
1	1	1	1	1	1	X	X	X

Pin Out Diagrams

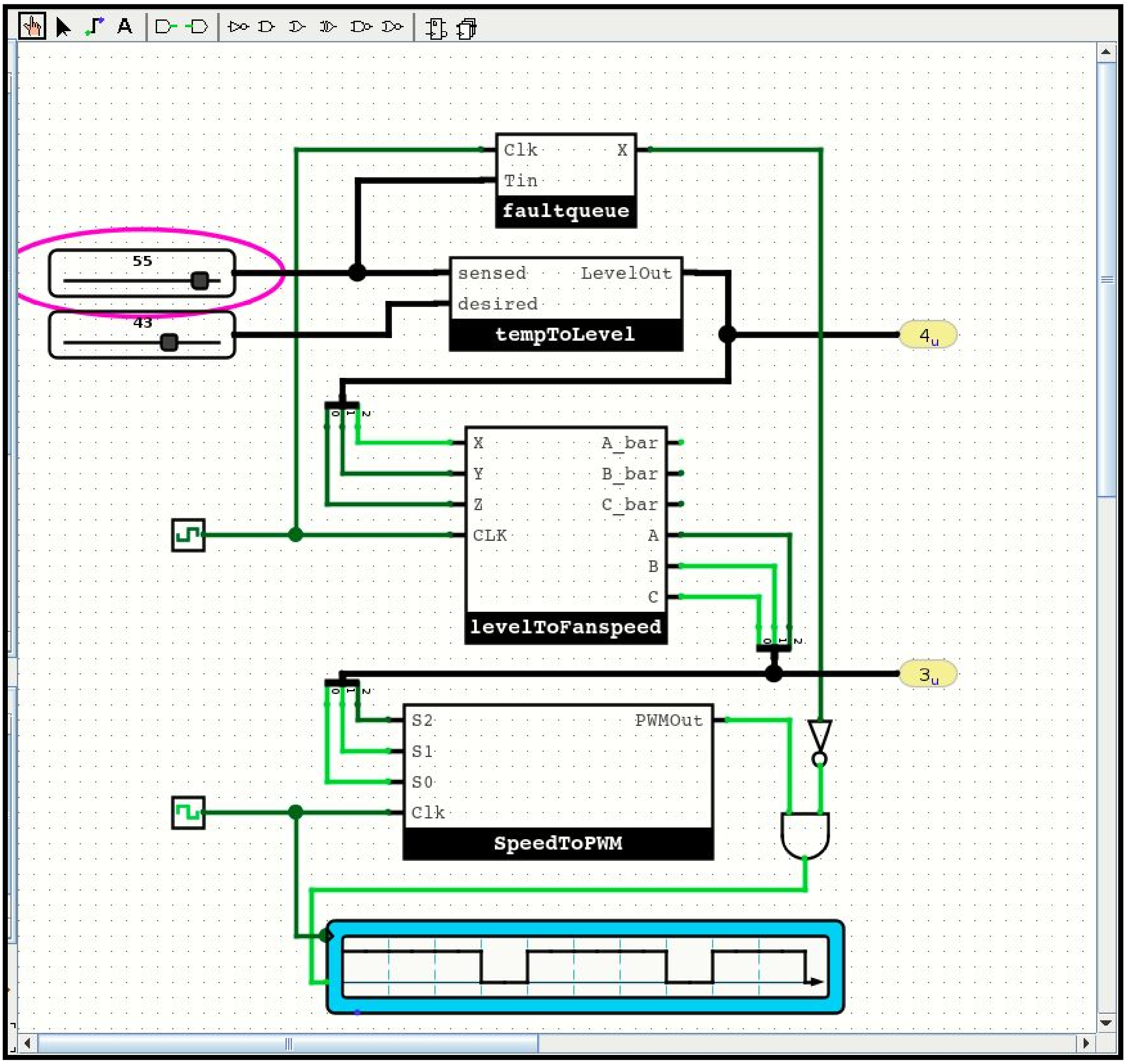
FSM mapping the relative temperature levels to the fan speed levels



Circuit mapping the real world temperature to relative temperature levels



Sample Simulation

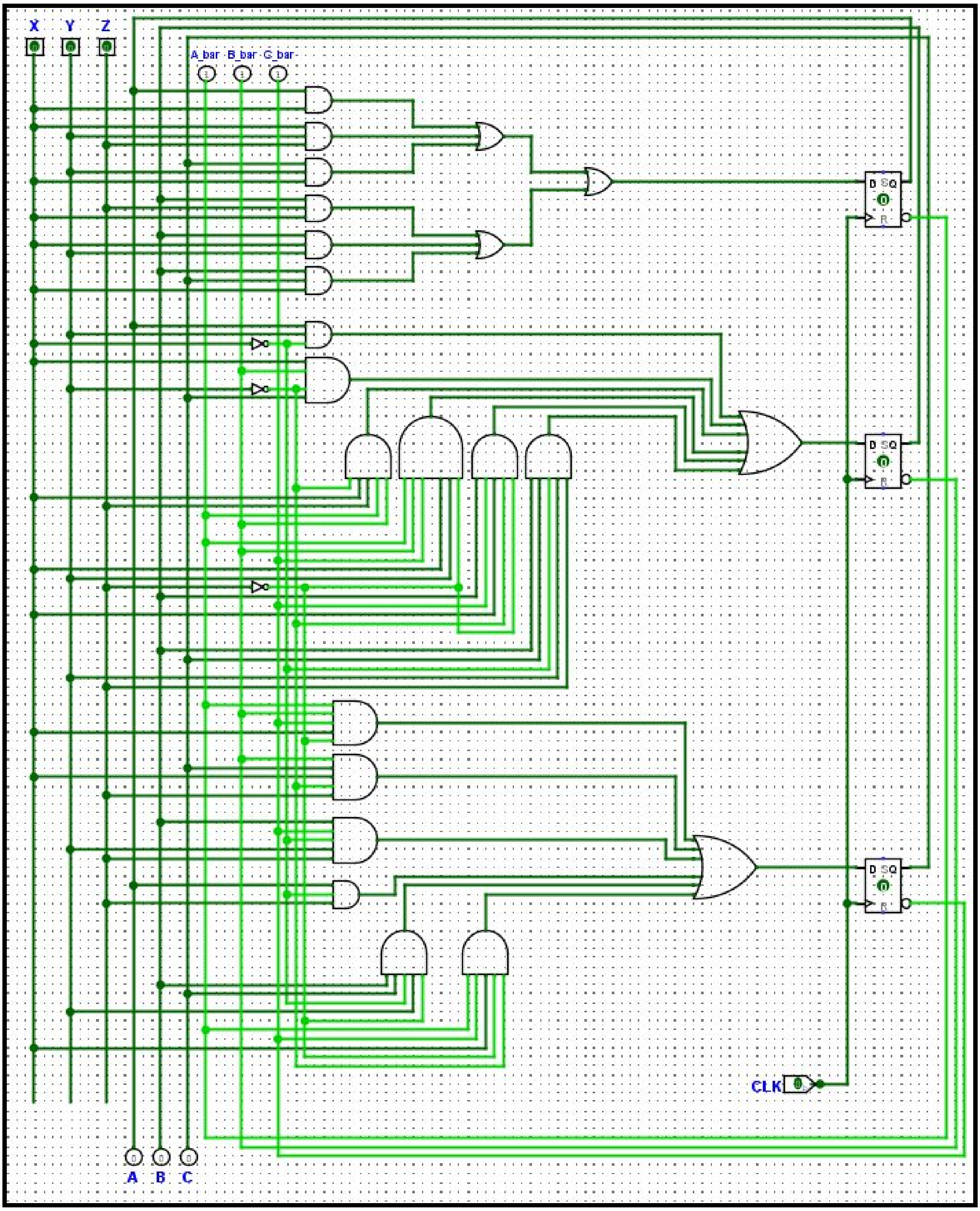


When the room is sensed to be (55 – 43 =) 12°C hotter than desired, we map that to a "+1" relative temperature disparity. The fan speed increases by 1 every second; the width of the driving square pulses grows accordingly.

The screenshot shows the circuit in fan speed 3 which corresponds to a 75% duty cycle. It keeps adjusting speed to minimise disparity between sensed and desired temperature.

Circuit Design

FSM mapping the relative temperature levels to the Fan speed levels



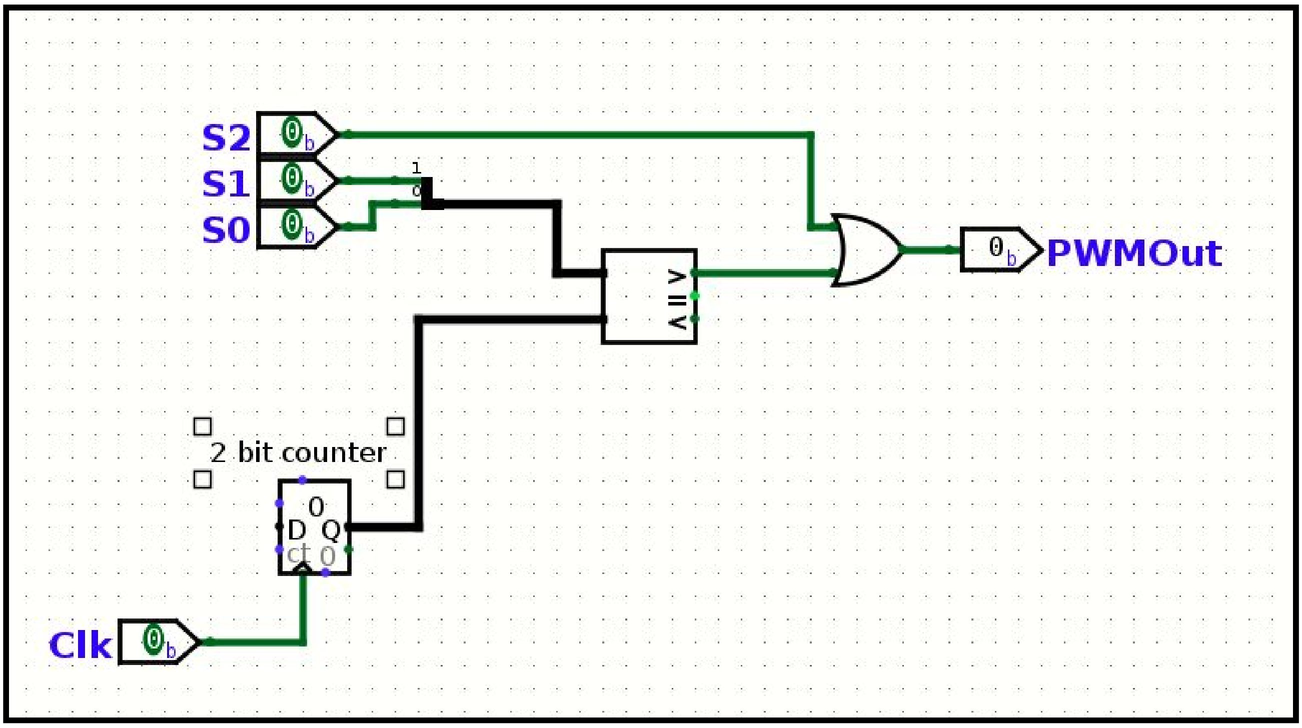
The circuit implements the aforementioned FSM specifications. The boolean expressions implemented by the three D flipflops are given as follows :

D_A = AX + XYZ + CXY + BXZ + BXY + BCX

D_B = AX'Y + B'CXY' + A'B'XY'Z + A'B'C'XYZ' + BC'XY'Z' + BCX'YZ

D_C = AX'Z + A'B'C'XZ' + B'CXY'Z + BC'X'YZ + BCX'YZ' + A'C'XY'Z'

Speed to PWM Fan Drive signal

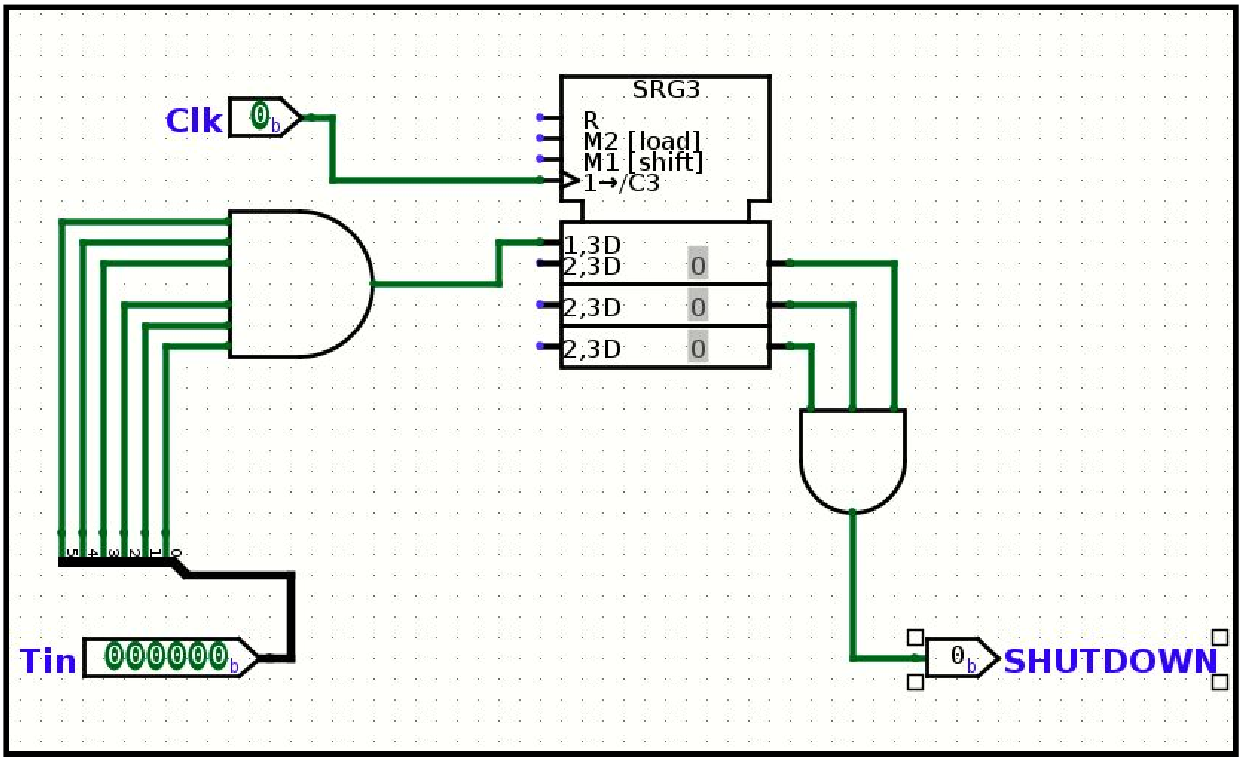


Inputs an unsigned 3-bit number representing fan speed 'S' and generates a square wave. Its width is 'S' clock cycles. The 2 bit counter generates 4 timing signals; the comparator checks the last two bits of input against count. If the first bit of the input is 1, then regardless of the comparator output, the output is always HIGH. So a speed of 2 means a 50% duty cycle; output stays HIGH for every 2 clock cycles in 4. For max speed 100_2 output is always HIGH. We added this to mimic PWM Drive Signal used to control 4-wire computer cooling fans. (See Ref 1)

Example:

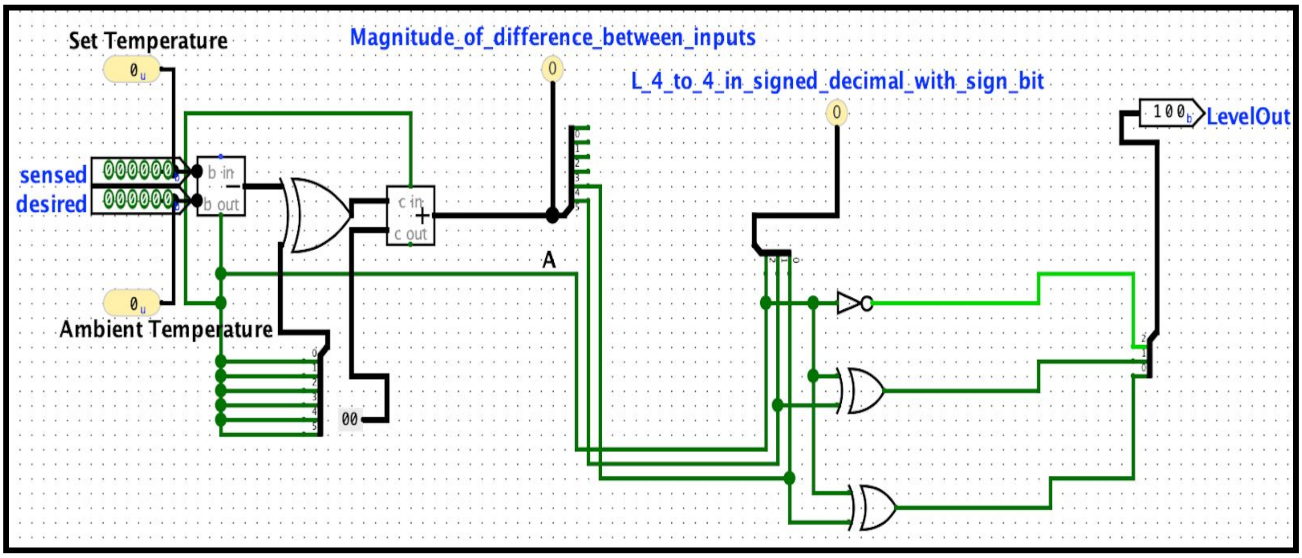
Counter	00	01	10	11
Speed (Last two bits)	10	10	10	10
Output	HIGH	HIGH	LOW	LOW

Fault Queue



The temperature sensed is taken as the input (Tin) and if all the bits are 1(corresponding to 63 degrees), the shift register shifts a 1 at each clock cycle. If the sensed temperature is 1 for 3 consecutive clock cycles(Register stores 111), the fan shuts down.

Temperature to Level



A subtractor outputs the difference between sensed temperature and desired temperature. If the difference is negative, it outputs the two's complement of the difference magnitude. So we xor it with the borrow and add borrow to the subtractor output, which essentially outputs the magnitude difference of the temperatures. We then map that to the four levels above and four levels below the temperature sensor input[-4,+4], which gets further mapped to [0,7]. 0 to 3 indicate the fan speed should be lowered, 4 to 7 indicate it to be increased.

Additional Functionalities

Fault Queue

When the sensed ambient temperature is maxed out for multiple clock cycles, which signifies an unnatural state of the room which could potentially ruin the circuit components due to high temperatures , the fan is stopped and a shutdown signal is generated.

Temperature Set

We let the user set a desired temperature. Then we compare it to the sensor input to calculate relative temperature levels and thus generate the 4 levels below and 4 levels above sensed temperature.

PWM Drive Output

Instead of outputting a number that presumably adjusts the fan's power supply voltage, we generate a PWM signal whose duty cycle controls the speed of the fan. (Square pulses whose width controls the duration for which the fan receives full voltage.)

Bill of Materials

IC	Description	Qty
7400	Quad 2-input NAND Gate	1
74175	HEX/QUADRUPLE D-Type Flip-Flops	1
7411	TRIPLE 3-INPUT AND GATE	3
7432	Quad 2-Input OR Gate	5
7421	DUAL 4-INPUT POSITIVE AND GATE	5
7408	Quad 2-Input AND Gates	2
7486	Quad 2-Input Exclusive-OR Gate	4
74283	4-BIT BINARY FULL ADDER WITH FAST CARRY	4

Appendix

References

1. http://www.digikey.pt/Web%20Export/Supplier%20Content/Maxim_175/pdf/Maxim_ThermalManagement.pdf (Pages 27 through 31)
2. Datasheets:

   http://web.mit.edu/6.131/www/document/7400.pdf

   [74175]: https://datasheetspdf.com/pdf-file/526285/ETC/74175/1

   http://ee-classes.usc.edu/ee459/library/datasheets/DM74LS11.pdf

   http://ee-classes.usc.edu/ee459/library/datasheets/DM74LS32.pdf

   https://www.digchip.com/datasheets/download_datasheet.php?id=3147103&part-number=7421

   https://www.electroschematics.com/wp-content/uploads/2013/07/7408-datasheet.pdf

   http://makeyourownchip.tripod.com/7486.pdf

   https://mil.ufl.edu/4712/docs/sn74ls283rev5.pdf

3. Mano, M. M. (2011). *Digital design*. Prentice Hall.