Design and Implementation of 6T SRAM Cell

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Abstract

Static Random Access (SRAM) constitutes a large percentage of area in the VLSI designs due to the high number of transistors for a single SRAM cell. Thus, the SRAM cell generally employs a minimum size transistor to have a high packing density. The main concern for SRAM cell design is stability. Stability of memory is affected by the aspect ratio of MOSFET and operating conditions. The aim of stability in memory is to operate it correctly. The measure of stability in the SRAM cell is Static Noise Margin (SNM). The proposed paper shows the implementation of an 6T SRAM Cell using CMOS Technology and the simulations of read mode of SRAM. The applied voltage is 1volt. eSim and Ngspice tool is used for the implementation with 130nm technology.

1. Reference Circuit Details

The architecture of the 6T SRAM Cell is shown in Figure 1. The architecture consists of two-cross coupled CMOS inverters P1-N1 and P2-N2 used for storing a bit, and two access transistors N3-N4 used for performing read and write operations. The access transistors are activated/deactivated using the word line (WL). The bit line acts as input while performing the read operation.

An SRAM cell works in different states: standby where the circuit is idle, reading when the data has been requested and writing when updating the data. The SRAM to operate in read mode and write mode should have "readability". The different states work as follows

> Standby: If the word line is not asserted, the access transistors N3 and N4 disconnect the cell from the bit lines. The two cross coupled inverters formed by P1-N1, P2-N2 will continue to reinforce each other as
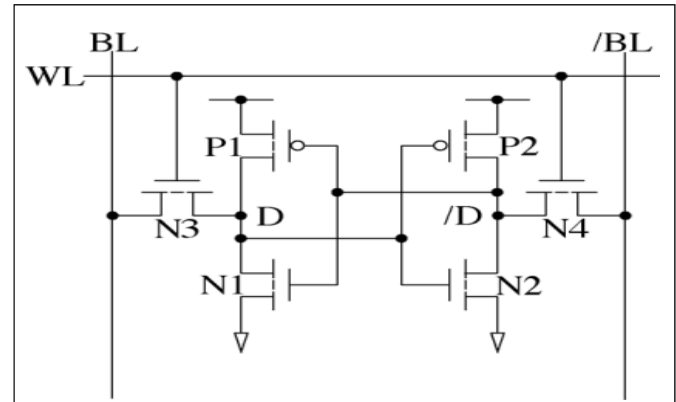
2. Reference Circuit

Figure 1. Conventional 6T SRAM Cell

3. Reference Circuit Waveforms

Figure 2. Reference Waveforms

References

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[2]. Design of Read and Write Operations for 6t Sram Cell https://www.iosrjournals.org/iosr-jvlsi/papers/vol8-issue1/Version-1/E0801014346.pdf