**Registers:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **$s0** | **$s1** | **$s2** | **$s3** | **$s4** | **$s5** | **$s6** | **$s7** |
| 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **$t0** | **$t1** | **$t2** | **$t3** | **$t4** | **$t5** | **$t6** | **$t7** |
| 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |

**R – Type Instructions:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| OP Code | First operand / first register | 2nd operand / second register | Destination | Shift | function |

6 bits 5 bits 5 bits 5bits 5 bits 6 bits

* Add
* Sub
* SRL (shift right logic)
* SLL (shift left logic)

**Add $s0, $t1,$t2**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 9 | 10 | 16 | 0 | 32 |
| 000000 | 0 1001 | 0 1010 | 1 0000 | 00000 | 10 0000 |

**Sub $s0, $t1, $t2**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 9 | 10 | 16 | 0 | 34 |
| 000000 | 0 1001 | 0 1010 | 1 0000 | 00000 | 10 0100 |

**$srl $t0, $t1, 2 # $t0 = $t1/4;**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 0 | 9 | 8 | 2 | 2 |
| 000000 | 0 | 0 1001 | 0 1000 | 00010 | 00 0010 |

**$sll $t0, $t1, 2 # $t0 = $t1\*4;**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 0 | 9 | 8 | 2 | 0 |
| 000000 | 0 | 0 1001 | 0 1000 | 00010 | 00 0000 |

**$slt $t0,$s3,$s4 (if $s3<$s4) (Set Less than)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 19 | 20 | 8 | 0 | 42 |
| 000000 | 1 0011 | 1 0100 | 0 1000 | 00000 | 10 1010 |

**$slti $t0,$s2,10 (if $s2<10) (Set Less than Immediate) I type**

|  |  |  |  |
| --- | --- | --- | --- |
| 10 | 18 | 8 | 10 |
| 00 1010 | 1 0010 | 0 1000 | 0000 0000 0000 1010 |

**I – Type Instructions:**

|  |  |  |  |
| --- | --- | --- | --- |
| OP Code | Base Address | Destination | Constant / Offset |

6 bits 5 bits 5 bits 16 bits

* Lw
* Sw
* Beq
* Bne
* Addi

**Lw $t0, 64($s0)**

|  |  |  |  |
| --- | --- | --- | --- |
| 35 | 16 | 8 | 64 |
| 10 0101 | 1 0000 | 0 1000 | 0000 0000 0100 0000 |

**Sw $t0, 64($s0)**

|  |  |  |  |
| --- | --- | --- | --- |
| 43 | 16 | 8 | 64 |
| 10 1011 | 1 0000 | 0 1000 | 0000 0000 0100 0000 |

**Addi $s0, $s1, 8**

|  |  |  |  |
| --- | --- | --- | --- |
| 8 | 17 | 16 | 8 |
| 00 1000 | 1 0001 | 1 0000 | 0000 0000 0000 1000 |

**beq $s0, $s1, Loop**

|  |  |  |  |
| --- | --- | --- | --- |
| OP Code | Register 1 | Register 2 | Address |

|  |  |  |  |
| --- | --- | --- | --- |
| 4 | 16 | 17 | 123 (Loop Address) |
| 00 0100 | 1 0000 | 1 0001 | 0000 0000 0111 1011 |

**bne $s0, $s1, Loop**

|  |  |  |  |
| --- | --- | --- | --- |
| 5 | 16 | 17 | 123 (Loop Address) |
| 00 0101 | 1 0000 | 1 0001 | 0000 0000 0111 1011 |

