

**REPORT**  
**ON**  
**“NUMEROUS CIRCUIT SIMULATION”**

Submitted in partial fulfilment of the requirements for the partial completion of  
**ANALOG INTEGRATED CIRCUITS**  
**IN**  
**ELECTRONICS AND COMMUNICATION ENGINEERING**

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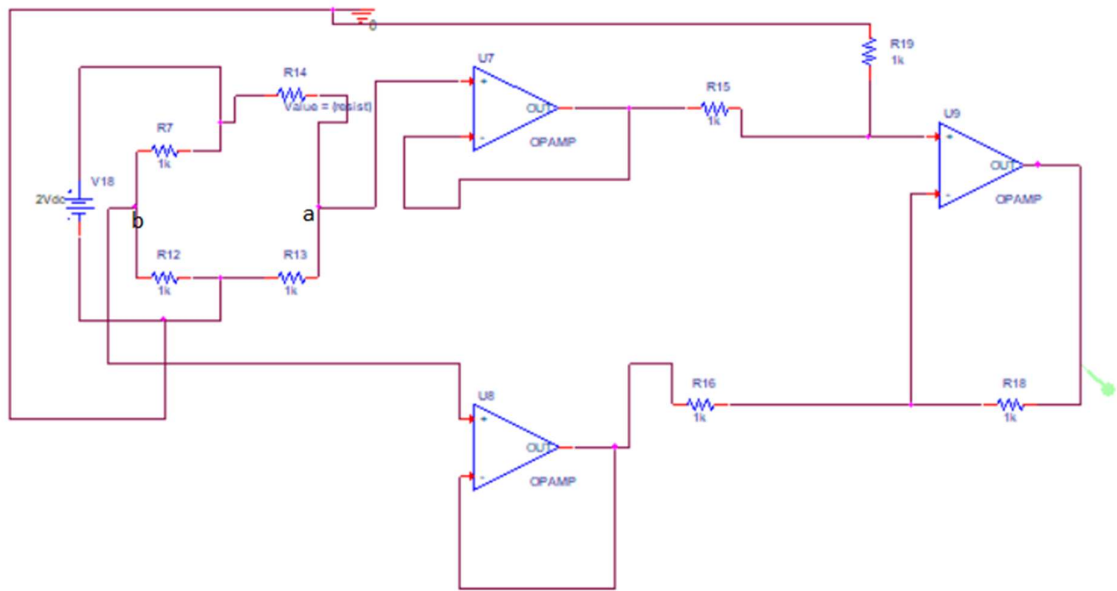
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## **CONTENTS:**

- 1. Instrumentation amplifier.**
- 2. Voltage regulator.**
- 3. Sample and hold.**
- 4. Multiplier.**
- 5. Divider.**

## CIRCUIT 1: INSTRUMENTATION AMPLIFIER USING TRANSDUCER BRIDGE



Above figure shows a simplified differential instrumentation amplifier using a transducer bridge. A resistive transducer whose resistance changes as a function of some physical energy is connected in one arm of the bridge (R14). The bridge is dc excited. For the balanced bridge at some reference condition,

$$V_b = V_a$$

$$R7/R12 = R14/R13$$

Generally, resistors for the bridge is selected so that they are equal in value to the transducer resistance. As the physical quantity to be measured changes, the resistance of the transducer also changes, which causes the bridge to be unbalanced, the output voltage of the bridges can be expressed as a function of the change in resistance of the transducer. Let the change in resistance of the transducer be  $\Delta R$ . Since R7 and R12 are fixed resistor, the voltage  $V_b$  is constant. However voltage  $V_a$  varies as a function of change in transducer resistance. Therefore

$$V_a = R13 (V_{dc}) / (R13 + (R14 + \Delta R))$$

$$V_b = R12(V_{dc})/(R7 + R12)$$

Consequently, the voltage  $V_{ab}$  across the output terminals of the bridge is

$$V_{ab} = V_a - V_b$$

If  $R7=R12=R14=R13=R$ , then

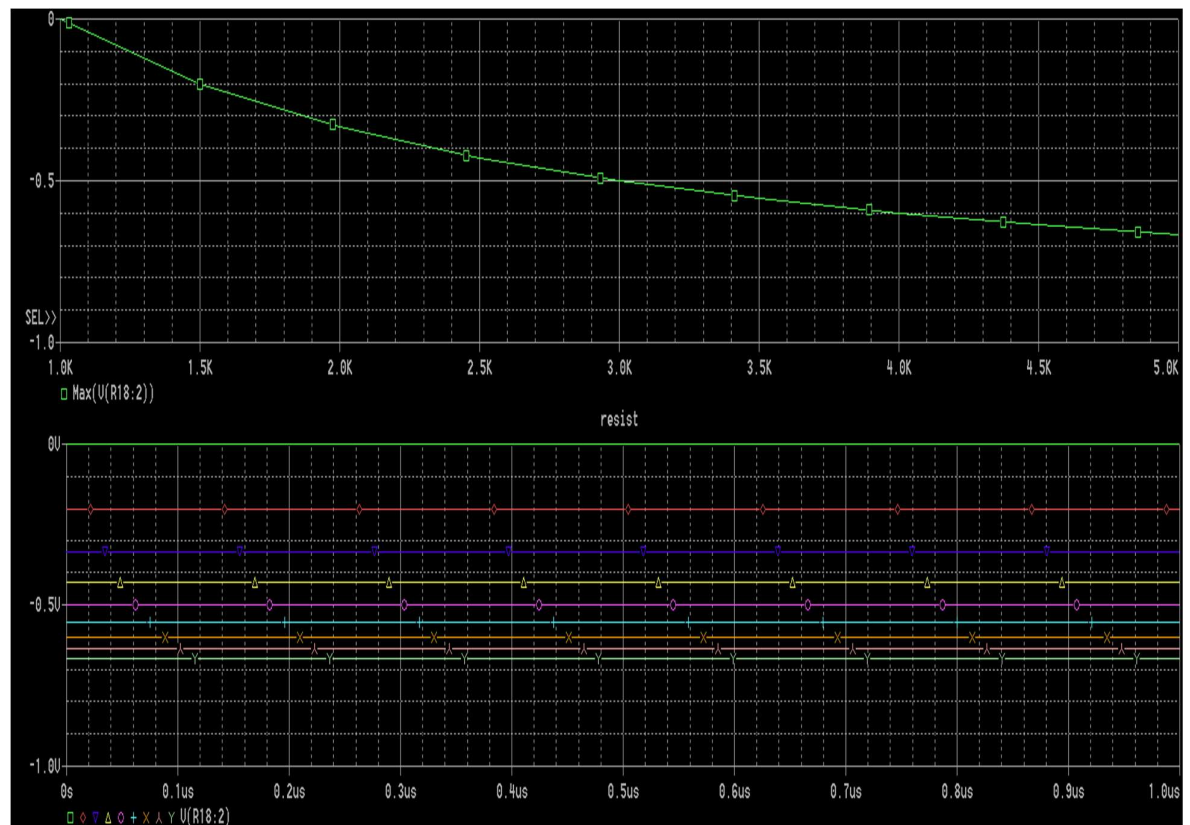
$$V_{ab} = \Delta R (V_{dc}) / 2(2R + \Delta R)$$

The output voltage  $V_{ab}$  of the bridge is then applied to differential instrumentation amplifier composed of three opamps. The voltage followers help to eliminate loading of the bridge circuit. The gain of the basic differential amplifier is  $(-R_{18}/R_{16})$ . Therefore the output  $V_o$  of the circuit is

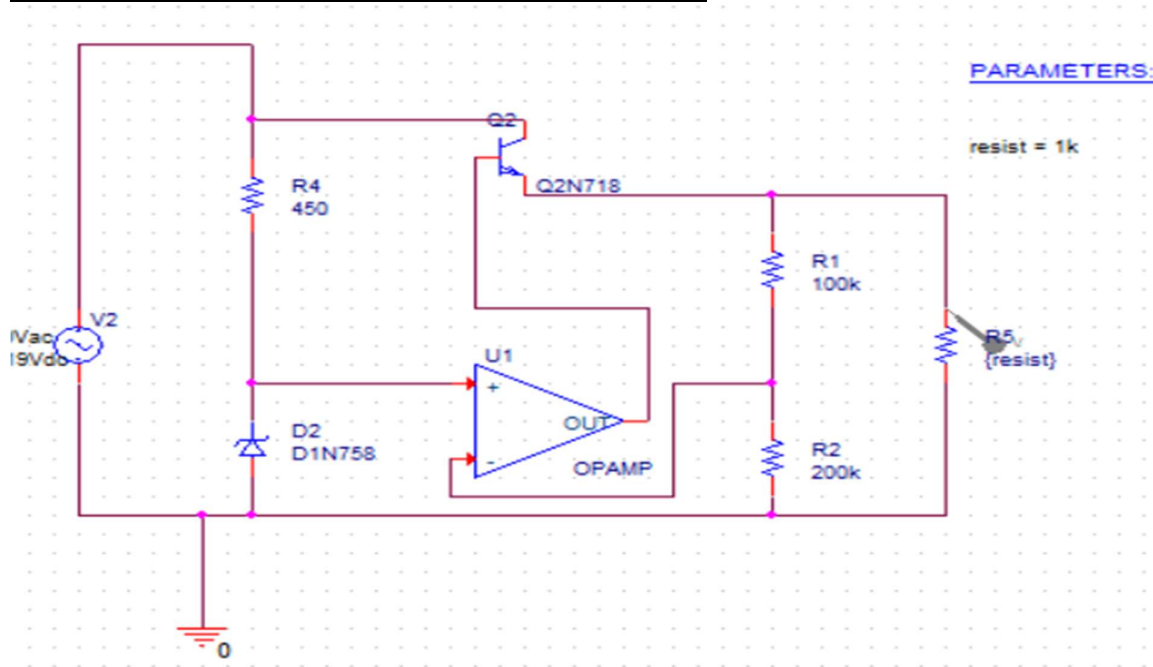
$$\begin{aligned} V_o &= V_{ab} (-R/R_1) = (\Delta R) V_{dc} / 2(2R + \Delta R) (R_{18}/R_{16}) \\ &= (R_{18}/R_{16}) (\Delta R) / 4R V_{dc} \end{aligned}$$

### **SIMULATION OUTPUT:**

The resistance value of  $R_{14}$  is changed from 1k to 5k ohm and the output is shown below.



## CIRCUIT 2: VOLTAGE REGULATOR



The above circuit is voltage regulator designed for 15V output with a maximum load current 50mA.

DESIGN:

$$V_i(\min) = V_o + 3V = 18V$$

Assuming the ripple voltage 2V(max), the input voltage is  $V_i(\min) = 19V$   
 Then  $V_z = V_i/2 = 9.5V$  (1N758)

Therefore,  $V_z = 10V$  and  $I_z \gg 20mA$

$$R4 = V_i - V_z / I_z = 19 - 10 / 20 \times 10^{-3} = 450 \text{ ohm}$$

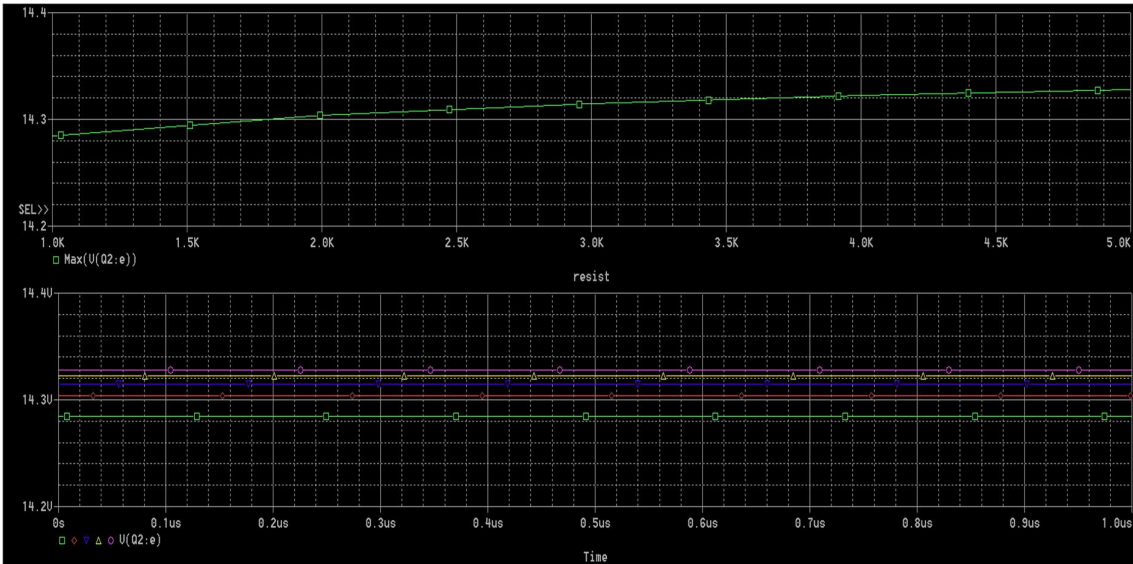
Let  $I_2$  through  $R1$  and  $R2$  be 50microA

$$R1 = V_o - V_z / I_2 = 15 - 10 / 50 \times 10^{-6} = 100k\text{ohm}$$

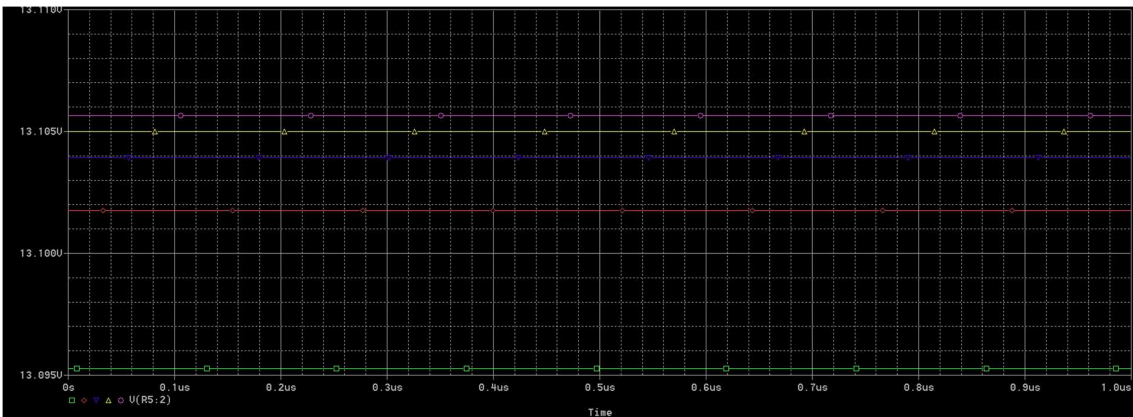
$$R2 = V_z / I_2 = 10 / 50 \times 10^{-6} = 200k\text{ohm}$$

# SIMULATION RESULTS:

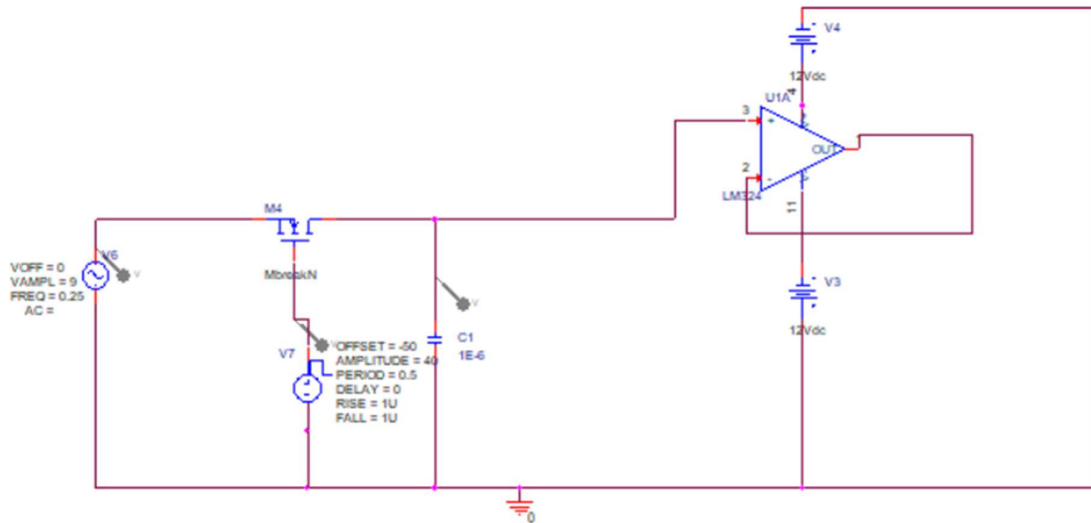
The load resistance R5 is varied till 5k ohm and output is as shown in the 1<sup>st</sup> figure



Output when input is less than 19v(for 13v input).

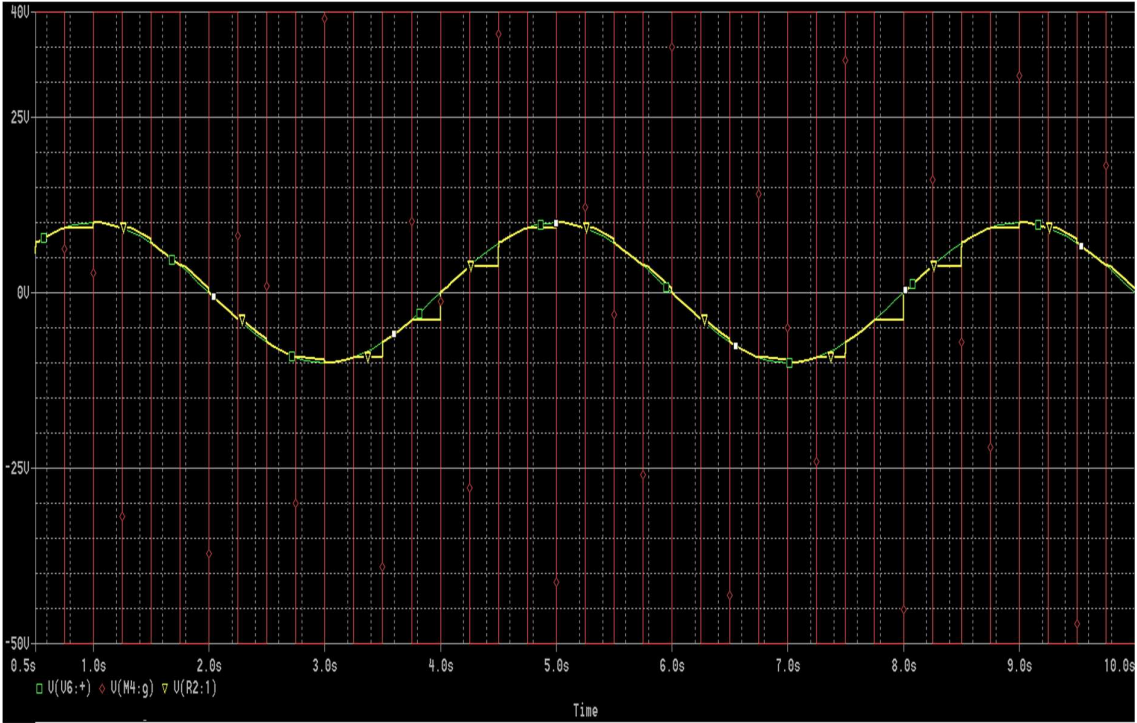


### CIRCUIT 3: SAMPLE AND HOLD



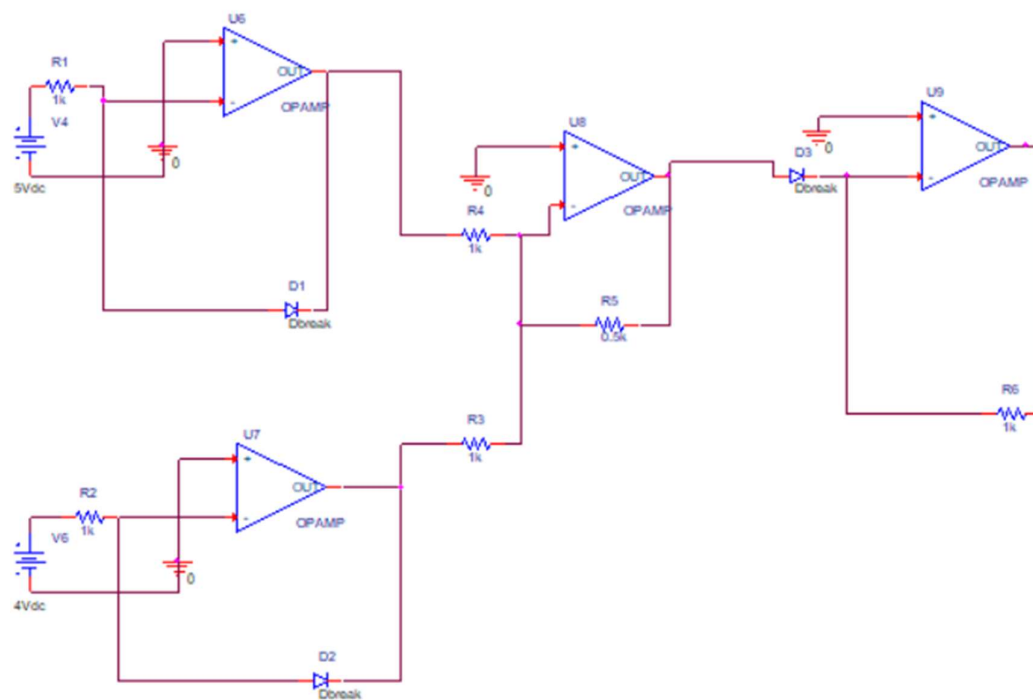
- The frequency of the input voltage is 0.25 hertz and its time period will be 4s.
- The time period of control signal is 0.5s.
- Since the signal is sampled when control signal is negative or zero, there would be 8 samples for a period of input signal.
- Since the minimum sampling for a signal is 2, hence sampling has been done more than that.
- The simulation output is as shown below.

**SIMULATION RESULT:**





## CIRCUIT 4: MULTIPLIER



Multiplier circuit gives the scaled value of the product of the input voltages. Above circuit consist of 2 log op-amp at the input which is followed by a op-amp which carries out addition. The output from this is given to anti-log op-amp to get the required output.

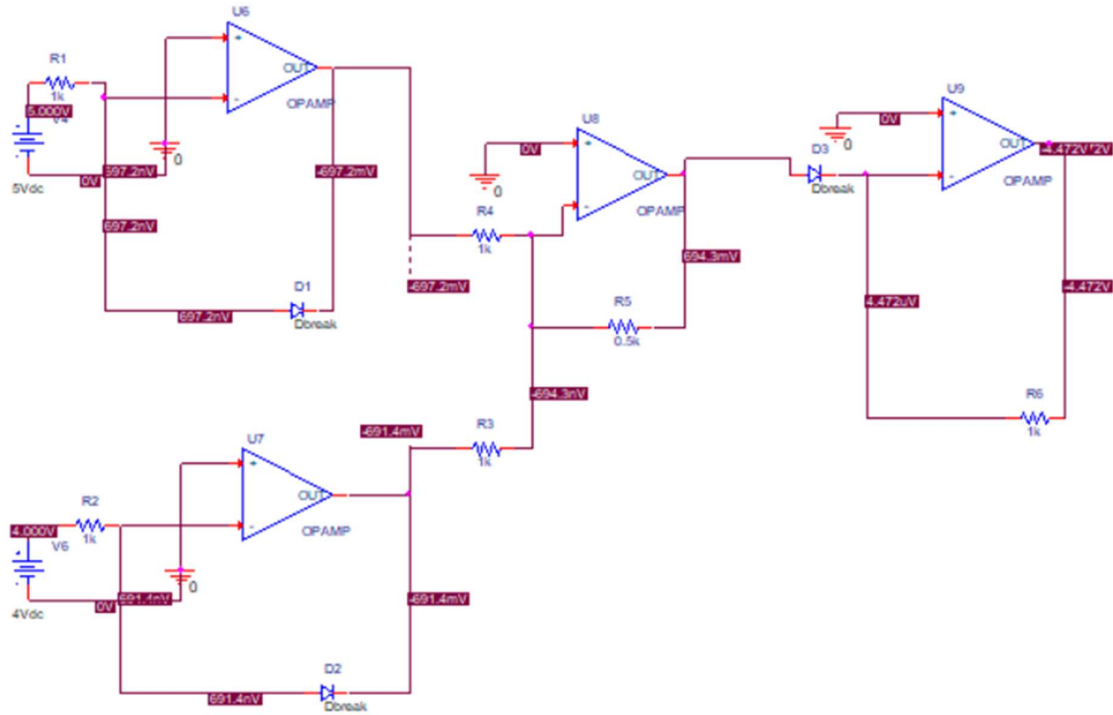
According to the circuit designed above the output expression is ,

$$V_o = - (V_4 \times V_6)^{0.5} V$$

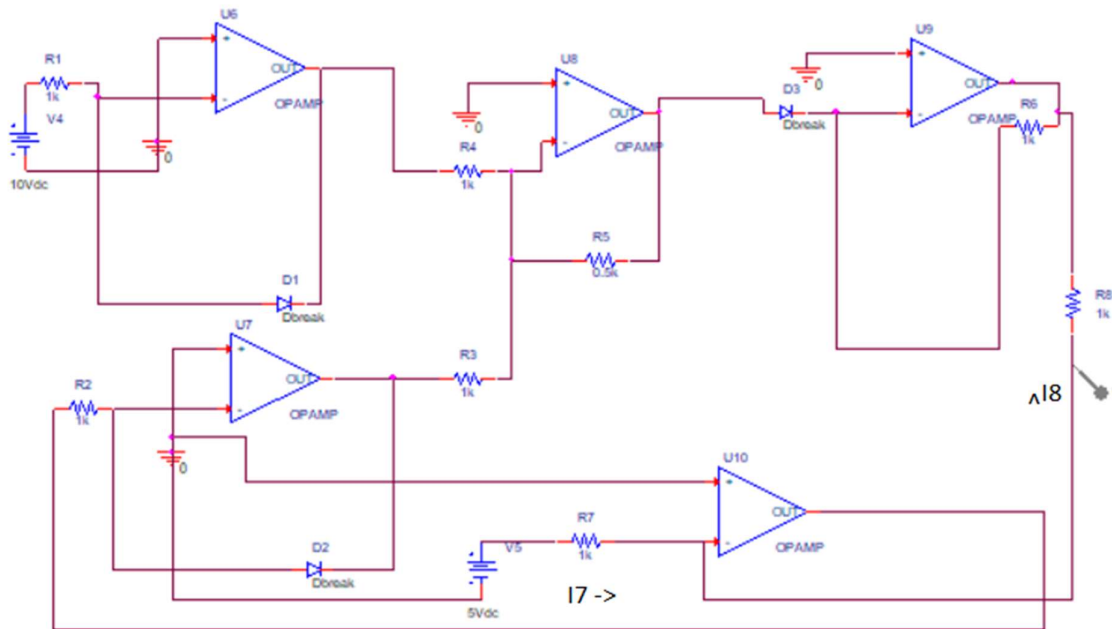
As u can see the circuit designed above gives root of the product of the input voltages. It is so because of the 0.5k (R5) ohm resistor used. The circuit was getting saturated for resistance values above 0.5k ohm.

## SIMULATION RESULTS:

The output of the circuit when input voltages are 4v and 5v is -4.472V.



## CIRCUIT 5: DIVIDER



The divider circuit consist of a multiplier circuit whose one of the input is connected to output of an op-amp circuit as shown in the above figure.

Design:

Multiplier circuit is same as the one used before so its output will be  $(\text{product of the input})^{0.5}$ . From the circuit it can be said that  $I7=I8$

$$I8 = \text{output of multiplier} / R$$

$$= -(V4 \times V_o)^{0.5} / R8$$

$$V5 = I7 \times R7$$

$$V5 = -(V4 \times V_o)^{0.5} / R8 \times R7$$

$$R8 \text{ and } R7 \text{ are equal so, } V_o = V5^2 / V4$$

Keeping  $V4 = X \text{ times } V5$  we can divide the input voltage by X. Where X is a positive integer.

**SIMULATION RESULTS:**

Here the value of X is 2 times input , i.e  $2 \times 5$ . The corresponding output is 2.478V.

