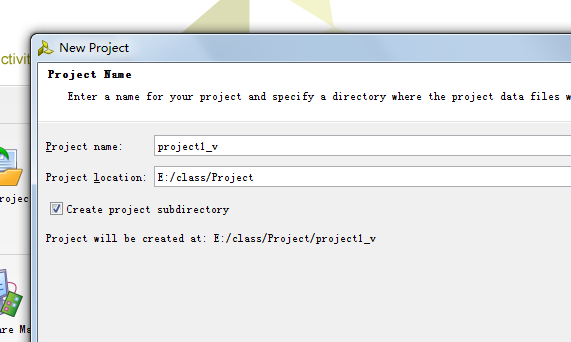
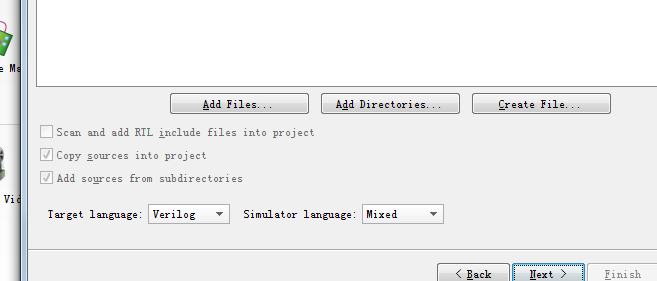
# LABI\_Verilog

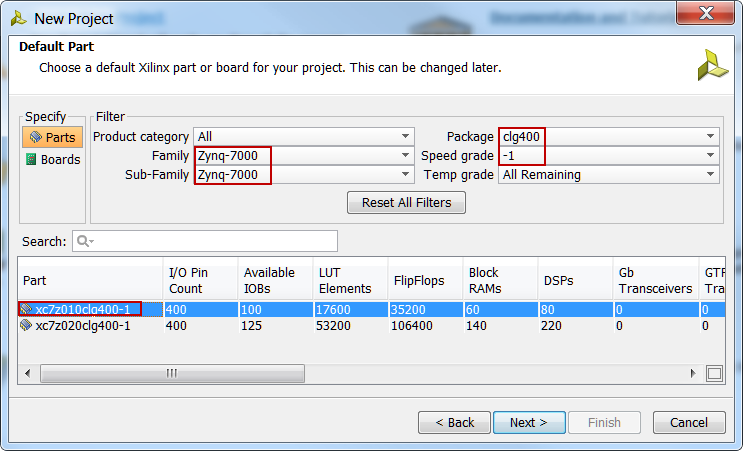
I·建立工程



选择verilog语言

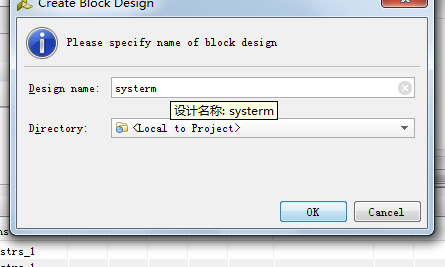


选择模块设置

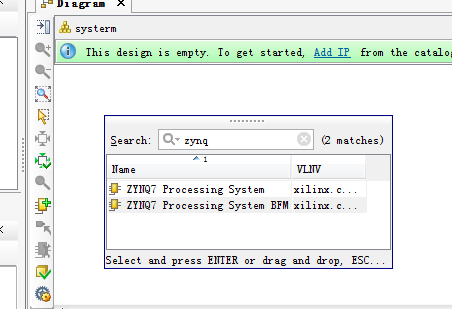


II·设置IP内核

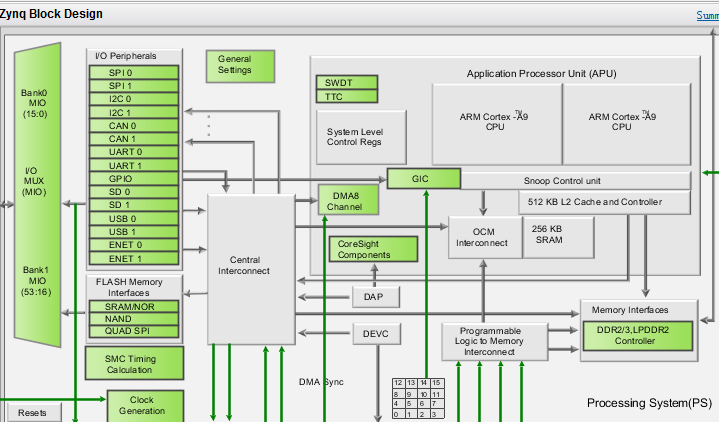
添加IP



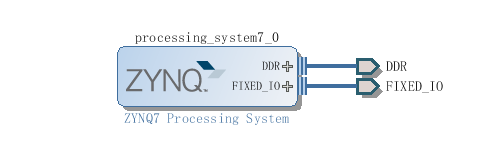
选择zynq7



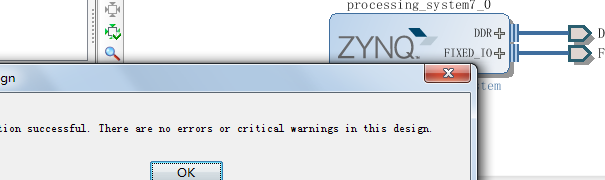
设置ip借口



添加uart1，其余借口全部和谐掉

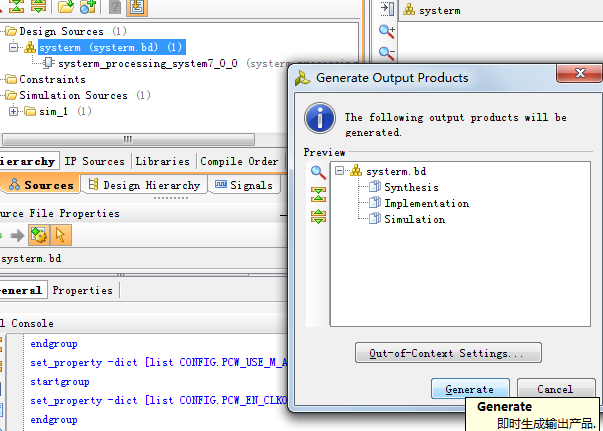


Ip设计完成

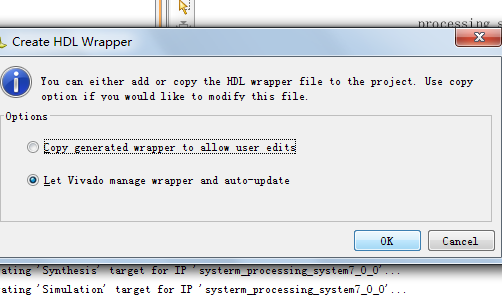


III·连线并添加进sdk

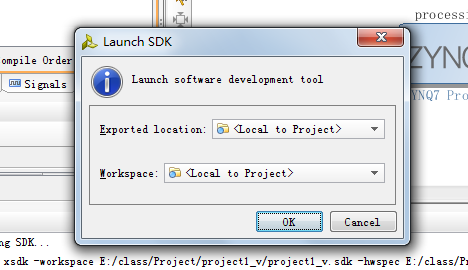
文件生成



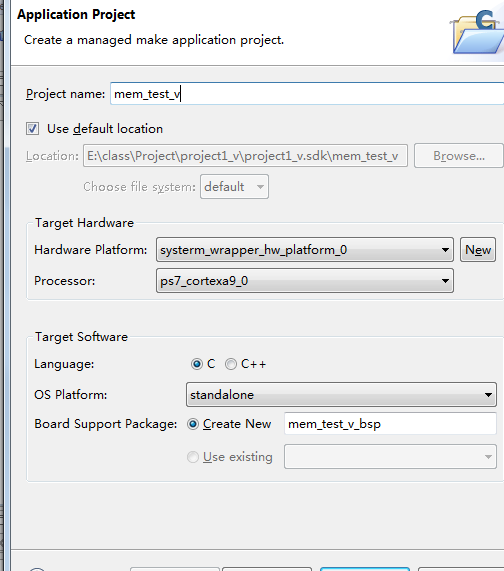
建立连线



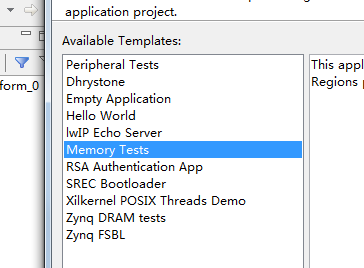
导入到sdk中



建立项目



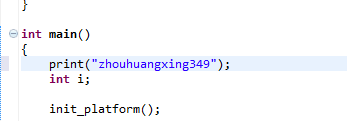
选择内存测试代码



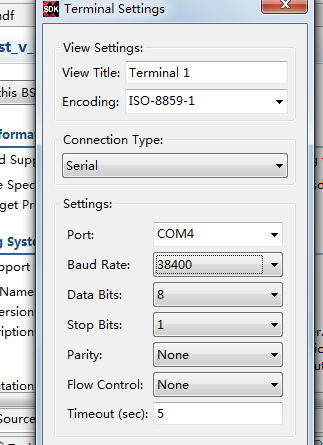
项目建立完成

IV·机器测试

添加代码段



设置串口



运行