


Combinational circuits

↳ Adder

↳ Subtractor

↳ Encoder

↳ Decoder

Logic Gates

AND

OR

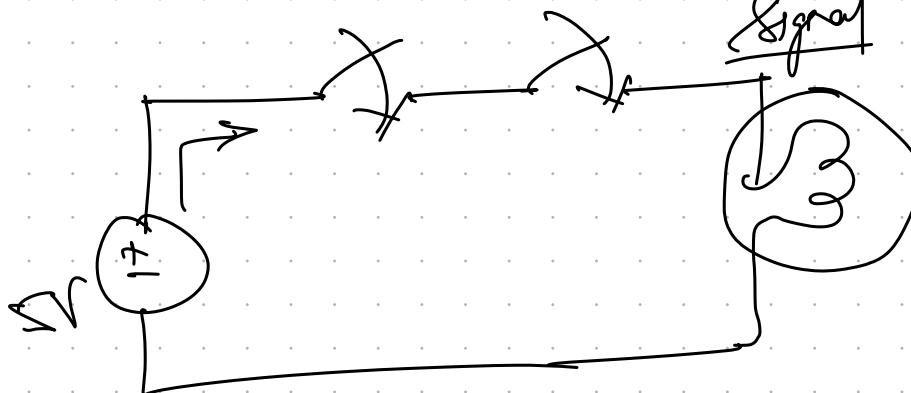
NOT

NAND

EX-OR

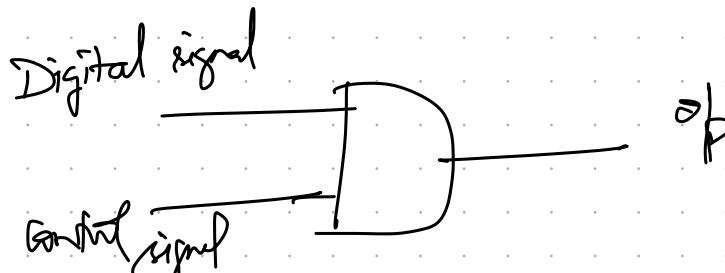
NOR

AND



| A | B | Op |
|---|---|----|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Application



$$Y = AB$$

IC 7408

IC 7409

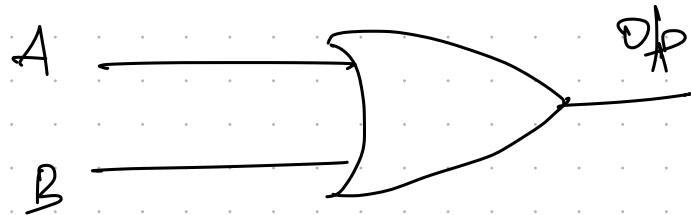
IC 7411

IC 7421

$$Y = ABCD$$

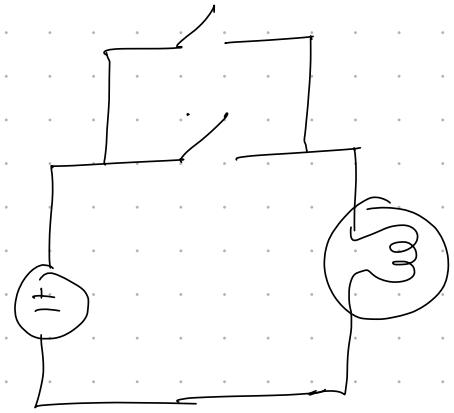
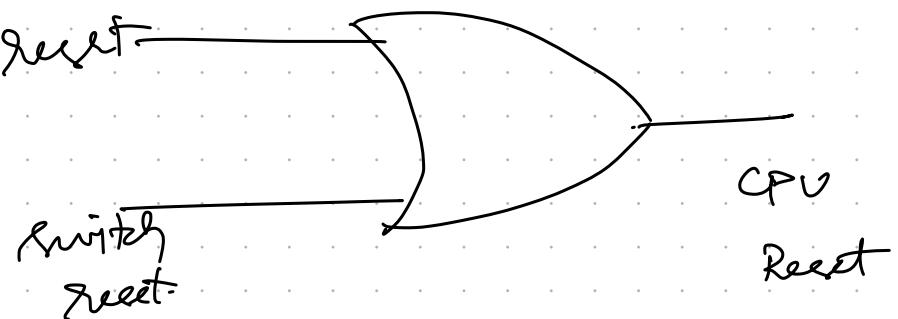
$$Y = ABC$$

OR

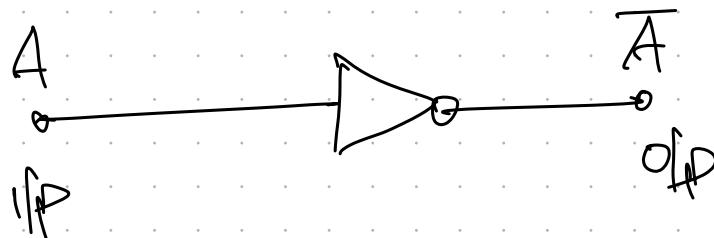


| A | B | D/P |
|---|---|-----|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Power on
reset



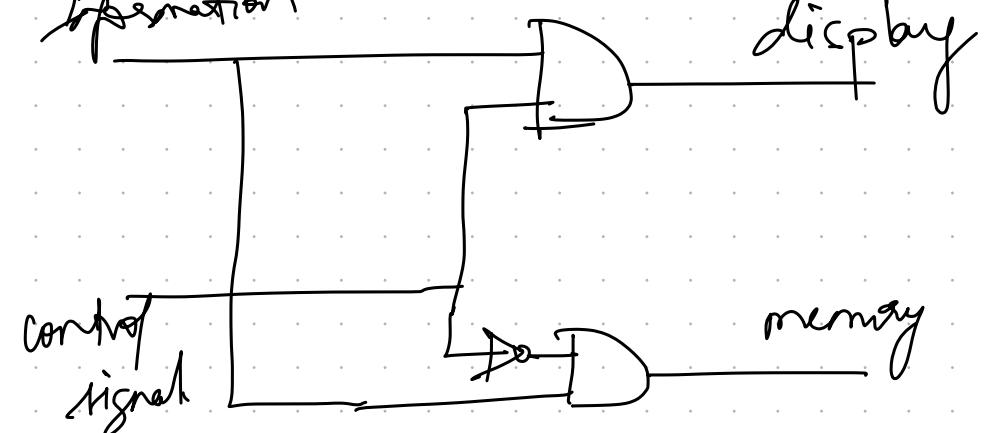
NOT



| A | O/P |
|---|-----|
| 0 | 1 |
| 1 | 0 |

Inverter gate Inhibitor

operation



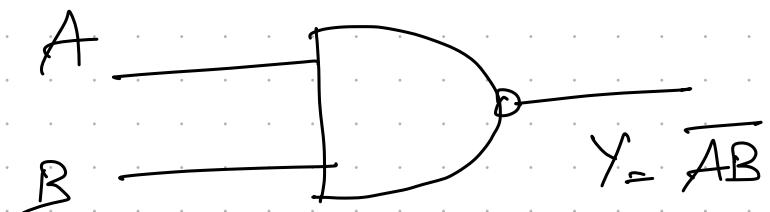
T_C 7404 }
7405 }

7406 }
7416 } → high voltage
o/p

NAND gate

2 OR more \rightarrow 2Ps

Only one - 0P



IC 7400 2Dp

A B 0P

0 0 1

0 1 1

1 0 1

1 1 0

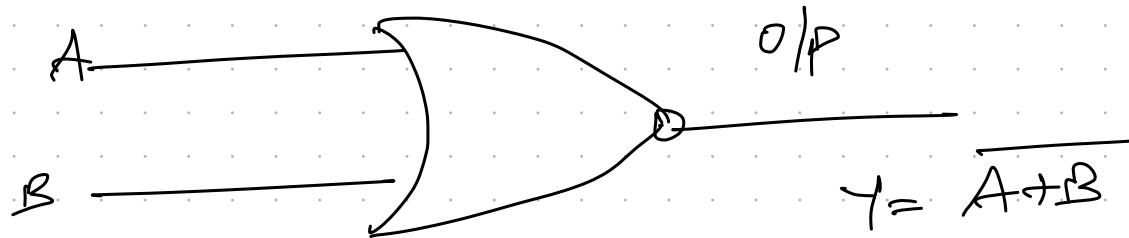
IC 7410 \rightarrow 8P

IC 7420 \rightarrow 4Dp

IC 7430 \rightarrow 8P

IC 74133 \rightarrow 13P

NOR gate



IC 7402 \rightarrow 2²p

IC 7425 \rightarrow 1²p

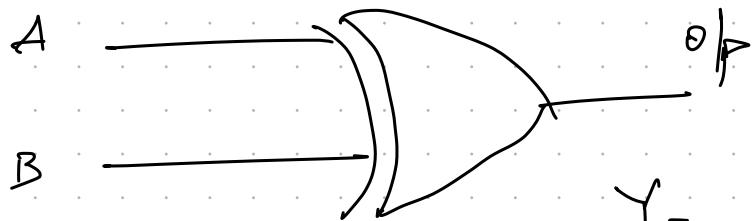
IC 7427 \rightarrow 3²p

IC 74260

↓
5 2²p.

| A | B | O/P |
|---|---|-----|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Eg - OR



$$Y = \bar{A}B + A\bar{B}$$

$$Y = A \oplus B$$

| A | B | OP |
|---|---|----|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

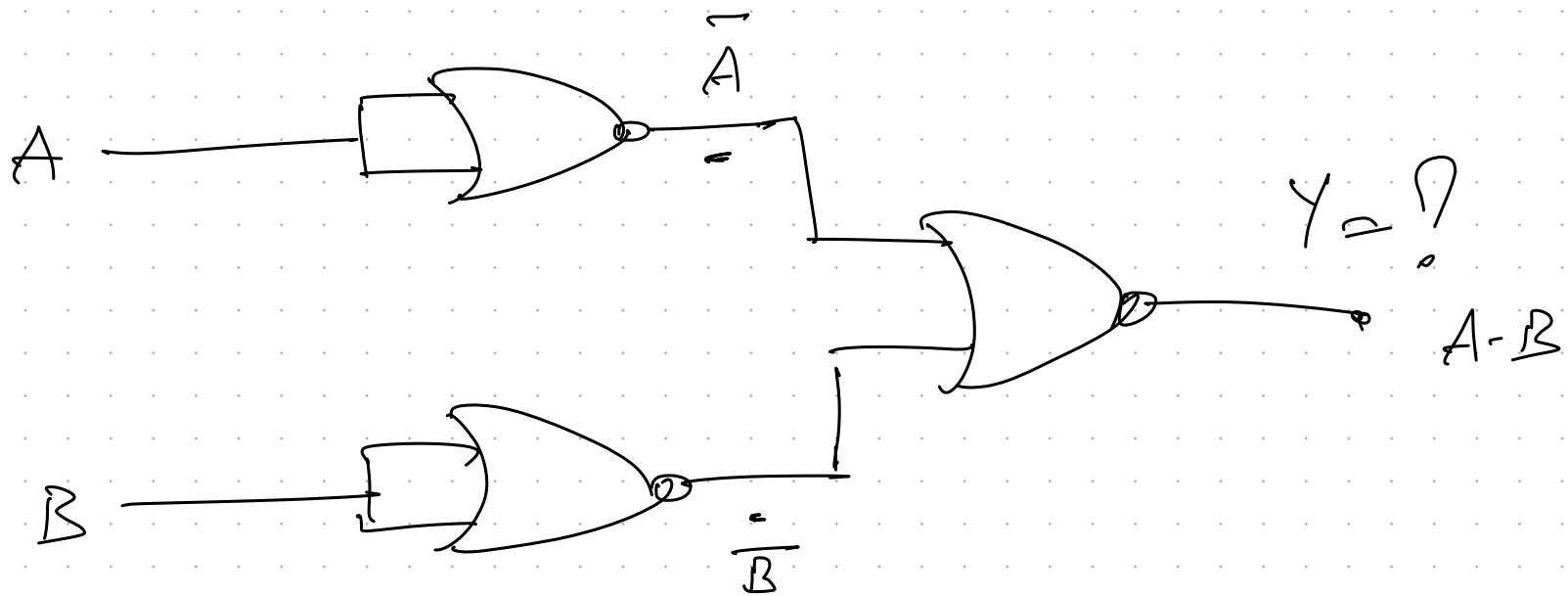
DC $\neg A \oplus B \rightarrow 2^{\text{DfP}}$

DC $\neg A \oplus B \rightarrow 3^{\text{DfP}}$

Exercise

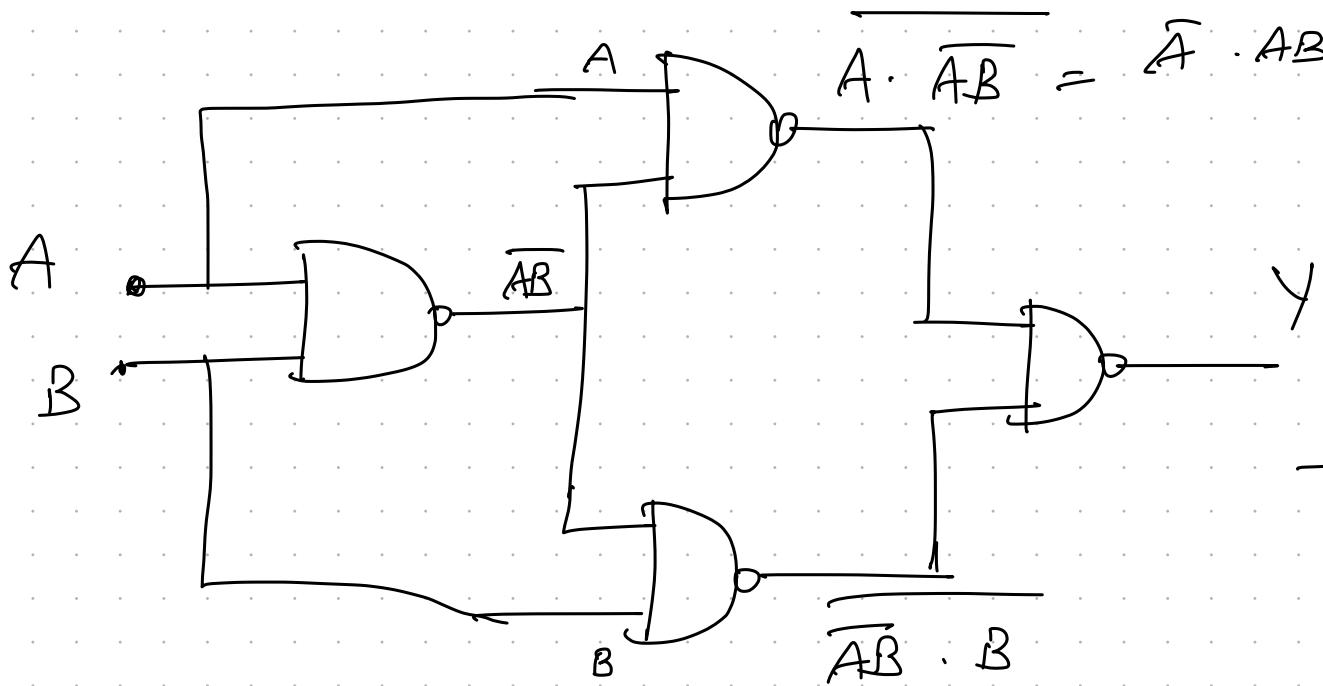
(i) $Y = \overline{A}B + A\overline{B}$

(ii)



(iii)

$$\bar{A} \cdot A \cdot B$$



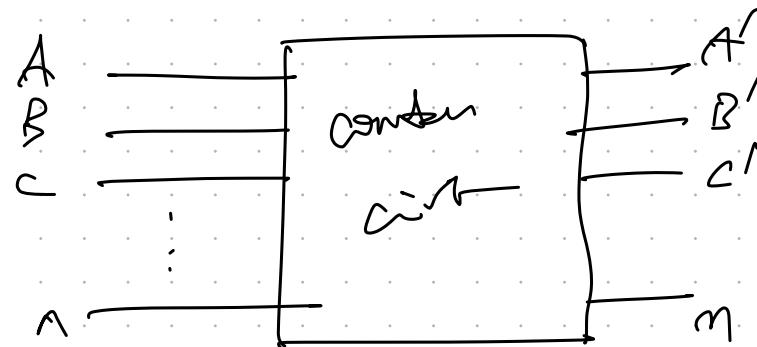
$$Y = ?$$

$$AB \cdot \bar{B}$$

$$A \cdot B \cdot \bar{B}$$

Combinational circuit

→ Combine different gates



Characteristics :-

- (i) The O/P of combinational circuit at any instant of time depends only on the levels present at its terminal.

② The 'C' do not use any memory. The previous state of D_P does not have any effect on the present state of the clt.

③ $1 \rightarrow D_P$ & $m \rightarrow O_P$

$m = 2^n$ Combinational O_P is possible

Half Adder



| A | B | Sum (\bar{S}) | Carry (C) |
|---|---|-------------------|-----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

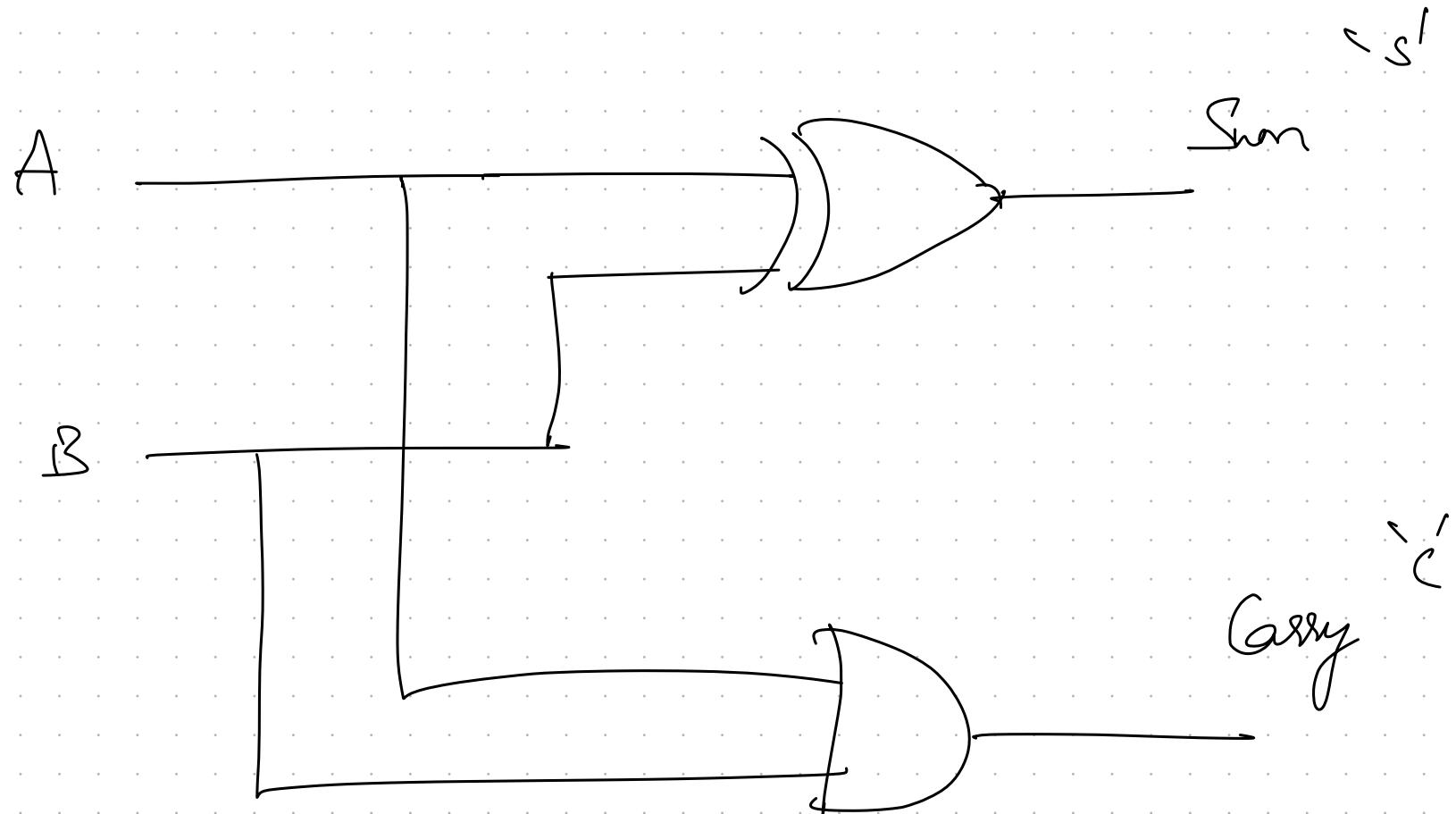
10
↓

0

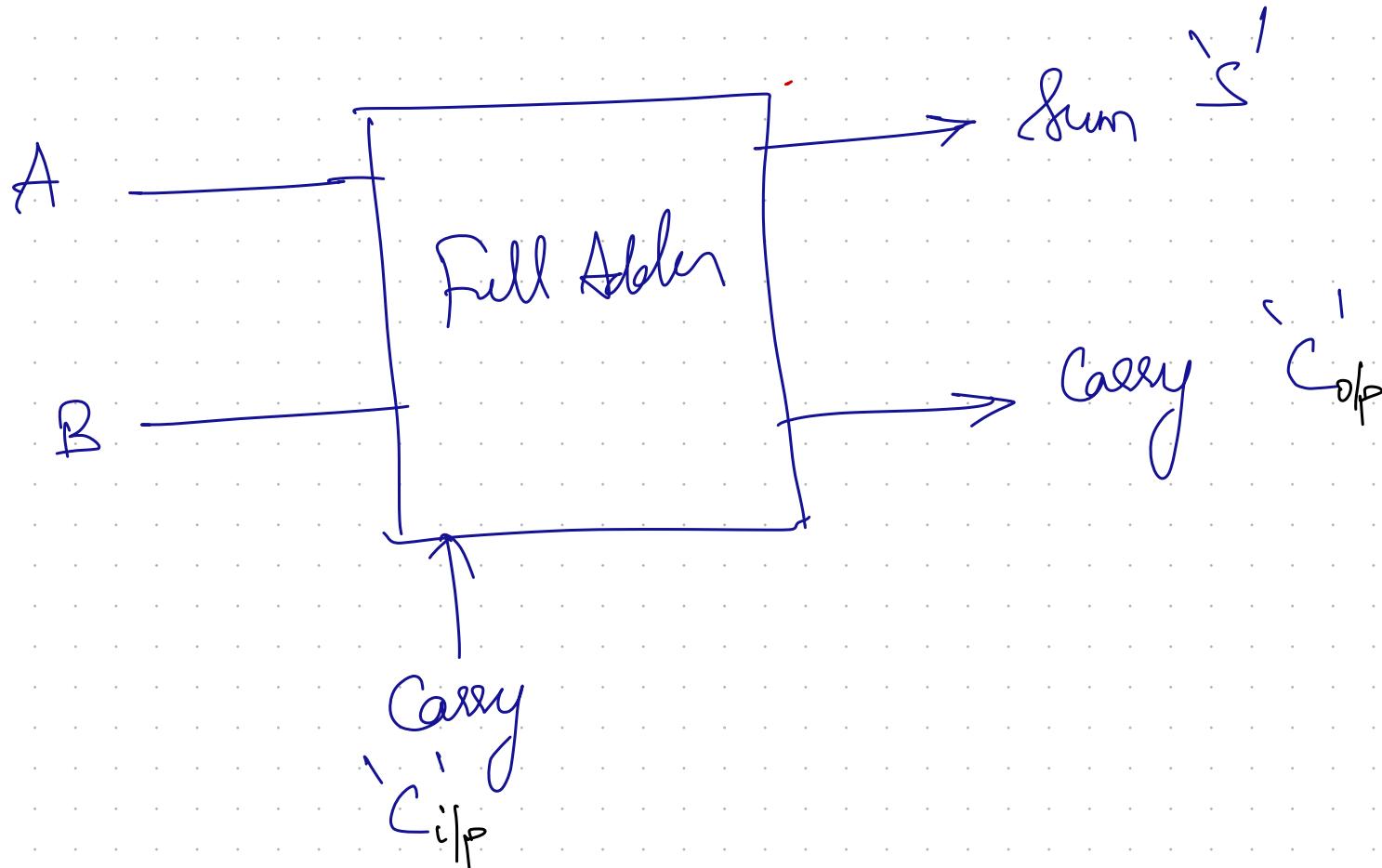
0

1

1



Full Adder



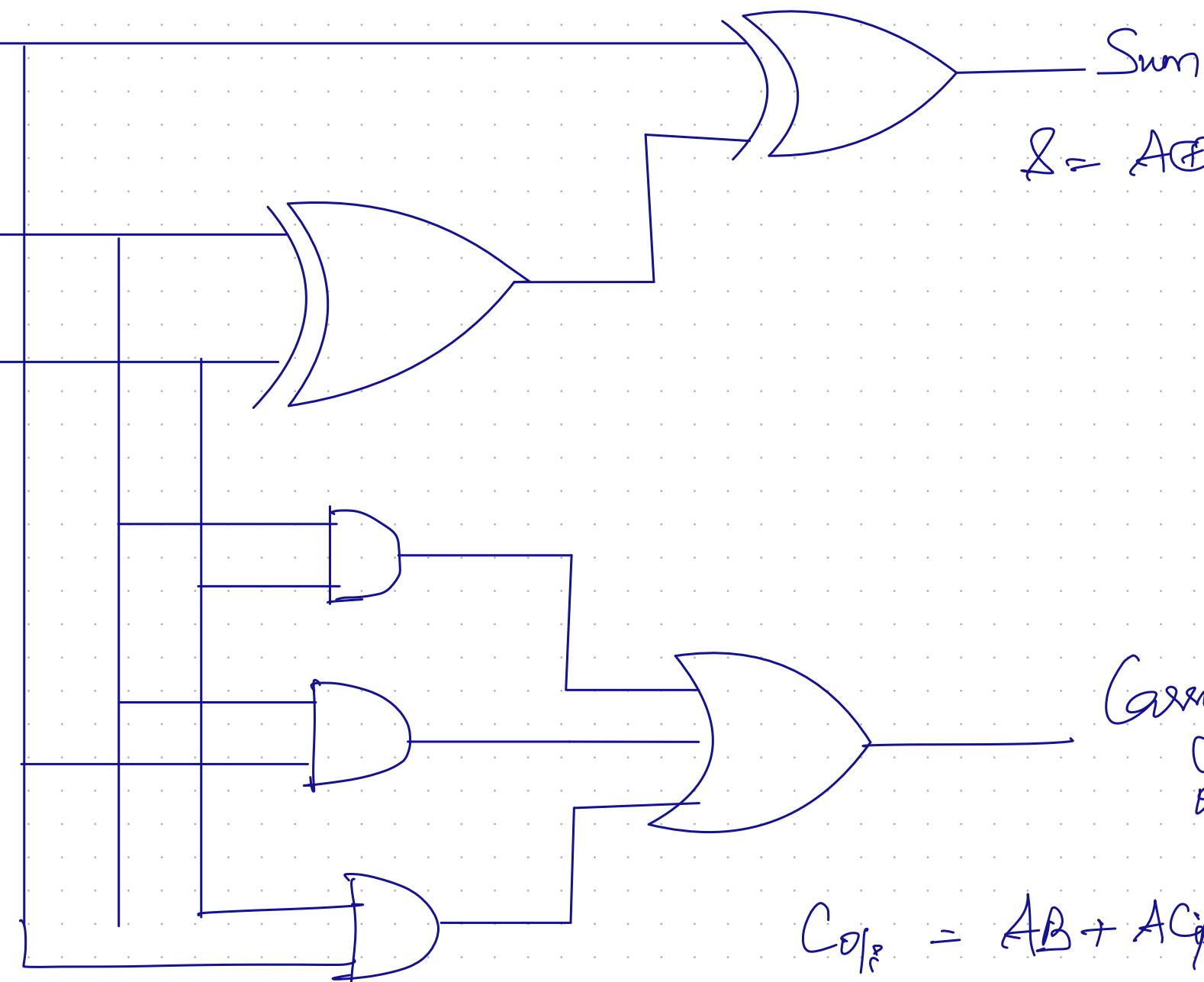
Truth table

| A | B | 'C _{in} | S | C _{out} |
|---|---|------------------|---|------------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

A

B

C

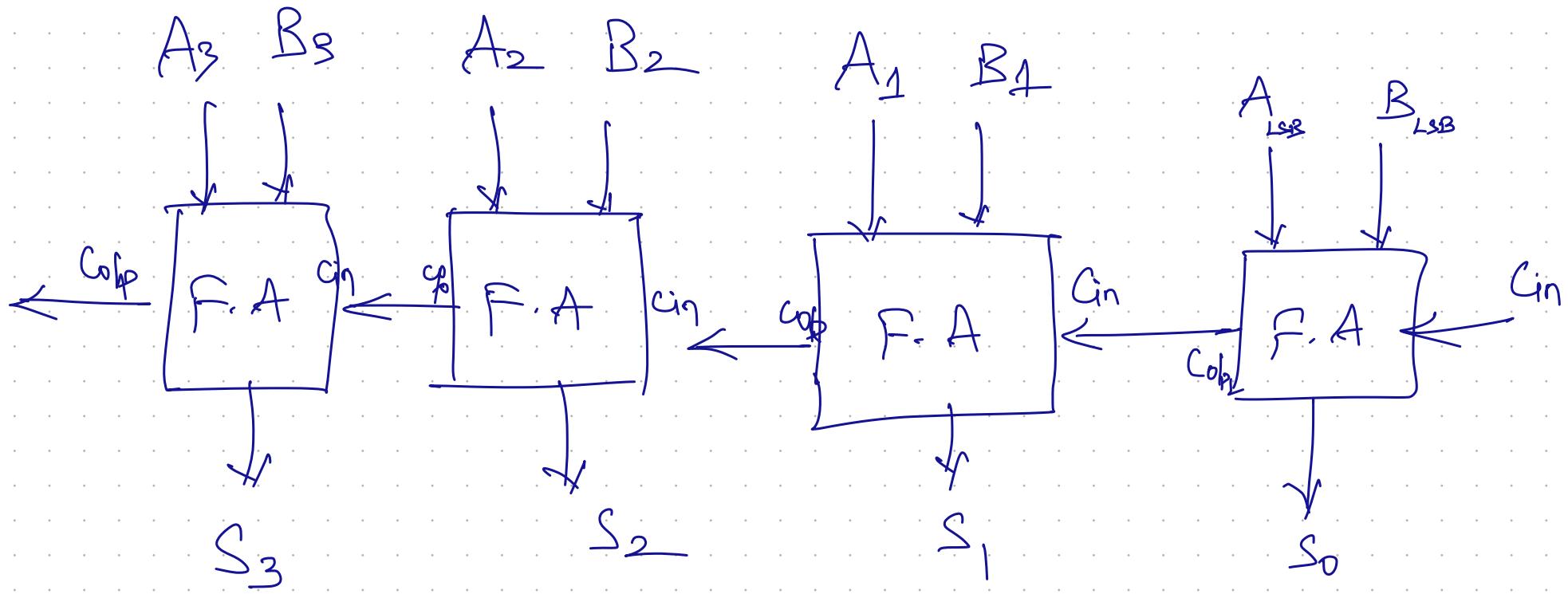
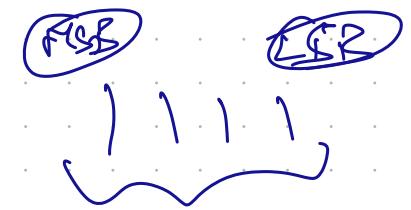


$$S = A \oplus B \oplus C$$

Carry
out

$$C_{OF} = AB + AC_{IP} + BC_{IP}$$

n -bit Parallel Adder



4 -bit Parallel Adder

Half Subtractor

→ Half subtractor → Combinational Ckt with two inputs & 2 outputs (difference & borrow).

if $A \geq B$

Truth table

\bar{A}

1

1

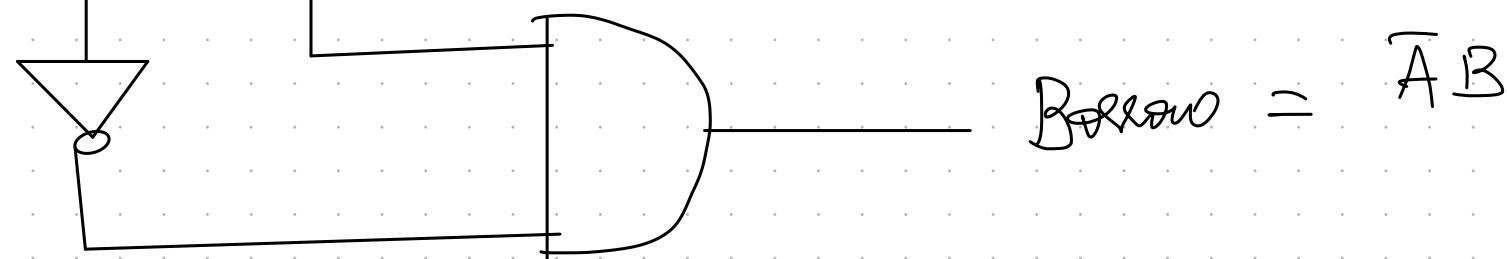
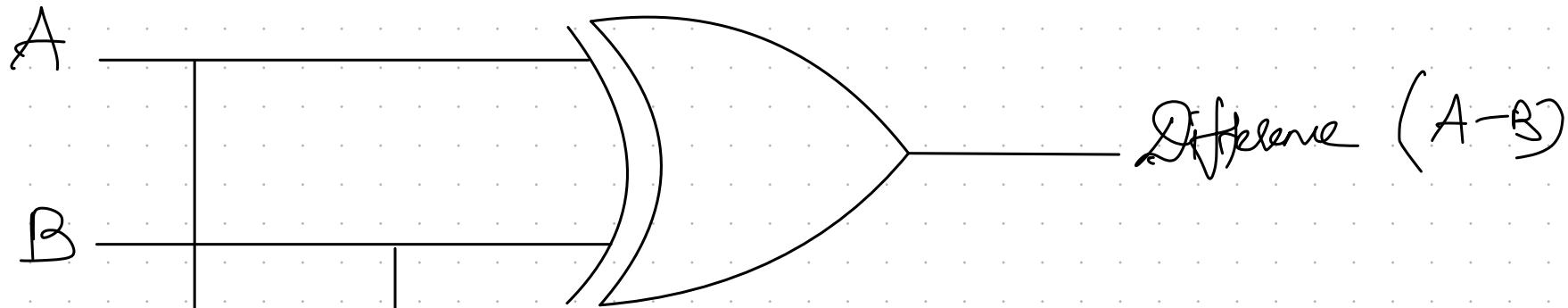
0

0

| | A | B | (A - B) | Borrow |
|---|---|---|---------|--------|
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |

Minuend bit

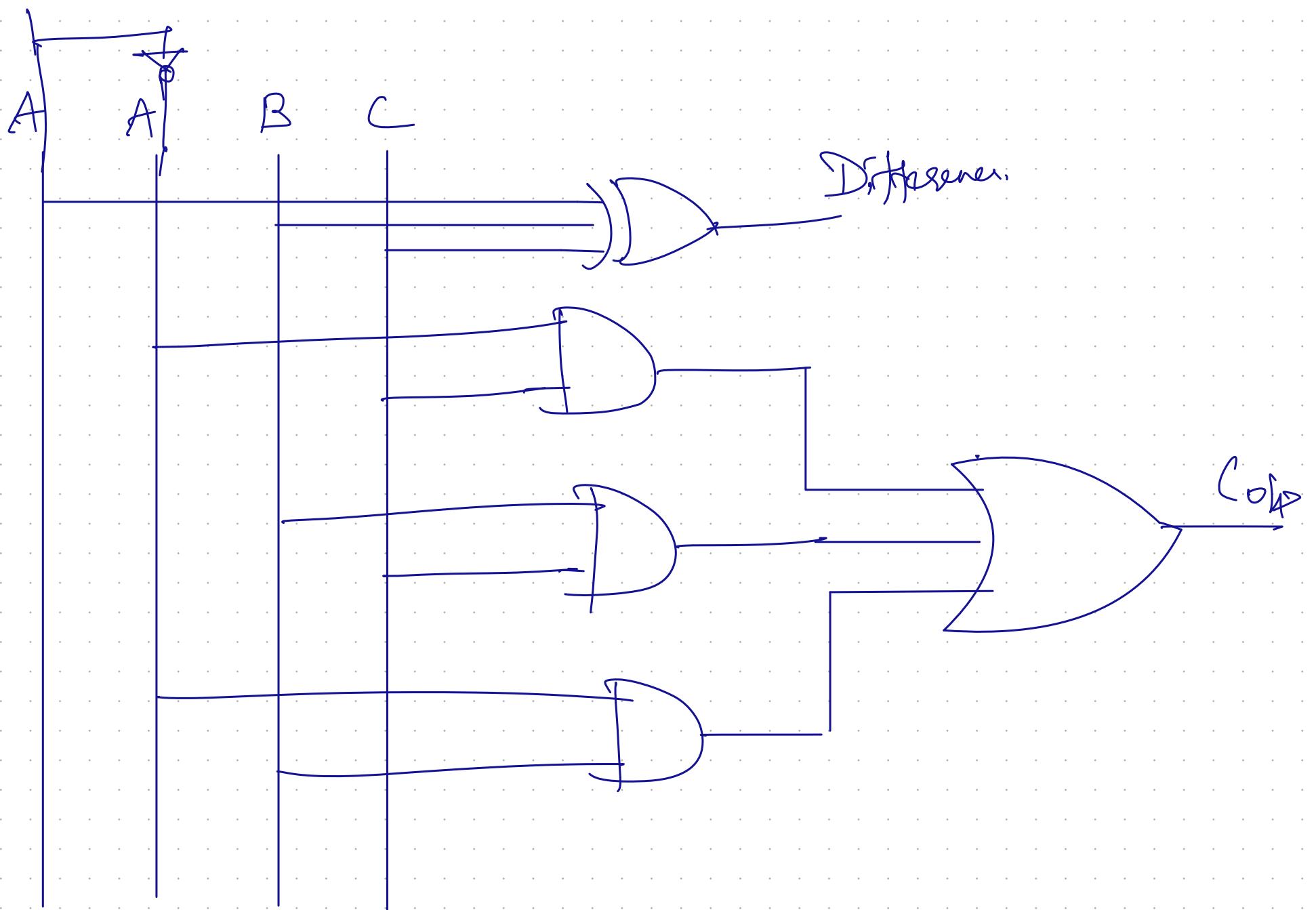
Subtrahend bit



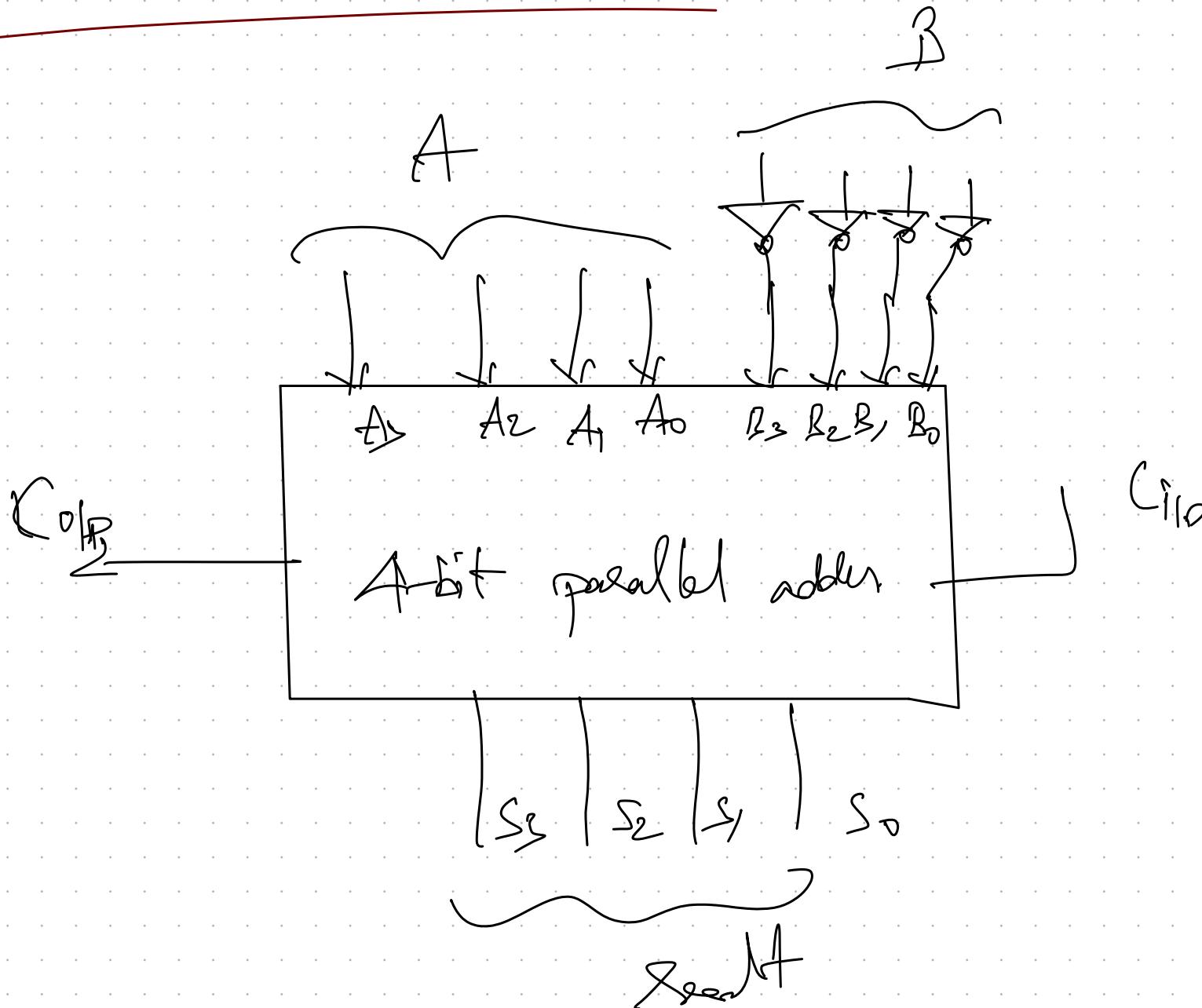
Full Subtractor

$$C' = \bar{A}C + \bar{A}\bar{B} + BC$$

| A' | A | B | C | $(A-B-C)$ | $C' \rightarrow \text{borrow off}$ |
|------|-----|-----|-----|-----------|------------------------------------|
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |

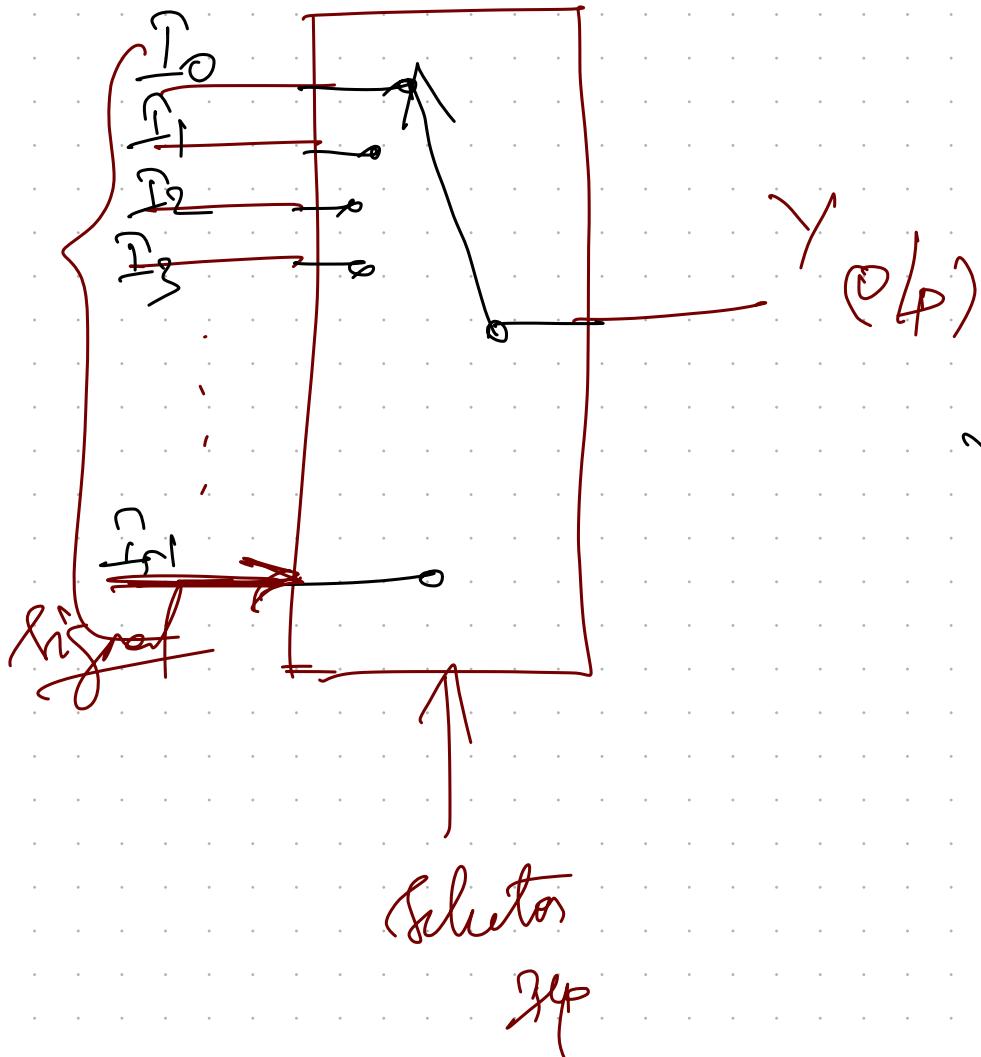


N-bit Subtractor



Multiplexers

Data D_P

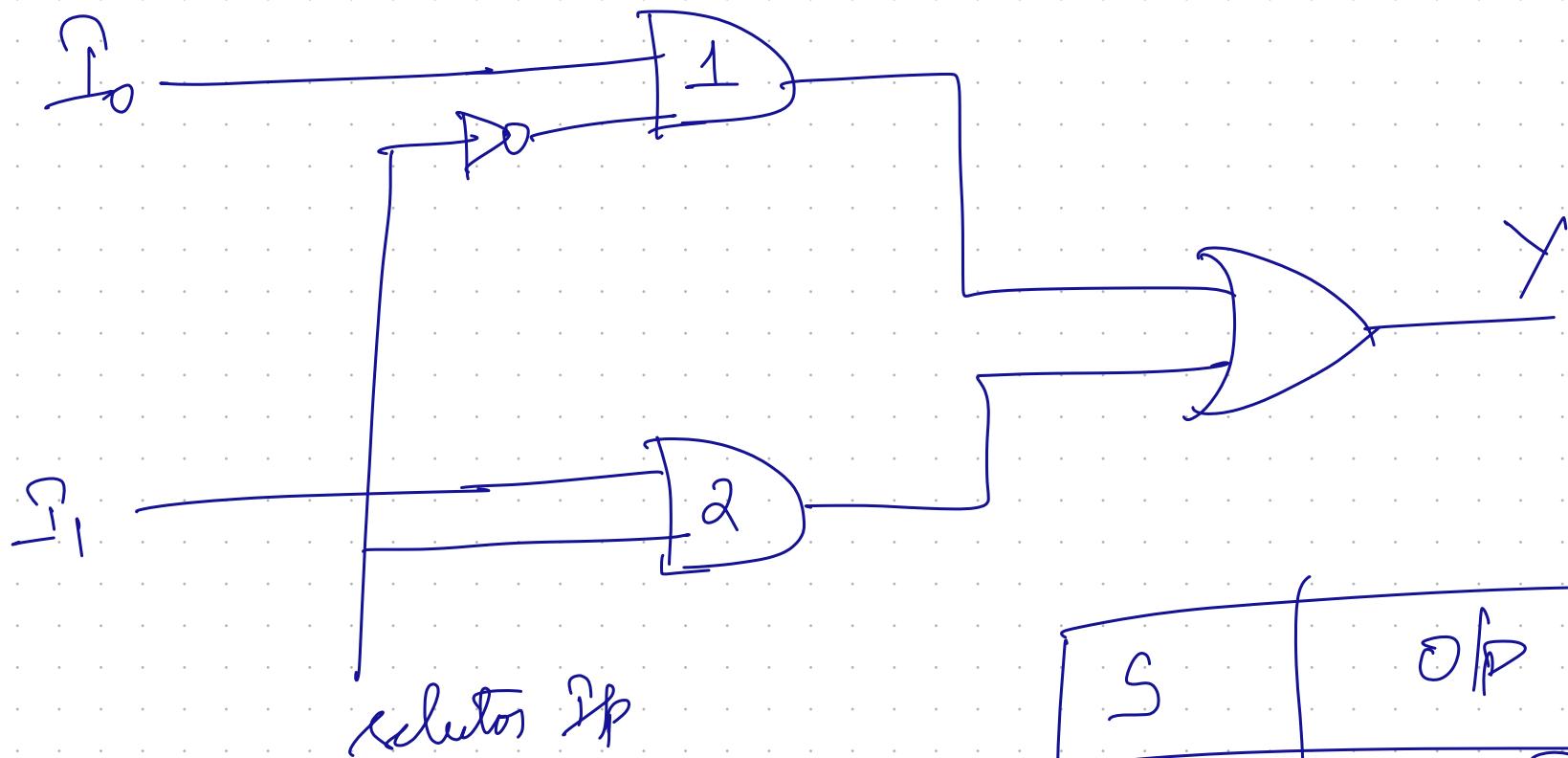


Same wire / line

Particular Selector D_P

Basic two-to-one Mux

$$Y = \bar{S}I_0 + S I_1$$



| S | Op |
|-----|-----------|
| 0 | $Y = I_0$ |
| 1 | $Y = I_1$ |

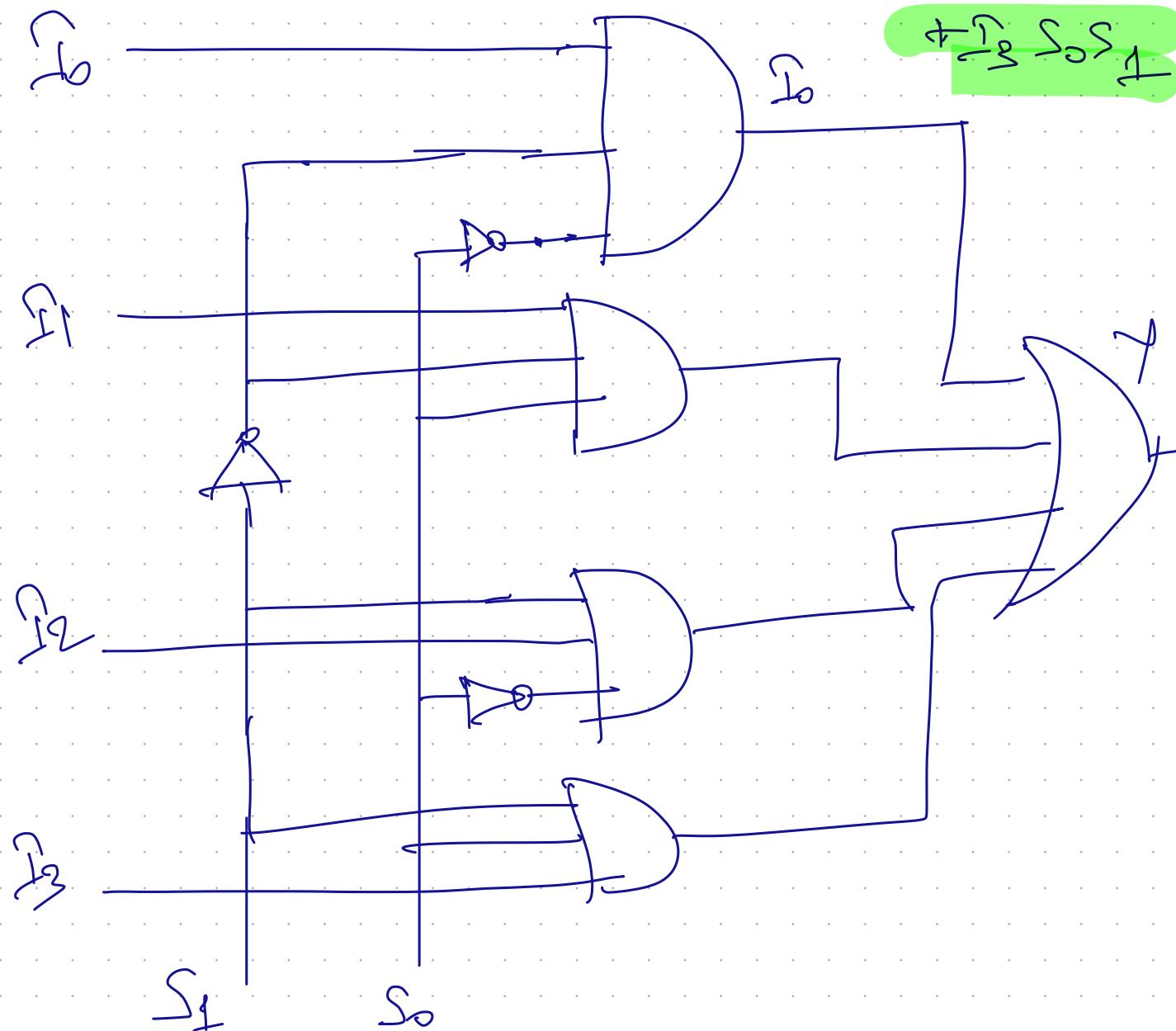
Four-Input MUX

→ 4 data IP & 2 - 8 IP

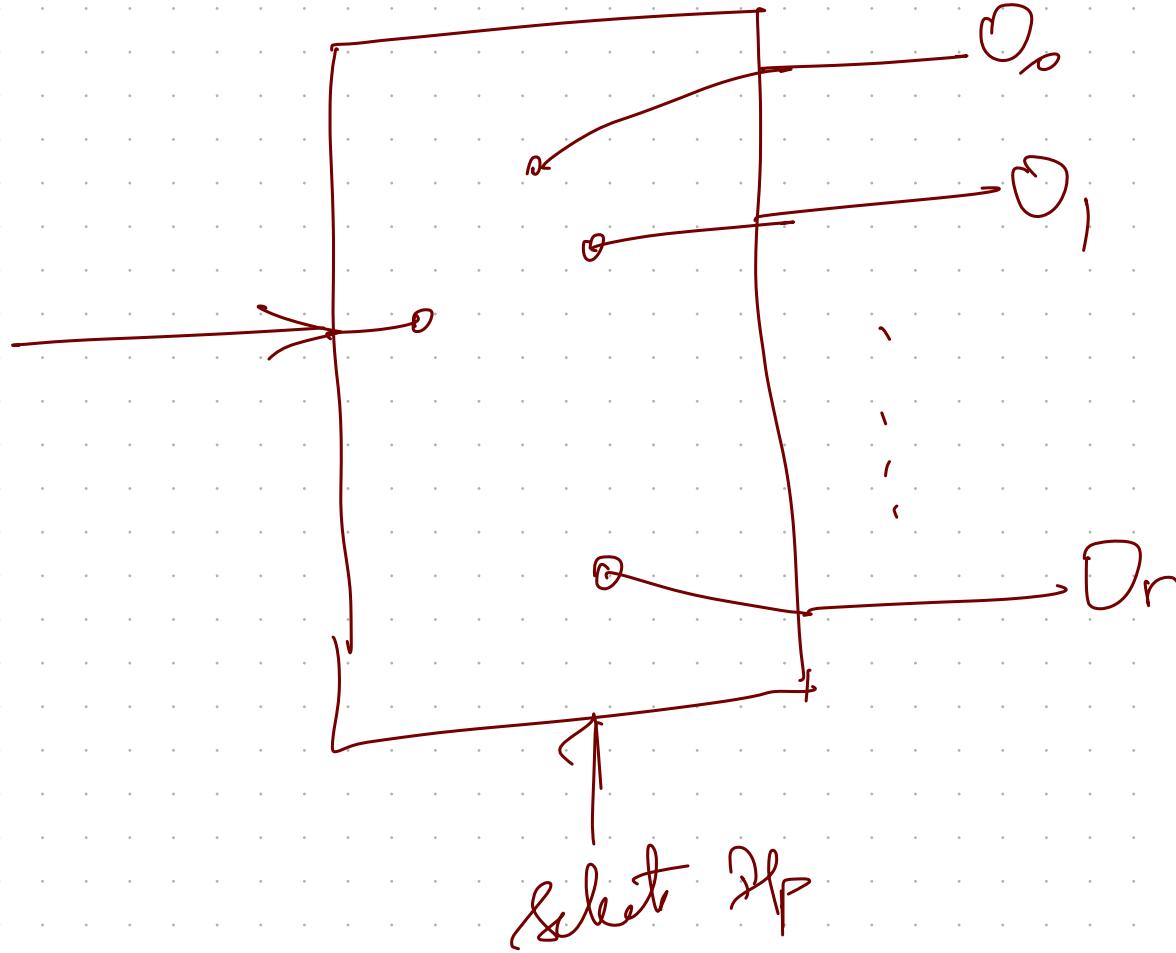
| S_1 | S_0 | Y |
|-------|-------|-------|
| 0 | 0 | I_0 |
| 0 | 1 | I_1 |
| 1 | 0 | I_2 |
| 1 | 1 | I_3 |

$$Y = I_0 \bar{S}_0 \bar{S}_1 + I_1 S_0 \bar{S}_1 + I_2 \bar{S}_0 S_1 + I_3 S_0 S_1$$

$$+ I_3 S_0 S_1$$



DR Multiplexers



1 - A de Mux

→ 2 Selectors If having 4 combinations
to have → 4 Ops.

S_1

S_0

0

0

0

I

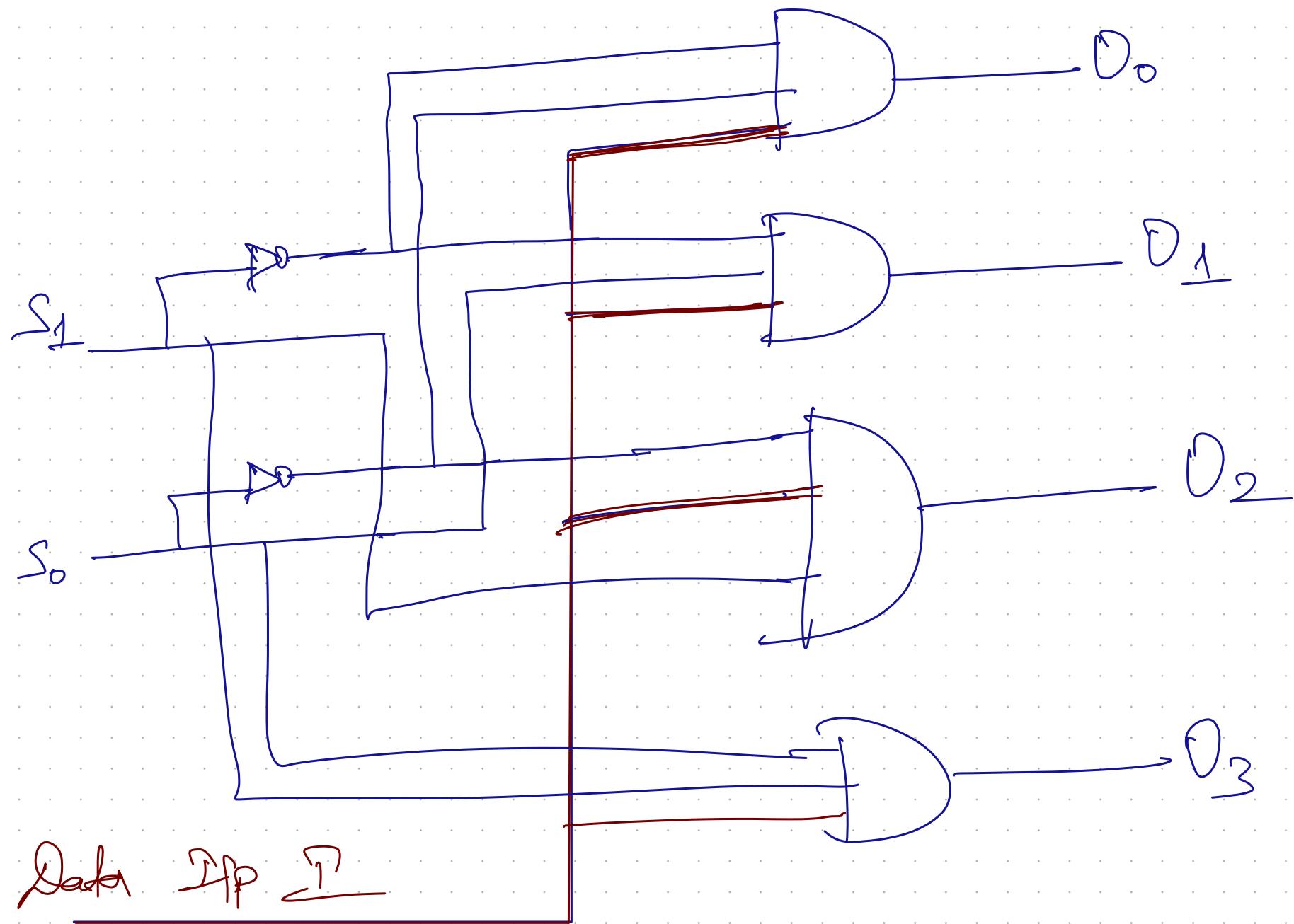
I

0

I

I

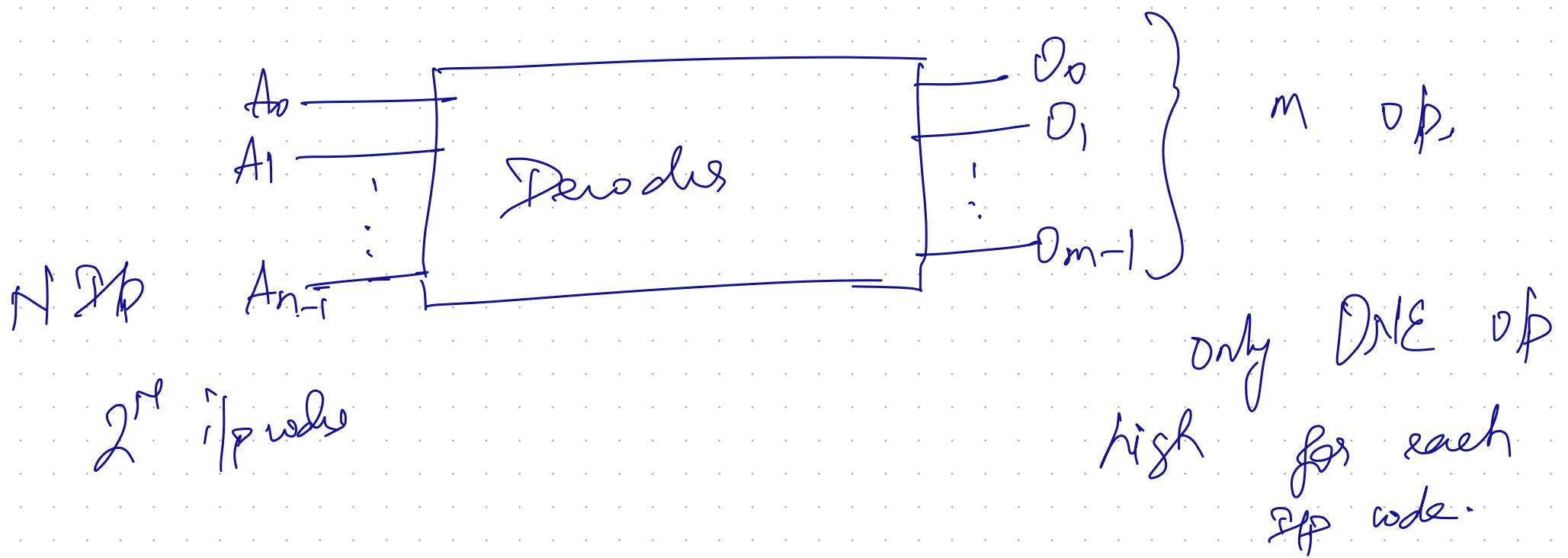
O_3 O_2 O_1 O_0
0 0 0 I
0 0 I 0
0 I 0 0
I 0 0 0



1 - 8 Dr. Mud

Decoders

for each SPP \rightarrow Only one DP as high



Applications

①

→ Cook Converters

→ BCD to Seven segment decoder

→ Relay actuators

2 - 4 line decoders

I_P

O/P

| A | B | D_0 | D_1 | D_2 | D_3 |
|---|---|-------|-------|-------|-------|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

3-8 line Decoder

C B A

0 0 0

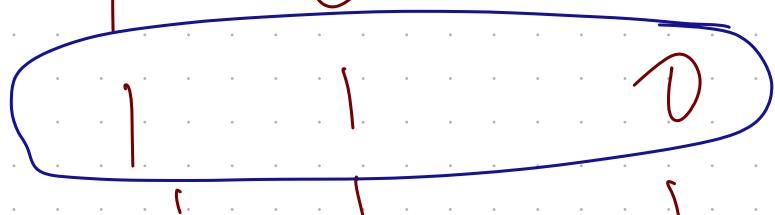
0 0 1

0 1 0

D 1 1

1 0 0

1 0 1



O₀ O₁ O₂ O₃ O₄ O₅ O₆ O₇

1 0 0 0 0 0 0 0

0 1 0 0 0 0 0 0

0 0 1 0 0 0 0 0

0 0 0 1 0 0 0 0

0 0 0 0 1 0 0 0

0 0 0 0 0 1 0 0

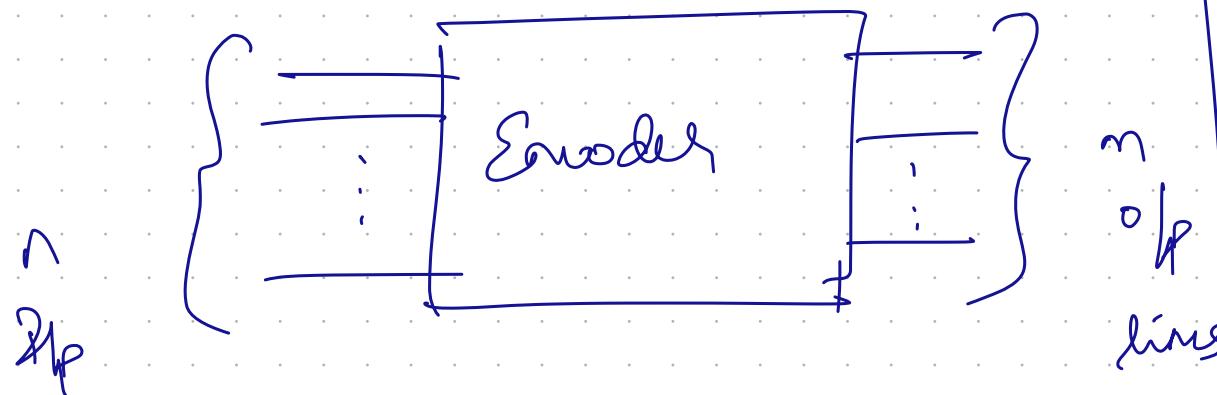
0 0 0 0 0 0 1 0

0 0 0 0 0 0 0 1

Encoders

It is a combinational dt.

$$n \rightarrow 2^m \quad m \rightarrow 2^n$$



Examples

- Priority encoder
- Decimal to BCD
- Datal to BCD

Priority Encoder

A_3

$A_2 \quad A_1$

A_0

$Y_0 \quad Y_1$

0

0

0

0

X

X

0

0

0

1

0

0

0

0

1

X

0

1

0

1

X

X

1

0

1

X

X

X

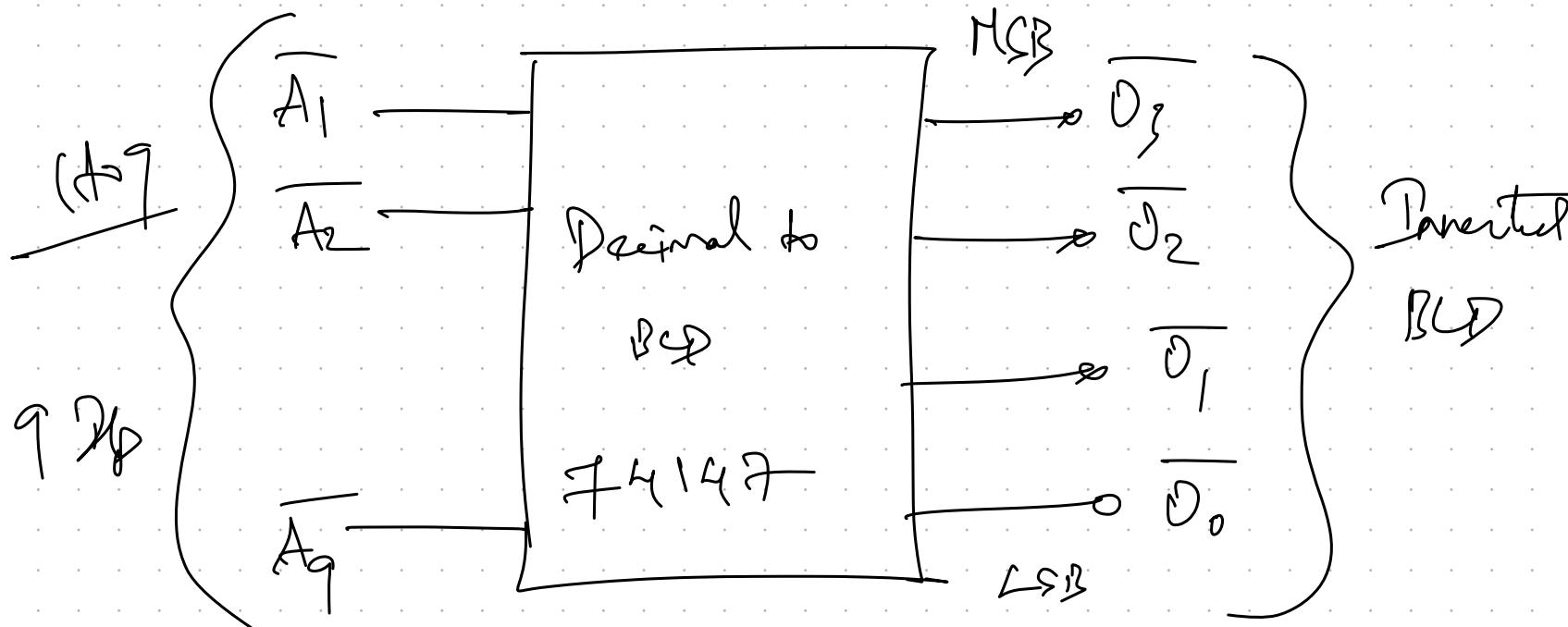
1

1

Decimal to BCD

High if
~~1~~

$O_3 \quad O_2 \quad O_1 \quad O_0$



This IC has low if

| | | | | | | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| \bar{A}_1 | \bar{A}_2 | \bar{A}_3 | \bar{A}_4 | \bar{A}_5 | \bar{A}_6 | \bar{A}_7 | \bar{A}_8 | \bar{A}_9 | \bar{Q}_1 | \bar{Q}_2 | \bar{Q}_3 | \bar{Q}_4 |
| | | | | | | | | | | | | |
| X | X | X | X | X | X | X | X | 0 | 0 | 1 | 1 | 0 |
| | | | | X | X | 0 | | | | | | |
| | | | | | O | O | | | | | | |

