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Started on Friday, 4 March 2022, 1:50 PM

State Finished

Completed on Friday, 4 March 2022, 1:56 PM

Time taken 6 mins

Marks 4.00/5.00

Grade 8.00 out of 10.00 (80%)

Question **1**

Complete

Mark 1.00 out of 1.00

For Implementing Instruction Pipeline ?

- ☐ a. Cycle time is determined by the smallest stage
- ☐ b. None of the mentioned
- ☐ c. Cycle time does not dependent on stages of the pipeline
- ☒ d. Cycle time is determined by the longest stage

Question **2**

Complete

Mark 1.00 out of 1.00

The Ideal RISC pipeline may have?

- ☐ a. Instructions can be divided into independent parts, each taking nearly equal time
- ☒ b. All of the mentioned
- ☐ c. Instructions are executed in sequence one after the other in the order in which they are written
- ☐ d. Successive instructions are independent of one another

Question **3**

Complete

Mark 1.00 out of 1.00

A four stage pipeline has the stage delays as 150, 120, 170 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate. The total time taken to process 1000 data items on the pipeline?

- ☐ a. 165.5 us
- ☐ b. 165.3 us
- ☒ c. 170.5 us
- ☐ d. 180.3 us

Question **4**

Complete

Mark 0.00 out of 1.00

For the of RISC pipeline. Choose the correct option.

- ☒ a. All operands are in registers
- ☐ b. The only operations that affect memory are loads and stores
- ☐ c. all instructions are the same size
- ☐ d. All of the mentioned

Question **5**

Complete

Mark 1.00 out of 1.00

For the single instruction pipeline (code given below). The two stalls are provided as a part of the program. Choose the correct option?

Begin: add t0, t1, t2

nop

nop

.end Begin

- ☒ a. For the given program two more stalls are required
- ☐ b. For the given program three more stalls are required
- ☐ c. For the given program one more stall is required
- ☐ d. For the given program no stalls are required

◀ [Assignment 3-25-02-2022](#)

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