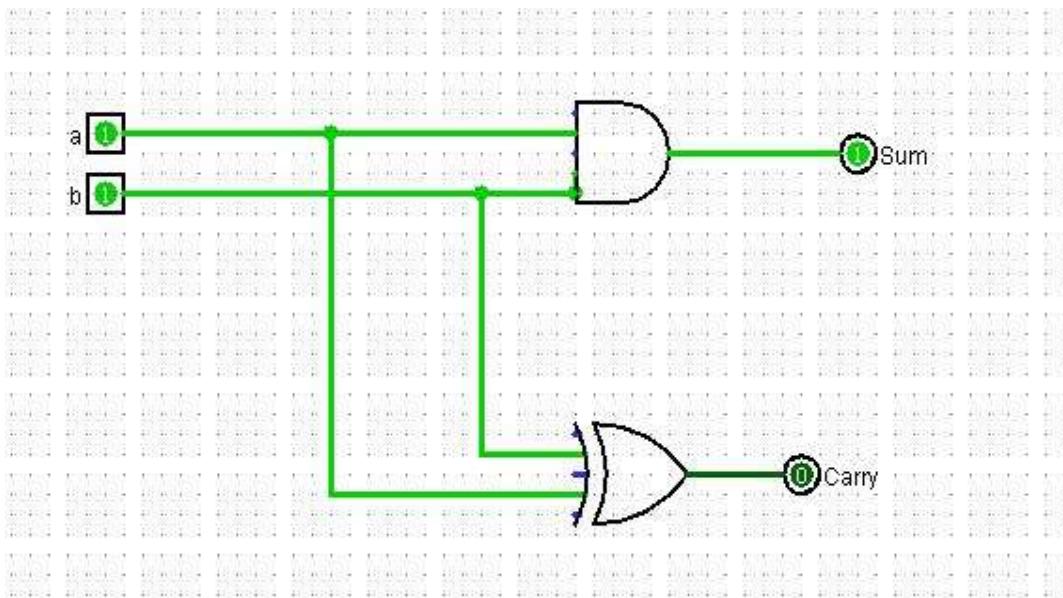


# EC201 : Assignment 3

## Problems with simulations

1. Draw two truth tables illustrating the outputs of a half-adder, one table for the sum output and the other for the output and Design in Logisim

Solution:

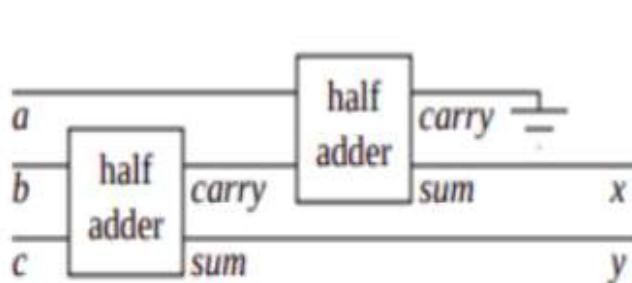


a	b	Sum	Carry
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

a	b	Carry
0	0	0
0	1	1
1	0	1
1	1	0

a	b	Sum
0	0	0
0	1	0
1	0	0
1	1	1

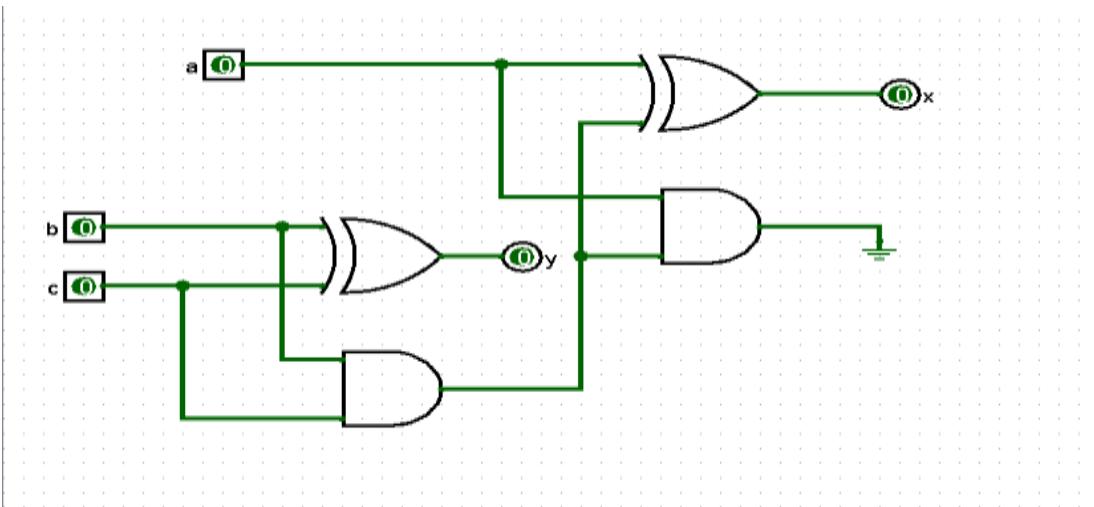
2. Fill in the truth table at right for the following circuit. Ignore rows not included in the table, then design in Logisim.



a	b	c	x	y
0	1	1		
1	0	1		
1	1	0		
1	1	1		

# EC201 : Assignment 3

Solution:



a	b	c	x	y
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

## Problems Without Simulations



### EC Assignment 3

#### Problems Without Simulations

3. Two 1's with no carry-in are added using a full adder. What are the outputs?

given  $A_1 = 1, B = 1, C_{in} = 0$

$$\begin{aligned} S &= A \oplus B \oplus C_{in} \\ &= 1 \oplus 1 \oplus 0 \\ S &= 0 \end{aligned}$$

$$\begin{aligned} C_{out} &= AB + C_{in}(A \oplus B) \\ &= 1 + 0(1 \oplus 1) \end{aligned}$$

$$C_{out} = 1$$

∴ Outputs are  $S = 0$  and  $C_{out} = 1$

4. Two 1's with a carry-in of 1 are added using a full adder. What are the outputs?

$$A = 1, B = 1, C_{in} = 1$$

$$\begin{aligned} S &= A \oplus B \oplus C_{in} \\ &= 1 \oplus 1 \oplus 1 \\ S &= 1 \end{aligned}$$

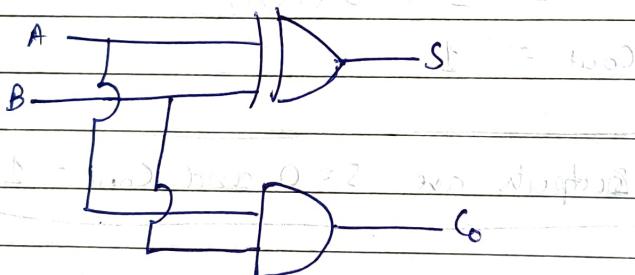
$$\begin{aligned} C_{out} &= AB + C_{in}(A \oplus B) \\ &= 1 + C_{in}(A \oplus B) \end{aligned}$$

$$C_{out} = 1$$

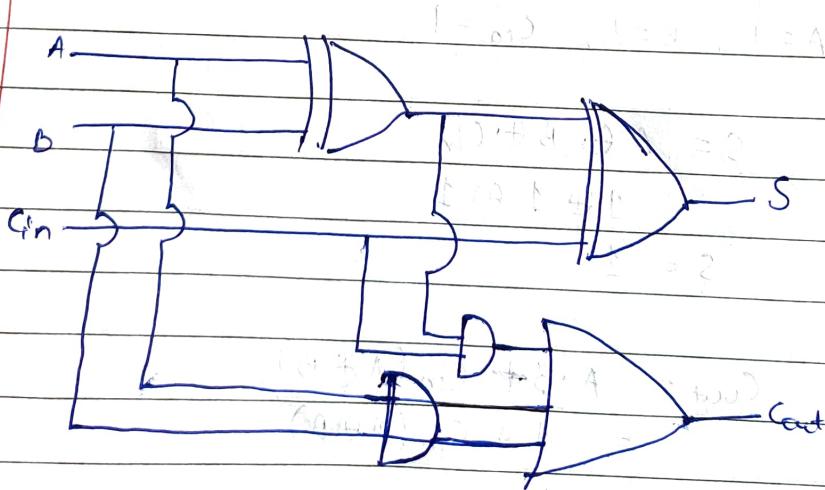
$\therefore$  Outputs are:  $S = 1$  and  $C_{out} = 1$

5. A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of AND/OR gate is 1.2 us. A 4-bit ripple carry binary adder is implemented by using full adders. Find out total propagation time of this 4-bit binary adder in us.

### Half Adder



### Full Adder:



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- from A or B to  $C_{out}$ : 4 gate delays ( $XOR \rightarrow AND \rightarrow OR$ )
- from  $A \oplus B$  to S: 4 gate delays ( $XOR \rightarrow XOR$ )
- from  $C_{in}$  to  $C_{out}$ : 2 gate delays ( $AND \rightarrow OR$ )
- from  $C_{in}$  to S: 2 gate delay ( $XOR$ )

because  $C_{out}$  of one stage is  $C_{in}$  for the next input:

- 4-gate delays from generating first carry signal (A or B to  $C_{out}$ ).
- 2-gate delays per intermediate stage ( $C_i$  to  $C_{i+1}$ )
- 2-gate delays at last stage to produce both the sum and carry-out outputs ( $C_{n-1}$  to  $C_n$  and  $S_{n-1}$ )

for an n-bit full adder, total propagation delay

$$t_p = 4 + 2(n-2) + 2$$

$$t_p = 2n + 2$$

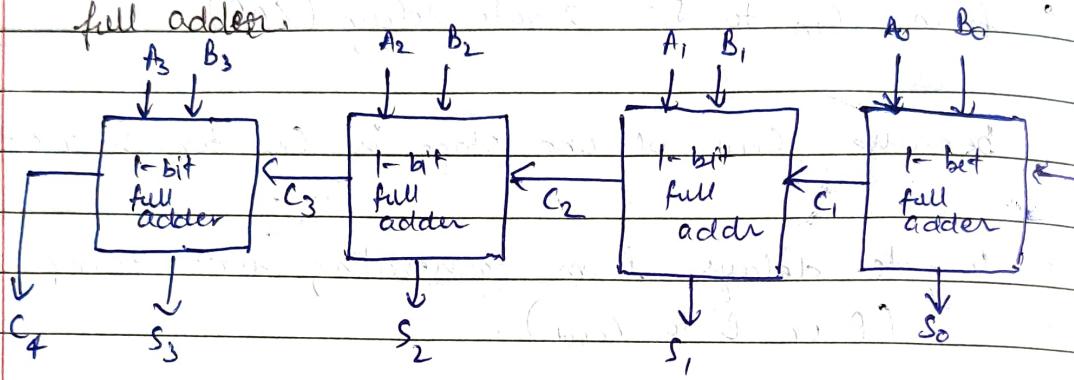
for 1-bit full adder,  $t_p = 4$

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∴ total delay of a 1-bit full adder is

$$\begin{aligned} t &= 4 \times 1.2 \\ &= 4.8 \mu\text{s} \end{aligned}$$

Diagram of 4-bit ripple adder using full adder:



delay of 4 full adders = $4 \times 4.8 \mu\text{s}$
$= 19.2 \mu\text{s}$

## ECE201: Assignment 4

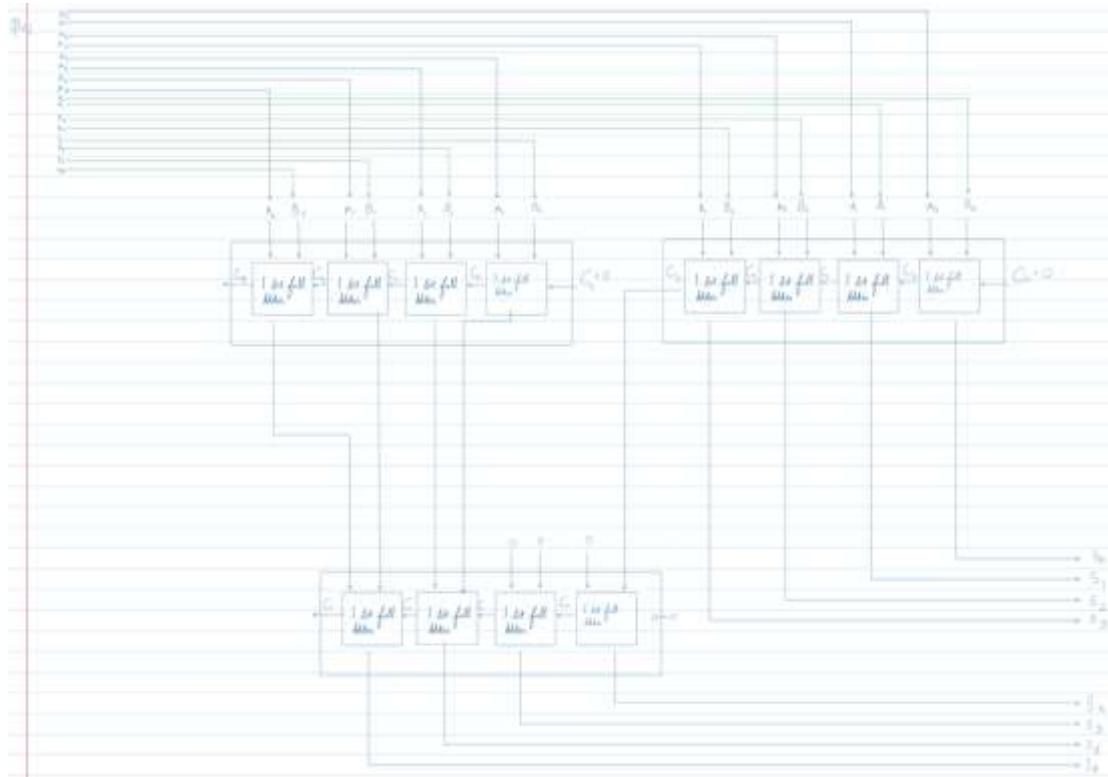
Q.1 What distinguishes the meaning of half adder's inputs and outputs from a full-adder?

Half-Adder	Full-Adder
• It adds two 1-bit binary digits ( $A, B$ )	• It adds three 1-bit binary digits ( $A, B, \text{cin}$ )
• Previous carry is not used	• previous carry is used
• $S = A \oplus B$ $C_{out} = A \cdot B$	• $S = A \oplus B \oplus \text{cin}$ $C_{out} = A \cdot B + \text{cin}(A \oplus B)$
• uses one XOR and one AND gate	• uses two XOR, two AND and one OR gate

# EC201 : Assignment 4

## Problems Without Simulations

2. Using only four-bit adders, construct an eight-bit adder. Each four-bit adder has two four-bit inputs and one five-bit output. Your eight-bit adder should have two eight-bit inputs and a one eight-bit output (don't worry about the ninth output bit).



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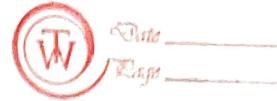


Q.3 The four inputs to a circuit ( $A, B, C, D$ ) represent an 8-4-2-1 BCD digit. Design the circuit so that the output ( $Z$ ) is 1 iff the decimal number represented by the inputs is exactly divisible by 3. Assume that only valid BCD digits occur as inputs!

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	x
1	0	1	1	x
1	1	0	0	x
1	1	0	1	x
1	1	1	0	x
1	1	1	1	x

} don't care

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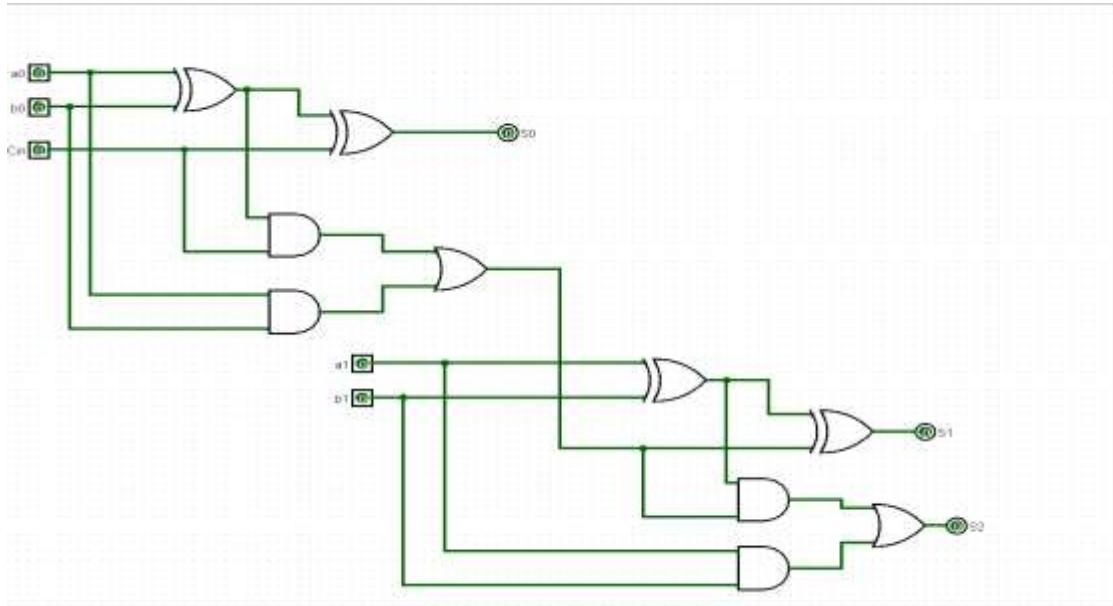
AB	CD	00	01	11	10
00		1		1	
01					1
11					
10		1			

$$Z = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D}$$

# EC201 : Assignment 4

## Problems with simulations

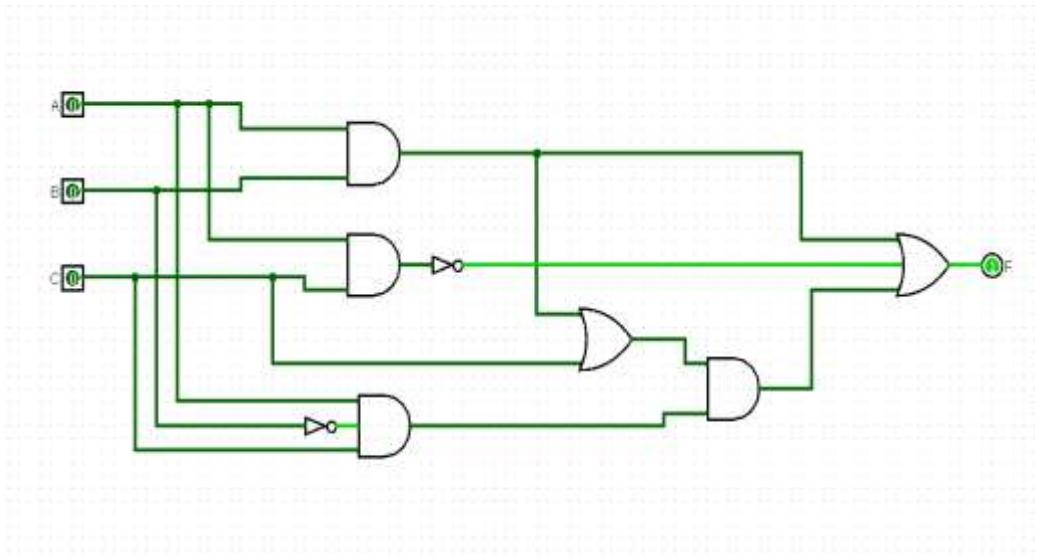
4. An adder is to be designed which adds two 2-bit binary numbers to give a 3-bit binary sum. Find the truth table for the circuit and equation. Design in Logisim



$a_0$	$b_0$	$C_{in}$	$a_1$	$b_1$	$S_0$	$S_1$	$S_2$
0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0
0	0	0	1	0	0	1	0
0	0	0	1	1	0	0	1
0	0	1	0	0	1	0	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	0	1	0	0
0	1	0	0	1	1	1	0
0	1	0	1	0	1	0	0
0	1	0	1	1	1	1	0
0	1	1	0	0	0	0	1
0	1	1	0	1	0	0	1
0	1	1	1	0	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	0	1	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	0	0	1
1	0	1	1	0	0	0	1
1	0	1	1	1	0	1	1
1	1	0	0	0	0	1	0
1	1	0	0	1	0	0	1
1	1	0	1	0	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	0	1	1	0
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1

# EC201 : Assignment 4

5. Reduce  $AB + (AC)' + AB'C$  ( $AB + C$ ) and design in Logisim



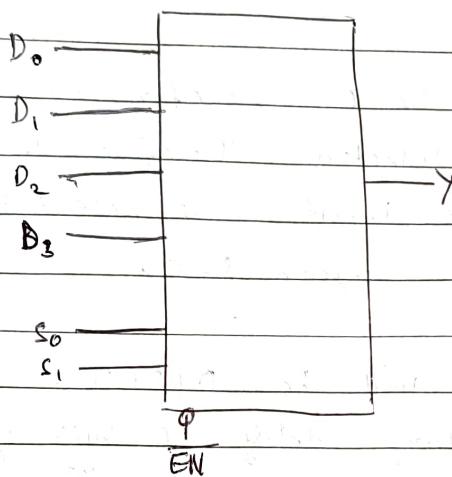
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

# **EC201 : Assignment 4**

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## EC201: Assignment 5

1. Let all D inputs be LOW, both S inputs be HIGH, and the enable input be LOW. What is the status of Y output?

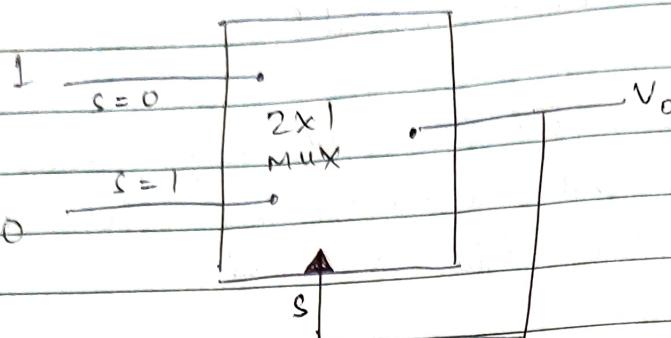


circuit  
 Since, enable is active when enable input is low (negative logic), therefore, using the select inputs multiplexer will direct to input  $D_3$  as both S inputs are given high.  
 Since  $D_3$  is Low, output Y will also be LOW in the given state of the inputs.

2. A 2 to 1 multiplexer having a switching delay of 1 ns is connected as shown in the figure. The output of the multiplexer is tied to its own select input. The input which gets selected when  $S=0$ , is tied to 1 and the input that gets selected when  $S=1$  is tied to 0. The output  $V_o$  will be?

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Initially  $V_0$  will be 0, therefore  $S = 0$ .

- $\therefore$  Input 1 is selected, therefore  $V_0 = 1$ ,
- $\therefore S = 1$ , hence, input 2 is selected,  
hence  $V_0 = 0$ , again  $S = 0$ .

$\therefore$  the output  $V_0$  will be 010101

Since, the switching delay of MUX is 1  $\mu s$ , ~~and~~ therefore the time interval at which the output is repeated is 2  $\mu s$ .

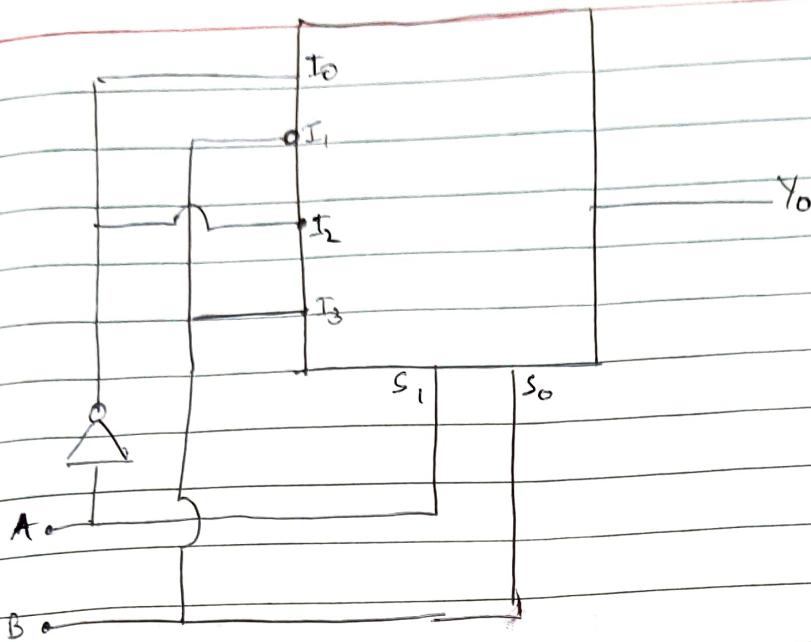
$$\therefore \text{frequency of output pulse} = \frac{1}{2\mu s} = 0.5 \text{ MHz}$$

$\therefore V_0$  will be a pulse of 0 and 1 of frequency 0.5 MHz.

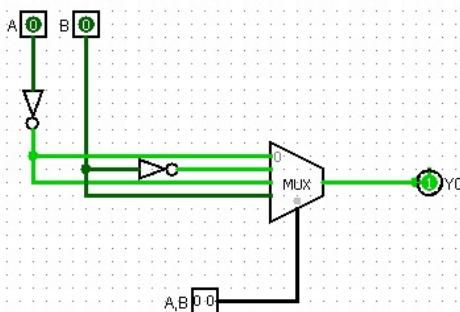
Problems based On Simulations

3. Realize  $Y_0$  using 4x1 MUX. Design in Logisim. Find out  $Y_0$ .

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The circuit designed in logisim:



The truth table obtained from the software:

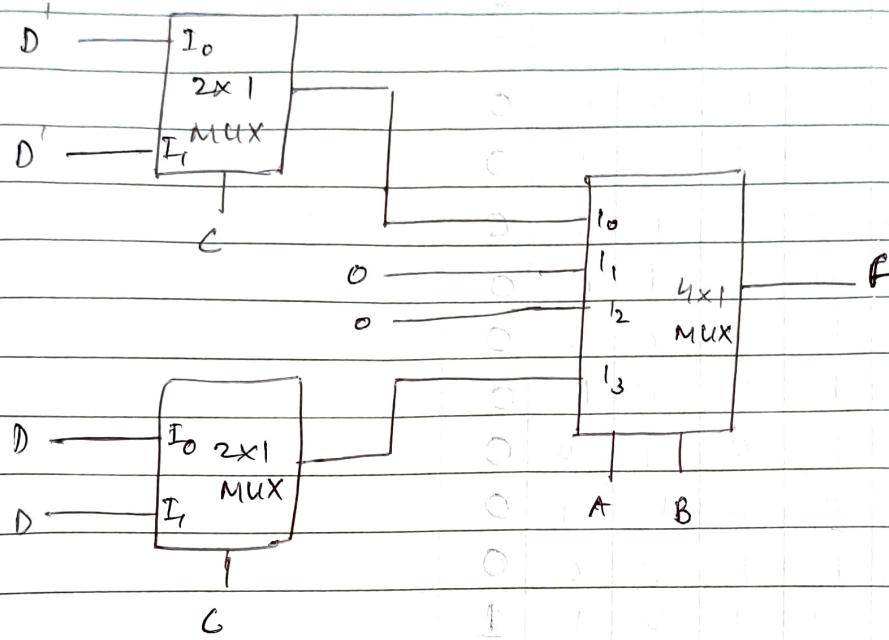
$S_1 = A$	$S_0 = B$	$T_0 = \bar{A}$	$T_1 = \bar{B}$	$T_2 = \bar{A}$	$T_3 = B$	$Y_0$
0	0	1	1	1	0	1
0	1	1	0	1	1	0
1	0	0	1	0	0	0
1	1	0	0	0	1	1

This is clearly the XNOR operation  
 $\therefore Y_0 = A \text{xnor} B$

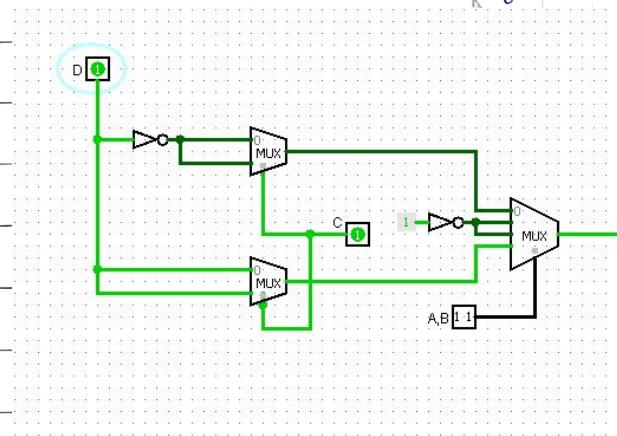
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4. Determine the output and design in Logisim software.



The circuit designed in Logisim:



The truth table that we got from the software is -

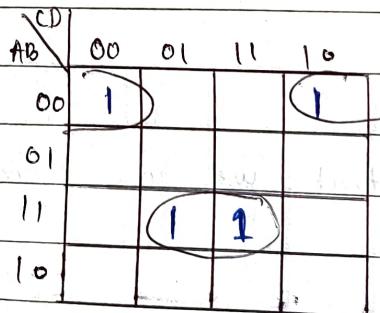
$C \oplus A + \bar{C}B = F$

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A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

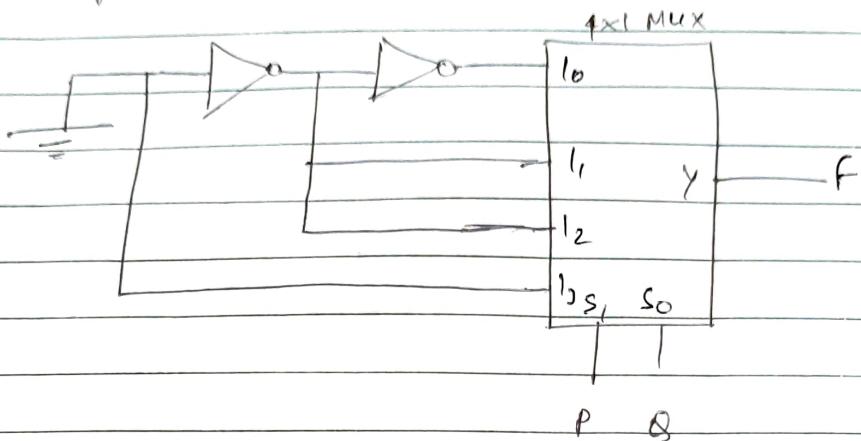
The K-map for this truth table is:



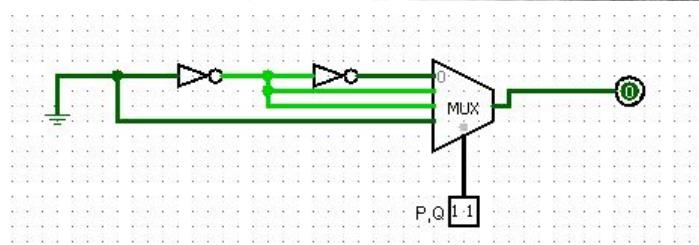
the possible pairings are shown:

$$\therefore F = ABD + \bar{A}\bar{B}\bar{D}$$

- 5) Determine the output function  $f$  and design in Logisim software



The circuit designed in Logisim:



The truth table obtained from the software is:

P	Q	$l_0$	$l_1$	$l_2$	$l_3$	F
0	0	0	1	1	0	0
0	1	0	1	1	0	1
1	0	0	1	1	0	1
1	1	0	1	1	0	0

Clearly it is XOR operation,

$$\therefore f = P \text{xor} Q$$