20205213

EC201 : Assignment 4

Q.1 What distinguishes the meaning of half adder's inputs and outputs from a full-adder?

Half-Adder	Full-Adder
• It adds two 1-bit binary digits (A, B)	• It adds three 1-bit binary digits (A, B, C_{in})
• Previous carry is not used	• previous carry is used
• $S = A \oplus B$ $C_{out} = A \cdot B$	• $S = A \oplus B \oplus C_{in}$ $C_{out} = AB + C_{in}(A \oplus B)$
• uses one XOR and one AND gate	• uses two XOR, two AND and one OR gate

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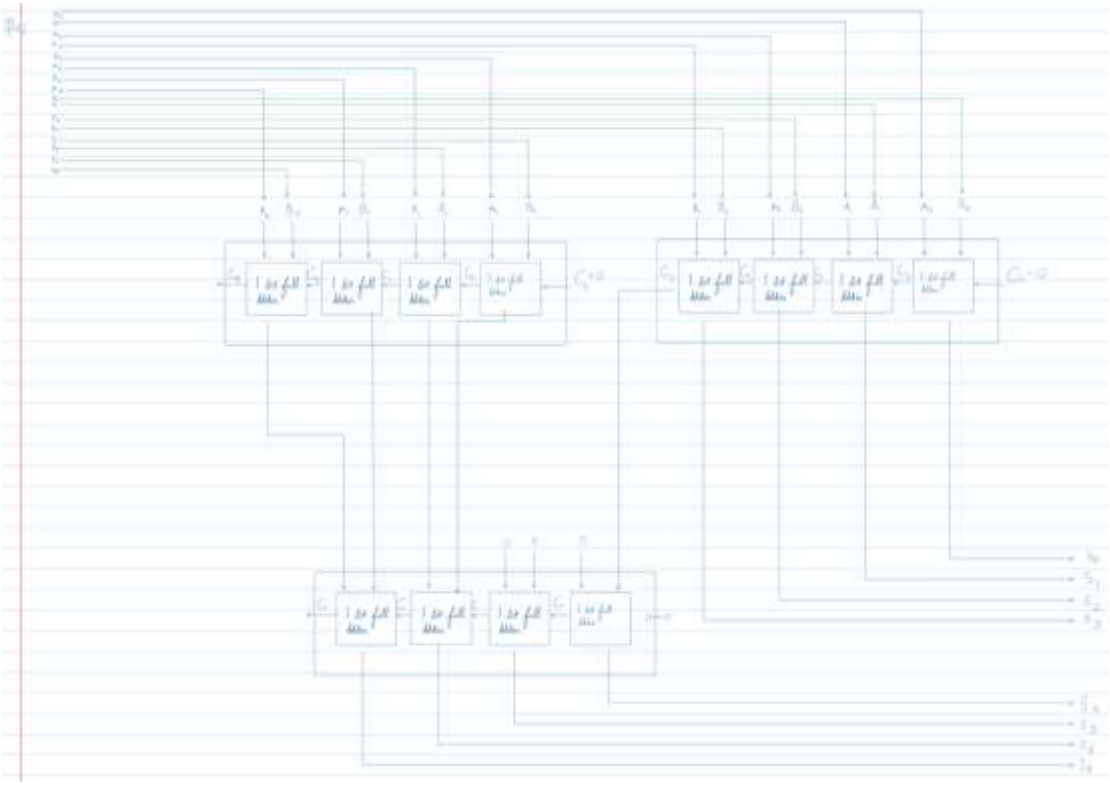
Problems Without Simulations

2. **Using only four-bit adders, construct an eight-bit adder. Each four-bit adder has two four-bit inputs and one five-bit output. Your eight-bit adder should have two eight-bit inputs and a one eight-bit output (don't worry about the ninth output bit).**



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Q-3 The four inputs to a circuit (A, B, C, D) represent an 8-4-2-1 bcd digit. Design the circuit so that the output (Z) is 1 iff the decimal number represented by the inputs is exactly divisible by 3. Assume that only valid BCD digits occur as inputs:

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	x
1	0	1	1	x
1	1	0	0	x
1	1	0	1	x
1	1	1	0	x
1	1	1	1	x

} don't care

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AB \ CD	00	01	11	10
00	1		1	
01				1
11				
10		1		

$$Z = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D + \bar{A}BC\bar{D}$$

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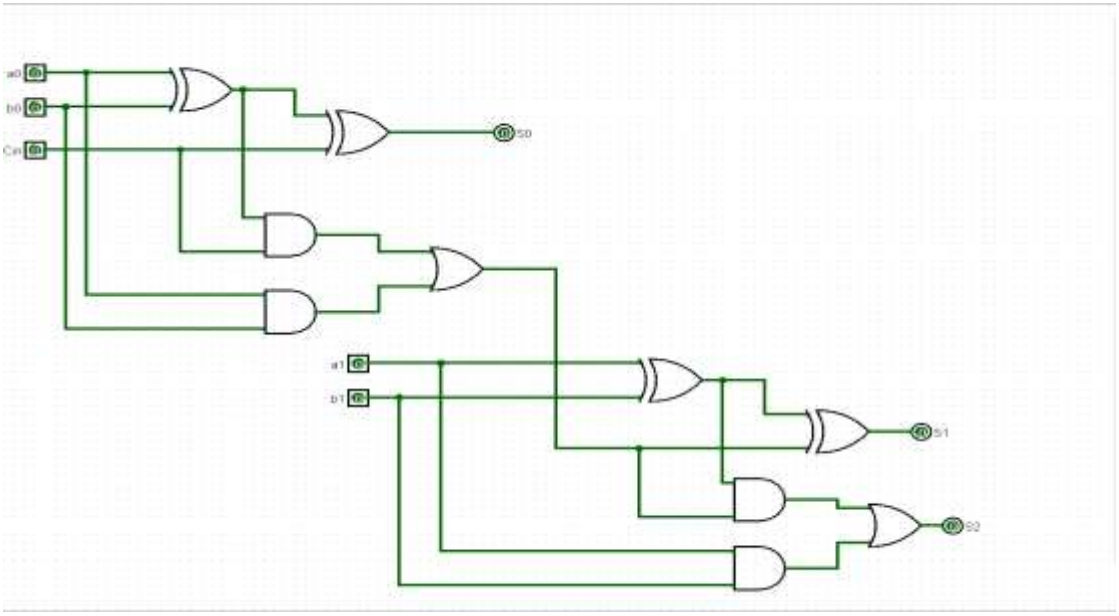
Problems with simulations

4. **An adder is to be designed which adds two 2-bit binary numbers to give a 3-bit binary sum. Find the truth table for the circuit and equation. Design in Logisim**



a0	b0	Cin	a1	b1	S0	S1	S2
0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0
0	0	0	1	0	0	1	0
0	0	0	1	1	0	0	1
0	0	1	0	0	1	0	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	0	1	0	0
0	1	0	0	1	1	1	0
0	1	0	1	0	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	0	0	1
0	1	1	1	0	0	0	1
0	1	1	1	1	0	1	1
1	0	0	0	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	0	1	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	0	0	1
1	0	1	1	0	0	0	1
1	0	1	1	1	0	1	1
1	1	0	0	0	0	1	0
1	1	0	0	1	0	0	1
1	1	0	1	0	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	0	1	1	0
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1

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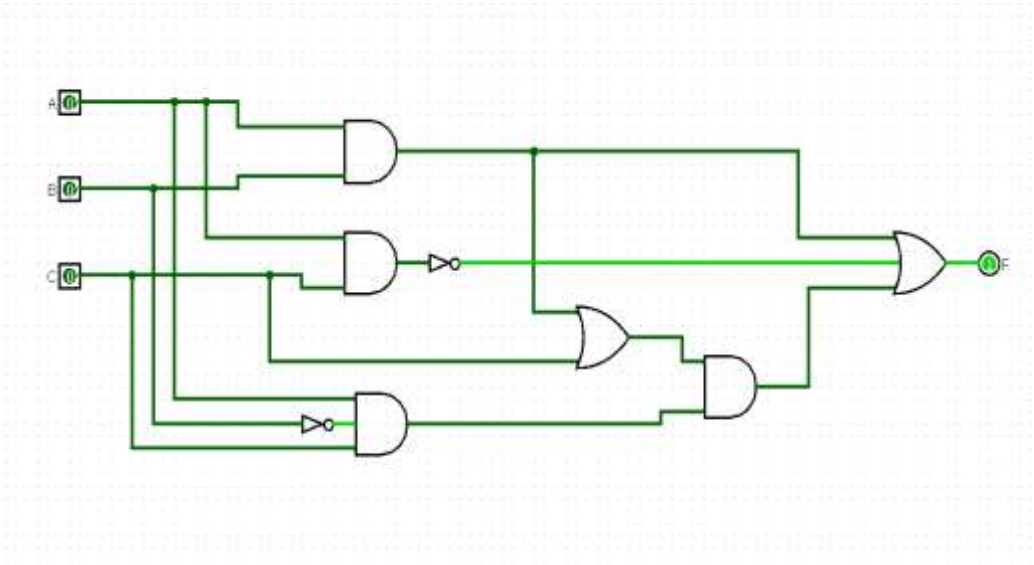
5. Reduce AB + (AC)' + AB'C (AB + C) and design in Logisim



A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

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