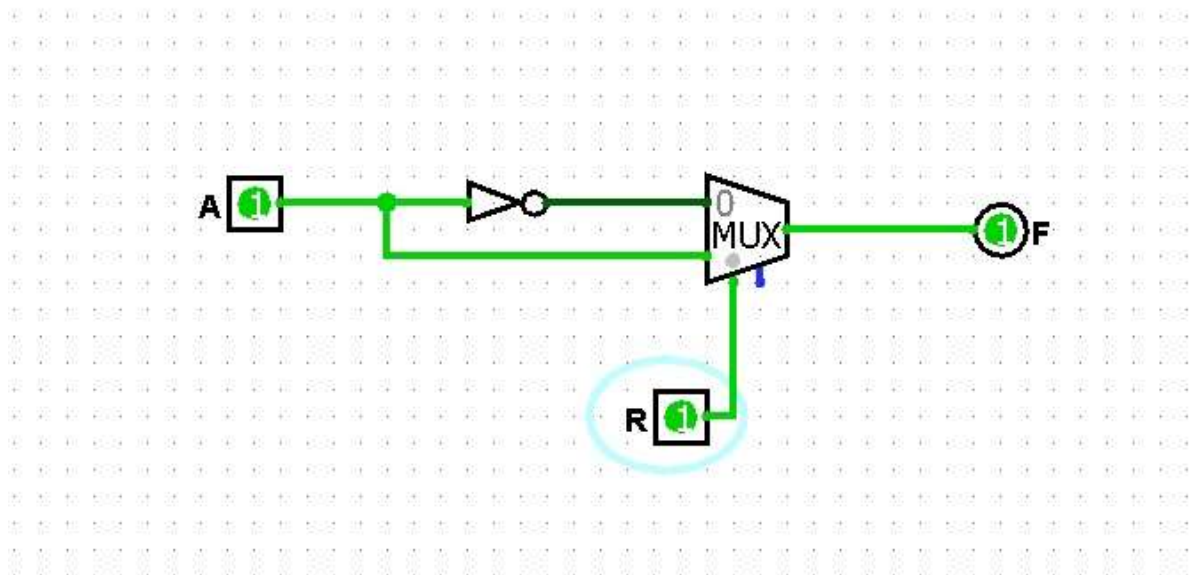


EC201 : Assignment 2

Problems based on simulations

1. Implement the XNOR gate using the multiplexer in Logisim.
Output should be in the form of your first name of 2 letters.
Design in Logisim.



Combinational Analysis

File Edit Project Simulate Window Help

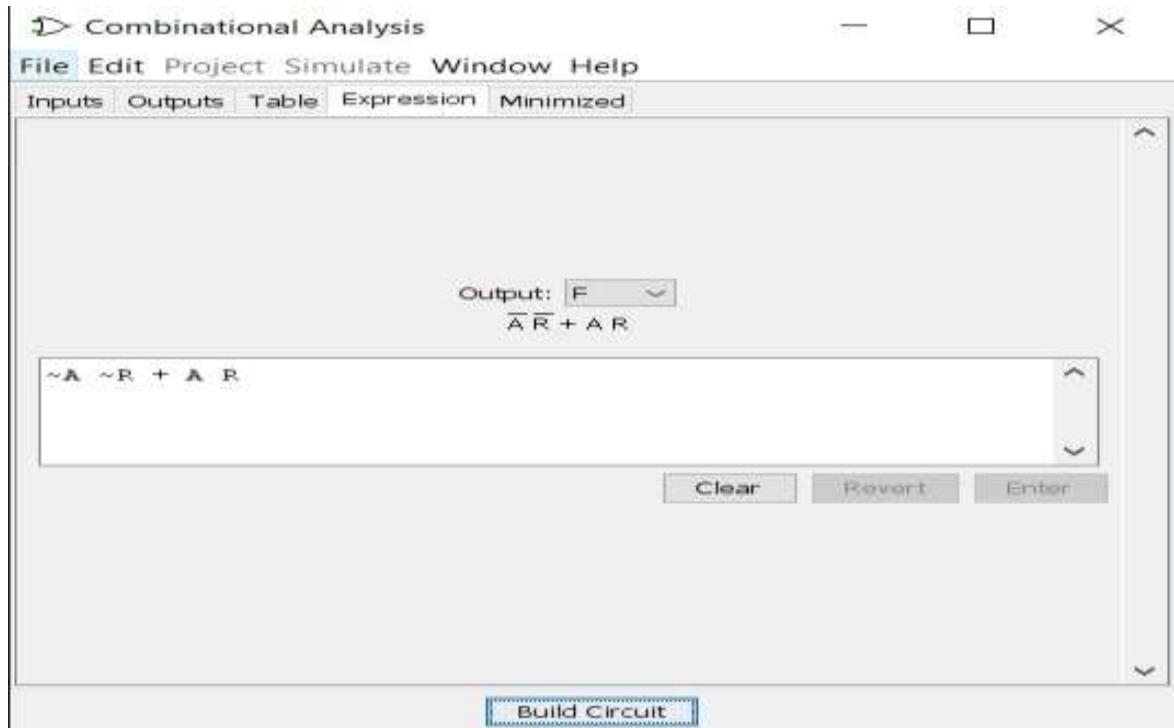
Inputs Outputs Table Expression Minimized

A	R	F
0	0	1
0	1	0
1	0	0
1	1	1

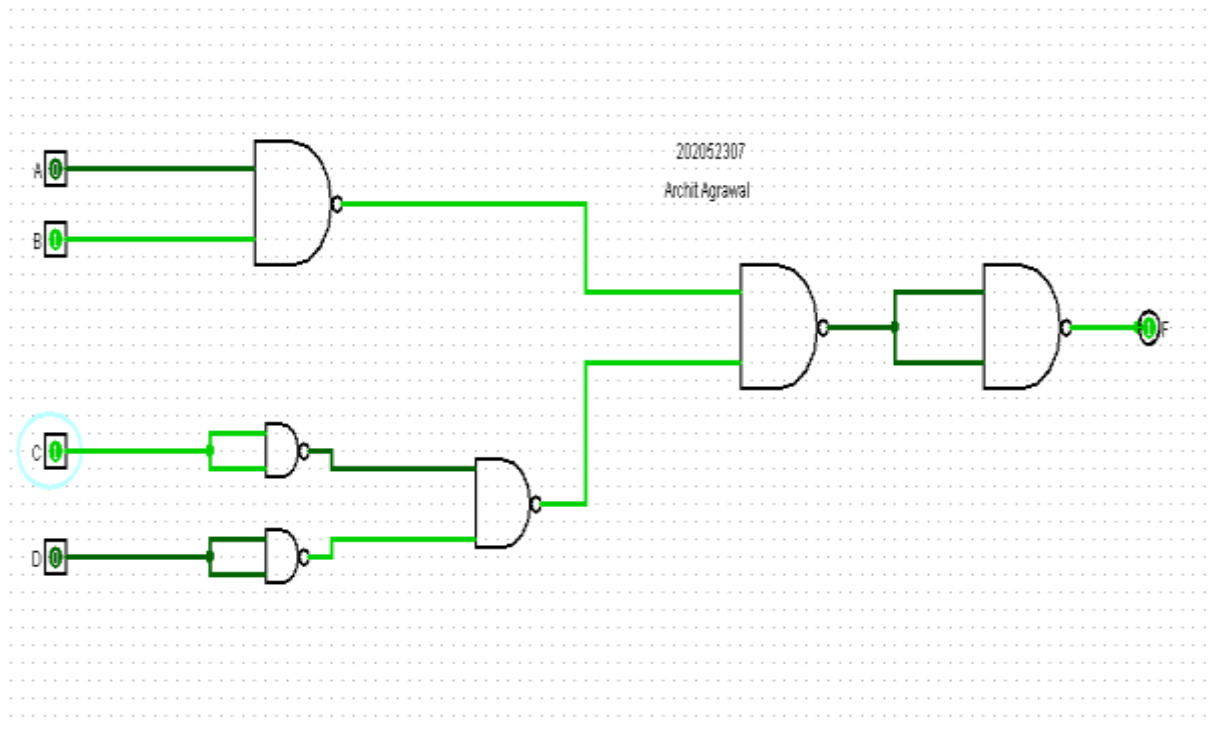
Build Circuit

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2. Implement $F=(A'+B')(C+D)$ using 2 input NAND gates in Logisim.



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A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Output:

Format:

		C, D			
		00	01	11	10
A, B	00	0	1	1	1
	01	0	1	1	1
	11	0	0	0	0
	10	0	1	1	1

$$\bar{A}D + \bar{B}D + \bar{A}C + \bar{B}C$$

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3. $F(A,B,C,D)=\Sigma m(2,3,5,7,8,9,12)$ sketch and verify in Logisim.

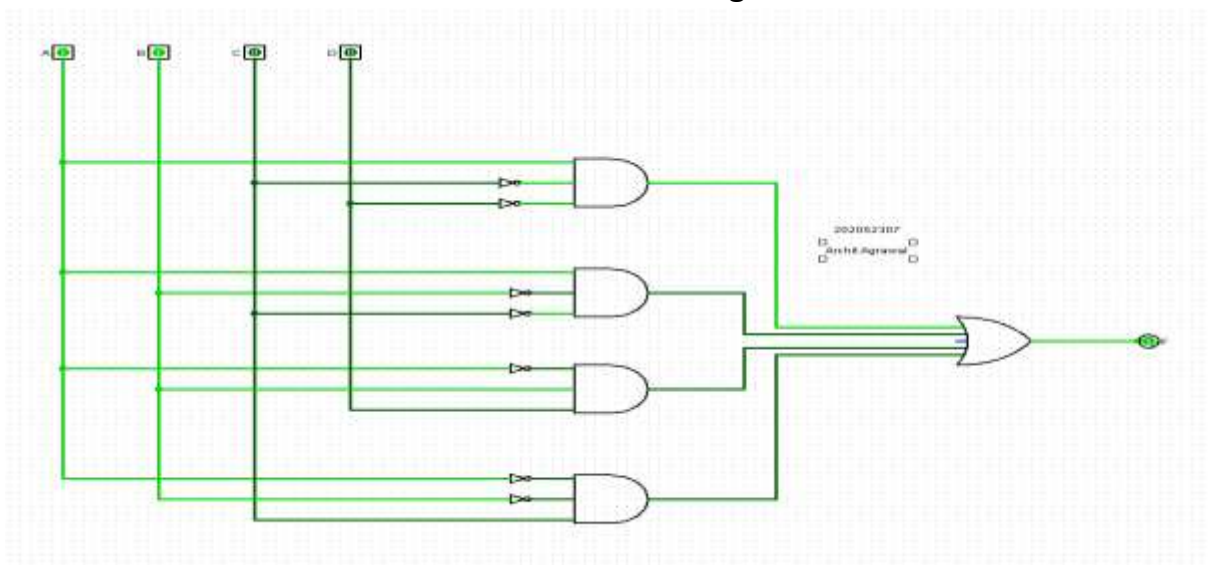
The K-Map with the possible pairs for the given function is:

CD \ AB	00	01	11	10
00			1	1
01		1	1	
11	1			
10	1	1		

Using K-Map we get:

$$F(A,B,C,D) = A\bar{C}\bar{D} + A\bar{B}\bar{C} + \bar{A}BD + \bar{A}\bar{B}C$$

Let us draw the circuit for above function in Logisim:



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A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Output:

Format:

C, D

		00	01	11	10
A, B	00	0	0	1	1
	01	0	1	1	0
	11	1	0	0	0
	10	1	1	0	0

$\bar{A}\bar{B}C + \bar{A}BD + A\bar{B}\bar{C} + A\bar{C}\bar{D}$

We can now easily verify the K-Map and the expression that we formed and that we got from Logisim. Hence, the given function is verified.

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Problems: Without the Simulations

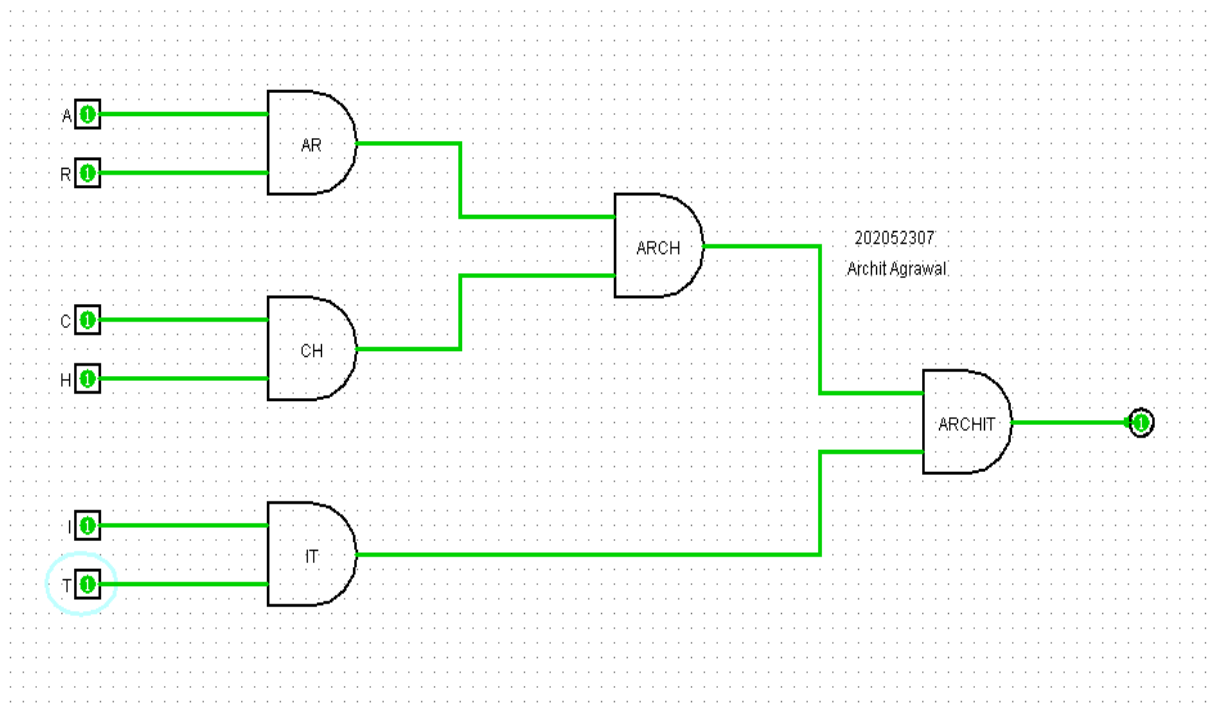
4. Take your roll number digits and add them if sum is even number then realize your first name by using the two input NAND gates only else using the basic gates.

Solution:

Student ID = 202052307

Sum = $2 + 0 + 2 + 0 + 5 + 2 + 3 + 0 + 7 = 21$ (odd).

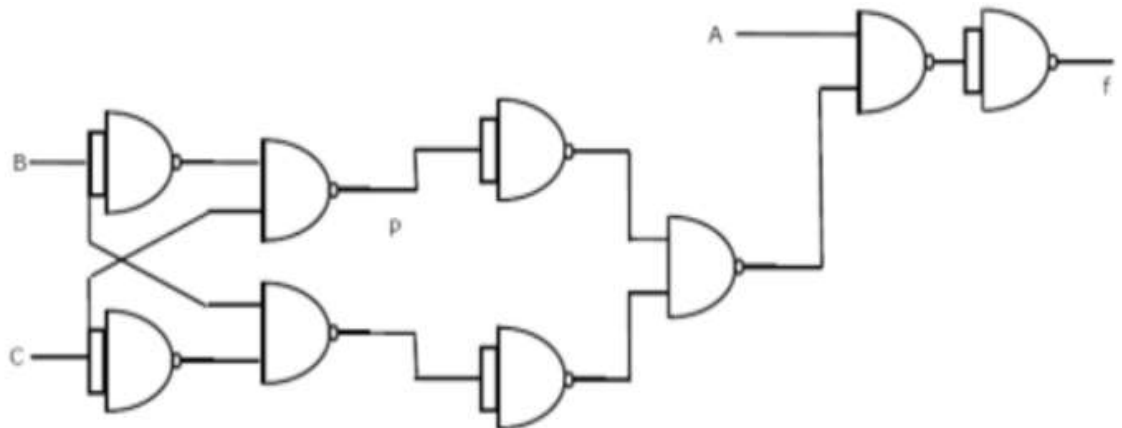
Therefore, I have to use basic gates to realize my name.



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5. Find the output for the circuit given below.



Date: ____/____/____

The handwritten diagram shows the same logic circuit as above. The output of the first AND gate in the top path is labeled $\overline{B} \cdot C$. The output of the first AND gate in the bottom path is labeled $\overline{B} \cdot \overline{C}$. The output of the second AND gate in the top path is labeled $\overline{B} \cdot C$. The output of the second AND gate in the bottom path is labeled $B \cdot \overline{C}$. The output of the third AND gate is labeled $(\overline{B} \cdot C) \cdot (B \cdot \overline{C})$. The output of the final AND gate is labeled f .

The expression for above circuit is:

$$f = A \cdot (\overline{B} \cdot C) \cdot (B \cdot \overline{C})$$
$$f = A \cdot (\overline{B} \cdot C + B \cdot \overline{C}) \quad (\text{De Morgan's Law})$$
$$f = A \cdot (B + \overline{C} + \overline{B} + C) \quad (\text{De Morgan's Law})$$
$$f = A \cdot ((B + \overline{B}) + (C + \overline{C}))$$
$$f = A \cdot 1 \quad (\because B + \overline{B} = 1 \text{ and } C + \overline{C} = 1 \text{ and } 1 + 1 = 1)$$
$$\therefore f = A$$

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