Started on	Wednesday, 2 March 2022, 12:10 PM
State	Finished
Completed on	Wednesday, 2 March 2022, 12:14 PM
Time taken	4 mins 33 secs
Marks	2.00/7.00
Grade	**2.86** out of 10.00 (**29**%)

Question **1**

Incorrect

Mark 0.00 out of 1.00

Which one of the following about the MIPS rating of a computer is FALSE?

- a. MIPS rating of computer depends on the computer being used
- b. MIPS rating of a computer can very based on which instruction of a processor are being considered ✖
- c. None of the mentioned
- d. MIPS rating of a processor is independent of the program is being executed.

Your answer is incorrect.

The correct answer is:
MIPS rating of a processor is independent of the program is being executed.

Question **2**

Incorrect

Mark 0.00 out of 1.00

DIV.D F0,F2,F4

ADD.D F6,F0,F8

S.D F6,0(R1)

SUB.D F8,F10,F14

MUL.D F6,F10,F8

How many possible hazards are available in the above-given code?

- a. 5
- b. 3
- c. 4 ✖
- d. 2

Your answer is incorrect.

The correct answer is:
3

Question **3**

Incorrect

Mark 0.00 out of 1.00

In MIPS architecture, increasing the number of stages --

- a. Will always improve the performance. ✖
- b. Will always decrease the performance.
- c. Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease
- d. Will always improve the performance after the optimal value of the stages

Your answer is incorrect.

The correct answers are:
Will always decrease the performance.,

Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Question **4**

Correct

Mark 1.00 out of 1.00

The processor speed has been increased over the last five decades due the --

- a. Krammar's Law
- b. Charl's law
- c. Newton's law
- d. Moore's Law ✔

Your answer is correct.

The correct answer is: Moore's Law

Question **5**

Incorrect

Mark 0.00 out of 1.00

For the code given below choose the wrong answer.

MIPS Code:

1. ADD r1, r2, r3
2. SUB r4, r1, r5
3. AND r6, r1, r7
4. OR r8, r1, r9
5. XOR r10, r1, r11

- a. Direct data dependence is there ✖
- b. Using split phase of the clock, data hazard can be eliminated from instruction no. fifth
- c. Using split phase of the clock, data hazard can be eliminated from instruction no. second
- d. Using split phase of the clock, data hazard can be eliminated from instruction no. fourth

Your answer is incorrect.

The correct answer is:
Using split phase of the clock, data hazard can be eliminated from instruction no. second

Question **6**

Correct

Mark 1.00 out of 1.00

For the code given below. Select the right option.

```
if p1 {
S1;
};
if p2 {
S2;
};
```

- a. All of the mentioned ✔
- b. S1 cannot be moved before the branch
- c. S1 is control dependent on p1, but S2 is not control dependent on p1
- d. S2 cannot be moved after the branch

Your answer is correct.

The correct answers are: S1 is control dependent on p1, but S2 is not control dependent on p1, S1 cannot be moved before the branch, All of the mentioned

Question **7**

Incorrect

Mark 0.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 5 ns. What is the Pipeline cycle time?

- a. 95 ns
- b. 105 ns
- c. 75 ns
- d. 100 ns ✖

Your answer is incorrect.

The correct answer is:
95 ns

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