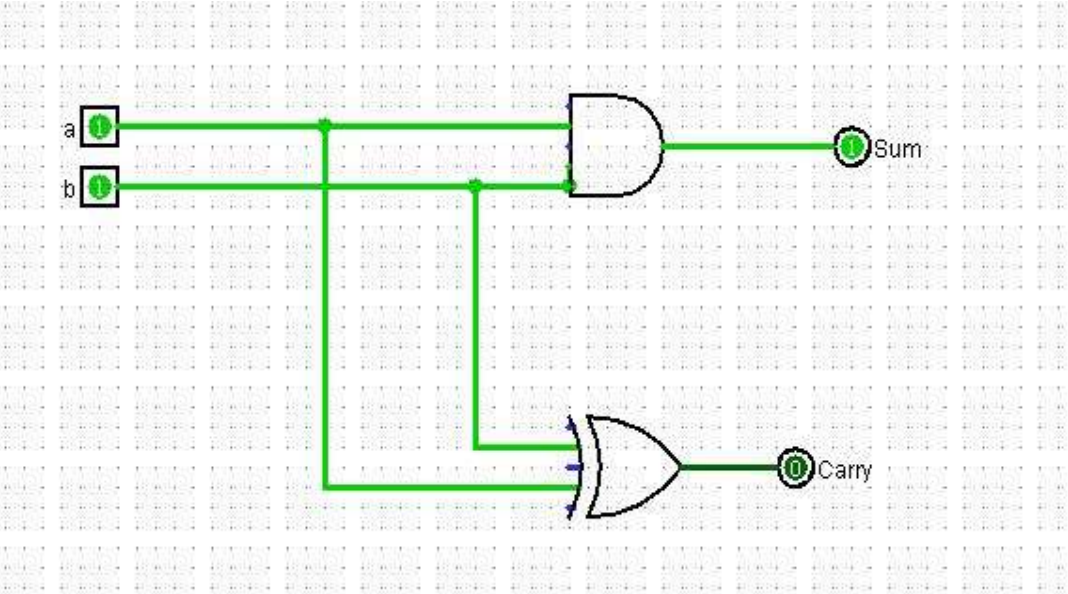
EC201 : Assignment 3

Problems with simulations

1. **Draw two truth tables illustrating the outputs of a half-adder, one table for the sum output and the other for the output and Design in Logisim**

   ***Solution*:**

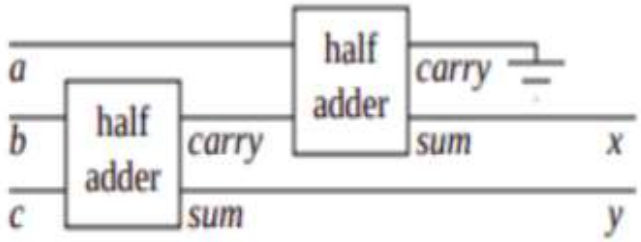


a	b	Sum	Carry
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

a	b	Carry
0	0	0
0	1	1
1	0	1
1	1	0

a	b	Sum
0	0	0
0	1	0
1	0	0
1	1	1

2. **Fill in the truth table at right for the following circuit. Ignore rows not included in the table, then design in Logisim.**



a	b	c	x	y
0	1	1		
1	0	1		
1	1	0		
1	1	1		

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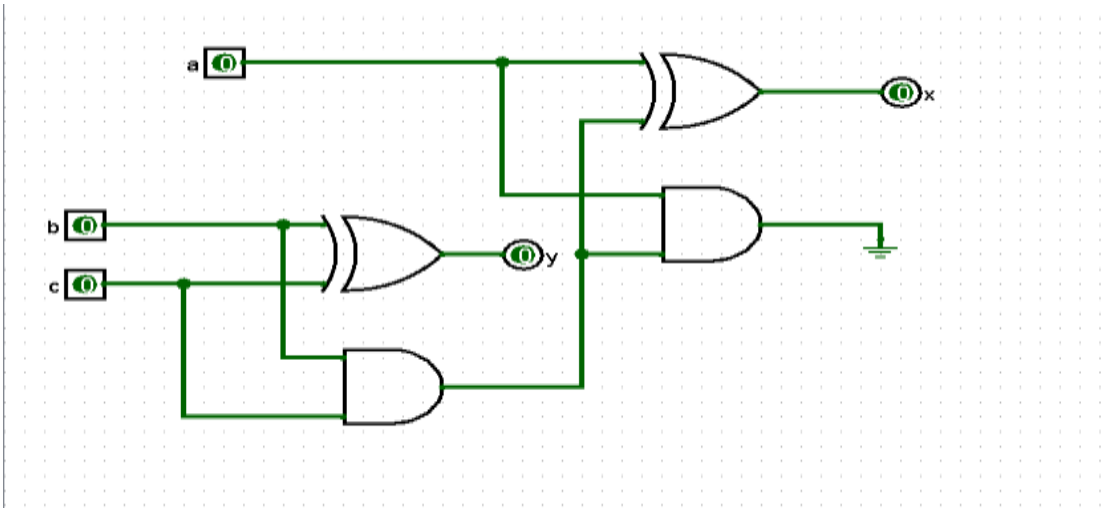
***Solution*:**



a	b	c	x	y
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Problems Without Simulations

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Problems Without Simulations

3. Two 1's with no carry-in are added using a full adder. What are the outputs?

given $A = 1$, $B = 1$, $C_{in} = 0$

$\because \quad S = A \oplus B \oplus C_{in}$

$= 1 \oplus 1 \oplus 0$

$S = 0$

$C_{out} = AB + C_{in}(A \oplus B)$

$= 1 + 0(1 \oplus 1)$

$C_{out} = 1$

$\therefore$ Outputs are $S = 0$ and $C_{out} = 1$

4. Two 1's with a carry-in of 1 are added using a full adder. What are the outputs?

$A = 1$, $B = 1$, $C_{in} = 1$

$S = A \oplus B \oplus C_{in}$

$= 1 \oplus 1 \oplus 1$

$S = 1$

$C_{out} = A \cdot B + C_{in}(A \oplus B)$

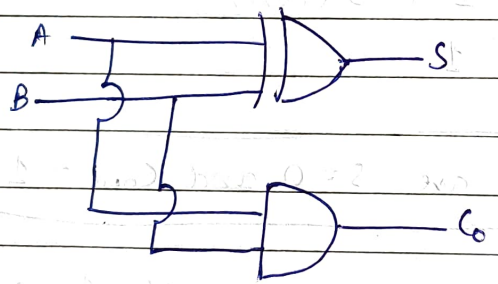
$= 1 + C_{in}(A \oplus B)$

$C_{out} = 1$

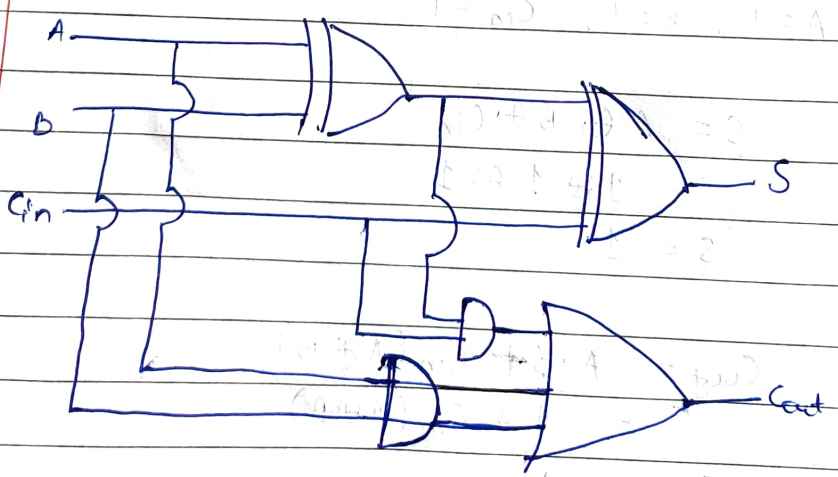
∴ Outputs are: S = 1 and Cout = 1

5. A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of AND/OR gate is 1.2 us. A 4-bit ripple carry binary adder is implemented by using full adders. Find out total propagation time of this 4-bit binary adder in us.

Half Adder



Full Adder:



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- from A or B to C_{out} : 4 gate delays (XOR → AND → OR)
- from A or B to S : 4 gate delays (XOR → XOR)
- from C_{in} to C_{out} : 2 gate delays (AND → OR)
- from C_{in} to S : 2 gate delay (XOR)

because C_{out} of one stage is C_{in} for the next input :

- 4-gate delays from generating first carry signal (A or B to C_{out}).
- 2-gate delays per intermediate stage (C_i to C_{i+1})
- 2-gate delays at last stage to produce both the sum and carry-out outputs (C_{n-1} to C_n and S_{n-1})

For an n-bit full adder, total propagation delay

$$t_p = 4 + 2(n-2) + 2$$

$$t_p = 2n + 2$$

For 1-bit full adder, $t_p = 4$

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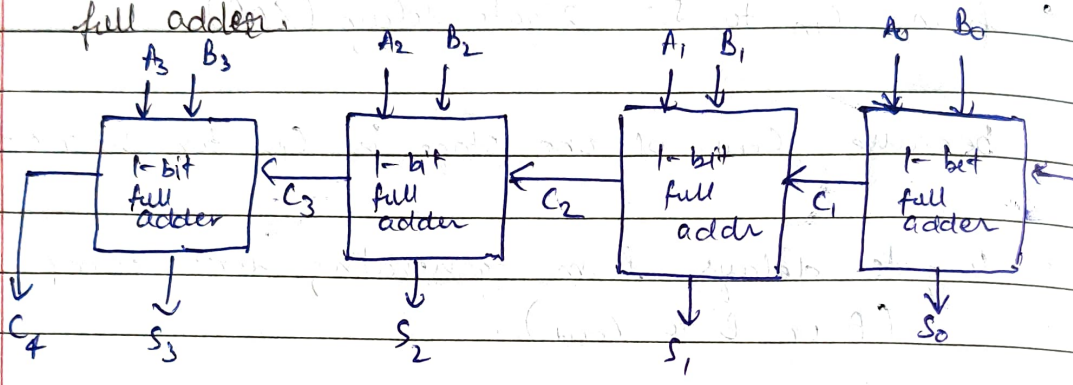
∴ total delay of a 1-bit full adder is

$$t = 4 \times 1.2$$
$$= 4.8\ \mu s$$

Diagram of 4-bit ripple adder using full adder.



delay of 4 full adders = $4 \times 4.8\ \mu s$
$= 19.2\ \mu s$