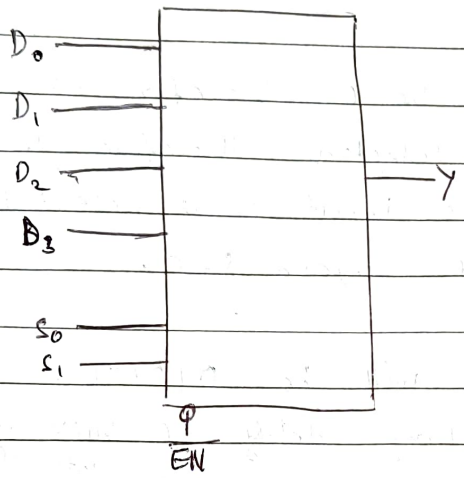
20205213

Date
Page

EC201 : Assignment 5

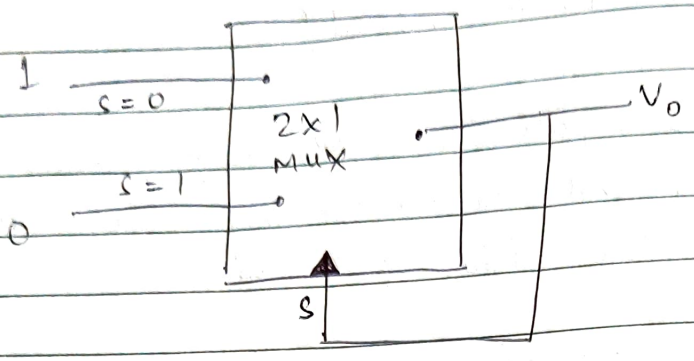
1. Let all D inputs be LOW, both S inputs be HIGH, and the enable input be LOW. What is the status of Y output?



Since, ~~enable~~ circuit is active when enable input is low (negative logic), therefore, using the select inputs multiplexer will direct to input D_3 as both S inputs are given high. Since D_3 is LOW, output Y will also be LOW in the given state of the inputs.

2. A 2 to 1 multiplexer having a switching delay of 1 us is connected as shown in the figure. The output of the multiplexer is tied to its own select input. The input which gets selected when $S=0$, is tied to 1 and the input that gets selected when $S=1$ is tied to 0. The output V_0 will be?

20205/2/13



Initially V_o will be 0, therefor $S = 0$,
∴ input 1 is selected, therefore $V_o = 1$,
∴ $S = 1$, hence, input 2 is selected,
hence $V_o = 0$, again $S = 0$.

∴ the output V_o will be 0 1 0 1 0 1 ---
Since, the switching delay of MUX is 1 μs, therefore the time interval at which the output is repeated is 2 μs.

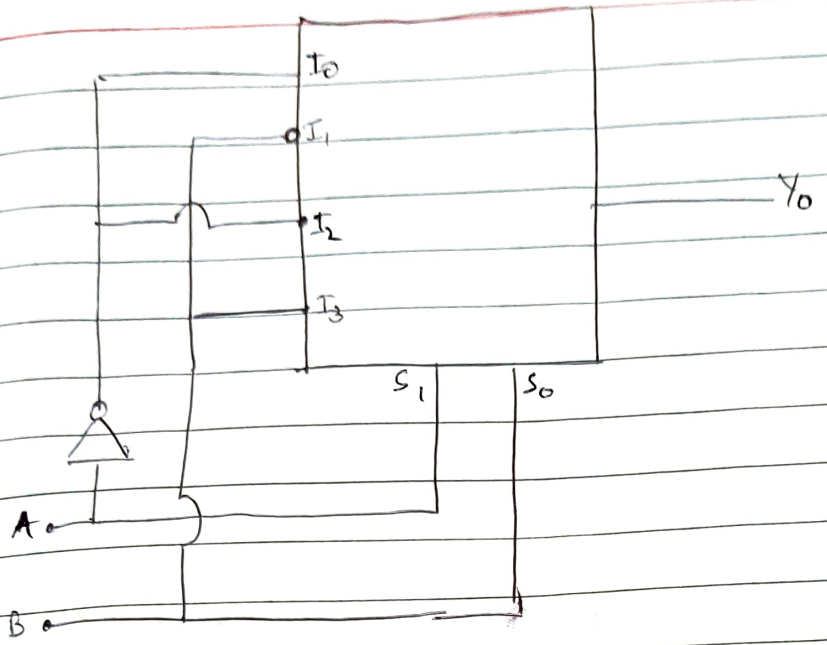
∴ frequency of output pulse = $\frac{1}{2\,\mu s} = 0.5$ MHz

∴ V_o will be a pulse of 0 and 1 of frequency 0.5 MHz.

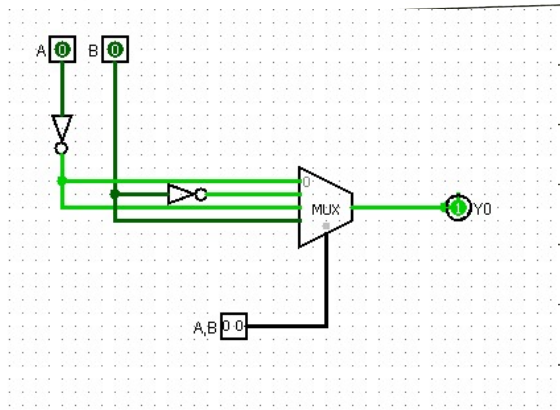
Problems based on Simulations

3. Realize Y_o using 4 x 1 MUX. Design in Logisim. Find out Y_o.

20205123



The circuit designed in logisim:



The truth table obtained from the software:

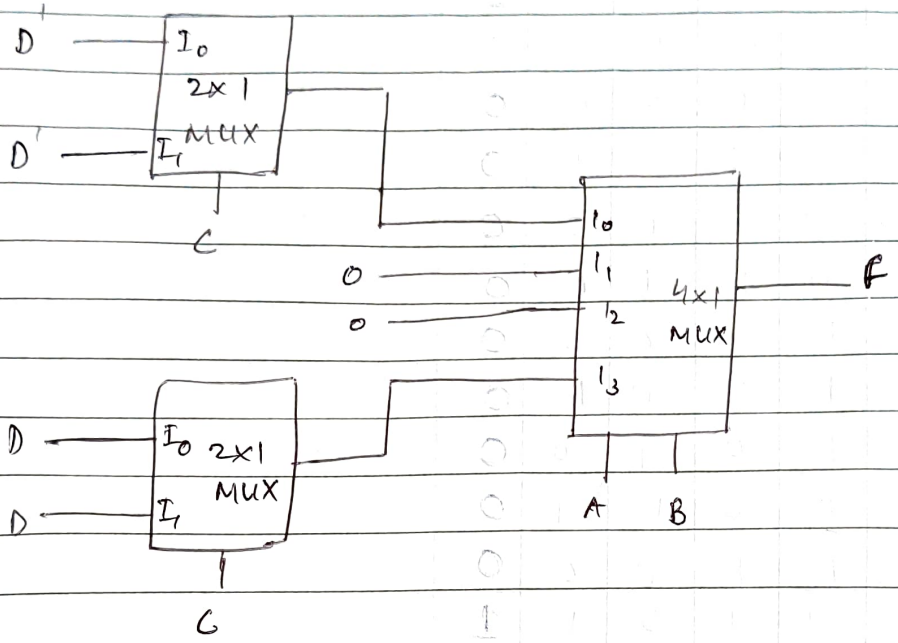
$S_1 = A$	$S_0 = B$	$I_0 = \overline{A}$	$I_1 = \overline{B}$	$I_2 = \overline{A}$	$I_3 = B$	Y_0
0	0	1	1	1	0	1
0	1	1	0	1	1	0
1	0	0	1	0	0	0
1	1	0	0	0	1	1

This is clearly the XNOR operation

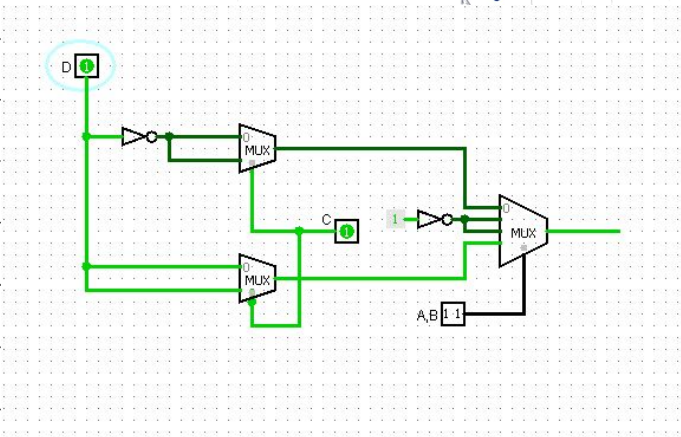
$\therefore$ Y_0 = A xnor B

20/05/23

4. Determine the output and design in Logisim software.



The circuit designed in Logisim:

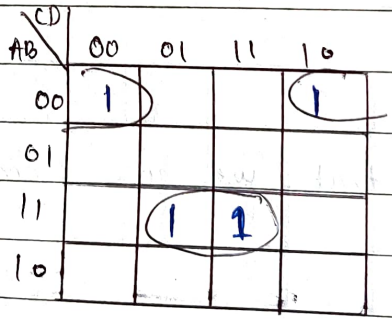


The truth table that we got from the software is -

202051213

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

The K-map for this truth table is:

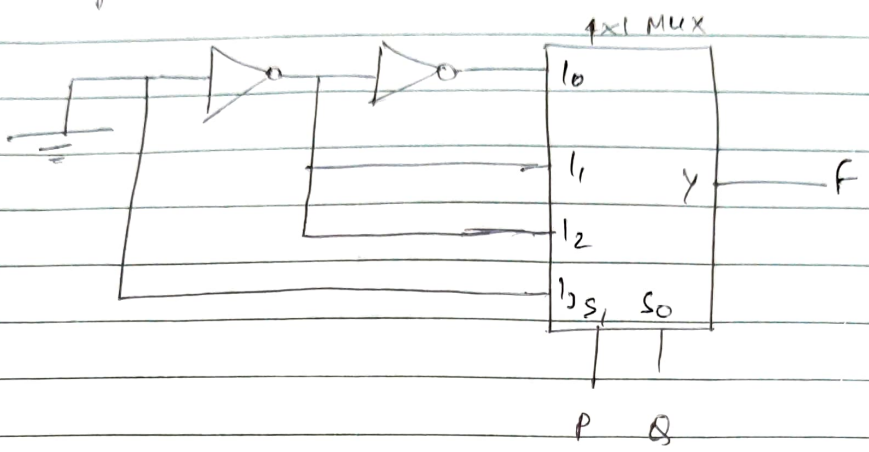


the possible pairings are shown:

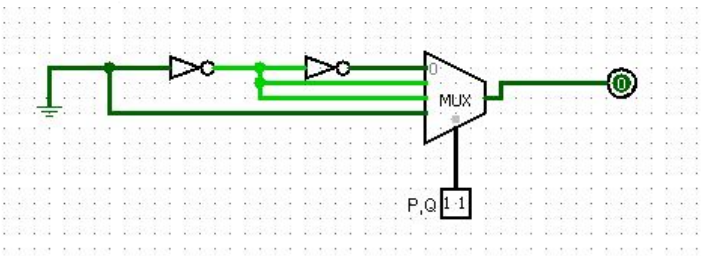
$\therefore F = ABD + \bar{A}\bar{B}\bar{D}$

20200513

(5) Determine the output function F and design in Logisim software



The circuit designed in Logisim:



The truth table obtained from the software is:

P	Q	I_0	I_1	I_2	I_3	F
0	0	0	1	1	0	0
0	1	0	1	1	0	1
1	0	0	1	1	0	1
1	1	0	1	1	0	0

Clearly it is XOR operation,

$\therefore F = P \text{ xor } Q$