# LAB3: Single Cycle CPU

# **EE 312 Computer Architecture**

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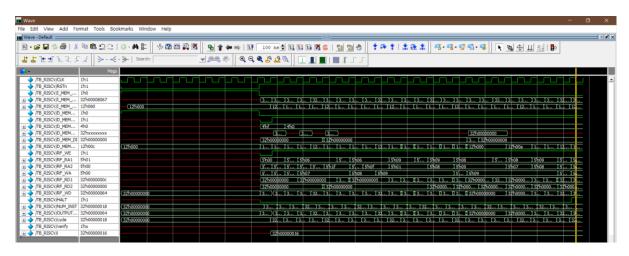
20150146 Sanghyun Kim

## Inst test:

### Transcript:

```
VSIM 16> run -all
 # Test #
            1 has been passed
  Test #
            2 has been passed
            3 has been passed
  Test #
  Test #
            4 has been passed
  Test #
            5 has been passed
            6 has been passed
  Test #
            7 has been passed
  Test #
  Test #
            8 has been passed
            9 has been passed
  Test #
           10 has been passed
  Test #
  Test #
           11 has been passed
  Test #
           12 has been passed
  Test #
           13 has been passed
  Test #
           14 has been passed
  Test #
           15 has been passed
  Test #
           16 has been passed
           17 has been passed
  Test #
           18 has been passed
  Test #
  Test #
           19 has been passed
           20 has been passed
  Test #
  Test #
           21 has been passed
           22 has been passed
  Test #
                 24 cycle
  Finish:
  Success.
                     : C:/Users/iamarohan/Desktop/lab33/TB_RISCV_inst.v(174)
```

## Wave:



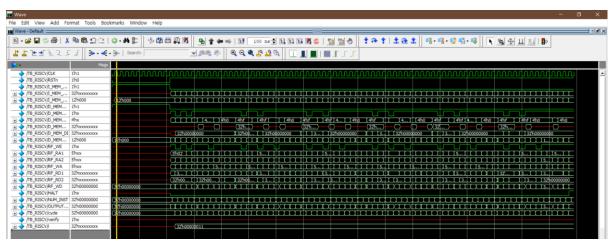
## forloop test:

## transcript:

```
VSIM 11> vsim -gui work.TB_RISCV work.SW_byteset work.Simple_ALU work.RISCV_TOP wor
work.ALU
# vsim
# Start time: 15:17:25 on Oct 10,2018
# Loading work.TB_RISCV
# Loading work.RISCV_CLKRST
# Loading work.RISCV TOP
# Loading work.Control
# Loading work.ALU_Control
# Loading work.ALU
# Loading work.Simple_ALU
# Loading work. Immediate
# Loading work.LW_byteset
# Loading work.SW byteset
# Loading work.Data BE
# Loading work.Multiplexer
# Loading work.SP SRAM
# Loading work.REG FILE
add wave -position end sim:/TB_RISCV/*
VSIM 13> run -all
# Test #
             1 has been sucess!
# Test #
             2 has been sucess!
# Test #
             3 has been sucess!
 # Test #
            4 has been sucess!
# Test #
             5 has been sucess!
# Test #
            6 has been sucess!
# Test #
            7 has been sucess!
 # Test #
             8 has been sucess!
             9 has been sucess!
  Test #
# Test #
           10 has been sucess!
# Test #
           11 has been sucess!
           12 has been sucess!
# Test #
           13 has been sucess!
14 has been sucess!
# Test #
# Test #
 # Test #
           15 has been sucess!
# Test # 16 has been sucess!
# Test # 17 has been sucess!
# Finish:
                   73 cycle
# Success.
  ** Note: $finish : C:/Users/iamarohan/Desktop/lab33/TB_RISCV_forloop.v(168)
Time: 845 ns Iteration: 1 Instance: /TB_RISCV
```

\*\* I spelled success wrong @ forgive me

## Wave:

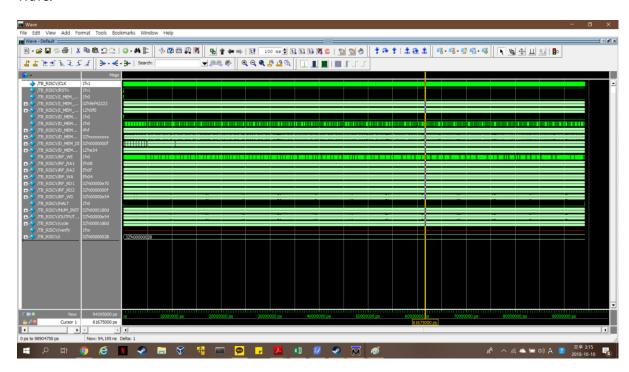


## sort test:

## Transcript

```
add wave -position end sim:/RISCV_TOP/*
VSIM 7> run -all
# Test #
           1 has been success!
           2 has been success!
 Test #
           3 has been success!
# Test #
           4 has been success!
           5 has been success!
6 has been success!
 Test #
 Test #
 Test #
           7 has been success!
 Test #
           8 has been success!
 Test #
           9 has been success!
          10 has been success!
 Test #
 Test #
          11 has been success!
          12 has been success!
 Test #
          13 has been success!
          14 has been success!
 Test #
          15 has been success!
 Test #
 Test #
          16 has been success!
 Test #
          17 has been success!
 Test #
          18 has been success!
 Test #
          19 has been success!
          20 has been success!
 Test #
 Test #
          21 has been success!
 Test #
          22 has been success!
          23 has been success!
 Test #
          24 has been success!
 Test #
 Test #
          25 has been success!
 Test #
          26 has been success!
 Test #
          27 has been success!
          28 has been success!
 Test #
 Test #
          29 has been success!
 Test #
          30 has been success!
 Test #
          31 has been success!
 Test #
          32 has been success!
          33 has been success!
 Test #
 Test #
          34 has been success!
 Test #
          35 has been success!
          36 has been success!
 Test #
          37 has been success!
 Test #
          38 has been success!
 Test #
 Test #
         39 has been success!
         40 has been success!
9408 cycle
 Test #
 Finish:
 Success.
```

### Wave:



## Wave (zoomed in):

