EE312 Lab2 – Simulation results

EE312 Computer Architecture

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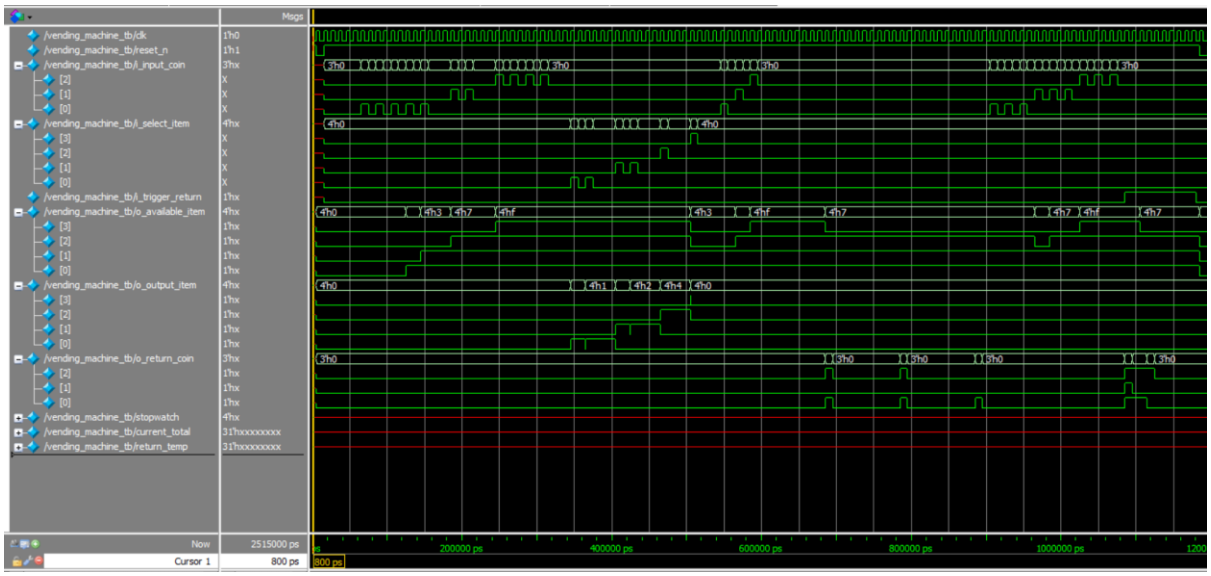
Transcript:

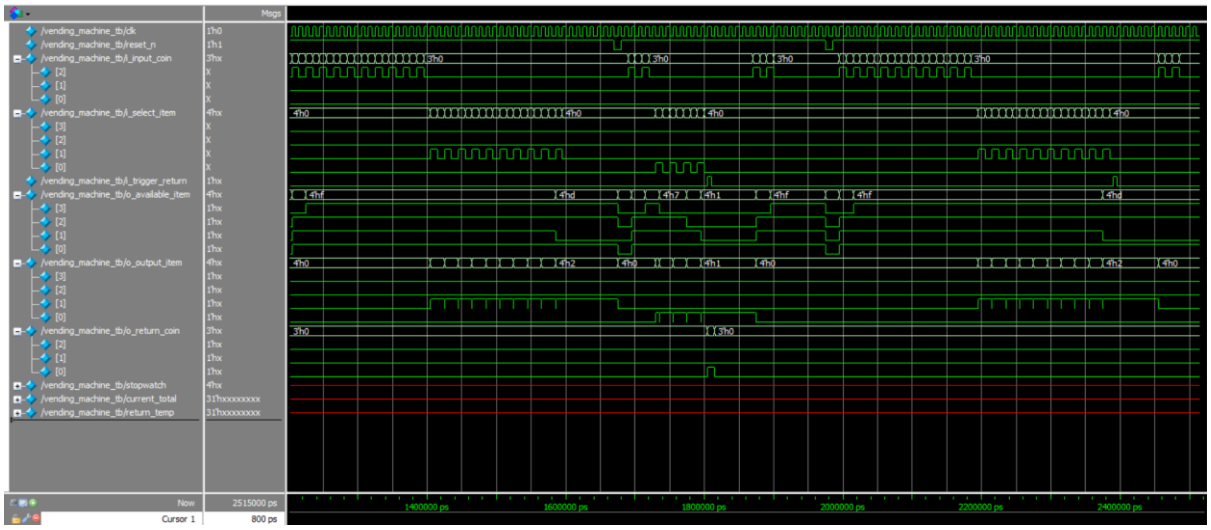
```
# TEST                      InitialTest :
# PASSED
# TEST                  Insert100CoinTest :
# PASSED
# TEST                  Insert500CoinTest :
# PASSED
# TEST                 Insert1000CoinTest :
# PASSED
# TEST                  Select1stItemTest :
# PASSED
# TEST                  Select2ndItemTest :
# PASSED
# TEST                  Select3rdItemTest :
# PASSED
# TEST                  Select4thItemTest :
# PASSED
# TEST                     WaitReturnTest :
# PASSED
# TEST                  TriggerReturnTest :
# PASSED
# TEST                       ItemTestTest :
# PASSED
# TEST                       ItemTestTest :
# PASSED
# TEST                       ItemTestTest :
# PASSED
# Passed = 13, Failed = 0
```

As we can see from the above, we pass all the tests in the provided testbench.

Wave simulation result 1:



Wave simulation result 2:



From the wave simulation result, we can see how different output signals react correctly on the input signals. For example, when i_input_coin signal is increased, the o_available_item signal increases incrementally. This shows that our lab was done correctly.

Another noteworthy element is how the stopwatch, current_total, and return_temp is signified with a red line. I believe this is because they are not input or output signals but a register that is defined as inputs and output of vending_machine.v just for the sake of the lab.