Ahsanullah University of Science and Technology (AUST)

Department of Computer Science and Engineering

LAB REPORT

Course No: CSE2210

Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number: 03

Name of the Experiment: Study of a TTL NAND gate with totem-pole output.

Submitted By: **Group 05**	
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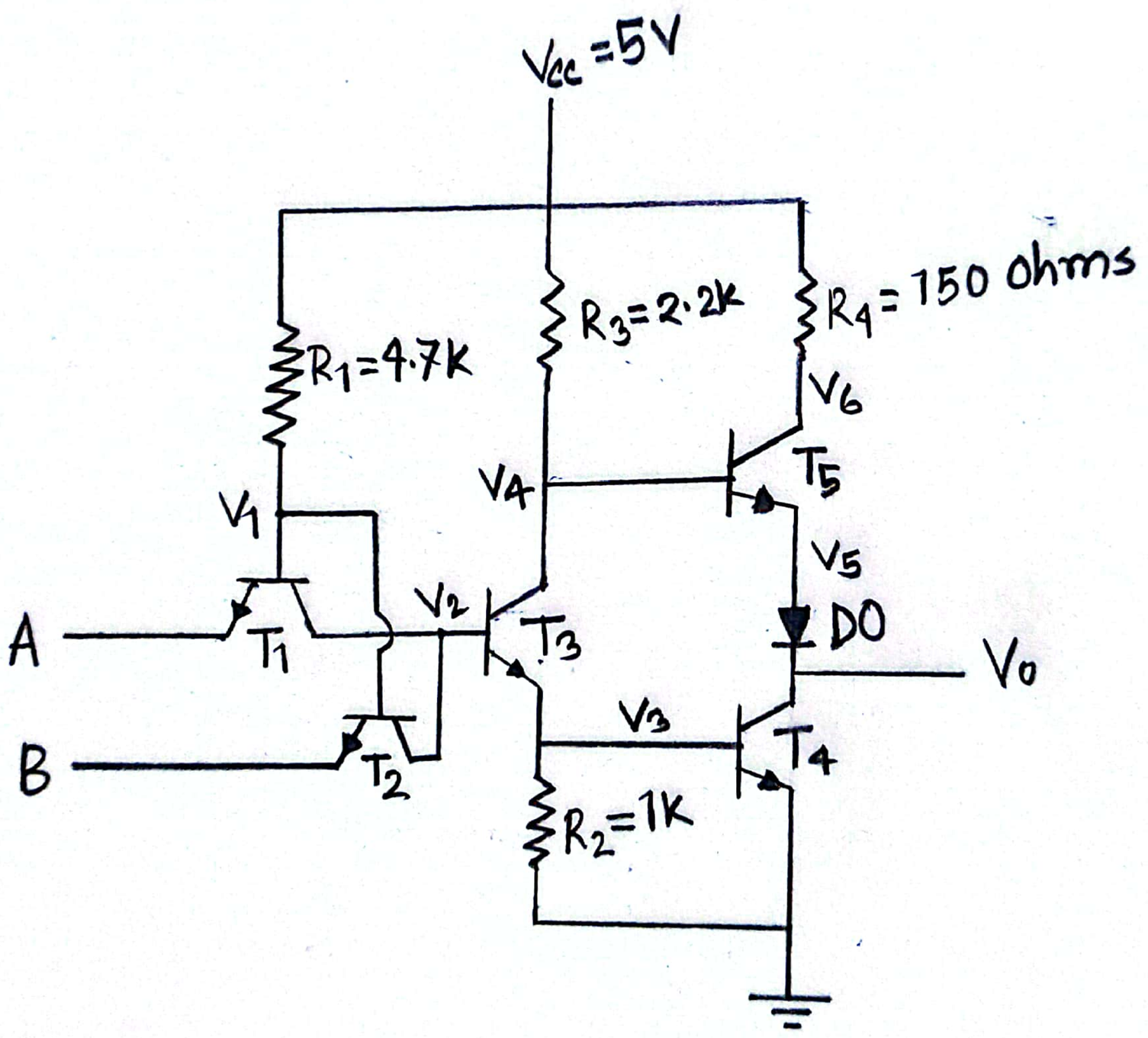
Objective: The objective of the experciment is to study of a TTL NAND Gate with totempole output and measurce the voltages at varcious points forc all possible input combinations and find out the noise marcgin.

Circuit Diagram:



Question No-01: Analyze the operation of TTL NAND gate with the expercimental data.

Answerc: In this expercirment, we have implemented a TTL NAND GIAte. After implementing, the output voltage we get:

A	B	V_o
0	0	4.31
0	1	4.31
1	0	4.31
1	1	0.01

From table, we can see that, for first three combination, the output is high and for the last combination, output is low. So, this circuit works like a TTL ~~or~~ NAND Gate.

Question no-02: What are the differences of transistors T_1 and T_2 with that of a ~~multi-emi-~~ multi-emitter transistor?

Answer: In a multi-emitter transistor, there is a connection between every emitter with a diode which worked as an input diode. In T_1 and T_2, there is no connection between emitter and diode. In multi-emitter transistor, a low input or any two of transistor pulls the base low. So, the collector stops the flow of current. It means, the collector current depends on these two transistors.

Question No-03: What is totem-pole stage? Why it is used in place of passive pull up resistor?

Answer: In this circuit totem-pole stage sits upon T_4 resistor. This configure is called totem-pole stage. Here, transistor T_5 acts as an active pull-up. If we decrease the value of a passive pull-up resistor, it increases the power discipation. When output is in its low-state, the voltage across passive pull-up resistor is $V_{CC}-V_{CE}$ (sat). To solve this problem, totem-pole stage is used in place of passive pull-up resistor.

Question No-04: What is the function of T_3?

Answer: The transistor T_3 acts as a phase spitter since the emitter voltage is a phase with the collector voltage.

Question No-05: Why resistor R_4 is used?

Answer: The R_4 R resistor is used to limit the current spikes when the transistor is in turn on state. The supply voltage would be short circuited if R_4 were missing. That's why R_4 resistor is used.

Question No-06: Why diode D0 is used in the circuit? Can it be placed elsewhere?

Answere: If the output diode D0 were missing, the base emitter voltage of T_5 would be $V_{BE_5} = V_{BE_5} - V_{CE4}$ $= 1 - 0.2 = 0.8V$ which put T_5 into saturation. So, T_5 into saturation and the wastage of current will occure if we don't use D0. The D0 can be placed from the emitter into the base of T_5. the configuration is also used by some manufactures.

Question No-07: Why two totem-pole gates cannot be wire ANDed?

Answere: Two totem-pole gates cannot be wire ANDed because if output from a gate is high and output from another gate is low and both are tied together, then large amount of curercent flown from Vcc to ground through high curercent flows state gate transistore and low state transistore And this curcrent can damage the output transistores.

Question No-08: What are the feature and advantages of TTL gates?

Answers:

1. TTL requires only one supply voltage.
2. It has good Fan-Out. TTL gates can drive upto 10 gates.
3. TTL gates exhibit low output impedance for high/low state.

Experimental Data:

A	B	V_0	V_1	V_2	V_3	V_4	V_5	V_6
0	0	4.31	0.53	0.01	0.00	5.00	4.71	5.00
0	1	4.31	0.55	0.03	0.00	5.00	4.71	5.00
1	0	4.31	0.55	0.03	0.00	5.00	4.71	5.00
1	1	0.01	1.66	1.16	0.58	0.61	0.37	5.00

Calculation:

NM(0): When all input 1, $V_2 + V_3 = 1.16 + 0.58$
$= 1.74$

So, $NM(0) = -(5 - 1.74)$
$= -3.26$ V

NM(1):

From the experiment, when at least one input is 1, $V_2 = 0.03$ V.

$$NM(1) = (1 - 0.03)\ V$$
$$= 0.97\ V.$$

Discussion: In this experiment, we worcked on a TTL NAND Gate with totem-pole output. We measured voltage of differcent point of the circuit and obsercne that voltage. Last of all, we measured the NM(0) and NM(1).