# Ahsanullah University of Science and Technology

## Department of Computer Science and Engineering

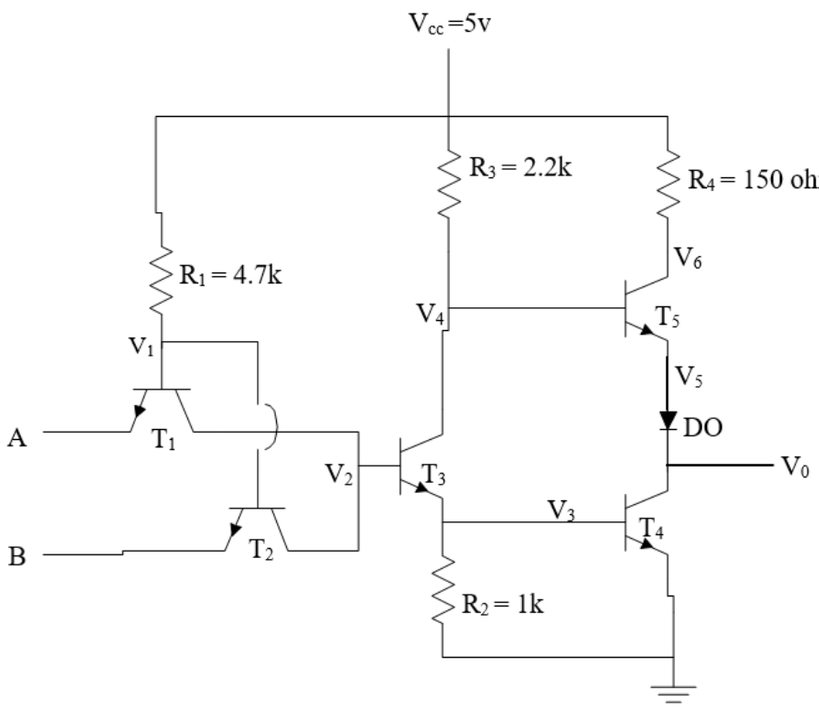
CSE 2210: Digital Electronics and Pulse Techniques Lab

Group: B1

Experiment # 3

**Name of the experiment: Study of a TTL NAND gate with totem-pole output.**

**Circuit Diagram:**




**Procedure:**

1. Measure the $V_0$, $V_1$, $V_2$, $V_3$, $V_4$, $V_5$ & $V_6$ for all possible input combinations.
2. Calculate noise margins.

**Questions:**

1. Analyze the operation of TTL NAND gate with the experimental data.
2. What are the differences of transistors $T_1$ & $T_2$ with that of a multi-emitter transistor? [Hint: Millman Sec 4-7,5-11]
3. What is totem-pole stage? Why it is used in place of passive pull-up resistor? [Hint: Millman Sec 5-12]
4. What is the function of $T_3$? [Hint: Millman Sec 5-12]
5. Why resistor $R_4$ is used? [Hint: Millman Sec 5-12]
6. Why diode D0 is used in the circuit? Can it be placed elsewhere? [Hint: Millman Sec 5-12]
7. Why two totem pole gates cannot be wire ANDed? [Hint: Millman pg. 151]
8. What are the features and advantages of TTL gates? [Hint: Millman Sec 5-15]

**Report:**

1. Objective.
2. Circuit diagram.
3. Answer to the questions.
4. Experimental data.
5. Calculations.
6. Discuss the findings.

**This is a theoretical explanation. Your NM(0) and NM(1) will change according to the measurement you have taken. Do not copy-paste these values directly to your lab report.**

**NM(0):**

Negative Spike:

For all inputs high, the output should be low. So, a negative spike will change the output to high. For the given circuit, if $T_3$ and $T_4$ will have to stop conducting to change the output to high.

We consider the case of the negative spike. We know that a diode will start conducting at 0.6 volts. emitter-base junction of $T_1$ and $T_2$ can be considered as a diode. So it will start conducting when it gets at least 0.6 volts.

When all input 1, Suppose $V_2 + V_3 = 1.44+0.728 = 2.168$ V. So, NM(0) = - (5-2.168) = -2.832V

**NM(1):**

Positive Spike:

If only one input is at V(1), and the other is at V(0), then if V(0) tends to increase we need only 0.5+0.5 = 1.0 volt at $T_3$'s base to make the path along $T_3$ -$T_4$ to conduct. Suppose, $V_2 = 0.025$V

NM(1) = 1 – 0.025 = 0.975 V