Ahsanullah University of Science and Technology

Department of Computer Science and Engineering

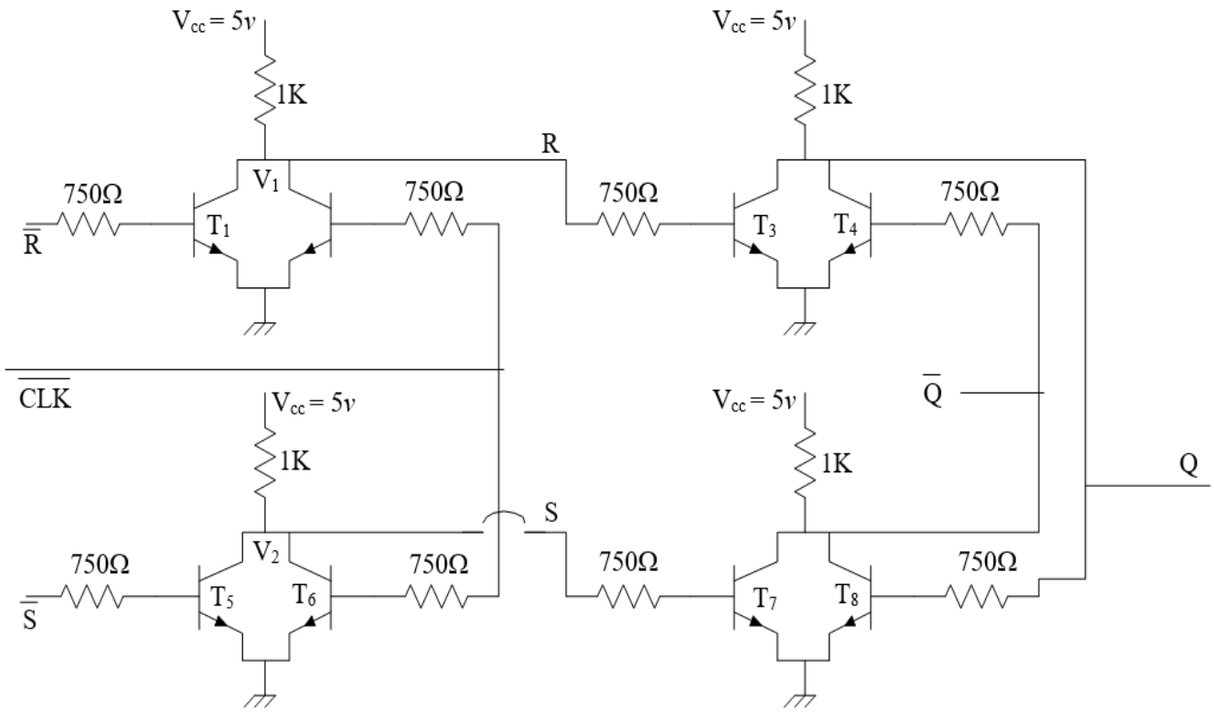
CSE 2210: Digital Electronics and Pulse Techniques Lab

Group: B1

Experiment # 5

Name of the Experiment: Implementation of clocked SR Flip Flop using RTL NOR gates.

Circuit Diagram:



Procedure:

1. Measure the output voltages at Q & $\overline{Q}$ and voltages V_1, V_2 for all possible input (S,R) combinations.

Questions:

1. Analyze the operation of SR FF with the experimental data.
2. What is the race-around condition in SR FF? Discuss with respect to the internal circuit.

Report:

1. Objective.
2. Circuit diagram.
3. Answer to the questions.
4. Experimental data.
5. Calculations.
6. Discuss the findings.

S’	R’	Q_{t+1}	State
1	1	Q_t	Hold
0	1	1	Set
1	0	0	Reset
0	0	-	Race Condition

Output Table:

S’	R’	Q	Q’
5V	0V	0.04	2.48
5V	5V		
0V	5V		
5V	5V		
5V	0V		
0V	0V		
0V	5V		
0V	0V		