

Preliminary

TMS320F2837xD Delfino Microcontrollers

Technical Reference Manual



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Read This First

About This Manual

This Technical Reference Manual (TRM) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F2837xD Microcontroller processors.

This TRM has been designated *Preliminary* because the documentation is in the formative or design phase of development. Texas Instruments reserves the right to change this TRM without notice. Visit the Texas Instruments website at <http://www.ti.com> to determine the latest version of this TRM.

Notational Conventions

These documents use the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

For a complete listing of related documentation and development-support tools for these devices, visit the Texas Instruments website at <http://www.ti.com>. Additionally, the *TMS320C28x CPU and Instruction Set Reference Guide* ([SPRU430](#)) and *TMS320C28x Floating Point Unit and Instruction Set Reference Guide* ([SPRUOE02](#)) must be used in conjunction with this TRM.

System Control

This chapter explains system control and interrupts found on this MCU. The system control module configures and manages the overall operation of the device and provides information about the device status. Configurable features in system control include reset control, NMI operation, power control, clock control, and low-power modes.

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1.1 Introduction

On this device, CPU1 acts as a master, and by default (upon reset), it owns all the configuration and control. Through software running on CPU1, peripherals and I/Os can be configured to be accessible by CPU2 and the configuration so chosen could be locked.

PLL clock configuration is also owned by CPU1 subsystem by default but a clock control semaphore is provided using which CPU2 can grab access to the clock configuration registers.

Each CPU has its own NMI module to handle different exceptions during run time. Any NMI exception unhandled before the NMIWD (NMI WatchDOG) timer expiration will reset the entire device if the NMI was on CPU1 and if the NMI was on CPU2 subsystem then CPU2 subsystem alone will get reset , in which case the CPU1 subsystem will be informed by another NMI that CPU2 subsystem got reset because of NMIWD timer expiration.

Each CPU subsystem has its own watchdog timer module for software to use. Watch dog timer expiration on CPU2 will reset CPU2 subsystem alone when configured to do generate a reset but watch dog timer expiration on CPU1 will reset the entire device.

Except for a CPU2 stand-alone internal resets like CPU2.NMIWD or CPU2.WD each time the device is reset, the CPU2 subsystem will be held under reset until CPU1 subsystem brings it out of reset. This is done by the boot ROM software running on CPU1 core.

The registers space of the device system control module is divided in to three categories as will be explained further in this chapter. They are :

1. System Control Device Configuration Registers (DEV_CFG_REGS), these registers are mapped to CPU1 only. The base address of these registers on CPU1 address space starts at 0x5D000.
2. System Control Clock Configuration Registers (CLK_CFG_REGS), these registers are mapped to both CPU1 and CPU2 address space but access control is based on a Clock Control Semaphore register. The base address of these registers on both the CPU is at 0x5D200.
3. System control CPU subsystem Registers (CPU_SYS_REGS), these registers are mapped to both the CPU subsystems. The base address of these registers on both the CPU is at 0x5D300.

This chapter explains the system control module on both the CPU subsystems.

1.2 System Control Functional Description

The system control module provides the following capabilities:

- Device identification and configuration registers
- Reset control
- Exceptions and Interrupt control
- Safety and error handling features of the device
- Power control
- Clock control
- Low Power modes
- Security module
- Inter-Processor Communication (IPC)

1.2.1 Device Identification

Device identification registers provide information on device class, device family, revision, part number, pin count, operating temperature range, package type, pin count and device qualification status.

All of the device information is part of the DEV_CFG_REGS space and is accessible only by the software running on the CPU1 subsystem.

The control subsystem device identification registers are: PARTIDL, PARTIDH, and REVID.

1.2.2 Device Configuration Registers

Several registers provide user with configuration information for debug/identification purposes on this MCU. This information tells user what peripheral features and how much RAM and FLASH memory are available on this part.

These registers are part of DEV_CFG_REGS space and are accessible only by the software running on CPU1 subsystem.

DC0 – DC20: Device Configuration or Capabilities registers, if a particular bit in these registers is set to '1' then the associated/feature or module is available in the device. Refer to section 1.12.2.1.3 to section 1.12.2.1.7 for more details.

PERCNF:- Peripheral configuration register, that configures ADC capabilities and enable/disable of USB internal PHY.

1.3 Reset Control

This section explains the reset sources for this device and aspects of hardware functions during reset as well as how system software should handle the reset cause and what boot ROM does to handle the reset cause.

1.3.1 Device Level Reset Sources

Table 1-1 shows various reset signals in this device and how it affects different hardware modules in the device.

Table 1-1. Reset Signals

No.	Reset Source	CPU1 Core Reset	CPU2 Core Reset (C28x, TMU, FPU, VCU)	JTAG / debug logic Reset	CPU1 subsystem	CPU2 subsystem	CPU2 held under reset?	Flash Pump	IOs	XRSn output
		(C28x, TMU, FPU, VCU)								
1.	POR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	HiZ	Yes
2.	XRSn Input	Yes	Yes	Yes	Yes	Yes	Yes	Yes	HiZ	---
3.	TRSTn	No	No	Yes	No	No	No	No	No Affect	No
4.	CPU1.WD RSn	Yes	Yes	Yes	Yes	Yes	Yes	Yes	HiZ	Yes
5.	CPU2.WD RSn	No	Yes	No	No	Yes	No	No	???	No
6.	CPU1.NMI WDRSn	Yes	Yes	Yes	Yes	Yes	Yes	Yes	HiZ	Yes
7.	CPU2.NMI WDRSn	No	Yes	No	No	Yes	No	No	???	No
8.	CPU1.HW BISTRSn	Yes	No	No	No	No	No	No	No Affect	No
9.	CPU2.HW BISTRSn	No	Yes	No	No	No	No	No	No Affect	No
10.	CPU1.DC SM.SCCR ESETn	Yes	Yes	Yes	Yes	Yes	Yes	No	HiZ	No
11.	CPU2.DC SM.SCCR ESETn	No	Yes	No	No	Yes	No	No	???	No

Table 1-1. Reset Signals (continued)

No.	Reset Source	CPU1 Core Reset	CPU2 Core Reset (C28x, TMU, FPU, VCU)	JTAG / debug logic Reset	CPU1 subsystem	CPU2 subsystem	CPU2 held under reset?	Flash Pump	IOs	XRSn output
12.	CPU1 Debugger Reset (from CCS)	Yes	Yes	No	Yes	Yes	Yes	Yes	HiZ	No
13.	CPU2 Debugger Reset (from CCS)	No	Yes	No	No	Yes	No	No	???	No
14.	HIBRESE_Tn	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No Affect	No
15.										

As shown in [Table 1-1](#), whenever CPU1 is reset, the entire device is reset, including the CPU2 core and subsystem. Apart from this whenever CPU2 subsystem is reset because of a reset to CPU1, the CPU2 subsystem is held under reset until software running on CPU1 brings it out of reset by writing to CPU2.RESCTL.RESET bit .

After a reset, the reset cause register (RESC) is updated with the reset cause. The bits in the reset cause register are sticky and maintain their state across multiple resets except when PMM module is the reset cause, in which case all the bits in the RESC register are cleared. Each subsystem has its own RESC register which is referred to as CPU1.RESC and CPU2.RESC respectively by CPU1 and CPU2 subsystems.

At any reset that resets the CPU1 core, the boot ROM code on the CPU1 Sub system will be run which brings out CPU2 out of reset and starts the application software as per the boot mode configured. Please refer to the boot ROM section in this document.

[Table 1-2](#) is the device bringup timeline on power up.

Table 1-2. Device Timeline

Timeline	CPU1 Subsystem	CPU2 Subsystem
T0	(Power Management Module (PMM) indicates that device is not yet fully powered and is in reset	Power Management Module (PMM) indicates that device is not yet fully powered and is in reset
T1:	CPU1 subsystem is out of reset and executes CPU-Boot ROM as explained in the boot ROM chapter <ul style="list-style-type: none"> • RESC check and action • PLL power up • Flash Power up • Switch to PLL output • RAM INITs • DCSM INIT • NMI • PLL BYPASS 	CPU2 subsystem held under reset
T2:	Bring CPU2 out of reset Emulation Boot or Standalone Boot or Hibernate Boot	CPU2 starts executing CPU2-BootROM <ul style="list-style-type: none"> • RE.SC check and action • RAM INIT • SM INIT • NMI

Table 1-2. Device Timeline (continued)

Timeline	CPU1 Subsystem	CPU2 Subsystem
T3	Read EMUBOOT MODE or Boot mode based on GPIO boot mode pins (explained in CPU1 boot ROM chapter)	EMU Boot Mode or Stand alone Boot Mode or Hibernate Boot Mode <ul style="list-style-type: none"> • Decode boot Mode (explained in CPU2 Boot ROM chapter)
T4	<ul style="list-style-type: none"> • If boot from flash, jump to flash • If boot from peripheral download application code from peripheral and save it in RAM and jump to start of application. • If wait Boot, enable PIE for C2TOC1 IPC support and enter WAIT BOOT MODE 	If CCS is connected (EMU Boot Mode) boot as per EMU BOOT MODE or go to WAIT Boot Mode If stand alone and not booting to flash (not CPU2 OTP BOOT MODE programmed), then enable PIE and enter IDLE mode
T5	Running Application on CPU1	CPU1 application decides how CPU2 should further boot, if CPU2 didn't boot to flash as configured in CPU2 OTP or CPU2 is already running application in CPU2 Flash.

1.3.2 Power-on Reset (POR)

The power-on reset (POR) circuit creates a clean reset throughout the device enabling glitchless GPIOs during the power-on procedure. The POR keeps the XRSn pin driven low during device power up. The power-on reset also resets the JTAG controller. While in most applications, the POR generated reset has a long-enough duration to also reset other system ICs, some applications may require a longer lasting pulse. In these cases, the XRSn reset pin (which is an open-drain) can also be driven low to match the time the device is held in a reset state with the rest of the system.

1.3.3 External Reset Input

The XRSn pin responds to an external reset signal (active LOW). The XRSn pin also drives the reset signal out of the chip to external circuitry whenever any of the internal Master Subsystem resets becomes active as shown in the above table. The internal resets which pull XRSn LOW are resets because of CPU1 Watch Dog modules (WDT0, WDT1 and NMIWD)

Whenever a POR condition exists, XRSn is also pulled LOW. Whenever CPU1 subsystem is reset by an XRSn condition it will hold the CPU2 subsystem in reset and bit1 of CPU1/2.RESC register will be set to indicate an XRSn caused the reset.

1.3.4 TRSTn

TBD

1.4 Exceptions and Interrupts Control

This device has exception capturing and handling ability which enables the device to be used in many safety critical applications. Device run-time exceptions that can be detected and acted upon include clock failure detection, memory access errors detection, bus fault detection, and interrupt handler address mismatch errors. This device also supports back-to-back, non-maskable interrupt handling capability along with highly configurable peripheral interrupt handling.

This device introduces an enhanced version of the PIE module named ePIE. This module doubles the interrupt handling capability of the legacy PIE from 96 to 192 interrupts.

Note that in this section, PIE and ePIE denote the same enhanced peripheral interrupt expansion module.

1.4.1 CPU1/CPU2 Enhanced PIE (ePIE)

The CPU1 and CPU2 subsystem each supports the peripheral interrupt expansion block to handle different exceptions and interrupts that occur during the device operation. The ePIE enables multiplexing of numerous interrupt sources into a smaller set of CPU interrupt inputs. The ePIE block can support up to 192 individual interrupts that are grouped into blocks of sixteen. Each group is fed into one of 12 core interrupt lines (INT1 to INT12). Each of the 192 interrupts is supported by its own vector stored in a dedicated RAM block that is modifiable. The CPU, upon servicing the interrupt, automatically fetches the appropriate interrupt vector. It takes nine CPU clock cycles to fetch the vector and save critical CPU registers. Therefore, the CPU can respond quickly to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the ePIE block.

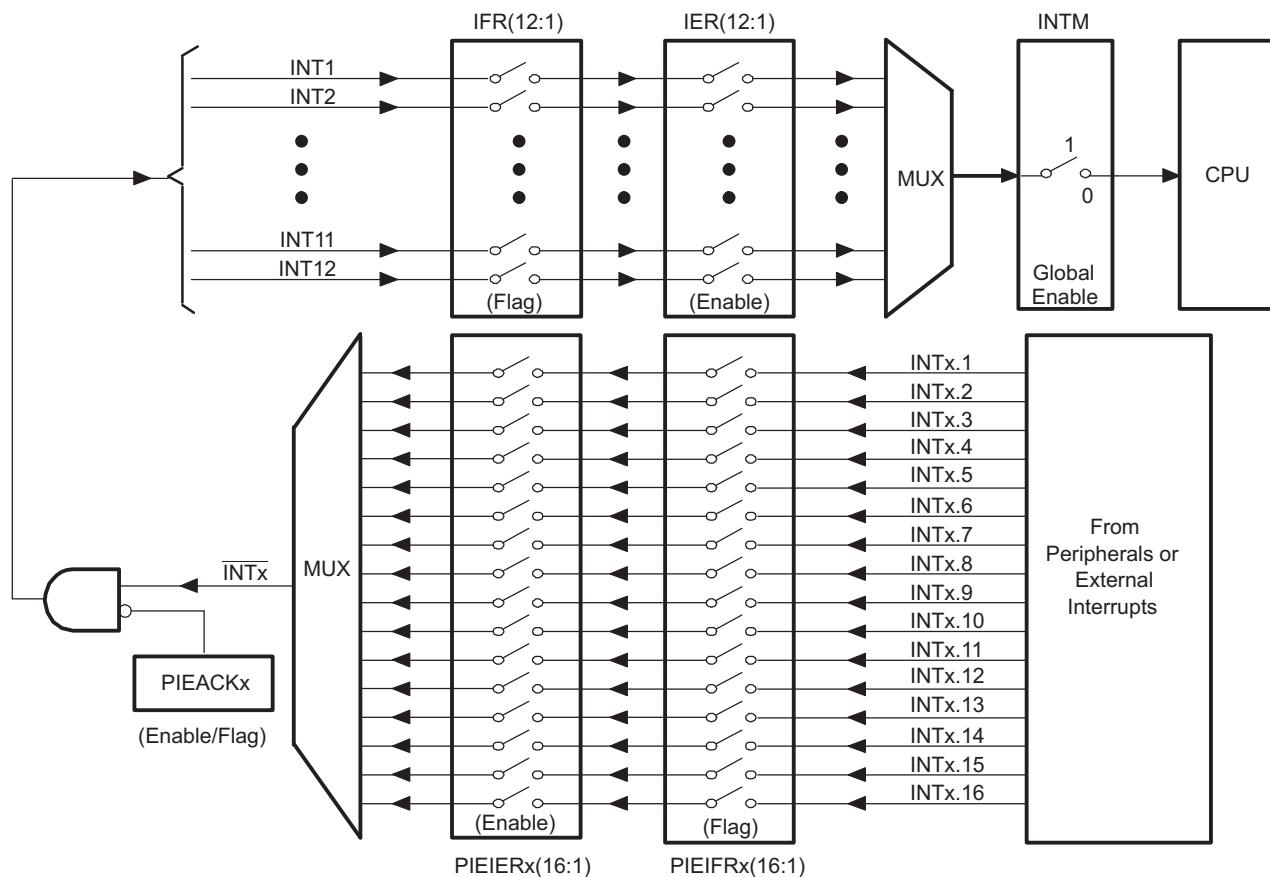
By default on power-up or on reset (any reset which can reset the CPU), the ePIE is disabled and none of the peripheral interrupts are enabled. However, NMI and ITRAP exceptions are enabled by default. When the ePIE is disabled, any NMI and ITRAP exception will use the handlers registered in the ROM vector table, and when the ePIE is enabled, NMI and ITRAP exceptions will use the handler's registers in the ePIE vector table, which is located in ePIE RAM. More details are explained in the following sections.

1.4.1.1 Overview of the ePIE Controller

The 28x CPU supports one nonmaskable interrupt (NMI) and 16 maskable prioritized interrupt requests (INT1-INT14, RTOSINT, and DLOGINT) at the CPU level. The 28x devices have many peripherals and each peripheral is capable of generating one or more interrupts in response to many events at the peripheral level. Because the CPU does not have sufficient capacity to handle all peripheral interrupt requests at the CPU level, a centralized peripheral interrupt expansion (PIE) controller is required to arbitrate the interrupt requests from various sources such as peripherals and other external pins. The PIE vector table is used to store the address (vector) of each interrupt service routine (ISR) within the system. There is one vector per interrupt source including all MUXed and non-MUXed interrupts. The user populates the vector table during device initialization and updates it during operation.

1.4.1.1.1 Interrupt Operation Sequence

Figure 1-1 shows an overview of the interrupt operation sequence for all multiplexed PIE interrupts. Interrupt sources that are not multiplexed are fed directly to the CPU.

Figure 1-1. ePIE Interrupts Multiplexing

1.4.1.1.2 Peripheral Level

If an interrupt-generating event occurs in a peripheral, the interrupt flag (PIEIFRx) bit corresponding to that event is set in a register for that particular peripheral.

If the corresponding interrupt enable (PIEIERx) bit is set, the peripheral generates an interrupt request to the ePIE controller. If the interrupt is not enabled at the peripheral level, then the (PIEIFRx) remains set until cleared by software. If the interrupt is enabled at a later time, and if the interrupt flag is still set, the interrupt request is asserted to the ePIE. Interrupt flags within the peripheral registers must be manually cleared.

1.4.1.1.3 ePIE Level

The ePIE block multiplexes sixteen peripheral and external pin interrupts into one CPU interrupt. These interrupts are divided into twelve groups: ePIE group 1 - ePIE group 12. The interrupts within a group are multiplexed into one CPU interrupt. For example, ePIE group 1 is multiplexed into CPU interrupt 1 (INT1) while ePIE group 12 is multiplexed into CPU interrupt 12 (INT12). Interrupt sources connected to the remaining CPU interrupts are not multiplexed. For the non-multiplexed interrupts, the ePIE passes the request directly to the CPU.

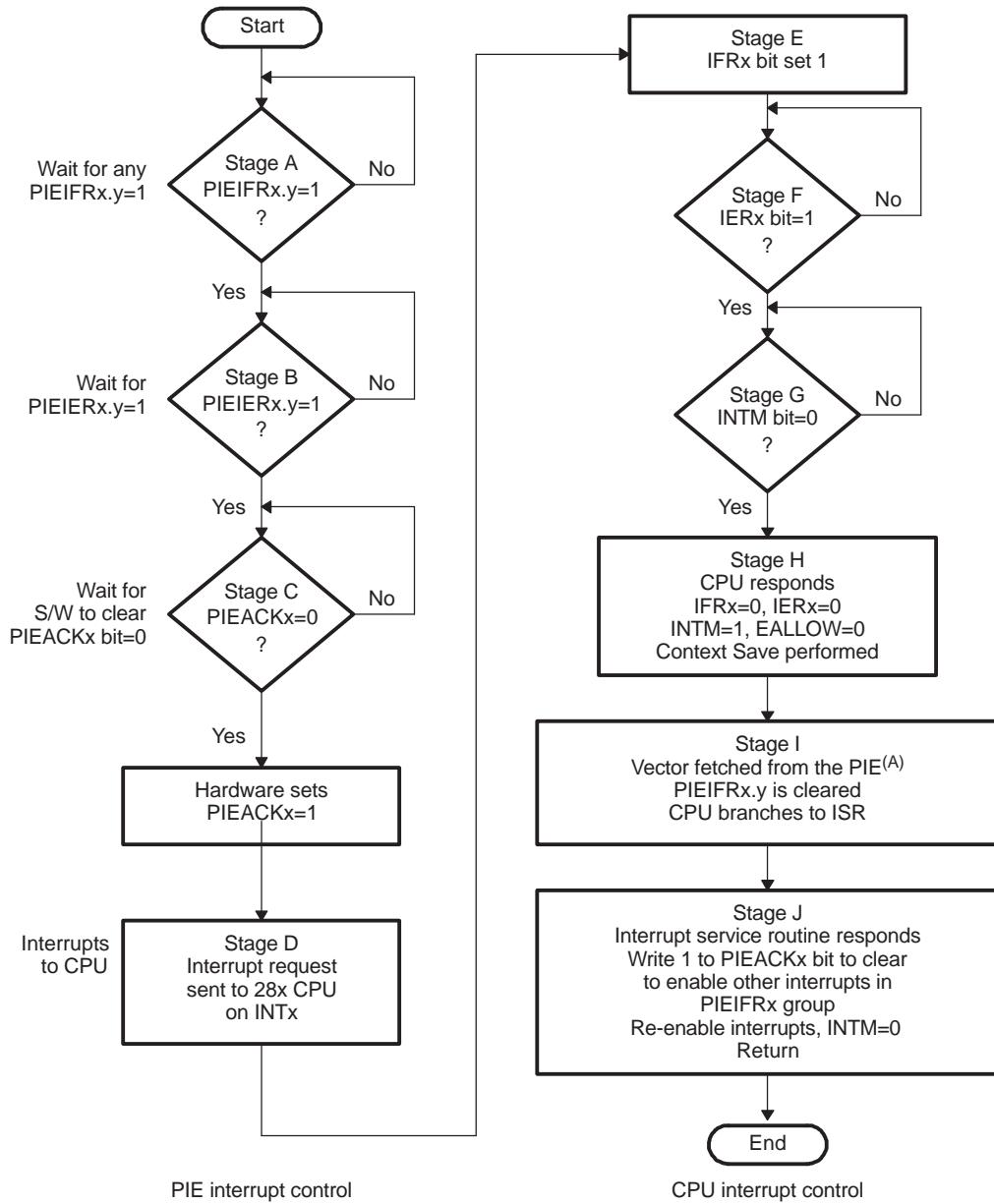
For multiplexed interrupt sources, each interrupt group in the ePIE block has an associated flag register (PIEIFRx) and enable (PIEIERx) register ($x = \text{ePIE group 1} - \text{ePIE group 12}$). Each bit, referred to as y , corresponds to one of the 16 MUXed interrupts within the group. Thus PIEIFRx.y and PIEIERx.y correspond to interrupt y ($y = 1-16$) in ePIE group x ($x = 1-12$). In addition, there is one acknowledge bit (PIEACK) for every ePIE interrupt group referred to as PIEACK_x ($x = 1-12$).

Once the request is made to the ePIE controller, the corresponding ePIE interrupt flag (PIEIFRx.y) bit is set. If the ePIE interrupt enable (PIEIERx.y) bit is also set for the given interrupt then the ePIE checks the corresponding PIEACKx bit to determine if the CPU is ready for an interrupt from that group. If the PIEACKx bit is clear for that group, then the ePIE sends the interrupt request to the CPU. If PIEACKx is set, then the ePIE waits until it is cleared to send the request for INTx.

1.4.1.1.4 CPU Level

Once the request is sent to the CPU, the CPU level interrupt flag (IFR) bit corresponding to INTx is set. After a flag has been latched in the IFR, the corresponding interrupt is not serviced until it is appropriately enabled in the CPU interrupt enable (IER) register or the debug interrupt enable register (DBGIER) and the global interrupt mask (INTM) bit.

Figure 1-2. CPU Level Interrupt Handling



NOTE: For multiplexed interrupts, the ePIE responds with the highest priority interrupt that is both flagged and enabled. If there is no interrupt both flagged and enabled, then the highest priority interrupt within the group (INTx.1 where x is the ePIE group) is used.

As shown in [Table 1-3](#), the requirements for enabling the maskable interrupt at the CPU level depends on the interrupt handling process being used. In the standard process, which happens most of the time, the DBGIER register is not used. When the 28x is in real-time emulation mode and the CPU is halted, a different process is used. In this special case, the DBGIER is used and the INTM bit is ignored. If the DSP is in real-time mode and the CPU is running, the standard interrupt-handling process applies.

Table 1-3. Enabling Interrupt

Interrupt Handling Process	Interrupt Enabled If...
Standard	INTM = 0 and bit in IER is 1
DSP in real-time mode and halted	Bit in IER is 1 and DBGIER is 1

The CPU then prepares to service the interrupt. This preparation process is described in detail in *TMS320x28x DSP CPU and Instruction Set Reference Guide* (literature number [SPRU430](#)). In preparation, the corresponding CPU IFR and IER bits are cleared, EALLOW and LOOP are cleared, INTM and DBGM are set, the pipeline is flushed and the return address is stored, and the automatic context save is performed. The vector of the ISR is then fetched from the ePIE module. If the interrupt request comes from a multiplexed interrupt, the ePIE module uses the PIEIERx and PIEIFRx registers to decode which interrupt needs to be serviced.

The address for the interrupt service routine that is executed is fetched directly from the ePIE interrupt vector table. There is one 32-bit vector for each of the possible 96 interrupts within the ePIE. Interrupt flags within the ePIE module (PIEIFRx.y) are automatically cleared when the interrupt vector is fetched. The ePIE acknowledge bit for a given interrupt group, however, must be cleared manually when ready to receive more interrupts from the ePIE group.

1.4.1.2 Vector Table Mapping

On C28x devices, the interrupt vector table can be mapped to four distinct locations in memory. In practice only the ePIE vector table mapping is used.

This vector mapping is controlled by the following mode bits/signals:

VMAP	VMAP is found in Status Register 1 ST1 (bit 3). A device reset sets this bit to 1. The state of this bit can be modified by writing to ST1 or by SETC/CLRC VMAP instructions. For normal operation leave this bit set.
M0M1MAP	M0M1MAP is found in Status Register 1 ST1 (bit 11). A device reset sets this bit to 1. The state of this bit can be modified by writing to ST1 or by SETC/CLRC M0M1MAP instructions. For normal device operation, this bit should remain set. M0M1MAP = 0 is reserved for TI testing only.
ENPIE	ENPIE is found in PIECTRL Register (bit 0). The default value of this bit, on reset, is set to 0 (ePIE disabled). The state of this bit can be modified after reset by writing to the PIECTRL register (address 0x0000 0CE0).

Using these bits and signals the possible vector table mappings are shown in [Table 1-4](#).

Table 1-4. Interrupt Vector Table Mapping

Vector MAPS	Vectors Fetched From	Address Range	VMAP	M0M1MAP	ENPIE
M1 Vector ⁽¹⁾	M1 SARAM Block	0x000000 - 0x00003F	0	0	X
M0 Vector ⁽¹⁾	M0 SARAM Block	0x000000 - 0x00003F	0	1	X
BROM Vector	Boot ROM Block	0x3FFFC0 - 0x3FFFFF	1	X	0
ePIE Vector	ePIE Block	0x000D00 - 0x000EFF	1	X	1

⁽¹⁾ Vector map M0 and M1 Vector is a reserved mode only. On the 28x devices these are used as SARAM.

The M1 and M0 vector table mapping are reserved for TI testing only. When using other vector mappings, the M0 and M1 memory blocks are treated as SARAM blocks and can be used freely without any restrictions.

After a device reset operation, the vector table is mapped as shown in [Table 1-5](#).

Table 1-5. Vector Table Mapping After Reset Operation

Vector MAPS	Reset Fetched From	Address Range	VMAP ⁽¹⁾	M0M1MAP ⁽¹⁾	ENPIE ⁽¹⁾
BROM Vector ⁽²⁾	Boot ROM Block	0x3FFFC0 - 0x3FFFFF	1	1	0

⁽¹⁾ On the 28x devices, the VMAP and M0M1MAP modes are set to 1 on reset. The ENPIE mode is forced to 0 on reset.

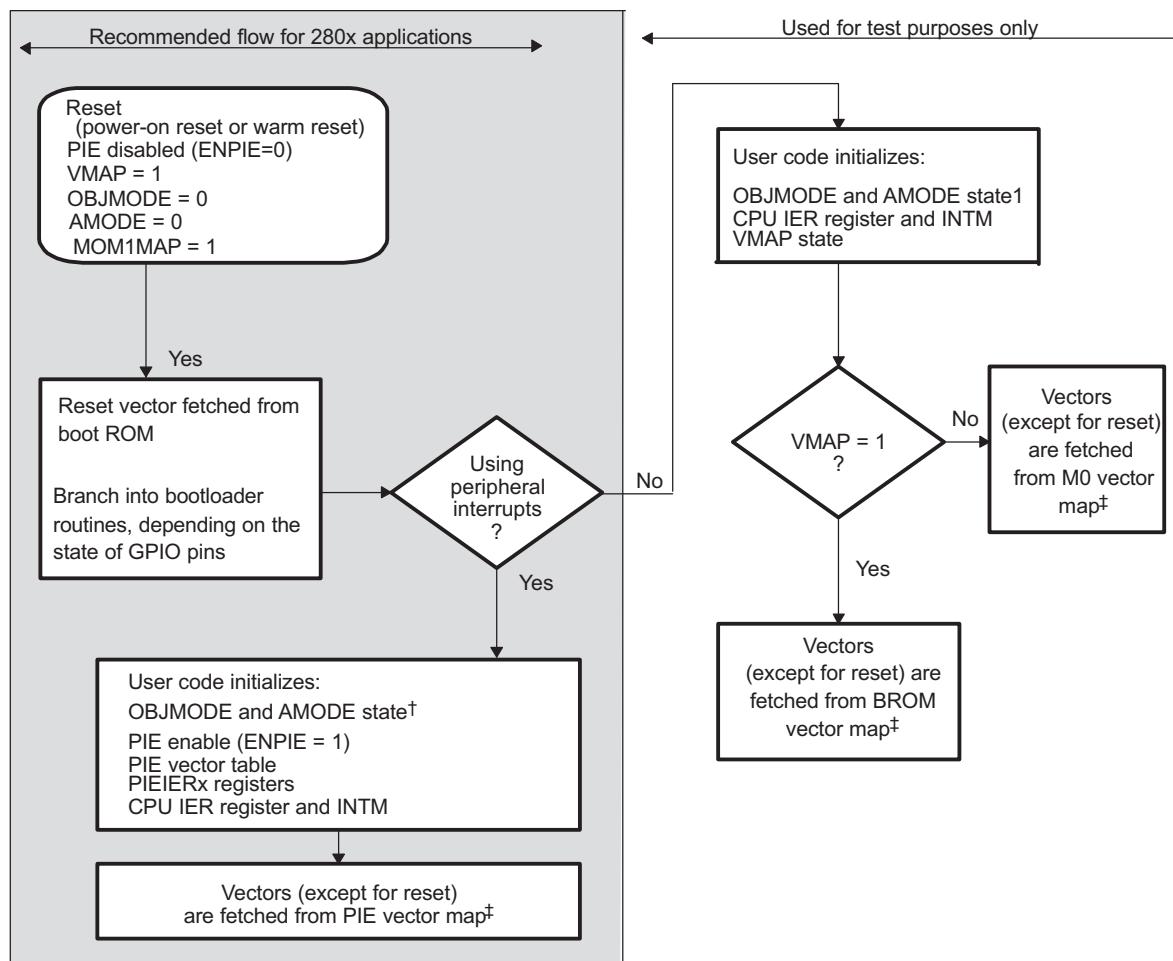
⁽²⁾ The reset vector is always fetched from the boot ROM.

After the reset and boot is complete, the ePIE vector table should be initialized by the user's code. Then the application enables the ePIE vector table. From that point on the interrupt vectors are fetched from the ePIE vector table.

Note: When a reset occurs, the reset vector is always fetched from the vector table as shown in [Table 1-5](#). After a reset the ePIE vector table is always disabled.

[Figure 1-3](#) illustrates the process by which the vector table mapping is selected.

Figure 1-3. Reset Flow Diagram



A The compatibility operating mode of the 28x CPU is determined by a combination of the OBJMODE and AMODE bits in Status Register 1 (ST1):

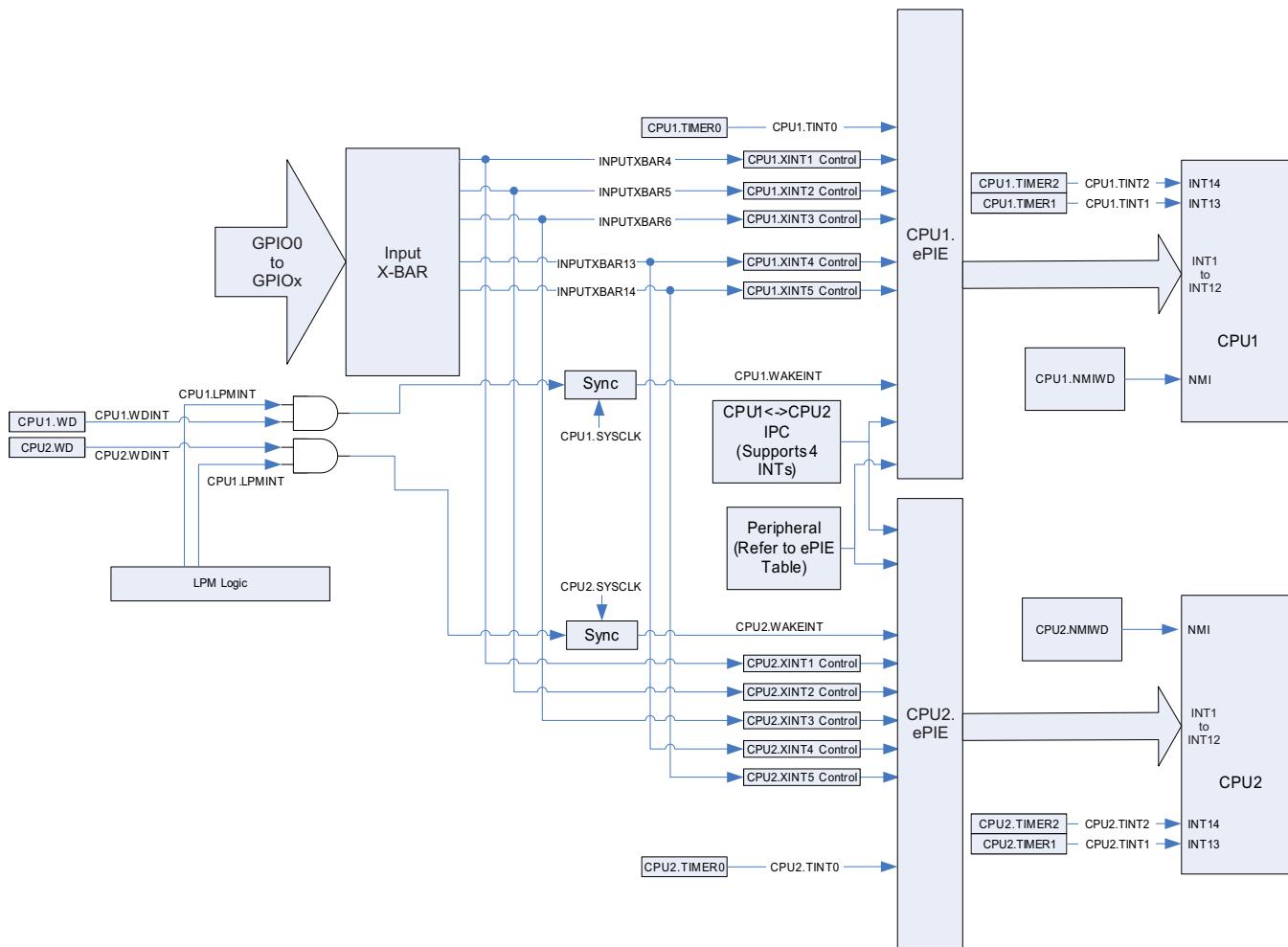
Operating Mode	OBJMODE	AMODE
C28x Mode	1	0
24x/240xA Source-Compatible	1	1
C27x Object-Compatible	0	0 (Default at reset)

B The reset vector is always fetched from the boot ROM.

1.4.1.3 Interrupt Sources

Figure 1-4 shows how the various interrupt sources are multiplexed within the devices. This multiplexing (MUX) scheme may not be exactly the same on all 28x devices. See the device data manual for details.

Figure 1-4. ePIE Interrupt Sources and External Interrupts XINT1/XINT2/XINT3



1.4.1.3.1 Procedure for Handling Multiplexed Interrupts

The ePIE module multiplexes 16 peripheral and external pin interrupts into one CPU interrupt. These interrupts are divided into 12 groups: PIE group 1 - PIE group 12. Each group has an associated enable PIEIER and flag PIEIFR register. These registers are used to control the flow of interrupts to the CPU. The ePIE module also uses the PIEIER and PIEIFR registers to decode to which interrupt service routine the CPU should branch.

There are three steps that should be followed when clearing bits within the PIEIFR and the PIEIER registers:

Rule 1: Never clear a PIEIFR bit by software

An incoming interrupt may be lost while a write or a read-modify-write operation to the PIEIFR register takes place. To clear a PIEIFR bit, the pending interrupt must be serviced. If you want to clear the PIEIFR bit without executing the normal service routine, then use the following procedure:

1. Set the EALLOW bit to allow modification to the ePIE vector table.
2. Modify the ePIE vector table so that the vector for the peripheral's service routine points to a temporary ISR. This temporary ISR will only perform a return from interrupt (IRET) operation.
3. Enable the interrupt so that the interrupt will be serviced by the temporary ISR.
4. After the temporary interrupt routine is serviced, the PIEIFR bit will be clear.
5. Modify the ePIE vector table to re-map the peripheral's service routine to the proper service routine.
6. Clear the EALLOW bit.

Rule 2: Procedure for software-prioritizing interrupts

Use the method found in the device support examples in controlSUITE (literature number SPRCA85).

1. Use the CPU IER register as a global priority and the individual PIEIER registers for group priorities. In this case the PIEIER register is only modified within an interrupt. In addition, only the PIEIER for the same group as the interrupt being serviced is modified. This modification is done while the PIEACK bit holds additional interrupts back from the CPU.
2. Never disable a PIEIER bit for a group when servicing an interrupt from an unrelated group.

Rule 3: Disabling interrupts using PIEIER

If the PIEIER registers are used to enable and then later disable an interrupt then the procedure described in [Section 1.4.1.3.2](#) must be followed.

1.4.1.3.2 Procedures for Enabling And Disabling Multiplexed Peripheral Interrupts

The proper procedure for enabling or disabling an interrupt is by using the peripheral interrupt enable/disable flags. The primary purpose of the PIEIER and CPU IER registers is for software prioritization of interrupts within the same PIE interrupt group. The software package C280x C/C++ Header Files and Peripheral Examples in C (literature number SPRC191) includes an example that illustrates this method of software prioritizing interrupts. Should bits within the PIEIER registers need to be cleared outside of this context, one of the following two procedures should be followed. The first method preserves the associated ePIE flag register so that interrupts are not lost. The second method clears the associated ePIE flag register.

Method 1: Use the PIEIERx register to disable the interrupt and preserve the associated PIEIFRx flags.

To clear bits within a PIEIERx register while preserving the associated flags in the PIEIFRx register, the following procedure should be followed:

1. Disable global interrupts (INTM = 1).
2. Clear the PIEIERx.y bit to disable the interrupt for a given peripheral. This can be done for one or more peripherals within the same group.
3. Wait 5 cycles. This delay is required to be sure that any interrupt that was incoming to the CPU has been flagged within the CPU IFR register.
4. Clear the CPU IFRx bit for the peripheral group. This is a safe operation on the CPU IFR register.
5. Clear the PIEACKx bit for the peripheral group.
6. Enable global interrupts (INTM = 0).

Method 2: Use the PIEIERx register to disable the interrupt and clear the associated PIEIFRx flags.

To perform a software reset of a peripheral interrupt and clear the associated flag in the PIEIFRx register and CPU IFR register, the following procedure should be followed:

1. Disable global interrupts (INTM = 1).
2. Set the EALLOW bit.
3. Modify the PIE vector table to temporarily map the vector of the specific peripheral interrupt to a empty interrupt service routine (ISR). This empty ISR will only perform a return from interrupt (IRET)

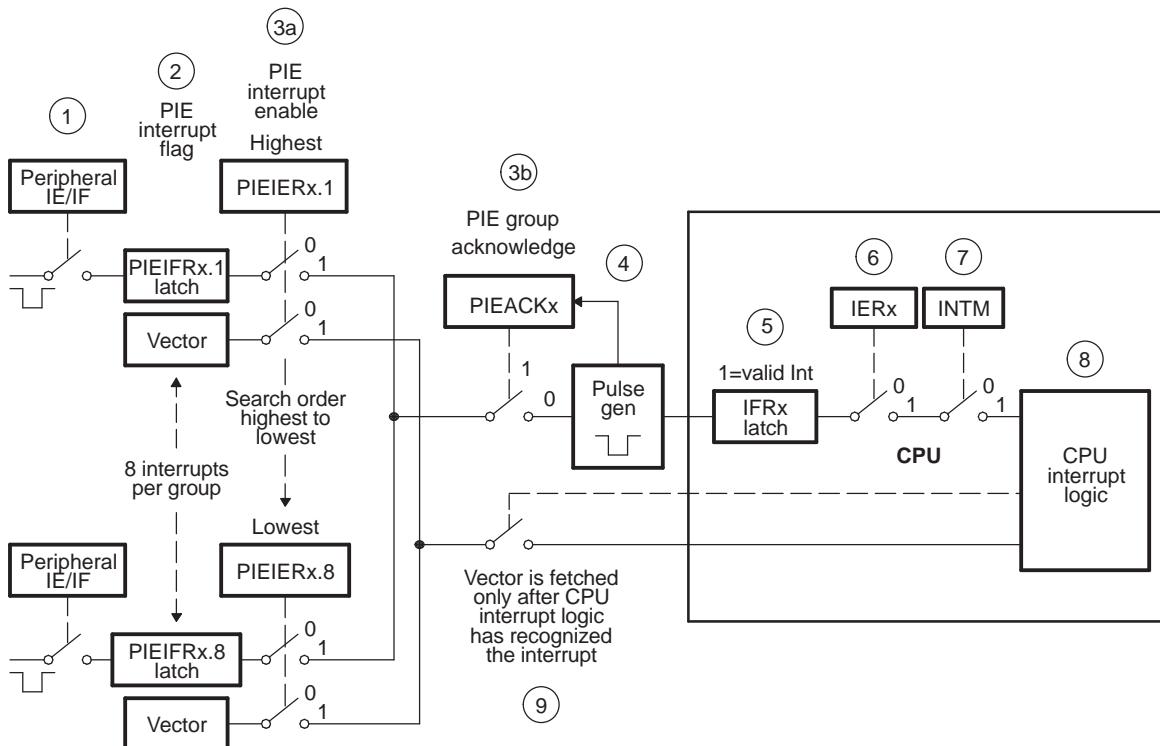
instruction. This is the safe way to clear a single PIEIFRx.y bit without losing any interrupts from other peripherals within the group.

4. Disable the peripheral interrupt at the peripheral register.
5. Enable global interrupts (INTM = 0).
6. Wait for any pending interrupt from the peripheral to be serviced by the empty ISR routine.
7. Disable global interrupts (INTM = 1).
8. Modify the ePIE vector table to map the peripheral vector back to its original ISR.
9. Clear the EALLOW bit.
10. Disable the PIEIER bit for given peripheral.
11. Clear the IFR bit for given peripheral group (this is safe operation on CPU IFR register).
12. Clear the PIEACK bit for the ePIE group.
13. Enable global interrupts.

1.4.1.3.3 Flow of a Multiplexed Interrupt Request From a Peripheral to the CPU

Figure 1-5 shows the flow with the steps shown in circled numbers. Following the diagram, the steps are described.

Figure 1-5. Multiplexed Interrupt Request Flow



1. Any peripheral or external interrupt within the ePIE group generates an interrupt. If interrupts are enabled within the peripheral module then the interrupt request is sent to the ePIE module.
2. The ePIE module recognizes that interrupt y within ePIE group x (INTx.y) has asserted an interrupt and the appropriate ePIE interrupt flag bit is latched: PIEIFRx.y = 1.
3. For the interrupt request to be sent from the ePIE to the CPU, both of the following conditions must be true:
 - (a) The proper enable bit must be set (PIEIERx.y = 1) and
 - (b) The PIEACKx bit for the group must be clear.
4. If both conditions in 3a and 3b are true, then an interrupt request is sent to the CPU and the acknowledge bit is again set (PIEACKx = 1). The PIEACKx bit will remain set until you clear it to 0.

- indicate that additional interrupts from the group can be sent from the ePIE to the CPU.
5. The CPU interrupt flag bit is set (CPU IFR_x = 1) to indicate a pending interrupt x at the CPU level.
 6. If the CPU interrupt is enabled (CPU IER bit x = 1, or DBGIER bit x = 1) AND the global interrupt mask is clear (INTM = 0) then the CPU will service the INT_x.
 7. The CPU recognizes the interrupt and performs the automatic context save, clears the IER bit, sets INTM, and clears EALLOW. All of the steps that the CPU takes in order to prepare to service the interrupt are documented in the *TMS320C28x DSP CPU and Instruction Set Reference Guide* (literature number [SPRU430](#)).
 8. The CPU will then request the appropriate vector from the ePIE.
 9. For multiplexed interrupts, the ePIE module uses the current value in the PIEIER_x and PIEIFR_x registers to decode which vector address should be used. There are two possible cases:
 - (a) The vector for the highest priority interrupt within the group that is both enabled in the PIEIER_x register and flagged as pending in the PIEIFR_x is fetched and used as the branch address. In this manner if an even higher priority enabled interrupt was flagged after Step 7, it will be serviced first.
 - (b) If no flagged interrupts within the group are enabled, then the ePIE will respond with the vector for the highest priority interrupt within that group. That is the branch address used for INT_{x.1}. This behavior corresponds to the 28x TRAP or INT instructions.

NOTE: Because the PIEIER_x register is used to determine which vector will be used for the branch, you must take care when clearing bits within the PIEIER_x register. The proper procedure for clearing bits within a PIEIER_x register is described and failure to follow these steps can result in changes occurring to the PIEIER_x register after an interrupt has been passed to the CPU. In this case, the ePIE will respond as if a TRAP or INT instruction was executed unless there are other interrupts both pending and enabled.

At this point, the PIEIFR_{x.y} bit is cleared and the CPU branches to the vector of the interrupt fetched from the ePIE.

1.4.1.3.4 The ePIE Vector Table on CPU1 and CPU2

[Table 1-7](#) and [Table 1-8](#) consist of a 512 x 16 SARAM block. The ePIE vector table contents are undefined on reset. The CPU fixes interrupt priority for INT1 to INT12. The ePIE controls priority for each group of 16 interrupts. For example, if INT1.1 should occur simultaneously with INT8.1, both interrupts are presented to the CPU simultaneously by the ePIE block, and the CPU services INT1.1 first. If INT1.1 should occur simultaneously with INT1.8, then INT1.1 is sent to the CPU first and then INT1.8 follows. Interrupt prioritization is performed during the vector fetch portion of the interrupt processing.

When the ePIE is enabled, a TRAP #1 through TRAP #12 or an INTR INT1 to INTR INT12 instruction transfers program control to the interrupt service routine corresponding to the first vector within the ePIE group. For example: TRAP #1 fetches the vector from INT1.1, TRAP #2 fetches the vector from INT2.1 and so forth. Similarly an OR IFR, #16-bit operation causes the vector to be fetched from INTR1.1 to INTR12.1 locations, if the respective interrupt flag is set. All other TRAP, INTR, OR IFR,#16-bit operations fetch the vector from the respective table location. The vector table is EALLOW protected.

Out of the 192 possible MUXed interrupts in [Table 1-6](#), 66 interrupts are currently used. The remaining interrupts are reserved for future devices. These reserved interrupts can be used as software interrupts if they are enabled at the PIEIFR_x level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming from peripherals may be lost by accidentally clearing their flags when modifying the PIEIFR.

To summarize, there are two safe cases when the reserved interrupts can be used as software interrupts:

- - No peripheral within the group is asserting interrupts.
 - No peripheral interrupts are assigned to the group. For example, ePIE group 11 and 12 do not have any peripherals attached to them.

The interrupt grouping for peripherals and external interrupts connected to the PIE module is shown in [Table 1-6](#). Each row in the table shows the eight interrupts multiplexed into a particular CPU interrupt.

Table 1-6. PIE Vector Table Mapping

	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16	
INT1.y	ADCA1	ADCB1	ADCC1	XINT1	XINT2	ADCD1	TIMER0	WAKE	-	-	-	-	IPC0	IPC1	IPC2	IPC3	
INT2.y	EPWM1_TZ	EPWM2_TZ	EPWM3_TZ	EPWM4_TZ	EPWM5_TZ	EPWM6_TZ	EPWM7_TZ	EPWM8_TZ	EPWM9_TZ	EPWM10_T_Z	EPWM11_T_Z	EPWM12_T_Z	-	-	-	-	
INT3.y	EPWM1	EPWM2	EPWM3	EPWM4	EPWM5	EPWM6	EPWM7	EPWM8	EPWM9	EPWM10	EPWM11	EPWM12	-	-	-	-	
INT4.y	ECAP1	ECAP2	ECAP3	ECAP4	ECAP5	ECAP6	-	-	-	-	-	-	-	-	-	-	
INT5.y	EQEP1	EQEP2	EQEP3	-	CLB1	CLB2	CLB3	CLB4	SD1	SD2	-	-	-	-	-	-	
INT6.y	SPIA_RX	SPIA_TX	SPIB_RX	SPIB_TX	MCBSPA_RX	MCBSPA_TX	MCBSPB_RX	MCBSPB_TX	SPIC_RX	SPIC_TX	-	-	-	-	-	-	
INT7.y	DMA_CH1	DMA_CH2	DMA_CH3	DMA_CH4	DMA_CH5	DMA_CH6	-	-	-	-	-	-	-	-	-	-	
INT8.y	I2CA	I2CA_FIFO	I2CB	I2CB_FIFO	SCIC_RX	SCIC_TX	SCID_RX	SCID_TX	-	-	-	-	-	-	UPPA (CPU1 only)		
INT9.y	SCIA_RX	SCIA_TX	SCIB_RX	SCIB_TX	DCANA_1	DCANA_2	DCANB_1	DCANB_2	-	-	-	-	-	-	USBA (CPU1 only)		
INT10.y	ADCA_EVT	ADCA2	ADCA3	ADCA4	ADCB_EVT	ADCB2	ADCB3	ADCB4	ADCC_EVT	ADCC2	ADCC3	ADCC4	ADCD_EVT	ADCD2	ADCD3	ADCD4	
INT11.y	CLA1_1	CLA1_2	CLA1_3	CLA1_4	CLA1_5	CLA1_6	CLA1_7	CLA1_8	-	-	-	-	-	-	-	-	
INT12.y	XINT3	XINT4	XINT5	PBIST	FMC	VCU	"FPU_						RAM_ACCE_SS_VIOLATION	SYS_PLL_S_LIP	AUX_PLL_S_LIP	CLA_UNDERFLOW	CLA_UNDERFLOW

Note: Cells marked "-" are Reserved

Table 1-7. CPU Interrupt Vectors

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
Reset	0	0x0000 0D00	2	Reset is always fetched from location 0x003F_FFC0 in Boot ROM	1 (Highest)	-
INT1	1	0x0000 0D02	2	Not used. See PIE Group 1	5	-
INT2	2	0x0000 0D04	2	Not used. See PIE Group 2	6	-
INT3	3	0x0000 0D06	2	Not used. See PIE Group 3	7	-
INT4	4	0x0000 0D08	2	Not used. See PIE Group 4	8	-
INT5	5	0x0000 0D0A	2	Not used. See PIE Group 5	9	-
INT6	6	0x0000 0D0C	2	Not used. See PIE Group 6	10	-
INT7	7	0x0000 0D0E	2	Not used. See PIE Group 7	11	-
INT8	8	0x0000 0D10	2	Not used. See PIE Group 8	12	-
INT9	9	0x0000 0D12	2	Not used. See PIE Group 9	13	-
INT10	10	0x0000 0D14	2	Not used. See PIE Group 10	14	-
INT11	11	0x0000 0D16	2	Not used. See PIE Group 11	15	-
INT12	12	0x0000 0D18	2	Not used. See PIE Group 12	16	-
INT13	13	0x0000 0D1A	2	CPU TIMER1 Interrupt	17	-
INT14	14	0x0000 0D1C	2	CPU TIMER2 Interrupt (for TI/RTOS use)	18	-
DATALOG	15	0x0000 0D1E	2	CPU Data Logging Interrupt	19 (lowest)	-
RTOSINT	16	0x0000 0D20	2	CPU Real-Time OS Interrupt	4	-
EMUINT	17	0x0000 0D22	2	CPU Emulation Interrupt	2	-
NMI	18	0x0000 0D24	2	Non-Maskable Interrupt	3	-
ILLEGAL	19	0x0000 0D26	2	Illegal Operation	-	-
USER 1	20	0x0000 0D28	2	User-Defined Trap	-	-
USER 2	21	0x0000 0D2A	2	User-Defined Trap	-	-
USER 3	22	0x0000 0D2C	2	User-Defined Trap	-	-
USER 4	23	0x0000 0D2E	2	User-Defined Trap	-	-
USER 5	24	0x0000 0D30	2	User-Defined Trap	-	-
USER 6	25	0x0000 0D32	2	User-Defined Trap	-	-
USER 7	26	0x0000 0D34	2	User-Defined Trap	-	-
USER 8	27	0x0000 0D36	2	User-Defined Trap	-	-
USER 9	28	0x0000 0D38	2	User-Defined Trap	-	-
USER 10	29	0x0000 0D3A	2	User-Defined Trap	-	-
USER 11	30	0x0000 0D3C	2	User-Defined Trap	-	-
USER 12	31	0x0000 0D3E	2	User-Defined Trap	-	-

Table 1-8. ePIE Interrupt Vectors

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
PIE Group 1 Vectors - MUXed into CPU INT1						
INT1.1	32	0x0000 0D40	2	ADCA1 interrupt	5	1 (Highest)
INT1.2	33	0x0000 0D42	2	ADCB1 interrupt	5	2
INT1.3	34	0x0000 0D44	2	ADCC1 interrupt	5	3
INT1.4	35	0x0000 0D46	2	XINT1 interrupt	5	4
INT1.5	36	0x0000 0D48	2	XINT2 interrupt	5	5
INT1.6	37	0x0000 0D4A	2	ADCD1 interrupt	5	6
INT1.7	38	0x0000 0D4C	2	TIMER0 interrupt	5	7
INT1.8	39	0x0000 0D4E	2	WAKE interrupt	5	8
INT1.9	128	0x0000 0E00	2	Reserved	5	9
INT1.10	129	0x0000 0E02	2	Reserved	5	10
INT1.11	130	0x0000 0E04	2	Reserved	5	11
INT1.12	131	0x0000 0E06	2	Reserved	5	12
INT1.13	132	0x0000 0E08	2	IPC0 interrupt	5	13
INT1.14	133	0x0000 0E0A	2	IPC1 interrupt	5	14
INT1.15	134	0x0000 0E0C	2	IPC2 interrupt	5	15
INT1.16	135	0x0000 0E0E	2	IPC3 interrupt	5	16 (Lowest)
PIE Group 2 Vectors - MUXed into CPU INT2						
INT2.1	40	0x0000 0D50	2	EPWM1_TZ interrupt	6	1 (Highest)
INT2.2	41	0x0000 0D52	2	EPWM2_TZ interrupt	6	2
INT2.3	42	0x0000 0D54	2	EPWM3_TZ interrupt	6	3
INT2.4	43	0x0000 0D56	2	EPWM4_TZ interrupt	6	4
INT2.5	44	0x0000 0D58	2	EPWM5_TZ interrupt	6	5
INT2.6	45	0x0000 0D5A	2	EPWM6_TZ interrupt	6	6
INT2.7	46	0x0000 0D5C	2	EPWM7_TZ interrupt	6	7
INT2.8	47	0x0000 0D5E	2	EPWM8_TZ interrupt	6	8
INT2.9	136	0x0000 0E10	2	EPWM9_TZ interrupt	6	9
INT2.10	137	0x0000 0E12	2	EPWM10_TZ interrupt	6	10
INT2.11	138	0x0000 0E14	2	EPWM11_TZ interrupt	6	11
INT2.12	139	0x0000 0E16	2	EPWM12_TZ interrupt	6	12
INT2.13	140	0x0000 0E18	2	Reserved	6	13
INT2.14	141	0x0000 0E1A	2	Reserved	6	14
INT2.15	142	0x0000 0E1C	2	Reserved	6	15
INT2.16	143	0x0000 0E1E	2	Reserved	6	16 (Lowest)
PIE Group 3 Vectors - MUXed into CPU INT3						
INT3.1	48	0x0000 0D60	2	EPWM1 interrupt	7	1 (Highest)
INT3.2	49	0x0000 0D62	2	EPWM2 interrupt	7	2
INT3.3	50	0x0000 0D64	2	EPWM3 interrupt	7	3
INT3.4	51	0x0000 0D66	2	EPWM4 interrupt	7	4

Table 1-8. ePIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT3.5	52	0x0000 0D68	2	EPWM5 interrupt	7	5
INT3.6	53	0x0000 0D6A	2	EPWM6 interrupt	7	6
INT3.7	54	0x0000 0D6C	2	EPWM7 interrupt	7	7
INT3.8	55	0x0000 0D6E	2	EPWM8 interrupt	7	8
INT3.9	144	0x0000 0E20	2	EPWM9 interrupt	7	9
INT3.10	145	0x0000 0E22	2	EPWM10 interrupt	7	10
INT3.11	146	0x0000 0E24	2	EPWM11 interrupt	7	11
INT3.12	147	0x0000 0E26	2	EPWM12 interrupt	7	12
INT3.13	148	0x0000 0E28	2	Reserved	7	13
INT3.14	149	0x0000 0E2A	2	Reserved	7	14
INT3.15	150	0x0000 0E2C	2	Reserved	7	15
INT3.16	151	0x0000 0E2E	2	Reserved	7	16 (Lowest)
PIE Group 4 Vectors - MUXed into CPU INT4						
INT4.1	56	0x0000 0D70	2	ECAP1 interrupt	8	1 (Highest)
INT4.2	57	0x0000 0D72	2	ECAP2 interrupt	8	2
INT4.3	58	0x0000 0D74	2	ECAP3 interrupt	8	3
INT4.4	59	0x0000 0D76	2	ECAP4 interrupt	8	4
INT4.5	60	0x0000 0D78	2	ECAP5 interrupt	8	5
INT4.6	61	0x0000 0D7A	2	ECAP6 interrupt	8	6
INT4.7	62	0x0000 0D7C	2	Reserved	8	7
INT4.8	63	0x0000 0D7E	2	Reserved	8	8
INT4.9	152	0x0000 0E30	2	Reserved	8	9
INT4.10	153	0x0000 0E32	2	Reserved	8	10
INT4.11	154	0x0000 0E34	2	Reserved	8	11
INT4.12	155	0x0000 0E36	2	Reserved	8	12
INT4.13	156	0x0000 0E38	2	Reserved	8	13
INT4.14	157	0x0000 0E3A	2	Reserved	8	14
INT4.15	158	0x0000 0E3C	2	Reserved	8	15
INT4.16	159	0x0000 0E3E	2	Reserved	8	16 (Lowest)
PIE Group 5 Vectors - MUXed into CPU INT5						
INT5.1	64	0x0000 0D80	2	EQEP1 interrupt	9	1 (Highest)
INT5.2	65	0x0000 0D82	2	EQEP2 interrupt	9	2
INT5.3	66	0x0000 0D84	2	EQEP3 interrupt	9	3
INT5.4	67	0x0000 0D86	2	Reserved	9	4
INT5.5	68	0x0000 0D88	2	CLB1 interrupt	9	5
INT5.6	69	0x0000 0D8A	2	CLB2 interrupt	9	6
INT5.7	70	0x0000 0D8C	2	CLB3 interrupt	9	7
INT5.8	71	0x0000 0D8E	2	CLB4 interrupt	9	8
INT5.9	160	0x0000 0E40	2	SD1 interrupt	9	9
INT5.10	161	0x0000 0E42	2	SD2 interrupt	9	10
INT5.11	162	0x0000 0E44	2	Reserved	9	11
INT5.12	163	0x0000 0E46	2	Reserved	9	12
INT5.13	164	0x0000 0E48	2	Reserved	9	13
INT5.14	165	0x0000 0E4A	2	Reserved	9	14
INT5.15	166	0x0000 0E4C	2	Reserved	9	15

Table 1-8. ePIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT5.16	167	0x0000 0E4E	2	Reserved	9	16 (Lowest)
PIE Group 6 Vectors - MUXed into CPU INT6						
INT6.1	72	0x0000 0D90	2	SPIA_RX interrupt	10	1 (Highest)
INT6.2	73	0x0000 0D92	2	SPIA_TX interrupt	10	2
INT6.3	74	0x0000 0D94	2	SPIB_RX interrupt	10	3
INT6.4	75	0x0000 0D96	2	SPIB_TX interrupt	10	4
INT6.5	76	0x0000 0D98	2	MCBSPA_RX interrupt	10	5
INT6.6	77	0x0000 0D9A	2	MCBSPA_TX interrupt	10	6
INT6.7	78	0x0000 0D9C	2	MCBSPB_RX interrupt	10	7
INT6.8	79	0x0000 0D9E	2	MCBSPB_TX interrupt	10	8
INT6.9	168	0x0000 0E50	2	SPIC_RX interrupt	10	9
INT6.10	169	0x0000 0E52	2	SPIC_TX interrupt	10	10
INT6.11	170	0x0000 0E54	2	Reserved	10	11
INT6.12	171	0x0000 0E56	2	Reserved	10	12
INT6.13	172	0x0000 0E58	2	Reserved	10	13
INT6.14	173	0x0000 0E5A	2	Reserved	10	14
INT6.15	174	0x0000 0E5C	2	Reserved	10	15
INT6.16	175	0x0000 0E5E	2	Reserved	10	16 (Lowest)
PIE Group 7 Vectors - MUXed into CPU INT7						
INT7.1	80	0x0000 0DA0	2	DMA_CH1 interrupt	11	1 (Highest)
INT7.2	81	0x0000 0DA2	2	DMA_CH2 interrupt	11	2
INT7.3	82	0x0000 0DA4	2	DMA_CH3 interrupt	11	3
INT7.4	83	0x0000 0DA6	2	DMA_CH4 interrupt	11	4
INT7.5	84	0x0000 0DA8	2	DMA_CH5 interrupt	11	5
INT7.6	85	0x0000 0DAA	2	DMA_CH6 interrupt	11	6
INT7.7	86	0x0000 0DAC	2	Reserved	11	7
INT7.8	87	0x0000 0DAE	2	Reserved	11	8
INT7.9	176	0x0000 0E60	2	Reserved	11	9
INT7.10	177	0x0000 0E62	2	Reserved	11	10
INT7.11	178	0x0000 0E64	2	Reserved	11	11
INT7.12	179	0x0000 0E66	2	Reserved	11	12
INT7.13	180	0x0000 0E68	2	Reserved	11	13
INT7.14	181	0x0000 0E6A	2	Reserved	11	14
INT7.15	182	0x0000 0E6C	2	Reserved	11	15
INT7.16	183	0x0000 0E6E	2	Reserved	11	16 (Lowest)
PIE Group 8 Vectors - MUXed into CPU INT8						

Table 1-8. ePIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT8.1	88	0x0000 0DB0	2	I2CA interrupt	12	1 (Highest)
INT8.2	89	0x0000 0DB2	2	I2CA_FIFO interrupt	12	2
INT8.3	90	0x0000 0DB4	2	I2CB interrupt	12	3
INT8.4	91	0x0000 0DB6	2	I2CB_FIFO interrupt	12	4
INT8.5	92	0x0000 0DB8	2	SCIC_RX interrupt	12	5
INT8.6	93	0x0000 0DBA	2	SCIC_TX interrupt	12	6
INT8.7	94	0x0000 0DBC	2	SCID_RX interrupt	12	7
INT8.8	95	0x0000 0DBE	2	SCID_TX interrupt	12	8
INT8.9	184	0x0000 0E70	2	Reserved	12	9
INT8.10	185	0x0000 0E72	2	Reserved	12	10
INT8.11	186	0x0000 0E74	2	Reserved	12	11
INT8.12	187	0x0000 0E76	2	Reserved	12	12
INT8.13	188	0x0000 0E78	2	Reserved	12	13
INT8.14	189	0x0000 0E7A	2	Reserved	12	14
INT8.15	190	0x0000 0E7C	2	UPPA interrupt (CPU1 only)	12	15
INT8.16	191	0x0000 0E7E	2	Reserved	12	16 (Lowest)
PIE Group 9 Vectors - MUXed into CPU INT9						
INT9.1	96	0x0000 0DC0	2	SCIA_RX interrupt	13	1 (Highest)
INT9.2	97	0x0000 0DC2	2	SCIA_TX interrupt	13	2
INT9.3	98	0x0000 0DC4	2	SCIB_RX interrupt	13	3
INT9.4	99	0x0000 0DC6	2	SCIB_TX interrupt	13	4
INT9.5	100	0x0000 0DC8	2	DCANA_1 interrupt	13	5
INT9.6	101	0x0000 0DCA	2	DCANA_2 interrupt	13	6
INT9.7	102	0x0000 0DCC	2	DCANB_1 interrupt	13	7
INT9.8	103	0x0000 0DCE	2	DCANB_2 interrupt	13	8
INT9.9	192	0x0000 0E80	2	Reserved	13	9
INT9.10	193	0x0000 0E82	2	Reserved	13	10
INT9.11	194	0x0000 0E84	2	Reserved	13	11
INT9.12	195	0x0000 0E86	2	Reserved	13	12
INT9.13	196	0x0000 0E88	2	Reserved	13	13
INT9.14	197	0x0000 0E8A	2	Reserved	13	14
INT9.15	198	0x0000 0E8C	2	USBA interrupt (CPU1 only)	13	15
INT9.16	199	0x0000 0E8E	2	Reserved	13	16 (Lowest)
PIE Group 10 Vectors - MUXed into CPU INT10						
INT10.1	104	0x0000 0DD0	2	ADCA_EVT interrupt	14	1 (Highest)

Table 1-8. ePIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT10.2	105	0x0000 0DD2	2	ADCA2 interrupt	14	2
INT10.3	106	0x0000 0DD4	2	ADCA3 interrupt	14	3
INT10.4	107	0x0000 0DD6	2	ADCA4 interrupt	14	4
INT10.5	108	0x0000 0DD8	2	ADCB_EVT interrupt	14	5
INT10.6	109	0x0000 0DDA	2	ADCB2 interrupt	14	6
INT10.7	110	0x0000 0DDC	2	ADCB3 interrupt	14	7
INT10.8	111	0x0000 0DDE	2	ADCB4 interrupt	14	8
INT10.9	200	0x0000 0E90	2	ADCC_EVT interrupt	14	9
INT10.10	201	0x0000 0E92	2	ADCC2 interrupt	14	10
INT10.11	202	0x0000 0E94	2	ADCC3 interrupt	14	11
INT10.12	203	0x0000 0E96	2	ADCC4 interrupt	14	12
INT10.13	204	0x0000 0E98	2	ADCD_EVT interrupt	14	13
INT10.14	205	0x0000 0E9A	2	ADCD2 interrupt	14	14
INT10.15	206	0x0000 0E9C	2	ADCD3 interrupt	14	15
INT10.16	207	0x0000 0E9E	2	ADCD4 interrupt	14	16 (Lowest)
PIE Group 11 Vectors - MUXed into CPU INT11						
INT11.1	112	0x0000 0DE0	2	CLA1_1 interrupt	15	1 (Highest)
INT11.2	113	0x0000 0DE2	2	CLA1_2 interrupt	15	2
INT11.3	114	0x0000 0DE4	2	CLA1_3 interrupt	15	3
INT11.4	115	0x0000 0DE6	2	CLA1_4 interrupt	15	4
INT11.5	116	0x0000 0DE8	2	CLA1_5 interrupt	15	5
INT11.6	117	0x0000 0DEA	2	CLA1_6 interrupt	15	6
INT11.7	118	0x0000 0DEC	2	CLA1_7 interrupt	15	7
INT11.8	119	0x0000 0DEE	2	CLA1_8 interrupt	15	8
INT11.9	208	0x0000 0EA0	2	Reserved	15	9
INT11.10	209	0x0000 0EA2	2	Reserved	15	10
INT11.11	210	0x0000 0EA4	2	Reserved	15	11
INT11.12	211	0x0000 0EA6	2	Reserved	15	12
INT11.13	212	0x0000 0EA8	2	Reserved	15	13
INT11.14	213	0x0000 0EAA	2	Reserved	15	14
INT11.15	214	0x0000 0EAC	2	Reserved	15	15
INT11.16	215	0x0000 0EAE	2	Reserved	15	16 (Lowest)
PIE Group 12 Vectors - MUXed into CPU INT12						
INT12.1	120	0x0000 0DF0	2	XINT3 interrupt	16	1 (Highest)
INT12.2	121	0x0000 0DF2	2	XINT4 interrupt	16	2
INT12.3	122	0x0000 0DF4	2	XINT5 interrupt	16	3
INT12.4	123	0x0000 0DF6	2	PBIST interrupt	16	4
INT12.5	124	0x0000 0DF8	2	FMC interrupt	16	5
INT12.6	125	0x0000 0DFA	2	VCU interrupt	16	6
INT12.7	126	0x0000 0DFC	2	FPU_OVERFLOW interrupt	16	7
INT12.8	127	0x0000 0DFE	2	FPU_UNDERFLOW interrupt	16	8
INT12.9	216	0x0000 0EB0	2	EMIF_ERROR interrupt	16	9

Table 1-8. ePIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT12.10	217	0x0000 0EB2	2	RAM_CORRECTABLE_ERROR interrupt	16	10
INT12.11	218	0x0000 0EB4	2	FLASH_CORRECTABLE_ERROR interrupt	16	11
INT12.12	219	0x0000 0EB6	2	RAM_ACCESS_VIOLATION interrupt	16	12
INT12.13	220	0x0000 0EB8	2	SYS_PLL_SLIP interrupt	16	13
INT12.14	221	0x0000 0EBA	2	AUX_PLL_SLIP interrupt	16	14
INT12.15	222	0x0000 0EBC	2	CLA_OVERFLOW interrupt	16	15
INT12.16	223	0x0000 0EBE	2	CLA_UNDERFLOW interrupt	16	16 (Lowest)

1.4.1.4 ePIE Registers

The ePIE registers are as follows:

- ePIE Configuration Register (PIECTRL)
- ePIE Interrupt Acknowledgment Register (PIEACK)
- ePIE Interrupt Flag Registers (PIEIFR). There are 12 PIEIFR registers, one for each CPU interrupt in the PIE module (INT1-INT12).
- ePIE Interrupt Enable Registers (PIEIER). There are 12 PIEIER () one for each CPU interrupt in the PIE module (INT1-INT12).

Please refer to the respective ePIE registers for details.

1.4.1.4.1 CPU Interrupt Flag Register (IFR)

The CPU interrupt flag register (IFR), is a 16-bit, CPU register and is used to identify and clear pending interrupts. The IFR contains flag bits for all the maskable interrupts at the CPU level (INT1-INT14, DLOGINT and RTOSINT). When the ePIE is enabled, the ePIE module multiplexes interrupt sources for INT1-INT12.

When a maskable interrupt is requested, the flag bit in the corresponding peripheral control register is set to 1. If the corresponding mask bit is also 1, the interrupt request is sent to the CPU, setting the corresponding flag in the IFR. This indicates that the interrupt is pending or waiting for acknowledgment.

To identify pending interrupts, use the PUSH IFR instruction and then test the value on the stack. Use the OR IFR instruction to set IFR bits and use the AND IFR instruction to manually clear pending interrupts. All pending interrupts are cleared with the AND IFR #0 instruction or by a hardware reset.

The following events also clear an IFR flag:

- The CPU acknowledges the interrupt.
- The 28x device is reset.

NOTE:

1. To clear a CPU IFR bit, you must write a zero to it, not a one.
 2. When a maskable interrupt is acknowledged, only the IFR bit is cleared automatically. The flag bit in the corresponding peripheral control register is not cleared. If an application requires that the control register flag be cleared, the bit must be cleared by software.
 3. When an interrupt is requested by an INTR instruction and the corresponding IFR bit is set, the CPU does not clear the bit automatically. If an application requires that the IFR bit be cleared, the bit must be cleared by software.
 4. IMR and IFR registers pertain to core-level interrupts. All peripherals have their own interrupt mask and flag bits in their respective control/configuration registers. Note that several peripheral interrupts are grouped under one core-level interrupt.
-

1.4.1.4.2 Interrupt Enable Register (IER) and Debug Interrupt Enable Register (DBGIER)

The IER 16-bit CPU register contains enable bits for all the maskable CPU interrupt levels (INT1-INT14, RTOSINT and DLOGINT). Neither NMI nor \overline{XRS} is included in the IER; thus, IER has no effect on these interrupts.

You can read the IER to identify enabled or disabled interrupt levels, and you can write to the IER to enable or disable interrupt levels. To enable an interrupt level, set its corresponding IER bit to one using the OR IER instruction. To disable an interrupt level, set its corresponding IER bit to zero using the AND IER instruction. When an interrupt is disabled, it is not acknowledged, regardless of the value of the INTM bit. When an interrupt is enabled, it is acknowledged if the corresponding IFR bit is one and the INTM bit is zero.

When using the OR IER and AND IER instructions to modify IER bits make sure they do not modify the state of bit 15 (RTOSINT) unless a real-time operating system is present.

When a hardware interrupt is serviced or an INTR instruction is executed, the corresponding IER bit is cleared automatically. When an interrupt is requested by the TRAP instruction the IER bit is not cleared automatically. In the case of the TRAP instruction if the bit needs to be cleared it must be done by the interrupt service routine.

At reset, all the IER bits are cleared to 0, disabling all maskable CPU level interrupts.

The Debug Interrupt Enable Register (DBGIER) is used only when the CPU is halted in real-time emulation mode. An interrupt enabled in the DBGIER is defined as a time-critical interrupt. When the CPU is halted in real-time mode, the only interrupts that are serviced are time-critical interrupts that are also enabled in the IER. If the CPU is running in real-time emulation mode, the standard interrupt-handling process is used and the DBGIER is ignored.

As with the IER, you can read the DBGIER to identify enabled or disabled interrupts and write to the DBGIER to enable or disable interrupts. To enable an interrupt, set its corresponding bit to 1. To disable an interrupt, set its corresponding bit to 0. Use the PUSH DBGIER instruction to read from the DBGIER and POP DBGIER to write to the DBGIER register. At reset, all the DBGIER bits are set to 0.

1.4.2 CPU1 and CPU2 Control Subsystem Exceptions Handling

The illegal exception trap condition (ITRAP) is the only type of exception (other than programmable interrupts; TRAPs and NMI), which the control subsystem supports. An ITRAP exception occurs if an illegal instruction is fetched and executed. On an ITRAP exception when the ePIE is enabled, the program counter is loaded with the vector address located at address location 0x00000D26. When the ePIE is disabled the vector address loaded in the program counter is fetched from the ROM Vector table location 0x3FFE4.

NOTE: RAM Access Violation Interrupt (INT12.12):

ePIE INT12.12 is defined for C28x RAM access violations, but for a **fetch access violation**, the C28x will receive zero data and will ITRAP. The ITRAP occurs in the same cycle at which the INT12.12 is fired to the C28x. Since the ITRAP has priority over normal interrupt, the ITRAP ISR gets executed before the INT12.12 ISR. The user needs to take this into account when servicing the ITRAP.

Please refer to the *Boot ROM* chapter for details on how the boot ROM handles this exception if it occurs during its execution.

1.4.3 CPU1 and CPU2 NMI Module

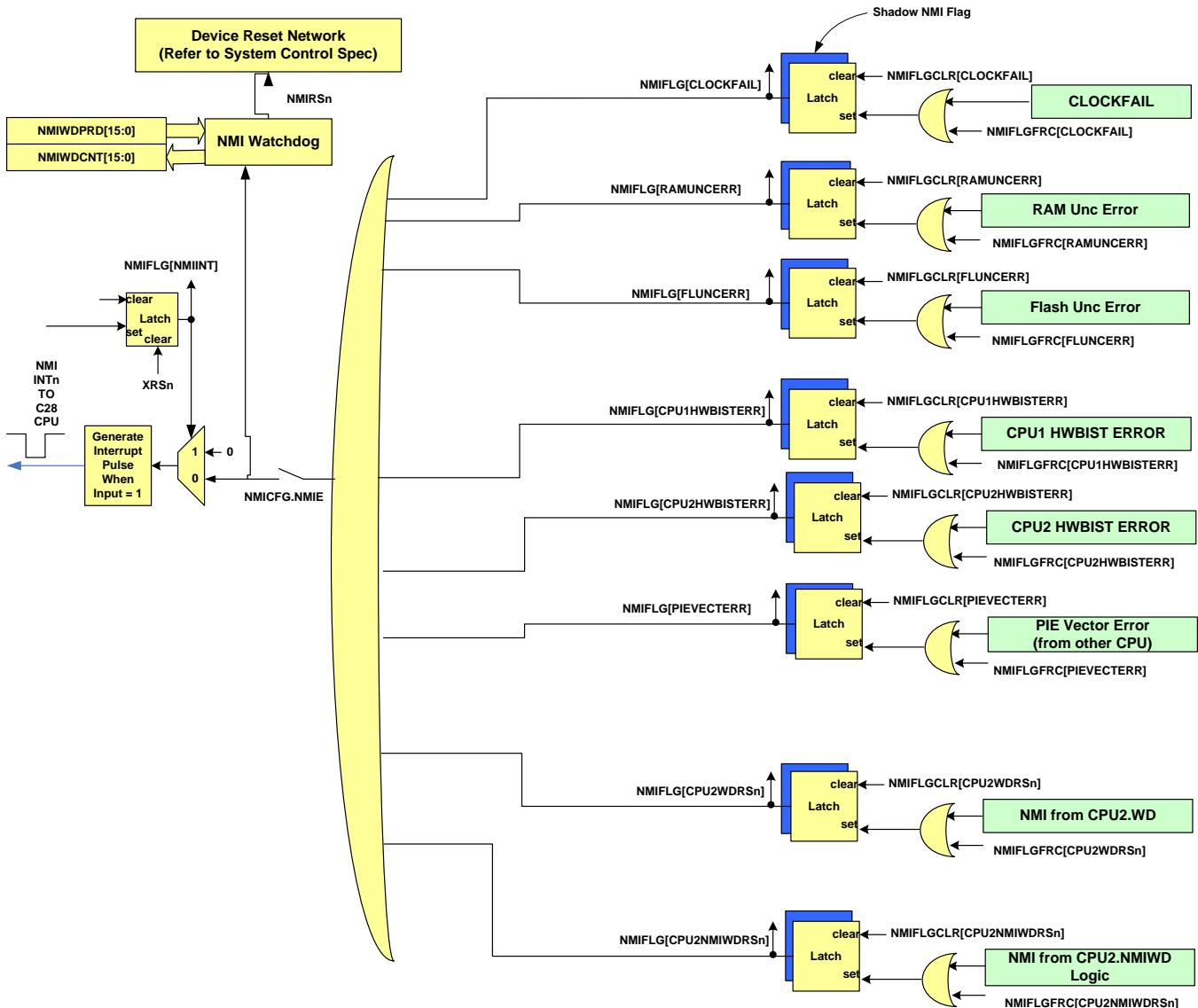
On this device, the NMI interrupt is used to monitor erroneous conditions in the system. There is a dedicated NMIWD module for each CPU. The conditions monitored are:

1. A missing clock condition
2. Uncorrectable memory errors on C28 access to Flash
3. Uncorrectable memory errors on C28, CLA or DMA access to RAM
4. C28 HW BIST ERROR (Signature FAIL or TIMEOUT) from both CPUs
5. Vector fetch ERROR on the other CPU (PIE Mismatch; refer to Safety Features)

An NMI is generated to the respective CPU if any of the above errors occur. If an NMI is triggered to the CPU, the NMI WatchDog timer will start counting and will reset the system if the counter value reaches a programmed period value. An NMI is generated to the CPU1 if the CPU2 subsystem is reset by the CPU2 NMI watchdog and an NMI watchdog reset on CPU1 will reset both CPU1 and CPU2 subsystem as shown in the **Reset Control** chapter above.

Each NMI module on the respective CPU has a shadow flag register with bits that are not cleared across an NMIWD reset. Thus, they can be used by applications to find out which NMI FLAG is set in case the CPU is recovering from a NMIWD (NMI Watchdog) reset.

[Figure 1-6](#) explains how an NMI is generated to the CPU. This is same on both CPU1 and CPU2, except that CPU2NMIWDRST and CPU2WDRST NMI sources are invalid on a CPU2 subsystem.

Figure 1-6. Control Subsystem NMI Sources and CNMIWD


As shown in [Figure 1-6](#), any of the listed errors can trigger an NMI to the C28x CPU. There is also an NMI Flag Force (NMIFLGRC) register to simulate an NMI error condition to aid in debug and development. When an NMI error event occurs:

- Respective bit in the NMIFLG register is set
- NMIINT bit in the NMIFLG register is set
- NMWD timer is triggered and starts counting. The respective FLAG bit in the NMISHDWFLG register is set.

The user has to handle the error condition that triggered the NMI by checking the individual flag bits in the NMIFLG register, clearing the set bits in the NMIFLG register, and clearing the NMIINT bit in the NMIFLG register. Clearing the NMIINT bit in the NMIFLG register will also clear the respective bit in the NMI Shadow Flag Register (NMISHDWFLG) and will stop and reset the NMWD counter back to zero. If the NMIINT bit is not cleared by the time the NMWD counter reaches the value programmed in the NMWDPRD register, the CPU subsystem in case of CPU2 and the entire device in case of CPU1 is reset. If this was CPU2, then an NMI is triggered to the CPU1 core showing that the CPU2 subsystem was reset by its NMI watchdog.

1.4.3.1 CPU1 and CPU2 NMI Sources

For information on the bits set for each of the NMI sources, please refer to NMIFLG and NMISHDWFLG register descriptions.

1.4.3.1.1 Clock Fail Condition

This error condition is detected by the missing clock detection logic explained in the Safety Features chapter. If the device was working on INTOSC2 (default) or XTALOSC and if the source clock goes missing then device automatically switches to INTOSC1 (the fall back clock) and an NMI is generated to both the cores.

1.4.3.1.2 RAMUNCERR

RAM uncorrectable error is generated by RAM wrapper logic in case a double bit ECC error is detected on the RAM(s). Please refer to the *Internal Memories* chapter for more details on this. Each CPU can only receive the NMI from its own RAM wrapper logic in case of error error detection. .

1.4.3.1.3 FLUNCERR

Flash uncorrectable error is generated by Flash wrapper logic in case a double bit ECC error is detected on the flash memories. Please refer to the *Internal Memory* chapter. Each CPU can only receive the NMI from its own flash wrapper logic in case of error detection.

1.4.3.1.4 CPU1HWBISTERR

This NMI is generated if the CPU1 HWBIST module detects any errors. Both the CPU would get this NMI.

1.4.3.1.5 CPU2HWBISTERR

This NMI is generated if the CPU2 HWBIST module detects any errors. Both the CPU would get this NMI.

1.4.3.1.6 PIEVECTERR

This NMI is generated to the current CPU if there was a vector fetch mismatch error during the fetch on an NMI on the other CPU. Please refer to safety feature chapter for more details on PIE Mismatch error detection feature.

1.4.3.1.7 CPU2WDRSn and CPU2NMIWDRSn

This NMI is generated to CPU1 only in case CPU2 is reset by its own watchdog or NMI watchdog respectively. On CPU2 these NMI bits/sources are reserved.

1.4.3.2 NMI Watchdog Module (NMIWD)

Each CPU subsystem is equipped with an NMI Watchdog module that when a non-maskable interrupt is triggered, allocates time for the user software to handle the NMI by clearing the error conditions and clearing the respective flags in the NMIFLG register or by acknowledging the NMI and gracefully shutting down the system. If none of the actions mentioned are taken, the NMIWD counter keeps counting. As soon as the counter value reaches the NMIWD period register value, it will generate a NMIWD reset, which will reset the entire device.

The NMIWD counter is clocked by the C28 system clock. The NMI WatchDog Period register (NMIWDPRD) can be programmed with a period limit as per user requirements with the clock cycle limit the user requires for software to handle or acknowledge the NMI.

1.4.3.2.1 Emulation Considerations

The NMI watchdog module behaves as below under various debug conditions.

CPU Suspended	When the CPU is suspended, the NMI watchdog counter will be suspended.
Run-Free Mode	When the CPU is placed in run-free mode, the NMI watchdog counter will resume operation as normal.
Real-Time Single-Step Mode	When the CPU is in real-time single-step mode, the NMI watchdog counter will be suspended. The counter remains suspended even within real-time interrupts.
Real-Time Run-Free Mode	When the CPU is in real-time run-free mode, the NMI watchdog counter operates as normal.

1.4.3.3 Handling of NMI

User software must clear all the flag bits which are set in the NMIFLG register before clearing the NMIINT bit (bit 0) of the NMIFLG register. If the user clears the NMIINT bit of the NMIFLG register before clearing all the individual flag bits, as soon as the NMIINT bit is cleared, it will be set back to "1" again. If a user returns from the NMI handler without clearing the NMIINT bit of the NMIFLG register, then a reset is generated when the NMWD counter value reaches the programmed period value.

1.5 Safety Features

This section gives details on different modules or features that safe guard device operation during run time and help catch serious errors that can occur. Also included are details on hardware behavior when any of the serious errors occur in the device.

1.5.1 Write Protection on Registers

1.5.1.1 LOCK Protection on System Configuration Registers

Several system configuration registers are protected from spurious CPU writes by "LOCK" registers. Once these associated LOCK register bits are set the respective locked registers can no longer be modified by software. See specific register descriptions for details.

1.5.1.2 EALLOW Protection

Several control registers are protected from spurious CPU writes by the EALLOW protection mechanism. The EALLOW bit in status register 1 (ST1) indicates the state of protection as shown in [Table 1-9](#).

Table 1-9. Access to EALLOW-Protected Registers

EALLOW Bit	CPU Writes	CPU Reads	JTAG Writes	JTAG Reads
0	Ignored	Allowed	Allowed ⁽¹⁾	Allowed
1	Allowed	Allowed	Allowed	Allowed

⁽¹⁾ The EALLOW bit is overridden via the JTAG port, allowing full access of protected registers during debug from the Code Composer Studio interface.

At reset, the EALLOW bit is cleared, enabling EALLOW protection. While protected, all writes to protected registers by the CPU are ignored and only CPU reads, JTAG reads, and JTAG writes are allowed. If this bit is set, by executing the EALLOW instruction, the CPU is allowed to write freely to protected registers. After modifying registers, they can once again be protected by executing the EDI instruction to clear the EALLOW bit.

1.5.2 Missing Clock Detection Logic

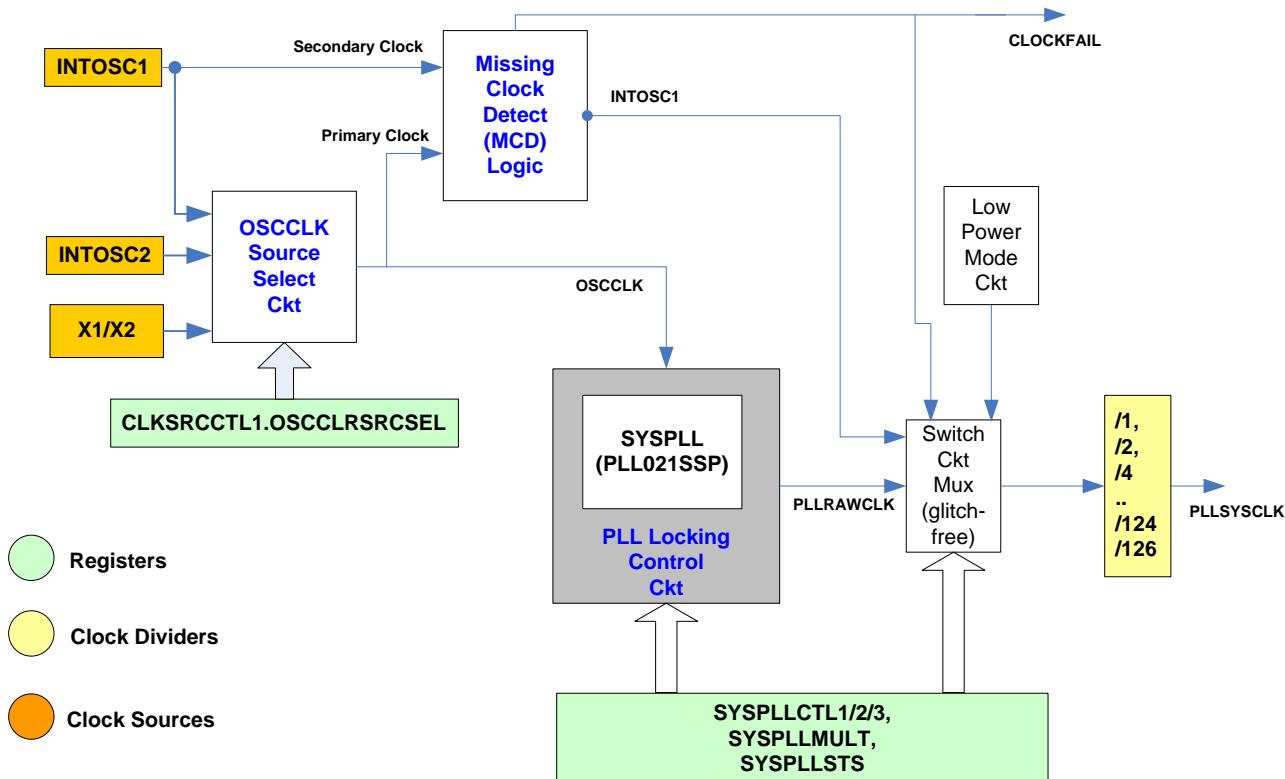
The Missing Clock Detect (MCD) logic detects OSCCLK failure using INTOSC1 as the reference clock source. This circuit only detects complete loss of OSCCLK and doesn't do any detection of frequency drift on the OSCCLK.

This circuit monitors the OSCLK (primary clock) using the 10 MHz clock provided by the INTOSC1 (secondary clock) as backup clock. This circuit functions as below:

1. The Primary Clock (OSCCLK) clock keeps ticking a 7-bit counter (named as MCDPCNT). This counter is asynchronously reseted with XRSn.
2. The Secondary Clock (INTOSC1) clock keeps ticking a 13-bit counter (named as MCDSCNT). This counter is asynchronously reseted with XRSn.
3. Every time MCDPCNT overflows, the MCDSCNT counter is reseted. Thus, if OSCCLK is present or not slower than INTOSC1 by a factor of 64, MCDSCNT will never overflow.
4. On the other hand if OSCCLK stops (for some reason) or is slower than INTOSC1 by at-least a factor of 64, the MCDSCNT will overflow and a missing clock condition will be detected on OSCCLK.
5. The above check is continuously active, unless the MCD is disabled using MCDCR register (by making MCLKOFF bit 1)
6. If the circuit ever detects a missing OSCCLK, below are the things that happen:
 - MCDSTS flag is set
 - MCDSCNT counter is frozen to prevent further missing clock detection.
 - CLOCKFAIL signal goes high, which generates TRIP events to PWM modules and fires NMIs to CPU1.NMIWD and CPU2.NMIWD
 - OSCCLK is switched to INTOSC1.
 - PLL is forcefully bypassed and clocks to the system are switched to INTOSC1 (after PLLSYSCLK divider). PLLMULT is zeroed out automatically in this case.
 - While MCDSTS bit is set, the OSCCLKSRCSEL bits have no effect and OSCCLK is forcefully connected to INTOSC1.
 - The PLLRAWCLK going to the system is switched to INTOSC1 automatically
7. If MCLKCLR bit is written (this is a W=1 bit), MCDSTS bit will be cleared and OSCCLK source will be decided by the OSCCLKSRCSEL bits. Writing to MCLKCLR will also clear the MCDPCNT and MCDSCNT counters to allow the circuit re-evaluate missing clock detection. If user wants to lock the PLL after missing clock detection, he needs to first switch the clock source to INTOSC1 (using OSCCLKSRCSEL register), do a MCLKCLR and re-lock the PLL.
8. The MCD comes up enabled at power up. There is no support of missing clock detection if INTOSC2 is failed right from the device power-up. The chance for this happening is very low as system always powers-up with an internal oscillator (INTOSC2).
9. Design must also ensure that user can dynamically switch OSCCLK source between INTOSC2 and X1/X2 without any spurious missing clock detection.

[Figure 1-7](#) shows the missing clock logic functional flow.

Figure 1-7. Missing Clock Detection Logic



1.5.3 PLLSLIP Detection

The PLL SLIP detection on this device can detect if the PLL reference clock goes too high or too slow while PLL is locked. An interrupt to both the CPU is triggered as shown in the ePIE table in [Section 1.4](#). Apart from the interrupt to both the CPUs PLLSTS.SLIP bit is set for user software to check the error.

The SLIP detection is available on both SYSPLL and AUXPLL.

Note: When SLIP happens, there is a possibility that the PLL output clock is clocking out of limits. Such situations can be detected due to the presence of WDs.

1.5.4 CPU1 and CPU2 PIE Vector Address Validity Check

The ePIE vector table on both the CPUs is duplicated into these two parts:

- Main ePIE Vector Table mapped from 0xD00 to 0xEFF in the C28x memory space
- Redundant ePIE Vector Table mapped from 0x1000D00 to 0x1000EFF in the C28x memory space

Following is the behavior of accesses to the ePIE memories:

- Data Writes to Main Vector Table: Writes to both memories
- Data Writes to Redundant Vector Table: Writes only to the Redundant Vector Table
- Vector Fetch: Data from both the vector tables are compared
- Data Read: Can read the Main and Redundant vector table separately

On every vector fetch from the ePIE, a hardware comparison (no cycle penalty is incurred to do the comparison) of both the vector table outputs is performed and if there is a mismatch between the two vector table outputs, the following happens:

1. ePIE returns a fixed value of 0x3FFFBE that points to an error handler in the boot ROM code. For each CPU, there exists a Vector Fetch Error Handler Register (CPU1.PIEVERRADDR and CPU2.PIEVERRADDR), which can be programmed by the user to jump to a user-defined routine from the default handler. The CPUx.PIEVERRADDR registers are reset to 0xffffffff. The error handler at

- address 0x3FFFBE should jump to a user-defined routine only if they are programmed to a “non 0xffffffff” value.
2. Hardware also generates EPWM Trip signals which will trip the PWM outputs using TRIPIN15.
 3. An NMI to the other CPU is sent if the current mismatch is during an NMI fetch. For example, on an nmi vector fetch error for CPU2, an NMI input is fired to CPU1.NMIWD.

If there is no mismatch, the correct vector is jammed on to the C28 program control.

1.5.5 NMIWDs

Both the CPU subsystems have user-programmable NMIWD period registers in which users can set a limit on how much time they want to allocate for the device to acknowledge the NMI. If the NMI is not acknowledged, it will cause a device reset.

1.5.6 ECC and Parity Enabled RAMs, Shared RAMs Protection

RAM memories in both the CPU subsystems are ECC and parity enabled. All single-bit errors in RAM are auto corrected and an error counter is incremented every time a single bit error is incremented. If the error counter reaches a predefined user configured limit, then an interrupt is generated to each CPU. Refer to the *Internal Memory* chapter for more details on RAM errors.

All uncorrectable double-bit errors end up triggering a BUS FAULT on the master subsystem's CPU and an NMI on the control subsystem. A RAMACCVIOL on the master subsystem triggers an NMI on both the CPUs.

1.5.7 ECC Enabled Flash Memory

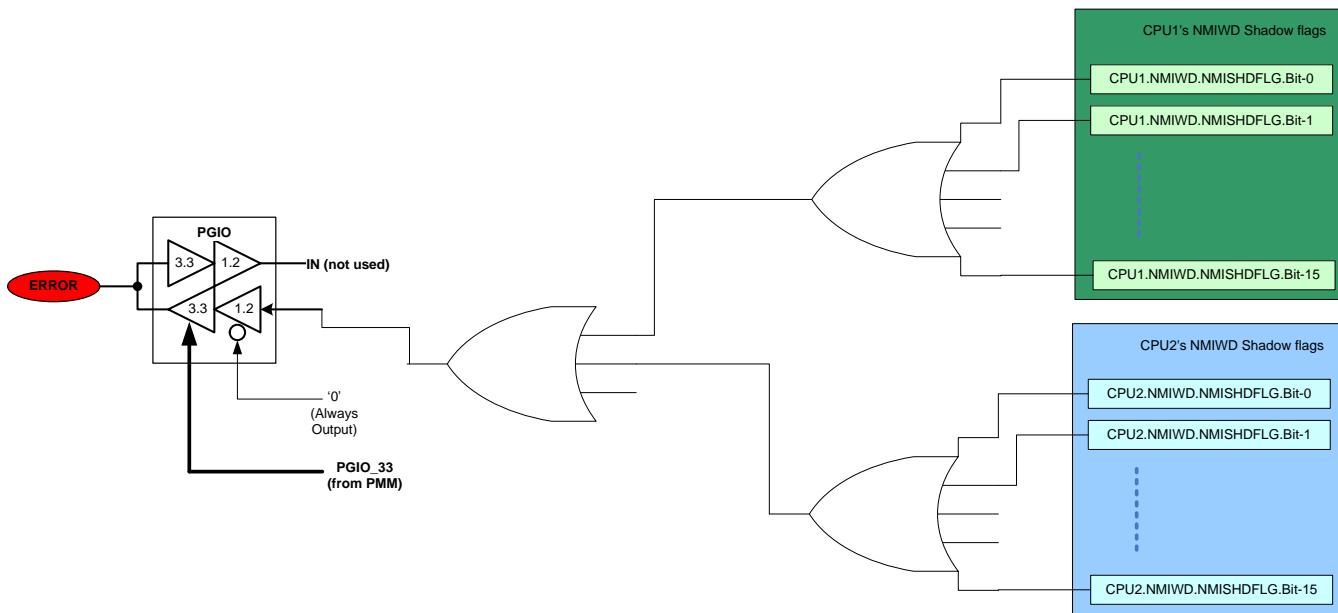
When ECC is programmed and enabled, Flash single-bit errors are corrected automatically by ECC logic before giving data to the CPU, but they are not corrected in flash memory. Flash memory will still contain wrong data until another erase/program operation happens to correct the flash contents. Irrespective of whether the error interrupt is enabled or disabled, single bit errors are always corrected before giving data to the CPU. When the interrupt is disabled, users can check the single-bit error counter register for any single bit error occurrences. The error counter stops incrementing once its value is equal to the threshold+1. It is always suggested to set the threshold register to a non-zero value so that the error counter can increment. It is up to the user to decide the threshold value at which they have to reprogram the flash with the correct data.

When ECC is programmed and enabled, Flash uncorrectable errors end up triggering an NMI to the respective CPU. Please refer to the *Internal Memory* chapter of this document for more details on flash error correction and error catching mechanisms.

1.5.8 Error Pin

The ERROR pin is an ‘always output’ pin and remains low till an error is detected inside the chip. On an error, the ERROR pin goes high till the corresponding internal error status flag for that error source is cleared. Below diagram shows functionality of the ERROR pin.

The error pin will be tri-stated till the chip power rails ramp up to operational limit. As the ERROR pin is an active-high pin, users who care about the state of this pin during power-up should connect an external pull-down on this pin.

Figure 1-8. Error Pin Diagram


1.6 Power Management

External 3.3V and 1.2V low-dropout regulators (LDO) will need to be used to supply the 3.3V and 1.2V power rails. Tie the VREGENZ pin high through a 2.2-k Ω external pullup resistor.

1.7 Clock Control

In this device, clock registers can be acquired by either CPU1 and CPU2 using clock semaphore (CLKSEM). By default, CPU1 owns the clock semaphore (CLKSEM) which provides control of clock configuration registers to CPU1. When CPU1 owns the clock semaphore, CPU2 writes to clock configuration registers are ignored and CPU2 reads 0x0000s.

1.7.1 Clock Sources

There are four possible reference clock sources in this device:

Clock source	Comments
INTOSC1	Two zero-pin overhead 10Mhz internal oscillators
INTOSC2	Two zero-pin overhead 10Mhz internal oscillators
XTAL	External oscillator, connected between X1 and X2 pins
GPIO_AUXCLKIN	Single-ended 3.3v level clock source

The following sections give more details on each clock source.

1.7.1.1 OSCCLK

The OSCCLK selected is used as the reference clock by the system PLL to generate the system clock for the device as shown in [Figure 1-9](#).

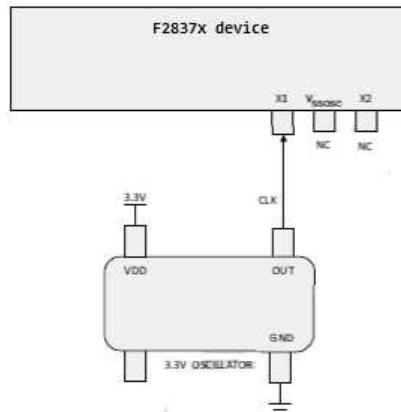
OSCCLK source	Register settings
INTOSC2	CLKSRCCTL1.OSCCLKSRCSEL = 0 (default option)
XTAL	CLKSRCCTL1.OSCCLKSRCSEL = 1
INTOSC1	CLKSRCCTL1.OSCCLKSRCSEL = 2

- Internal oscillator 1 (INTOSC1): On-chip 10 MHz internal oscillator. This can provide the clock for the watchdog block, system clock and CPU timers.
- Internal oscillator (INTOSC2): On-chip 10 MHz internal oscillator. This can provide clock for system clock, auxiliary clock and CPU timers.
- External clock (XTAL): This option allows the user to provide an external clock to the device. This can provide clock for system clock, auxiliary clock, and CPU timers.

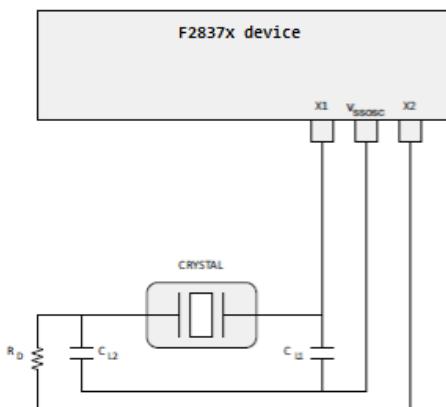
When the XTAL option is selected, the clock source can be externally provided by one of the following options:

- Connect an external single ended clock source connected to X1 pin and X2 unconnected as shown here.

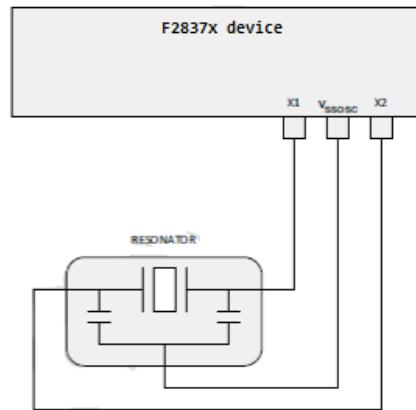
Figure 1-9. OSCCLK Reference



- Connect an external crystal across X1 input and X2 output pin as shown here.



- Connect a external resonator across X1 input and X2 output pin as shown here.



NOTE: The frequency of input clock source applied through single ended clock source, crystal (or) resonator should be according to the data sheet recommendations.

1.7.1.2 AUXOSCCLK Clock Source

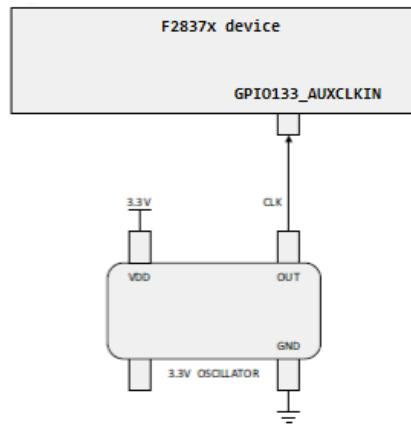
AUXOSCCLK selected is used as reference clock by AUXPLL to generate 60MHz USB clock as shown in [Figure 1-10](#).

Table 1-10. AUXOSCCLK Source

AUXOSCCLK source	Register settings
INTOSC2	CLKSRCCTL2.AUXOSCCLKSRCSEL = 0 (default option)
XTAL	CLKSRCCTL2.AUXOSCCLKSRCSEL = 1
GPIO_AUXCLKIN	CLKSRCCTL2.AUXOSCCLKSRCSEL = 2

The GPIO133 / AUXCLKIN pin can be used provide external clock input as shown in [Figure 1-10](#).

Figure 1-10. AUXCLKIN



1.7.2 PLLs

This device includes a PLL for clocking the entire system, known as the System PLL (SYSPLL) and a second PLL, known as Auxiliary PLL (AUXPLL) is used to generate a fixed 60MHz clock used for timing the USB bit-level communication or to clock the delay-line portion of the HRCAP modules.

SYSPLL generates output frequency PLLCLK, based on the following relationship with OSCLK, the input frequency. The SYSPLL by itself supports a PLLCLK range of 110-550MHz. Therefore, application must ensure that the PLL multiplier values should be chosen such that PLLCLK is always within permissible PLLCLK range, namely between 110 and 550MHz.

$$\text{PLLCLK} = \text{OSCCLK} \times (\text{SYSPLLMULT.IMULT} + \text{SYSPLLMULT.FMULT})$$

So,

$$\text{PLLSYSCLK} = \text{PLLCLK} / \text{SYCLKDIVSEL}$$

Similarly, AUXPLL generates output frequency AUXPLLRAWCLK, based on the following relationship with AUXOSCCLK, the input frequency.

$$\text{AUXPLLRAWCLK} = \text{AUXOSCCLK} \times (\text{AUXPLLMULT.IMULT} + \text{AUXPLLMULT.FMULT})$$

So,

$$\text{AUXPLLCLK} = \text{AUXPLLRAWCLK} / \text{AUXCLKDIVSEL}$$

For example,

If OSCCLK = 10Mhz

With SYSPLL settings, SYSPLLMULT.IMULT = 30, SYSPLLMULT.FMULT = 2 (0.50) and SYCLKDIVSEL = 2

PLLCLK = 10 Mhz x (30+0.50) = 305 Mhz (PLLCLK within acceptable PLLCLK range of 110 – 550 Mhz)

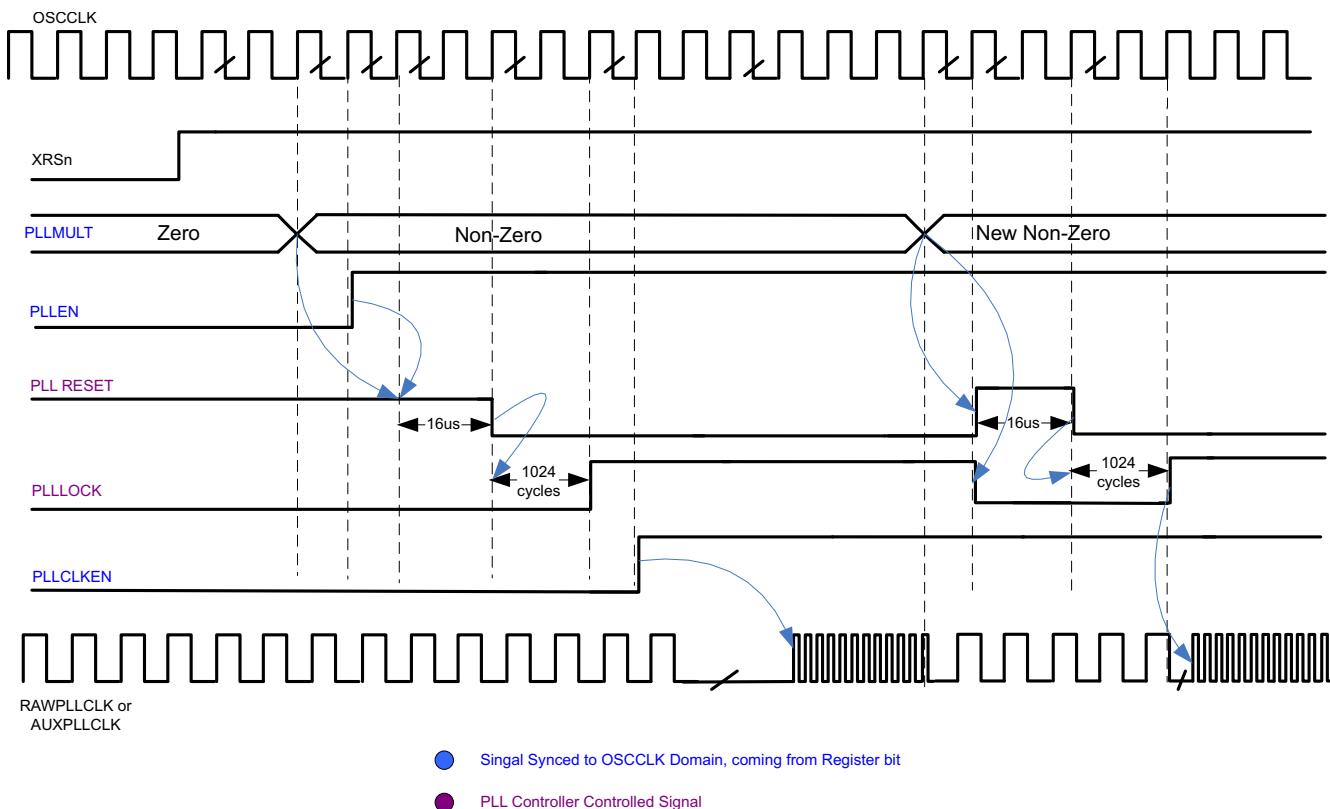
$$\text{PLLSYSCLK} = 305 \text{ Mhz} / 2 = 152.5 \text{ Mhz}$$

NOTE:

1. The application must ensure that SYSPLLMULT values should be chosen such that PLLCLK is always within a permissible PLLCLK range, namely between 110 and 550 MHz.
2. The purpose of /2, /4, /6 and /8 dividers (SYCLKDIVSEL) is to reduce inrush current at power-up.
3. In SUSPLLMULT and AUXPLLMULT registers, both IMULT and FMULT bit fields must be written by the CPU on the same cycle for proper operation of the PLL.
4. Ensure no resources are using a clock source prior to disabling it (for example, OSCCLKSRCSEL(SYSPLL), AUXOSCCLKSRCSEL(AUXPLL), CANx Clock, CPUTIMER2 and XCLOCKOUT).

1.7.2.1 PLL Locking Sequence

Figure 1-11 shows the graphical view of the locking sequence and the steps below provide the explanation of the sequence.

Figure 1-11. PLL Locking Sequence


1. To lock the PLL first-time after power-up, program the **PLLMULT** and write to the **PLLLEN** bit to power-up the PLL.
2. Once the PLL is powered up, the **RESET** is kept asserted for 16us. This time is counted using the 10Mhz INTOSC1 counter.
3. Once **RESET** is de-asserted, PLL takes 1024 reference clock cycles to get locked. At the end of 1024 cycle, **PLLLOCK** bit will be set.
4. Software can poll the **PLLLOCK** bit and once it detects that the PLL is locked, clocks to the system (or to USB bit-clock) can be switched to PLL output by setting to the **PLLCLKEN** bit.
5. The PLL can be powered down any time by software using the **PLLLEN** bit. If this happens, clocks to the system (or to the USB bit-clock) automatically switch to OSCCLK. Also, when device goes to the HALT mode, PLL is powered down.
6. After the PLL is locked, if user changes the **PLLMULT** to re-lock the PLL, this change in **PLLMULT** is detected and steps 3 to 6 repeats to re-lock the PLL.
7. While the PLL is locked, any changes to the reference clock to the PLL (using CLKSRCCTL1 register for SYSPLL and CLKSRCCTL2 register for AUXPLL) will automatically bypass the PLL. This rule has the below exception:
 - In F2837x, the clock registers can be acquired by either CPU1 and CPU2 using clock semaphore (CLKSEM). Note that if CPU2 acquires the clock control registers after the PLL has been clocked from CPU1, any change in the PLL reference clock from CPU2 doesn't automatically bypass the PLL. For such scenarios, users need to first bypass the PLL and then change the PLL reference clock source.
8. While the PLL is powered down, any write to PLL multiplier register (SYSPLLMULT register for SYSPLL and AUXPLLMULT for AUXPLL) will automatically power-up the PLL.

Bypassing SYSPLL

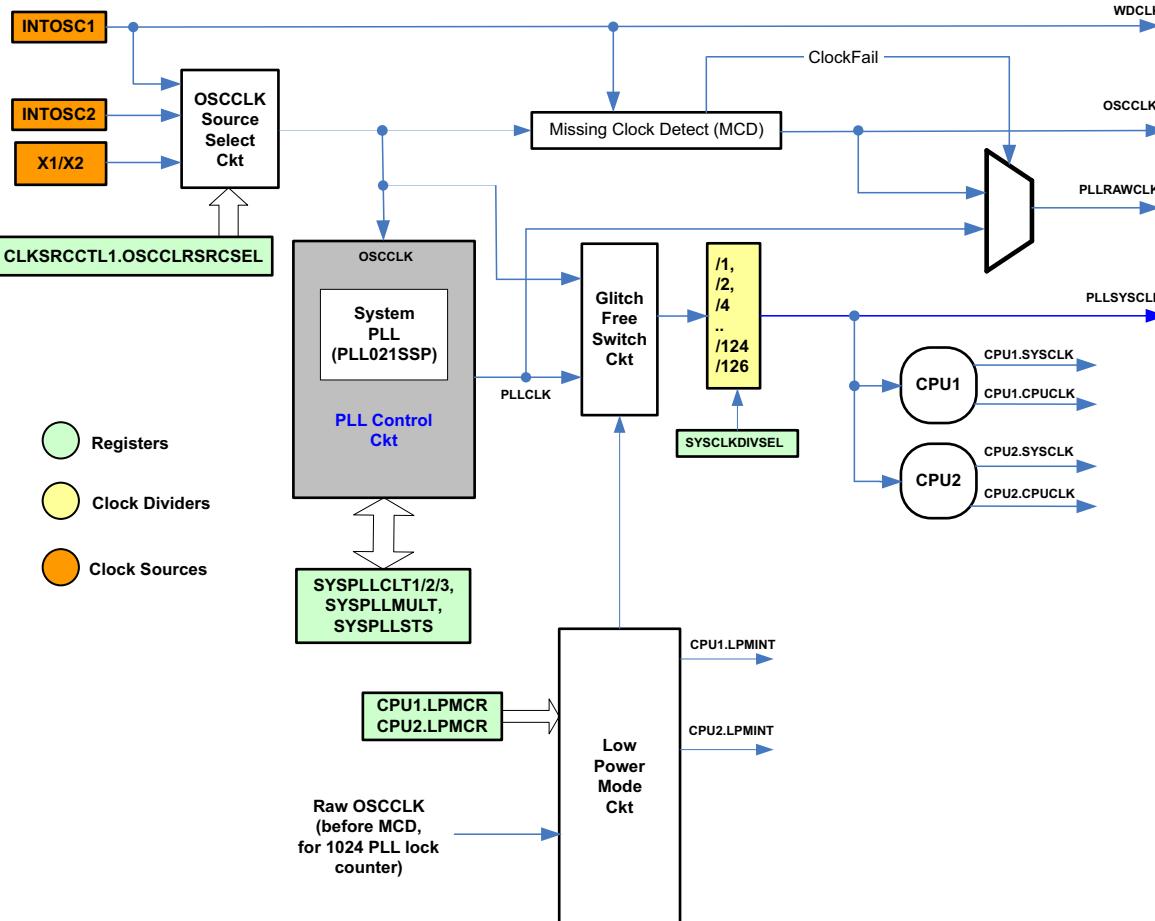
When **SYSPLLCTL1.PLLCLKEN = 0**, SYSPLL will be bypassed and **PLLSYSCLK** is directly fed from **OSCCLK**

or

When SYSPLLMMULT = 0, SYSPLL is bypassed

Bypassing AUXPLL-**1.7.2.2 System PLL Clocking Section**

Figure 1-12 shows the block diagram of system PLL clocking section and shows how each of the clock are derived.

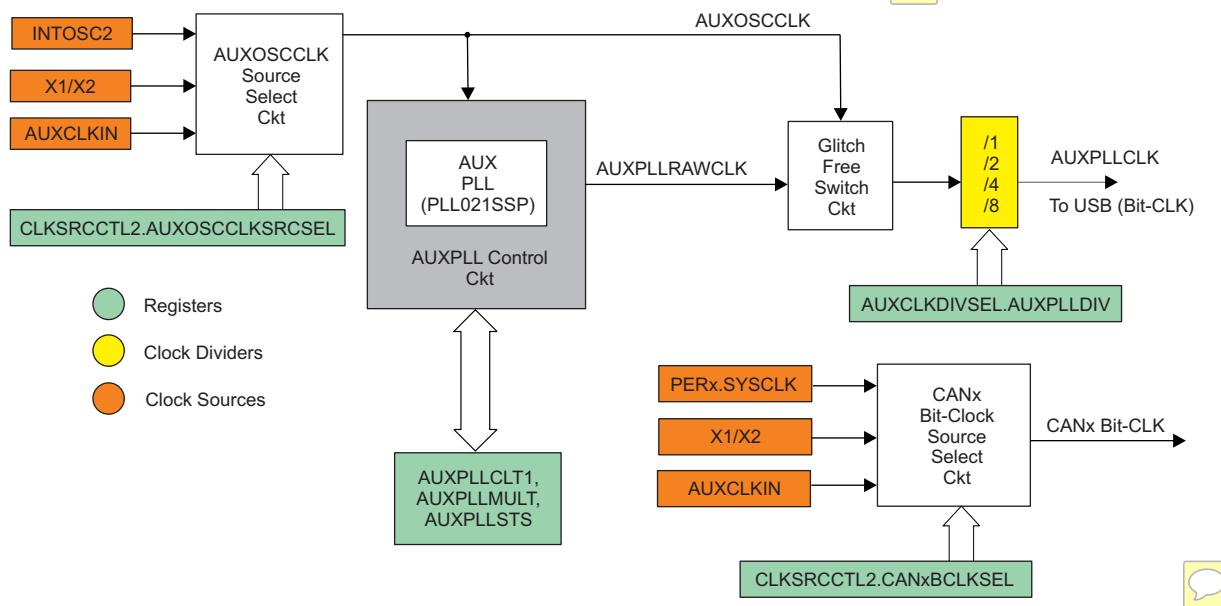
Figure 1-12. Clocking Options for System PLL

Note: The clock name for peripheral clocking 'PERx.SYSCLK' is used interchangeably with 'SYSLKOUT' in the device documentation.

1.7.2.3 AUX PLL Clocking Section

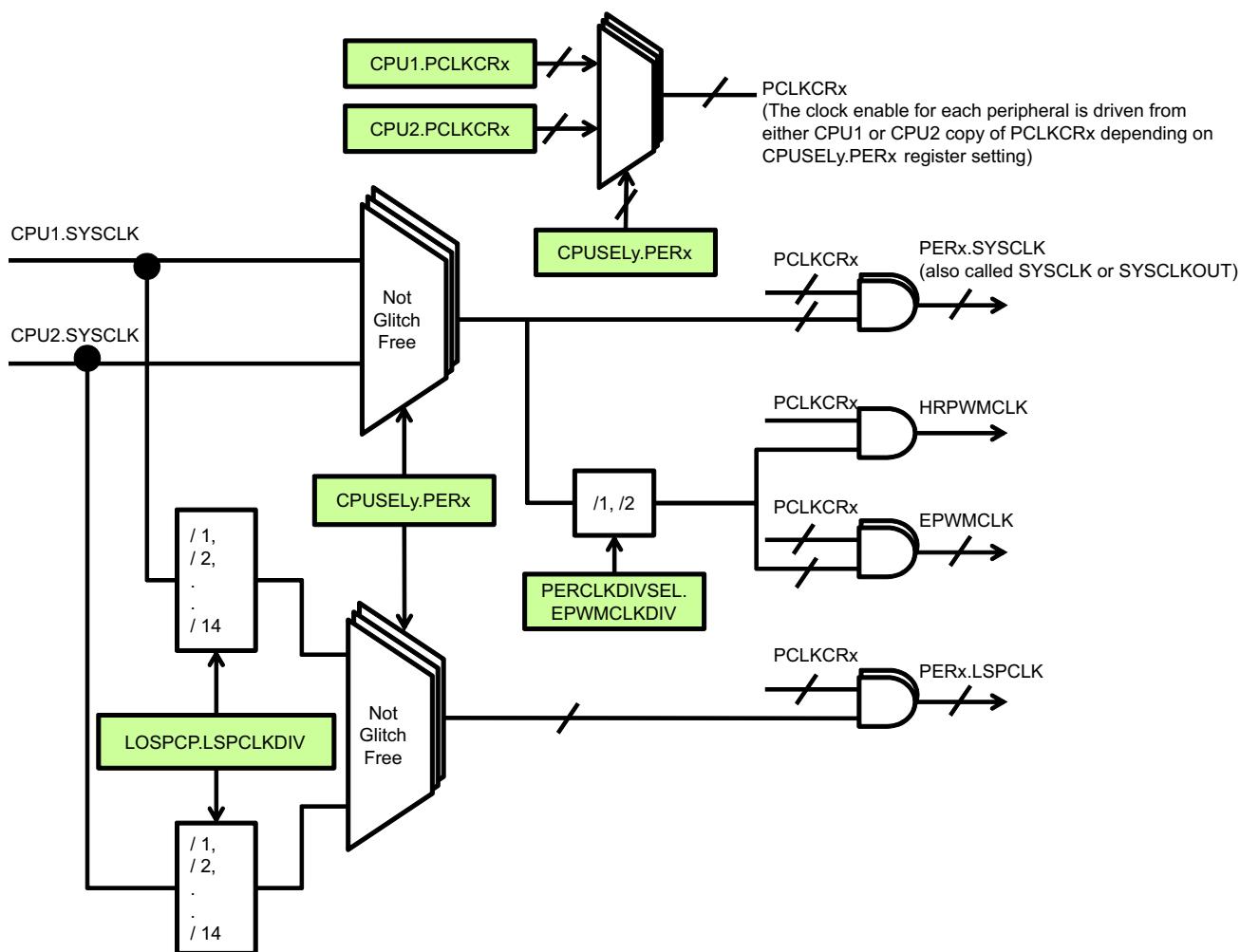
Figure 1-13 shows the block diagram of AUX PLL clocking section and shows how AUXPLLCLK and CANx bit CLK are derived.

Figure 1-13. Clocking Options for Auxiliary PLL



1.7.2.4 Peripheral Clocking Section

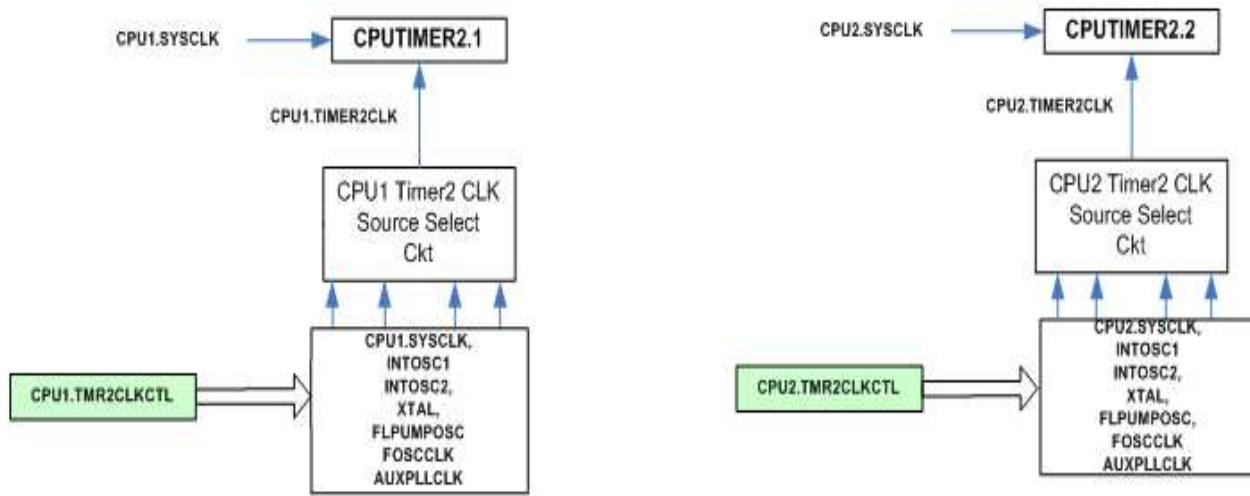
Each peripheral can be clocked by either CPU1.LSPCLK (or) CPU2.LSPCLK by using CPUSEL_y.PER_x as shown in [Figure 1-14](#).

Figure 1-14. Peripheral Clock Options

1.7.2.5 CPU Timer Clocking Section

The CPU timer2 clock options are shown in [Figure 1-15](#).

Figure 1-15. CPU Timer2 Clock Options

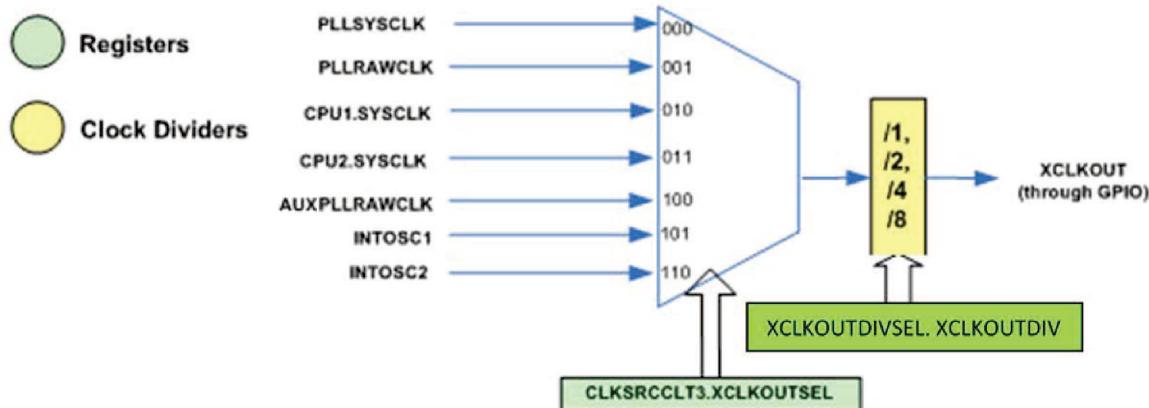


1.7.2.6 XCLKOUT Generation

GPIO73 can be configured to bring out XCLKOUT functionality. Refer to the GPIOs chapter of this document on how to configure this GPIO for XCLKOUT operation.

CLKSRCCTL3.XCLKOUTSEL can be used to bring out one of the clock domains to XCLKOUT pin as shown in Figure 1-16.

Figure 1-16. XCLKOUT Generation



1.7.2.7 Clock Connectivity Information

The tables below provide details of the clocks' connectivity to all the modules present in the device.

CPU1/2.SYSCLK: System Clock output of the respective C28x cores which keeps ticking even when C28x is in IDLE.

CPU1.SYSCLK	CPU2.SYSCLK
CPU1.CLA1	CPU2.CLA1
CPU1.DMA	CPU2.DMA
CPU1.ePIE	CPU2.ePIE
CPU1.Timers	CPU2.Timers
CPU1.DCSM	CPU2.DCSM
EMIF1	EMIF1
EMIF2	
CLA to CPU1 MSG RAM wrapper	CLA to CPU2 MSG RAM wrapper
CPU1 to CLA MSG RAM wrapper	CPU2 to CLA MSG RAM wrapper
GPIO	GPIO
CPU1.LS0-LS5 RAM	CPU2.LS0-LS5 RAM
uPP_A/B	
USB and USB-PHY	
XINT	

CPU1/2.CPUCLK: System Clock output of the respective C28x cores which stops ticking when C28x is in IDLE.

CPU1.CPUCLK	CPU2.CPUCLK
CPU1.VCU	CPU2.VCU
CPU1.FPU	CPU2.FPU
CPU1.TMU	CPU2.TMU
CPU1.Flash wrapper	CPU2.Flash wrapper
CPU1.M0 RAM	CPU2.M0 RAM
CPU1.M1 RAM	CPU2.M1 RAM
CPU1.D0 RAM	CPU2.D0 RAM
CPU1.D1 RAM	CPU2.D1 RAM
CPU1.BOOTROM	CPU2.BOOTROM

PLLSYSCLK: Clock source which is after the SYSPLL DIV divider (refer to [Figure 1-12](#)).

PLLSYSCLK
All Syscontrol registers
CPU1.NMIWD
CPU2.NMIWD
CPU1.NMIWD
GS0-GS15 RAM Wrappers
IPC between CPU1 & CPU2

PERx.SYSCLK: The clock to each of the common peripherals can be selectively connected to either CPU1.SYSCLK or CPU2.SYSCLK using the CPUSEL register as shown in [Figure 1-12](#).

PERx.SYSCLK
eCAP
eQEP
SDFM
CAN
ADC wrapper
DAC + CMPSS Wrappers
SPI
SCI
McBSP

PERx.LSPCLK: Refer to [Figure 1-14](#).

PERx.LSPCLK
SPI
SCI
McBSP

INTOSC1 Refer to [Figure 1-14](#).

INTOSC1
CPU1.Watchdog
CPU2.Watchdog

1.8 32-Bit CPU Timers 0/1/2

This section describes the three 32-bit CPU-timers (TIMER0/1/2) shown in (Figure 1-17).

CPU Timer-0 and CPU-Timer 1 can be used in user applications. Timer 2 is reserved for DSP/BIOS. If the application is not using DSP/BIOS, then Timer 2 can be used in the application. The CPU-timer interrupt signals (TINT0, TINT1, TINT2) are connected as shown in Figure 1-18.

Figure 1-17. CPU-Timers

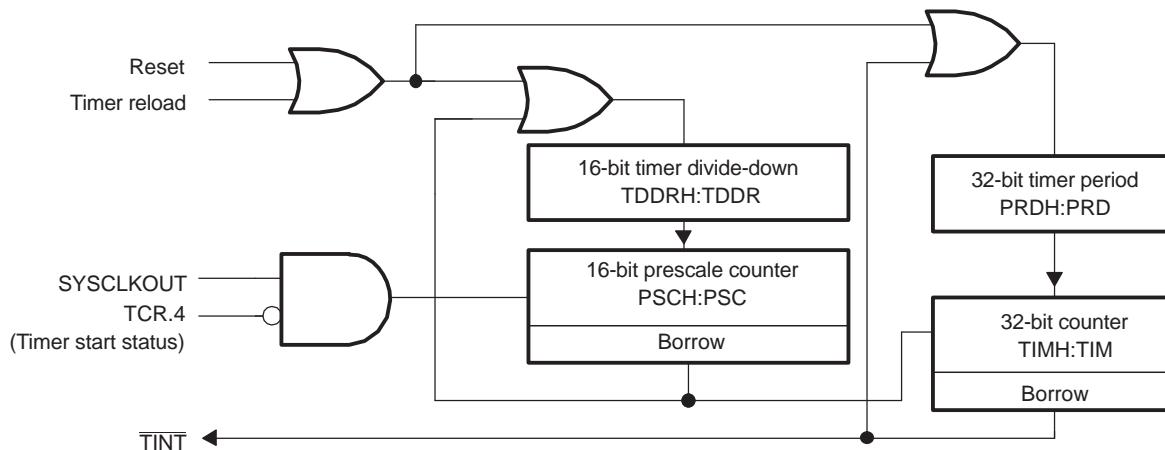
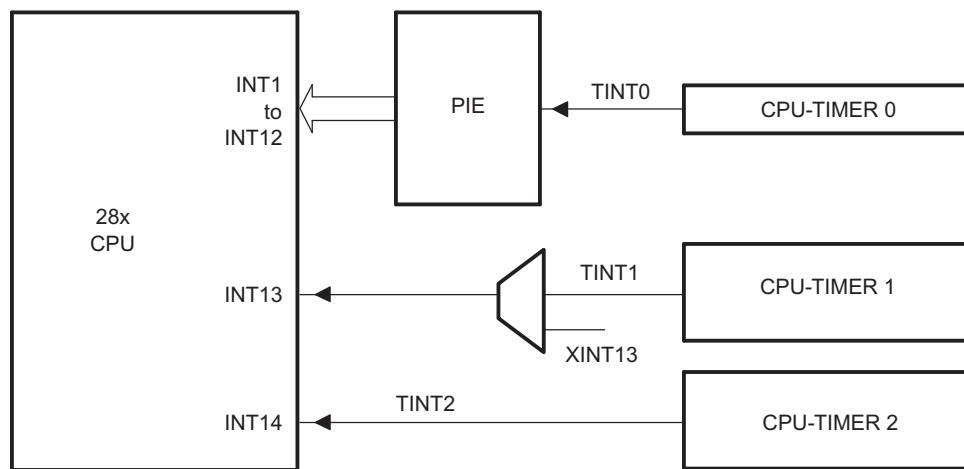


Figure 1-18. CPU-Timer Interrupts Signals and Output Signal



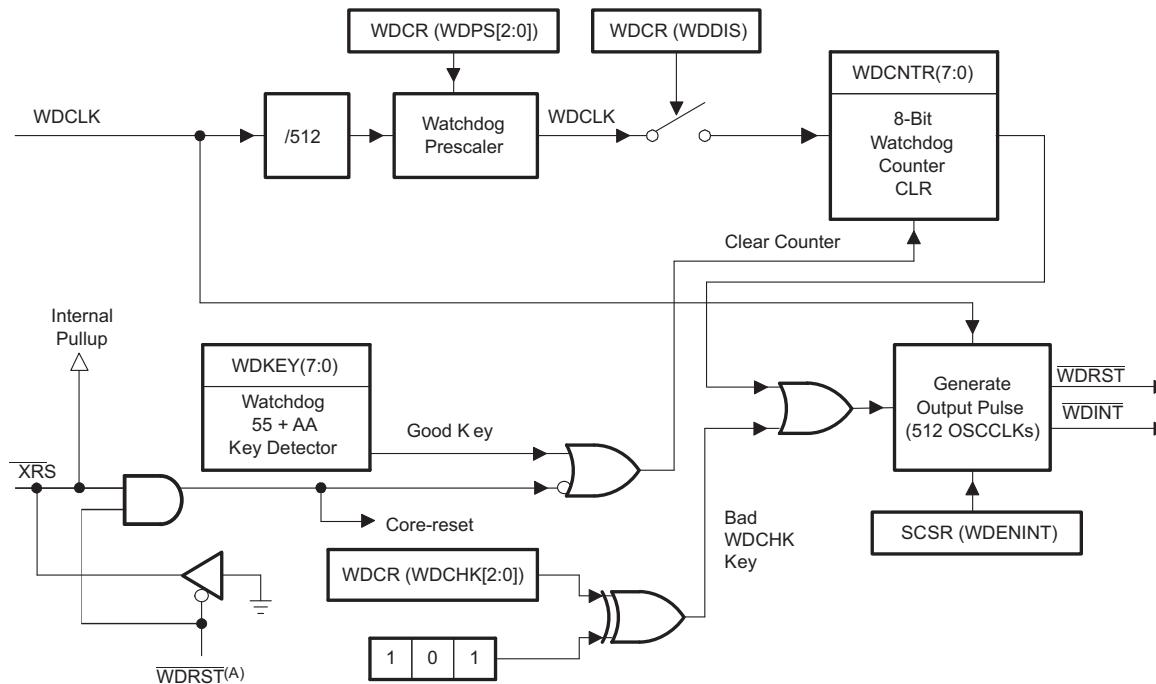
- A The timer registers are connected to the Memory Bus of the C28x processor.
- B The timing of the CPU timers are synchronized to SYSCLKOUT of the processor clock.

The general operation of the CPU-timer is as follows: The 32-bit counter register TIMH:TIM is loaded with the value in the period register PRDH:PRD. The counter decrements once every $(TPR[TDDRH:TDDR]+1)$ SYSCLKOUT cycles, where TDDRH:TDDR is the timer divider. When the counter reaches 0, a timer interrupt output signal generates an interrupt pulse. The registers listed below are used to configure the timers.

1.9 Watchdog Timers

The watchdog module generates an output pulse 512 oscillator clocks (OSCCLKs) wide whenever the 8-bit watchdog up counter has reached its maximum value. Software must periodically write a 0x55 + 0xAA sequence into the watchdog key register to reset the watchdog counter. The counter can also be disabled. Figure 1-19 shows the various functional blocks within the watchdog module.

Figure 1-19. CPU Watchdog Module



1.9.1 Servicing the Watchdog Timer

The WDCNTR is reset when the proper sequence is written to the WDKEY register before the 8-bit watchdog counter (WDCNTR) overflows. The WDCNTR is reset-enabled when a value of 0x55 is written to the WDKEY. When the next value written to the WDKEY register is 0xAA then the WDCNTR is reset. Any value written to the WDKEY other than 0x55 or 0xAA causes no action. Any sequence of 0x55 and 0xAA values can be written to the WDKEY without causing a system reset; only a write of 0x55 followed by a write of 0xAA to the WDKEY resets the WDCNTR.

Table 1-11. Example Watchdog Key Sequences

Step	Value Written to WDKEY	Result
1	0xAA	No action
2	0xAA	No action
3	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
4	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
5	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
6	0xAA	WDCNTR is reset.
7	0xAA	No action
8	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
9	0xAA	WDCNTR is reset.
10	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
11	0x32	Improper value written to WDKEY. No action, WDCNTR no longer enabled to be reset by next 0xAA.
12	0xAA	No action due to previous invalid value.

Table 1-11. Example Watchdog Key Sequences (continued)

Step	Value Written to WDKEY	Result
13	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
14	0xAA	WDCNTR is reset.

Step 3 in Table 1-11 is the first action that enables the WDCNTR to be reset. The WDCNTR is not actually reset until step 6. Step 8 again re-enables the WDCNTR to be reset and step 9 resets the WDCNTR. Step 10 again re-enables the WDCNTR to be reset. Writing the wrong key value to the WDKEY in step 11 causes no action, however the WDCNTR is no longer enabled to be reset and the 0xAA in step 12 now has no effect.

If the watchdog is configured to reset the device, then a WDCR overflow or writing the incorrect value to the WDCR[WDCHK] bits will reset the device and set the watchdog flag (WDFLAG) in the WDCR register. After a reset, the program can read the state of this flag to determine the source of the reset. After reset, the WDFLAG should be cleared by software to allow the source of subsequent resets to be determined. Watchdog resets are not prevented when the flag is set.

1.9.2 Minimum Window Check

To complement the timeout mechanism, the watchdog also contains an optional "windowing" feature that requires a minimum delay between counter resets. This can help protect against error conditions that bypass large parts of the normal program flow but still include watchdog handling.

To set the window minimum, write the desired minimum watchdog count to the WDWCR register. This value will take effect after the next WDKEY sequence. From then on, any attempt to service the watchdog when WDCNTR is less than WDWCR will trigger a watchdog interrupt or reset. When WDCNTR is greater than or equal to WDWCR, the watchdog can be serviced normally.

At reset, the window minimum is zero, which disables the windowing feature.

1.9.3 Watchdog Reset or Watchdog Interrupt Mode

The watchdog can be configured in the SCSR register to either reset the device (WDRST) or assert an interrupt (WDINT) if the watchdog counter reaches its maximum value. The behavior of each condition is described below:

- **Reset mode:**

If the watchdog is configured to reset the device, then the WDRST signal will pull the device reset (XRS) pin low for 512 OSCCLK cycles when the watchdog counter reaches its maximum value.

- **Interrupt mode:**

When the watchdog counter expires, it will assert an interrupt by driving the WDINTn signal low for 512 OSCCLK cycles. The falling edge of WDINTn triggers a WAKEINT interrupt in the PIE if it is enabled. Because the PIE is edge-triggered, re-enabling the WAKEINT while WDINTn is active will not produce a duplicate interrupt.

To avoid unexpected behavior, software should not change the configuration of the watchdog while WDINTn is active. For example, changing from interrupt mode to reset mode while WDINTn is active will immediately reset the device. Disabling the watchdog while WDINTn is active will cause a duplicate interrupt if the watchdog is later re-enabled. If a debug reset is issued while WDINTn is active, the reset cause register (RESC) will show a watchdog reset. The WDINTS bit in the SCSR register can be read to determine the current state of WDINTn.

1.9.4 Watchdog Operation in Low Power Modes

In IDLE mode, the watchdog interrupt (WDINTn) signal can generate an interrupt to the CPU to take the CPU out of IDLE mode. As with any other peripheral, the watchdog interrupt will trigger a WAKEINT interrupt in the PIE during IDLE mode. User software must determine which peripheral caused the interrupt.

In STANDBY mode, all of the clocks to the peripherals are turned off within the CPU subsystem. The only peripheral that remains functional is the watchdog since the watchdog module runs off the oscillator clock (OSCCLK). The WDINTn signal is fed to the Low Power Modes (LPM) block so that it can be used to wake the CPU from STANDBY low power mode. This feature is enabled by setting LPMCR.WDINTE = 1. See the Low Power Modes section of the device technical reference manual for details.

Note: If the watchdog interrupt is used to wake-up from an IDLE or STANDBY low power mode condition, software must make sure that the WDINTn signal goes back high before attempting to re-enter the IDLE or STANDBY mode. The WDINTn signal will be held low for 512 OSCCLK cycles when the watchdog interrupt is generated. You can determine the current state of WDINTn by reading the watchdog interrupt status bit (WDINTS) bit in the SCSR register. WDINTS follows the state of WDINTn by two SYSCLKOUT cycles.

In HALT mode, the internal oscillators and CPU1 watchdog are kept active if the user sets CLKSRCCTL1.WDHALTI = 1. A watchdog reset can wake the system from HALT mode, but a watchdog interrupt cannot.

1.9.5 Emulation Considerations

The watchdog module behaves as follows under various debug conditions:

CPU Suspended:	When the CPU is suspended, the watchdog clock (WDCLK) is suspended
Run-Free Mode:	When the CPU is placed in run-free mode, then the watchdog module resumes operation as normal.
Real-Time Single-Step Mode:	When the CPU is in real-time single-step mode, the watchdog clock (WDCLK) is suspended. The watchdog remains suspended even within real-time interrupts.
Real-Time Run-Free Mode:	When the CPU is in real-time run-free mode, the watchdog operates as normal.

1.10 Low Power Modes

This device has three clock-gating low-power modes and a special power-gating mode. All low-power modes are entered by setting the LPMCR register and executing the C28x CPU's IDLE instruction. More information about this instruction can be found in section 6.2 of the TMS320C28x CPU and Instruction Set Reference Guide (SPRU430).

1.10.1 IDLE

IDLE is a standard feature of the C28x CPU. In this mode, the CPU clock is gated while all peripheral clocks are left running. IDLE can thus be used to conserve power while a CPU is waiting for peripheral events. When one CPU is in IDLE, there is no effect on the other CPU subsystem.

Any enabled interrupt will wake the CPU up from IDLE mode.

To enter IDLE mode, set LPMCR.LPM to 00 and execute the IDLE instruction.

1.10.2 STANDBY

STANDBY is a more aggressive low-power mode that gates both the CPU clock and any peripheral clocks derived from that CPU's SYSCLK. The watchdog, however, is left active. Like IDLE, this mode affects only one CPU subsystem. The other CPU subsystem and all of its peripherals are unaffected. STANDBY is best suited for an application where the wake-up signal will come from an external system (or CPU subsystem) rather than a peripheral input.

IPC interrupt 1 (flag 0), an NMI fired to the other CPU, or (optionally) a watchdog interrupt will wake the CPU subsystem up from STANDBY mode. Any of GPIOs 0-63 can also be configured to wake up the subsystem when they are driven active low. On wakeup, the CPU receives a WAKEINT interrupt, even if it was woken by an IPCINT1 signal.

To enter STANDBY mode:

1. Set LPMCR.LPM to 01.
2. Enable the WAKEINT interrupt in the PIE.
3. For watchdog interrupt wakeup, set LPMCR.WDINTE to 1 and configure the watchdog to generate interrupts.
4. For GPIO wakeup, set GPIOLOPMSEL0 and GPIOLOPMSEL1 to connect the chosen GPIOs to the LPM module, and set LPMCR.QUALSTDBY to select the number of OSCCLK cycles for input qualification.
5. execute the IDLE instruction to enter STANDBY.

To wake up from Standby mode:

1. Configure the desired GPIO to trigger the wakeup, as well as the number of OSCCLK cycles for qualification, via the GPIOLOPMSEL0/1 register.
2. Drive the selected GPIO signal low; it must remain low for the number of OSCCLK cycles specified in the QUALSTDBY bits in the LPMCR register. If the signal is sampled high during this period, the count restarts.

At the end of the qualification period, the PLL enables the CLKIN to the CPU and the WAKEINT interrupt is latched in the PIE Block. WAKEINT interrupt can also triggered by IPCINT1 sent from the other CPU and a watchdog interrupt.

The device is now out of Standby mode and can resume normal execution.

1.10.3 HALT

HALT is a global low-power mode that gates almost all system clocks and allows for power-down of oscillators and analog blocks. This mode affects both CPU subsystems. HALT can be used for additional power savings over putting both CPU subsystems in STANDBY, although the options for wakeup are more limited.

Similar to STANDBY, any of GPIOs 0-63 can be configured to wake up the system from HALT. No other wakeup option is available. However, CPU1's watchdog is still clocked, and can be configured to produce a watchdog reset if a timeout mechanism is needed. On wakeup, both CPUs receive a WAKEINT interrupt.

To enter HALT mode:

1. Enable the WAKEINT interrupt in the PIE on both CPUs.
2. Put CPU2 into IDLE mode. (Using STANDBY will cause a duplicate WAKEINT on CPU2). CPU1 should verify this by checking the LPMSTAT register.
3. Set LPMCR.LPM to 10. Set GPIOLOPMSEL0 and GPIOLOPMSEL1 to connect the chosen GPIOs to the LPM module.
4. Set CLKSRCCTL1.WDHALTI to 1 to keep the CPU1 watchdog active and INTOSC1 and INTOSC2 powered up in HALT.
5. Set CLKSRCCTL1.WDHALTI to 0To disable the CPU1 watchdog and power down INTOSC1 and INTOSC2 in HALT.
6. Execute the IDLE instruction on CPU1 to enter HALT.

If an interrupt or NMI is received while the IDLE instruction is in the pipeline, the system will begin executing the WAKEINT ISR. After HALT wake-up, ISR execution will resume where it left off.

NOTE: Before entering HALT mode, if the system PLL is locked (SYSPLL.LOCKS = 1), it must also be connected to the system clock (PLLCTL1.PLLCLKEN = 1). Otherwise, the device will never wake up.

To wake up from HALT mode:

1. Drive the selected GPIO low for a minimum 5us. This will activate the CPU1.WAKEINT and CPU2.WAKEINT PIE interrupts.
2. Drive the wake-up GPIO high again to initiate the powering up of the SYSPLL and AUXPLL
3. Wait 16us plus 1024 OSCLK cycles to allow the PLLs to lock and the WAKEINT ISR to be latched.
4. Execute the WAKEINT ISR.

The device is now out of HALT mode and can resume normal execution.

1.10.4 HIB

HIB (short for ".hibernate") is a global low-power mode that gates the supply voltages to most of the system. This mode affects both CPU subsystems. HIB is essentially a controlled power-down with remote wakeup capability, and can be used to save power during long periods of inactivity. Because gating the supply voltage corrupts the state of the logic, a reset is required to exit HIB. To prevent external systems from being affected by the reset, HIB provides isolation of the IO pin states as well as low-power data retention via the M0 and M1 memories.

Unlike the clock-gating modes, HIB does not have a true wakeup. Instead, GPIO41 becomes HIBWAKEn, an asynchronous reset signal. When the boot ROM detects a HIB wakeup, it will avoid clearing M0 and M1 and call a user-specified IO restore function. (To prevent glitches on internal and external signals, XRSn will also generate a HIBWAKEn signal during HIB.) The IO restore function should set up the GPIO control registers to match their pre-HIB state, then write a 1 to LPMCR.IOISODIS to deactivate IO isolation. If the restore function does not disable isolation, the boot ROM will do it.

To enter HIB mode:

1. Save any necessary state to the M0 and M1 memories of both CPUs.
2. Put all IOs in the desired state for isolation and deactivate any analog modules in use.
3. Write the address of the IO restore function for each CPU to its IORESTOREADDR register.
4. Put CPU2 in reset, IDLE, or STANDBY.
5. Bypass the PLL by setting PLLCLKEN to 0.
6. Set CPU1s LPMCR.LPM to 11 and execute the IDLE instruction.

Any debugger connection will be lost on HIB entry since the JTAG logic is powered down.

Due to the loss of system state on HIB entry, it is possible for error information to be lost if an NMI is triggered while the IDLE instruction is in the pipeline. The ERRORSTS pin will be set and remain set until IO isolation is disabled, but there will be no way to tell what caused the error.

To wake the device from HIB mode:

1. Assert the dedicated GPIOHIBWAKEn pin (GPIO41) low to enable the power-up of the device clock sources.
2. Assert GPIOHIBWAKEn pin high again. This triggers the power-up of the rest of the device.
3. Boot-ROM code will execute on HIB wake-up. Boot-ROM will read CPU1.RESC.HIBRESTn bit to determine this is a wakeup from HIB.
4. Boot-ROM calls the IO context restore routine. This IO restore function should reconfigure the IO configuration and do any other necessary application setup.

Since waking up from HIB mode is a type of reset, the device will enter the main function. The device is now out of HIB mode and can normal execution.

Note: The BOOTROM uses locations 0x02 through 0x122 on CPU1's M0 RAM and locations 0x02-0x80 on CPU2's M0 RAM. To prevent losing any data during HIB wake-up, avoid saving any critical data to these locations.

Note: The application must bypass the PLL before executing the IDLE instruction to enter HIB. If the PLL is not bypassed when entering HIB, there will be a brief current spike on the Vdd supply that may cause the device to reset.

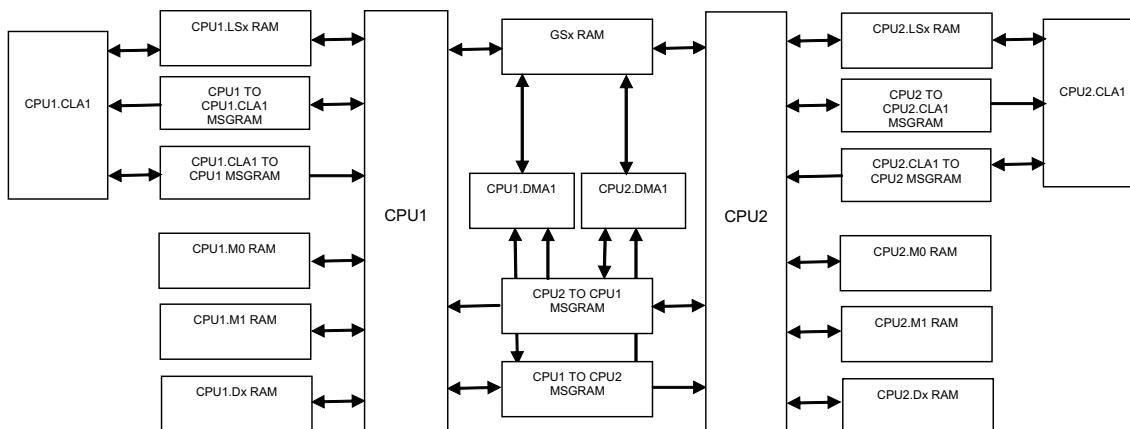
1.11 Memory Controller Module

For these devices, the RAMs have different characteristics. Some are:

- dedicated to each CPU (Dx RAMs),
- shared between CPU and its own CLA (LSx RAM),
- shared between CPU and DMA of both subsystems (GSx RAM), and
- used to send/receive message between processors (MSGRAM).

All these RAMs are highly configurable to achieve control for write access and fetch access from different masters. There are also RAMs - called IPC MSGRAMs - that are used for interprocessor communication. All dedicated RAMs are enabled with the ECC feature (both data and addr) and shared RAMs, as well as IPC MSGRAMs, are enabled with the PARITY (both data and addr) feature. Some of the dedicated memories are secure memory as well. Refer to the Security section of the *System Control and Interrupts* chapter for more details. Each RAM has its own controller which takes care of the access protection/security related checks and ECC/Parity features for that RAM. [Figure 1-20](#) shows the configuration of these RAMs.

Figure 1-20. Memory Architecture



NOTE: All RAMs on these devices are SRAMs.

1.11.1 Functional Description

This section further defines and discusses the dedicated RAMs, shared RAMs, and MSG RAMs on this device.

1.11.1.1 Dedicated RAM (Dx RAM)

Each CPU subsystem has four dedicated RAM blocks: M0, M1, D0, and D1. M0/M1 memories are small blocks of memory which are tightly coupled with the CPU. Only the CPU has access to these memories. No other masters (including DMA) have any access to these memories.

All dedicated RAMs have the ECC feature. All dedicated memories (except for M0/M1) are secure memory and also have the access protection (CPU write protection/CPU fetch protection) feature. Each type of access protection for each RAM block can be enabled/disabled by configuring the specific bit in the access protection register, allocated to each subsystem (DxACCPROT).

1.11.1.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs). On these devices, all such memories are secure memory and have the parity feature. By default these memories are dedicated to the CPU only, and the user could choose to share these memories with the CLA by appropriately configuring the MSEL_LSx bit field in the LSxMSEL register. Further, when these memories are shared between the CPU and CLA, the user could choose to use these memories as CLA program memory by configuring the CLAPGM_LSx bit field in the LSxCLAPGM registers. CPU access to all memory blocks which are programmed as CLA program memory are blocked.

All these RAMs have the access protection (CPU write/CPU fetch) feature. Each type of access protection for each RAM block can be enabled/disabled by configuring the specific bit in the local shared RAM access protection registers, mapped to each CPU subsystem.

Table 1-12. Local Shared RAM

MSEL_LSx	CLAPGM_LSx	CPUx Allowed Access	CPUx.CLA1 Allowed Access	Comment
00	X	All	-	LSx memory is configured as CPU dedicated RAM
01	0	All	Data Read Data Write	LSx memory is shared between CPU and CLA1
01	1	Emulation Read Emulation Write	Fetch Only	LSx memory is CLA1 program memory

1.11.1.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and their respective DMA are called global shared RAMs (GSx RAMs). Each shared RAM can be owned by either CPU subsystem based on the configuration of respective bits (one bit for each LSx memory) in the GSxMSEL register. When a particular GSx RAM block is owned by the CPU1 subsystem, CPU1 and CPU1.DMA1 have full access to that RAM block, whereas CPU2 and CPU2.DMA1 have only read access to it (no fetch/write access). Similarly, when a particular GSx RAM block is owned by the CPU2 subsystem, CPU1 and CPU1.DMA1 will have only read access (no fetch/write access) to that RAM block, whereas CPU2 and CPU2.DMA1 will have full access to it.

Table 1-13. Global Shared RAM

GSxMSEL	CPU1	CPU1	CPU1	CPU1.DMA1	CPU1.DMA1	CPU2	CPU2	CPU2	CPU2.DMA1	CPU2.DMA1
	Fetch	Read	Write	Read	Write	Fetch	Read	Write	Read	Write

Table 1-13. Global Shared RAM (continued)

GSxMSE L	CPU1	CPU1	CPU1	CPU1.DM A1	CPU1.DM A1	CPU2	CPU2	CPU2	CPU2.DM A1	CPU2.DM A1
0	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	No
1	No	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes

Like other shared RAM, these RAMs also have different levels of access protection which can be enabled or disabled by configuring specific bits in the GSxACCPROT registers mapped in each subsystem.

Master select and access protection configuration for each GSx RAM block can be individually locked by the user to prevent further update to these bit fields unless unlocked. The user can also choose to permanently lock the configuration to individual bit fields by setting the specific bit fields in the GSxCOMMIT register (refer to the register description for more details). Once configuration is committed for a particular GSx RAM block, it can not be changed further until CPUx.SYSRS is issued. Only the CPU1 SW can change the master select configuration by writing into the GSxMSEL register, mapped on the CPU1. The GSxMSEL register, which is mapped to the CPU2 subsystem, is a status register which can only be used by CPU2 SW to know the master ownership for each GSx RAM block.

1.11.1.4 Message RAM (MSG RAM)

Message RAMs are small RAMs used to share information between the CPU and CLA of the same subsystem or CPU1 and CPU2. There are four such memory blocks in this device. Since these RAMs are used for interprocessor communication, they are also called IPC RAMs. The message RAMs between the two CPUs will have CPU/DMA read/write access from one subsystem, and CPU/DMA read-only access from the other subsystem. Similarly for message RAMs between the CPU and CLA of the same subsystem, one CPU or CLA will have read/write access, whereas the other one will have only read access.

1.11.1.5 Access Arbitration

For a shared RAM, multiple accesses can happen at a given time. The maximum number of accesses to any shared RAM at any given time depends on the type of shared RAM. On this device, a combination of a fixed and round robin scheme is followed to arbitrate multiple access at any given time. Accesses from the same masters are arbitrated in a fixed priority manner, but the accesses from different masters are arbitrated using the round robin scheme.

The following is the order of fixed priority for CPU accesses:

1. Data Write/Program Write
2. Data Read
3. Program Read/Program Fetch

Following is the order of fixed priority for CLA accesses:

1. Data Write
2. Data Read/Program Fetch

Figure 1-21 represents the arbitration scheme on global shared memories:

Figure 1-21. Arbitration Scheme on Global Shared Memories

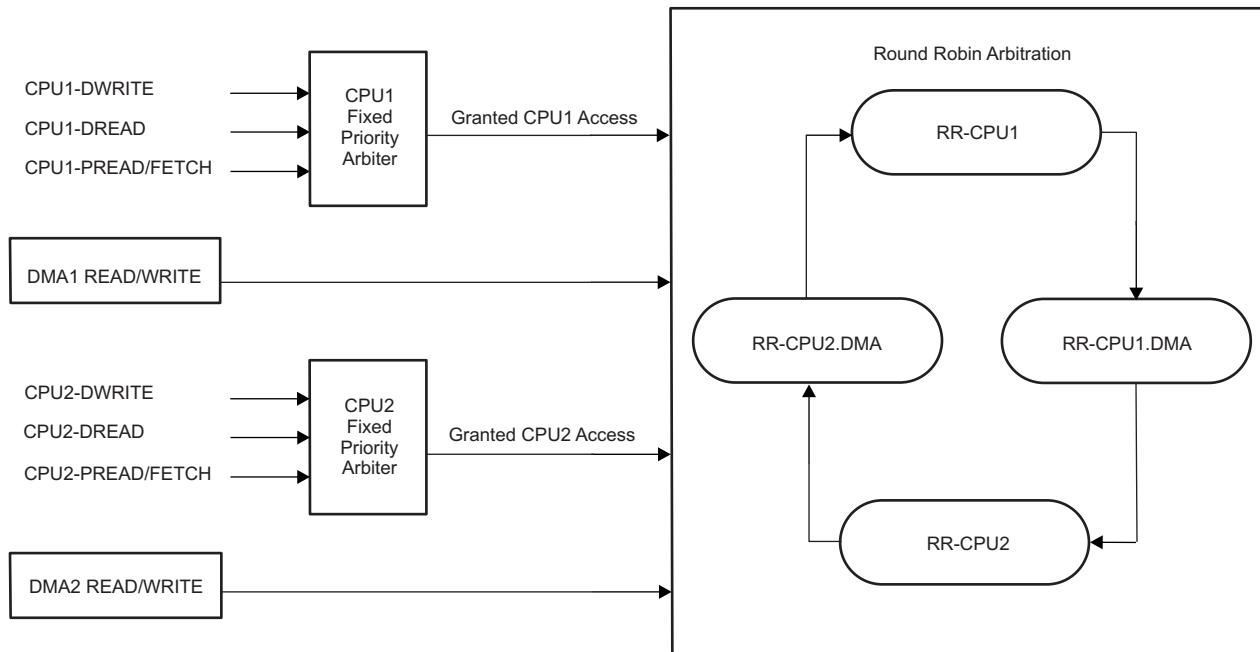
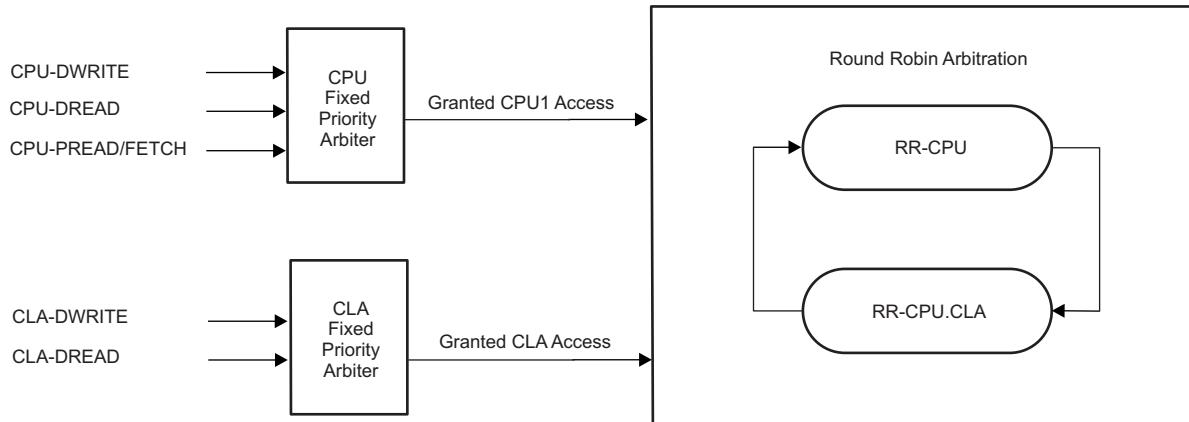


Figure 1-22 represents arbitration scheme on local shared memories.

Figure 1-22. Arbitration Scheme on Local Shared Memories



1.11.1.6 Access Protection

All RAM blocks except for M0/M1 on both subsystems have different levels of protection. This feature allows the user to enable or disable specific access to individual RAM blocks from individual masters. There is no protection for RD accesses, hence RDs are always allowed from all the masters which have access to that RAM block.

The following sections describe the different kinds of protection available for RAM blocks on this device.

Note: For debug accesses, all the protections are disabled.

1.11.1.6.1 CPU Fetch Protection

A CPU has execution permission from a memory, only if that memory is dedicated to that CPU or its respective subsystem is master for that memory (in case of GSx memory). When fetch accesses are allowed based on the mastership, it can be further protected by setting the FETCHPROTx bit of the specific register to '1'. If fetch access is done by the CPU to a memory where CPU fetch protection is enabled, a fetch protection violation occurs.

There are two types of fetch protection violations:

- Non-master CPU fetch protection violation
- Master CPU fetch protection violation

If a fetch access is made to a memory by a non-master CPU, it is called a non-master fetch protection violation. If a fetch access is made to a dedicated or shared memory by master CPU, and FETCHPROTx is set to '1' for that memory, the violation is called a master CPU fetch protection violation.

If a fetch protection violation occurs, it results in an ITRAP for CPU. A flag gets set into the appropriate access violation flag register, and the memory address for which the access violation occurred, get latched into the appropriate CPU fetch access violation address register.

1.11.1.6.2 CPU Write Protection

A CPU has write permission to a memory only if that memory is dedicated to that CPU, or if its respective subsystem is the master for that memory (in case of GSx memory). When write accesses are allowed based on the mastership, it can be further protected by setting the CPUWRPROTx bit of the specific register to '1'. If write access is done by CPU to memory where it is protected, a write protection violation occurs.

There are two types of CPU write protection violations:

- Non-master CPU write protection violation
- Master CPU write protection violation

If a write access is made to a dedicated or shared memory by the master CPU and CPUWRPROTx is set to '1' for that memory, it's called a master CPU write protection violation.

If a write protection violation occurs, write gets ignored, a flag gets set into the appropriate access violation flag register, and the memory address for which the access violation occurred, gets latched into the appropriate CPU write access violation address register. Also, access violation interrupt is generated if enabled in the interrupt enable register.

1.11.1.6.3 CPU Read Protection

For local shared RAM, if memory is shared between the CPU and its CLA, the CPU will only have access if the memory is configured as Data RAM for CLA. If it is programmed as program RAM, all the access from the CPU, including READ, will be blocked and the violation will be considered as non-master access violation.

If a read protection violation occur, a flag gets set into the appropriate access violation flag register, and the memory address for which the access violation occurred, gets latched into the appropriate CPU read access violation address register. Also, access violation interrupt is generated, if enabled in the interrupt enable register.

1.11.1.6.4 CLA Fetch Protection

If local shared RAM is configured as dedicated RAM for the CPU, or if it is configured as DATA RAM for the CLA, any fetch access from CLA to that particular LSx RAM results in a CLA fetch protection violation which is a non-master access violation.

If a CLA fetch protection violation occurs, it results in a MSTOP, a flag gets set into the appropriate access violation flag register, and the memory address for which the access violation occurred, gets latched into the appropriate CLA fetch access violation address register. Also, access violation interrupt is generated to the master CPU if enabled in the interrupt enable register.

1.11.1.6.5 CLA Write Protection

If local shared RAM is configured as dedicated RAM for the CPU, or if it is configured as program RAM for the CLA, any data write access from the CLA to that particular LSx RAM results in a CLA write protection violation which is a non-master access violation.

If a CLA write protection violation occurs, write gets ignored, a flag gets set into the appropriate access violation flag register, and the memory address for which the access violation occurred, gets latched into the appropriate CLA write access violation address register. Also, access violation interrupt is generated to the master CPU if enabled in the interrupt enable register.

1.11.1.6.6 CLA Read Protection

If local shared RAM is configured as dedicated RAM for the CPU, or if it is configured as program RAM for the CLA, any data read access from the CLA to that particular LSx RAM results in a CLA read protection violation which is a non-master access violation.

If a CLA read protection violation occurs, a flag gets set into the appropriate access violation flag register, and the memory address for which the access violation occurred, gets latched into the appropriate CLA read access violation address register. Also, access violation interrupt is generated to the master CPU if enabled in the interrupt enable register.

1.11.1.6.7 DMA Write Protection

The CPU1 or CPU2 DMA has write permission to a GSx memory only if its respective subsystem is master for that memory. When write accesses from a DMA are allowed based on the mastership, it can be further protected by setting the DMAWRPROTx bit of specific register to '1'. If write access is done by DMA to protected memory, a write protection violation occurs.

There are two types of DMA write protection violations

- Non-master DMA write protection violation (only applicable to Sx memories)
- Master DMA write protection violation

If a write access is made to Sx memory by a non-master DMA, it is called a non-master write protection violation. If a write access is made to a dedicated or shared memory by master DMA, and DMAWRPROTx is set to '1' for that memory, it is called a master DMA write protection violation.

If a write protection violation occurs on CPU1, write is ignored and a dmaerr interrupt gets generated, whereas in case of CPU2, write is ignored and an access violation interrupt is generated if enabled in the interrupt enable register. A flag gets set into the dma access violation flag register, and the memory address where the violation happened gets latched into the dma fetch access violation address register. These are dedicated registers for each subsystem.

Note 1: All access protections are ignored during debug accesses. Writes access to a protected memory will go through when it is done via the debugger, irrespective of the write protection configuration for that memory.

Note 2: Access protection is not implemented for M0 and M1 memories.

Note 3: In case of local shared RAM, if memory is shared between the CPU and its CLA, the CPU will only have access if the memory is configured as Data RAM for CLA. If it is programmed as program RAM, all the access from the CPU (including RD) and Data access from the CLA will be blocked, and violation will be considered as a non-master access violation. If the memory is configured as dedicated to the CPU, all access from the CLA will be blocked and the violation will be considered a non-master access violation.

1.11.1.7 Memory Error Detection, Correction and Error Handling

These devices have memory error detection and correction features to satisfy safety standards requirements. These requirements warrant the addition of detection mechanisms for finite dangerous failures.

In this device, all dedicated RAMs support error correction code (ECC) protection and the shared RAMs have parity protection. The ECC scheme used is Single Error Correction Double Error Detection (SECDED). The parity scheme used is even parity. ECC/Parity will cover the data bits stored in memory as well as address.

ECC/Parity calculation is done inside the memory controller module and then calculated. ECC/parity is written into the memory along with the data. ECC/Parity is computed for 16-bit data; hence, for each 32-bit data, there will be three 7-bit ECC codes (or 3-bit parity), two of which are for data and a third one for the address.

1.11.1.7.1 Error Detection and Correction

Error detection is done while reading the data from memory. The error detection is performed for data as well as address. For parity memory, only a single-bit error gets detected whereas, in case of ECC memory, along with a single-bit error, a double-bit error also gets detected. These errors are called correctable error and uncorrectable errors. The following are characteristics of these errors:

- Parity errors are always uncorrectable errors
- Single-bit ECC errors are correctable errors
- Double-bit ECC errors are uncorrectable errors
- Address ECC errors are also uncorrectable errors

Correctable errors get corrected by the memory controller module and then correct data is given back as read data to master and also written back into the memory to prevent double-bit error due to another single-bit error at same memory address

1.11.1.7.2 Error Handling

For each correctable error, the count in the correctable error count register will increment by one. When the value in this count register becomes equal to the value configured into the correctable error threshold register, an interrupt is generated to the respective CPU, if the interrupt is enabled in the correctable interrupt enable register. The user needs to configure the correctable error threshold register based on the system requirements. Also, the address for which the error occurred, gets latched into the master specific status register and a flag gets set. Each of these registers are dedicated for each CPU subsystem.

If there are uncorrectable errors, an NMI gets generated for the respective CPU. In this case, the address for which error occurred, also gets latched into the master-specific address status register, and a flag gets set.

Table 1-14 summarizes different error situations that can arise. These need to be handled appropriately in the software, using the status and interrupt indications provided.

Table 1-14. Error Handling in Different Scenarios

Access Type	Error Found In	Error Type	Status Indication	Error Notification
Reads	Data read from memory	Uncorrectable Error (Single-bit error for Parity RAMs OR Double bit Error for ECC RAMs)	Yes - CPUx/CPUx.DMA1/CPU x.CLA1 CPU/DMA/CLA Read Error Address Register Data returned to CPUx/CPUx.DMA1/CPU x.CLA1 is incorrect	NMI for CPUx access NMI for CPUx.DMA1 access NMI to CPU for CPUx.CLA1 access
Reads	Data read from memory	Single-bit error for ECC RAMs	Yes - CPUx/CPUx.DMA1 CPU/DMA Read Error Address Register Increment single error counter	Interrupt when error counter reaches the user programmable threshold for single errors

Table 1-14. Error Handling in Different Scenarios (continued)

Access Type	Error Found In	Error Type	Status Indication	Error Notification
Reads	Address	Address error	Yes - CPUx/CPUx.DMA1/CPU x.CLA1 CPU/DMA/CLA Read Address Error Register Data returned to CPUx/CPUx.DMA1/CPU x.CLA1 is incorrect	NMI to CPU for CPUx access NMI to CPU for CPUx.DMA1 access NMI to CPU for CPUx.CLA1 access

Notes: In case of uncorrectable error during fetch on the CPU, there is the possibility of getting ITRAP before NMI, since garbage instructions enter into the CPU pipeline before NMI gets generated. During debug accesses, correctable as well as uncorrectable errors are masked.

1.11.1.8 Application Test Hooks for Error Detection and Correction

Since error detection and correction logic is part of safety critical logic, safety applications may need to ensure that the logic is working fine always (during run time also). To enable this, a test mode is provided in which a user can modify the data bits (without modifying the ECC/Parity bits) or ECC/Parity bits directly. Using this feature, an ECC/parity error could be injected into data.

Notes: The memory map for ECC/parity bits and data bits are the same. The user must choose a different test mode to access ECC/Parity bits.

In test mode, all access to memories (data as well as ECC/parity) should be done as 32-bit access only.

The following table shows the bit mapping for the ECC/parity bits when they are read in RAMTEST mode using their respective addresses.

Table 1-15. Mapping of ECC Bits in Read Data from ECC/Parity Address Map

Data Bits Location in Read Data	Content (ECC Memory)
6:0	ECC Code for lower 16 bits of data
7	Not Used
14:8	ECC Code for upper 16 bits of data
15	Not Used
22:16	ECC Code for address
31:23	Not Used

Table 1-16. Mapping of Parity Bits in Read Data from ECC/Parity Address Map

Data Bits Location in Read Data	Content (Parity Memory)
0	Parity for lower 16 bits of data
7:1	Not Used
8	Parity for upper 16 bits of data
15:9	Not Used
16	Parity for address
31:17	Not Used

1.11.1.9 RAM Initialization

To ensure that read/fetch from uninitialized RAM locations do not cause ECC or parity errors, the RAM_INIT feature is provided for each memory block. Using this feature, any RAM block can be initialized with 0x0 data and respective ECC/parity bits accordingly. This can be initiated by setting the INIT bit to '1' for the specific RAM block in INIT registers. To check the status of RAM initialization, SW should poll for the INITDONE bit for that RAM block in the INITDONE register to be set. Unless this bit gets set, no access should be made to that RAM memory block.

In case of GSx memory, the CPU of the subsystem, which is configured as the master for a particular GSx RAM block, can only initiate the RAM initialization.

NOTE: None of the masters should access the memory while initialization is taking place. If memory is accessed before RAMINITDONE is set, the memory read/write as well as initialization will not happen correctly.

1.12 Flash Controller Memory Module

Flash is an electrically erasable/programmable nonvolatile memory. Flash can be electrically programmed and erased many times to ease code development. Flash memory can be used primarily as a program memory for the core, and secondarily as static data memory.

This section describes the proper sequence to configure the wait states and operating mode of flash. It also includes information on flash and OTP power modes, how to improve flash performance by enabling the flash prefetch/cache mode, and the SECDED safety feature.

1.12.1 Features

Features of flash memory include:

- Dedicated flash bank in the CPU1 subsystem (refer to the device data manual for the size of flash bank)
- Dedicated flash bank in the CPU2 subsystem (refer to the device data manual for the size of flash bank)
- Dedicated flash module controller (FMC) in CPU1 and CPU2 subsystems
- Multiple sectors providing the option of leaving some sectors programmed and only erasing specific sectors
- User-programmable OTP locations for configuring security, OTP Boot mode and boot pins (if user doesn't like factory default boot mode pins)
- Single-flash pump shared by the CPU1 subsystem and CPU2 subsystem
- Hardware flash pump semaphore to control ownership of the pump between the two subsystems
- Enhanced performance using code-prefetch mechanism and data cache in CPU1-FMC and CPU2-FMC
- Configurable wait states to give the best performance for a given execution speed
- Safety Features
 - SECDED-single error correction and double error detection is supported in both FMCs
 - Address bits are included in ECC
 - Test mode to check the health of ECC logic
- Supports low-power modes for flash bank and pump for power savings
- Built-in power mode control logic
- Integrated program/erase state machine (FSM) in both FMCs
 - Simple flash API algorithms
 - Fast erase and program times (refer to the device data manual for details)
- Code Security Module to prevent access to the flash by unauthorized persons (refer to [Section 1.13](#) for details)

1.12.2 Flash Tools

Texas Instruments provides the following tools for flash:

- Code Composer Studio V5.5 - the development environment with integrated flash plugin
- F021 Flash API Library - a set of software peripheral functions to erase/program flash
Please refer to the *Flash Application Programming Interface User's Specification* for more information.
- UniFlash - tool to erase/program/verify the flash content through JTAG
- Linker ECC generation - to generate the Flash ECC from the Flash data and to introduce errors in Flash/ECC space. Please refer to the *TMS320C28x Assembly Language Tools User's Guide* for more information.

1.12.3 Default Flash Configuration

The following are flash module configuration settings at power-up, in both CPU1 and CPU2 subsystems:

- Dedicated flash banks are in sleep power mode
- Shared pump is in sleep mode
- ECC is enabled
- Wait-states are set to max (0xF)
- Code-prefetch mechanism and data cache are disabled in both FMCs

Note that during the boot process, the Boot ROM performs a dummy read of the Code Security Module (CSM) password locations located in the OTP. This read is performed to unlock a new or erased device that has no password stored in it, so that flash programming or loading of code into CSM protected SRAM can be performed. On devices with a password stored, this read has no effect and the CSM remains locked. One effect of this read is that the flash will transition from the sleep (reset) state to the active state.

User application software must initialize wait-states using the FRDCNTL register, and configure cache/prefetch features using the RD_INTF_CTRL register, to achieve optimum system performance. Software that configures flash settings like wait-states, cache/prefetch features, and so on, must be executed only from RAM memory, **not** from flash memory.

Note: Before initializing wait-states, cache/prefetch mechanisms must **always** be disabled, if they are enabled. After the initialization of wait-states is done, cache/prefetch mechanisms can be enabled as needed.

1.12.4 Flash Bank, OTP and Pump

There is a dedicated flash bank in the CPU1 subsystem called the CPU1 flash bank and a dedicated flash bank in the CPU2 subsystem called the CPU2 flash bank. Also, there is a one-time programmable (OTP) memory on the CPU1 subsystem called USER OTP which the user can program only once and cannot erase. Flash and OTP are uniformly mapped in both program and data memory space.

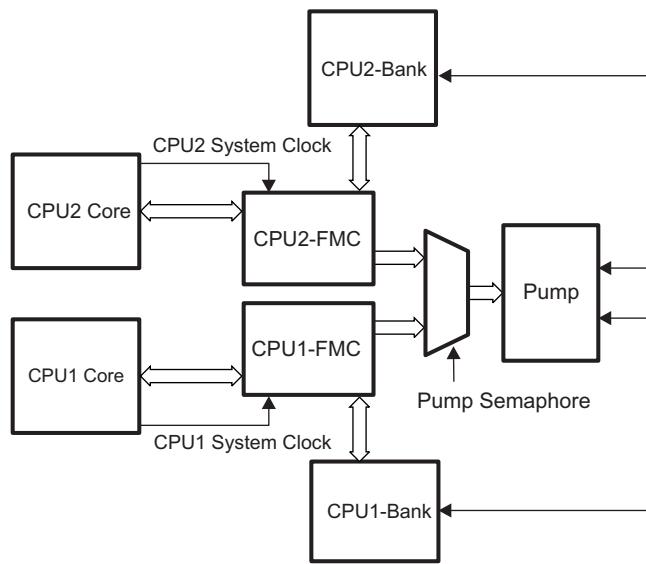
Both the CPU1 subsystem and CPU2 subsystem have a TI-OTP which contains manufacturing information like settings used by the flash state machine for erase and program operations, and so on. Users may read TI-OTP but cannot program or erase. For memory map and size information of the CPU1-Bank, CPU1 TI-OTP, CPU1 USER OTP, CPU2 flash bank, CPU2 TI-OTP, CPU2 USER-OTP and corresponding ECC locations, please refer to the device data manual.

The CPU1 flash bank/User OTP and CPU2 flash bank/USER OTP share a common flash pump. A hardware semaphore, called the flash pump semaphore, is provided to control the access of the flash pump between the CPU1 subsystem and CPU2 subsystem.

Figure 1-27 depicts the user-programmable OTP locations in CPU1 USER-OTP and CPU2 USER-OTP. For more information on the functionality of these fields, please refer to [Dual Code Security Module](#) and the [ROM Code and Peripheral Booting](#) chapter.

1.12.5 Flash Module Controller (FMC)

There is a dedicated flash module controller in both the CPU1 subsystem (CPU1-FMC) and the CPU2 subsystem (CPU2-FMC). The CPU1 in the CPU1 subsystem interfaces with the CPU1 flash module controller (CPU1-FMC), which in turn, interfaces with the CPU1 flash bank and shared pump to perform erase/program operations as well as to read data/execute code from the CPU1 flash bank.

Figure 1-23. FMC Interface with Core, Bank and Pump

The CPU2 in the CPU2 subsystem interfaces with the CPU2 flash module controller (CPU2-FMC) which in turn, interfaces with the CPU2 flash bank and shared pump to perform erase/program operations as well as to read data/execute code from the CPU2 flash bank. Control signals to the flash pump will be controlled by either CPU2-FMC or CPU1-FMC, depending on who gains the flash pump semaphore.

There is a state machine in both CPU1-FMC and CPU2-FMC which generates the erase/program sequences in hardware. This simplifies the Flash API software (refer to the *F021 Application Programming Interface Users Specification* for details on Flash API) which configures control registers in FMC to perform flash erase and program operations.

The following sections ([Section 1.12.6](#), [Section 1.12.7](#), [Section 1.12.8](#), [Section 1.12.9](#), and [Section 1.12.10](#)) will describe FMC in detail.

1.12.6 Flash and OTP Automatic Power-Down Modes

Flash bank and pump consume a significant amount of power when active. The flash module provides a mechanism to automatically power-down flash banks after they have not been accessed for some user programmable time. Special timers automatically sequence the power-up and power-down of the CPU1 flash bank and CPU2 flash bank independently of each other. The shared charge pump module has its own independent power up/down timers as well.

1.12.6.1 Flash/OTP and Pump Power Modes and Wakeup

Flash bank and OTP (CPU1/CPU2) operate in three power modes: Sleep (lowest power), Standby, and Active (highest power)

- Sleep State

This is the state after a device reset. In this state, the bank is in a sleep state (lowest power). When the flash bank is in the sleep state, a CPU data read or opcode fetch to the flash or OTP memory map area will automatically initiate a change in power modes to the standby state and then to the active state. During this transition time to the active state, the CPU will automatically be stalled.

- Standby State

In this state, the bank is in standby power mode state. This state uses more power than the sleep state, but takes a shorter time to transition to the active or read state. When the flash is in the standby state, a CPU data read or opcode fetch to the flash or OTP memory map area will automatically initiate a change in power modes to the active state. During this transition time to the active state, the CPU will automatically be stalled. Once the flash/OTP has reached the active state, the CPU access will complete as normal.

- Active or Read State

In this state, the bank and pump are in active power mode state (highest power)

Charge pump operates in two power modes:

- Sleep (lowest power)
- Active (highest power)

Any access to a flash bank/OTP causes the charge pump to go into active mode if it is not in sleep mode. Also, any erase or program command causes the charge pump and bank to become active. Also, if any bank is active or in standby mode, the charge pump is active, independent of the charge pump fallback power mode. While pump is in sleep state, a charge pump sleep down counter holds a user configurable value (PSLEEP bit field in FPAC1 register) and when the charge pump exits sleep power mode, the down counter delays from 0 to PSLEEP prescaled SYSCLK clock cycles before putting the charge pump into active power mode. Refer to the Flash registers for more details.

1.12.6.2 Active Grace Period

The active grace period (AGP) can be used to optimize the flash module power consumption versus access time. Faster access times are associated with higher-power modes of operation. At one extreme, the power control logic could attempt to reduce power consumption by putting the banks and charge pump into a low-power mode immediately at the end of every flash access. However, if accesses are only a few cycles apart, this can actually increase power consumption versus leaving the flash powered, because the banks and charge pump consume more power during flash startup and access.

The active grace periods (supported for CPU1 flash bank and CPU2 flash bank independently in addition to the charge pump module) allow the banks and/or charge pump to be maintained in active mode for a specified period following an access. This is done in anticipation of another read within the AGP time, to allow the subsequent read to have a faster access and spend less time dissipating power, than if the bank went into one of the low power modes immediately. If the next access does not occur within the AGP time, the power control logic can automatically put the bank and/or charge pump into a low-power mode to reduce power consumption during long periods of inactivity.

The AGP value is programmed by a set of programmable counters (FBAC and FPAC2) which keep the flash bank or charge pump in active mode until the counter expires, at which time the bank or charge pump reverts to its fallback power mode as defined in the FBFALLBACK and FPAC1 registers. The application software can program the fallback power mode to be standby or sleep mode to reduce power consumption, or program it to be active mode to keep the bank active regardless of counter settings (default). The charge pump AGP counter remains in its initialized state when any one of the banks is active, including the AGP counter of the bank. The charge pump AGP counter begins counting when both banks have become inactive.

As the charge pump is shared between CPU1-FMC and CPU2-FMC, the effective PAGP value and PMPPWR value used when powering down the pump will be of the FMC (out of CPU1-FMC and CPU2-FMC) which owns the pump. As the pump is shared between both CPU1 and CPU2-Banks, if an access is made either to the CPU1-Bank or CPU2-Bank, the value of PMPPWR bit in both CPU1-FMC and CPU2-FMC changes to 1 (active). The application software can also check the current power mode of flash bank and charge pump by reading the FBPRDY register. See register descriptions for detailed information.

1.12.7 Flash and OTP Performance

Once flash bank and pump are in the active power state, then a read or fetch access to the bank memory map area can be classified as a flash access (access to an address location in flash) or an OTP access (access to an address location in OTP). Once CPU throws an access to a Flash memory address, data is returned after RWAIT+1 number of SYSCLK cycles. For a USER-OTP access, data is returned after 11 SYSCLK cycles.

RWAIT defines the number of random access wait states and is configurable using the RWAIT bit-field in FRDCNTL register. At reset the RWAIT has the reset value of fifteen wait states. The RWAIT bit-field value defaults to a worst-case wait state count (15) and, thus, needs to be initialized for the appropriate number of wait states to improve performance based on the CPU clock rate and the access time of the flash. The flash supports 1-wait accesses when the RWAIT bits are set to zero. This assumes that the CPU speed is low enough to accommodate the access time.

For a given system clock frequency, RWAIT has to be configured using below formula:

$$\text{RWAIT} = (\text{SYSCLK/FCLK})-1$$

where

SYSCLK is the system operating frequency

FCLK is flash clock frequency. FCLK should be \leq FCLKmax, allowed maximum flash clock frequency with one wait state.

If RWAIT results in a fractional value when calculated using the above formula, RWAIT has to be rounded up to the nearest integer.

NOTE: Flash characterization is pending for these devices; therefore, the allowed maximum flash clock frequency with one wait state (FCLK max) is not given in the device data manual. However from design simulations, FCLK max can be given as 50MHz. This value will be updated later in the data manual when Flash characterization is complete.

1.12.8 Flash Read Interface

This section provides details about the data read modes to access flash bank/OTP and the configuration registers which control the read interface. In addition to a standard read mode, FMC's have built-in prefetch and cache mechanisms to allow increased clock speeds and CPU throughput wherever applicable.

1.12.8.1 FMC Flash Read Interface

1.12.8.1.1 Standard Read Mode

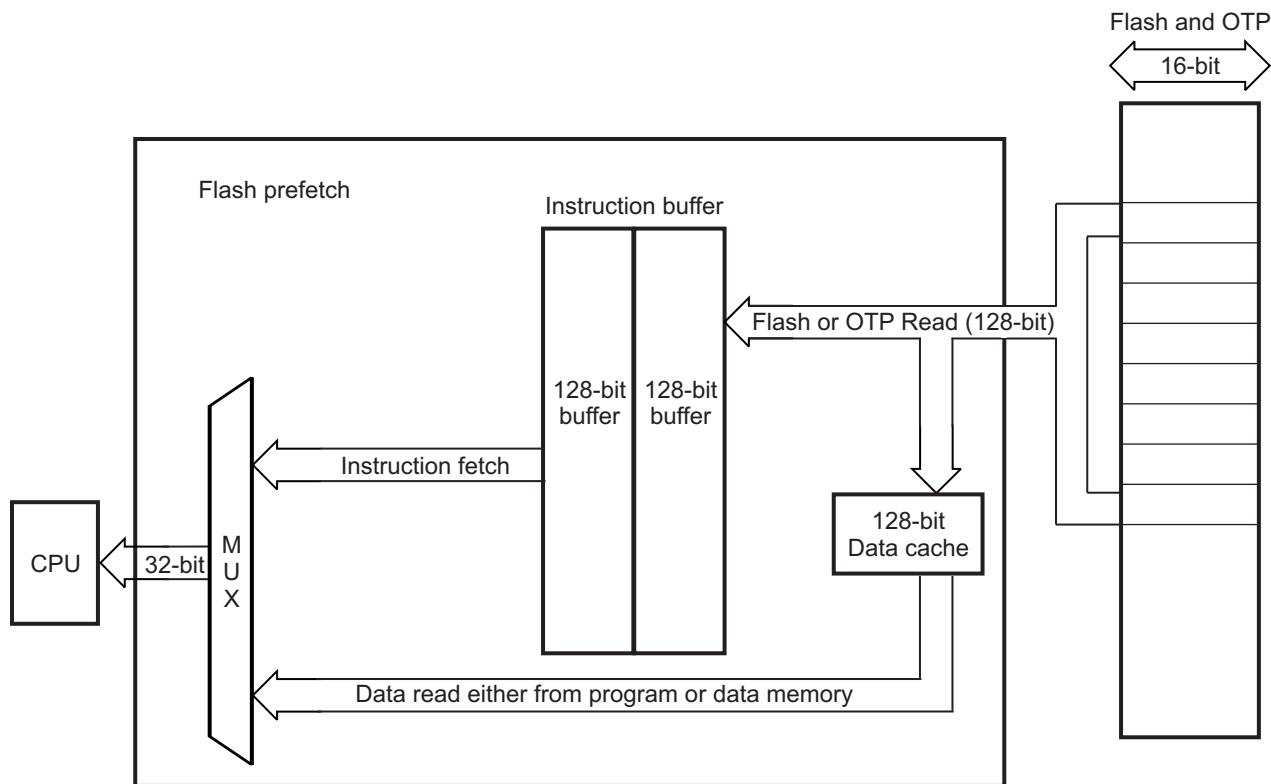
Standard read mode is defined as the read mode in effect when code prefetch-mechanism and data cache are disabled. It is also the default read mode after reset. During this mode, each read access to flash is decoded by the flash wrapper to fetch the data from the addressed location and the data is returned after the RWAIT+1 number of cycles.

Prefetch buffers associated with prefetch mechanism and data cache are bypassed in standard read mode; therefore, every access to the flash/OTP is used by the CPU immediately and every access creates a unique flash bank access.

Standard read mode is the recommended mode for lower system frequency operation in which RWAIT can be set to zero to provide single-cycle access operation. FMC can operate at higher frequencies using standard read mode at the expense of adding wait states. At higher system frequencies, it is recommended to enable cache and prefetch mechanisms to improve performance. Refer to device specific data manual to determine maximum flash frequency allowed in standard read mode (that is, maximum flash clock frequency with one wait state - FCLKmax).

1.12.8.1.2 Prefetch Mode

Flash memory is typically used to store application code. During code execution, instructions are fetched from sequential memory addresses, except when a discontinuity occurs. Usually the portion of the code that resides in sequential addresses makes up the majority of the application code and is referred to as linear code. To improve the performance of linear code execution, a flash prefetch-mechanism has been implemented in FMC. [Figure 1-24](#) illustrates how this mode functions.

Figure 1-24. Flash Prefetch Mode

This prefetch mechanism does a look-ahead prefetch on linear address increments starting from the address of the last instruction fetch. The flash prefetch mechanism is disabled by default. Setting the PREFETCH_EN bit in the FRD_INTF_CTRL register enables this prefetch mode.

An instruction fetch from the flash or OTP reads out 128 bits per access. The starting address of the access from flash is automatically aligned to a 128-bit boundary, such that the instruction location is within the 128 bits to be fetched. With flash prefetch mode enabled, the 128 bits read from the instruction fetch are stored in a 128-bit wide by 2-level deep instruction prefetch buffer. The contents of this prefetch buffer are then sent to the CPU for processing as required.

Up to four 32-bit instructions or up to eight 16-bit instructions can reside within a single 128-bit access. The majority of C28x instructions are 16 bits, so for every 128-bit instruction fetch from the flash bank, it is likely that there are up to eight instructions in the prefetch buffer ready to process through the CPU. During the time it takes to process these instructions, the flash prefetch mechanism automatically initiates another access to the flash bank to prefetch the next 128 bits. In this manner, the flash prefetch mechanism works in the background to keep the instruction prefetch buffers as full as possible. Using this technique, the overall efficiency of sequential code execution from flash or OTP is improved significantly. If the prefetch mechanism is enabled, then the last row of 128-bits in the bank should not be used, because the prefetch logic which does a look-ahead prefetch, will try to fetch from outside the bank and would result in ECC error.

The flash prefetch is aborted only on a PC discontinuity caused by executing an instruction such as a branch, BANZ, call, or loop. When this occurs, the prefetch is aborted and the contents of the prefetch buffer are flushed. There are two possible scenarios when this occurs: 1. If the destination address is within the flash

1. If the destination address is within the flash or OTP, the prefetch aborts and then resumes at the destination address.

2. If the destination address is outside of the flash and OTP, the prefetch is aborted and begins again only when a branch is made back into the flash or OTP. The flash prefetch mechanism only applies to instruction fetches from program space. Data reads from data memory and from program memory do not utilize the prefetch buffer capability and thus bypass the prefetch buffer. For example, instructions such as MAC, DMAC, and PREAD read a data value from program memory. When this read happens, the prefetch buffer is bypassed but the buffer is not flushed. If an instruction prefetch is already in progress when a data read operation is initiated, then the data read will be stalled until the prefetch completes.

1.12.8.1.2.1 Data Cache

Along with the prefetch mechanism, a data cache of 128 bits width is also implemented to improve data space read and program space read performance. This data cache will not be filled by the prefetch mechanism. When any kind of data-space read or program-space read is made by the CPU from an address in the bank, and if the data corresponding to the requested address is not in the data cache, then 128 bits of data will be read from the bank and is loaded in the data cache. This data is eventually sent to the CPU for processing. The starting address of the access from flash is automatically aligned to a 128-bit boundary such that the requested address location is within the 128 bits to be read from the bank. By default, this data cache is disabled and can be enabled by setting DATA_CACHE_EN bit in the FRD_INTF_CTRL register.

Some other points to keep in mind when working with flash/USER OTP::

- Reads of the USER OTP locations are hardwired for 10 wait states. The RWAIT bits have no effect on these locations.
- CPU writes to the flash or OTP memory map areas are ignored. They complete in a single cycle.
- If a security zone is in the locked state and the respective password lock bits are not all 1s, then,
 - Data reads to Zx-CSMPSWD, Zx-ECSLPSWD will return 0
 - Program space reads to Zx-CSMPSWD, Zx-ECSLPSWD will return 0
 - Program fetches to Zx-CSMPSWD, Zx-ECSLPSWD will return 0
 - .
- When the Code Security Module (CSM) is secured, reads to the flash/OTP memory map area from outside the secure zone take the same number of cycles as a normal access. However, the read operation returns a zero.
- The arbitration scheme in FMC prioritizes CPU accesses in the fixed priority order of data read (highest priority), program space read and program fetches/program prefetches (lowest priority).
- When FSM interface is active for erase/program operations, data in the prefetch buffers and data cache in FMC will be flushed.

1.12.9 Erase/Program Flash

The F021 Flash (F2837xD Flash) should be programmed, erased, and verified only by using the F021 Flash API library. These functions are written, compiled and validated by Texas Instruments. The flash module contains a flash state machine (FSM) to perform program and erase operations. This section only provides a high level description for these operations, refer to the *Flash Application Programming Interface User's Specification* for more information.

A typical flow to program flash is:

Erase → Program → Verify

1.12.9.1 Erase

When the target flash is erased, it reads as all 1's. This state is called as 'blank.' The erase function must be executed before programming. The user should NOT skip erase on sectors that read as 'blank' because these sectors may require additional erasing due to marginally erased bits columns. The FSM provides an "Erase Sector" command to erase the target sector. The erase function erases the data and the ECC together. These commands are implemented by the following Flash API function:

```
Fapi_issueAsyncCommandWithAddress();
```

The Flash API provides the following function to determine if the flash bank is 'blank':

```
Fapi_doBlankCheck();
```

1.12.9.2 Program

The FSM provides a command to program the customer OTP area and Flash program data area. This command is also used to program ECC check bits.

This command is implemented by the following Flash API functions:

```
Fapi_issueProgrammingCommand();
```

Program function provides the options to program data without ECC, data along with user provided ECC data, data along with ECC calculated by API software, and to program ECC only.

1.12.9.3 Verify

After programming, the user must perform verify using API function Fapi_doVerify(). This function verifies the flash contents against supplied data in normal read mode and also in read-margin modes. Read-margin modes 0 and 1 are used to test cells for marginality. Read margin 0 is used to test cells for marginality of programmed cells. Read margin 1 is used to test cells for marginality of erased cells.

Application software is generally developed to enter read-margin mode during power-up and perform a full CRC check of the flash contents. In this way, a potential read mode failure can be identified prior to data loss or gain causing a bit flip.

NOTE: The read-margin modes are intended for diagnostic capabilities. Flash content is guaranteed for the lifetime specified in the datasheet.

Read margin modes should only be entered when executing from RAM. Banks must be powered up before entering a read margin mode. When entering a read margin mode, or changing from one read margin mode to the other, allow 1us delay before the first flash access to allow the flash banks to adjust to the new mode.

Read margin modes 0/1 are enabled by setting the RM0/RM1 bits in the special read control register FSPRD. The recommended procedures to enter, change and exit read margin mode are shown below.

To enter read-margin mode:

1. Start execution out of RAM.
2. Set the banks to remain powered up by writing 3 to bits 0:1 of FBFAULTBACK register.
3. Turn on read margin 0 or 1 by writing 1 or 2 to FSPRD register.
4. Do one dummy read from each bank to turn on the bank.
5. Flush the data cache by reading two Flash locations separated by at least 32 bytes. The read data should be ignored for these reads.
6. Wait 1 us

Any reads will now be with the selected read margins. The application can now return to flash if desired.

To exit read-margin mode:

1. Start execution out of RAM.
2. Turn off read margin 0 or 1 by writing 0 to FSPRD register.
3. Flush the data cache by reading two Flash locations separated by at least 32 bytes. The read data should be ignored for these reads.
4. Wait 1 us

Any reads will now be a standard read. The application can now return to flash if desired. The application can also set the FBFAULTBACK register to the original values.

To change one read margin mode to the other:

1. Follow the procedure to exit read margin mode above.

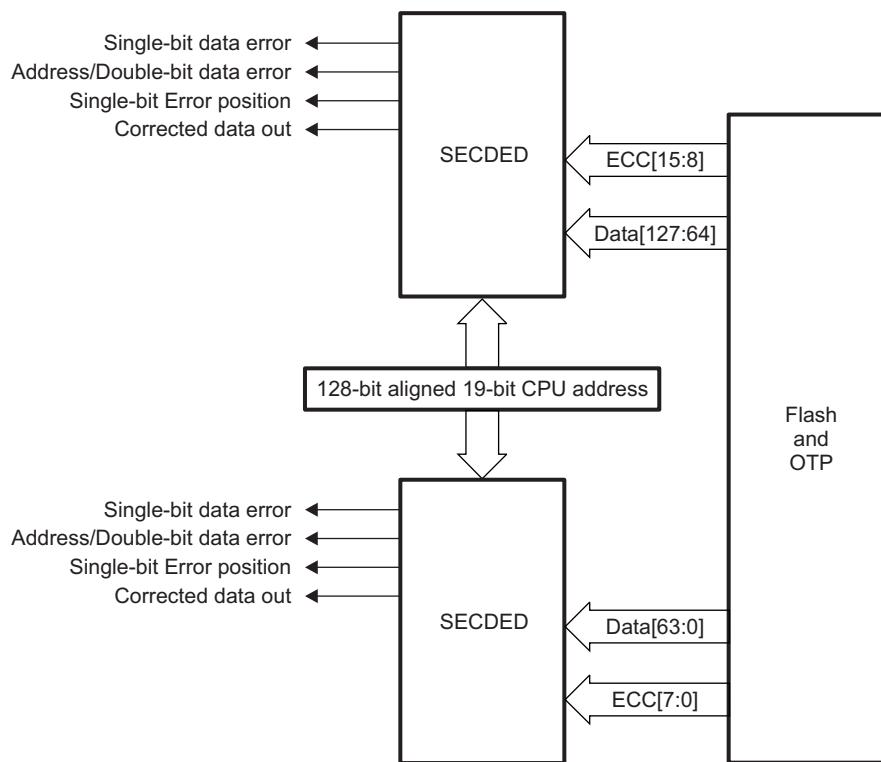
2. Follow the procedure to enter read margin mode above.

1.12.10 ECC Protection

CPU1-FMC and CPU2-FMC contain an embedded single error correction and double error detection (SECDED) module. SECDED, when enabled, provides the capability to screen out memory faults. SECDED can detect and correct single-bit data errors and detect address errors/double-bit data errors. For every 64 bits of flash/OTP data (aligned on a 64-bit memory boundary) that is programmed, eight ECC check bits have to be calculated and programmed in ECC memory space. Refer to the device data manual for the Flash/OTP ECC memory map. SECDED works with a total of eight user-calculated error correction code (ECC) check bits associated with each 64-bit wide data word and its corresponding 128-bit memory-aligned address. If users want to use this SECDED feature, they have to program the ECC check bits along with flash data. Users can use the F021 Flash API to calculate and program ECC data along with flash data. Flash API uses hardware ECC logic in device to generate the ECC data for the given Flash data. (Flash Plugin, the Flash programming tool, integrated with Code Composer Studio uses Flash API to generate and program ECC data). Alternatively users can use linker supported ECC generation option to generate and place ECC in separate sections through the linker command file. Please refer to the *TMS320C28x Assembly Language Tools User's Guide* for more information on using linker supported ECC generation method.

Figure 1-25 illustrates the ECC logic inputs and outputs.

Figure 1-25. ECC Logic Inputs and Outputs



During instruction fetch or data read operation, the 19 address bits (three least significant bits of address are not considered), together with the 64-bit data/8-bit ECC read-out of flash banks/ECC memory map area, pass through the SECDED logic and the eight checkbits are produced in FMC. These eight calculated ECC check bits are then XORed with the stored check bits (user programmed check bits) associated with the address and the read data. The 8-bit output is decoded inside the SECDED module to determine one of three conditions:

- No error occurred
- A correctable error (single bit data error) occurred
- A non-correctable error (double bit data error or address error) occurred

If the SECDED logic finds a single bit error in the address field, then it is considered to be a non-correctable error.

NOTE: Since ECC is calculated for an entire 64-bit data, a non 64-bit read such as a byte read or a half-word read will still force the entire 64-bit data to be read and calculated, but only the byte or half-word will be actually used by the CPU.

This ECC (SECDED) feature is enabled at reset. ECC_ENABLE register can be used to configure enable/disable of ECC feature. There are two SECDED modules in each FMC. Out of the 128-bit data (aligned on a 128-bit memory boundary) read from the bank/OTP address, lower 64-bits of data and corresponding 8 ECC bits (read from user programmable ECC memory area) are fed as inputs to one SECDED module along with 128-bit aligned 19-bit address from where data has been read. The upper 64-bits of data and corresponding 8 ECC bits are fed as inputs to another SECDED module in parallel along with 128-bit aligned 19-bit address. Each of the SECDED modules evaluate their inputs and determine if there is any single bit data error or double bit data error/address error.

ECC logic will be bypassed when the 64 data bits and the associated ECC bits fetched from the bank are either all ones or zeros.

1.12.10.1 Single-Bit Data Error

This section provides information for both single-bit data errors and single-bit ECC check bit errors. If there is a single bit flip (0 to 1 or 1 to 0) in flash data or in ECC data, then it is considered as a single-bit data error. The SECDED module detects and corrects single bit errors, if any, in the 64-bit flash data or eight ECC check bits read from the flash/ECC memory map before the read data is provided to the CPU.

When SECDED finds and corrects single bit data errors, the following information is logged in ECC registers if the ECC feature is enabled:

- Address where the error occurred – If the single bit error occurs in lower 64-bits of a 128-bit memory aligned data, lower 64-bit memory aligned address will be captured in SINGLE_ERR_ADDR_LOW register. If the single bit error occurs in upper 64-bits of a 128-bit memory aligned data, upper 64-bit memory aligned address will be captured in SINGLE_ERR_ADDR_HIGH register.
- Whether error occurred in data bits or ECC bits – ERR_TYPE_L, ERR_TYPE_H bit fields in ERR_POS register indicate whether the error occurred in data bits or ECC bits of lower 64-bits, upper 64-bits respectively of a 128-bit memory aligned data.
- Bit position at which error occurred – ERR_POS_L, ERR_POS_H bit fields in ERR_POS register indicate the bit position of the error in the lower 64-bits/lower 8-bit ECC, upper 64-bits/upper 8-bit ECC respectively of a 128-bit memory aligned data.
- Whether the corrected value is 0 (FAIL_0_L, FAIL_0_H flags in ERR_STATUS register)
- Whether the corrected value is 1 (FAIL_1_L, FAIL_1_H flags in ERR_STATUS register)
- A single bit error counter that increments on every single bit error occurrence (ERR_CNT register) until a user-configurable threshold (see ERR_THRESHOLD) is met
- A flag that gets set when one more single bit error occurs after ERR_CNT equals ERR_THRESHOLD (SINGLE_ERR_INT_FLG flag in ERR_INTCR register)

When the ERR_CNT value equals THRESHOLD+1 value and a single bit error occurs, the SINGLE_ERR_INT flag is set, and an interrupt (FLASH_CORRECTABLE_ERR on C28x PIE has to be enabled for interrupt, if needed) is fired. The SINGLE_ERR interrupt will not be fired again until the SINGLE_ERR_INTCR is cleared. If the single error interrupt flag is not cleared using the corresponding error interrupt clear bit in the ERR_INTCR register, the error interrupt will not come again, as this is an edge-based interrupt.

1.12.10.2 Uncorrectable Error

Uncorrectable errors include address errors and double-bit errors in data/ECC. When SECDED finds uncorrectable errors, the following information is logged in ECC registers if the ECC feature is enabled:

- Address where the error occurred – If the uncorrectable error occurs in lower 64-bits of a 128-bit memory aligned data, lower 64-bit memory aligned address will be captured in

UNC_ERR_ADDR_LOW register. If the uncorrectable error occurs in upper 64-bits of a 128-bit memory aligned data, upper 64-bit memory aligned address will be captured in UNC_ERR_ADDR_HIGH register.

- A flag is set indicating that an uncorrectable error occurred – UNC_ERR_L, UNC_ERR_H flags in ERR_STATUS register indicate the uncorrectable error occurrence in the lower 64-bits/lower 8-bit ECC, upper 64-bits/upper 8-bit ECC respectively, of a 128-bit memory aligned data.
- A flag is set indicating that an uncorrectable error interrupt is fired (UNC_ERR_INTFLG in ERR_INTFLG register)

When an uncorrectable error occurs, the UNC_ERR_INTFLG bit is set and an uncorrectable error interrupt is fired. This uncorrectable error interrupt generates a NMI on C28x core, if enabled. If an uncorrectable error interrupt flag is not cleared using the corresponding error interrupt clear bit in the ERR_INTCLEAR register, an error interrupt will not come again, as this is an edge based interrupt.

Although ECC is calculated on 64-bit basis, a read of any address location within a 128-bit aligned Flash memory will cause the uncorrectable error flag to get set when there is a uncorrectable error in both or in either one of the lower 64 and upper 64 bits (or corresponding ECC check bits) of that 128-bit data. NMI will occur on CPU for a read of any address location within a 128-bit aligned Flash memory when there is a uncorrectable error in both or in either one of the lower 64 and upper 64 bits (or corresponding ECC check bits) of that 128-bit data.

1.12.10.3 SECDED Logic Correctness Check

Since error detection and correction logic is part of safety-critical logic, safety applications may need to ensure that the SECDED logic is working fine always. For these safety concerns, in order to ensure the correctness of the SECDED logic, an ECC test mode is provided to test the correctness of ECC logic periodically. In this ECC test mode, instead of a data/ECC read from bank and address given to the FMC for read, a user-configurable 64-bit data/8-bit ECC check bits (FDATAH_TEST, FDATAL_TEST, FECC_TEST) and address (FADDR_TEST) are fed to SECDED logic. Using this test mode, users can introduce single bit errors or double bit errors or address errors and check whether SECDED logic is catching those errors or not. Users can also check if SECDED logic is reporting any false errors when no errors are introduced.

This ECC test mode can be enabled by setting the ECC_TEST_EN bit in the FECC_CTRL register. When ECC test mode is enabled, CPU cannot read the data from flash and instead CPU gets data from ECC test mode registers (FDATAH_TEST/FDATAL_TEST). This is because ECC test mode registers (FDATAH_TEST, FDATAL_TEST, FECC_TEST) are multiplexed with data from the flash. Hence CPU should not read/fetch from Flash when ECC test mode is enabled. For this reason, ECC test mode code should be executed from RAM and not from flash.

Only one of the SECDED modules (out of the two SECDED modules that work on lower 64 bits and upper 64 bits of a read 128-bit data) at a time can be tested. The ECC_SELECT bit in the FECC_CTRL register can be configured by users to select one of the SECDED modules for test.

To test the ECC logic using ECC test mode, users can follow below steps:

1. Obtain the ECC for a given Flash address (128-bit aligned) and 64-bit data by using Auto ECC generation option provided in Flash API or by using the linker ECC generation method.
2. Then develop an application to test ECC logic using the above data. In this application
 - Write the 128-bit aligned 19-bit Flash address in FADDR_TEST
 - Write 64-bit data in FDATAx_TEST (FDATAL_TEST or FDATAH_TEST depending on which ECC logic user want to test) register
 - Write corresponding 8-bit ECC in FECC_TEST register
 - In any of the above three steps, users can insert errors (single bit data error or double bit data error or address error or single bit ECC error or double bit ECC error) so that they can check whether ECC logic is able to catch the errors or not
 - Select the ECC logic block (lower 64-bits or upper 64-bits) which needs to be tested using ECC_SELECT bit in the FECC_CTRL register
 - Enable ECC test mode using ECC_TEST_EN bit in FECC_CTRL register
 - Write a value of 1 in DO_ECC_CALC bit in FECC_CTRL register and this will enable ECC test

logic for a single cycle to evaluate the address, data, ECC in FADDR_TEST, FDATAx_TEST and FECC_TEST registers for ECC errors

Once the above ECC test mode registers are written by the user:

- The FECC_OUTH register holds the data output bits 63:32 from the SECDED block under test
- The FECC_OUTL register holds the data output bits 31:0 from the SECDED block under test
- The FECC_STATUS register holds the status of single-bit error occurrence, uncorrectable error occurrence, and error position of single bit error in data/check bits

1.12.11 Reserved Locations Within Flash and OTP

When allocating code and data to flash and OTP memory, keep the following reserved locations of flash/OTP in mind:

- Entire USER OTP has reserved user configurable locations for security and Boot process. For more details on the functionality of these fields, please refer to the *Dual Code Security Module (DCSM)* section of this chapter, and the *ROM Code and Peripheral Booting* chapter.
- Refer to the *ROM Code and Peripheral Booting* chapter for reserved locations in flash for SYSBIOS usage and boot to flash entry point (boot to flash entry point is reserved for an entry into flash branch instruction. When the boot to flash boot option is used, the boot ROM will jump to this address in flash. If the user programs a branch instruction here, that will then re-direct code execution to the entry point of the application).

1.12.12 Procedure to Change the Flash Control Registers

During flash configuration, no accesses to the flash or OTP can be in progress. This includes instructions still in the CPU pipeline, data reads, and instruction pre-fetch operations. To be sure that no access takes place during the configuration change, you should follow the procedure shown below for any code that modifies the flash control registers. This is applicable for both CPU1 subsystem and CPU2 subsystem application.

1. Start executing application code from RAM/Flash/OTP.
2. Branch to or call the flash configuration code (that writes to flash control registers) in RAM. This is required to properly flush the CPU pipeline before the configuration change. The function that changes the flash configuration cannot execute from the Flash or OTP. It must reside in RAM.
3. Execute the Flash configuration code (should be located in RAM) that writes to flash control registers like FRDCNTL, FRD_INTF_CTRL, and so on.
4. At the end of the Flash configuration code execution, wait eight cycles to let the write instructions propagate through the CPU pipeline. This must be done before the return-from-function call is made.
5. Return to the calling function which might reside in RAM or Flash/OTP and continue execution.

1.13 Dual Code Security Module (DCSM)

The dual code security module (DCSM) is a security feature incorporated in this device. It prevents access and visibility to on-chip secure memories (and other secure resources) to unauthorized persons (it prevents duplication and reverse engineering of proprietary code). The term “secure” implies access to on-chip secure memories and resources is blocked. The term “unsecure” implies access is allowed (the contents of the memory could be read by any means); for example, through a debugging tool such as Code Composer Studio™.

There are two CPUs on this device and both CPU sub-systems have their own CSM for code protection. Each CPU sub-system's CSM has dual-zone security, which means the CPU1 sub-system has two zones (zone1/zone2) and CPU2 also has two zones (zone1/zone2).

All the security features discussed in this chapter are applicable to both CPU sub-systems, unless otherwise mentioned.

1.13.1 Functional Description

The security module restricts the CPU access to on-chip secure memory/resource without interrupting or stalling CPU execution. When a read occurs to a secure memory location, the read returns a zero value and CPU execution continues with the next instruction. This, in effect, blocks read and writes access to secure memories through the JTAG port or external peripherals.

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). Security mechanism for both the zones is identical. Each zone has its own dedicated secure resource and allocated secure resource. The following are different secure resources available on this device:

- OTP : Each zone has its own dedicated secure OTP . This contains the security configurations for individual Zone.
- CLA: The CLA is a secure resource which can be allocated to either zone by configuring the GRABRAM location in the user-OTP. CLA configuration can only be performed by code running from the zone to which it has been allocated. The CLA message RAMs also belong to the same zone.
- RAM: All LSx RAMs can be secure RAM on this device. These RAMs can be allocated to either zone by configuring the respective GRABRAM location in the user-OTP .
- Flash Sectors: Flash Sectors can be secure on this device. Each Flash sector can be allocated to either zone by configuring the respective GRABSECT location in the user-OTP
- Secure ROM: This device also has secure ROM which is EXEONLY protected. This ROM contains specific function for the user, provided by TI.

Table 1-17 shows the status of a RAM block based on the configuration in GRABRAM register.

Table 1-17. RAM Status

GRAB-Lx Bits in Z1_GRABRAMR Register	GRAB-Lx Bits in Z2_GRABRAMR Register	Ownership
00	XX	Lx RAM is inaccessible
XX	00	Lx RAM is inaccessible
Differential Value (01/10)	Differential Value (01/10)	Lx RAM is inaccessible
Differential Value (01/10)	11	Lx RAM belongs to Z1
11	Differential Value (01/10)	Lx RAM belongs to Z2
11	11	Lx RAM is Non-Secure

Security of each zone is ensured by its own 128-bit (four 32-bit words) password (CSM password). The password for each Zone is stored in its dedicated OTP location based on a zone specific link pointer. A zone can be unsecured by executing the password match flow (PMF), described in [Section 1.13.3.3.2](#).

There are three types of accesses: data/program reads, JTAG access, and instruction fetches (calls, jumps, code executions, ISRs). Instruction fetches are never blocked. JTAG accesses are always blocked when a memory is secure. Data reads to a secure memory are always blocked unless the program is executing from a memory which belongs to the same zone. Data reads to unsecure memory are always allowed. [Table 1-18](#) shows the levels of security.

Table 1-18. Security Levels

PMF Executed With Correct Password?	Operating Mode of the Zone	Program Fetch Location	Security Description
No	Secure	Outside secure memory	Only instruction fetches by the CPU are allowed to secure memory. In other words, code can still be executed, but not read.
No	Secure	Inside secure memory	CPU has full access (except for EXEONLY memories where read is not allowed). JTAG port cannot read the secured memory contents.
Yes	Non-Secure	Anywhere	Full access for CPU and JTAG port to secure memory of that zone.

If the password locations of a zone have all 128 bits as ones, the Zone is considered unsecure. Since new Flash devices have erased Flash (all ones), only a read of the password locations is required to bring any Zone into unsecure mode. If the password locations of a Zone have all 128 bits as zeros, the Zone is secure, regardless of the contents of the CSMKEY registers which means zone can't be unlocked using PMF. The user should never use all zeros as a password. If password locations are programmed with all zeros, the device cannot be unlocked by the password match flow described in [Section 1.13.3.3.2](#). A password of all zeros will prevent debug of secure code or re-programming the Flash.

CSMKEY registers are user accessible registers that are used to unsecure the zones.

1.13.1.1 Emulation Code Security Logic (ECSL)

In addition to the CSM, the emulation code security logic (ECSL) has been implemented using a 64-bit password (part of existing CSM password) for each zone to prevent unauthorized users from stepping through secure code. A halt in secure code while the emulator is connected will trip the ECSL and break the emulation connection to the specific CPU subsystem for which the ECSL violation occurred. To allow emulation of secure code, while maintaining the CSM protection against secure memory reads, the user must write the correct 64-bit password into the CSMKEY (0/1) registers, which matches the password value stored in the user-OTP of that zone. This will disable the ECSL for the specific zone.

When initially debugging a device with the password locations in OTP programmed (secured), the emulator takes some time to take control of the CPU. During this time, the CPU will start running and may execute an instruction that performs an access to a protected ECSL area and if CPU is halted when program-counter (PC) is pointing to a secure location, the ECSL will trip and cause the emulator connection to be broken.

The solution to this problem is:

- Use the “Branch to check boot mode” boot option. In this mode, core will be in a loop and continuously poll the boot-mode select pins. You can select this boot-mode and then exit this mode once the emulator is connected by re-mapping the PC to another address or by changing the boot-mode selection pin to the desired boot-mode.

1.13.1.2 CPU Secure Logic

CPU Secure Logic (CPUSL) on this device prevents a hacker from reading the CPU register in watch window while code is running through secure zone. All accesses to CPU registers when PC points to a secure location are blocked by this logic. Only exception to this is read access to PC. It's highly recommended not to write into CPU register in this case else proper code execution may get affected. If CSM is unlocked using CSM password match flow, CPUSL logic also gets disabled.

1.13.1.3 Execute-Only Protection

To achieve higher level of security on secure Flash sectors and RAM blocks that store critical user code (instruction opcodes), Execute-Only protection feature is provided. When the Execute-Only protection is turned on for any secure Flash sector or RAM block, data reads to that Flash sectors are disallowed from any code (even from secure code). Execute-only protection for a Flash sector and RAM block can be turned on by configuring the bit field associated for that particular sector/RAM block in the zones (which has ownership of that sector/RAM block) EXEONLYSECT and EXEONLYRAM register, respectively.

1.13.1.4 Password Lock

The password locations for each zone can be locked by programming the zone's PSWDLOCK field with any value other than "1111" (0xF) at PSWDLOCK location in OTP . Until passwords of a zone is locked, password locations will not be secure and can be read from debugger as well as code running from non-secure memory. This feature can be used by the user to avoid accidental locking of zone while programming the Flash sectors during software development phase. On fresh device the value for password lock fields for all zones at PSWDLOCK location in OTP will be "1111" which means password for all zone will be unlocked.

NOTE: Password unlock only makes password locations non-secure. All other secure memories and other locations of Flash sectors, which contains password, remains secure as per security settings. But since passwords are non-secure, anyone can read the password and make zone non-secure by running through PMF.

1.13.1.5 Link Pointer and Zone Select

For each of the two security zones of each CPU sub-system on this device, a dedicated OTP block exists that holds configuration related to zone's security. The following are the configurations that are programmed in these respective OTP Flash.

- Zx-LINKPOINTER1
- Zx-LINKPOINTER2
- Zx-LINKPOINTER3
- Zx-PSWDLOCK
- Zx-CRCLOCK
- Zx-BOOTCTRL
- Zx-EXEONLYRAM
- Zx-EXEONLYSECT
- Zx-GRABRAM
- Zx-GRABRAM
- Zx-CSMPASSWORD

Since OTP can't be erased, to provide flexibility of configuring some of the security settings like CSM passwords, allocation of RAM/Flash sectors and there attributes, multiple times by the user, following configuration are placed in zone select region of each zone's OTP Flash.

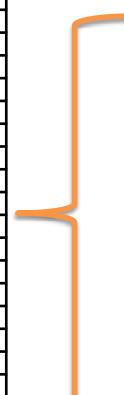
- Zx-EXEONLYRAM
- Zx-EXEONLYSECT
- Zx-GRABRAM
- Zx-GRABSECT
- Zx-CSMPASSWORD

Location of the zone select region in OTP is decided based on value of three 29-bit Link Pointers (Zx-LINKPOINTERx) programmed in OTP of each zone of both CPU sub-systems. All OTP locations except Link Pointer locations are protected with ECC. Since the Link Pointer locations are not protected with ECC, three Link Pointers are provided that need to be programmed with same value and the final value of Link Pointer is resolved in hardware when dummy read is done to all the link pointer by comparing all the

three values (bit-wise voting logic). Since in OTP, a ‘1’ can be flipped by the user to ‘0’ but ‘0’ can’t be flipped to ‘1’ (no erase operation for OTP), the most significant bit position in the resolved Link-Pointer which is ‘0’, defines the valid base-address for zone select region. While generating the final Link Pointer value if the bit patterns looks anything different than the following pattern, the final Link Pointer value becomes All_1 (0xFFFF_FFFF) which select the Zone-Select-Block1 (also known as default Zone Select Block).

`1[1][1]...0[0][0]` :: '1' on MSB -> 0 or more occurrence of '1' -> at-least one occurrence of '0' -> 0 or more occurrence of '0'.

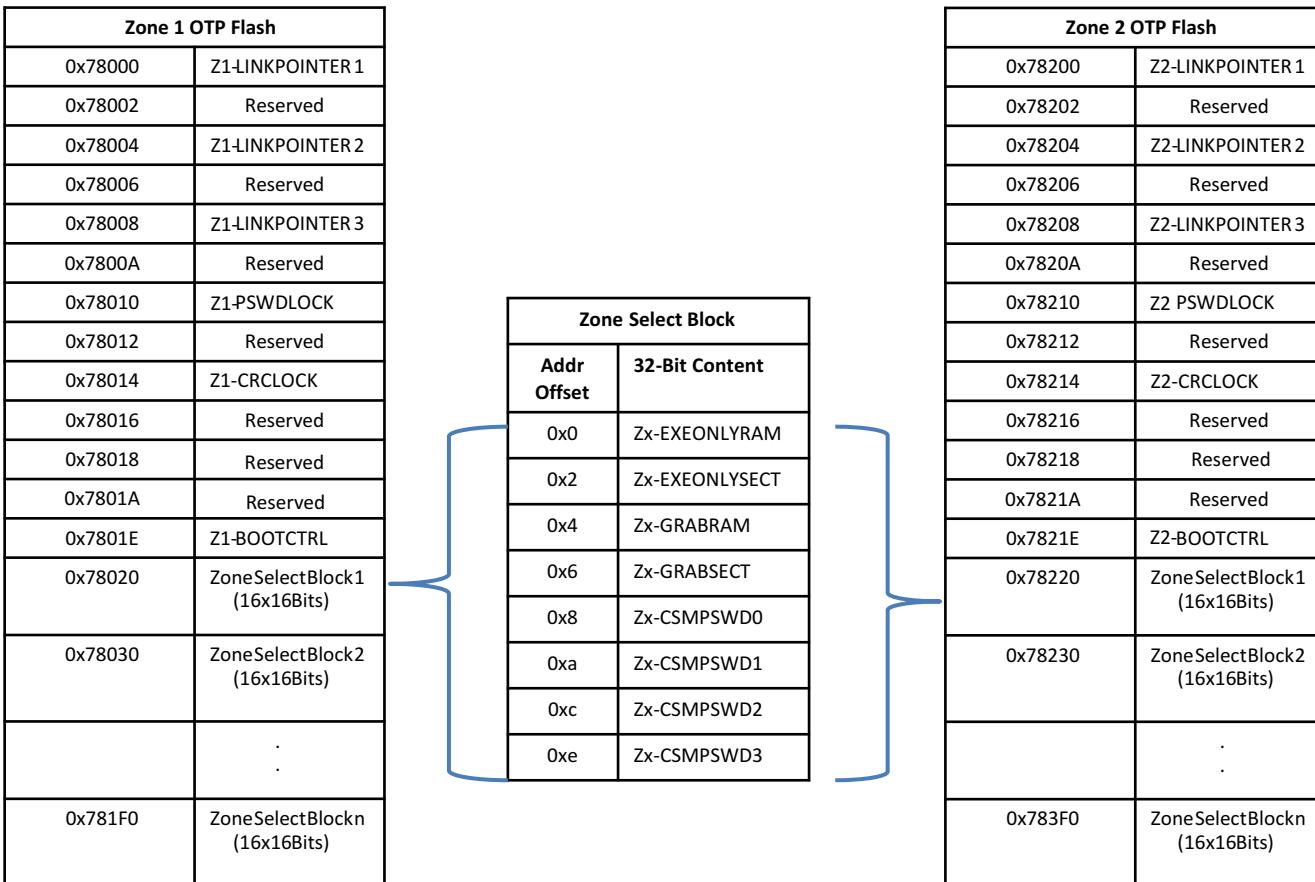
Figure 1-26. Storage of Zone-Select Bits in OTP



The diagram illustrates the mapping between memory addresses and the Zone Select Block. The main table lists memory addresses (32'bxxx...) and their corresponding 'Addr Offset Of Zone-Select Block' values (0x20, 0x30, etc.). A separate table, titled 'Zone Select Block', shows the 32-bit content for each offset. An orange bracket connects the 'Addr Offset' column in the main table to the 'Addr Offset' column in the secondary table.

Zone Select Block	
Addr Offset	32-Bit Content
0x0	Zx-EXEONLYRAM
0x2	Zx-EXEONLYSECT
0x4	Zx-GRABRAM
0x6	Zx-GRABSECT
0x8	Zx-CSMPSPWD0
0xa	Zx-CSMPSPWD1
0xc	Zx-CSMPSPWD2
0xe	Zx-CSMPSPWD3

NOTE: Address locations for other security settings (PASWDLOCK/CRCLOCK) that are not part of Zone Select blocks can be programmed only once; therefore, the user should program them towards end of the development cycle.

Figure 1-27. Location of Zone-Select Block Based on Link-Pointer


1.13.1.5.1 C Code Example to get Zone Select Block Addr for Zone1

```

unsigned long LinkPointer;
unsigned long *Zone1SelBlockPtr;
int Bitpos = 28;
int ZeroFound = 0;

// Read Z1-Linkpointer register of DCSM module.
LinkPointer = *(unsigned long *)0x5F000;

// Bits 31 30 and 29 as most-significant 0 are reserved LinkPointer options

LinkPointer = LinkPointer << 2;

while ((ZeroFound == 0) && (bitpos > -1))
{
    if ((LinkPointer & 0x80000000) == 0)
    {
        ZeroFound = 1;
        Zone1SelBlockPtr = (unsigned long *) (0x78000 + ((bitpos + 3)*16));
    } else
    {
        bitpos--;
        LinkPointer = LinkPointer << 1;
    }
}
if (ZeroFound == 0)
{

```

```

    //Default in case there is no zero found.
    Zone1SelBlockPtr = (unsigned long *)0x78020;
}

```

1.13.1.6 Flash and OTP Erase/Program

On this device, OTP as well as normal Flash are secure resources. Each zone has its own dedicated OTP where as normal Flash sectors can be allocated to any zone based on the value programmed in GRABSECT location in OTP . Each zone has its own CSM passwords, and read and write accesses are not allowed to resources owned by Z1 from code running from memory allocated to Z2 and vice versa. Before programming any secure Flash sector, the user must unlock the zone, to which that particular sector belongs to, using PMF. Same is the case for erasing any secure Flash sector. Similarly to program the security settings in OTP Flash, the user must unlock the CSM of the respective zone. OTP content cannot be erased.

This device has only one Flash pump used for erase/program operation of normal Flash and OTP Flash. A semaphore mechanism is provided to avoid the conflict between Zone1 and Zone2. A zone need to grab this semaphore to successfully complete the erase/program operation on the Flash sectors allocated to that zone. Semaphore can be grabbed by a zone by writing appropriate value in SEM field of FLSEM register. For further details of this field, see the register description.

1.13.1.7 Safe Copy Code

In some applications, the user may want to copy the code from secure Flash to secure RAM for better performance. The user cannot do this for EXEONLY Flash sector because of the fact that EXEONLY secure memories cannot be read from anywhere. TI provides specific “Safe Copy Code” library functions for each zone to enable the user to copy content from EXEONLY secure Flash sectors to EXEONLY RAM block. These functions do the copy-code operation in a highly secure environment and allow copy only in following condition.

- Secure RAM block & Secure Flash sectors belongs to same zone.
- Both Secure RAM block and Secure Flash sector have EXEONLY protection.

For further usage of these library functions, see the device-specific Boot ROM documentation.

1.13.1.8 SafeCRC

Since read from EXEONLY memories is not allowed, the user cannot calculate CRC for content in EXEONLY memories using VCU-II. But in some safety critical application, the user may have to calculate the CRC on these memories as well. To enable this without compromising on security, TI provides specific “SafeCRC” library functions for each zone. These functions do the CRC calculation in highly secure environment and allow CRC calculation in only following condition.

- Source address should be module of no. of words (based on length_id) for which CRC need to be calculated.
- Destination address should belong to same zone as source address.

For further usage of these library functions, see the device-specific Boot ROM documentation.

NOTE: The user must disable all the interrupts before calling the safe copy code and the safeCRC function. If there is a vector fetch during copy code operation, CPU gets reset immediately.

Disclaimer: Code Security Module Disclaimer The Code Security Module (CSM) included on this device was designed to password protect the data stored in the associated memory and is warranted by Texas Instruments (TI), in accordance with its standard terms and conditions, to conform to TI's published specifications for the warranty period applicable for this device. TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IN NO

EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

1.13.2 CSM Impact on Other On-Chip Resources

On this device, M0/M1 and GSx memories are not secure. But to avoid any potential hacking when device is in default state (post reset), accesses (all types) to all memories (secure as well as non-secure, except BOOT-ROM and OTP) are disabled till proper security initialization is done. This means just after reset none of the memory resource except BOOT_ROM and OTP is accessible to the user.

The following are the steps required after reset (any type of reset) to initialize the security on each CPU sub-system.

- Dummy Read to address location of SECDC (0x703F0) in TI OTP
- Dummy Read to address location of Z1_LINKPOINTER1 in Z1 OTP
- Dummy Read to address location of Z1_LINKPOINTER2 in Z1 OTP
- Dummy Read to address location of Z1_LINKPOINTER3 in Z1 OTP
- Dummy Read to address location of Z1_PSWDLOCK in Z1 OTP
- Dummy Read to address location of Z1_CRCLOCK in Z1 OTP
- Dummy Read to address location 0x78018 in Z1 OTP
- Dummy Read to address location of Z1_BOOTCTRL in Z1 OTP
- Read to memory map register of Z1_LINKPOINTER in DCSM module to calculate the address of zone select block for Z1
- Dummy read to address location of Z1_EXEONLYRAM in Z1 OTP
- Dummy read to address location of Z1_EXEONLYSECT in Z1 OTP
- Dummy read to address location of Z1_GRABRAM in Z1 OTP
- Dummy read to address location of Z1_GRABSECT in Z1 OTP
- Dummy Read to address location of Z2_LINKPOINTER1 in Z2 OTP
- Dummy Read to address location of Z2_LINKPOINTER2 in Z2 OTP
- Dummy Read to address location of Z2_LINKPOINTER3 in Z2 OTP
- Dummy Read to address location of Z2_PSWDLOCK in Z2 OTP
- Dummy Read to address location of Z2_CRCLOCK in Z2 OTP
- Dummy Read to address location 0x78218 in Z2 OTP
- Dummy Read to address location of Z2_BOOTCTRL in Z2 OTP
- Read to memory map register of Z2_LINKPOINTER in DCSM module to calculate the address of zone select block for Z2
- Dummy read to address location of Z2_EXEONLYRAM in Z2 OTP
- Dummy read to address location of Z2_EXEONLYSECT in Z2 OTP
- Dummy read to address location of Z2_GRABRAM in Z2 OTP
- Dummy read to address location of Z2_GRABSECT in Z2 OTP

1.13.3 Incorporating Code Security in User Applications

Code security is typically not required in the development phase of a project. However, security is needed once a robust code is developed for a zone. Before such a code is programmed in the Flash memory, a CSM password should be chosen to secure the zone. Once a CSM password is in place for a zone, the zone is secured (programming a password at the appropriate locations and either performing a device reset or setting the FORCESEC bit ($Zx_CR.15$) is the action that secures the device. From that time on, access to debug the contents of secure memory by any means (via JTAG, code running off external/on-chip memory, and so forth) requires supply of a valid password. A password is not needed to run the code out of secure memory (such as in a typical end-customer usage); however, access to secure memory contents for debug purpose, requires a password.

1.13.3.1 Environments That Require Security Unlocking

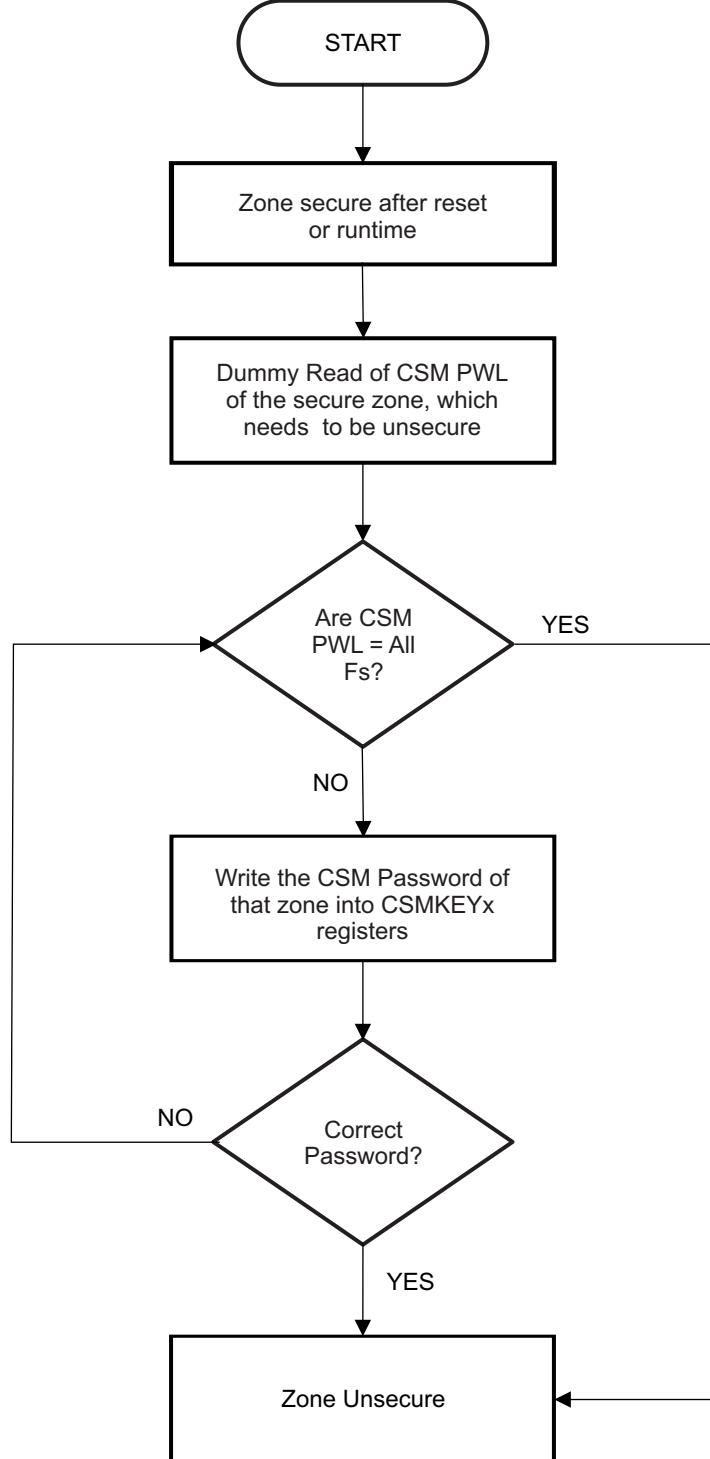
The following are the typical situations under which unsecuring can be required:

- Code development using debuggers (such as Code Composer Studio). This is the most common environment during the design phase of a product.
- Flash programming using TI's Flash utilities such as Code Composer Studio On-Chip Flash Programmer plug-in or the Uniflash tool. Flash programming is common during code development and testing. Once the user supplies the necessary password, the Flash utilities disable the security logic before attempting to program the Flash. The Flash utilities can disable the code security logic in new devices without any authorization, since new devices come with an erased Flash. However, reprogramming devices (that already contain a custom password) require the password to be supplied to the Flash utilities in order to unlock the device to enable programming. In custom programming solutions that use the Flash API supplied by TI unlocking the CSM can be avoided by executing the Flash programming algorithms from secure memory.
- Custom environment defined by the application In addition to the above, access to secure memory contents can be required in situations such as:
 - Using the on-chip bootloader to load code or data into secure SARAM or to erase and program the Flash.
 - Executing code from on-chip unsecure memory and requiring access to secure memory for lookup table. This is not a suggested operating condition as supplying the password from external code could compromise code security.

The unsecuring sequence is identical in all the above situations. This sequence is referred to as the password match flow (PMF) for simplicity. [Figure 1-28](#) explains the sequence of operation that is required every time the user attempts to unsecure a particular zone. A code example is listed for clarity.

1.13.3.2 CSM Password Match Flow

Password match flow (PMF) is essentially a sequence of four dummy reads from password locations (PWL) followed by four writes (32-bit writes) to CSMKEY(0/1/2/3) registers. [Figure 1-28](#) shows how PMF helps to initialize the security logic registers and disable security logic.

Figure 1-28. CSM Password Match Flow (PMF)

1.13.3.3 Unsecuring Considerations for Zones With and Without Code Security

Case 1 and Case 2 provide unsecuring considerations for zones with and without code security.

- **Case 1: Zone With Code Security**

A zone with code security should have a predetermined password stored in the password locations of that zone. In addition, reserved password locations of that zone should be programmed with all 0x0000

and not used for program and/or data storage. The following are steps to unsecure any secure zone:

1. Perform a dummy read of the password locations of that zone.
2. Write the password into the CSMKEY registers.
3. If the password is correct, the zone becomes unsecure; otherwise, it stays secure.

- **Case 2: Zone Without Code Security**

A zone without code security should have 0x FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF (128 bits of all ones) stored in the password locations. The following are steps to use this zone:

1. At reset, the CSM will lock memory regions protected by the CSM.
2. Perform a dummy read of the password locations.
3. Since the password is all ones, this alone will unlock the zone and all the secure memories dedicated to that zone are fully accessible immediately after this operation is completed.

NOTE: Even if a zone is not protected with a password (all password locations all ones), the CSM will lock at reset. Thus, a dummy read operation must still be performed on these zones prior to reading, writing, or programming secure memory if the code performing the access is executing from outside of the CSM protected memory region. The Boot ROM code does this dummy read for convenience.

1.13.3.3.1 C Code Example to Unsecure C28x Zone1

```

volatile long int *CSM = (volatile long int *)0x5F000;      //CSM register file
volatile long int *CSMPWL = (volatile long int *)0x78028; //CSM Password location (assuming
default Zone sel block)
volatile int tmp;
int I;
// Read the 128-bits of the CSM password locations (PWL)
//
for (I=0; i<4; I++) tmp = *CSMPWL++;
// If the password locations (CSMPWL) are all = ones (0xFFFF),
// then the zone will now be unsecure. If the password
// is not all ones (0xFFFF), then the code below is required
// to unsecure the CSM.
// Write the 128-bit password to the CSMKEY registers
// If this password matches that stored in the
// CSLPWL then the CSM will become unsecure. If it does not
// match, then the zone will remain secure.
// An example password of:
// 0x11112222333344445555666677778888 is used.
*CSM++ = 0x22221111; // Register Z1_CSMKEY0 at 0x5F010
*CSM++ = 0x44443333; // Register Z1_CSMKEY1 at 0x5F012
*CSM++ = 0x66665555; // Register Z1_CSMKEY2 at 0x5F014
*CSM++ = 0x88887777; // Register Z1_CSMKEY3 at 0x5F016

```

1.13.3.3.2 C Code Example to Resecure C28x Zone1

```

volatile int *Z1_CR = 0x5F019; //CSMSCR register
//Set FORCESEC bit
*Z1_CR = 0x8000;

```

1.13.3.4 Environments That Require ECSL Unlocking

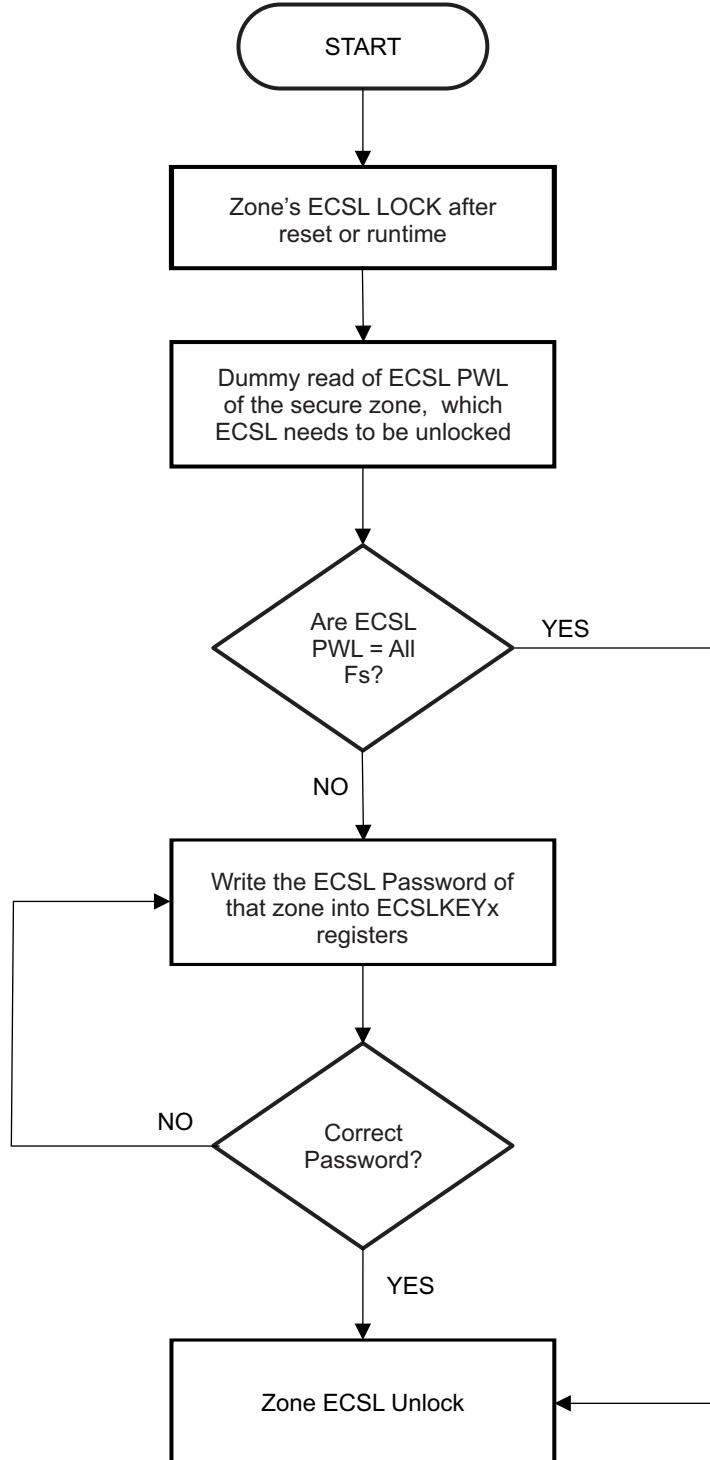
The following are the typical situations under which unsecuring can be required:

- The user develops some main IP, and then outsources peripheral functions to a subcontractor who must be able to run the customer code during debug and may halt while main IP code is running. If ECSL is not unlocked, then Code Composer Studio connections will get disconnected, which can be inconvenient for the user. Note that unlocking ECSL doesn't enable access to secure code but only avoids disconnection of CCS (JTAG).

1.13.3.5 ECSL Password Match Flow

Password match flow (PMF) is essentially a sequence of eight dummy reads from password locations (PWL) followed by two writes to KEY registers. [Figure 1-29](#) shows how the PMF helps to initialize the security logic registers and disable security logic.

Figure 1-29. ECSL Password Match Flow (PMF)



1.13.4 DCSM Registers

A DCSM register is provided to prevent spurious writes from modifying the DACCTL, DACVALS, and DACOUTEN registers. Once a register is protected through DACLOCK, write access will be locked out until the device is reset.

1.13.4.1 ECSL Disable Considerations for any Zone

A zone with ECSL enabled should have a predetermined ECSL password stored in the ECSL password locations in Flash (same as lower 64 bits of CSM passwords). The following are steps to disable the ECSL for any particular zone:

- Perform a dummy read of CAM password locations of that Zone
- Write the password into the CSMKEYx registers, corresponding to that Zone.
- If the password is correct, the ECSL gets disabled; otherwise, it stays enabled.

1.13.4.1.1 C Code Example to Disable ECSL for C28x-Zone1

```

volatile long int *ECSL = (volatile int *)0x5F000;      //ECSL register file
volatile long int *ECSLPWL = (volatile int *)0x78028; //ECSL Password location (assuming default
Zone sel block)
volatile int tmp;
int I;
// Read the 64-bits of the password locations (PWL)
.
for (I=0; i<2; I++) tmp = *ECSLPWL++;
// If the ECSL password locations (ECSLPWL) are all = ones (0xFFFF),
// then the ECSL will now be disable. If the password
// is not all ones (0xFFFF), then the code below is required
// to disable the ECSL.
// Write the 64-bit password to the CSMKEYx registers
// If this password matches that stored in the
// CSMPWL then ECSL will get disable. If it does not
// match, then the zone will remain secure.
// An example password of:
// 0x1111222233334444 is used.
*ECSL++ = 0x22221111; // Register Z1_CSMKEY0 at 0x5F010
*ECSL++ = 0x44443333; // Register Z1_CSMKEY1 at 0x5F012

```

1.14 Registers

1.14.1 Base Addresses

Table 1-19. System Control Base Address Table

Device Registers	Register Name	Start Address	End Address
CpuTimer0Regs	CPU_TIMER_REGS	0x0000_0C00	0x0000_3C07
CpuTimer1Regs	CPU_TIMER_REGS	0x0000_0C08	0x0000_5C0F
CpuTimer2Regs	CPU_TIMER_REGS	0x0000_0C10	0x0000_C17F
PieCtrlRegs	PIE_CTRL_REGS	0x0000_0CE0	0x0000_0CFF
WdRegs	WD_REGS	0x0000_7000	0x0000_703F
NmiIntruptRegs	NMI_INTERRUPT_REGS	0x0000_7060	0x0000_706F
XintRegs	XINT_REGS	0x0000_7070	0x0000_707F
DmaClaSrcSelRegs	DMA_CLA_SRC_SEL_REGS	0x0000_7980	0x0000_79BF
DevCfgRegs ⁽¹⁾	DEV_CFG_REGS	0x0005_D000	0x0005_D19F
ClkCfgRegs	CLK_CFG_REGS	0x0005_D200	0x0005_D2FF
CpuSysRegs	CPU_SYS_REGS	0x0005_D300	0x0005_D3FF
RomPrefetchRegs ⁽¹⁾	ROM_PREFETCH_REGS	0x0005_E608	0x0005_E609
DcsmZ1Regs	DCSM_Z1_REGS	0x0005_F000	0x0005_F02F
DcsmZ2Regs	DCSM_Z2_REGS	0x0005_F040	0x0005_F05F
DcsmCommonRegs	DCSM_COMMON_REGS	0x0005_F070	0x0005_F07F
MemCfgRegs	MEM_CFG_REGS	0x0005_F400	0x0005_F47F
Emif1ConfigRegs	EMIF1_CONFIG_REGS	0x0005_F480	0x0005_F49F
Emif2ConfigRegs	EMIF2_CONFIG_REGS	0x0005_F4A0	0x0005_F4BF
AccessProtectionRegs	ACCESS_PROTECTION_REGS	0x0005_F4C0	0x0005_F4FF
MemoryErrorRegs	MEMORY_ERROR_REGS	0x0005_F500	0x0005_F53F
RomWaitStateRegs ⁽¹⁾	ROM_WAIT_STATE_REGS	0x0005_F540	0x0005_F541
FlashCtrlRegs	FLASH_CTRL_REGS	0x0005_F800	0x0005_FAFF
FlashEccRegs	FLASH_ECC_REGS	0x0005_FB00	0x0005_FB3F

⁽¹⁾ Only available on CPU1.

1.14.2 CPU_TIMER_REGS Registers

Table 1-20 lists the memory-mapped registers for the CPU_TIMER_REGS. All register offset addresses not listed in **Table 1-20** should be considered as reserved locations and the register contents should not be modified.

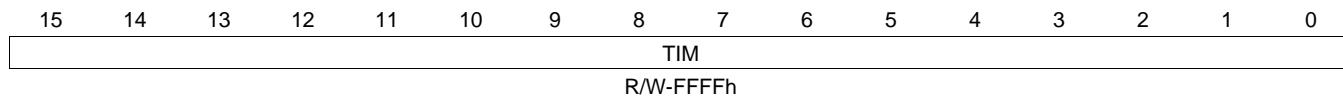
Table 1-20. CPU_TIMER_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	TIM	CPU-Timer, Counter Register	Section 1.14.2.1	
1h	TIMH	CPU-Timer, Counter Register High	Section 1.14.2.2	
2h	PRD	CPU-Timer, Period Register	Section 1.14.2.3	
3h	PRDH	CPU-Timer, Period Register High	Section 1.14.2.4	
4h	TCR	CPU-Timer, Control Register	Section 1.14.2.5	
6h	TPR	CPU-Timer, Prescale Register	Section 1.14.2.6	
7h	TPRH	CPU-Timer, Prescale Register High	Section 1.14.2.7	

1.14.2.1 TIM Register (offset = 0h) [reset = FFFFh]

TIM is shown in [Figure 1-30](#) and described in [Table 1-21](#).

CPU-Timer, Counter Register

Figure 1-30. TIM Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-21. TIM Register Field Descriptions

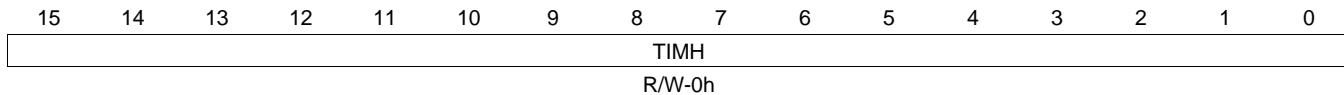
Bit	Field	Type	Reset	Description
15-0	TIM	R/W	FFFFh	CPU-Timer Counter Registers The TIM register holds the low 16 bits of the current 32-bit count of the timer. The TIMH:TIM decrements by one every (TDDRH:TDDR+1) clock cycles, where TDDRH:TDDR is the timer prescale dividen down value. When the TIMH:TIM decrements to zero, the TIMH:TIM register is reloaded with the period value contained in the PRDH:PRD registers. The timer interrupt (TINT) signal is generated.

1.14.2.2 TIMH Register (offset = 1h) [reset = 0h]

TIMH is shown in [Figure 1-31](#) and described in [Table 1-22](#).

CPU-Timer, Counter Register High

Figure 1-31. TIMH Register



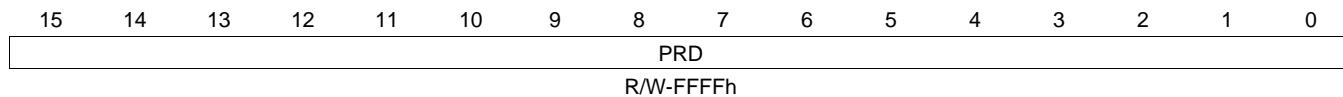
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-22. TIMH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TIMH	R/W	0h	<p>CPU-Timer Counter Registers</p> <p>The TIMH register holds the high 16 bits of the current 32-bit count of the timer. The TIMH:TIM decrements by one every (TDDRH:TDDR+1) clock cycles, where TDDRH:TDDR is the timer prescale dividedown value. When the TIMH:TIM decrements to zero, the TIMH:TIM register is reloaded with the period value contained in the PRDH:PRD registers. The timer interrupt (TINT) signal is generated.</p>

1.14.2.3 PRD Register (offset = 2h) [reset = FFFFh]PRD is shown in [Figure 1-32](#) and described in [Table 1-23](#).

CPU-Timer, Period Register

Figure 1-32. PRD Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

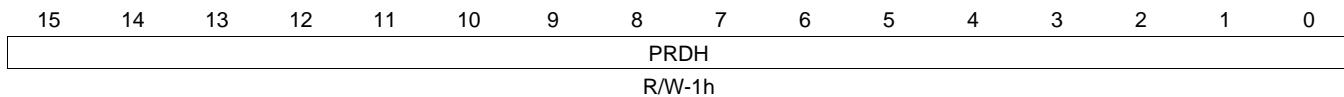
Table 1-23. PRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRD	R/W	FFFFh	CPU-Timer Counter Registers The PRD register holds the low 16 bits of the 32-bit period. When the TIMH:TIM decrements to zero, the TIMH:TIM register is reloaded with the period value contained in the PRDH:PRD registers, at the start of the next timer input clock cycle (the output of the prescaler). The PRDH:PRD contents are also loaded into the TIMH:TIM when you set the timer reload bit (TRB) in the Timer Control Register (TCR).

1.14.2.4 PRDH Register (offset = 3h) [reset = 1h]

PRDH is shown in [Figure 1-33](#) and described in [Table 1-24](#).

CPU-Timer, Period Register High

Figure 1-33. PRDH Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-24. PRDH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRDH	R/W	1h	<p>CPU-Timer Counter Registers</p> <p>The PRDH register holds the high 16 bits of the 32-bit period. When the TIMH:TIM decrements to zero, the TIMH:TIM register is reloaded with the period value contained in the PRDH:PRD registers, at the start of the next timer input clock cycle (the output of the prescaler). The PRDH:PRD contents are also loaded into the TIMH:TIM when you set the timer reload bit (TRB) in the Timer Control Register (TCR).</p>

1.14.2.5 TCR Register (offset = 4h) [reset = 1h]

TCR is shown in [Figure 1-34](#) and described in [Table 1-25](#).

CPU-Timer, Control Register

Figure 1-34. TCR Register

15	14	13	12	11	10	9	8
TIF	TIE	RESERVED		FREE_SOFT		RESERVED	
R/W1toClr-0h	R/W-0h	R-0h		R/W-0h		R-0h	
7	6	5	4	3	2	1	0
RESERVED	TRB	TSS		RESERVED		R-1h	
R-0h	R/W-0h	R/W-0h					

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-25. TCR Register Field Descriptions

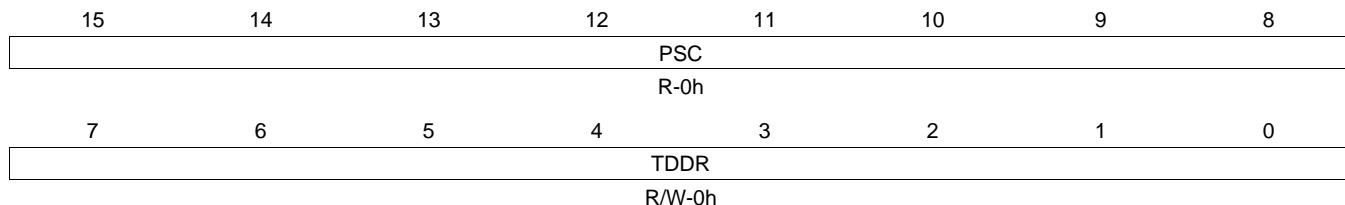
Bit	Field	Type	Reset	Description
15	TIF	R/W1toClr	0h	CPU-Timer Overflow Flag. TIF indicates whether a timer overflow has happened since TIF was last cleared. TIF is not cleared automatically and does not need to be cleared to enable the next timer interrupt. 0h (R/W) = The CPU-Timer has not decremented to zero. Writes of 0 are ignored. 1h (R/W) = This flag gets set when the CPU-timer decrements to zero. Writing a 1 to this bit clears the flag.
14	TIE	R/W	0h	CPU-Timer Interrupt Enable. 0h (R/W) = The CPU-Timer interrupt is disabled. 1h (R/W) = The CPU-Timer interrupt is enabled. If the timer decrements to zero, and TIE is set, the timer asserts its interrupt request.
13-12	RESERVED	R	0h	Reserved
11-10	FREE_SOFT	R/W	0h	CPU-Timer Emulation Modes: These bits are special emulation bits that determine the SOFT state of the timer when a breakpoint is encountered in the high-level language debugger. If the FREE bit is set to 1, then, upon a software breakpoint, the timer continues to run (that is, free runs). In this case, SOFT is a don't care. But if FREE is 0, then SOFT takes effect. In this case, if SOFT = 0, the timer halts the next time the TIMH:TIM decrements. If the SOFT bit is 1, then the timer halts when the TIMH:TIM has decremented to zero. 0h (R/W) = Stop after the next decrement of the TIMH:TIM (hard stop) 1h (R/W) = Stop after the TIMH:TIM decrements to 0 (soft stop) In the SOFT STOP mode, the timer generates an interrupt before shutting down (since reaching 0 is the interrupt causing condition). 2h (R/W) = Free run 3h (R/W) = Free run
9-6	RESERVED	R	0h	Reserved

Table 1-25. TCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TRB	R/W	0h	<p>Timer reload</p> <p>0h (R/W) = The TRB bit is always read as zero. Writes of 0 are ignored.</p> <p>1h (R/W) = When you write a 1 to TRB, the TIMH:TIM is loaded with the value in the PRDH:PRD, and the prescaler counter (PSCH:PSC) is loaded with the value in the timer dividedown register (TDDRH:TDDR).</p>
4	TSS	R/W	0h	<p>CPU-Timer stop status bit.</p> <p>TSS is a 1-bit flag that stops or starts the CPU-timer.</p> <p>0h (R/W) = Reads of 0 indicate the CPU-timer is running.</p> <p>To start or restart the CPU-timer, set TSS to 0. At reset, TSS is cleared to 0 and the CPU-timer immediately starts.</p> <p>1h (R/W) = Reads of 1 indicate that the CPU-timer is stopped.</p> <p>To stop the CPU-timer, set TSS to 1.</p>
3-0	RESERVED	R	1h	Reserved

1.14.2.6 TPR Register (offset = 6h) [reset = 0h]TPR is shown in [Figure 1-35](#) and described in [Table 1-26](#).

CPU-Timer, Prescale Register

Figure 1-35. TPR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

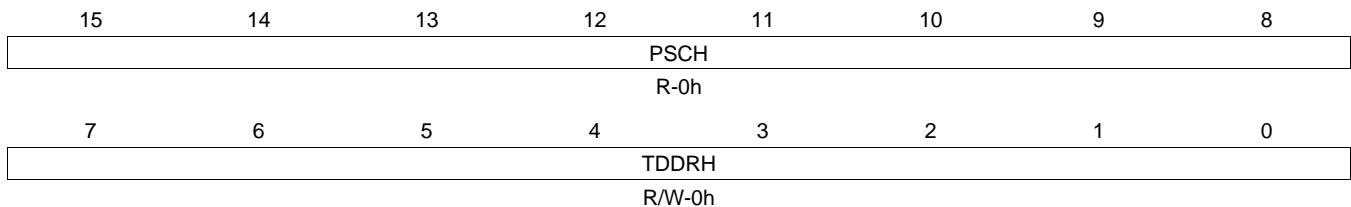
Table 1-26. TPR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PSC	R	0h	CPU-Timer Prescale Counter. These bits hold the current prescale count for the timer. For every timer clock source cycle that the PSCH:PSC value is greater than 0, the PSCH:PSC decrements by one. One timer clock (output of the timer prescaler) cycle after the PSCH:PSC reaches 0, the PSCH:PSC is loaded with the contents of the TDDRH:TDDR, and the timer counter register (TIMH:TIM) decrements by one. The PSCH:PSC is also reloaded whenever the timer reload bit (TRB) is set by software. The PSCH:PSC can be checked by reading the register, but it cannot be set directly. It must get its value from the timer divide-down register (TDDRH:TDDR). At reset, the PSCH:PSC is set to 0.
7-0	TDDR	R/W	0h	CPU-Timer Divide-Down. Every (TDDRH:TDDR + 1) timer clock source cycles, the timer counter register (TIMH:TIM) decrements by one. At reset, the TDDRH:TDDR bits are cleared to 0. To increase the overall timer count by an integer factor, write this factor minus one to the TDDRH:TDDR bits. When the prescaler counter (PSCH:PSC) value is 0, one timer clock source cycle later, the contents of the TDDRH:TDDR reload the PSCH:PSC, and the TIMH:TIM decrements by one. TDDRH:TDDR also reloads the PSCH:PSC whenever the timer reload bit (TRB) is set by software.

1.14.2.7 TPRH Register (offset = 7h) [reset = 0h]

TPRH is shown in [Figure 1-36](#) and described in [Table 1-27](#).

CPU-Timer, Prescale Register High

Figure 1-36. TPRH Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-27. TPRH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PSCH	R	0h	See description of TIMERxTPR.
7-0	TDDRH	R/W	0h	See description of TIMERxTPR.

1.14.3 PIE_CTRL_REGS Registers

Table 1-28 lists the memory-mapped registers for the PIE_CTRL_REGS. All register offset addresses not listed in Table 1-28 should be considered as reserved locations and the register contents should not be modified.

Table 1-28. PIE_CTRL_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	PIECTRL	Control Register	Section 1.14.3.1	
1h	PIEACK	Acknowledge Register	Section 1.14.3.2	
2h	PIEIER1	INT1 Group Enable Register	Section 1.14.3.3	
3h	PIEIFR1	INT1 Group Flag Register	Section 1.14.3.4	
4h	PIEIER2	INT2 Group Enable Register	Section 1.14.3.5	
5h	PIEIFR2	INT2 Group Flag Register	Section 1.14.3.6	
6h	PIEIER3	INT3 Group Enable Register	Section 1.14.3.7	
7h	PIEIFR3	INT3 Group Flag Register	Section 1.14.3.8	
8h	PIEIER4	INT4 Group Enable Register	Section 1.14.3.9	
9h	PIEIFR4	INT4 Group Flag Register	Section 1.14.3.10	
Ah	PIEIER5	INT5 Group Enable Register	Section 1.14.3.11	
Bh	PIEIFR5	INT5 Group Flag Register	Section 1.14.3.12	
Ch	PIEIER6	INT6 Group Enable Register	Section 1.14.3.13	
Dh	PIEIFR6	INT6 Group Flag Register	Section 1.14.3.14	
Eh	PIEIER7	INT7 Group Enable Register	Section 1.14.3.15	
Fh	PIEIFR7	INT7 Group Flag Register	Section 1.14.3.16	
10h	PIEIER8	INT8 Group Enable Register	Section 1.14.3.17	
11h	PIEIFR8	INT8 Group Flag Register	Section 1.14.3.18	
12h	PIEIER9	INT9 Group Enable Register	Section 1.14.3.19	
13h	PIEIFR9	INT9 Group Flag Register	Section 1.14.3.20	
14h	PIEIER10	INT10 Group Enable Register	Section 1.14.3.21	
15h	PIEIFR10	INT10 Group Flag Register	Section 1.14.3.22	
16h	PIEIER11	INT11 Group Enable Register	Section 1.14.3.23	
17h	PIEIFR11	INT11 Group Flag Register	Section 1.14.3.24	
18h	PIEIER12	INT12 Group Enable Register	Section 1.14.3.25	
19h	PIEIFR12	INT12 Group Flag Register	Section 1.14.3.26	

1.14.3.1 PIECTRL Register (offset = 0h) [reset = 0h]

PIECTRL is shown in [Figure 1-37](#) and described in [Table 1-29](#).

Control Register

Figure 1-37. PIECTRL Register

15	14	13	12	11	10	9	8
PIEVECT							
R-0h							
7	6	5	4	3	2	1	0
PIEVECT							ENPIE
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-29. PIECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	PIEVECT	R	0h	These bits indicate the vector address of the vector fetched from the ePIE Vector Table. The least significant bit of the address is ignored and only bits 1 to 15 of the address is shown. The vector value can be read by the user to determine which interrupt generated the vector fetch.
0	ENPIE	R/W	0h	Enable vector fetching from ePIE block. When this bit is set to 1, all vectors are fetched from the ePIE vector table. If this bit is set to 0, the ePIE block is disabled and vectors are fetched as normal. All ePIE block registers (PIEACK, PIEIFR, PIEIER) can be accessed even when the ePIE block is disabled. Note: ,The state of this bit will be reflected on the ENPIES signal, which is an output from the ePIE block.

1.14.3.2 PIEACK Register (offset = 1h) [reset = 0h]

PIEACK is shown in [Figure 1-38](#) and described in [Table 1-30](#).

Acknowledge Register

Writing a 1 to the respective interrupt bit enables the ePIE block to drive a pulse into the core interrupts input, if an interrupt is pending on any of the group interrupts.

Reading this register indicates if an interrupt is pending in the respective group.

Note: Writes of 0 are ignored.

Figure 1-38. PIEACK Register

15	14	13	12	11	10	9	8
		RESERVED		ACK12	ACK11	ACK10	ACK9
		R=0-0h		R/W=1-0h	R/W=1-0h	R/W=1-0h	R/W=1-0h
7	6	5	4	3	2	1	0
ACK8	ACK7	ACK6	ACK5	ACK4	ACK3	ACK2	ACK1
R/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-30. PIEACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11	ACK12	R/W=1	0h	Acknowledge PIE Interrupt Group 12
10	ACK11	R/W=1	0h	Acknowledge PIE Interrupt Group 11
9	ACK10	R/W=1	0h	Acknowledge PIE Interrupt Group 10
8	ACK9	R/W=1	0h	Acknowledge PIE Interrupt Group 9
7	ACK8	R/W=1	0h	Acknowledge PIE Interrupt Group 8
6	ACK7	R/W=1	0h	Acknowledge PIE Interrupt Group 7
5	ACK6	R/W=1	0h	Acknowledge PIE Interrupt Group 6
4	ACK5	R/W=1	0h	Acknowledge PIE Interrupt Group 5
3	ACK4	R/W=1	0h	Acknowledge PIE Interrupt Group 4
2	ACK3	R/W=1	0h	Acknowledge PIE Interrupt Group 3
1	ACK2	R/W=1	0h	Acknowledge PIE Interrupt Group 2
0	ACK1	R/W=1	0h	Acknowledge PIE Interrupt Group 1

1.14.3.3 PIEIER1 Register (offset = 2h) [reset = 0h]

PIEIER1 is shown in [Figure 1-39](#) and described in [Table 1-31](#).

INT1 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-39. PIEIER1 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-31. PIEIER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT1.16
14	INTx15	R/W	0h	Interrupt Enable for INT1.15
13	INTx14	R/W	0h	Interrupt Enable for INT1.14
12	INTx13	R/W	0h	Interrupt Enable for INT1.13
11	INTx12	R/W	0h	Interrupt Enable for INT1.12
10	INTx11	R/W	0h	Interrupt Enable for INT1.11
9	INTx10	R/W	0h	Interrupt Enable for INT1.10
8	INTx9	R/W	0h	Interrupt Enable for INT1.9
7	INTx8	R/W	0h	Interrupt Enable for INT1.8
6	INTx7	R/W	0h	Interrupt Enable for INT1.7
5	INTx6	R/W	0h	Interrupt Enable for INT1.6
4	INTx5	R/W	0h	Interrupt Enable for INT1.5
3	INTx4	R/W	0h	Interrupt Enable for INT1.4
2	INTx3	R/W	0h	Interrupt Enable for INT1.3
1	INTx2	R/W	0h	Interrupt Enable for INT1.2
0	INTx1	R/W	0h	Interrupt Enable for INT1.1

1.14.3.4 PIEIFR1 Register (offset = 3h) [reset = 0h]

PIEIFR1 is shown in [Figure 1-40](#) and described in [Table 1-32](#).

INT1 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-40. PIEIFR1 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-32. PIEIFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT1.16
14	INTx15	R/W	0h	Interrupt Flag for INT1.15
13	INTx14	R/W	0h	Interrupt Flag for INT1.14
12	INTx13	R/W	0h	Interrupt Flag for INT1.13
11	INTx12	R/W	0h	Interrupt Flag for INT1.12
10	INTx11	R/W	0h	Interrupt Flag for INT1.11
9	INTx10	R/W	0h	Interrupt Flag for INT1.10
8	INTx9	R/W	0h	Interrupt Flag for INT1.9
7	INTx8	R/W	0h	Interrupt Flag for INT1.8
6	INTx7	R/W	0h	Interrupt Flag for INT1.7
5	INTx6	R/W	0h	Interrupt Flag for INT1.6
4	INTx5	R/W	0h	Interrupt Flag for INT1.5
3	INTx4	R/W	0h	Interrupt Flag for INT1.4
2	INTx3	R/W	0h	Interrupt Flag for INT1.3
1	INTx2	R/W	0h	Interrupt Flag for INT1.2
0	INTx1	R/W	0h	Interrupt Flag for INT1.1

1.14.3.5 PIEIER2 Register (offset = 4h) [reset = 0h]

PIEIER2 is shown in [Figure 1-41](#) and described in [Table 1-33](#).

INT2 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-41. PIEIER2 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-33. PIEIER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT2.16
14	INTx15	R/W	0h	Interrupt Enable for INT2.15
13	INTx14	R/W	0h	Interrupt Enable for INT2.14
12	INTx13	R/W	0h	Interrupt Enable for INT2.13
11	INTx12	R/W	0h	Interrupt Enable for INT2.12
10	INTx11	R/W	0h	Interrupt Enable for INT2.11
9	INTx10	R/W	0h	Interrupt Enable for INT2.10
8	INTx9	R/W	0h	Interrupt Enable for INT2.9
7	INTx8	R/W	0h	Interrupt Enable for INT2.8
6	INTx7	R/W	0h	Interrupt Enable for INT2.7
5	INTx6	R/W	0h	Interrupt Enable for INT2.6
4	INTx5	R/W	0h	Interrupt Enable for INT2.5
3	INTx4	R/W	0h	Interrupt Enable for INT2.4
2	INTx3	R/W	0h	Interrupt Enable for INT2.3
1	INTx2	R/W	0h	Interrupt Enable for INT2.2
0	INTx1	R/W	0h	Interrupt Enable for INT2.1

1.14.3.6 PIEIFR2 Register (offset = 5h) [reset = 0h]

PIEIFR2 is shown in [Figure 1-42](#) and described in [Table 1-34](#).

INT2 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-42. PIEIFR2 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-34. PIEIFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT2.16
14	INTx15	R/W	0h	Interrupt Flag for INT2.15
13	INTx14	R/W	0h	Interrupt Flag for INT2.14
12	INTx13	R/W	0h	Interrupt Flag for INT2.13
11	INTx12	R/W	0h	Interrupt Flag for INT2.12
10	INTx11	R/W	0h	Interrupt Flag for INT2.11
9	INTx10	R/W	0h	Interrupt Flag for INT2.10
8	INTx9	R/W	0h	Interrupt Flag for INT2.9
7	INTx8	R/W	0h	Interrupt Flag for INT2.8
6	INTx7	R/W	0h	Interrupt Flag for INT2.7
5	INTx6	R/W	0h	Interrupt Flag for INT2.6
4	INTx5	R/W	0h	Interrupt Flag for INT2.5
3	INTx4	R/W	0h	Interrupt Flag for INT2.4
2	INTx3	R/W	0h	Interrupt Flag for INT2.3
1	INTx2	R/W	0h	Interrupt Flag for INT2.2
0	INTx1	R/W	0h	Interrupt Flag for INT2.1

1.14.3.7 PIEIER3 Register (offset = 6h) [reset = 0h]

PIEIER3 is shown in [Figure 1-43](#) and described in [Table 1-35](#).

INT3 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-43. PIEIER3 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-35. PIEIER3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT3.16
14	INTx15	R/W	0h	Interrupt Enable for INT3.15
13	INTx14	R/W	0h	Interrupt Enable for INT3.14
12	INTx13	R/W	0h	Interrupt Enable for INT3.13
11	INTx12	R/W	0h	Interrupt Enable for INT3.12
10	INTx11	R/W	0h	Interrupt Enable for INT3.11
9	INTx10	R/W	0h	Interrupt Enable for INT3.10
8	INTx9	R/W	0h	Interrupt Enable for INT3.9
7	INTx8	R/W	0h	Interrupt Enable for INT3.8
6	INTx7	R/W	0h	Interrupt Enable for INT3.7
5	INTx6	R/W	0h	Interrupt Enable for INT3.6
4	INTx5	R/W	0h	Interrupt Enable for INT3.5
3	INTx4	R/W	0h	Interrupt Enable for INT3.4
2	INTx3	R/W	0h	Interrupt Enable for INT3.3
1	INTx2	R/W	0h	Interrupt Enable for INT3.2
0	INTx1	R/W	0h	Interrupt Enable for INT3.1

1.14.3.8 PIEIFR3 Register (offset = 7h) [reset = 0h]

PIEIFR3 is shown in [Figure 1-44](#) and described in [Table 1-36](#).

INT3 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-44. PIEIFR3 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-36. PIEIFR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT3.16
14	INTx15	R/W	0h	Interrupt Flag for INT3.15
13	INTx14	R/W	0h	Interrupt Flag for INT3.14
12	INTx13	R/W	0h	Interrupt Flag for INT3.13
11	INTx12	R/W	0h	Interrupt Flag for INT3.12
10	INTx11	R/W	0h	Interrupt Flag for INT3.11
9	INTx10	R/W	0h	Interrupt Flag for INT3.10
8	INTx9	R/W	0h	Interrupt Flag for INT3.9
7	INTx8	R/W	0h	Interrupt Flag for INT3.8
6	INTx7	R/W	0h	Interrupt Flag for INT3.7
5	INTx6	R/W	0h	Interrupt Flag for INT3.6
4	INTx5	R/W	0h	Interrupt Flag for INT3.5
3	INTx4	R/W	0h	Interrupt Flag for INT3.4
2	INTx3	R/W	0h	Interrupt Flag for INT3.3
1	INTx2	R/W	0h	Interrupt Flag for INT3.2
0	INTx1	R/W	0h	Interrupt Flag for INT3.1

1.14.3.9 PIEIER4 Register (offset = 8h) [reset = 0h]

PIEIER4 is shown in [Figure 1-45](#) and described in [Table 1-37](#).

INT4 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-45. PIEIER4 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-37. PIEIER4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT4.16
14	INTx15	R/W	0h	Interrupt Enable for INT4.15
13	INTx14	R/W	0h	Interrupt Enable for INT4.14
12	INTx13	R/W	0h	Interrupt Enable for INT4.13
11	INTx12	R/W	0h	Interrupt Enable for INT4.12
10	INTx11	R/W	0h	Interrupt Enable for INT4.11
9	INTx10	R/W	0h	Interrupt Enable for INT4.10
8	INTx9	R/W	0h	Interrupt Enable for INT4.9
7	INTx8	R/W	0h	Interrupt Enable for INT4.8
6	INTx7	R/W	0h	Interrupt Enable for INT4.7
5	INTx6	R/W	0h	Interrupt Enable for INT4.6
4	INTx5	R/W	0h	Interrupt Enable for INT4.5
3	INTx4	R/W	0h	Interrupt Enable for INT4.4
2	INTx3	R/W	0h	Interrupt Enable for INT4.3
1	INTx2	R/W	0h	Interrupt Enable for INT4.2
0	INTx1	R/W	0h	Interrupt Enable for INT4.1

1.14.3.10 PIEIFR4 Register (offset = 9h) [reset = 0h]

PIEIFR4 is shown in [Figure 1-46](#) and described in [Table 1-38](#).

INT4 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-46. PIEIFR4 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-38. PIEIFR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT4.16
14	INTx15	R/W	0h	Interrupt Flag for INT4.15
13	INTx14	R/W	0h	Interrupt Flag for INT4.14
12	INTx13	R/W	0h	Interrupt Flag for INT4.13
11	INTx12	R/W	0h	Interrupt Flag for INT4.12
10	INTx11	R/W	0h	Interrupt Flag for INT4.11
9	INTx10	R/W	0h	Interrupt Flag for INT4.10
8	INTx9	R/W	0h	Interrupt Flag for INT4.9
7	INTx8	R/W	0h	Interrupt Flag for INT4.8
6	INTx7	R/W	0h	Interrupt Flag for INT4.7
5	INTx6	R/W	0h	Interrupt Flag for INT4.6
4	INTx5	R/W	0h	Interrupt Flag for INT4.5
3	INTx4	R/W	0h	Interrupt Flag for INT4.4
2	INTx3	R/W	0h	Interrupt Flag for INT4.3
1	INTx2	R/W	0h	Interrupt Flag for INT4.2
0	INTx1	R/W	0h	Interrupt Flag for INT4.1

1.14.3.11 PIEIER5 Register (offset = Ah) [reset = 0h]

PIEIER5 is shown in [Figure 1-47](#) and described in [Table 1-39](#).

INT5 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-47. PIEIER5 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-39. PIEIER5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT5.16
14	INTx15	R/W	0h	Interrupt Enable for INT5.15
13	INTx14	R/W	0h	Interrupt Enable for INT5.14
12	INTx13	R/W	0h	Interrupt Enable for INT5.13
11	INTx12	R/W	0h	Interrupt Enable for INT5.12
10	INTx11	R/W	0h	Interrupt Enable for INT5.11
9	INTx10	R/W	0h	Interrupt Enable for INT5.10
8	INTx9	R/W	0h	Interrupt Enable for INT5.9
7	INTx8	R/W	0h	Interrupt Enable for INT5.8
6	INTx7	R/W	0h	Interrupt Enable for INT5.7
5	INTx6	R/W	0h	Interrupt Enable for INT5.6
4	INTx5	R/W	0h	Interrupt Enable for INT5.5
3	INTx4	R/W	0h	Interrupt Enable for INT5.4
2	INTx3	R/W	0h	Interrupt Enable for INT5.3
1	INTx2	R/W	0h	Interrupt Enable for INT5.2
0	INTx1	R/W	0h	Interrupt Enable for INT5.1

1.14.3.12 PIEIFR5 Register (offset = Bh) [reset = 0h]

PIEIFR5 is shown in [Figure 1-48](#) and described in [Table 1-40](#).

INT5 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-48. PIEIFR5 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-40. PIEIFR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT5.16
14	INTx15	R/W	0h	Interrupt Flag for INT5.15
13	INTx14	R/W	0h	Interrupt Flag for INT5.14
12	INTx13	R/W	0h	Interrupt Flag for INT5.13
11	INTx12	R/W	0h	Interrupt Flag for INT5.12
10	INTx11	R/W	0h	Interrupt Flag for INT5.11
9	INTx10	R/W	0h	Interrupt Flag for INT5.10
8	INTx9	R/W	0h	Interrupt Flag for INT5.9
7	INTx8	R/W	0h	Interrupt Flag for INT5.8
6	INTx7	R/W	0h	Interrupt Flag for INT5.7
5	INTx6	R/W	0h	Interrupt Flag for INT5.6
4	INTx5	R/W	0h	Interrupt Flag for INT5.5
3	INTx4	R/W	0h	Interrupt Flag for INT5.4
2	INTx3	R/W	0h	Interrupt Flag for INT5.3
1	INTx2	R/W	0h	Interrupt Flag for INT5.2
0	INTx1	R/W	0h	Interrupt Flag for INT5.1

1.14.3.13 PIEIER6 Register (offset = Ch) [reset = 0h]

PIEIER6 is shown in [Figure 1-49](#) and described in [Table 1-41](#).

INT6 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-49. PIEIER6 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-41. PIEIER6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT6.16
14	INTx15	R/W	0h	Interrupt Enable for INT6.15
13	INTx14	R/W	0h	Interrupt Enable for INT6.14
12	INTx13	R/W	0h	Interrupt Enable for INT6.13
11	INTx12	R/W	0h	Interrupt Enable for INT6.12
10	INTx11	R/W	0h	Interrupt Enable for INT6.11
9	INTx10	R/W	0h	Interrupt Enable for INT6.10
8	INTx9	R/W	0h	Interrupt Enable for INT6.9
7	INTx8	R/W	0h	Interrupt Enable for INT6.8
6	INTx7	R/W	0h	Interrupt Enable for INT6.7
5	INTx6	R/W	0h	Interrupt Enable for INT6.6
4	INTx5	R/W	0h	Interrupt Enable for INT6.5
3	INTx4	R/W	0h	Interrupt Enable for INT6.4
2	INTx3	R/W	0h	Interrupt Enable for INT6.3
1	INTx2	R/W	0h	Interrupt Enable for INT6.2
0	INTx1	R/W	0h	Interrupt Enable for INT6.1

1.14.3.14 PIEIFR6 Register (offset = Dh) [reset = 0h]

PIEIFR6 is shown in [Figure 1-50](#) and described in [Table 1-42](#).

INT6 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-50. PIEIFR6 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-42. PIEIFR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT6.16
14	INTx15	R/W	0h	Interrupt Flag for INT6.15
13	INTx14	R/W	0h	Interrupt Flag for INT6.14
12	INTx13	R/W	0h	Interrupt Flag for INT6.13
11	INTx12	R/W	0h	Interrupt Flag for INT6.12
10	INTx11	R/W	0h	Interrupt Flag for INT6.11
9	INTx10	R/W	0h	Interrupt Flag for INT6.10
8	INTx9	R/W	0h	Interrupt Flag for INT6.9
7	INTx8	R/W	0h	Interrupt Flag for INT6.8
6	INTx7	R/W	0h	Interrupt Flag for INT6.7
5	INTx6	R/W	0h	Interrupt Flag for INT6.6
4	INTx5	R/W	0h	Interrupt Flag for INT6.5
3	INTx4	R/W	0h	Interrupt Flag for INT6.4
2	INTx3	R/W	0h	Interrupt Flag for INT6.3
1	INTx2	R/W	0h	Interrupt Flag for INT6.2
0	INTx1	R/W	0h	Interrupt Flag for INT6.1

1.14.3.15 PIEIER7 Register (offset = Eh) [reset = 0h]

PIEIER7 is shown in [Figure 1-51](#) and described in [Table 1-43](#).

INT7 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-51. PIEIER7 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-43. PIEIER7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT7.16
14	INTx15	R/W	0h	Interrupt Enable for INT7.15
13	INTx14	R/W	0h	Interrupt Enable for INT7.14
12	INTx13	R/W	0h	Interrupt Enable for INT7.13
11	INTx12	R/W	0h	Interrupt Enable for INT7.12
10	INTx11	R/W	0h	Interrupt Enable for INT7.11
9	INTx10	R/W	0h	Interrupt Enable for INT7.10
8	INTx9	R/W	0h	Interrupt Enable for INT7.9
7	INTx8	R/W	0h	Interrupt Enable for INT7.8
6	INTx7	R/W	0h	Interrupt Enable for INT7.7
5	INTx6	R/W	0h	Interrupt Enable for INT7.6
4	INTx5	R/W	0h	Interrupt Enable for INT7.5
3	INTx4	R/W	0h	Interrupt Enable for INT7.4
2	INTx3	R/W	0h	Interrupt Enable for INT7.3
1	INTx2	R/W	0h	Interrupt Enable for INT7.2
0	INTx1	R/W	0h	Interrupt Enable for INT7.1

1.14.3.16 PIEIFR7 Register (offset = Fh) [reset = 0h]

PIEIFR7 is shown in [Figure 1-52](#) and described in [Table 1-44](#).

INT7 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-52. PIEIFR7 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-44. PIEIFR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT7.16
14	INTx15	R/W	0h	Interrupt Flag for INT7.15
13	INTx14	R/W	0h	Interrupt Flag for INT7.14
12	INTx13	R/W	0h	Interrupt Flag for INT7.13
11	INTx12	R/W	0h	Interrupt Flag for INT7.12
10	INTx11	R/W	0h	Interrupt Flag for INT7.11
9	INTx10	R/W	0h	Interrupt Flag for INT7.10
8	INTx9	R/W	0h	Interrupt Flag for INT7.9
7	INTx8	R/W	0h	Interrupt Flag for INT7.8
6	INTx7	R/W	0h	Interrupt Flag for INT7.7
5	INTx6	R/W	0h	Interrupt Flag for INT7.6
4	INTx5	R/W	0h	Interrupt Flag for INT7.5
3	INTx4	R/W	0h	Interrupt Flag for INT7.4
2	INTx3	R/W	0h	Interrupt Flag for INT7.3
1	INTx2	R/W	0h	Interrupt Flag for INT7.2
0	INTx1	R/W	0h	Interrupt Flag for INT7.1

1.14.3.17 PIEIER8 Register (offset = 10h) [reset = 0h]

PIEIER8 is shown in [Figure 1-53](#) and described in [Table 1-45](#).

INT8 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-53. PIEIER8 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-45. PIEIER8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT8.16
14	INTx15	R/W	0h	Interrupt Enable for INT8.15
13	INTx14	R/W	0h	Interrupt Enable for INT8.14
12	INTx13	R/W	0h	Interrupt Enable for INT8.13
11	INTx12	R/W	0h	Interrupt Enable for INT8.12
10	INTx11	R/W	0h	Interrupt Enable for INT8.11
9	INTx10	R/W	0h	Interrupt Enable for INT8.10
8	INTx9	R/W	0h	Interrupt Enable for INT8.9
7	INTx8	R/W	0h	Interrupt Enable for INT8.8
6	INTx7	R/W	0h	Interrupt Enable for INT8.7
5	INTx6	R/W	0h	Interrupt Enable for INT8.6
4	INTx5	R/W	0h	Interrupt Enable for INT8.5
3	INTx4	R/W	0h	Interrupt Enable for INT8.4
2	INTx3	R/W	0h	Interrupt Enable for INT8.3
1	INTx2	R/W	0h	Interrupt Enable for INT8.2
0	INTx1	R/W	0h	Interrupt Enable for INT8.1

1.14.3.18 PIEIFR8 Register (offset = 11h) [reset = 0h]

PIEIFR8 is shown in [Figure 1-54](#) and described in [Table 1-46](#).

INT8 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-54. PIEIFR8 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 1-46. PIEIFR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT8.16
14	INTx15	R/W	0h	Interrupt Flag for INT8.15
13	INTx14	R/W	0h	Interrupt Flag for INT8.14
12	INTx13	R/W	0h	Interrupt Flag for INT8.13
11	INTx12	R/W	0h	Interrupt Flag for INT8.12
10	INTx11	R/W	0h	Interrupt Flag for INT8.11
9	INTx10	R/W	0h	Interrupt Flag for INT8.10
8	INTx9	R/W	0h	Interrupt Flag for INT8.9
7	INTx8	R/W	0h	Interrupt Flag for INT8.8
6	INTx7	R/W	0h	Interrupt Flag for INT8.7
5	INTx6	R/W	0h	Interrupt Flag for INT8.6
4	INTx5	R/W	0h	Interrupt Flag for INT8.5
3	INTx4	R/W	0h	Interrupt Flag for INT8.4
2	INTx3	R/W	0h	Interrupt Flag for INT8.3
1	INTx2	R/W	0h	Interrupt Flag for INT8.2
0	INTx1	R/W	0h	Interrupt Flag for INT8.1

1.14.3.19 PIEIER9 Register (offset = 12h) [reset = 0h]

PIEIER9 is shown in [Figure 1-55](#) and described in [Table 1-47](#).

INT9 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-55. PIEIER9 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-47. PIEIER9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT9.16
14	INTx15	R/W	0h	Interrupt Enable for INT9.15
13	INTx14	R/W	0h	Interrupt Enable for INT9.14
12	INTx13	R/W	0h	Interrupt Enable for INT9.13
11	INTx12	R/W	0h	Interrupt Enable for INT9.12
10	INTx11	R/W	0h	Interrupt Enable for INT9.11
9	INTx10	R/W	0h	Interrupt Enable for INT9.10
8	INTx9	R/W	0h	Interrupt Enable for INT9.9
7	INTx8	R/W	0h	Interrupt Enable for INT9.8
6	INTx7	R/W	0h	Interrupt Enable for INT9.7
5	INTx6	R/W	0h	Interrupt Enable for INT9.6
4	INTx5	R/W	0h	Interrupt Enable for INT9.5
3	INTx4	R/W	0h	Interrupt Enable for INT9.4
2	INTx3	R/W	0h	Interrupt Enable for INT9.3
1	INTx2	R/W	0h	Interrupt Enable for INT9.2
0	INTx1	R/W	0h	Interrupt Enable for INT9.1

1.14.3.20 PIEIFR9 Register (offset = 13h) [reset = 0h]

PIEIFR9 is shown in [Figure 1-56](#) and described in [Table 1-48](#).

INT9 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-56. PIEIFR9 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 1-48. PIEIFR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT9.16
14	INTx15	R/W	0h	Interrupt Flag for INT9.15
13	INTx14	R/W	0h	Interrupt Flag for INT9.14
12	INTx13	R/W	0h	Interrupt Flag for INT9.13
11	INTx12	R/W	0h	Interrupt Flag for INT9.12
10	INTx11	R/W	0h	Interrupt Flag for INT9.11
9	INTx10	R/W	0h	Interrupt Flag for INT9.10
8	INTx9	R/W	0h	Interrupt Flag for INT9.9
7	INTx8	R/W	0h	Interrupt Flag for INT9.8
6	INTx7	R/W	0h	Interrupt Flag for INT9.7
5	INTx6	R/W	0h	Interrupt Flag for INT9.6
4	INTx5	R/W	0h	Interrupt Flag for INT9.5
3	INTx4	R/W	0h	Interrupt Flag for INT9.4
2	INTx3	R/W	0h	Interrupt Flag for INT9.3
1	INTx2	R/W	0h	Interrupt Flag for INT9.2
0	INTx1	R/W	0h	Interrupt Flag for INT9.1

1.14.3.21 PIEIER10 Register (offset = 14h) [reset = 0h]

PIEIER10 is shown in [Figure 1-57](#) and described in [Table 1-49](#).

INT10 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-57. PIEIER10 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-49. PIEIER10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT10.16
14	INTx15	R/W	0h	Interrupt Enable for INT10.15
13	INTx14	R/W	0h	Interrupt Enable for INT10.14
12	INTx13	R/W	0h	Interrupt Enable for INT10.13
11	INTx12	R/W	0h	Interrupt Enable for INT10.12
10	INTx11	R/W	0h	Interrupt Enable for INT10.11
9	INTx10	R/W	0h	Interrupt Enable for INT10.10
8	INTx9	R/W	0h	Interrupt Enable for INT10.9
7	INTx8	R/W	0h	Interrupt Enable for INT10.8
6	INTx7	R/W	0h	Interrupt Enable for INT10.7
5	INTx6	R/W	0h	Interrupt Enable for INT10.6
4	INTx5	R/W	0h	Interrupt Enable for INT10.5
3	INTx4	R/W	0h	Interrupt Enable for INT10.4
2	INTx3	R/W	0h	Interrupt Enable for INT10.3
1	INTx2	R/W	0h	Interrupt Enable for INT10.2
0	INTx1	R/W	0h	Interrupt Enable for INT10.1

1.14.3.22 PIEIFR10 Register (offset = 15h) [reset = 0h]

PIEIFR10 is shown in [Figure 1-58](#) and described in [Table 1-50](#).

INT10 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-58. PIEIFR10 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-50. PIEIFR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT10.16
14	INTx15	R/W	0h	Interrupt Flag for INT10.15
13	INTx14	R/W	0h	Interrupt Flag for INT10.14
12	INTx13	R/W	0h	Interrupt Flag for INT10.13
11	INTx12	R/W	0h	Interrupt Flag for INT10.12
10	INTx11	R/W	0h	Interrupt Flag for INT10.11
9	INTx10	R/W	0h	Interrupt Flag for INT10.10
8	INTx9	R/W	0h	Interrupt Flag for INT10.9
7	INTx8	R/W	0h	Interrupt Flag for INT10.8
6	INTx7	R/W	0h	Interrupt Flag for INT10.7
5	INTx6	R/W	0h	Interrupt Flag for INT10.6
4	INTx5	R/W	0h	Interrupt Flag for INT10.5
3	INTx4	R/W	0h	Interrupt Flag for INT10.4
2	INTx3	R/W	0h	Interrupt Flag for INT10.3
1	INTx2	R/W	0h	Interrupt Flag for INT10.2
0	INTx1	R/W	0h	Interrupt Flag for INT10.1

1.14.3.23 PIEIER11 Register (offset = 16h) [reset = 0h]

PIEIER11 is shown in [Figure 1-59](#) and described in [Table 1-51](#).

INT11 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-59. PIEIER11 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-51. PIEIER11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT11.16
14	INTx15	R/W	0h	Interrupt Enable for INT11.15
13	INTx14	R/W	0h	Interrupt Enable for INT11.14
12	INTx13	R/W	0h	Interrupt Enable for INT11.13
11	INTx12	R/W	0h	Interrupt Enable for INT11.12
10	INTx11	R/W	0h	Interrupt Enable for INT11.11
9	INTx10	R/W	0h	Interrupt Enable for INT11.10
8	INTx9	R/W	0h	Interrupt Enable for INT11.9
7	INTx8	R/W	0h	Interrupt Enable for INT11.8
6	INTx7	R/W	0h	Interrupt Enable for INT11.7
5	INTx6	R/W	0h	Interrupt Enable for INT11.6
4	INTx5	R/W	0h	Interrupt Enable for INT11.5
3	INTx4	R/W	0h	Interrupt Enable for INT11.4
2	INTx3	R/W	0h	Interrupt Enable for INT11.3
1	INTx2	R/W	0h	Interrupt Enable for INT11.2
0	INTx1	R/W	0h	Interrupt Enable for INT11.1

1.14.3.24 PIEIFR11 Register (offset = 17h) [reset = 0h]

PIEIFR11 is shown in [Figure 1-60](#) and described in [Table 1-52](#).

INT11 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-60. PIEIFR11 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-52. PIEIFR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT11.16
14	INTx15	R/W	0h	Interrupt Flag for INT11.15
13	INTx14	R/W	0h	Interrupt Flag for INT11.14
12	INTx13	R/W	0h	Interrupt Flag for INT11.13
11	INTx12	R/W	0h	Interrupt Flag for INT11.12
10	INTx11	R/W	0h	Interrupt Flag for INT11.11
9	INTx10	R/W	0h	Interrupt Flag for INT11.10
8	INTx9	R/W	0h	Interrupt Flag for INT11.9
7	INTx8	R/W	0h	Interrupt Flag for INT11.8
6	INTx7	R/W	0h	Interrupt Flag for INT11.7
5	INTx6	R/W	0h	Interrupt Flag for INT11.6
4	INTx5	R/W	0h	Interrupt Flag for INT11.5
3	INTx4	R/W	0h	Interrupt Flag for INT11.4
2	INTx3	R/W	0h	Interrupt Flag for INT11.3
1	INTx2	R/W	0h	Interrupt Flag for INT11.2
0	INTx1	R/W	0h	Interrupt Flag for INT11.1

1.14.3.25 PIEIER12 Register (offset = 18h) [reset = 0h]

PIEIER12 is shown in [Figure 1-61](#) and described in [Table 1-53](#).

INT12 Group Enable Register

These register bits individually enable an interrupt within a group. They behave very much like the core interrupt enable register.

Setting a bit to 1 will enable the servicing of the respective interrupt.

Setting a bit to 0 will disable the servicing of the bit.

Figure 1-61. PIEIER12 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-53. PIEIER12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Enable for INT12.16
14	INTx15	R/W	0h	Interrupt Enable for INT12.15
13	INTx14	R/W	0h	Interrupt Enable for INT12.14
12	INTx13	R/W	0h	Interrupt Enable for INT12.13
11	INTx12	R/W	0h	Interrupt Enable for INT12.12
10	INTx11	R/W	0h	Interrupt Enable for INT12.11
9	INTx10	R/W	0h	Interrupt Enable for INT12.10
8	INTx9	R/W	0h	Interrupt Enable for INT12.9
7	INTx8	R/W	0h	Interrupt Enable for INT12.8
6	INTx7	R/W	0h	Interrupt Enable for INT12.7
5	INTx6	R/W	0h	Interrupt Enable for INT12.6
4	INTx5	R/W	0h	Interrupt Enable for INT12.5
3	INTx4	R/W	0h	Interrupt Enable for INT12.4
2	INTx3	R/W	0h	Interrupt Enable for INT12.3
1	INTx2	R/W	0h	Interrupt Enable for INT12.2
0	INTx1	R/W	0h	Interrupt Enable for INT12.1

1.14.3.26 PIEIFR12 Register (offset = 19h) [reset = 0h]

PIEIFR12 is shown in [Figure 1-62](#) and described in [Table 1-54](#).

INT12 Group Flag Register

These register bits indicate if an interrupt is currently active. They behave very much like the core interrupt flag register.

When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit.

This register can also be read to determine which interrupts are active or pending.

Figure 1-62. PIEIFR12 Register

15	14	13	12	11	10	9	8
INTx16	INTx15	INTx14	INTx13	INTx12	INTx11	INTx10	INTx9
R/W-0h							
7	6	5	4	3	2	1	0
INTx8	INTx7	INTx6	INTx5	INTx4	INTx3	INTx2	INTx1
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-54. PIEIFR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INTx16	R/W	0h	Interrupt Flag for INT12.16
14	INTx15	R/W	0h	Interrupt Flag for INT12.15
13	INTx14	R/W	0h	Interrupt Flag for INT12.14
12	INTx13	R/W	0h	Interrupt Flag for INT12.13
11	INTx12	R/W	0h	Interrupt Flag for INT12.12
10	INTx11	R/W	0h	Interrupt Flag for INT12.11
9	INTx10	R/W	0h	Interrupt Flag for INT12.10
8	INTx9	R/W	0h	Interrupt Flag for INT12.9
7	INTx8	R/W	0h	Interrupt Flag for INT12.8
6	INTx7	R/W	0h	Interrupt Flag for INT12.7
5	INTx6	R/W	0h	Interrupt Flag for INT12.6
4	INTx5	R/W	0h	Interrupt Flag for INT12.5
3	INTx4	R/W	0h	Interrupt Flag for INT12.4
2	INTx3	R/W	0h	Interrupt Flag for INT12.3
1	INTx2	R/W	0h	Interrupt Flag for INT12.2
0	INTx1	R/W	0h	Interrupt Flag for INT12.1

1.14.4 WD_REGS Registers

Table 1-55 lists the memory-mapped registers for the WD_REGS. All register offset addresses not listed in **Table 1-55** should be considered as reserved locations and the register contents should not be modified.

Table 1-55. WD_REGS REGISTERS

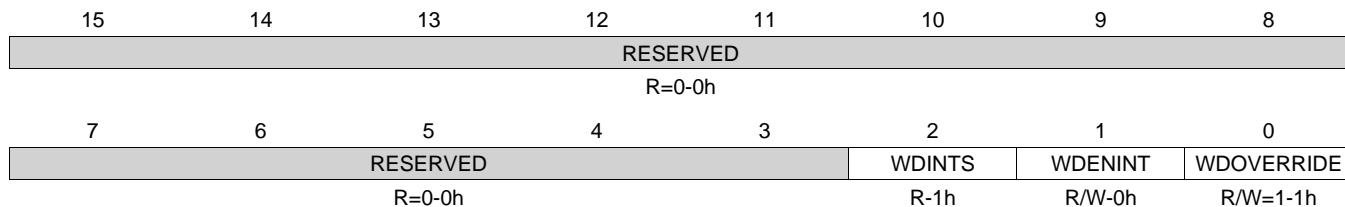
Offset	Acronym	Register Name	Section	Write Protection
22h	SCSR	System Control & Status Register	Section 1.14.4.1	EALLOW
23h	WDCNTR	Watchdog Counter Register	Section 1.14.4.2	EALLOW
25h	WDKEY	Watchdog Reset Key Register	Section 1.14.4.3	EALLOW
29h	WDCR	Watchdog Control Register	Section 1.14.4.4	EALLOW
2Ah	WDWCR	Watchdog Windowed Control Register	Section 1.14.4.5	EALLOW

1.14.4.1 SCSR Register (offset = 22h) [reset = 5h]

SCSR is shown in [Figure 1-63](#) and described in [Table 1-56](#).

System Control & Status Register

Figure 1-63. SCSR Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

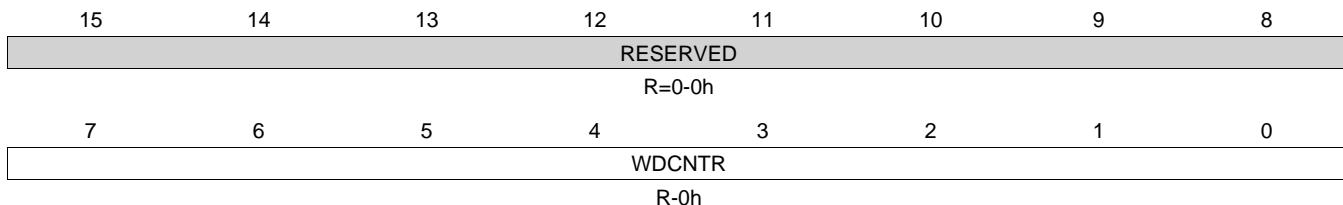
Table 1-56. SCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R=0	0h	Reserved
2	WDINTS	R	1h	Watchdog interrupt (WDINTn) status signal. This is a read only bit reflecting the current state of the WDINTn signal from the watchdog block (after synchronization with SYSCLKOUT). If this bit is 1, the watchdog interrupt is not active. If this bit is 0, then the watchdog interrupt is active. Note: If the WDINTn signal is used to wake up from IDLE or STANDBY condition, then the user should make sure that the WDINTn signal goes back high again before attempting to go back into IDLE or STANDBY mode. Reading this bit will tell the user the current state of this signal.
1	WDENINT	R/W	0h	If this bit is set to 1, the watchdog reset (WDRSTn) output signal is disabled and the watchdog interrupt (WDINTn) output signal is enabled. If this bit is zero, then the WDRSTn output signal is enabled and the WDINTn output signal is disabled. This is the default state on system reset (SYSRSn).
0	WDOVERRIDE	R/W=1	1h	If this bit is set to 1, the user is allowed to change the state of the Watchdog disable (WDDIS) bit in the Watchdog Control (WDCR) register (refer to Watchdog Block section of this spec). If the WDOVERRIDE bit is cleared, by writing a 1 the WDDIS bit cannot be modified by the user. Writing a 0 will have no effect. If this bit is cleared, then it will remain in this state until a reset occurs. The current state of this bit is readable by the user.

1.14.4.2 WDCNTR Register (offset = 23h) [reset = 0h]

WDCNTR is shown in [Figure 1-64](#) and described in [Table 1-57](#).

Watchdog Counter Register

Figure 1-64. WDCNTR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-57. WDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7-0	WDCNTR	R	0h	These bits contain the current value of the WD counter. The 8-bit counter continually increments at the WDCLK rate. If the counter overflows, then a watchdog output pulse (WDOUTn) is generated. If the WDKEY register is written with a valid combination, then the counter is reset to zero.

1.14.4.3 WDKEY Register (offset = 25h) [reset = 0h]WDKEY is shown in [Figure 1-65](#) and described in [Table 1-58](#).

Watchdog Reset Key Register

Figure 1-65. WDKEY Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-58. WDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7-0	WDKEY	R/W	0h	Writing 0x55 followed by 0xAA will cause the WDCNTR bits to be cleared. Note: [1] Reads from the WDKEY return the value of WDCR register.

1.14.4.4 WDCR Register (offset = 29h) [reset = 0h]

WDCR is shown in [Figure 1-66](#) and described in [Table 1-59](#).

Watchdog Control Register

Figure 1-66. WDCR Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
WDFLG	WDDIS		WDCHK		WDPS		
R/W=1-0h	R/W-0h		R=0/W-0h		R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

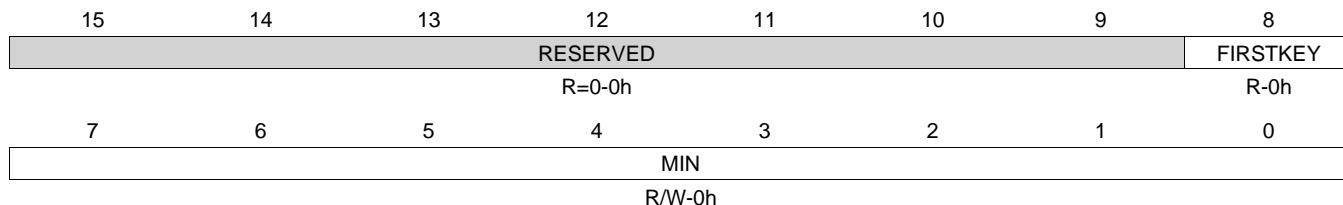
Table 1-59. WDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7	WDFLG	R/W=1	0h	Watchdog reset status flag bit. This bit, if set, indicates a watchdog reset (WDRSTn) generated the reset condition. If 0, then it was an external device or power-up reset condition. This bit remains latched until the user writes a 1 to clear the condition. Writes of 0 will be ignored.
6	WDDIS	R/W	0h	Writing a 1 to this bit will disable the watchdog module. Writing a 0 will enable the module. This bit can only be modified if the WDOVERRIDE bit in the SCSR2 register is set to 1. On reset, the watchdog module is enabled.
5-3	WDCHK	R=0/W	0h	The user must ALWAYS write 1,0,1 to these bits whenever a write to this register is performed. Writing any other value will cause an immediate reset to the core (if WD enabled).
2-0	WDPS	R/W	0h	These bits configure the watchdog counter clock (WDCLK) rate relative to OSCCLK/512: 000 WDCLK = OSCCLK/512/1 001 WDCLK = OSCCLK/512/1 010 WDCLK = OSCCLK/512/2 011 WDCLK = OSCCLK/512/4 100 WDCLK = OSCCLK/512/8 101 WDCLK = OSCCLK/512/16 110 WDCLK = OSCCLK/512/32 111 WDCLK = OSCCLK/512/64

1.14.4.5 WDWCR Register (offset = 2Ah) [reset = 0h]

WDWCR is shown in [Figure 1-67](#) and described in [Table 1-60](#).

Watchdog Windowed Control Register

Figure 1-67. WDWCR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-60. WDWCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R=0	0h	Reserved
8	FIRSTKEY	R	0h	<p>This bit indicates if the 1st valid WDKEY (0x55 + 0xAA) got detected after MIN was configured to a non-zero value</p> <p>0: First Valid Key after non-zero MIN configuration has not happened yet</p> <p>1: First Valid key after non-zero MIN configuration got detected</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If MIN = 0, this bit is never set [2] If MIN is changed back to 0x0 from a non-zero value, this bit is auto-cleared [3] This bit is added for debug purposes only
7-0	MIN	R/W	0h	These bits define the lower limit of the Windowed functionality

1.14.5 NMIINTERRUPT Registers

Table 1-61 lists the memory-mapped registers for the NMIINTERRUPT. All register offset addresses not listed in **Table 1-61** should be considered as reserved locations and the register contents should not be modified.

Table 1-61. NMIINTERRUPT REGISTERS

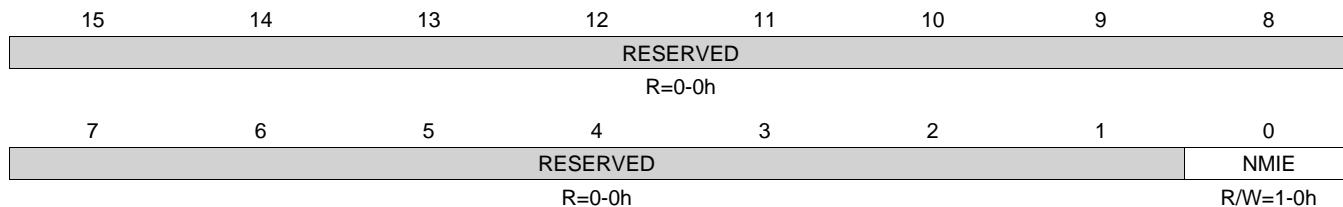
Offset	Acronym	Register Name	Section	Write Protection
0h	NMICFG	NMI Configuration Register	Section 1.14.5.1	EALLOW
1h	NMIFLG	NMI Flag Register (XRSn Clear)	Section 1.14.5.2	
2h	NMIFLGCLR	NMI Flag Clear Register	Section 1.14.5.3	EALLOW
3h	NMIFLGFRC	NMI Flag Force Register	Section 1.14.5.4	EALLOW
4h	NMIWDCNT	NMI Watchdog Counter Register	Section 1.14.5.5	
5h	NMIWDPRD	NMI Watchdog Period Register	Section 1.14.5.6	EALLOW
6h	NMISHDFLG	NMI Shadow Flag Register	Section 1.14.5.7	

1.14.5.1 NMICFG Register (offset = 0h) [reset = 0h]

NMICFG is shown in [Figure 1-68](#) and described in [Table 1-62](#).

NMI Configuration Register

Figure 1-68. NMICFG Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-62. NMICFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R=0	0h	Reserved
0	NMIE	R/W=1	0h	When set to 1 any condition will generate an NMI interrupt to the C28 CPU and kick off the NMI watchdog counter. As part of boot sequence this bit should be set after the device security related initialization is complete. 0 NMI disabled 1 NMI enabled

1.14.5.2 NMIFLG Register (offset = 1h) [reset = 0h]NMIFLG is shown in [Figure 1-69](#) and described in [Table 1-63](#).

NMI Flag Register (XRSn Clear)

Figure 1-69. NMIFLG Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED	CPU2NMIWDRSn	CPU2WDRSn	RESERVED
				R=0-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	PIEVECTERR	CPU2HWBISTERR	CPU1HWBISTERR	FLUNCERR	RAMUNCERR	CLOCKFAIL	NMIINT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-63. NMIFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11	RESERVED	R	0h	Reserved
10	CPU2NMIWDRSn	R	0h	CPU2 NMIWDRSn Reset Indication Flag: This bits indicates if CPU2s NMIWDRSn was fired or not. 0 No CPU2.NMIWDRSn was fired 1 CPU2.NMIWDRSn was fired to CPU2 Note: [1] This bits is reserved for CPU2.NMIFLG register
9	CPU2WDRSn	R	0h	CPU2 WDRSn Reset Indication Flag: This bits indicates if CPU2s WDRSn was fired or not. 0 No CPU2.WDRsn was fired 1 CPU2.WDRSn was fired to CPU2 Note: [1] This bits is reserved for CPU2.NMIFLG register
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	PIEVECTERR	R	0h	PIE Vector Fetch Error Flag: This bit indicates if an error occurred on an Vector Fect by the other CPU in the device. For example, CPU1.NMIWD gets an NMI on an Vector fetch Error on CPU2. This bit can only be cleared by the user writing to the corresponding clear bit in the NMIFLGCLR register or by an XRSn reset: 0,No Vector Fetch Error condition (on the other CPU) pending 1,Vector Fetch error condition (on the other CPU) generated
5	CPU2HWBISTERR	R	0h	HW BIST Error NMI Flag: This bit indicates if the time out error or a signature mismatch error condition during hardware BIST of C28 CPU2 occurred. This bit can only be cleared by the user writing to the corresponding clear bit in the NMIFLGCLR register or by an XRSn reset: 0,No C28 HWBIST error condition pending 1,C28 BIST error condition generated
4	CPU1HWBISTERR	R	0h	HW BIST Error NMI Flag: This bit indicates if the time out error or a signature mismatch error condition during hardware BIST of C28 CPU1 occurred. This bit can only be cleared by the user writing to the corresponding clear bit in the NMIFLGCLR register or by an XRSn reset: 0,No C28 HWBIST error condition pending 1,C28 BIST error condition generated

Table 1-63. NMIFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	FLUNCERR	R	0h	Flash Uncorrectable Error NMI Flag: This bit indicates if an uncorrectable error occurred on a C28 Flash access and that condition is latched. This bit can only be cleared by the user writing to the corresponding clear bit in the NMIFLGCLR register or by an XRSn reset: 0,No C28 Flash uncorrectable error condition pending 1,C28 Flash uncorrectable error condition generated
2	RAMUNCERR	R	0h	RAM Uncorrectable Error NMI Flag: This bit indicates if an uncorrectable error occurred on a RAM access (by any master) and that condition is latched. This bit can only be cleared by the user writing to the corresponding clear bit in the NMIFLGCLR register or by an XRSn reset: 0,No RAM uncorrectable error condition pending 1,RAM uncorrectable error condition generated
1	CLOCKFAIL	R	0h	Clock Fail Interrupt Flag: These bits indicates if the CLOCKFAIL condition is latched. These bits can only be cleared by the user writing to the respective bit in the NMIFLGCLR register or by an XRSn reset: 0,No CLOCKFAIL Condition Pending 1,CLOCKFAIL Condition Generated
0	NMIINT	R	0h	NMI Interrupt Flag: This bit indicates if an NMI interrupt was generated. This bit can only be cleared by the user writing to the respective bit in the NMIFLGCLR register or by an XRSn reset: 0 No NMI Interrupt Generated 1 NMI Interrupt Generated No further NMI interrupts pulses are generated until this flag is cleared by the user.

1.14.5.3 NMIFLGCLR Register (offset = 2h) [reset = 0h]

NMIFLGCLR is shown in [Figure 1-70](#) and described in [Table 1-64](#).

NMI Flag Clear Register

Figure 1-70. NMIFLGCLR Register

15	14	13	12	11	10	9	8
RESERVED				OVF	CPU2NMIWDRSn	CPU2WDRSs	RESERVED
				R=0-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h
7	6	5	4	3	2	1	0
RESERVED	PIEVECTERR	CPU2HWBISTERR	CPU1HWBISTERR	FLUNCERR	RAMUNCERR	CLOCKFAIL	NMIINT
R-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-64. NMIFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11	OVF	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.
10	CPU2NMIWDRSn	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.
9	CPU2WDRSs	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag. [3] CPU2WDRSs and CPU2NMIWDRSn bits are reserved for CPU2.NMIFLGCLR registers
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	PIEVECTERR	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.

Table 1-64. NMIFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU2HWBISTERR	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.
4	CPU1HWBISTERR	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.
3	FLUNCERR	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.
2	RAMUNCERR	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.
1	CLOCKFAIL	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.
0	NMIINT	R=0/W=1	0h	<p>Writing a 1 to the respective bit clears the corresponding flag bit in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] If hardware is trying to set a bit to 1 while software is trying to clear a bit to 0 on the same cycle, hardware has priority. [2] Users should clear the pending FAIL flag first and then clear the NMIINT flag.

1.14.5.4 NMIFLGFC Register (offset = 3h) [reset = 0h]

NMIFLGFC is shown in [Figure 1-71](#) and described in [Table 1-65](#).

NMI Flag Force Register

Figure 1-71. NMIFLGFC Register

15	14	13	12	11	10	9	8
RESERVED				OVF	CPU2NMIWDRSn	CPU2WDRS _n	RESERVED
				R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0h
7	6	5	4	3	2	1	0
RESERVED	PIEVECTERR	CPU2HWBISTERR	CPU1HWBISTERR	FLUNCERR	RAMUNCERR	CLOCKFAIL	RESERVED
R-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-65. NMIFLGFC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11	OVF	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms.
10	CPU2NMIWDRSn	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms. Note: [1] CPU2WDRS _n and CPU2NMIWDRSn bits are reserved for CPU2.NMIFLGCLR registers
9	CPU2WDRS _n	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms. Note: [1] CPU2WDRS _n and CPU2NMIWDRSn bits are reserved for CPU2.NMIFLGCLR registers
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	PIEVECTERR	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms.
5	CPU2HWBISTERR	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms.
4	CPU1HWBISTERR	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms.
3	FLUNCERR	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms.

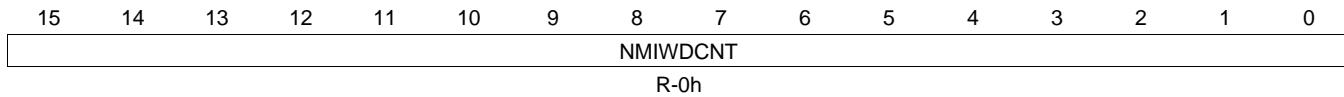
Table 1-65. NMIFLGFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RAMUNCERR	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms.
1	CLOCKFAIL	R=0/W=1	0h	Writing a 1 to these bits will set the respective FAIL flag in the NMIFLG and NMISHDFLG registers. Writes of 0 are ignored. Always reads back 0. This can be used as a means to test the NMI mechanisms.
0	RESERVED	R=0	0h	Reserved

1.14.5.5 NMIWDCNT Register (offset = 4h) [reset = 0h]

NMIWDCNT is shown in [Figure 1-72](#) and described in [Table 1-66](#).

NMI Watchdog Counter Register

Figure 1-72. NMIWDCNT Register

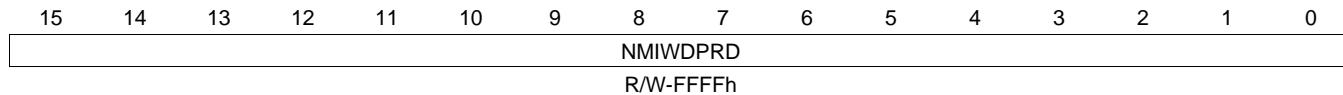
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-66. NMIWDCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NMIWDCNT	R	0h	<p>NMI Watchdog Counter: This 16-bit incremental counter will start incrementing whenever any one of the enabled FAIL flags are set. If the counter reaches the period value, an NMIRSn signal is fired which will then resets the system. The counter will reset to zero when it reaches the period value and will then restart counting if any of the enabled FAIL flags are set.</p> <p>If no enabled FAIL flag is set, then the counter will reset to zero and remain at zero until an enabled FAIL flag is set.</p> <p>Normally, the software would respond to the NMI interrupt generated and clear the offending FLAG(s) before the NMI watchdog triggers a reset. In some situations, the software may decide to allow the watchdog to reset the device anyway.</p> <p>The counter is clocked at the SYSCLKOUT rate.</p>

1.14.5.6 NMIWDPRD Register (offset = 5h) [reset = FFFFh]NMIWDPRD is shown in [Figure 1-73](#) and described in [Table 1-67](#).

NMI Watchdog Period Register

Figure 1-73. NMIWDPRD Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-67. NMIWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NMIWDPRD	R/W	FFFFh	NMI Watchdog Period: This 16-bit value contains the period value at which a reset is generated when the watchdog counter matches. At reset this value is set at the maximum. The software can decrease the period value at initialization time. Writing a PERIOD value that is smaller than the current counter value will automatically force an NMIRS _n and hence reset the watchdog counter.

1.14.5.7 NMISHDFLG Register (offset = 6h) [reset = 0h]

NMISHDFLG is shown in [Figure 1-74](#) and described in [Table 1-68](#).

NMI Shadow Flag Register

Figure 1-74. NMISHDFLG Register

15	14	13	12	11	10	9	8
RESERVED				OVF	CPU2NMIWDR Sn	CPU2WDRSn	RESERVED
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED	PIEVECTERR	CPU2HWBIST ERR	CPU1HWBIST ERR	FLUNCERR	RAMUNCERR	CLOCKFAIL	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R=0-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-68. NMISHDFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11	OVF	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGRC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] This register is added to keep the definition of System Control Reset Cause Register Clean.
10	CPU2NMIWDRSn	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGRC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] This register is added to keep the definition of System Control Reset Cause Register Clean.
9	CPU2WDRSn	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGRC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] This register is added to keep the definition of System Control Reset Cause Register Clean. [2] CPU2WDRSn and CPU2NMIWDRSn bits are reserved for CPU2.NMIFLGCLR registers
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	PIEVECTERR	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGRC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] This register is added to keep the definition of System Control Reset Cause Register Clean.

Table 1-68. NMISHDFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU2HWBISTERR	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGFC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <p>[1] This register is added to keep the definition of System Control Reset Cause Register Clean.</p>
4	CPU1HWBISTERR	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGFC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <p>[1] This register is added to keep the definition of System Control Reset Cause Register Clean.</p>
3	FLUNCERR	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGFC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <p>[1] This register is added to keep the definition of System Control Reset Cause Register Clean.</p>
2	RAMUNCERR	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGFC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <p>[1] This register is added to keep the definition of System Control Reset Cause Register Clean.</p>
1	CLOCKFAIL	R	0h	<p>Shadow NMI Flags: When an NMIFLG bit is set due to any of the possible NMI source in the device, the corresponding bit in this register is also set. Note that NMIFLGFC and NMIFLGCLR register also affects the bits of this register in the same way as they do for the NMIFLG register. This register is resetted only by PORn.</p> <p>Notes:</p> <p>[1] This register is added to keep the definition of System Control Reset Cause Register Clean.</p>
0	RESERVED	R=0	0h	Reserved

1.14.6 XINT_REGS Registers

Table 1-69 lists the memory-mapped registers for the XINT_REGS. All register offset addresses not listed in **Table 1-69** should be considered as reserved locations and the register contents should not be modified.

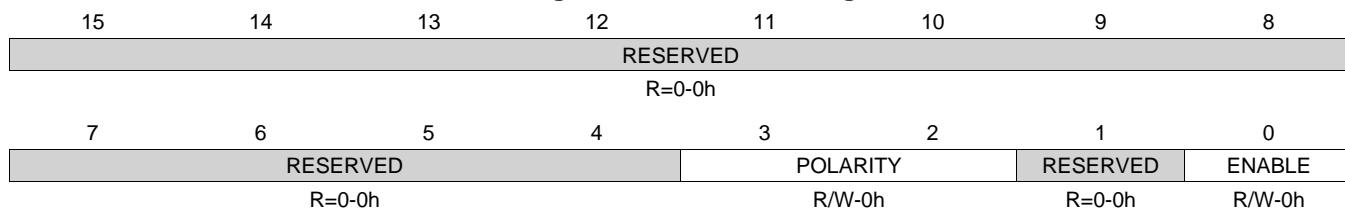
Table 1-69. XINT_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	XINT1CR	XINT1 configuration register	Section 1.14.6.1	
1h	XINT2CR	XINT2 configuration register	Section 1.14.6.2	
2h	XINT3CR	XINT3 configuration register	Section 1.14.6.3	
3h	XINT4CR	XINT4 configuration register	Section 1.14.6.4	
4h	XINT5CR	XINT5 configuration register	Section 1.14.6.5	
8h	XINT1CTR	XINT1 counter register	Section 1.14.6.6	
9h	XINT2CTR	XINT2 counter register	Section 1.14.6.7	
Ah	XINT3CTR	XINT3 counter register	Section 1.14.6.8	

1.14.6.1 XINT1CR Register (offset = 0h) [reset = 0h]

XINT1CR is shown in [Figure 1-75](#) and described in [Table 1-70](#).

XINT1 configuration register

Figure 1-75. XINT1CR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

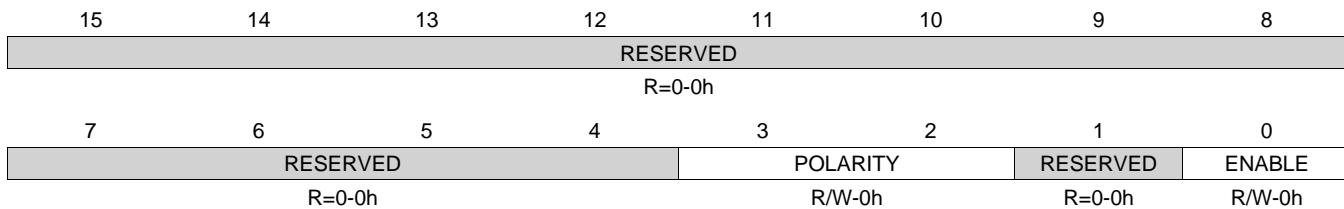
Table 1-70. XINT1CR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3-2	POLARITY	R/W	0h	00: Interrupt is selected as negative edge triggered 01: Interrupt is selected as positive edge triggered 10: Interrupt is selected as negative edge triggered 11: Interrupt is selected as positive or negative edge triggered
1	RESERVED	R=0	0h	Reserved
0	ENABLE	R/W	0h	0: Interrupt Disabled 1: Interrupt Enabled

1.14.6.2 XINT2CR Register (offset = 1h) [reset = 0h]

XINT2CR is shown in [Figure 1-76](#) and described in [Table 1-71](#).

XINT2 configuration register

Figure 1-76. XINT2CR Register

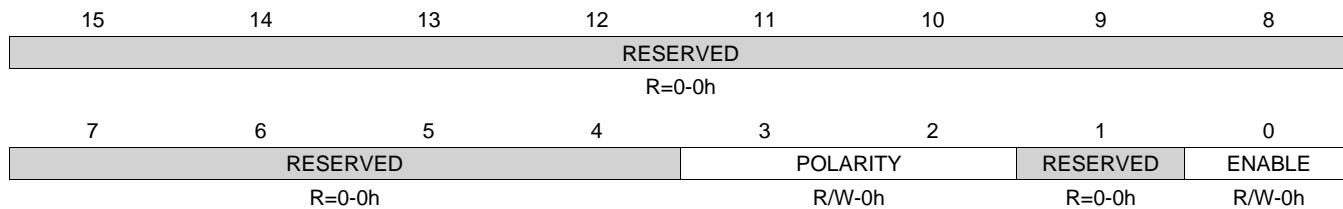
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-71. XINT2CR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3-2	POLARITY	R/W	0h	00: Interrupt is selected as negative edge triggered 01: Interrupt is selected as positive edge triggered 10: Interrupt is selected as negative edge triggered 11: Interrupt is selected as positive or negative edge triggered
1	RESERVED	R=0	0h	Reserved
0	ENABLE	R/W	0h	0: Interrupt Disabled 1: Interrupt Enabled

1.14.6.3 XINT3CR Register (offset = 2h) [reset = 0h]XINT3CR is shown in [Figure 1-77](#) and described in [Table 1-72](#).

XINT3 configuration register

Figure 1-77. XINT3CR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

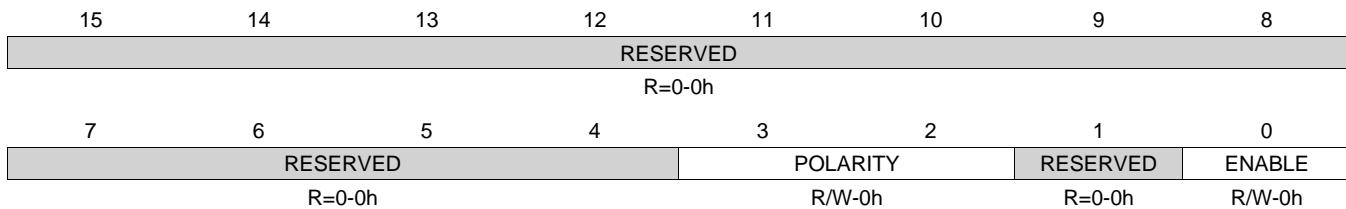
Table 1-72. XINT3CR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3-2	POLARITY	R/W	0h	00: Interrupt is selected as negative edge triggered 01: Interrupt is selected as positive edge triggered 10: Interrupt is selected as negative edge triggered 11: Interrupt is selected as positive or negative edge triggered
1	RESERVED	R=0	0h	Reserved
0	ENABLE	R/W	0h	0: Interrupt Disabled 1: Interrupt Enabled

1.14.6.4 XINT4CR Register (offset = 3h) [reset = 0h]

XINT4CR is shown in [Figure 1-78](#) and described in [Table 1-73](#).

XINT4 configuration register

Figure 1-78. XINT4CR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

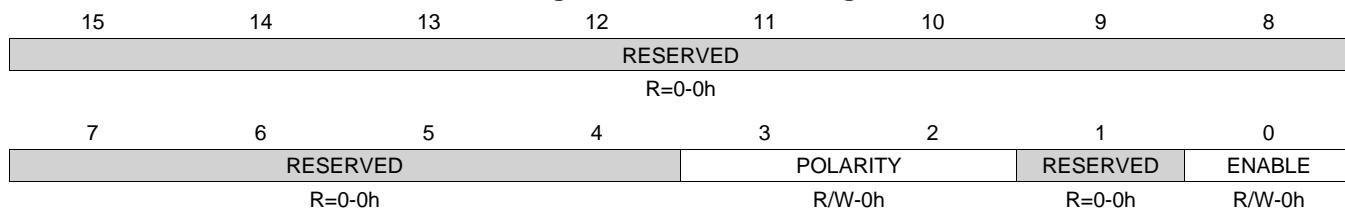
Table 1-73. XINT4CR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3-2	POLARITY	R/W	0h	00: Interrupt is selected as negative edge triggered 01: Interrupt is selected as positive edge triggered 10: Interrupt is selected as negative edge triggered 11: Interrupt is selected as positive or negative edge triggered
1	RESERVED	R=0	0h	Reserved
0	ENABLE	R/W	0h	0: Interrupt Disabled 1: Interrupt Enabled

1.14.6.5 XINT5CR Register (offset = 4h) [reset = 0h]

XINT5CR is shown in [Figure 1-79](#) and described in [Table 1-74](#).

XINT5 configuration register

Figure 1-79. XINT5CR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-74. XINT5CR Register Field Descriptions

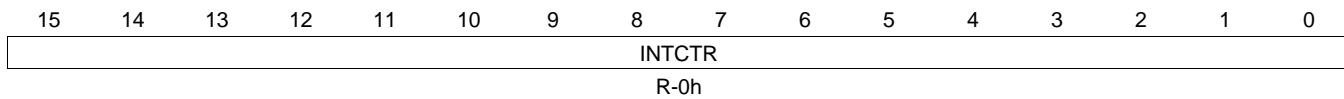
Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3-2	POLARITY	R/W	0h	00: Interrupt is selected as negative edge triggered 01: Interrupt is selected as positive edge triggered 10: Interrupt is selected as negative edge triggered 11: Interrupt is selected as positive or negative edge triggered
1	RESERVED	R=0	0h	Reserved
0	ENABLE	R/W	0h	0: Interrupt Disabled 1: Interrupt Enabled

1.14.6.6 XINT1CTR Register (offset = 8h) [reset = 0h]

XINT1CTR is shown in [Figure 1-80](#) and described in [Table 1-75](#).

XINT1 counter register

Figure 1-80. XINT1CTR Register



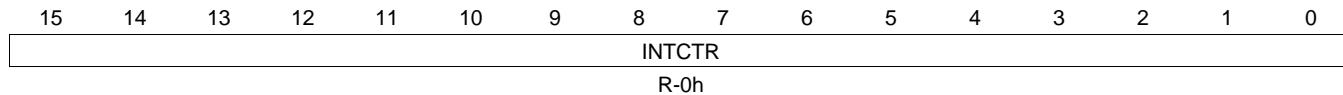
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-75. XINT1CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	INTCTR	R	0h	This is a free running 16-bit up-counter that is clocked at the SYSCLKOUT rate. The counter value is reset to 0x0000 when a valid interrupt edge is detected and then continues counting until the next valid interrupt edge is detected. The counter must only be reset by the selected POLARITY edge as selected in the respective interrupt control register. When the interrupt is disabled, the counter will stop. The counter is a free-running counter and will wrap around to zero when the max value is reached. The counter is a read only register and can only be reset to zero by a valid interrupt edge or by reset.

1.14.6.7 XINT2CTR Register (offset = 9h) [reset = 0h]XINT2CTR is shown in [Figure 1-81](#) and described in [Table 1-76](#).

XINT2 counter register

Figure 1-81. XINT2CTR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-76. XINT2CTR Register Field Descriptions

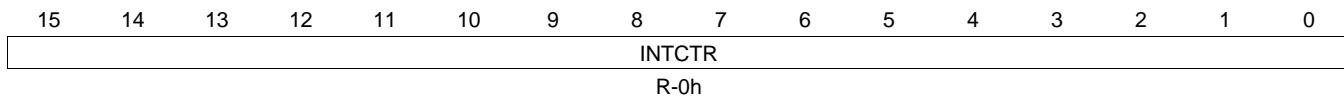
Bit	Field	Type	Reset	Description
15-0	INTCTR	R	0h	This is a free running 16-bit up-counter that is clocked at the SYSCLKOUT rate. The counter value is reset to 0x0000 when a valid interrupt edge is detected and then continues counting until the next valid interrupt edge is detected. The counter must only be reset by the selected POLARITY edge as selected in the respective interrupt control register. When the interrupt is disabled, the counter will stop. The counter is a free-running counter and will wrap around to zero when the max value is reached. The counter is a read only register and can only be reset to zero by a valid interrupt edge or by reset.

1.14.6.8 XINT3CTR Register (offset = Ah) [reset = 0h]

XINT3CTR is shown in [Figure 1-82](#) and described in [Table 1-77](#).

XINT3 counter register

Figure 1-82. XINT3CTR Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-77. XINT3CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	INTCTR	R	0h	This is a free running 16-bit up-counter that is clocked at the SYSCLKOUT rate. The counter value is reset to 0x0000 when a valid interrupt edge is detected and then continues counting until the next valid interrupt edge is detected. The counter must only be reset by the selected POLARITY edge as selected in the respective interrupt control register. When the interrupt is disabled, the counter will stop. The counter is a free-running counter and will wrap around to zero when the max value is reached. The counter is a read only register and can only be reset to zero by a valid interrupt edge or by reset.

1.14.7 DMA_CLA_SRC_SEL_REGS Registers

Table 1-78 lists the memory-mapped registers for the DMA_CLA_SRC_SEL_REGS. All register offset addresses not listed in Table 1-78 should be considered as reserved locations and the register contents should not be modified.

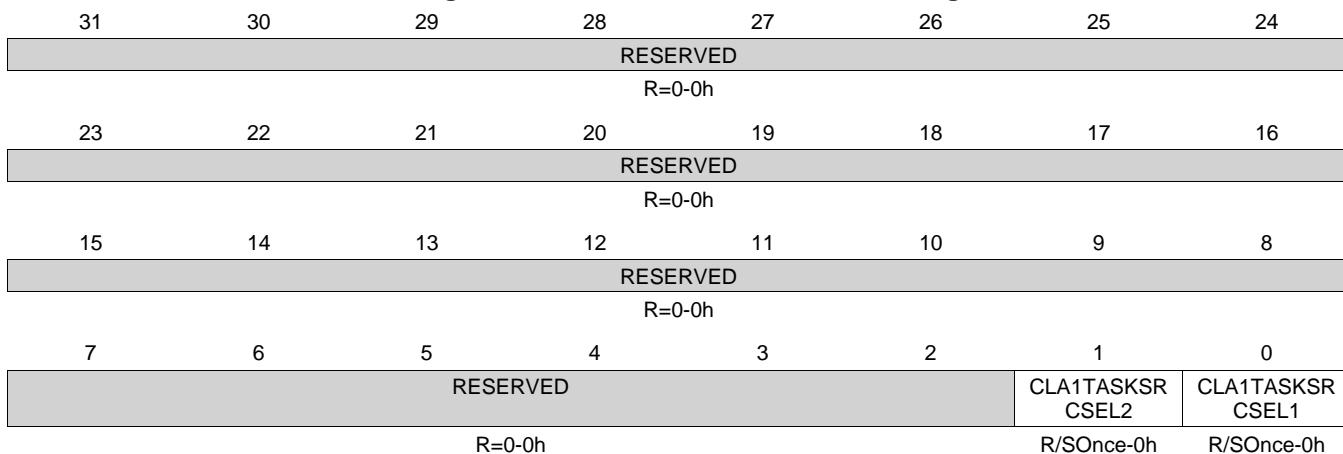
Table 1-78. DMA_CLA_SRC_SEL_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	CLA1TASKSRCSELLOCK	CLA1 Task Trigger Source Select Lock Register	Section 1.14.7.1	EALLOW
4h	DMACHSRCSELLOCK	DMA Channel Triger Source Select Lock Register	Section 1.14.7.2	EALLOW
6h	CLA1TASKSRCSEL1	CLA1 Task Trigger Source Select Register-1	Section 1.14.7.3	EALLOW
8h	CLA1TASKSRCSEL2	CLA1 Task Trigger Source Select Register-2	Section 1.14.7.4	EALLOW
16h	DMACHSRCSEL1	DMA Channel Trigger Source Select Register-1	Section 1.14.7.5	EALLOW
18h	DMACHSRCSEL2	DMA Channel Trigger Source Select Register-2	Section 1.14.7.6	EALLOW

1.14.7.1 CLA1TASKSRCSELLOCK Register (offset = 0h) [reset = 0h]

CLA1TASKSRCSELLOCK is shown in [Figure 1-83](#) and described in [Table 1-79](#).

CLA1 Task Trigger Source Select Lock Register

Figure 1-83. CLA1TASKSRCSELLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-79. CLA1TASKSRCSELLOCK Register Field Descriptions

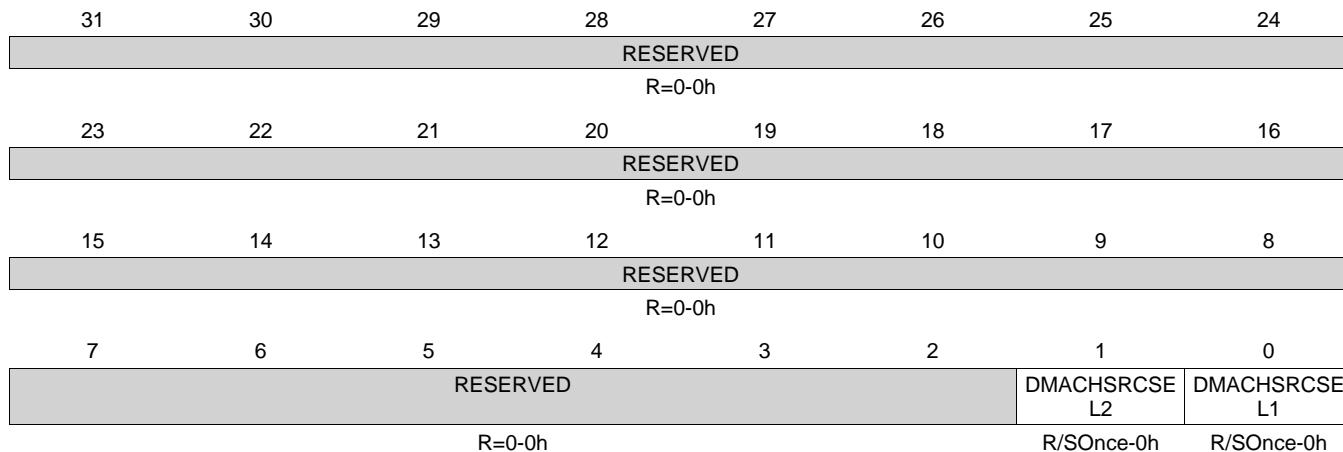
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	CLA1TASKSRCSEL2	R/SOnce	0h	CLA1TASKSRCSEL2 Register Lock bit: 0: Respective register is not locked 1: Respective register is locked. Notes: [1] Any SOnce bit in this register, once set can only be cleared through a SYRSRs. Write of 0 to any bit of this register has no effect [2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed
0	CLA1TASKSRCSEL1	R/SOnce	0h	CLA1TASKSRCSEL1 Register Lock bit: 0: Respective register is not locked 1: Respective register is locked. Notes: [1] Any SOnce bit in this register, once set can only be cleared through a SYRSRs. Write of 0 to any bit of this register has no effect [2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed

1.14.7.2 DMACHSRCSELLOCK Register (offset = 4h) [reset = 0h]

DMACHSRCSELLOCK is shown in [Figure 1-84](#) and described in [Table 1-80](#).

DMA Channel Triger Source Select Lock Register

Figure 1-84. DMACHSRCSELLOCK Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-80. DMACHSRCSELLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	DMACHSRCSEL2	R/SOnce	0h	<p>DMACHSRCSEL2 Register Lock bit: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] Any SOnce bit in this register, once set can only be cleared through a SYSRSn. Write of 0 to any bit of this register has no effect [2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed
0	DMACHSRCSEL1	R/SOnce	0h	<p>DMACHSRCSEL1 Register Lock bit: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] Any SOnce bit in this register, once set can only be cleared through a SYSRSn. Write of 0 to any bit of this register has no effect [2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed

1.14.7.3 CLA1TASKSRCSEL1 Register (offset = 6h) [reset = 0h]

CLA1TASKSRCSEL1 is shown in [Figure 1-85](#) and described in [Table 1-81](#).

CLA1 Task Trigger Source Select Register-1

Figure 1-85. CLA1TASKSRCSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TASK4								TASK3								TASK2								TASK1							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-81. CLA1TASKSRCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TASK4	R/W	0h	Selects the Trigger Source for TASK4 of CLA1
23-16	TASK3	R/W	0h	Selects the Trigger Source for TASK3 of CLA1
15-8	TASK2	R/W	0h	Selects the Trigger Source for TASK2 of CLA1
7-0	TASK1	R/W	0h	Selects the Trigger Source for TASK1 of CLA1

1.14.7.4 CLA1TASKSRCSEL2 Register (offset = 8h) [reset = 0h]CLA1TASKSRCSEL2 is shown in [Figure 1-86](#) and described in [Table 1-82](#).

CLA1 Task Trigger Source Select Register-2

Figure 1-86. CLA1TASKSRCSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TASK8								TASK7								TASK6								TASK5							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-82. CLA1TASKSRCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TASK8	R/W	0h	Selects the Trigger Source for TASK8 of CLA1
23-16	TASK7	R/W	0h	Selects the Trigger Source for TASK7 of CLA1
15-8	TASK6	R/W	0h	Selects the Trigger Source for TASK6 of CLA1
7-0	TASK5	R/W	0h	Selects the Trigger Source for TASK5 of CLA1

1.14.7.5 DMACHSRCSEL1 Register (offset = 16h) [reset = 0h]

DMACHSRCSEL1 is shown in [Figure 1-87](#) and described in [Table 1-83](#).

DMA Channel Trigger Source Select Register-1

Figure 1-87. DMACHSRCSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH4								CH3								CH2								CH1							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-83. DMACHSRCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CH4	R/W	0h	Selects the Trigger and Sync Source CH4 of DMA
23-16	CH3	R/W	0h	Selects the Trigger and Sync Source CH3 of DMA
15-8	CH2	R/W	0h	Selects the Trigger and Sync Source CH2 of DMA
7-0	CH1	R/W	0h	Selects the Trigger and Sync Source CH1 of DMA

1.14.7.6 DMACHSRCSEL2 Register (offset = 18h) [reset = 0h]DMACHSRCSEL2 is shown in [Figure 1-88](#) and described in [Table 1-84](#).

DMA Channel Trigger Source Select Register-2

Figure 1-88. DMACHSRCSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				CH6			CH5								
R=0-0h																				R/W-0h			R/W-0h								

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-84. DMACHSRCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	CH6	R/W	0h	Selects the Trigger and Sync Source CH6 of DMA
7-0	CH5	R/W	0h	Selects the Trigger and Sync Source CH5 of DMA

1.14.8 DEV_CFG_REGS Registers

Table 1-85 lists the memory-mapped registers for the DEV_CFG_REGS. All register offset addresses not listed in Table 1-85 should be considered as reserved locations and the register contents should not be modified.

Table 1-85. DEV_CFG_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	DEVCFGLOCK1	Lock bit for CPUSELx registers	Section 1.14.8.1	EALLOW
8h	PARTIDL	Lower 32-bit of Device PART Identification Number	Section 1.14.8.2	
Ah	PARTIDH	Upper 32-bit of Device PART Identification Number	Section 1.14.8.3	
Ch	REVID	Device Revision Number	Section 1.14.8.4	
10h	DC0	Device Capability: Device Information	Section 1.14.8.5	
12h	DC1	Device Capability: Processing Block Customization	Section 1.14.8.6	
14h	DC2	Device Capability: EMIF Customization	Section 1.14.8.7	
16h	DC3	Device Capability: Peripheral Customization	Section 1.14.8.8	
18h	DC4	Device Capability: Peripheral Customization	Section 1.14.8.9	
1Ah	DC5	Device Capability: Peripheral Customization	Section 1.14.8.10	
1Ch	DC6	Device Capability: Peripheral Customization	Section 1.14.8.11	
1Eh	DC7	Device Capability: Peripheral Customization	Section 1.14.8.12	
20h	DC8	Device Capability: Peripheral Customization	Section 1.14.8.13	
22h	DC9	Device Capability: Peripheral Customization	Section 1.14.8.14	
24h	DC10	Device Capability: Peripheral Customization	Section 1.14.8.15	
26h	DC11	Device Capability: Peripheral Customization	Section 1.14.8.16	
28h	DC12	Device Capability: Peripheral Customization	Section 1.14.8.17	
2Ah	DC13	Device Capability: Peripheral Customization	Section 1.14.8.18	
2Ch	DC14	Device Capability: Analog Modules Customization	Section 1.14.8.19	
2Eh	DC15	Device Capability: Analog Modules Customization	Section 1.14.8.20	
32h	DC17	Device Capability: Analog Modules Customization	Section 1.14.8.21	
34h	DC18	Device Capability: Lx.1 SRAM Customization	Section 1.14.8.22	
36h	DC19	Device Capability: Lx.2 SRAM Customization	Section 1.14.8.23	
38h	DC20	Device Capability: GSx SRAM Customization	Section 1.14.8.24	
60h	PERCNF1	Peripheral Configuration register	Section 1.14.8.25	
74h	FUSEERR	e-Fuse error Status register	Section 1.14.8.26	
82h	SOFTPRES0	Processing Block Software Reset register	Section 1.14.8.27	EALLOW

Table 1-85. DEV_CFG_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
84h	SOFTPRES1	EMIF Software Reset register	Section 1.14.8.28	EALLOW
86h	SOFTPRES2	Peripheral Software Reset register	Section 1.14.8.29	EALLOW
88h	SOFTPRES3	Peripheral Software Reset register	Section 1.14.8.30	EALLOW
8Ah	SOFTPRES4	Peripheral Software Reset register	Section 1.14.8.31	EALLOW
8Ch	SOFTPRES5	Peripheral Software Reset register	Section 1.14.8.32	EALLOW
8Eh	SOFTPRES6	Peripheral Software Reset register	Section 1.14.8.33	EALLOW
90h	SOFTPRES7	Peripheral Software Reset register	Section 1.14.8.34	EALLOW
92h	SOFTPRES8	Peripheral Software Reset register	Section 1.14.8.35	EALLOW
94h	SOFTPRES9	Peripheral Software Reset register	Section 1.14.8.36	EALLOW
98h	SOFTPRES11	Peripheral Software Reset register	Section 1.14.8.37	EALLOW
9Ch	SOFTPRES13	Peripheral Software Reset register	Section 1.14.8.38	EALLOW
9Eh	SOFTPRES14	Peripheral Software Reset register	Section 1.14.8.39	EALLOW
A2h	SOFTPRES16	Peripheral Software Reset register	Section 1.14.8.40	EALLOW
D6h	CPUSEL0	CPU Select register for common peripherals	Section 1.14.8.41	EALLOW
D8h	CPUSEL1	CPU Select register for common peripherals	Section 1.14.8.42	EALLOW
DAh	CPUSEL2	CPU Select register for common peripherals	Section 1.14.8.43	EALLOW
DCh	CPUSEL3	CPU Select register for common peripherals	Section 1.14.8.44	EALLOW
DEh	CPUSEL4	CPU Select register for common peripherals	Section 1.14.8.45	EALLOW
E0h	CPUSEL5	CPU Select register for common peripherals	Section 1.14.8.46	EALLOW
E2h	CPUSEL6	CPU Select register for common peripherals	Section 1.14.8.47	EALLOW
E4h	CPUSEL7	CPU Select register for common peripherals	Section 1.14.8.48	EALLOW
E6h	CPUSEL8	CPU Select register for common peripherals	Section 1.14.8.49	EALLOW
E8h	CPUSEL9	CPU Select register for common peripherals	Section 1.14.8.50	EALLOW
ECh	CPUSEL11	CPU Select register for common peripherals	Section 1.14.8.51	EALLOW
EEh	CPUSEL12	CPU Select register for common peripherals	Section 1.14.8.52	EALLOW
F2h	CPUSEL14	CPU Select register for common peripherals	Section 1.14.8.53	EALLOW
122h	CPU2RESCTL	CPU2 Reset Control Register	Section 1.14.8.54	EALLOW

Table 1-85. DEV_CFG_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
124h	RSTSTAT	Reset Status register for secondary C28x CPUs	Section 1.14.8.55	
125h	LPMSTAT	LPM Status Register for secondary C28x CPUs	Section 1.14.8.56	
126h	PSCONCTL1	Register for PSCON Configuration	Section 1.14.8.57	EALLOW
12Ch	SYSDBGCTL	System Debug Control register	Section 1.14.8.58	EALLOW

1.14.8.1 DEVCFGLOCK1 Register (offset = 0h) [reset = 0h]

DEVCFGLOCK1 is shown in [Figure 1-89](#) and described in [Table 1-86](#).

Lock bit for CPUSELx registers

The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed

Note:

Any SOnce bit in this register, once set can only be cleared through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect

Figure 1-89. DEVCFGLOCK1 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED	CPUSEL14	CPUSEL13	CPUSEL12	CPUSEL11	CPUSEL10	CPUSEL9	CPUSEL8
R=0-0h	R/SOnce-0h						
7	6	5	4	3	2	1	0
CPUSEL7	CPUSEL6	CPUSEL5	CPUSEL4	CPUSEL3	CPUSEL2	CPUSEL1	CPUSEL0
R/SOnce-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-86. DEVCFGLOCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15	RESERVED	R=0	0h	Reserved
14	CPUSEL14	R/SOnce	0h	Lock bit for CPUSEL14 register: 0: Register is not locked 1: Register is locked
13	CPUSEL13	R/SOnce	0h	Lock bit for CPUSEL13 register: 0: Register is not locked 1: Register is locked
12	CPUSEL12	R/SOnce	0h	Lock bit for CPUSEL12 register: 0: Register is not locked 1: Register is locked
11	CPUSEL11	R/SOnce	0h	Lock bit for CPUSEL11 register: 0: Register is not locked 1: Register is locked
10	CPUSEL10	R/SOnce	0h	Lock bit for CPUSEL10 register: 0: Register is not locked 1: Register is locked
9	CPUSEL9	R/SOnce	0h	Lock bit for CPUSEL9 register: 0: Register is not locked 1: Register is locked

Table 1-86. DEVCFGLOCK1 Register Field Descriptions (continued)

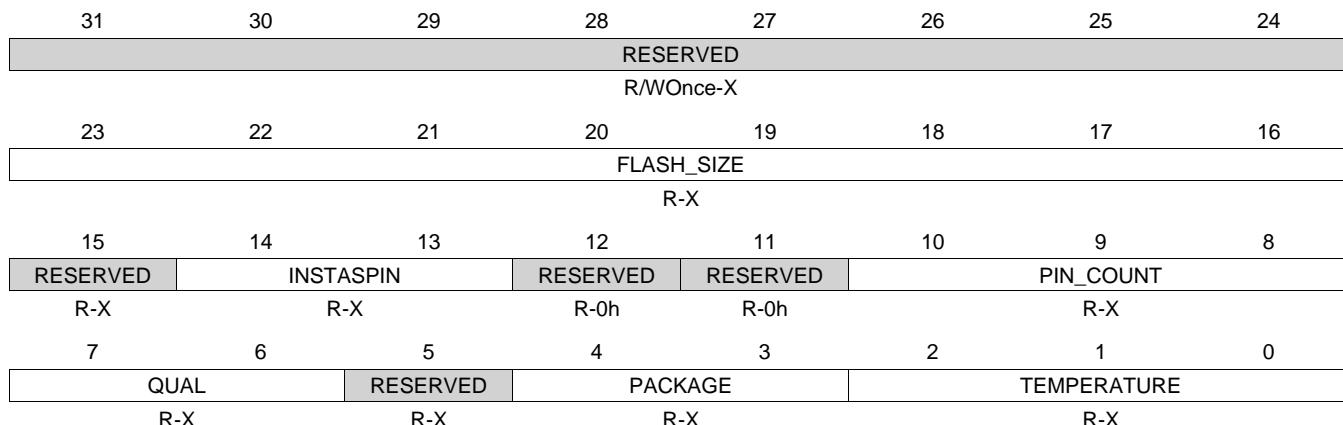
Bit	Field	Type	Reset	Description
8	CPUSEL8	R/SOnce	0h	Lock bit for CPUSEL8 register: 0: Register is not locked 1: Register is locked
7	CPUSEL7	R/SOnce	0h	Lock bit for CPUSEL7 register: 0: Register is not locked 1: Register is locked
6	CPUSEL6	R/SOnce	0h	Lock bit for CPUSEL6 register: 0: Register is not locked 1: Register is locked
5	CPUSEL5	R/SOnce	0h	Lock bit for CPUSEL5 register: 0: Register is not locked 1: Register is locked
4	CPUSEL4	R/SOnce	0h	Lock bit for CPUSEL4 register: 0: Register is not locked 1: Register is locked
3	CPUSEL3	R/SOnce	0h	Lock bit for CPUSEL3 register: 0: Register is not locked 1: Register is locked
2	CPUSEL2	R/SOnce	0h	Lock bit for CPUSEL2 register: 0: Register is not locked 1: Register is locked
1	CPUSEL1	R/SOnce	0h	Lock bit for CPUSEL1 register: 0: Register is not locked 1: Register is locked
0	CPUSEL0	R/SOnce	0h	Lock bit for CPUSEL0 register: 0: Register is not locked 1: Register is locked

1.14.8.2 PARTIDL Register (offset = 8h) [reset = 0h]

Register mask: 0h

PARTIDL is shown in [Figure 1-90](#) and described in [Table 1-87](#).

Lower 32-bit of Device PART Identification Number

Figure 1-90. PARTIDL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-87. PARTIDL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/WOnce	X	Reserved
23-16	FLASH_SIZE	R	X	0x7 - 512KB 0x6 - 256KB Note: This field shows flash size on CPU1 (see datasheet for flash size available)
15	RESERVED	R	X	Reserved
14-13	INSTASPIN	R	X	0 = Reserved for future 1 = Reserved for future 2 = Reserved for future 3 = NONE
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10-8	PIN_COUNT	R	X	0 = reserved for future 1 = reserved for future 2 = reserved for future 3 = reserved for future 4 = reserved for future 5 = 100 pin 6 = 176 pin 7 = 337 pin
7-6	QUAL	R	X	0 = Engineering sample.(TMX) 1 = Pilot production (TMP) 2 = Fully qualified (TMS)
5	RESERVED	R	X	Reserved

Table 1-87. PARTIDL Register Field Descriptions (continued)

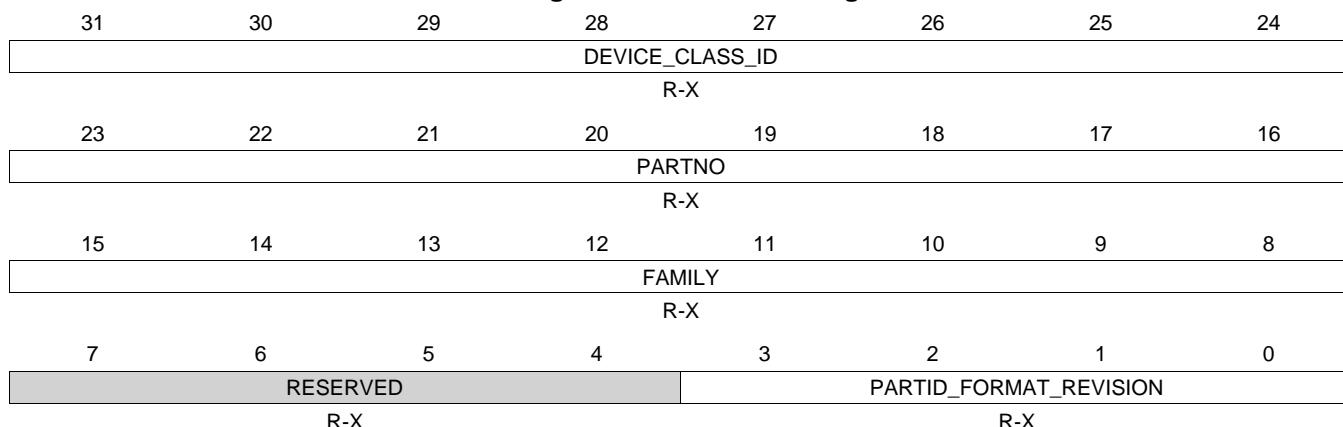
Bit	Field	Type	Reset	Description
4-3	PACKAGE	R	X	0x0 - SOIC 0x1 - QFP 0x2 - BGA 0x3 - QFN
2-0	TEMPERATURE	R	X	0x0 Commercial temperature range (0C to 70C) 0x1 Industrial temperature range (0C to 85C) 0x2 Extended temperature range (-40C to 105C) 0x3 Automotive temperature range (-40C to 125C) 0x4 Automotive temperature range (-40C to 155C)

1.14.8.3 PARTIDH Register (offset = Ah) [reset = 0h]

Register mask: 0h

PARTIDH is shown in [Figure 1-91](#) and described in [Table 1-88](#).

Upper 32-bit of Device PART Identification Number

Figure 1-91. PARTIDH Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-88. PARTIDH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DEVICE_CLASS_ID	R	X	Reserved
23-16	PARTNO	R	X	Refer to Datasheet for Device Part Number
15-8	FAMILY	R	X	Device Family 0x3 - DELFINO DUAL CORE 0x4 - DELFINO SINGLE CORE 0x5 - PICCOLO SINGLE CORE Other values Reserved
7-4	RESERVED	R	X	Reserved
3-0	PARTID_FORMAT_REVISION	R	X	Revision of the PARTID format

1.14.8.4 REVID Register (offset = Ch) [reset = 0h]

Register mask: 0h

REVID is shown in [Figure 1-92](#) and described in [Table 1-89](#).

Device Revision Number

Figure 1-92. REVID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVID																															
R-X																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-89. REVID Register Field Descriptions

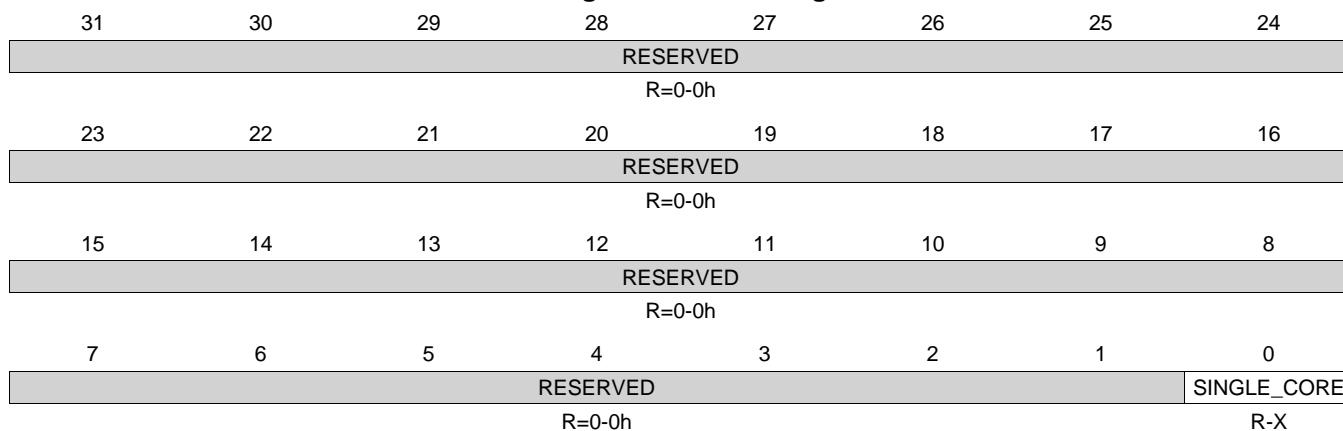
Bit	Field	Type	Reset	Description
31-0	REVID	R	X	These 32-bits specify the silicon revision 0x0 - Revision 0 0x0 - Revision A

1.14.8.5 DC0 Register (offset = 10h) [reset = 0h]

Register mask: FFFFFFFFEh

DC0 is shown in [Figure 1-93](#) and described in [Table 1-90](#).

Device Capability: Device Information

Figure 1-93. DC0 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-90. DC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-1	RESERVED	R=0	0h	Reserved
0	SINGLE_CORE	R	X	Single Core vs Dual Core 0: Single Core 1: Dual Core

1.14.8.6 DC1 Register (offset = 12h) [reset = 0h]

Register mask: FFFFFC30h

DC1 is shown in [Figure 1-94](#) and described in [Table 1-91](#).

Device Capability: Processing Block Customization

Figure 1-94. DC1 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED						RESERVED	CPU2_CLA1
R=0-0h						R-0h	R-X
7	6	5	4	3	2	1	0
RESERVED	CPU1_CLA1	RESERVED		CPU2_VCU	CPU1_VCU	CPU2_FPU_TMU	CPU1_FPU_TMU
R-0h	R-X	R=0-0h		R-X	R-X	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-91. DC1 Register Field Descriptions

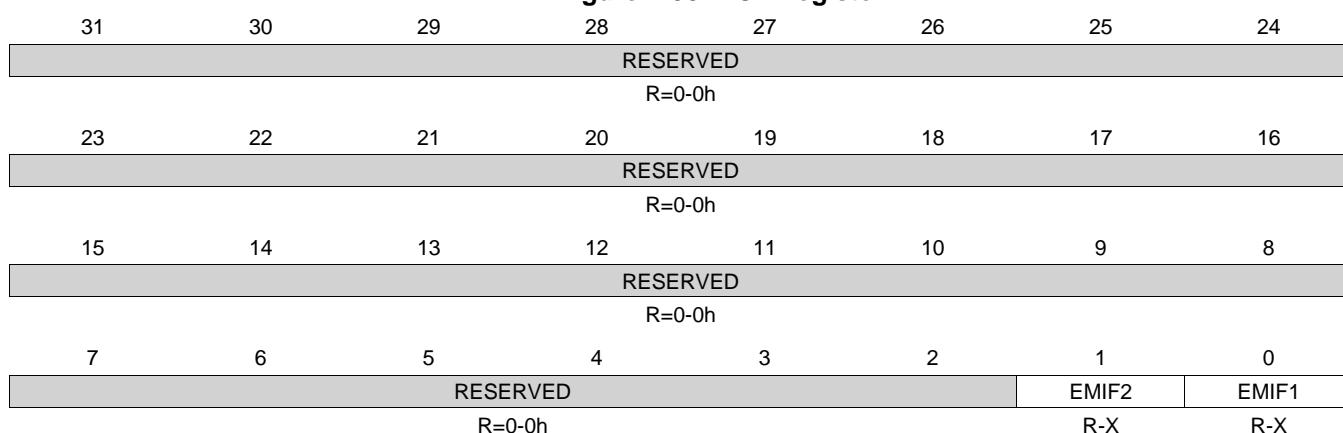
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-10	RESERVED	R=0	0h	Reserved
9	RESERVED	R	0h	Reserved
8	CPU2_CLA1	R	X	0 - feature is not present on this device 1 - feature is present on this device
7	RESERVED	R	0h	Reserved
6	CPU1_CLA1	R	X	0 - feature is not present on this device 1 - feature is present on this device
5-4	RESERVED	R=0	0h	Reserved
3	CPU2_VCU	R	X	0 - feature is not present on this device 1 - feature is present on this device
2	CPU1_VCU	R	X	0 - feature is not present on this device 1 - feature is present on this device
1	CPU2_FPU_TMU	R	X	0 - feature is not present on this device 1 - feature is present on this device
0	CPU1_FPU_TMU	R	X	0 - feature is not present on this device 1 - feature is present on this device

1.14.8.7 DC2 Register (offset = 14h) [reset = 0h]

Register mask: FFFFFFFFCh

DC2 is shown in [Figure 1-95](#) and described in [Table 1-92](#).

Device Capability: EMIF Customization

Figure 1-95. DC2 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-92. DC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	EMIF2	R	X	EMIF2 : 0: Feature not present on the device 1: Feature present on the device
0	EMIF1	R	X	EMIF1 : 0: Feature not present on the device 1: Feature present on the device

1.14.8.8 DC3 Register (offset = 16h) [reset = 0h]

Register mask: FFFF0000h

DC3 is shown in [Figure 1-96](#) and described in [Table 1-93](#).

Device Capability: Peripheral Customization

Figure 1-96. DC3 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	EPWM12	EPWM11	EPWM10	EPWM9
R-0h	R-0h	R-0h	R-0h	R-X	R-X	R-X	R-X
7	6	5	4	3	2	1	0
EPWM8	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-93. DC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	EPWM12	R	X	EPWM12 : 0: Feature not present on the device 1: Feature present on the device
10	EPWM11	R	X	EPWM11 : 0: Feature not present on the device 1: Feature present on the device
9	EPWM10	R	X	EPWM10 : 0: Feature not present on the device 1: Feature present on the device
8	EPWM9	R	X	EPWM9 : 0: Feature not present on the device 1: Feature present on the device
7	EPWM8	R	X	EPWM8 : 0: Feature not present on the device 1: Feature present on the device
6	EPWM7	R	X	EPWM7 : 0: Feature not present on the device 1: Feature present on the device
5	EPWM6	R	X	EPWM6 : 0: Feature not present on the device 1: Feature present on the device

Table 1-93. DC3 Register Field Descriptions (continued)

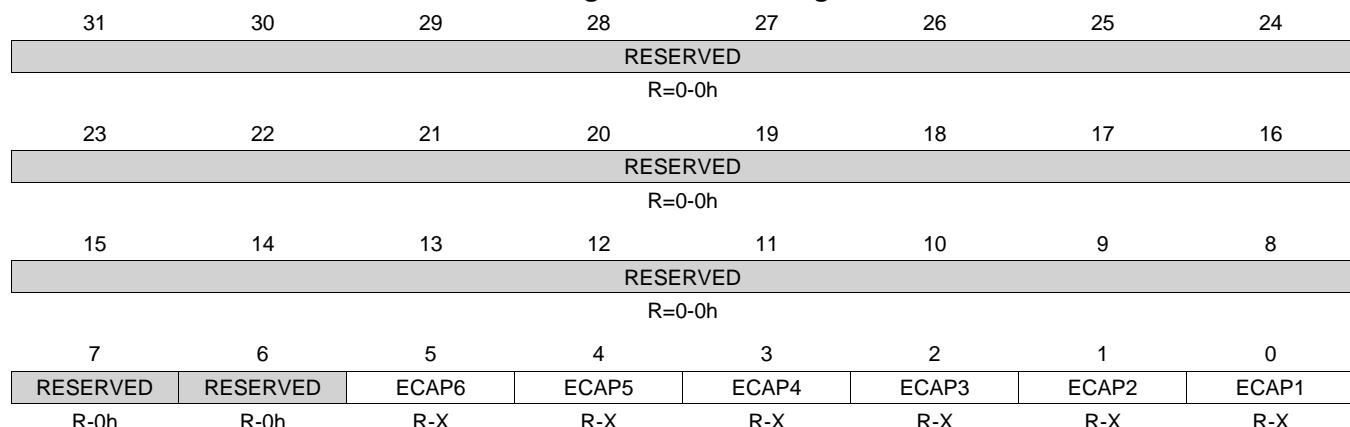
Bit	Field	Type	Reset	Description
4	EPWM5	R	X	EPWM5 : 0: Feature not present on the device 1: Feature present on the device
3	EPWM4	R	X	EPWM4 : 0: Feature not present on the device 1: Feature present on the device
2	EPWM3	R	X	EPWM3 : 0: Feature not present on the device 1: Feature present on the device
1	EPWM2	R	X	EPWM2 : 0: Feature not present on the device 1: Feature present on the device
0	EPWM1	R	X	EPWM1 : 0: Feature not present on the device 1: Feature present on the device

1.14.8.9 DC4 Register (offset = 18h) [reset = 0h]

Register mask: FFFFFFF00h

DC4 is shown in [Figure 1-97](#) and described in [Table 1-94](#).

Device Capability: Peripheral Customization

Figure 1-97. DC4 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-94. DC4 Register Field Descriptions

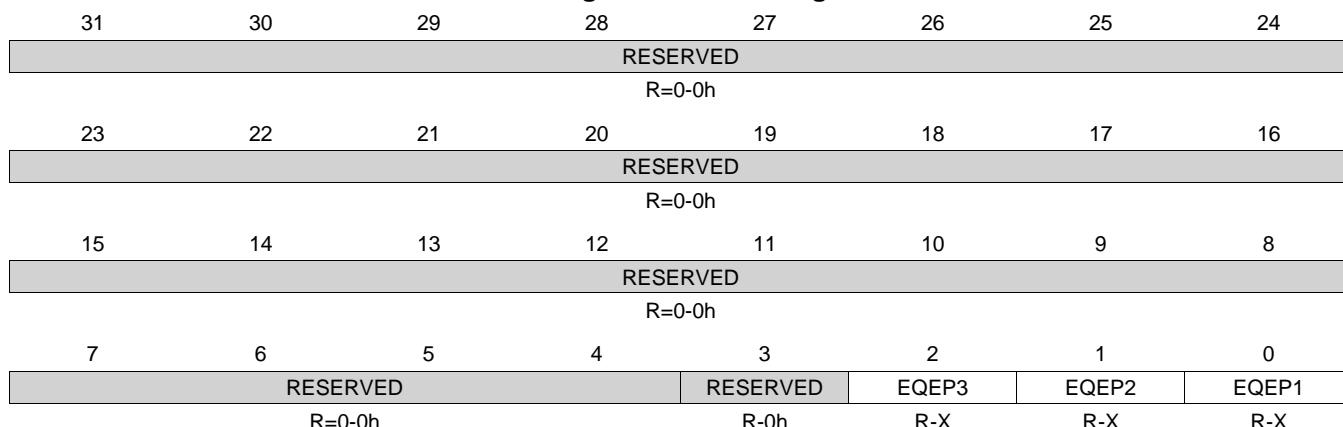
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	ECAP6	R	X	ECAP6 : 0: Feature not present on the device 1: Feature present on the device
4	ECAP5	R	X	ECAP5 : 0: Feature not present on the device 1: Feature present on the device
3	ECAP4	R	X	ECAP4 : 0: Feature not present on the device 1: Feature present on the device
2	ECAP3	R	X	ECAP3 : 0: Feature not present on the device 1: Feature present on the device
1	ECAP2	R	X	ECAP2 : 0: Feature not present on the device 1: Feature present on the device
0	ECAP1	R	X	ECAP1 : 0: Feature not present on the device 1: Feature present on the device

1.14.8.10 DC5 Register (offset = 1Ah) [reset = 0h]

Register mask: FFFFFFFF0h

DC5 is shown in [Figure 1-98](#) and described in [Table 1-95](#).

Device Capability: Peripheral Customization

Figure 1-98. DC5 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-95. DC5 Register Field Descriptions

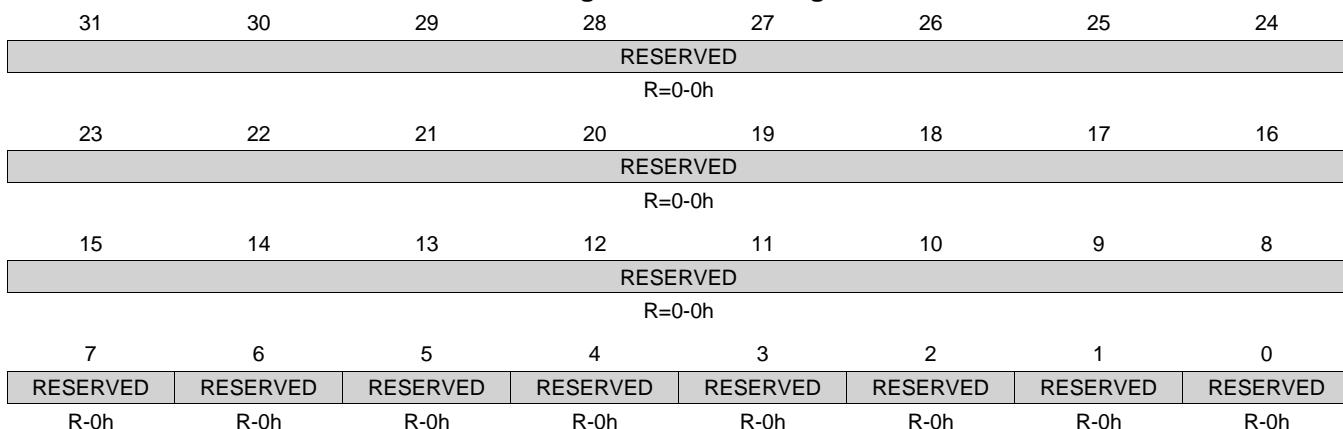
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	EQEP3	R	X	EQEP3 : 0: Feature not present on the device 1: Feature present on the device
1	EQEP2	R	X	EQEP2 : 0: Feature not present on the device 1: Feature present on the device
0	EQEP1	R	X	EQEP1 : 0: Feature not present on the device 1: Feature present on the device

1.14.8.11 DC6 Register (offset = 1Ch) [reset = 0h]

Register mask: FFFFFFF00h

DC6 is shown in [Figure 1-99](#) and described in [Table 1-96](#).

Device Capability: Peripheral Customization

Figure 1-99. DC6 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-96. DC6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.8.12 DC7 Register (offset = 1Eh) [reset = 0h]

Register mask: FFFFFFF00h

DC7 is shown in [Figure 1-100](#) and described in [Table 1-97](#).

Device Capability: Peripheral Customization

Figure 1-100. DC7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R=0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESE RVED	RESE RVED	RESE RVED	RESE RVED	RESE RVED	RESE RVED	SD2	SD1
R=0-0h								R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-97. DC7 Register Field Descriptions

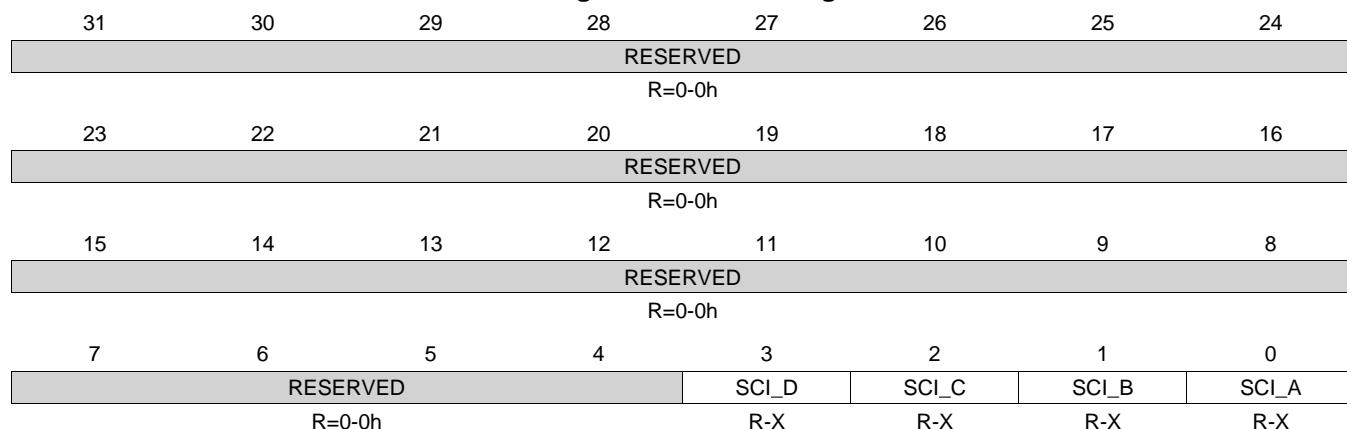
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	SD2	R	X	SD2 : 0: Feature not present on the device 1: Feature present on the device
0	SD1	R	X	SD1 : 0: Feature not present on the device 1: Feature present on the device

1.14.8.13 DC8 Register (offset = 20h) [reset = 0h]

Register mask: FFFFFFFF0h

DC8 is shown in [Figure 1-101](#) and described in [Table 1-98](#).

Device Capability: Peripheral Customization

Figure 1-101. DC8 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-98. DC8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	SCI_D	R	X	SCI_D : 0: Feature not present on the device 1: Feature present on the device
2	SCI_C	R	X	SCI_C : 0: Feature not present on the device 1: Feature present on the device
1	SCI_B	R	X	SCI_B : 0: Feature not present on the device 1: Feature present on the device
0	SCI_A	R	X	SCI_A : 0: Feature not present on the device 1: Feature present on the device

1.14.8.14 DC9 Register (offset = 22h) [reset = 0h]

Register mask: FFFCFFFF0h

DC9 is shown in [Figure 1-102](#) and described in [Table 1-99](#).

Device Capability: Peripheral Customization

Figure 1-102. DC9 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	SPI_C	SPI_B	SPI_A
R=0-0h				R-0h	R-X	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-99. DC9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	SPI_C	R	X	SPI_C : 0: Feature not present on the device 1: Feature present on the device
1	SPI_B	R	X	SPI_B : 0: Feature not present on the device 1: Feature present on the device
0	SPI_A	R	X	SPI_A : 0: Feature not present on the device 1: Feature present on the device

1.14.8.15 DC10 Register (offset = 24h) [reset = 0h]

Register mask: FFFCFFFCh

DC10 is shown in [Figure 1-103](#) and described in [Table 1-100](#).

Device Capability: Peripheral Customization

Figure 1-103. DC10 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED							
R=0-0h							
						I2C_B	I2C_A
						R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-100. DC10 Register Field Descriptions

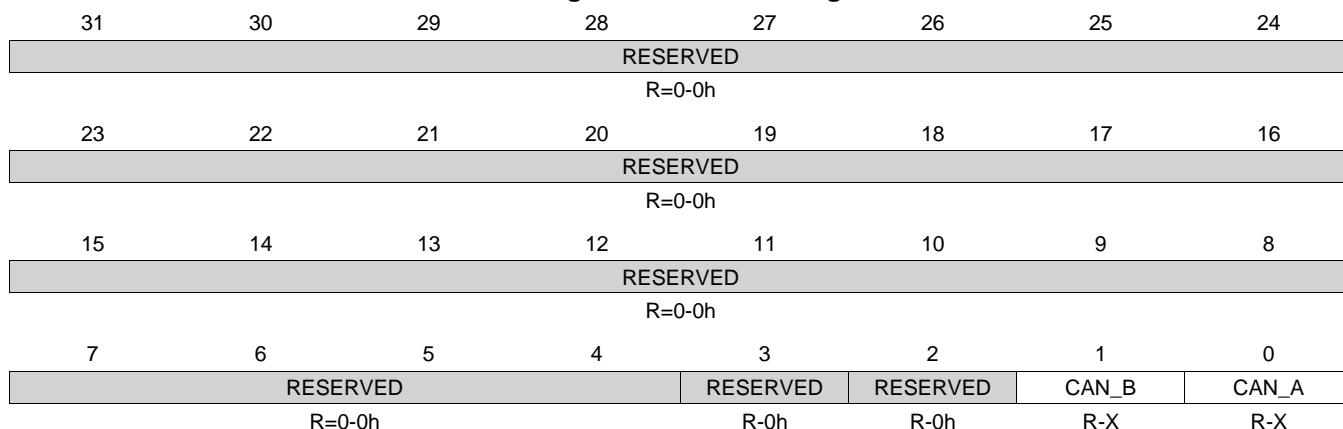
Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	I2C_B	R	X	I2C_B : 0: Feature not present on the device 1: Feature present on the device
0	I2C_A	R	X	I2C_A : 0: Feature not present on the device 1: Feature present on the device

1.14.8.16 DC11 Register (offset = 26h) [reset = 0h]

Register mask: FFFFFFFF0h

DC11 is shown in [Figure 1-104](#) and described in [Table 1-101](#).

Device Capability: Peripheral Customization

Figure 1-104. DC11 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-101. DC11 Register Field Descriptions

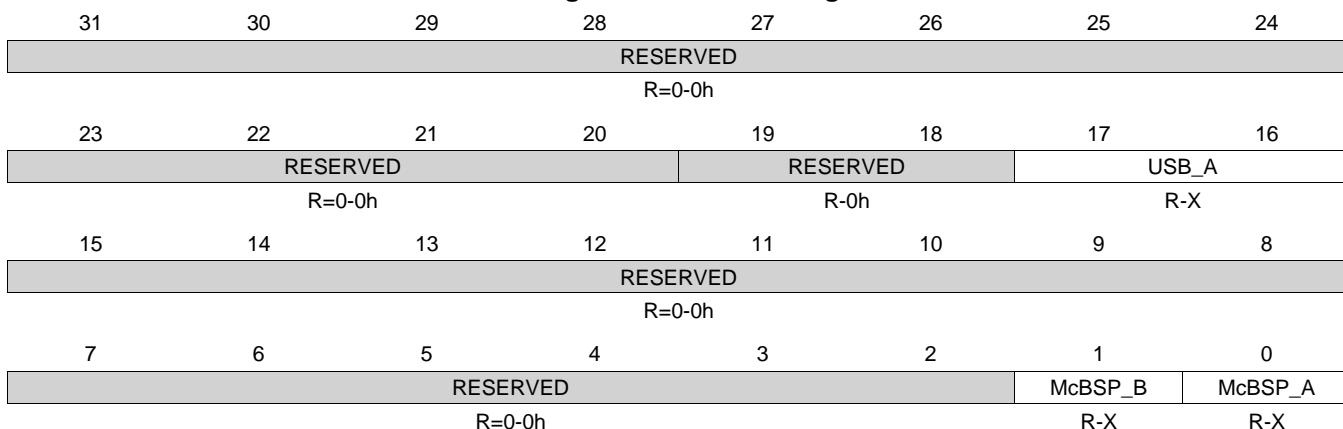
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	CAN_B	R	X	CAN_B : 0: Feature not present on the device 1: Feature present on the device
0	CAN_A	R	X	CAN_A : 0: Feature not present on the device 1: Feature present on the device

1.14.8.17 DC12 Register (offset = 28h) [reset = 0h]

Register mask: FFF0FFFCh

DC12 is shown in [Figure 1-105](#) and described in [Table 1-102](#).

Device Capability: Peripheral Customization

Figure 1-105. DC12 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-102. DC12 Register Field Descriptions

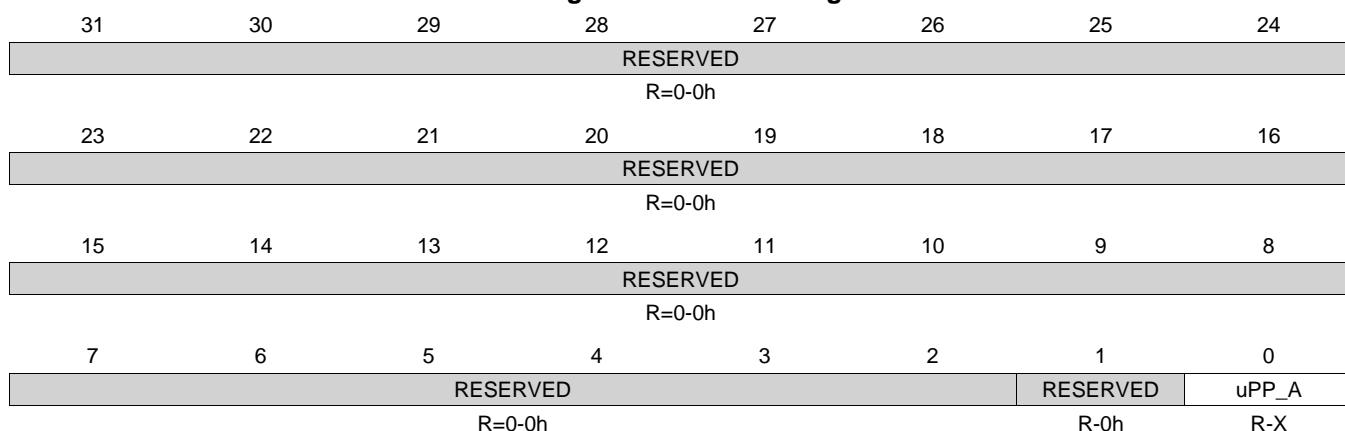
Bit	Field	Type	Reset	Description
31-20	RESERVED	R=0	0h	Reserved
19-18	RESERVED	R	0h	Reserved
17-16	USB_A	R	X	Capability of the USB_A Module: 2'b00: No USB function 2'b01: Device Only 2'b10: Device or Host 2'b11: OTG
15-2	RESERVED	R=0	0h	Reserved
1	McBSP_B	R	X	McBSP_B : 0: Feature not present on the device 1: Feature present on the device
0	McBSP_A	R	X	McBSP_A : 0: Feature not present on the device 1: Feature present on the device

1.14.8.18 DC13 Register (offset = 2Ah) [reset = 0h]

Register mask: FFFFFFFFCh

DC13 is shown in [Figure 1-106](#) and described in [Table 1-103](#).

Device Capability: Peripheral Customization

Figure 1-106. DC13 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-103. DC13 Register Field Descriptions

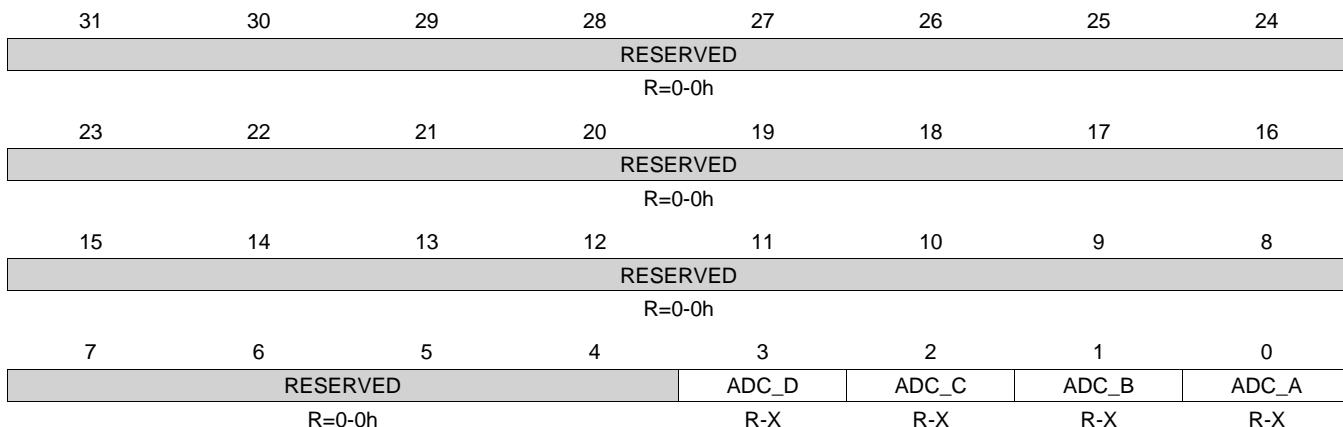
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	RESERVED	R	0h	Reserved
0	uPP_A	R	X	uPP_A : 0: Feature not present on the device 1: Feature present on the device

1.14.8.19 DC14 Register (offset = 2Ch) [reset = 0h]

Register mask: FFFFFFFF0h

DC14 is shown in [Figure 1-107](#) and described in [Table 1-104](#).

Device Capability: Analog Modules Customization

Figure 1-107. DC14 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-104. DC14 Register Field Descriptions

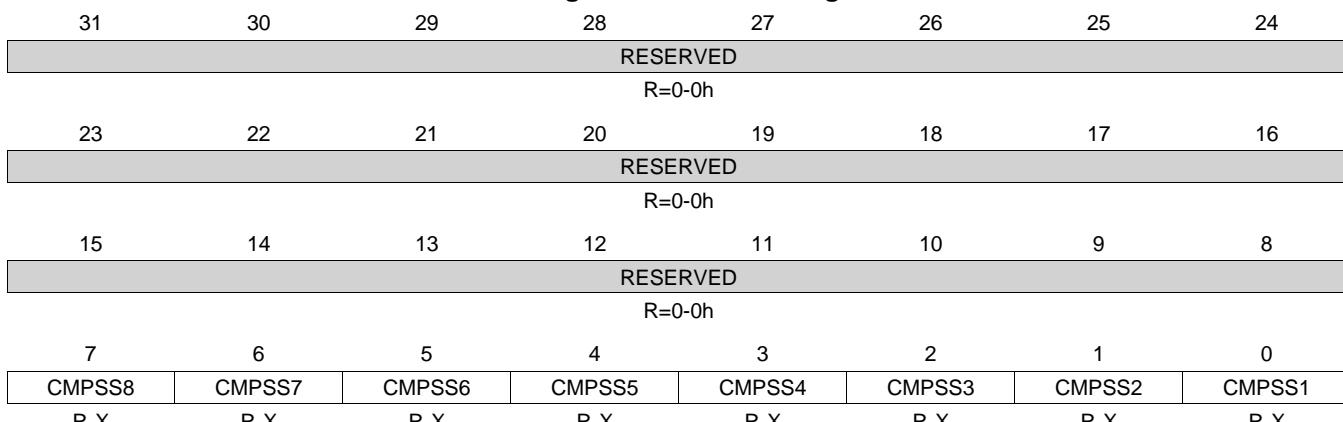
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	ADC_D	R	X	ADC_D : 0: Feature not present on the device 1: Feature present on the device
2	ADC_C	R	X	ADC_C : 0: Feature not present on the device 1: Feature present on the device
1	ADC_B	R	X	ADC_B : 0: Feature not present on the device 1: Feature present on the device
0	ADC_A	R	X	ADC_A : 0: Feature not present on the device 1: Feature present on the device

1.14.8.20 DC15 Register (offset = 2Eh) [reset = 0h]

Register mask: FFFFFFF00h

DC15 is shown in [Figure 1-108](#) and described in [Table 1-105](#).

Device Capability: Analog Modules Customization

Figure 1-108. DC15 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-105. DC15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	CMPSS8	R	X	CMPSS8 : 0: Feature not present on the device 1: Feature present on the device
6	CMPSS7	R	X	CMPSS7 : 0: Feature not present on the device 1: Feature present on the device
5	CMPSS6	R	X	CMPSS6 : 0: Feature not present on the device 1: Feature present on the device
4	CMPSS5	R	X	CMPSS5 : 0: Feature not present on the device 1: Feature present on the device
3	CMPSS4	R	X	CMPSS4 : 0: Feature not present on the device 1: Feature present on the device
2	CMPSS3	R	X	CMPSS3 : 0: Feature not present on the device 1: Feature present on the device
1	CMPSS2	R	X	CMPSS2 : 0: Feature not present on the device 1: Feature present on the device

Table 1-105. DC15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMPSS1	R	X	CMPSS1 : 0: Feature not present on the device 1: Feature present on the device

1.14.8.21 DC17 Register (offset = 32h) [reset = 0h]

Register mask: FFF0FFF0h

DC17 is shown in [Figure 1-109](#) and described in [Table 1-106](#).

Device Capability: Analog Modules Customization

Figure 1-109. DC17 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED			RESERVED		DAC_C	DAC_B	DAC_A
R=0-0h			R-0h		R-X	R-X	R-X
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED		RESERVED	
R=0-0h				R-0h		R-0h	
R=0-0h				R-0h		R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-106. DC17 Register Field Descriptions

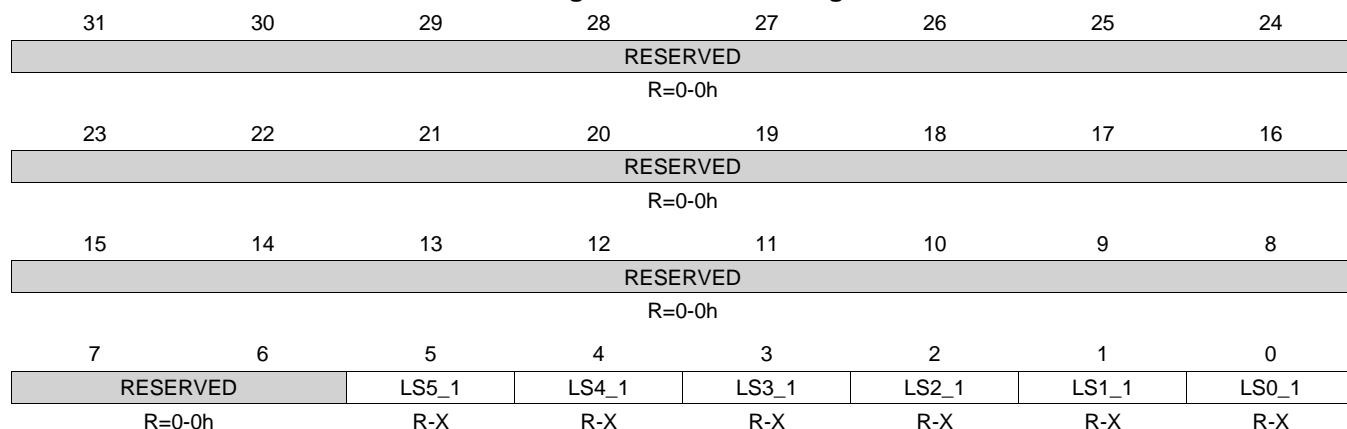
Bit	Field	Type	Reset	Description
31-20	RESERVED	R=0	0h	Reserved
19	RESERVED	R	0h	Reserved
18	DAC_C	R	X	Buffered-DAC_C : 0: Feature not present on the device 1: Feature present on the device
17	DAC_B	R	X	Buffered-DAC_B : 0: Feature not present on the device 1: Feature present on the device
16	DAC_A	R	X	Buffered-DAC_A : 0: Feature not present on the device 1: Feature present on the device
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.8.22 DC18 Register (offset = 34h) [reset = 0h]

Register mask: FFFFFFFC0h

DC18 is shown in [Figure 1-110](#) and described in [Table 1-107](#).

Device Capability: Lx.1 SRAM Customization

Figure 1-110. DC18 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-107. DC18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-6	RESERVED	R=0	0h	Reserved
5	LS5_1	R	X	LS5_1 : 0: Feature not present on the device 1: Feature present on the device
4	LS4_1	R	X	LS4_1 : 0: Feature not present on the device 1: Feature present on the device
3	LS3_1	R	X	LS3_1 : 0: Feature not present on the device 1: Feature present on the device
2	LS2_1	R	X	LS2_1 : 0: Feature not present on the device 1: Feature present on the device
1	LS1_1	R	X	LS1_1 : 0: Feature not present on the device 1: Feature present on the device
0	LS0_1	R	X	LS0_1 : 0: Feature not present on the device 1: Feature present on the device

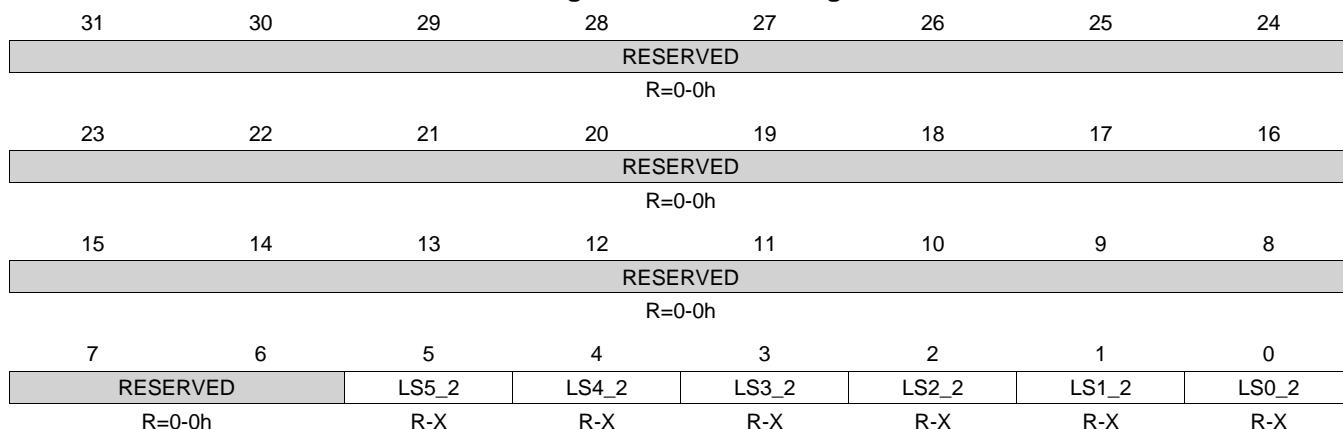
1.14.8.23 DC19 Register (offset = 36h) [reset = 0h]

Register mask: FFFFFFFC0h

DC19 is shown in [Figure 1-111](#) and described in [Table 1-108](#).

Device Capability: Lx.2 SRAM Customization

Figure 1-111. DC19 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-108. DC19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-6	RESERVED	R=0	0h	Reserved
5	LS5_2	R	X	LS5_2 : 0: Feature not present on the device 1: Feature present on the device
4	LS4_2	R	X	LS4_2 : 0: Feature not present on the device 1: Feature present on the device
3	LS3_2	R	X	LS3_2 : 0: Feature not present on the device 1: Feature present on the device
2	LS2_2	R	X	LS2_2 : 0: Feature not present on the device 1: Feature present on the device
1	LS1_2	R	X	LS1_2 : 0: Feature not present on the device 1: Feature present on the device
0	LS0_2	R	X	LS0_2 : 0: Feature not present on the device 1: Feature present on the device

1.14.8.24 DC20 Register (offset = 38h) [reset = 0h]

Register mask: FFFF0000h

DC20 is shown in [Figure 1-112](#) and described in [Table 1-109](#).

Device Capability: GSx SRAM Customization

Figure 1-112. DC20 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X
7	6	5	4	3	2	1	0
GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-109. DC20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15	GS15	R	X	GS15 : 0: Feature not present on the device 1: Feature present on the device
14	GS14	R	X	GS14 : 0: Feature not present on the device 1: Feature present on the device
13	GS13	R	X	GS13 : 0: Feature not present on the device 1: Feature present on the device
12	GS12	R	X	GS12 : 0: Feature not present on the device 1: Feature present on the device
11	GS11	R	X	GS11 : 0: Feature not present on the device 1: Feature present on the device
10	GS10	R	X	GS10 : 0: Feature not present on the device 1: Feature present on the device
9	GS9	R	X	GS9 : 0: Feature not present on the device 1: Feature present on the device
8	GS8	R	X	GS8 : 0: Feature not present on the device 1: Feature present on the device

Table 1-109. DC20 Register Field Descriptions (continued)

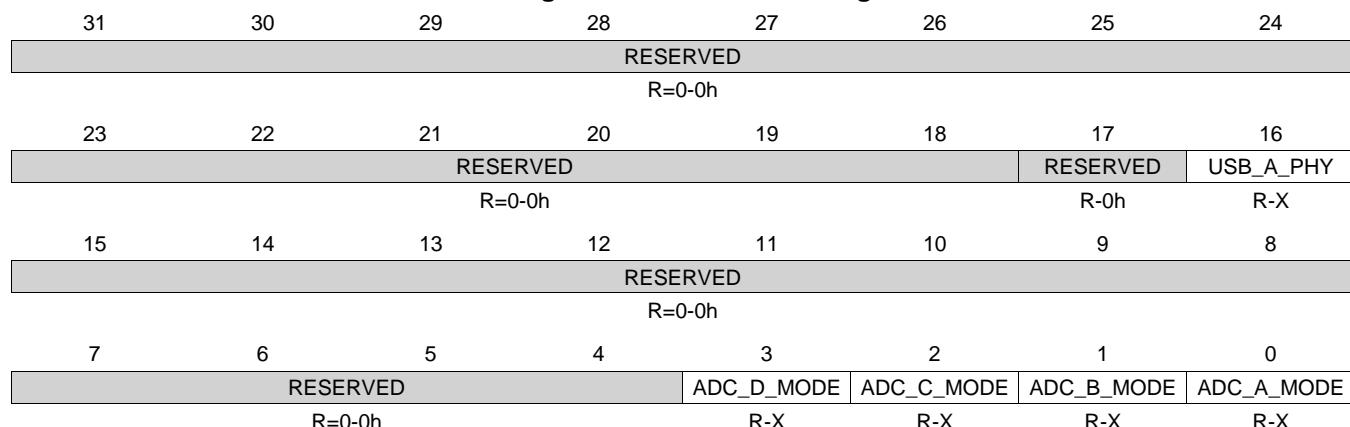
Bit	Field	Type	Reset	Description
7	GS7	R	X	GS7 : 0: Feature not present on the device 1: Feature present on the device
6	GS6	R	X	GS6 : 0: Feature not present on the device 1: Feature present on the device
5	GS5	R	X	GS5 : 0: Feature not present on the device 1: Feature present on the device
4	GS4	R	X	GS4 : 0: Feature not present on the device 1: Feature present on the device
3	GS3	R	X	GS3 : 0: Feature not present on the device 1: Feature present on the device
2	GS2	R	X	GS2 : 0: Feature not present on the device 1: Feature present on the device
1	GS1	R	X	GS1 : 0: Feature not present on the device 1: Feature present on the device
0	GS0	R	X	GS0 : 0: Feature not present on the device 1: Feature present on the device

1.14.8.25 PERCNF1 Register (offset = 60h) [reset = 0h]

Register mask: FFFCFFF0h

PERCNF1 is shown in [Figure 1-113](#) and described in [Table 1-110](#).

Peripheral Configuration register

Figure 1-113. PERCNF1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-110. PERCNF1 Register Field Descriptions

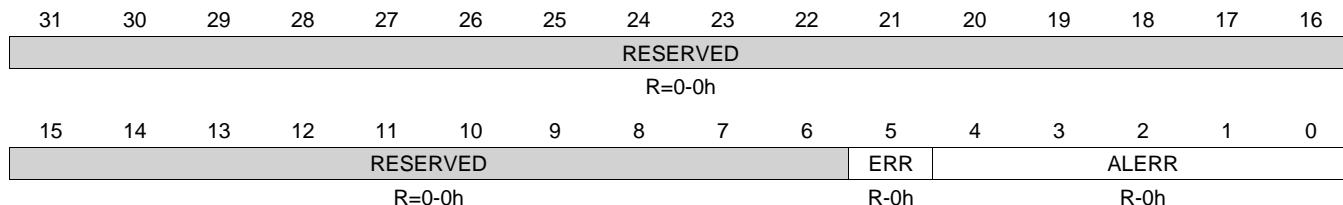
Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	USB_A_PHY	R	X	Internal PHY is present or not for the USB_A module: 0: Internal USB PHY Module is not present 1: Internal USB PHY Module is present.
15-4	RESERVED	R=0	0h	Reserved
3	ADC_D_MODE	R	X	0: 16-bit or 12-bit configurable in software 1: Only 12-bit operation available
2	ADC_C_MODE	R	X	0: 16-bit or 12-bit configurable in software 1: Only 12-bit operation available
1	ADC_B_MODE	R	X	0: 16-bit or 12-bit configurable in software 1: Only 12-bit operation available
0	ADC_A_MODE	R	X	0: 16-bit or 12-bit configurable in software 1: Only 12-bit operation available

1.14.8.26 FUSEERR Register (offset = 74h) [reset = 0h]

FUSEERR is shown in [Figure 1-114](#) and described in [Table 1-111](#).

e-Fuse error Status register

Figure 1-114. FUSEERR Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-111. FUSEERR Register Field Descriptions

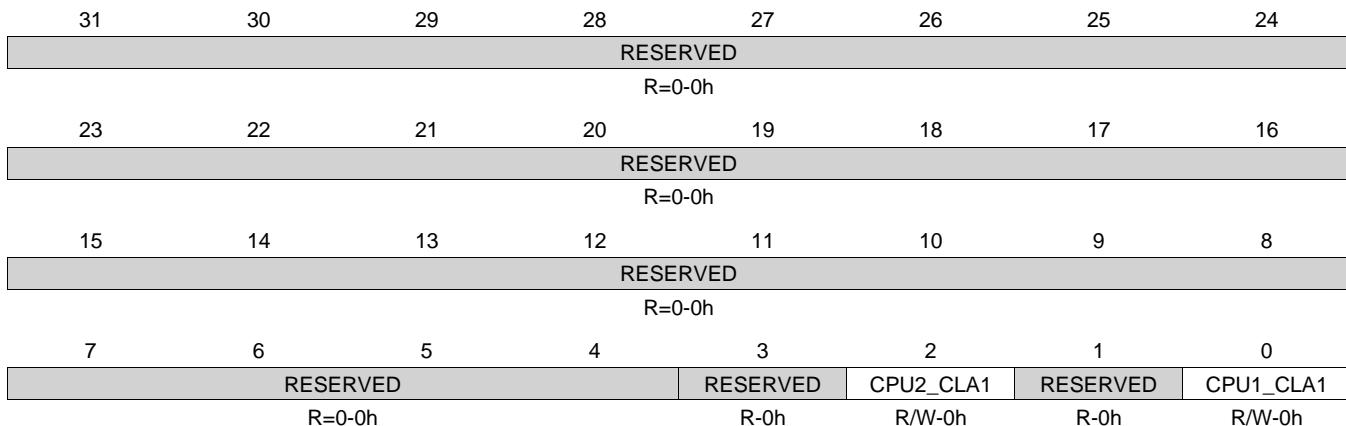
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-6	RESERVED	R=0	0h	Reserved
5	ERR	R	0h	Efuse Self Test Error Status set by hardware after fuse self test completes, in case of self test error 0: No error during fuse self test 1: Fuse self test error
4-0	ALERR	R	0h	Efuse Autoload Error Status set by hardware after fuse auto load completes 00000: No error in auto load Other: Non zero value indicates error in autoload

1.14.8.27 SOFTPRES0 Register (offset = 82h) [reset = 0h]

SOFTPRES0 is shown in [Figure 1-115](#) and described in [Table 1-112](#).

Processing Block Software Reset register

When bits in this register are set, the respective module is in reset. All design data is lost and the module registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-115. SOFTPRES0 Register

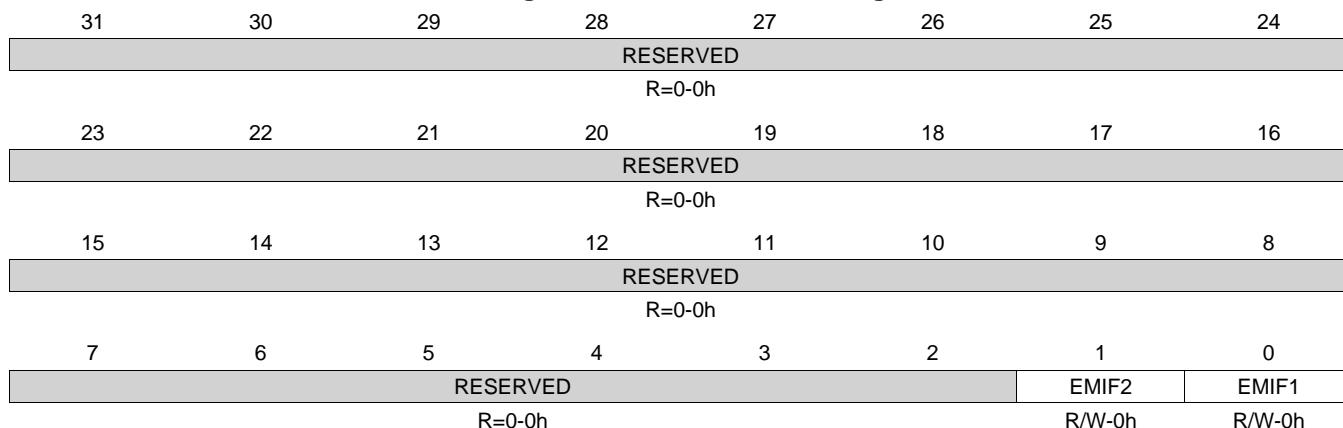
LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 1-112. SOFTPRES0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	CPU2_CLA1	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
1	RESERVED	R	0h	Reserved
0	CPU1_CLA1	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.28 SOFTPRES1 Register (offset = 84h) [reset = 0h]SOFTPRES1 is shown in [Figure 1-116](#) and described in [Table 1-113](#).

EMIF Software Reset register

Figure 1-116. SOFTPRES1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-113. SOFTPRES1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	EMIF2	R/W	0h	When this bit is set, only the control logic of the respective EMIF2 is reset. It does not reset the internal registers except the Total Access register and the Total Activate register. Refer to EMIF spec for more details on the EMIF SOFTRESET feature. This bit must be manually cleared after being set. 1: EMIF2 is under SOFTRESET 0: Module reset is determined by the device Reset Network
0	EMIF1	R/W	0h	When this bit is set, only the control logic of the respective EMIF1 is reset. It does not reset the internal registers except the Total Access register and the Total Activate register. Refer to EMIF spec for more details on the EMIF SOFTRESET feature. This bit must be manually cleared after being set. 1: EMIF1 is under SOFTRESET 0: Module reset is determined by the device Reset Network

1.14.8.29 SOFTPRES2 Register (offset = 86h) [reset = 0h]

SOFTPRES2 is shown in [Figure 1-117](#) and described in [Table 1-114](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-117. SOFTPRES2 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	EPWM12	EPWM11	EPWM10	EPWM9
R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EPWM8	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-114. SOFTPRES2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	EPWM12	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
10	EPWM11	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
9	EPWM10	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
8	EPWM9	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
7	EPWM8	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
6	EPWM7	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
5	EPWM6	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
4	EPWM5	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
3	EPWM4	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

Table 1-114. SOFTPRES2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EPWM3	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
1	EPWM2	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	EPWM1	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.30 SOFTPRES3 Register (offset = 88h) [reset = 0h]

SOFTPRES3 is shown in [Figure 1-118](#) and described in [Table 1-115](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-118. SOFTPRES3 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	ECAP6	ECAP5	ECAP4	ECAP3	ECAP2	ECAP1
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-115. SOFTPRES3 Register Field Descriptions

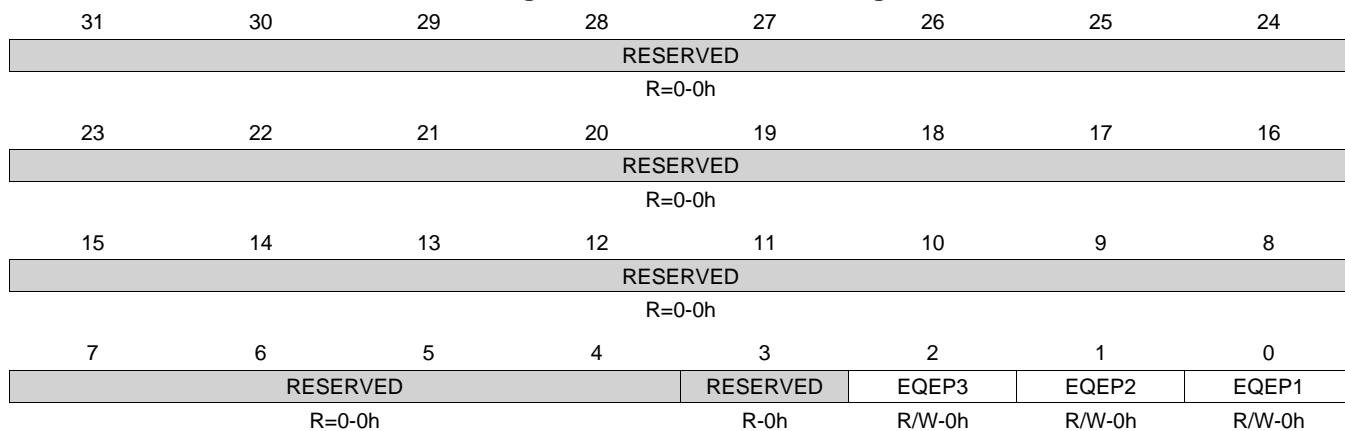
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	ECAP6	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
4	ECAP5	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
3	ECAP4	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
2	ECAP3	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
1	ECAP2	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	ECAP1	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.31 SOFTPRES4 Register (offset = 8Ah) [reset = 0h]

SOFTPRES4 is shown in [Figure 1-119](#) and described in [Table 1-116](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-119. SOFTPRES4 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-116. SOFTPRES4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	EQEP3	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
1	EQEP2	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	EQEP1	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

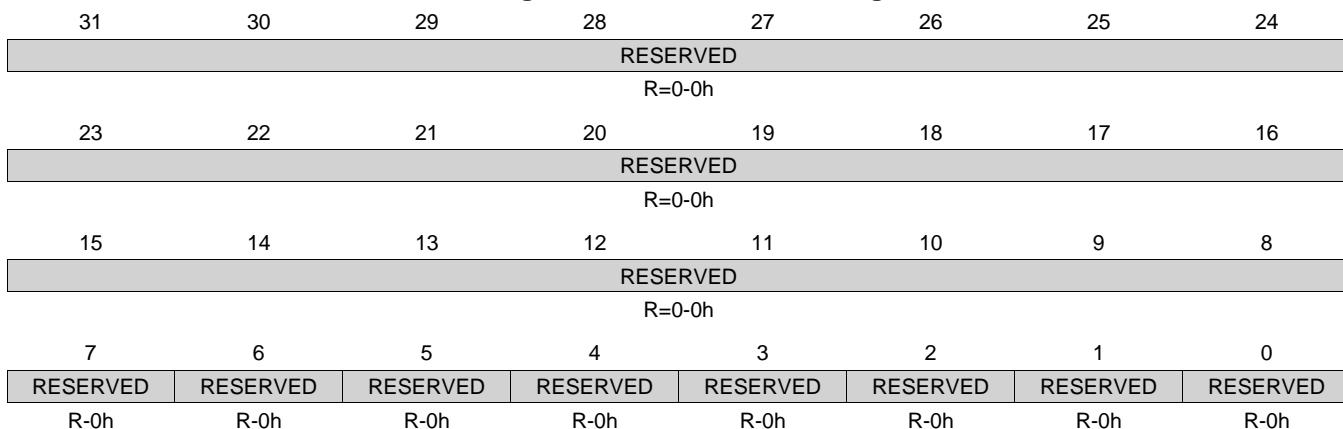
1.14.8.32 SOFTPRES5 Register (offset = 8Ch) [reset = 0h]

SOFTPRES5 is shown in [Figure 1-120](#) and described in [Table 1-117](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-120. SOFTPRES5 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-117. SOFTPRES5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.8.33 SOFTPRES6 Register (offset = 8Eh) [reset = 0h]

SOFTPRES6 is shown in [Figure 1-121](#) and described in [Table 1-118](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-121. SOFTPRES6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R=0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESE RVED	RESE RVED	RESE RVED	RESE RVED	RESE RVED	RESE RVED	SD2	SD1
R=0-0h								R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W- 0h
R-0h								R/W- 0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-118. SOFTPRES6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	SD2	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	SD1	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.34 SOFTPRES7 Register (offset = 90h) [reset = 0h]

SOFTPRES7 is shown in [Figure 1-122](#) and described in [Table 1-119](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-122. SOFTPRES7 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				SCI_D	SCI_C	SCI_B	SCI_A
R=0-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-119. SOFTPRES7 Register Field Descriptions

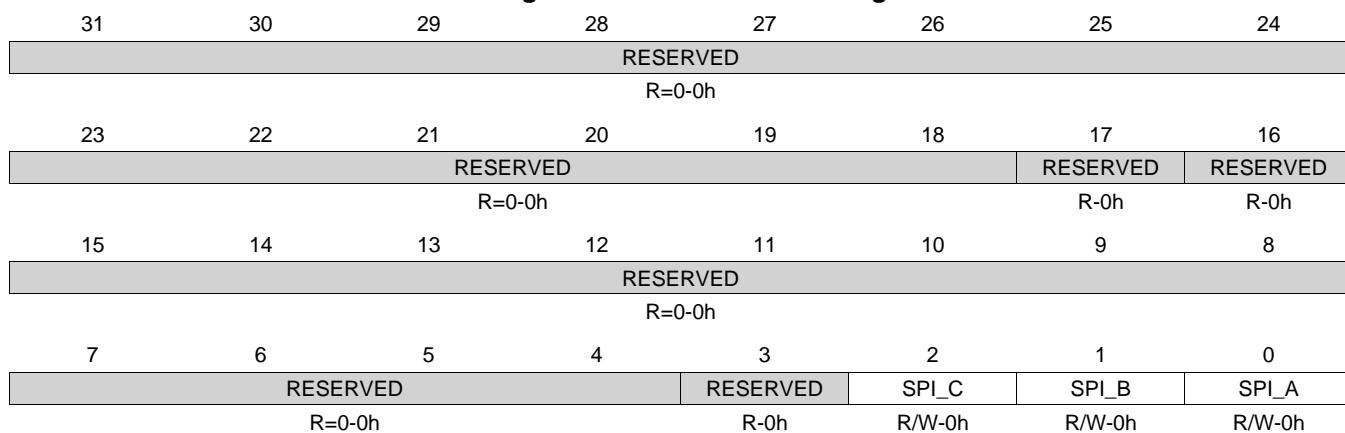
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	SCI_D	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
2	SCI_C	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
1	SCI_B	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	SCI_A	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.35 SOFTPRES8 Register (offset = 92h) [reset = 0h]

SOFTPRES8 is shown in [Figure 1-123](#) and described in [Table 1-120](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-123. SOFTPRES8 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-120. SOFTPRES8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	SPI_C	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
1	SPI_B	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	SPI_A	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.36 SOFTPRES9 Register (offset = 94h) [reset = 0h]

SOFTPRES9 is shown in [Figure 1-124](#) and described in [Table 1-121](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-124. SOFTPRES9 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED							
R=0-0h							
						I2C_B	I2C_A
						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-121. SOFTPRES9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	I2C_B	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	I2C_A	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.37 SOFTPRES11 Register (offset = 98h) [reset = 0h]

SOFTPRES11 is shown in [Figure 1-125](#) and described in [Table 1-122](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-125. SOFTPRES11 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED							
R=0-0h							
R/W-0h							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-122. SOFTPRES11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	USB_A	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
15-2	RESERVED	R=0	0h	Reserved
1	McBSP_B	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	McBSP_A	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.38 SOFTPRES13 Register (offset = 9Ch) [reset = 0h]

SOFTPRES13 is shown in [Figure 1-126](#) and described in [Table 1-123](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-126. SOFTPRES13 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				ADC_D	ADC_C	ADC_B	ADC_A
R=0-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-123. SOFTPRES13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	ADC_D	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
2	ADC_C	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
1	ADC_B	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	ADC_A	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.39 SOFTPRES14 Register (offset = 9Eh) [reset = 0h]

SOFTPRES14 is shown in [Figure 1-127](#) and described in [Table 1-124](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-127. SOFTPRES14 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
CMPSS8	CMPSS7	CMPSS6	CMPSS5	CMPSS4	CMPSS3	CMPSS2	CMPSS1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-124. SOFTPRES14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	CMPSS8	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
6	CMPSS7	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
5	CMPSS6	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
4	CMPSS5	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
3	CMPSS4	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
2	CMPSS3	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
1	CMPSS2	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
0	CMPSS1	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure

1.14.8.40 SOFTPRES16 Register (offset = A2h) [reset = 0h]

SOFTPRES16 is shown in [Figure 1-128](#) and described in [Table 1-125](#).

Peripheral Software Reset register

When bits in this register are set, the respective peripheral is in reset. All data is lost and the peripheral registers are returned to their reset states. Bits must be manually cleared after being set.

Figure 1-128. SOFTPRES16 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED				RESERVED	DAC_C	DAC_B	DAC_A
R=0-0h				R-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	RESERVED	RESERVED
R=0-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-125. SOFTPRES16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R=0	0h	Reserved
19	RESERVED	R	0h	Reserved
18	DAC_C	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
17	DAC_B	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
16	DAC_A	R/W	0h	1: Module is under reset 0: Module reset is determined by the normal device reset structure
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.8.41 CPUSEL0 Register (offset = D6h) [reset = 0h]

CPUSEL0 is shown in [Figure 1-129](#) and described in [Table 1-126](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-129. CPUSEL0 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	EPWM12	EPWM11	EPWM10	EPWM9
R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EPWM8	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-126. CPUSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	EPWM12	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
10	EPWM11	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
9	EPWM10	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
8	EPWM9	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
7	EPWM8	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
6	EPWM7	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
5	EPWM6	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
4	EPWM5	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

Table 1-126. CPUSEL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EPWM4	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
2	EPWM3	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
1	EPWM2	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	EPWM1	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.42 CPUSEL1 Register (offset = D8h) [reset = 0h]

CPUSEL1 is shown in [Figure 1-130](#) and described in [Table 1-127](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-130. CPUSEL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	ECAP6	ECAP5	ECAP4	ECAP3	ECAP2	ECAP1
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-127. CPUSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	ECAP6	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
4	ECAP5	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
3	ECAP4	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
2	ECAP3	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
1	ECAP2	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	ECAP1	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.43 CPUSEL2 Register (offset = DAh) [reset = 0h]

CPUSEL2 is shown in [Figure 1-131](#) and described in [Table 1-128](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-131. CPUSEL2 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	EQEP3	EQEP2	EQEP1
R=0-0h				R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-128. CPUSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	EQEP3	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
1	EQEP2	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	EQEP1	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.44 CPUSEL3 Register (offset = DCh) [reset = 0h]

CPUSEL3 is shown in [Figure 1-132](#) and described in [Table 1-129](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-132. CPUSEL3 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-129. CPUSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.8.45 CPUSEL4 Register (offset = DEh) [reset = 0h]

CPUSEL4 is shown in [Figure 1-133](#) and described in [Table 1-130](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-133. CPUSEL4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R=0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESE RVED	RESE RVED	RESE RVED	RESE RVED	RESE RVED	RESE RVED	SD2	SD1
R=0-0h								R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W- 0h	R/W- 0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-130. CPUSEL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	SD2	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	SD1	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.46 CPUSEL5 Register (offset = E0h) [reset = 0h]

CPUSEL5 is shown in [Figure 1-134](#) and described in [Table 1-131](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-134. CPUSEL5 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				SCI_D	SCI_C	SCI_B	SCI_A
R=0-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-131. CPUSEL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	SCI_D	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
2	SCI_C	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
1	SCI_B	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	SCI_A	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.47 CPUSEL6 Register (offset = E2h) [reset = 0h]

CPUSEL6 is shown in [Figure 1-135](#) and described in [Table 1-132](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-135. CPUSEL6 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED						RESERVED	RESERVED
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	SPI_C	SPI_B	SPI_A
R=0-0h				R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-132. CPUSEL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	SPI_C	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
1	SPI_B	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	SPI_A	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.48 CPUSEL7 Register (offset = E4h) [reset = 0h]

CPUSEL7 is shown in [Figure 1-136](#) and described in [Table 1-133](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-136. CPUSEL7 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED						RESERVED	RESERVED
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED						I2C_B	I2C_A
R=0-0h							
R/W-0h							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-133. CPUSEL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	I2C_B	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	I2C_A	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.49 CPUSEL8 Register (offset = E6h) [reset = 0h]

CPUSEL8 is shown in [Figure 1-137](#) and described in [Table 1-134](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-137. CPUSEL8 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	CAN_B	CAN_A
R=0-0h				R-0h	R-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-134. CPUSEL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	CAN_B	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	CAN_A	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.50 CPUSEL9 Register (offset = E8h) [reset = 0h]

CPUSEL9 is shown in [Figure 1-138](#) and described in [Table 1-135](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-138. CPUSEL9 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED					McBSP_B		McBSP_A
R=0-0h					R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-135. CPUSEL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	McBSP_B	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	McBSP_A	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.51 CPUSEL11 Register (offset = ECh) [reset = 0h]

CPUSEL11 is shown in [Figure 1-139](#) and described in [Table 1-136](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-139. CPUSEL11 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				ADC_D	ADC_C	ADC_B	ADC_A
R=0-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-136. CPUSEL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	ADC_D	R/W	0h	<p>0: Connected to CPU1 1: Connected to CPU2</p> <p>Note:</p> <p>[1] These CPUSEL bits affect the ownership of only ADC Configuration registers by CPU1 or CPU2 (which are mapped on the mapped to VBUS32). ADC result registers are readable from all masters without any CPUSEL dependency.</p>
2	ADC_C	R/W	0h	<p>0: Connected to CPU1 1: Connected to CPU2</p> <p>Note:</p> <p>[1] These CPUSEL bits affect the ownership of only ADC Configuration registers by CPU1 or CPU2 (which are mapped on the mapped to VBUS32). ADC result registers are readable from all masters without any CPUSEL dependency.</p>
1	ADC_B	R/W	0h	<p>0: Connected to CPU1 1: Connected to CPU2</p> <p>Note:</p> <p>[1] These CPUSEL bits affect the ownership of only ADC Configuration registers by CPU1 or CPU2 (which are mapped on the mapped to VBUS32). ADC result registers are readable from all masters without any CPUSEL dependency.</p>

Table 1-136. CPUSEL11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADC_A	R/W	0h	<p>0: Connected to CPU1 1: Connected to CPU2</p> <p>Note:</p> <p>[1] These CPUSEL bits affect the ownership of only ADC Configuration registers by CPU1 or CPU2 (which are mapped on the mapped to VBUS32). ADC result registers are readable from all masters without any CPUSEL dependency.</p>

1.14.8.52 CPUSEL12 Register (offset = EEh) [reset = 0h]

CPUSEL12 is shown in [Figure 1-140](#) and described in [Table 1-137](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-140. CPUSEL12 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
CMPSS8	CMPSS7	CMPSS6	CMPSS5	CMPSS4	CMPSS3	CMPSS2	CMPSS1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-137. CPUSEL12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	CMPSS8	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
6	CMPSS7	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
5	CMPSS6	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
4	CMPSS5	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
3	CMPSS4	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
2	CMPSS3	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
1	CMPSS2	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
0	CMPSS1	R/W	0h	0: Connected to CPU1 1: Connected to CPU2

1.14.8.53 CPUSEL14 Register (offset = F2h) [reset = 0h]

CPUSEL14 is shown in [Figure 1-141](#) and described in [Table 1-138](#).

CPU Select register for common peripherals

This register must be configured prior to enabling the peripheral clocks.

The clock for each peripheral is derived from the selected CPU subsystem. The clock mux controlled by this register is not glitch-free, therefore the CPUSELx register must be configured before the PCLKCRx register.

The reset for each peripheral is also driven from the selected CPU.

Figure 1-141. CPUSEL14 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED				RESERVED	DAC_C	DAC_B	DAC_A
R=0-0h				R-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	RESERVED	RESERVED
R=0-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

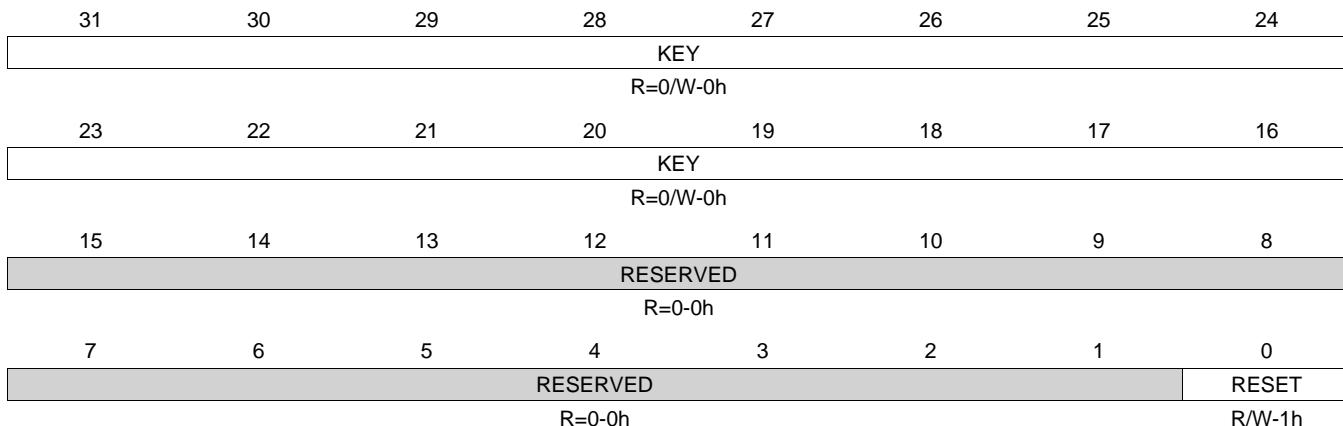
Table 1-138. CPUSEL14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R=0	0h	Reserved
19	RESERVED	R	0h	Reserved
18	DAC_C	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
17	DAC_B	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
16	DAC_A	R/W	0h	0: Connected to CPU1 1: Connected to CPU2
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.8.54 CPU2RESCTL Register (offset = 122h) [reset = 1h]

CPU2RESCTL is shown in [Figure 1-142](#) and described in [Table 1-139](#).

CPU2 Reset Control Register

Figure 1-142. CPU2RESCTL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

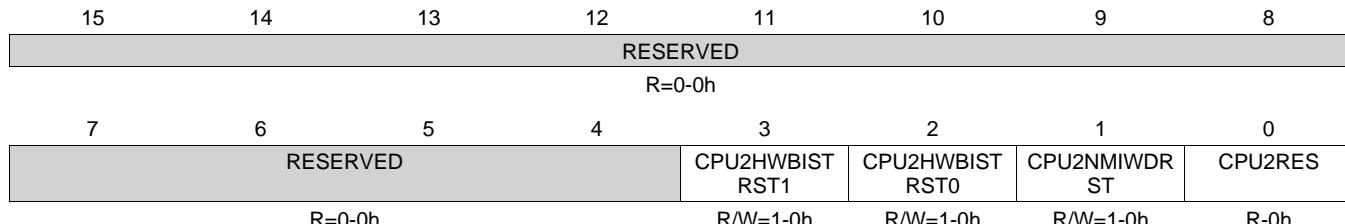
Table 1-139. CPU2RESCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R=0/W	0h	<p>Write to this register succeeds only if this field is written with a value of 0xa5a5</p> <p>Note:</p> <p>[1] Due to this KEY, only 32-bit writes will succeed (provided the KEY matches). 16-bit writes to the upper or lower half of this register will be ignored</p>
15-1	RESERVED	R=0	0h	Reserved
0	RESET	R/W	1h	<p>This bit controls the reset input of CPU2 core.</p> <p>1: CPU2 is held in reset (CPU2.RSn = 0)</p> <p>0: CPU2 reset is deactivated (CPU2.RSn = 1)</p> <p>Note:</p> <p>[1] If CPU2 is not used at-all by an application, it's advisable to put CPU2 in STANDBY mode rather than in reset to save on active power component on the CPU2 subsystem. This is because, all clocks keep toggling when reset is active on the CPU2 sub-system.</p>

1.14.8.55 RSTSTAT Register (offset = 124h) [reset = 0h]

RSTSTAT is shown in [Figure 1-143](#) and described in [Table 1-140](#).

Reset Status register for secondary C28x CPUs

Figure 1-143. RSTSTAT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

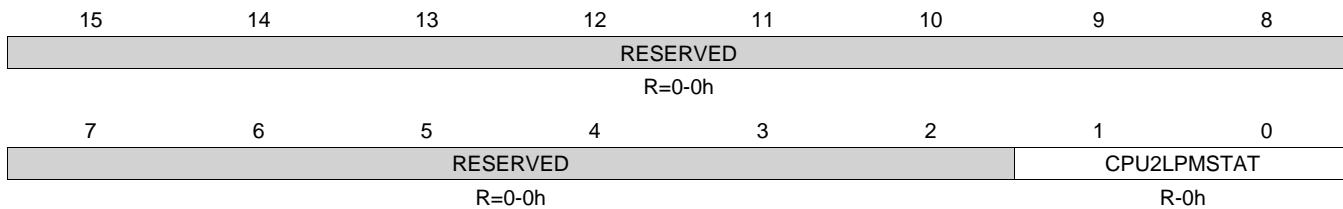
Table 1-140. RSTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3	CPU2HWBISTRST1	R/W=1	0h	CPU2HWBISTRST0 and CPU2HWBISTRST1 together indicates whether a HWBIST reset was issued to CPU2 or not 00: CPU2 was not reset by the CPU2 HWBIST 11: CPU2 was reset due to CPU2 HWBIST reset This status bit is a latched flag. This flag can be cleared by the CPU1 by writing a 1
2	CPU2HWBISTRST0	R/W=1	0h	CPU2HWBISTRST0 and CPU2HWBISTRST1 together indicates whether a HWBIST reset was issued to CPU2 or not 00: CPU2 was not reset by the CPU2 HWBIST 11: CPU2 was reset due to CPU2 HWBIST reset This status bit is a latched flag. This flag can be cleared by the CPU1 by writing a 1
1	CPU2NMIWDRST	R/W=1	0h	Indicates whether a CPU2.NMIWD reset was issued to CPU2 or not 0: CPU2 was not reset by the CPU2.NMIWD 1: CPU2 was reset due to CPU2.NMIWD reset This status bit is a latched flag. This flag can be cleared by the CPU1 by writing a 1
0	CPU2RES	R	0h	Reset status of CPU2 to CPU1 0: CPU2 core is in reset 1: CPU2 core is out of reset

1.14.8.56 LPMSTAT Register (offset = 125h) [reset = 0h]

LPMSTAT is shown in [Figure 1-144](#) and described in [Table 1-141](#).

LPM Status Register for secondary C28x CPUs

Figure 1-144. LPMSTAT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; $-n$ = value after reset

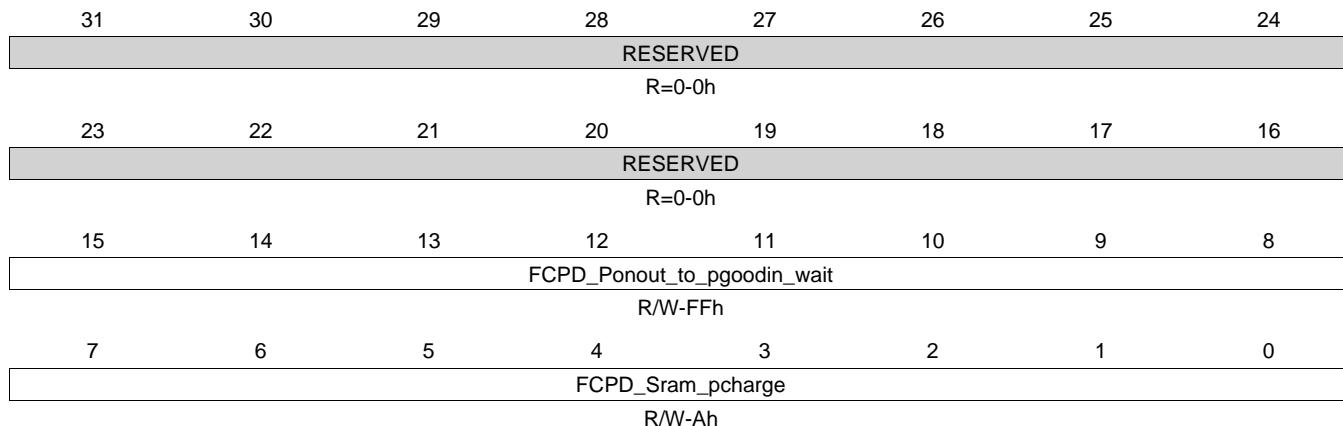
Table 1-141. LPMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R=0	0h	Reserved
1-0	CPU2LPMSTAT	R	0h	These bits indicate the power mode CPU2 00: CPU2 is in ACTIVE mode 01: CPU2 is in IDLE mode 10: CPU2 is in STANDBY mode 11: Reserved

1.14.8.57 PSCONCTL1 Register (offset = 126h) [reset = FF0Ah]

PSCONCTL1 is shown in [Figure 1-145](#) and described in [Table 1-142](#).

Register for PSCON Configuration

Figure 1-145. PSCONCTL1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

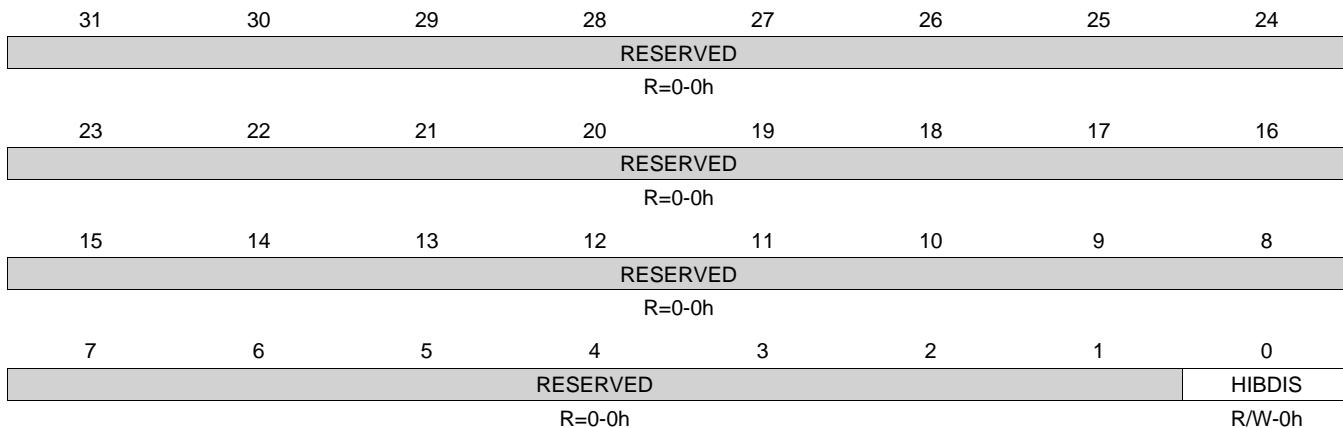
Table 1-142. PSCONCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	FCPD_Ponout_to_pgoodin_wait	R/W	FFh	This bit field is connected to FCPD.PSCON.Ponout_to_pgoodin_wait input
7-0	FCPD_Sram_pcharge	R/W	Ah	This bit field is connected to FCPD.PSCON.Sram_pcharge input

1.14.8.58 SYSDBGCTL Register (offset = 12Ch) [reset = 0h]

SYSDBGCTL is shown in [Figure 1-146](#) and described in [Table 1-143](#).

System Debug Control register

Figure 1-146. SYSDBGCTL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 1-143. SYSDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-1	RESERVED	R=0	0h	Reserved
0	HIBDIS	R/W	0h	<p>This bit defines if system is allowed to enter HIB mode when debugger is connected.</p> <p>0: System can enter HIB mode when debugger is connected</p> <p>1: System can't enter HIB mode when debugger is connected. Instead, system will enter HALT mode.</p> <p>Note:</p> <p>[1] This bit takes effect only when CPU1.DCON=1 indicating emulator is connected. Otherwise, this bit has no effect</p> <p>[2] This bit is in PORn to make sure that the configuration is retained even after debugger reset or WD reset (while the debugger is connected)</p>

1.14.9 CLK_CFG_REGS Registers

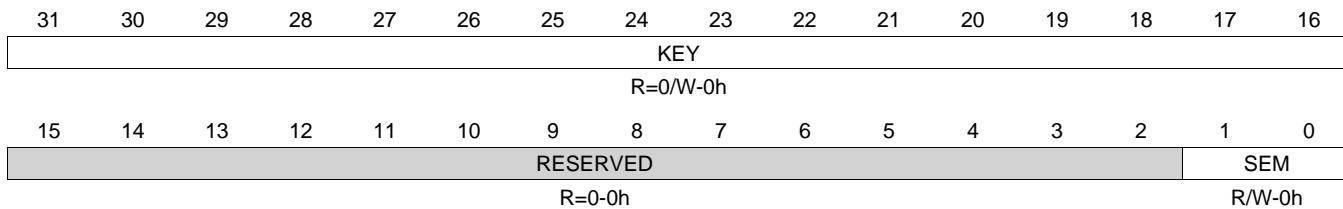
Table 1-144 lists the memory-mapped registers for the CLK_CFG_REGS. All register offset addresses not listed in Table 1-144 should be considered as reserved locations and the register contents should not be modified.

Table 1-144. CLK_CFG_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	CLKSEM	Clock Control Semaphore Register	Section 1.14.9.1	EALLOW
2h	CLKCFGLOCK1	Lock bit for CLKCFG registers	Section 1.14.9.2	EALLOW
8h	CLKSRCCTL1	Clock Source Control register-1	Section 1.14.9.3	EALLOW
Ah	CLKSRCCTL2	Clock Source Control register-2	Section 1.14.9.4	EALLOW
Ch	CLKSRCCTL3	Clock Source Control register-3	Section 1.14.9.5	EALLOW
Eh	SYSPLLCTL1	SYSPLL Control register-1	Section 1.14.9.6	EALLOW
14h	SYSPLLMULT	SYSPLL Multiplier register	Section 1.14.9.7	EALLOW
16h	SYSPLLSTS	SYSPLL Status register	Section 1.14.9.8	
18h	AUXPLLCTL1	AUXPLL Control register-1	Section 1.14.9.9	EALLOW
1Eh	AUXPLLMULT	AUXPLL Multiplier register	Section 1.14.9.10	EALLOW
20h	AUXPLLSTS	AUXPLL Status register	Section 1.14.9.11	
22h	SYCLKDIVSEL	System Clock Divider Select register	Section 1.14.9.12	EALLOW
24h	AUXCLKDIVSEL	Auxillary Clock Divider Select register	Section 1.14.9.13	EALLOW
26h	PERCLKDIVSEL	Peripheral Clock Divider Selet register	Section 1.14.9.14	EALLOW
28h	XCLKOUTDIVSEL	XCLKOUT Divider Select register	Section 1.14.9.15	EALLOW
2Ch	LOSPCP	Low Speed Clock Source Prescalar	Section 1.14.9.16	EALLOW
2Eh	MCDCR	Missing Clock Detect Control Register	Section 1.14.9.17	EALLOW
30h	X1CNT	10-bit Counter on X1 Clock	Section 1.14.9.18	

1.14.9.1 CLKSEM Register (offset = 0h) [reset = 0h]CLKSEM is shown in [Figure 1-147](#) and described in [Table 1-145](#).

Clock Control Semaphore Register

Figure 1-147. CLKSEM Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-145. CLKSEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R=0/W	0h	<p>Writing the value 0xa5a5 will allow the writing of the SEM bits, else writes are ignored. Reads will return 0.</p> <p>Note:</p> <p>[1] Due to this KEY, only 32-bit writes will succeed (provided the KEY matches). 16-bit writes to the upper or lower half of this register will be ignored</p>
15-2	RESERVED	R=0	0h	Reserved
1-0	SEM	R/W	0h	<p>This register provides a mechanism to acquire all the CLKCFG registers (except this register) by CPU1 or CPU2. A CPU can perform read/writes to any of the CLKCFG registers (except this register) only if it owns the semaphore. Otherwise, writes are ignored and reads will return 0x0.</p> <p>Semaphore State Transitions:</p> <p>A value of 00, 10, 11 gives ownership to CPU1</p> <p>A value of 01 gives ownership to CPU2.</p> <p>The following are the only state transitions allowed on these bits.</p> <p>00,11 <-> 01 (allowed by CPU2)</p> <p>00,11 <-> 10 (allowed by CPU1)</p> <p>If a CPU doesn't own the CLK_CFG_REGS set of registers (as defined by the state of this semaphore), reads from that CPU to all those registers return 0x0 and writes are ignore. Note that this is not true of CLKSEM register. The CLKSEM register's reads and writes are always allowed from both CPU1 and CPU2.</p>

1.14.9.2 CLKCFGLOCK1 Register (offset = 2h) [reset = 0h]

CLKCFGLOCK1 is shown in [Figure 1-148](#) and described in [Table 1-146](#).

Lock bit for CLKCFG registers

Notes:

[1] Any bit in this register, once set can only be cleared through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect

[2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed

Figure 1-148. CLKCFGLOCK1 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
LOSPCP	RESERVED	PERCLKDIVSEL	AUXCLKDIVSEL	SYSCLKDIVSEL	AUXPLLMMULT	RESERVED	RESERVED
R/SOnce-0h	R=0-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R=0-0h	R=0-0h
7	6	5	4	3	2	1	0
AUXPLLCTL1	SYSPLLMMULT	SYSPLLCTL3	SYSPLLCTL2	SYSPLLCTL1	CLKSRCCTL3	CLKSRCCTL2	CLKSRCCTL1
R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-146. CLKCFGLOCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15	LOSPCP	R/SOnce	0h	Lock bit for LOSPCP register: 0: Respective register is not locked 1: Respective register is locked.
14	RESERVED	R=0	0h	Reserved
13	PERCLKDIVSEL	R/SOnce	0h	Lock bit for PERCLKDIVSEL register: 0: Respective register is not locked 1: Respective register is locked.
12	AUXCLKDIVSEL	R/SOnce	0h	Lock bit for AUXCLKDIVSEL register: 0: Respective register is not locked 1: Respective register is locked.
11	SYSCLKDIVSEL	R/SOnce	0h	Lock bit for SYSCLKDIVSEL register: 0: Respective register is not locked 1: Respective register is locked.
10	AUXPLLMMULT	R/SOnce	0h	Lock bit for AUXPLLMMULT register: 0: Respective register is not locked 1: Respective register is locked.
9	RESERVED	R=0	0h	Reserved
8	RESERVED	R=0	0h	Reserved
7	AUXPLLCTL1	R/SOnce	0h	Lock bit for AUXPLLCTL1 register: 0: Respective register is not locked 1: Respective register is locked.

Table 1-146. CLKCFGLOCK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SYSPLLMULT	R/SOnce	0h	Lock bit for SYSPLLMULT register: 0: Respective register is not locked 1: Respective register is locked.
5	SYSPLLCTL3	R/SOnce	0h	Lock bit for SYSPLLCTL3 register: 0: Respective register is not locked 1: Respective register is locked.
4	SYSPLLCTL2	R/SOnce	0h	Lock bit for SYSPLLCTL2 register: 0: Respective register is not locked 1: Respective register is locked.
3	SYSPLLCTL1	R/SOnce	0h	Lock bit for SYSPLLCTL1 register: 0: Respective register is not locked 1: Respective register is locked.
2	CLKSRCCTL3	R/SOnce	0h	Lock bit for CLKSRCCTL3 register: 0: Respective register is not locked 1: Respective register is locked.
1	CLKSRCCTL2	R/SOnce	0h	Lock bit for CLKSRCCTL2 register: 0: Respective register is not locked 1: Respective register is locked.
0	CLKSRCCTL1	R/SOnce	0h	Lock bit for CLKSRCCTL1 register: 0: Respective register is not locked 1: Respective register is locked.

1.14.9.3 CLKSRCCTL1 Register (offset = 8h) [reset = 0h]

CLKSRCCTL1 is shown in [Figure 1-149](#) and described in [Table 1-147](#).

Clock Source Control register-1

Figure 1-149. CLKSRCCTL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED	WDHALTI	XTALOFF	INTOSC2OFF	RESERVED	OSCCLKSRCSEL		
R=0-0h	R/W-0h	R/W-0h	R/W-0h	R=0-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-147. CLKSRCCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-6	RESERVED	R=0	0h	Reserved
5	WDHALTI	R/W	0h	<p>Watchdog HALT Mode Ignore Bit: This bit determines if CPU1.WD is functional in the HALT mode or not.</p> <p>0 = CPU1.WD is not functional in the HALT mode. Clock to CPU1.WD is gated when system enters HALT mode. Additionally, INTOSC1 and INTOSC2 are powered-down when system enters HALT mode</p> <p>1 = CPU1.WD is functional in the HALT mode. Clock to CPU1.WD is not gated and INTOSC1/2 are not powered-down when system enters HALT mode</p> <p>Notes:</p> <p>[1] Clock to CPU2.WD clocks is always gated in the HALT mode.</p>
4	XTALOFF	R/W	0h	<p>Crystal (External) Oscillator Off Bit: This bit turns external oscillator off:</p> <p>0 = Crystal (External) Oscillator On (default on reset)</p> <p>1 = Crystal (External) Oscillator Off</p> <p>NOTE: Ensure no resources are using a clock source prior to disabling it. For example OSCCLKSRCSEL (SYSPLL), AUXOSCCLKSRCSEL (AUXPLL), CANxBCLKSEL (CAN Clock), TMR2CLKSRCSEL (CPUTIMER2) and XCLKOUTSEL(XCLKOUT).</p>
3	INTOSC2OFF	R/W	0h	<p>Internal Oscillator 2 Off Bit: This bit turns oscillator 2 off:</p> <p>0 = Internal Oscillator 2 On (default on reset)</p> <p>1 = Internal Oscillator 2 Off</p> <p>This bit could be used by the user to turn off the internal oscillator 2 if it is not used.</p> <p>NOTE: Ensure no resources are using a clock source prior to disabling it. For example OSCCLKSRCSEL (SYSPLL), AUXOSCCLKSRCSEL (AUXPLL), TMR2CLKSRCSEL (CPUTIMER2) and XCLOCKOUT (XCLKOUT).</p>
2	RESERVED	R=0	0h	Reserved

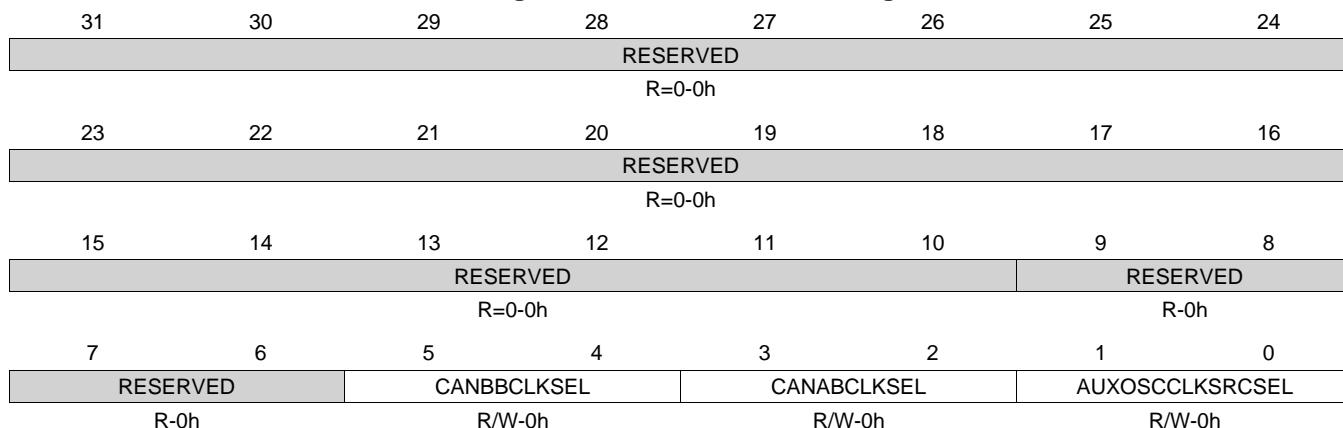
Table 1-147. CLKSRCCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	OSCCLKSRCSEL	R/W	0h	<p>Oscillator Clock Source Select Bit: This bit selects the source for OSCCLK.</p> <p>00 = INTOSC2 (default on reset) 01 = External Oscillator (XTAL) 10 = INTOSC1 11 = reserved (default to INTOSC1)</p> <p>On XRSn low and after XRSn goes high, INTOSC2 is selected by default. User can select external oscillator during their initialization process. Whenever the user changes the clock source, using these bits, the SYSPLLMMULT register will be automatically forced to zero. This prevents potential PLL overshoot. The user will then have to write to the SYSPLLMMULT register to configure the appropriate multiplier.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] Reserved selection defaults to 00 configuration [2] INTOSC1 is recommended to be used only after missing clock detection. If user wants to re-lock the PLL with INTOSC1 (the backup clock source) after missing clock is detected, he can do a MCLKCLR and lock the PLL.

1.14.9.4 CLKSRCCTL2 Register (offset = Ah) [reset = 0h]

CLKSRCCTL2 is shown in [Figure 1-150](#) and described in [Table 1-148](#).

Clock Source Control register-2

Figure 1-150. CLKSRCCTL2 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

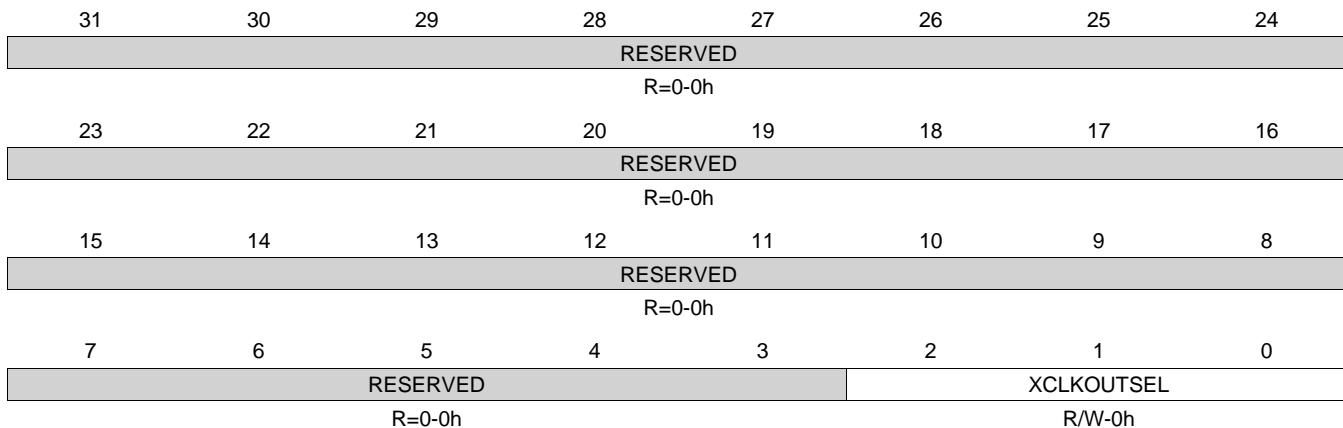
Table 1-148. CLKSRCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-10	RESERVED	R=0	0h	Reserved
9-8	RESERVED	R	0h	Reserved
7-6	RESERVED	R	0h	Reserved
5-4	CANBCLKSEL	R/W	0h	CANB Bit-Clock Source Select Bit: 00 = PERx.SYSCLK (default on reset) 01 = External Oscillator (XTAL) 10 = AUXCLKIN (from GPIO) 11 = Reserved Missing clock detect circuit doesnt have any impact on these bits.
3-2	CANABCLKSEL	R/W	0h	CANA Bit-Clock Source Select Bit: 00 = PERx.SYSCLK (default on reset) 01 = External Oscillator (XTAL) 10 = AUXCLKIN (from GPIO) 11 = Reserved Missing clock detect circuit doesnt have any impact on these bits.
1-0	AUXOSCCLKSRCSEL	R/W	0h	Oscillator Clock Source Select Bit: This bit selects the source for AUXOSCCLK: 00 = INTOSC2 (default on reset) 01 = External Oscillator (XTAL) 10 = AUXCLKIN (from GPIO) 11 = Reserved Whenever the user changes the clock source, using these bits, the AUXPLLMMULT register will be automatically forced to zero. This prevents potential PLL overshoot. The user will then have to write to the AUXPLLMMULT register to configure the appropriate multiplier. Missing clock detect circuit doesnt have any impact on these bits.

1.14.9.5 CLKSRCCTL3 Register (offset = Ch) [reset = 0h]

CLKSRCCTL3 is shown in [Figure 1-151](#) and described in [Table 1-149](#).

Clock Source Control register-3

Figure 1-151. CLKSRCCTL3 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

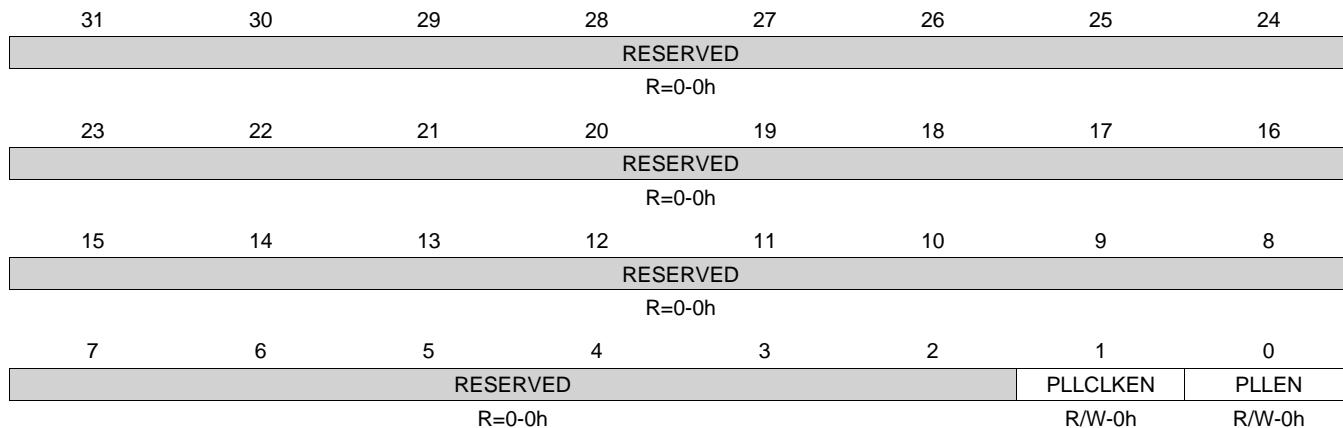
Table 1-149. CLKSRCCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-3	RESERVED	R=0	0h	Reserved
2-0	XCLKOUTSEL	R/W	0h	XCLKOUT Source Select Bit: This bit selects the source for XCLKOUT: 000 = PLLSYSCLK (default on reset) 001 = PLLRAWCLK 010 = CPU1.SYSCLK 011 = CPU2.SYSCLK 100 = AUXPLLRAWCLK 101 = INTOSC1 110 = INTOSC2 111 = Reserved

1.14.9.6 SYSPLLCTL1 Register (offset = Eh) [reset = 0h]

SYSPLLCTL1 is shown in [Figure 1-152](#) and described in [Table 1-150](#).

SYSPLL Control register-1

Figure 1-152. SYSPLLCTL1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-150. SYSPLLCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	PLLCLKEN	R/W	0h	SYSPLL bypassed or included in the PLLSYSCLK path: This bit decides if the SYSPLL is bypassed when PLLSYSCLK is generated 1 = PLLSYSCLK is fed from the SYSPLL clock output. Users need to make sure that the PLL is locked before enabling this clock to the system. 0 = SYSPLL is bypassed. Clock to system is direct feed from OSCCLK
0	PLLEN	R/W	0h	SYSPLL enabled or disabled: This bit decides if the SYSPLL is enabled or not 1 = SYSPLL is enabled 0 = SYSPLL is powered off. Clock to system is direct feed from OSCCLK

1.14.9.7 SYSPLLMULT Register (offset = 14h) [reset = 0h]

SYSPLLMULT is shown in [Figure 1-153](#) and described in [Table 1-151](#).

SYSPLL Multiplier register

NOTE: FMULT and IMULT fields must be written at the same time for correct PLL operation.

Figure 1-153. SYSPLLMULT Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							FMULT
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED		IMULT					
R=0-0h		R/W-0h					

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

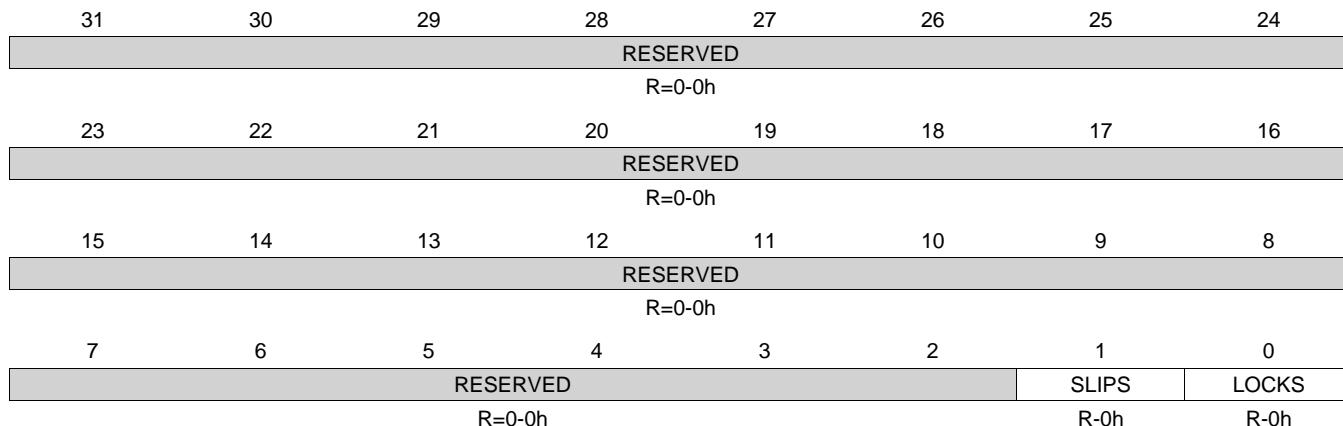
Table 1-151. SYSPLLMULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-10	RESERVED	R=0	0h	Reserved
9-8	FMULT	R/W	0h	SYSPLL Fractional Multiplier: 00 Fractional Multiplier = 0 01 Fractional Multiplier = 0.25 10 Fractional Multiplier = 0.5 11 Fractional Multiplier = 0.75
7	RESERVED	R=0	0h	Reserved
6-0	IMULT	R/W	0h	SYSPLL Integer Multiplier: For 0000000 Fout = Fref (PLLBYPASS) Integer Multiplier = 1 0000001 Integer Multiplier = 1 0000010 Integer Multiplier = 2 0000011 Integer Multiplier = 3 1111111 Integer Multiplier = 127

1.14.9.8 SYSPLLSTS Register (offset = 16h) [reset = 0h]

SYSPLLSTS is shown in [Figure 1-154](#) and described in [Table 1-152](#).

SYSPLL Status register

Figure 1-154. SYSPLLSTS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-152. SYSPLLSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	SLIPS	R	0h	<p>SYSPLL Slip Status Bit: This bit indicates whether the SYSPLL is out of lock range</p> <p>0 = SYSPLL is not out of lock</p> <p>1 = SYSPLL is out of lock</p> <p>Note:</p> <p>[1] If SYSPLL out of lock condition is detected then interrupts are fired to CPU1 and CPU2 through their respective ePIE modules. Software can decide to relock the PLL or switch to PLL bypass mode in the interrupt handler</p>
0	LOCKS	R	0h	<p>SYSPLL Lock Status Bit: This bit indicates whether the SYSPLL is locked or not</p> <p>0 = SYSPLL is not yet locked</p> <p>1 = SYSPLL is locked</p>

1.14.9.9 AUXPLLCTL1 Register (offset = 18h) [reset = 0h]

AUXPLLCTL1 is shown in [Figure 1-155](#) and described in [Table 1-153](#).

AUXPLL Control register-1

Figure 1-155. AUXPLLCTL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED						PLLCLKEN	PLLEN
R=0-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-153. AUXPLLCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	PLLCLKEN	R/W	0h	AUXPLL bypassed or included in the AUXPLLCLK path: This bit decides if the AUXPLL is bypassed when AUXPLLCLK is generated 1 = AUXPLLCLK is fed from the AUXPLL clock output. Users need to make sure that the PLL is locked before enabling this clock to the AUXPLLCLK connected modules. 0 = AUXPLL is bypassed. Clock to modules connected to AUXPLLCLK is direct feed from AUXOSCCLK
0	PLLEN	R/W	0h	AUXPLL enabled or disabled: This bit decides if the AUXPLL is enabled or not 1 = AUXPLL is enabled 0 = AUXPLL is powered off. Clock to system is direct feed from AUXOSCCLK

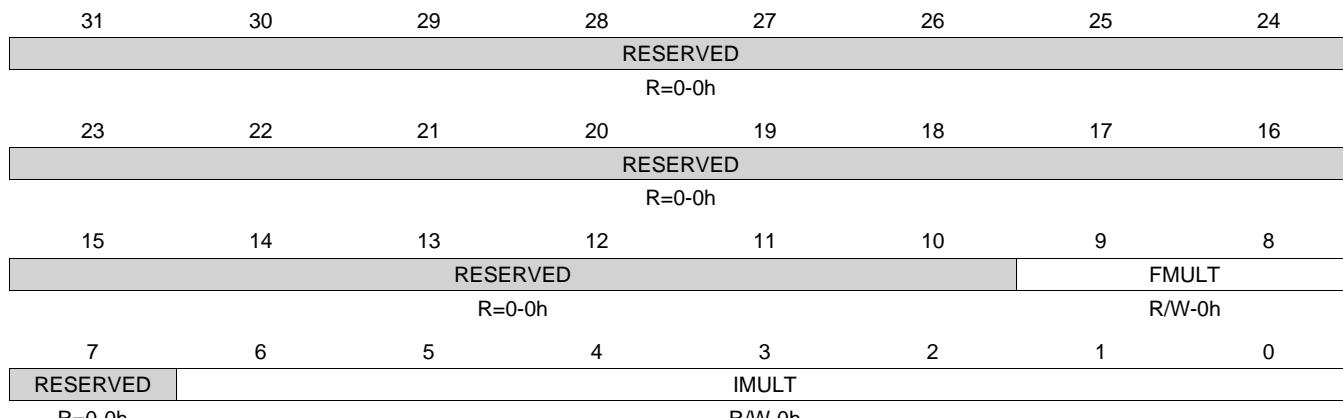
1.14.9.10 AUXPLLMMULT Register (offset = 1Eh) [reset = 0h]

AUXPLLMMULT is shown in [Figure 1-156](#) and described in [Table 1-154](#).

AUXPLL Multiplier register

NOTE: FMULT and IMULT fields must be written at the same time for correct PLL operation.

Figure 1-156. AUXPLLMMULT Register



LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

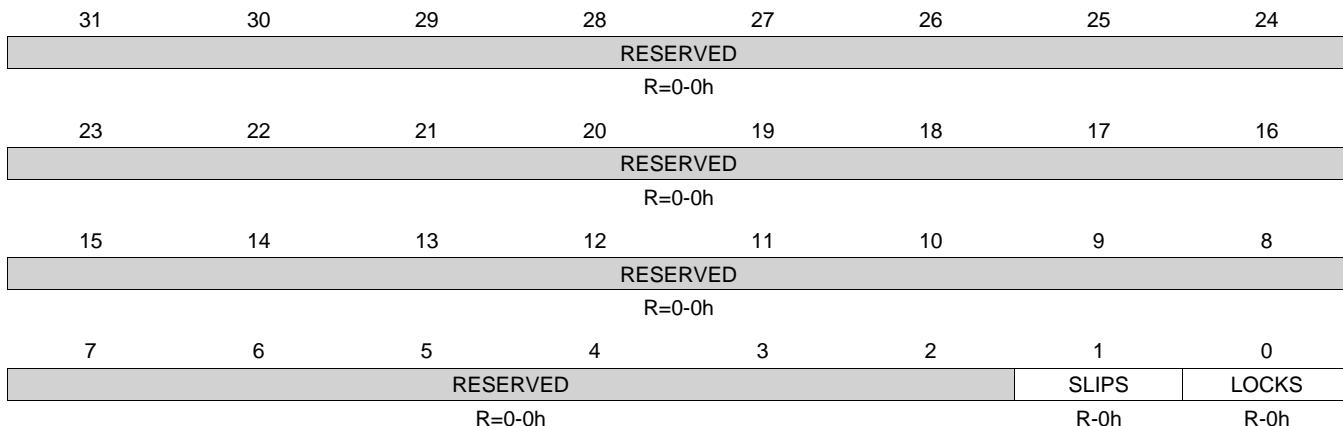
Table 1-154. AUXPLLMMULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-10	RESERVED	R=0	0h	Reserved
9-8	FMULT	R/W	0h	AUXPLL Fractional Multiplier : 00 Fractional Multiplier = 0 01 Fractional Multiplier = 0.25 10 Fractional Multiplier = 0.5 11 Fractional Multiplier = 0.75
7	RESERVED	R=0	0h	Reserved
6-0	IMULT	R/W	0h	AUXPLL Integer Multiplier: For 0000000 Fout = Fref (PLLBYPASS) Integer Multiplier = 1 0000001 Integer Multiplier = 1 0000010 Integer Multiplier = 2 0000011 Integer Multiplier = 3 1111111 Integer Multipler = 127

1.14.9.11 AUXPLLSTS Register (offset = 20h) [reset = 0h]

AUXPLLSTS is shown in [Figure 1-157](#) and described in [Table 1-155](#).

AUXPLL Status register

Figure 1-157. AUXPLLSTS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-155. AUXPLLSTS Register Field Descriptions

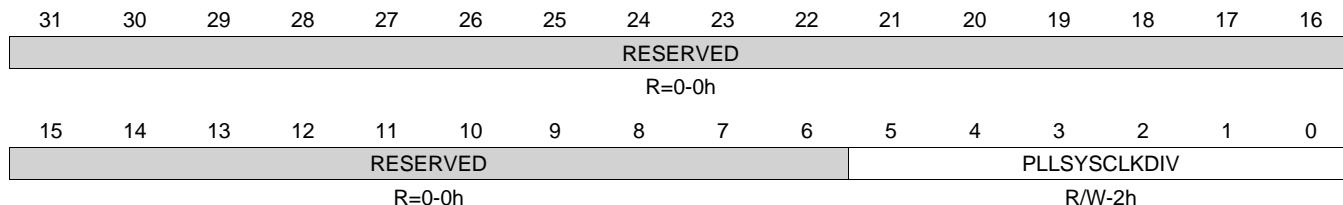
Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	SLIPS	R	0h	AUXPLL Slip Status Bit: This bit indicates whether the AUXPLL is out of lock range 0 = AUXPLL is not out of lock 1 = AUXPLL is out of lock Note: [1] If AUXPLL out of lock condition is detected then interrupts are fired to CPU1 and CPU2 through their respective ePIE modules. Software can decide to relock the PLL or switch to PLL bypass mode in the interrupt handler
0	LOCKS	R	0h	AUXPLL Lock Status Bit: This bit indicates whether the AUXPLL is locked or not 0 = AUXPLL is not yet locked 1 = AUXPLL is locked

1.14.9.12 SYSCLKDIVSEL Register (offset = 22h) [reset = 2h]

SYSCLKDIVSEL is shown in [Figure 1-158](#) and described in [Table 1-156](#).

System Clock Divider Select register

Figure 1-158. SYSCLKDIVSEL Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

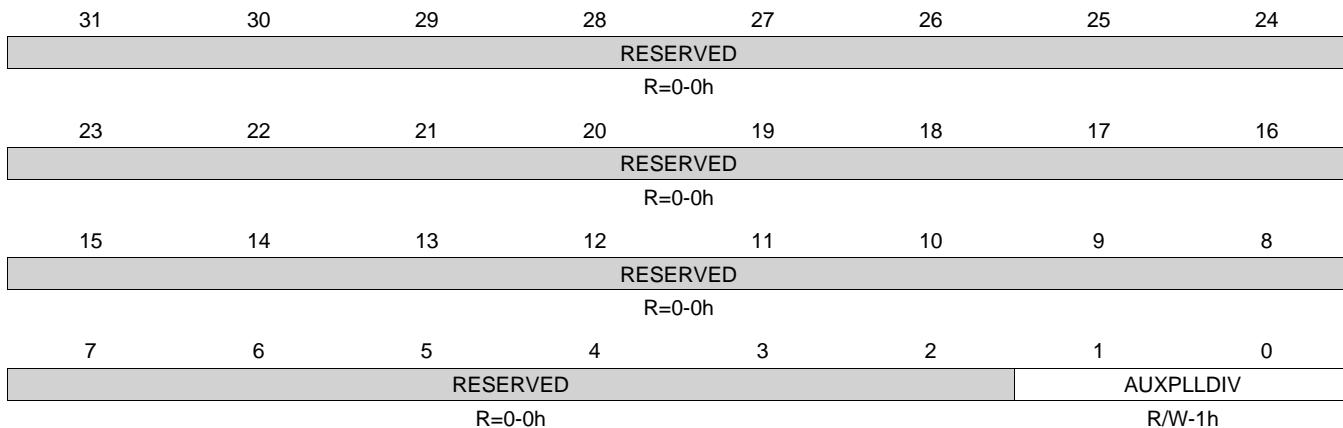
Table 1-156. SYSCLKDIVSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-6	RESERVED	R=0	0h	Reserved
5-0	PLLSYSCLKDIV	R/W	2h	PLLSYSCLK Divide Select: This bit selects the divider setting for the PLLSYSCLK. 000000 = /1 000001 = /2 000010 = /4 (default on reset) 000011 = /6 000100 = /8 111111 = /126 Design Note:, [1] The selection must not generate any clock glitches.

1.14.9.13 AUXCLKDIVSEL Register (offset = 24h) [reset = 1h]

AUXCLKDIVSEL is shown in [Figure 1-159](#) and described in [Table 1-157](#).

Auxillary Clock Divider Select register

Figure 1-159. AUXCLKDIVSEL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

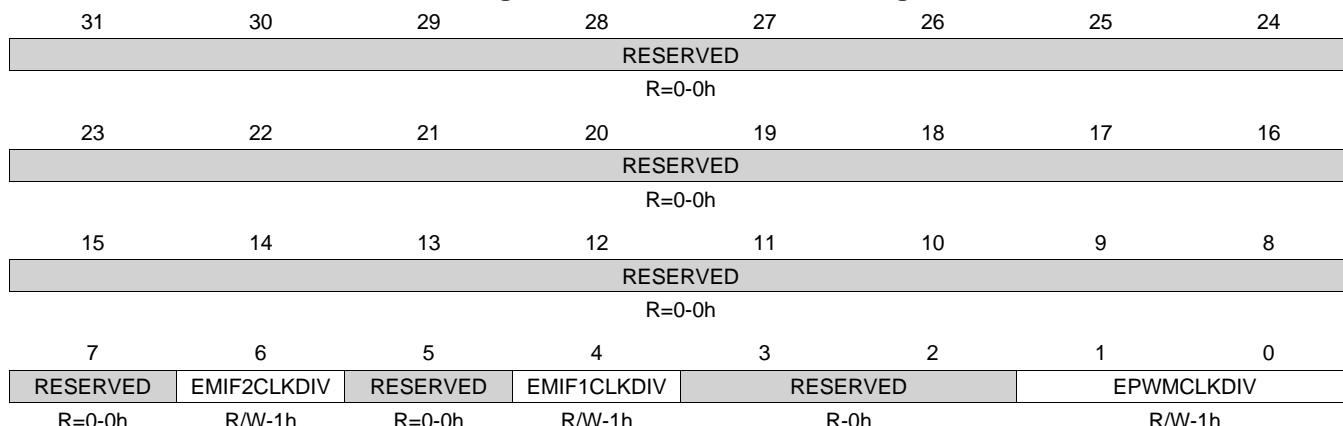
Table 1-157. AUXCLKDIVSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1-0	AUXPLL DIV	R/W	1h	AUXPLLCLK Divide Select: This bit selects the divider setting for the AUXPLLCK. 00 = /1 01 = /2 (default on reset) 10 = /4 11 = /8

1.14.9.14 PERCLKDIVSEL Register (offset = 26h) [reset = 51h]

PERCLKDIVSEL is shown in [Figure 1-160](#) and described in [Table 1-158](#).

Peripheral Clock Divider Selet register

Figure 1-160. PERCLKDIVSEL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

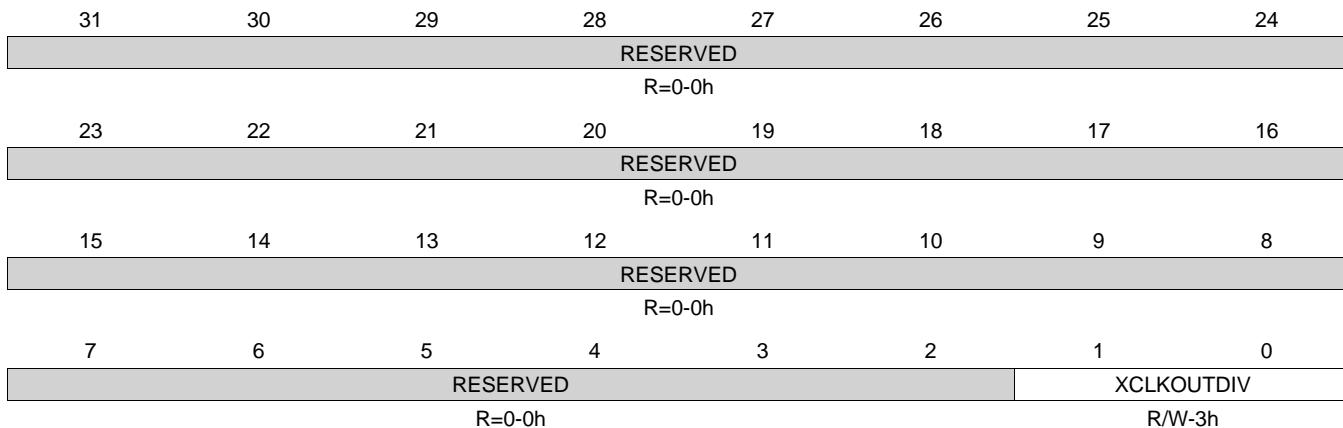
Table 1-158. PERCLKDIVSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-7	RESERVED	R=0	0h	Reserved
6	EMIF2CLKDIV	R/W	1h	EMIF2 Clock Divide Select: This bit selects whether the EMIF2 module run with a /1 or /2 clock. 0: /1 of CPU1.SYSCLK is selected 1: /2 of CPU1.SYSCLK is selected
5	RESERVED	R=0	0h	Reserved
4	EMIF1CLKDIV	R/W	1h	EMIF1 Clock Divide Select: This bit selects whether the EMIF1 module run with a /1 or /2 clock. For single core device 0: /1 of CPU1.SYSCLK is selected 1: /2 of CPU1.SYSCLK is selected For Dual core device 0: /1 of PLLSYSCLK is selected 1: /2 of PLLSYSCLK is selected
3-2	RESERVED	R	0h	Reserved
1-0	EPWMCLKDIV	R/W	1h	EPWM Clock Divide Select: This bit selects whether the EPWM modules run with a /1 or /2 clock. This divider sits in front of the PLLSYSCLK x0 = /1 of PLLSYSCLK x1 = /2 of PLLSYSCLK (default on reset) Note: Refer to the EPWM User Guide for maximum EPWM Frequency

1.14.9.15 XCLKOUTDIVSEL Register (offset = 28h) [reset = 3h]

XCLKOUTDIVSEL is shown in [Figure 1-161](#) and described in [Table 1-159](#).

XCLKOUT Divider Select register

Figure 1-161. XCLKOUTDIVSEL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-159. XCLKOUTDIVSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1-0	XCLKOUTDIV	R/W	3h	XCLKOUT Divide Select: This bit selects the divider setting for the XCLKOUT. 00 = /1 01 = /2 10 = /4 11 = /8 (default on reset)

1.14.9.16 LOSPCP Register (offset = 2Ch) [reset = 2h]

LOSPCP is shown in [Figure 1-162](#) and described in [Table 1-160](#).

Low Speed Clock Source Prescalar

Figure 1-162. LOSPCP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R=0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												LSPCLKDIV			
R=0-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

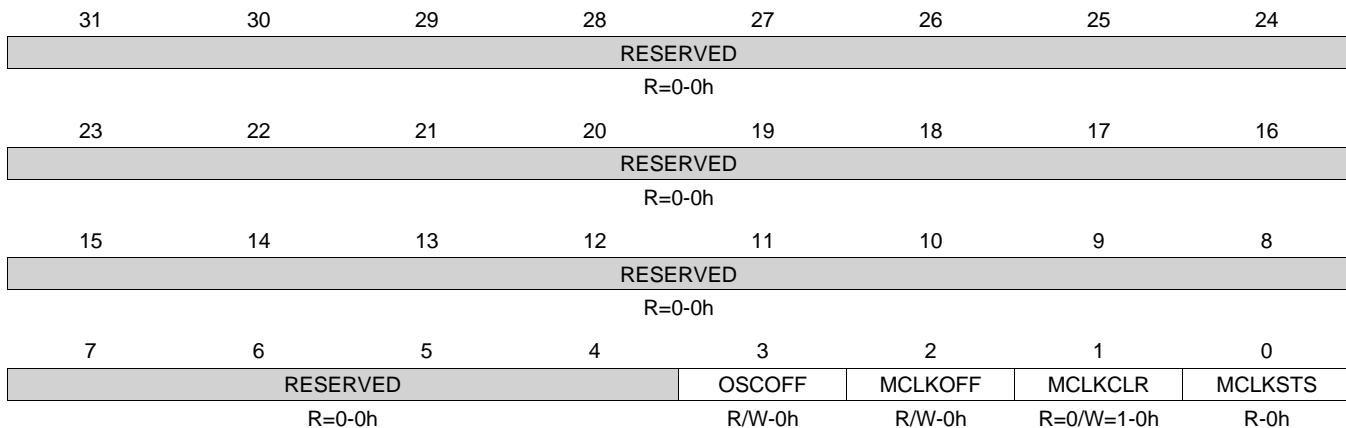
Table 1-160. LOSPCP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-3	RESERVED	R=0	0h	Reserved
2-0	LSPCLKDIV	R/W	2h	<p>These bits configure the low-speed peripheral clock (LSPCLK) rate relative to SYSCLK of CPU1 and CPU2.</p> <p>000,LSPCLK = / 1 001,LSPCLK = / 2 010,LSPCLK = / 4 (default on reset) 011,LSPCLK = / 6 100,LSPCLK = / 8 101,LSPCLK = / 10 110,LSPCLK = / 12 111,LSPCLK = / 14</p> <p>Note:</p> <p>[1] This clock is used as strobe for the SCI and SPI modules.</p>

1.14.9.17 MCDCR Register (offset = 2Eh) [reset = 0h]

MCDCR is shown in [Figure 1-163](#) and described in [Table 1-161](#).

Missing Clock Detect Control Register

Figure 1-163. MCDCR Register

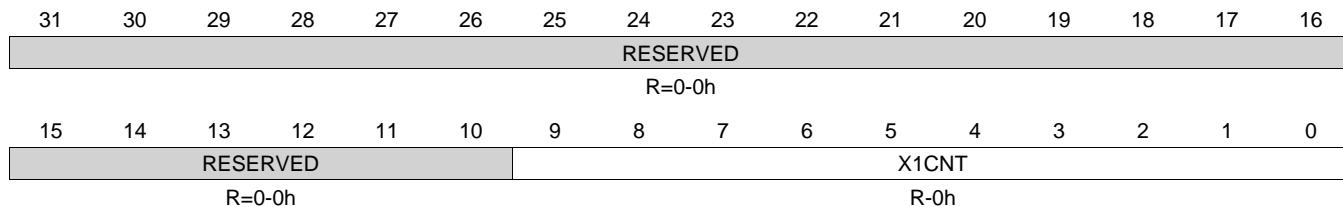
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-161. MCDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	OSCOFF	R/W	0h	Oscillator Clock Off Bit: 0 = OSCCLK Connected to OSCCLK Counter in MCD module 1 = OSCCLK Disconnected to OSCCLK Counter in MCD module
2	MCLKOFF	R/W	0h	Missing Clock Detect Off Bit: 0 = Missing Clock Detect Circuit Enabled 1 = Missing Clock Detect Circuit Disabled
1	MCLKCLR	R=0/W=1	0h	Missing Clock Clear Bit: Write 1" to this bit to clear MCLKSTS bit and reset the missing clock detect circuit."
0	MCLKSTS	R	0h	Missing Clock Status Bit: 0 = OSCCLK Is OK 1 = OSCCLK Detected Missing, CLOCKFAILn Generated

1.14.9.18 X1CNT Register (offset = 30h) [reset = 0h]X1CNT is shown in [Figure 1-164](#) and described in [Table 1-162](#).

10-bit Counter on X1 Clock

Figure 1-164. X1CNT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-162. X1CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-10	RESERVED	R=0	0h	Reserved
9-0	X1CNT	R	0h	X1 Counter: - This counter increments on every X1 CLOCKs positive-edge. - Once it reaches the values of 0x3ff, it freezes - Before switching from INTOSC2 to X1, application must check this counter and make sure that it has saturated. This will guarantee that the Crystal connected to X1/X2 is powered Up.

1.14.10 CPU_SYS_REGS Registers

Table 1-163 lists the memory-mapped registers for the CPU_SYS_REGS. All register offset addresses not listed in Table 1-163 should be considered as reserved locations and the register contents should not be modified.

Table 1-163. CPU_SYS_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	CPUSYSLOCK1	Lock bit for CPUSYS registers	Section 1.14.10.1	EALLOW
6h	HIBBOOTMODE	HIB Boot Mode Register	Section 1.14.10.2	EALLOW
8h	IORESTOREADDR	IORestore() routine Address Register	Section 1.14.10.3	EALLOW
Ah	PIEVERRADDR	PIE Vector Fetch Error Address register	Section 1.14.10.4	EALLOW
22h	PCLKCR0	Peripheral Clock Gating Registers	Section 1.14.10.5	EALLOW
24h	PCLKCR1	Peripheral Clock Gating Registers	Section 1.14.10.6	EALLOW
26h	PCLKCR2	Peripheral Clock Gating Registers	Section 1.14.10.7	EALLOW
28h	PCLKCR3	Peripheral Clock Gating Registers	Section 1.14.10.8	EALLOW
2Ah	PCLKCR4	Peripheral Clock Gating Registers	Section 1.14.10.9	EALLOW
2Ch	PCLKCR5	Peripheral Clock Gating Registers	Section 1.14.10.10	EALLOW
2Eh	PCLKCR6	Peripheral Clock Gating Registers	Section 1.14.10.11	EALLOW
30h	PCLKCR7	Peripheral Clock Gating Registers	Section 1.14.10.12	EALLOW
32h	PCLKCR8	Peripheral Clock Gating Registers	Section 1.14.10.13	EALLOW
34h	PCLKCR9	Peripheral Clock Gating Registers	Section 1.14.10.14	EALLOW
36h	PCLKCR10	Peripheral Clock Gating Registers	Section 1.14.10.15	EALLOW
38h	PCLKCR11	Peripheral Clock Gating Registers	Section 1.14.10.16	EALLOW
3Ah	PCLKCR12	Peripheral Clock Gating Registers	Section 1.14.10.17	EALLOW
3Ch	PCLKCR13	Peripheral Clock Gating Registers	Section 1.14.10.18	EALLOW
3Eh	PCLKCR14	Peripheral Clock Gating Registers	Section 1.14.10.19	EALLOW
42h	PCLKCR16	Peripheral Clock Gating Registers	Section 1.14.10.20	EALLOW
74h	SECMSEL	Secondary Master Select register for common peripherals: Selects between CLA & DMA	Section 1.14.10.21	EALLOW
76h	LPMCR	LPM Control Register	Section 1.14.10.22	EALLOW
78h	GPIOLPMSEL0	GPIO LPM Wakeup select registers	Section 1.14.10.23	EALLOW
7Ah	GPIOLPMSEL1	GPIO LPM Wakeup select registers	Section 1.14.10.24	EALLOW
7Ch	TMR2CLKCTL	Timer2 Clock Measurement functionality control register	Section 1.14.10.25	EALLOW

Table 1-163. CPU_SYS_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
80h	RESC	Reset Cause register	Section 1.14.10.26	

1.14.10.1 CPUSYSLOCK1 Register (offset = 0h) [reset = 0h]

CPUSYSLOCK1 is shown in [Figure 1-165](#) and described in [Table 1-164](#).

Lock bit for CPUSYS registers

Notes:

[1] Any bit in this register, once set can only be cleared through a CPU1.SYRSRs. Write of 0 to any bit of this register has no effect

[2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed

Figure 1-165. CPUSYSLOCK1 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
GPIOLPMSEL1	GPIOLPMSEL0	LPMCR	SECMSEL	PCLKCR16	PCLKCR15	PCLKCR14	PCLKCR13
R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h
15	14	13	12	11	10	9	8
PCLKCR12	PCLKCR11	PCLKCR10	PCLKCR9	PCLKCR8	PCLKCR7	PCLKCR6	PCLKCR5
R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h
7	6	5	4	3	2	1	0
PCLKCR4	PCLKCR3	PCLKCR2	PCLKCR1	PCLKCR0	PIEVERRADD R	IORESTOREA DDR	HIBBOOTMOD E
R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h	R/SOnce-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-164. CPUSYSLOCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R=0	0h	Reserved
23	GPIOLPMSEL1	R/SOnce	0h	Lock bit for GPIOLPMSEL1 Register: 0: Respective register is not locked 1: Respective register is locked.
22	GPIOLPMSEL0	R/SOnce	0h	Lock bit for GPIOLPMSEL0 Register: 0: Respective register is not locked 1: Respective register is locked.
21	LPMCR	R/SOnce	0h	Lock bit for LPMCR Register: 0: Respective register is not locked 1: Respective register is locked.
20	SECMSEL	R/SOnce	0h	Lock bit for SECMSEL Register: 0: Respective register is not locked 1: Respective register is locked.
19	PCLKCR16	R/SOnce	0h	Lock bit for PCLKCR16 Register: 0: Respective register is not locked 1: Respective register is locked.
18	PCLKCR15	R/SOnce	0h	Lock bit for PCLKCR15 Register: 0: Respective register is not locked 1: Respective register is locked.
17	PCLKCR14	R/SOnce	0h	Lock bit for PCLKCR14 Register: 0: Respective register is not locked 1: Respective register is locked.

Table 1-164. CPUSYSLOCK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PCLKCR13	R/SOnce	0h	Lock bit for PCLKCR13 Register: 0: Respective register is not locked 1: Respective register is locked.
15	PCLKCR12	R/SOnce	0h	Lock bit for PCLKCR12 Register: 0: Respective register is not locked 1: Respective register is locked.
14	PCLKCR11	R/SOnce	0h	Lock bit for PCLKCR11 Register: 0: Respective register is not locked 1: Respective register is locked.
13	PCLKCR10	R/SOnce	0h	Lock bit for PCLKCR10 Register: 0: Respective register is not locked 1: Respective register is locked.
12	PCLKCR9	R/SOnce	0h	Lock bit for PCLKCR9 Register: 0: Respective register is not locked 1: Respective register is locked.
11	PCLKCR8	R/SOnce	0h	Lock bit for PCLKCR8 Register: 0: Respective register is not locked 1: Respective register is locked.
10	PCLKCR7	R/SOnce	0h	Lock bit for PCLKCR7 Register: 0: Respective register is not locked 1: Respective register is locked.
9	PCLKCR6	R/SOnce	0h	Lock bit for PCLKCR6 Register: 0: Respective register is not locked 1: Respective register is locked.
8	PCLKCR5	R/SOnce	0h	Lock bit for PCLKCR5 Register: 0: Respective register is not locked 1: Respective register is locked.
7	PCLKCR4	R/SOnce	0h	Lock bit for PCLKCR4 Register: 0: Respective register is not locked 1: Respective register is locked.
6	PCLKCR3	R/SOnce	0h	Lock bit for PCLKCR3 Register: 0: Respective register is not locked 1: Respective register is locked.
5	PCLKCR2	R/SOnce	0h	Lock bit for PCLKCR2 Register: 0: Respective register is not locked 1: Respective register is locked.
4	PCLKCR1	R/SOnce	0h	Lock bit for PCLKCR1 Register: 0: Respective register is not locked 1: Respective register is locked.
3	PCLKCR0	R/SOnce	0h	Lock bit for PCLKCR0 Register: 0: Respective register is not locked 1: Respective register is locked.
2	PIEVERRADDR	R/SOnce	0h	Lock bit for PIEVERRADDR Register: 0: Respective register is not locked 1: Respective register is locked.

Table 1-164. CPUSYSLOCK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	IORESTOREADDR	R/SOnce	0h	Lock bit for IORESTOREADDR Register: 0: Respective register is not locked 1: Respective register is locked.
0	HIBBOOTMODE	R/SOnce	0h	Lock bit for HIBBOOTMODE register: 0: Respective register is not locked 1: Respective register is locked.

1.14.10.2 HIBBOOTMODE Register (offset = 6h) [reset = Fh]

HIBBOOTMODE is shown in [Figure 1-166](#) and described in [Table 1-165](#).

HIB Boot Mode Register

Figure 1-166. HIBBOOTMODE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMODE																															
R/W-Fh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-165. HIBBOOTMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BMODE	R/W	Fh	This register defined the boot mode on a HIB Wakeup. Its the responsibility of user to initialize the appropriate boot mode before going into HIB mode. Refer to Device Boot ROM Spec for more details on this register

1.14.10.3 IORESTOREADDR Register (offset = 8h) [reset = 3FFFFFFh]

IORESTOREADDR is shown in [Figure 1-167](#) and described in [Table 1-166](#).

IORestore() routine Address Register

Figure 1-167. IORESTOREADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR															
R=0-0h																R/W-3FFFFFFh															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-166. IORESTOREADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R=0	0h	Reserved
21-0	ADDR	R/W	3FFFFFFh	This register defines the address of the restoreIO() routine on a HIB wakeup. Its the responsibility of user to initialize this register with the restoreIO() routine address before going into HIB mode. Refer to Device Boot ROM Spec for more details on this register.

1.14.10.4 PIEVERRADDR Register (offset = Ah) [reset = 3FFFFFFh]PIEVERRADDR is shown in [Figure 1-168](#) and described in [Table 1-167](#).

PIE Vector Fetch Error Address register

Figure 1-168. PIEVERRADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR															

R=0-0h

R/W-3FFFFFFh

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-167. PIEVERRADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R=0	0h	Reserved
21-0	ADDR	R/W	3FFFFFFh	This register defines the address of the PIE Vector Fetch Error handler routine. Its the responsibility of user to initialize this register. If this register is not initialized, a default error handler at address 0x3fffbe will get executed. Refer to Device Boot ROM Spec for more details on this register.

1.14.10.5 PCLKCR0 Register (offset = 22h) [reset = 38h]

PCLKCR0 is shown in [Figure 1-169](#) and described in [Table 1-168](#).

Peripheral Clock Gating Registers

Figure 1-169. PCLKCR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED				GTBCLKSYNC	TBCLKSYNC	RESERVED	HRPWM
R=0-0h				R/W-0h	R/W-0h	R=0-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED	CPUTIMER2	CPUTIMER1	CPUTIMER0	DMA	RESERVED	CLA1	
R=0-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-168. PCLKCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R=0	0h	Reserved
19	GTBCLKSYNC	R/W	0h	EPWM Time Base Clock Global sync: When set by CPU1, PWM time bases of all modules start counting. The effect of this bit is seen on all the EPMW modules irrespective of their partitioning based on CPUSEL Notes: 1. This bit on the CPU2.PCLKCR0 register has no effect. 2. Writing '1' to this bit overrides the effect of write '1' to the TBCLKSYNC bit at the same time
18	TBCLKSYNC	R/W	0h	EPWM Time Base Clock sync: When set PWM time bases of all the PWM modules belonging to the same CPU-Subsystem (as partitioned using their CPUSEL bits) start counting Notes: 1. This bit from CPU1.PCLKCR0 or CPU2.PCLKCR0 is selected and fed to the individual EPWM modules based on their respective CPUSEL bit.
17	RESERVED	R=0	0h	Reserved
16	HRPWM	R/W	0h	HRPWM Clock Enable Bit: When set, this enables the clock to the HRPWM module 1: HRPWM clock is enabled 0: HRPWM clock is disabled Note: [1] This bit is present only in CPU1.PCLKCR0. This bit is not used (R/W) in CPU2.PCLKCR0
15-6	RESERVED	R=0	0h	Reserved
5	CPUTIMER2	R/W	1h	CPUTIMER2 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
4	CPUTIMER1	R/W	1h	CPUTIMER1 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

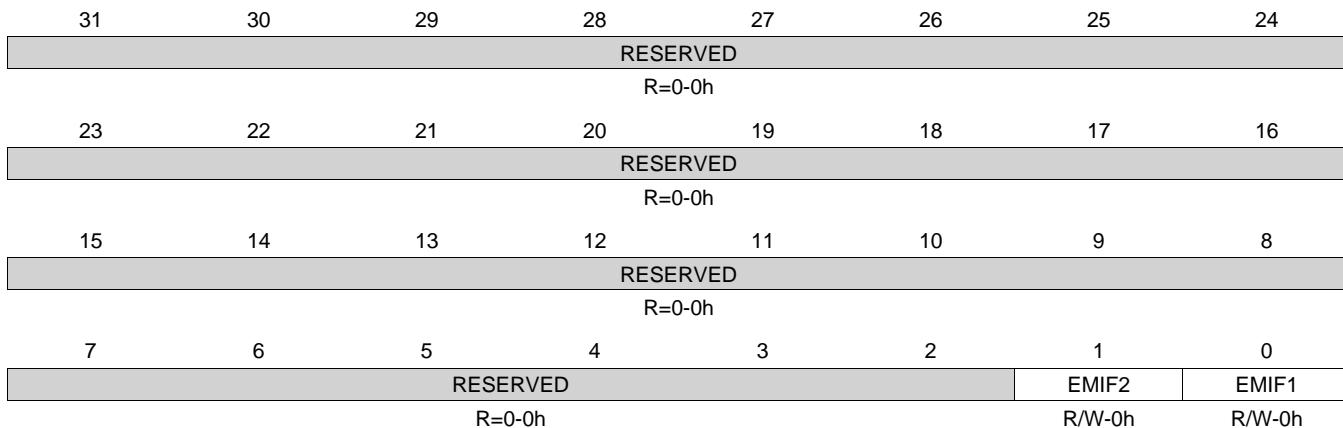
Table 1-168. PCLKCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CPUTIMER0	R/W	1h	CPUTIMER0 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
2	DMA	R/W	0h	DMA Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
1	RESERVED	R	0h	Reserved
0	CLA1	R/W	0h	CLA1 Clock Enable Bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.6 PCLKCR1 Register (offset = 24h) [reset = 0h]

PCLKCR1 is shown in [Figure 1-170](#) and described in [Table 1-169](#).

Peripheral Clock Gating Registers

Figure 1-170. PCLKCR1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-169. PCLKCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	EMIF2	R/W	0h	<p>EMIF2 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on</p> <p>Notes:</p> <p>[1] These bits are not used (R/W) in CPU2.PCLKCR1 register. EMIF1 & EMIF2 clock enabled are controlled only from CPU1.PCLKCR1 register.</p>
0	EMIF1	R/W	0h	<p>EMIF1 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on</p> <p>Notes:</p> <p>[1] These bits are not used (R/W) in CPU2.PCLKCR1 register. EMIF1 & EMIF2 clock enabled are controlled only from CPU1.PCLKCR1 register.</p>

1.14.10.7 PCLKCR2 Register (offset = 26h) [reset = 0h]

PCLKCR2 is shown in [Figure 1-171](#) and described in [Table 1-170](#).

Peripheral Clock Gating Registers

Figure 1-171. PCLKCR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	EPWM12	EPWM11	EPWM10	EPWM9
R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EPWM8	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-170. PCLKCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	EPWM12	R/W	0h	EPWM12 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
10	EPWM11	R/W	0h	EPWM11 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
9	EPWM10	R/W	0h	EPWM10 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
8	EPWM9	R/W	0h	EPWM9 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
7	EPWM8	R/W	0h	EPWM8 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
6	EPWM7	R/W	0h	EPWM7 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
5	EPWM6	R/W	0h	EPWM6 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

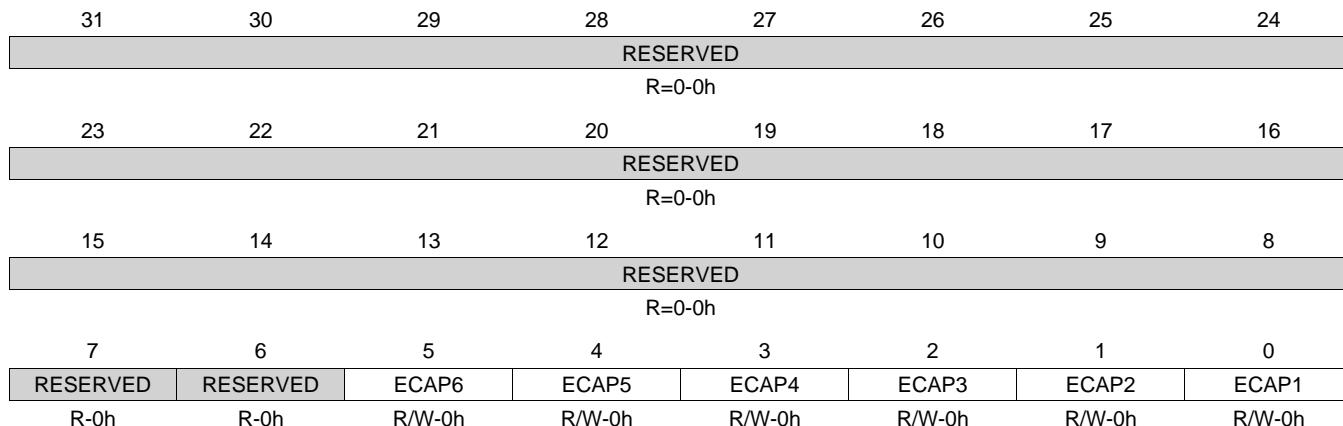
Table 1-170. PCLKCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EPWM5	R/W	0h	EPWM5 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
3	EPWM4	R/W	0h	EPWM4 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
2	EPWM3	R/W	0h	EPWM3 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
1	EPWM2	R/W	0h	EPWM2 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	EPWM1	R/W	0h	EPWM1 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.8 PCLKCR3 Register (offset = 28h) [reset = 0h]

PCLKCR3 is shown in [Figure 1-172](#) and described in [Table 1-171](#).

Peripheral Clock Gating Registers

Figure 1-172. PCLKCR3 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

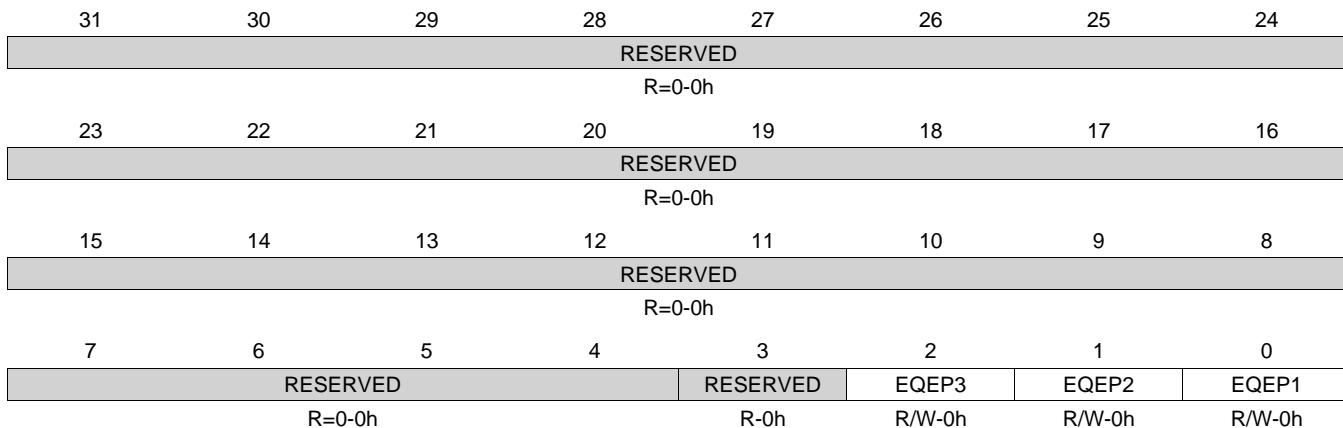
Table 1-171. PCLKCR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	ECAP6	R/W	0h	ECAP6 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
4	ECAP5	R/W	0h	ECAP5 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
3	ECAP4	R/W	0h	ECAP4 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
2	ECAP3	R/W	0h	ECAP3 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
1	ECAP2	R/W	0h	ECAP2 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	ECAP1	R/W	0h	ECAP1 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.9 PCLKCR4 Register (offset = 2Ah) [reset = 0h]

PCLKCR4 is shown in [Figure 1-173](#) and described in [Table 1-172](#).

Peripheral Clock Gating Registers

Figure 1-173. PCLKCR4 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

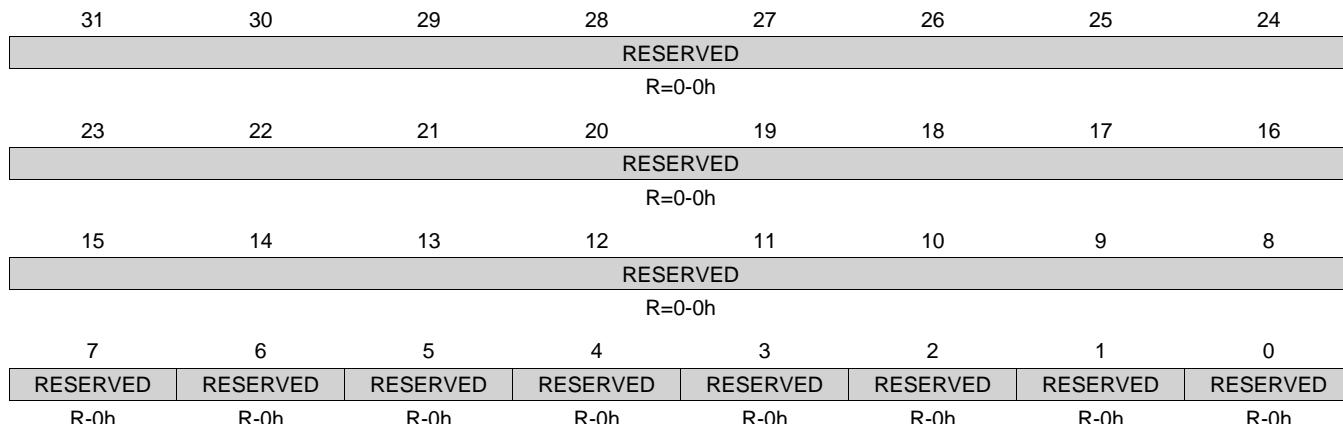
Table 1-172. PCLKCR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	EQEP3	R/W	0h	EQEP3 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
1	EQEP2	R/W	0h	EQEP2 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	EQEP1	R/W	0h	EQEP1 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.10 PCLKCR5 Register (offset = 2Ch) [reset = 0h]

PCLKCR5 is shown in [Figure 1-174](#) and described in [Table 1-173](#).

Peripheral Clock Gating Registers

Figure 1-174. PCLKCR5 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-173. PCLKCR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.10.11 PCLKCR6 Register (offset = 2Eh) [reset = 0h]

PCLKCR6 is shown in [Figure 1-175](#) and described in [Table 1-174](#).

Peripheral Clock Gating Registers

Figure 1-175. PCLKCR6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R=0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESE RVED	RESE RVED	RESE RVED	RESE RVED	RESE RVED	RESE RVED	SD2	SD1
R=0-0h								R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W- 0h	R/W- 0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

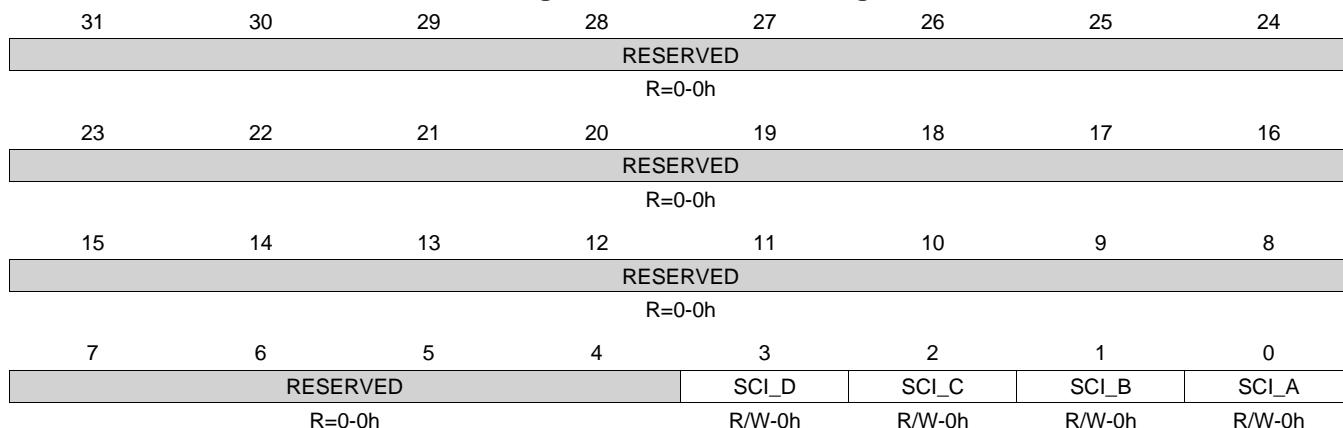
Table 1-174. PCLKCR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	SD2	R/W	0h	SD2 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	SD1	R/W	0h	SD1 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.12 PCLKCR7 Register (offset = 30h) [reset = 0h]

PCLKCR7 is shown in [Figure 1-176](#) and described in [Table 1-175](#).

Peripheral Clock Gating Registers

Figure 1-176. PCLKCR7 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

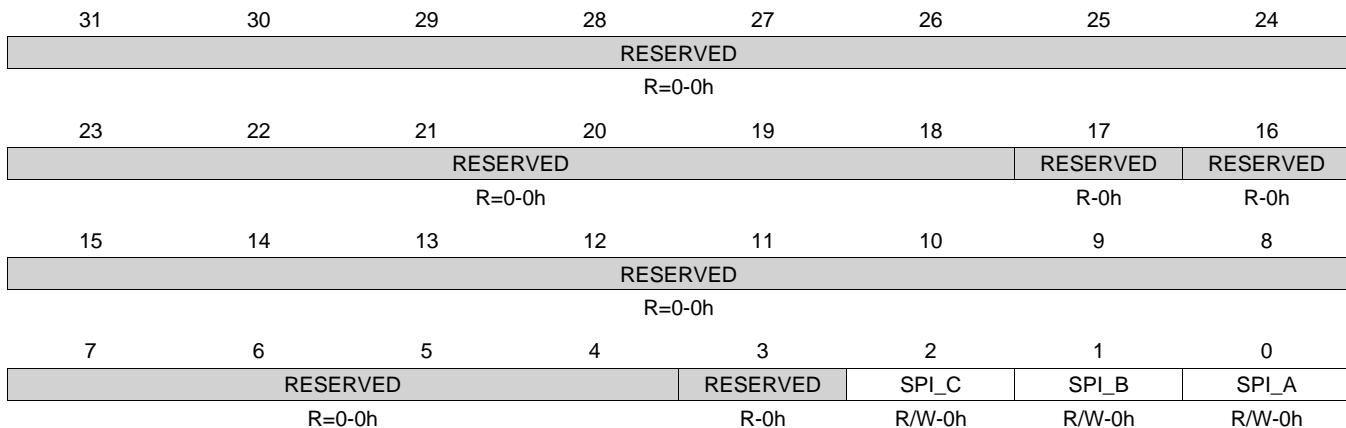
Table 1-175. PCLKCR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	SCI_D	R/W	0h	SCI_D Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
2	SCI_C	R/W	0h	SCI_C Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
1	SCI_B	R/W	0h	SCI_B Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	SCI_A	R/W	0h	SCI_A Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.13 PCLKCR8 Register (offset = 32h) [reset = 0h]

PCLKCR8 is shown in [Figure 1-177](#) and described in [Table 1-176](#).

Peripheral Clock Gating Registers

Figure 1-177. PCLKCR8 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

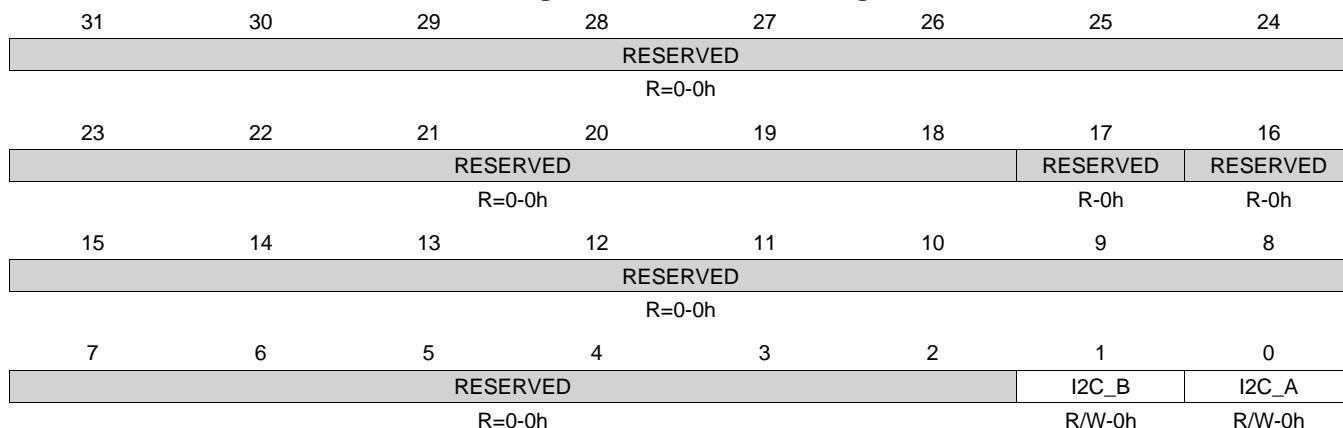
Table 1-176. PCLKCR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	SPI_C	R/W	0h	SPI_C Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
1	SPI_B	R/W	0h	SPI_B Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	SPI_A	R/W	0h	SPI_A Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.14 PCLKCR9 Register (offset = 34h) [reset = 0h]

PCLKCR9 is shown in [Figure 1-178](#) and described in [Table 1-177](#).

Peripheral Clock Gating Registers

Figure 1-178. PCLKCR9 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

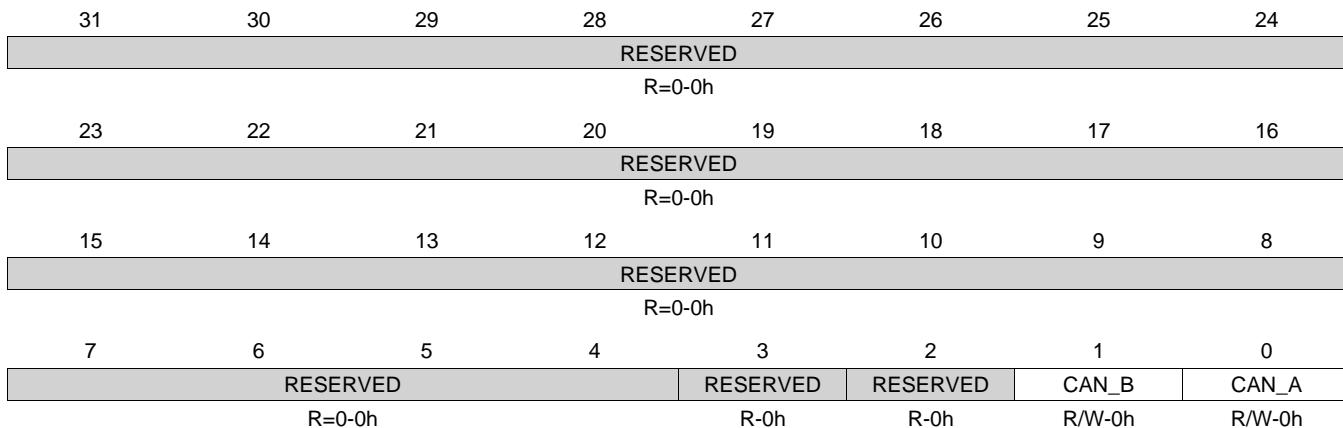
Table 1-177. PCLKCR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	I2C_B	R/W	0h	I2C_B Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	I2C_A	R/W	0h	I2C_A Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.15 PCLKCR10 Register (offset = 36h) [reset = 0h]

PCLKCR10 is shown in [Figure 1-179](#) and described in [Table 1-178](#).

Peripheral Clock Gating Registers

Figure 1-179. PCLKCR10 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

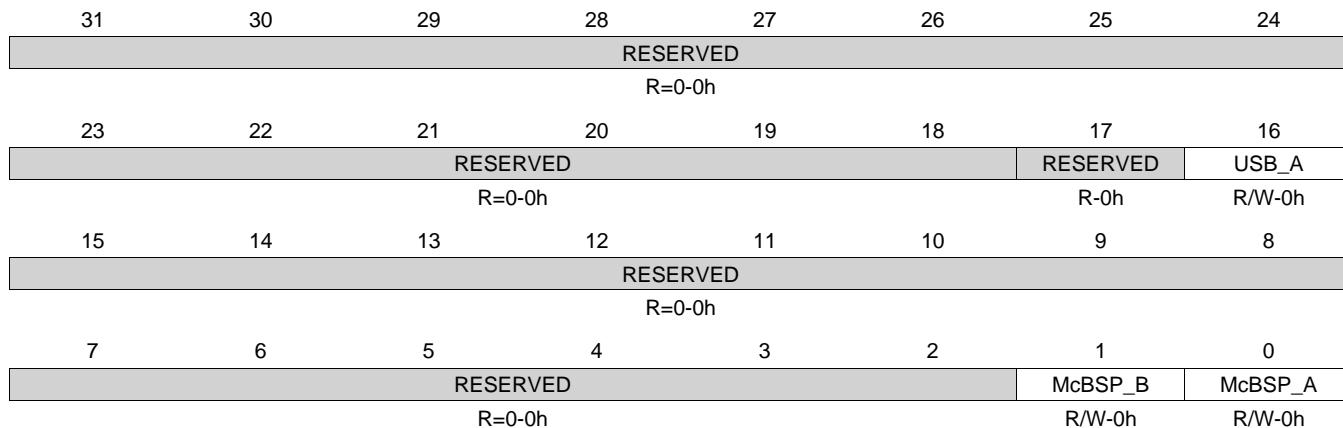
Table 1-178. PCLKCR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	CAN_B	R/W	0h	CAN_B Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	CAN_A	R/W	0h	CAN_A Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.16 PCLKCR11 Register (offset = 38h) [reset = 0h]

PCLKCR11 is shown in [Figure 1-180](#) and described in [Table 1-179](#).

Peripheral Clock Gating Registers

Figure 1-180. PCLKCR11 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

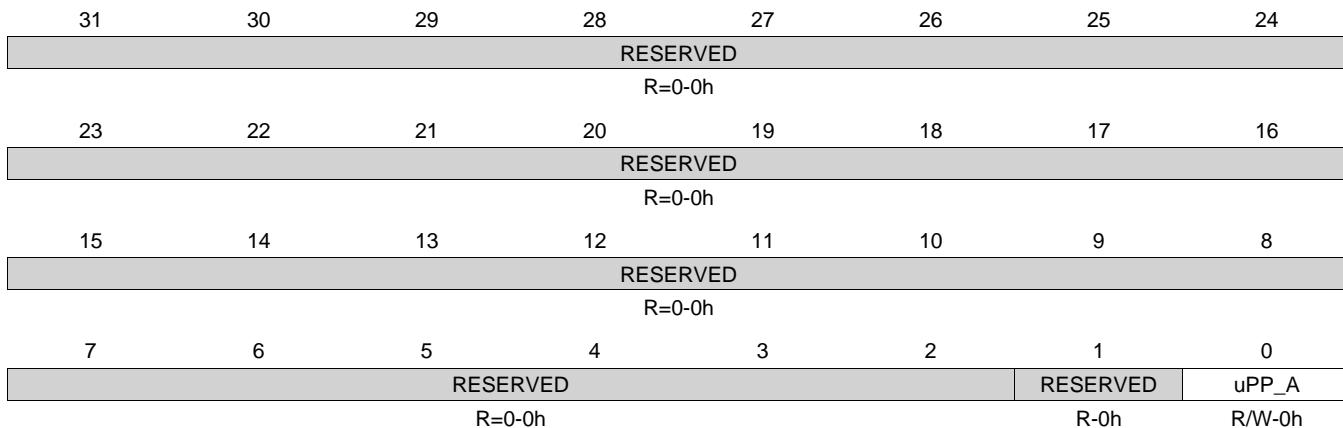
Table 1-179. PCLKCR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R=0	0h	Reserved
17	RESERVED	R	0h	Reserved
16	USB_A	R/W	0h	USB_A Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on Notes: [1] This bit is not used (R/W) in CPU2.PCLKCR11 register. USB_A clock enabled is controlled only from CPU1.PCLKCR11 register
15-2	RESERVED	R=0	0h	Reserved
1	McBSP_B	R/W	0h	McBSP_B Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	McBSP_A	R/W	0h	McBSP_A Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.17 PCLKCR12 Register (offset = 3Ah) [reset = 0h]

PCLKCR12 is shown in [Figure 1-181](#) and described in [Table 1-180](#).

Peripheral Clock Gating Registers

Figure 1-181. PCLKCR12 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

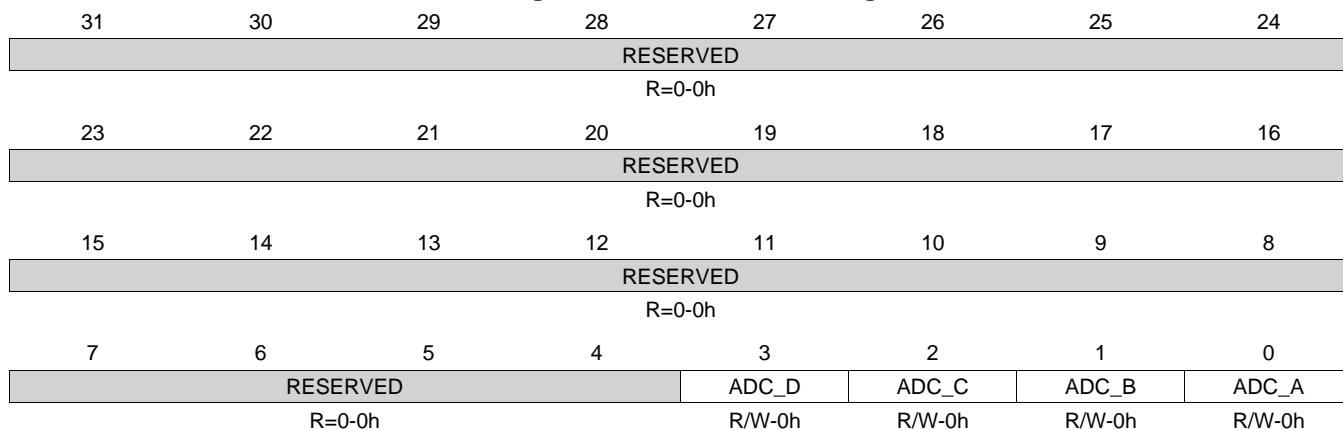
Table 1-180. PCLKCR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	RESERVED	R	0h	Reserved
0	uPP_A	R/W	0h	uPP_A Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on Notes: [1] This bit also affects the uPP message RAM wrapper associated with the respective uPP module [2] This bit is not used (R/W) in CPU2.PCLKCR12 register. UPP_A clock enabled is controlled only from CPU1.PCLKCR12 register

1.14.10.18 PCLKCR13 Register (offset = 3Ch) [reset = 0h]

PCLKCR13 is shown in [Figure 1-182](#) and described in [Table 1-181](#).

Peripheral Clock Gating Registers

Figure 1-182. PCLKCR13 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

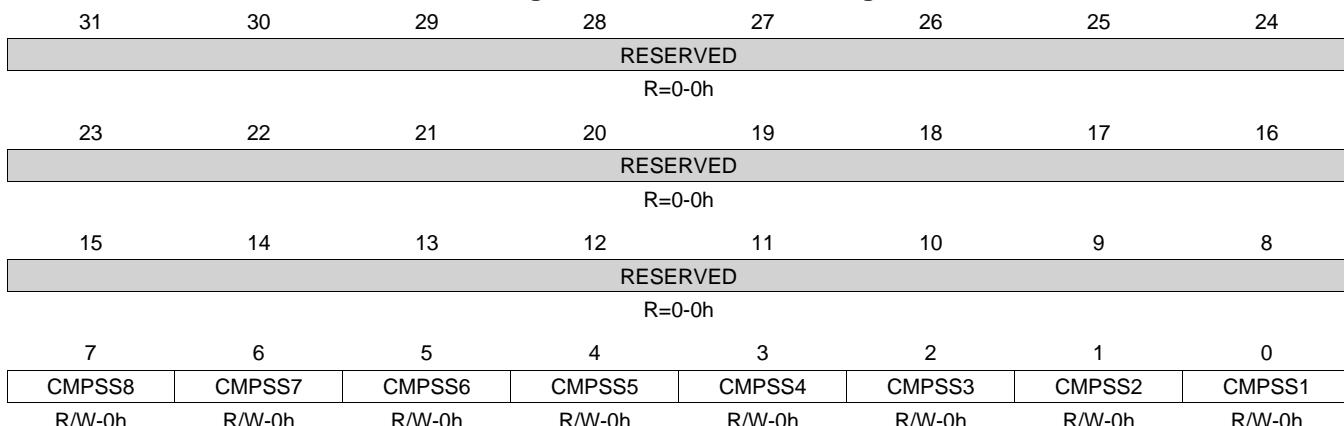
Table 1-181. PCLKCR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-4	RESERVED	R=0	0h	Reserved
3	ADC_D	R/W	0h	ADC_D Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
2	ADC_C	R/W	0h	ADC_C Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
1	ADC_B	R/W	0h	ADC_B Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	ADC_A	R/W	0h	ADC_A Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.19 PCLKCR14 Register (offset = 3Eh) [reset = 0h]

PCLKCR14 is shown in [Figure 1-183](#) and described in [Table 1-182](#).

Peripheral Clock Gating Registers

Figure 1-183. PCLKCR14 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-182. PCLKCR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	CMPSS8	R/W	0h	CMPSS8 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
6	CMPSS7	R/W	0h	CMPSS7 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
5	CMPSS6	R/W	0h	CMPSS6 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
4	CMPSS5	R/W	0h	CMPSS5 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
3	CMPSS4	R/W	0h	CMPSS4 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
2	CMPSS3	R/W	0h	CMPSS3 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
1	CMPSS2	R/W	0h	CMPSS2 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on
0	CMPSS1	R/W	0h	CMPSS1 Clock Enable bit: 0: Module clock is gated-off 1: Module clock is turned-on

1.14.10.20 PCLKCR16 Register (offset = 42h) [reset = 0h]

PCLKCR16 is shown in [Figure 1-184](#) and described in [Table 1-183](#).

Peripheral Clock Gating Registers

Figure 1-184. PCLKCR16 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED				RESERVED	DAC_C	DAC_B	DAC_A
R=0-0h				R-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	RESERVED	RESERVED
R=0-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

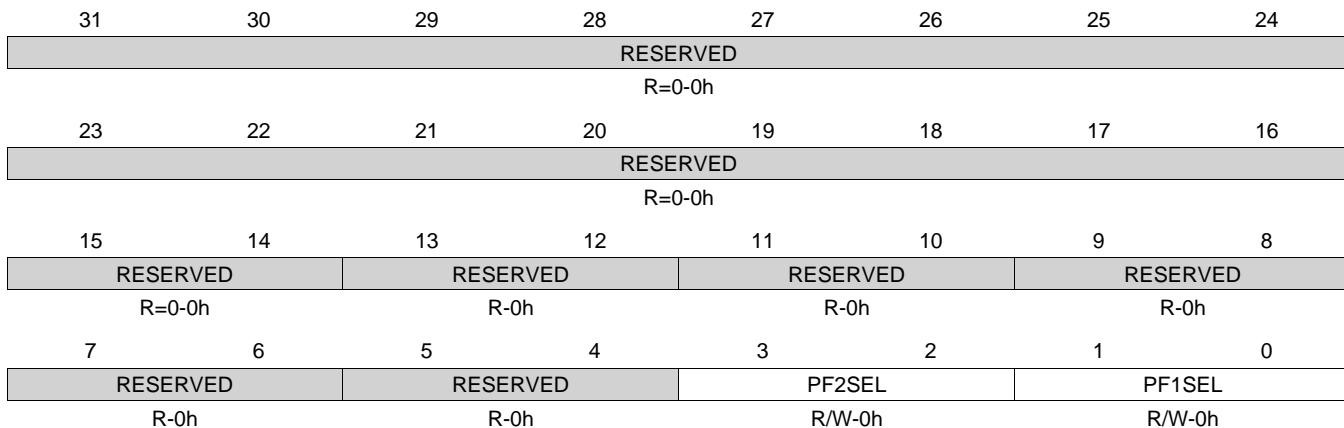
Table 1-183. PCLKCR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R=0	0h	Reserved
19	RESERVED	R	0h	Reserved
18	DAC_C	R/W	0h	Buffered_DAC_C Clock Enable Bit: 0: Module clock is gated-off 1: Module clock is turned-on
17	DAC_B	R/W	0h	Buffered_DAC_B Clock Enable Bit: 0: Module clock is gated-off 1: Module clock is turned-on
16	DAC_A	R/W	0h	Buffered_DAC_A Clock Enable Bit: 0: Module clock is gated-off 1: Module clock is turned-on
15-4	RESERVED	R=0	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.10.21 SECSEL Register (offset = 74h) [reset = 0h]

SECSEL is shown in [Figure 1-185](#) and described in [Table 1-184](#).

Secondary Master Select register for common peripherals: Selects between CLA & DMA

Figure 1-185. SECSEL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 1-184. SECSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-14	RESERVED	R=0	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11-10	RESERVED	R	0h	Reserved
9-8	RESERVED	R	0h	Reserved
7-6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-2	PF2SEL	R/W	0h	This bit selects whether the dual ported bridge is connected with DMA or CLA as the secondary master (C28x is always connected as primary master) x0: Bridge is connected to CLA x1: Bridge is connected to DMA
1-0	PF1SEL	R/W	0h	This bit selects whether the dual ported bridge is connected with DMA or CLA as the secondary master (C28x is always connected as primary master) x0: Bridge is connected to CLA x1: Bridge is connected to DMA

1.14.10.22 LPMCR Register (offset = 76h) [reset = FCh]

LPMCR is shown in [Figure 1-186](#) and described in [Table 1-185](#).

LPM Control Register

Figure 1-186. LPMCR Register

31	30	29	28	27	26	25	24
IOISODIS	RESERVED						
R/W=1-0h	R=0-0h						
23	22	21	20	19	18	17	16
RESERVED							M0M1MODE
R=0-0h							R/W-0h
15	14	13	12	11	10	9	8
WDINTE	RESERVED						
R/W-0h	R=0-0h						
7	6	5	4	3	2	1	0
QUALSTDBY							LPM
R/W-3Fh							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-185. LPMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IOISODIS	R/W=1	0h	0: Indicates IO ISOLATION is not turned ON 1: Indicates IO ISOLATION is turned ON. This bit is set one by hardware ONLY during HIB. This bit cant be set to 1 by software Writing 0 to this bit has not effect. Writing 1 to this bit deactivates IO ISOLATION Notes: [1] This bit is reserved in the register mapped to CPU2
30-18	RESERVED	R=0	0h	Reserved
17-16	M0M1MODE	R/W	0h	These bit control the state of CPU1's and CPU2's M0 & M1 memories when Device goes into HIB mode. 00: CPUx's M0 & M1 memories ON with low-leakage mode 01: CPUx's M0 & M1 memories OFF 1x: Reserved Notes: [1] Low-leakage mode for M0 & M1 memories uses the "Retention" feature of the SRAMs. [2] These bits take effect only when device goes into HIB mode. If the device is not in HIB mode, the value in this bit doesn't control the state of CPU1's and CPU2's M0 & M1 memories
15	WDINTE	R/W	0h	When this bit is set to 1, it enables the watchdog interrupt signal to wake the device from STANDBY mode. Note: [1] To use this signal, the user must also enable the WDINTn signal using the WDENINT bit in the SCSR register. This signal will not wake the device from HALT mode because the clock to watchdog module is turned off
14-8	RESERVED	R=0	0h	Reserved

Table 1-185. LPMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-2	QUALSTDBY	R/W	3Fh	Select number of OSCCLK clock cycles to qualify the selected inputs when waking from STANDBY mode: 000000 = 2 OSCCLKs 000001 = 3 OSCCLKs 111111 = 65 OSCCLKs
1-0	LPM	R/W	0h	These bits set the low power mode for the device. Takes effect when CPU executes the IDLE instruction (when IDLE instruction is out of EXE Phase of the Pipeline) 00: IDLE Mode 01: STANDBY Mode 10: HALT Mode (treated as STANDBY for CPU2) 11: HIB Mode (treated as STANDBY for CPU2) Note: [1] When debugger is connected to CPU1 (CPU1.DCON=1), if HIB is selected, system will enter HALT mode instead if SYSDBGCTL.HIBDIS=1. Refer to SYSDBGCTL for description on this.

1.14.10.23 GPIOLPSEL0 Register (offset = 78h) [reset = 0h]

GPIOLPSEL0 is shown in [Figure 1-187](#) and described in [Table 1-186](#).

GPIO LPM Wakeup select registers

Connects the selected pin to the LPM circuit. Refer to LPM section of the TRM for the wakeup capabilities of the selected pin.

Figure 1-187. GPIOLPSEL0 Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-186. GPIOLPSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
30	GPIO30	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
29	GPIO29	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
28	GPIO28	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
27	GPIO27	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
26	GPIO26	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
25	GPIO25	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
24	GPIO24	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
23	GPIO23	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
22	GPIO22	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
21	GPIO21	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
20	GPIO20	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit

Table 1-186. GPIOLPMSL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	GPIO19	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
18	GPIO18	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
17	GPIO17	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
16	GPIO16	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
15	GPIO15	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
14	GPIO14	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
13	GPIO13	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
12	GPIO12	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
11	GPIO11	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
10	GPIO10	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
9	GPIO9	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
8	GPIO8	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
7	GPIO7	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
6	GPIO6	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
5	GPIO5	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
4	GPIO4	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
3	GPIO3	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
2	GPIO2	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
1	GPIO1	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
0	GPIO0	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit

1.14.10.24 GPIOLPSEL1 Register (offset = 7Ah) [reset = 0h]

GPIOLPSEL1 is shown in [Figure 1-188](#) and described in [Table 1-187](#).

GPIO LPM Wakeup select registers

Connects the selected pin to the LPM circuit. Refer to LPM section of the TRM for the wakeup capabilities of the selected pin.

Figure 1-188. GPIOLPSEL1 Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-187. GPIOLPSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
30	GPIO62	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
29	GPIO61	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
28	GPIO60	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
27	GPIO59	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
26	GPIO58	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
25	GPIO57	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
24	GPIO56	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
23	GPIO55	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
22	GPIO54	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
21	GPIO53	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
20	GPIO52	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit

Table 1-187. GPIOLPMSL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	GPIO51	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
18	GPIO50	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
17	GPIO49	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
16	GPIO48	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
15	GPIO47	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
14	GPIO46	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
13	GPIO45	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
12	GPIO44	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
11	GPIO43	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
10	GPIO42	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
9	GPIO41	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
8	GPIO40	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
7	GPIO39	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
6	GPIO38	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
5	GPIO37	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
4	GPIO36	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
3	GPIO35	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
2	GPIO34	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
1	GPIO33	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit
0	GPIO32	R/W	0h	0 pin is dis-connected from LPM circuit 1 pin is connected to LPM circuit

1.14.10.25 TMR2CLKCTL Register (offset = 7Ch) [reset = 0h]

TMR2CLKCTL is shown in [Figure 1-189](#) and described in [Table 1-188](#).

Timer2 Clock Measurement functionality control register

Figure 1-189. TMR2CLKCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED		TMR2CLKPSCALE			TMR2CLKSRCSEL		
R=0-0h		R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-188. TMR2CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-6	RESERVED	R=0	0h	Reserved
5-3	TMR2CLKPSCALE	R/W	0h	CPU Timer 2 Clock Pre-Scale Value: These bits select the pre-scale value for the selected clock source for CPU Timer 2: 0,0,0,/1 (default on reset) 0,0,1,/2, 0,1,0,/4 0,1,1,/8 1,0,0,/16 1,0,1,spare (defaults to /16) 1,1,0,spare (defaults to /16) 1,1,1,spare (defaults to /16) Note: [1] The CPU Timer2s Clock sync logic detects an input clock edge when configured for any clock source other than SYSCLK and generates an appropriate clock pulse to the CPU timer2. If SYSCLK is approximately the same or less then the input clock source, then the user would need to configure the pre-scale value such that SYSCLK is at least twice as fast as the pre-scaled value.
2-0	TMR2CLKSRCSEL	R/W	0h	CPU Timer 2 Clock Source Select Bit: This bit selects the source for CPU Timer 2: 000 =SYSCLK Selected (default on reset, pre-scale is bypassed) 001 = INTOSC1 010 = INTOSC2 011 = XTAL 100 = FLPUMPOSC 101 = FOSCCLK 110 = AUXPLLCLK 111 = reserved

1.14.10.26 RESC Register (offset = 80h) [reset = 3h]

Register mask: 3FFFFFFFh

RESC is shown in [Figure 1-190](#) and described in [Table 1-189](#).

Reset Cause register

Figure 1-190. RESC Register

31	30	29	28	27	26	25	24
TRSTn_pin_status	XRSn_pin_status			RESERVED			
R-X	R-X			R=0-0h			
23	22	21	20	19	18	17	16
			RESERVED				
				R=0-0h			
15	14	13	12	11	10	9	8
			RESERVED				SCCRESETn
				R=0-0h			R/W=1-0h
7	6	5	4	3	2	1	0
RESERVED	HIBRESETn	HWBISTn	RESERVED	NMIWDRSn	WDRSn	XRSn	POR
R=0-0h	R/W=1-0h	R/W=1-0h	R=0-0h	R/W=1-0h	R/W=1-0h	R/W=1-1h	R/W=1-1h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-189. RESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRSTn_pin_status	R	X	Reading this bit provides the current status of TRSTn at the respective C28x CPUs TRSTn input port. Reset value is reflective of the pin status.
30	XRSn_pin_status	R	X	Reading this bit provides the current status of the XRSn pin. Reset value is reflective of the pin status.
29-16	RESERVED	R=0	0h	Reserved
15-9	RESERVED	R=0	0h	Reserved
8	SCCRESETn	R/W=1	0h	If this bit is set, indicates that the device was reset by SCCRESETn (fired by DCSM). Writing a 1 to this bit will force the bit to 0 Writing of 0 will have no effect.
7	RESERVED	R=0	0h	Reserved
6	HIBRESETn	R/W=1	0h	If this bit is set, indicates that the device was reset due to a Hibernate mode Wakeup. Writing a 1 to this bit will force the bit to 0 Writing of 0 will have no effect.
5	HWBISTn	R/W=1	0h	If this bit is set, indicates that the device was reset by HWBIST. Writing a 1 to this bit will force the bit to 0 Writing of 0 will have no effect.
4	RESERVED	R=0	0h	Reserved
3	NMIWDRSn	R/W=1	0h	If this bit is set, indicates that the device was reset by NMIWDRSn. Writing a 1 to this bit will force the bit to 0 Writing of 0 will have no effect. To know the exact cause of NMI after the reset, software needs to read CPU1/2.NMISHDFLG registers

Table 1-189. RESC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	WDRSn	R/W=1	0h	If this bit is set, indicates that the device was reset by WDRSn. Writing a 1 to this bit will force the bit to 0 Writing of 0 will have no effect. Note: [1] A bit inside WD module also provides the same information. This bit is present to keep things consistent. This register is a one-stop shop for the software to know the reset cause for the C28x core.
1	XRSn	R/W=1	1h	If this bit is set, indicates that the device was reset by XRSn. Writing a 1 to this bit will force the bit to 0 Writing of 0 will have no effect.
0	POR	R/W=1	1h	If this bit is set, indicates that the device was reset by PORn. Writing a 1 to this bit will force the bit to 0 Writing of 0 will have no effect.

1.14.11 ROM_PREFETCH_REGS Registers

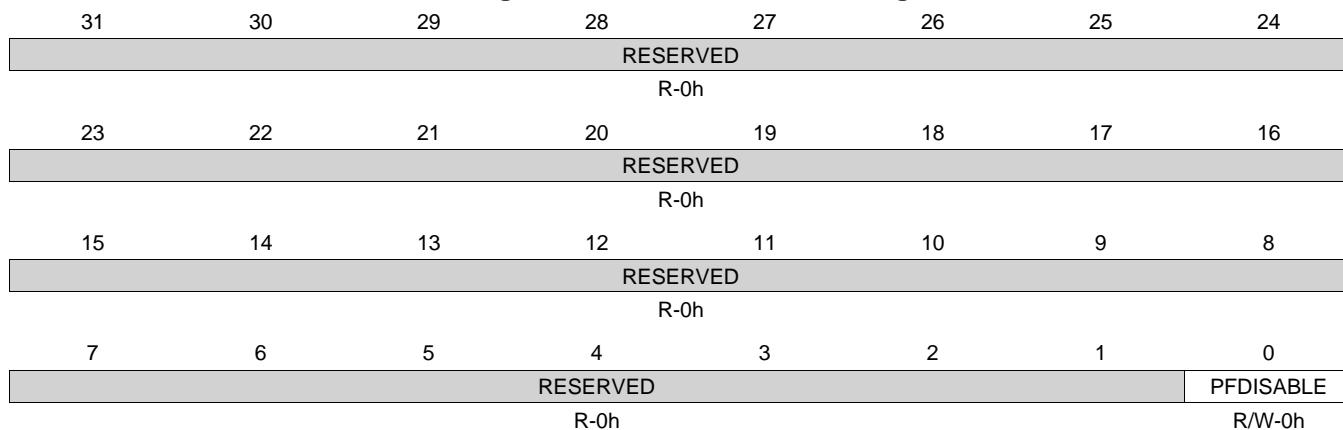
Table 1-190 lists the memory-mapped registers for the ROM_PREFETCH_REGS. All register offset addresses not listed in Table 1-190 should be considered as reserved locations and the register contents should not be modified.

Table 1-190. ROM_PREFETCH_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	ROMPREFETCH	ROM Prefetch Configuration Register	Section 1.14.11.1	EALLOW

1.14.11.1 ROMPREFETCH Register (offset = 0h) [reset = 0h]ROMPREFETCH is shown in [Figure 1-191](#) and described in [Table 1-191](#).

ROM Prefetch Configuration Register

Figure 1-191. ROMPREFETCH Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-191. ROMPREFETCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	PFDISABLE	R/W	0h	0: Prefetch is enabled for secure ROM and boot ROM. 1: Prefetch is disabled for secure ROM and boot ROM.

1.14.12 DCSM_Z1 OTP Registers

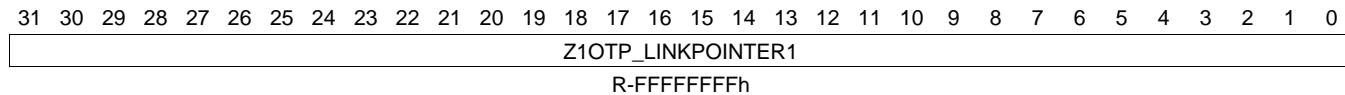
Table 1-192 lists the memory-mapped registers for the DCSM_Z1 OTP. All register offset addresses not listed in **Table 1-192** should be considered as reserved locations and the register contents should not be modified.

Table 1-192. DCSM_Z1 OTP REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	Z1OTP_LINKPOINTER1	Zone 1 Link Pointer1 in Z1 OTP	Section 1.14.12.1	
4h	Z1OTP_LINKPOINTER2	Zone 1 Link Pointer2 in Z1 OTP	Section 1.14.12.2	
8h	Z1OTP_LINKPOINTER3	Zone 1 Link Pointer3 in Z1 OTP	Section 1.14.12.3	
Ch	Z1OTP_PSWDLOCK	Secure Password Lock in Z1 OTP	Section 1.14.12.4	
10h	Z1OTP_CRCLOCK	Secure CRC Lock in Z1 OTP	Section 1.14.12.5	
18h	Z1OTP_BOOTCTRL	Boot Mode in Z1 OTP	Section 1.14.12.6	

1.14.12.1 Z1OTP_LINKPOINTER1 Register (offset = 0h) [reset = FFFFFFFFh]Z1OTP_LINKPOINTER1 is shown in [Figure 1-192](#) and described in [Table 1-193](#).

Zone 1 Link Pointer1 in Z1 OTP

Figure 1-192. Z1OTP_LINKPOINTER1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-193. Z1OTP_LINKPOINTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1OTP_LINKPOINTER1	R	FFFFFFFh	Zone1 Link Pointer 1 location in USER OTP.

1.14.12.2 Z1OTP_LINKPOINTER2 Register (offset = 4h) [reset = FFFFFFFFh]

Z1OTP_LINKPOINTER2 is shown in [Figure 1-193](#) and described in [Table 1-194](#).

Zone 1 Link Pointer2 in Z1 OTP

Figure 1-193. Z1OTP_LINKPOINTER2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1OTP_LINKPOINTER2																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-194. Z1OTP_LINKPOINTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1OTP_LINKPOINTER2	R	FFFFFFFh	Zone1 Link Pointer 2 location in USER OTP.

1.14.12.3 Z1OTP_LINKPOINTER3 Register (offset = 8h) [reset = FFFFFFFFh]

Z1OTP_LINKPOINTER3 is shown in [Figure 1-194](#) and described in [Table 1-195](#).

Zone 1 Link Pointer3 in Z1 OTP

Figure 1-194. Z1OTP_LINKPOINTER3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1OTP_LINKPOINTER3																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-195. Z1OTP_LINKPOINTER3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1OTP_LINKPOINTER3	R	FFFFFFFh	Zone1 Link Pointer 3 location in USER OTP.

1.14.12.4 Z1OTP_PSWDLOCK Register (offset = Ch) [reset = FFFFFFFFh]

Z1OTP_PSWDLOCK is shown in [Figure 1-195](#) and described in [Table 1-196](#).

Secure Password Lock in Z1 OTP

Figure 1-195. Z1OTP_PSWDLOCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1OTP_PSWDLOCK																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-196. Z1OTP_PSWDLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1OTP_PSWDLOCK	R	FFFFFFFh	Zone1 password lock location in USER OTP.

1.14.12.5 Z1OTP_CRCLOCK Register (offset = 10h) [reset = FFFFFFFFh]

Z1OTP_CRCLOCK is shown in [Figure 1-196](#) and described in [Table 1-197](#).

Secure CRC Lock in Z1 OTP

Figure 1-196. Z1OTP_CRCLOCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1OTP_CRCLOCK																															
R-FFFFFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-197. Z1OTP_CRCLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1OTP_CRCLOCK	R	FFFFFFFFh	Zone1 CRC lock location in USER OTP.

1.14.12.6 Z1OTP_BOOTCTRL Register (offset = 18h) [reset = FFFFFFFFh]

Z1OTP_BOOTCTRL is shown in [Figure 1-197](#) and described in [Table 1-198](#).

Boot Mode in Z1 OTP

Figure 1-197. Z1OTP_BOOTCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1OTP_BOOTCTRL																															
R-FFFFFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-198. Z1OTP_BOOTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1OTP_BOOTCTRL	R	FFFFFFFFh	Zone1 Boot control location in USER OTP.

1.14.13 DCSM_Z2 OTP Registers

Table 1-199 lists the memory-mapped registers for the DCSM_Z2 OTP. All register offset addresses not listed in Table 1-199 should be considered as reserved locations and the register contents should not be modified.

Table 1-199. DCSM_Z2 OTP REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	Z2OTP_LINKPOINTER1	Zone 2 Link Pointer1 in Z2 OTP	Section 1.14.13.1	
4h	Z2OTP_LINKPOINTER2	Zone 2 Link Pointer2 in Z2 OTP	Section 1.14.13.2	
8h	Z2OTP_LINKPOINTER3	Zone 2 Link Pointer3 in Z2 OTP	Section 1.14.13.3	
Ch	Z2OTP_PSWDLOCK	Secure Password Lock in Z2 OTP	Section 1.14.13.4	
10h	Z2OTP_CRCLOCK	Secure CRC Lock in Z2 OTP	Section 1.14.13.5	
18h	Z2OTP_BOOTCTRL	Boot Mode in Z2 OTP	Section 1.14.13.6	

1.14.13.1 Z2OTP_LINKPOINTER1 Register (offset = 0h) [reset = FFFFFFFFh]

Z2OTP_LINKPOINTER1 is shown in [Figure 1-198](#) and described in [Table 1-200](#).

Zone 2 Link Pointer1 in Z2 OTP

Figure 1-198. Z2OTP_LINKPOINTER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2OTP_LINKPOINTER1																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-200. Z2OTP_LINKPOINTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2OTP_LINKPOINTER1	R	FFFFFFFh	Zone2 Link Pointer 1 location in USER OTP.

1.14.13.2 Z2OTP_LINKPOINTER2 Register (offset = 4h) [reset = FFFFFFFFh]Z2OTP_LINKPOINTER2 is shown in [Figure 1-199](#) and described in [Table 1-201](#).

Zone 2 Link Pointer2 in Z2 OTP

Figure 1-199. Z2OTP_LINKPOINTER2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2OTP_LINKPOINTER2																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-201. Z2OTP_LINKPOINTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2OTP_LINKPOINTER2	R	FFFFFFFh	Zone2 Link Pointer 2 location in USER OTP.

1.14.13.3 Z2OTP_LINKPOINTER3 Register (offset = 8h) [reset = FFFFFFFFh]

Z2OTP_LINKPOINTER3 is shown in [Figure 1-200](#) and described in [Table 1-202](#).

Zone 2 Link Pointer3 in Z2 OTP

Figure 1-200. Z2OTP_LINKPOINTER3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2OTP_LINKPOINTER3																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-202. Z2OTP_LINKPOINTER3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2OTP_LINKPOINTER3	R	FFFFFFFh	Zone2 Link Pointer 3 location in USER OTP.

1.14.13.4 Z2OTP_PSWDLOCK Register (offset = Ch) [reset = FFFFFFFFh]Z2OTP_PSWDLOCK is shown in [Figure 1-201](#) and described in [Table 1-203](#).

Secure Password Lock in Z2 OTP

Figure 1-201. Z2OTP_PSWDLOCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2OTP_PSWDLOCK																															
R-FFFFFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

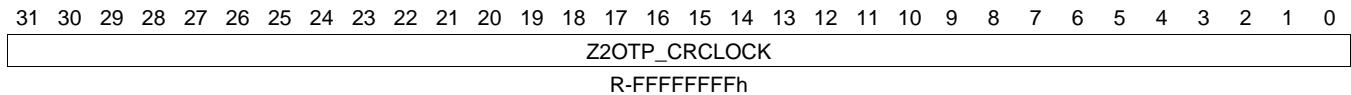
Table 1-203. Z2OTP_PSWDLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2OTP_PSWDLOCK	R	FFFFFFFFFFh	Zone2 password lock location in USER OTP.

1.14.13.5 Z2OTP_CRCLOCK Register (offset = 10h) [reset = FFFFFFFFh]

Z2OTP_CRCLOCK is shown in [Figure 1-202](#) and described in [Table 1-204](#).

Secure CRC Lock in Z2 OTP

Figure 1-202. Z2OTP_CRCLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-204. Z2OTP_CRCLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2OTP_CRCLOCK	R	FFFFFFFh	Zone2 CRC lock location in USER OTP.

1.14.13.6 Z2OTP_BOOTCTRL Register (offset = 18h) [reset = FFFFFFFFh]

Z2OTP_BOOTCTRL is shown in [Figure 1-203](#) and described in [Table 1-205](#).

Boot Mode in Z2 OTP

Figure 1-203. Z2OTP_BOOTCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2OTP_BOOTCTRL																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-205. Z2OTP_BOOTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2OTP_BOOTCTRL	R	FFFFFFFh	Zone2 Boot control location in USER OTP.

1.14.14 DCSM_Z1_REGS Registers

Table 1-206 lists the memory-mapped registers for the DCSM_Z1_REGS. All register offset addresses not listed in Table 1-206 should be considered as reserved locations and the register contents should not be modified.

Table 1-206. DCSM_Z1_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	Z1_LINKPOINTER	Zone 1 Link Pointer	Section 1.14.14.1	
2h	Z1_OTPSECLOCK	Zone 1 OTP Secure JTAG lock	Section 1.14.14.2	
4h	Z1_BOOTCTRL	Boot Mode	Section 1.14.14.3	
6h	Z1_LINKPOINTERR	Link Pointer Error	Section 1.14.14.4	
10h	Z1_CSMKEY0	Zone 1 CSM Key 0	Section 1.14.14.5	
12h	Z1_CSMKEY1	Zone 1 CSM Key 1	Section 1.14.14.6	
14h	Z1_CSMKEY2	Zone 1 CSM Key 2	Section 1.14.14.7	
16h	Z1_CSMKEY3	Zone 1 CSM Key 3	Section 1.14.14.8	
19h	Z1_CR	Zone 1 CSM Control Register	Section 1.14.14.9	
1Ah	Z1_GRABSECTR	Zone 1 Grab Flash Sectors Register	Section 1.14.14.10	
1Ch	Z1_GRABRAMR	Zone 1 Grab RAM Blocks Register	Section 1.14.14.11	
1Eh	Z1_EXEONLYSECTR	Zone 1 Flash Execute_Only Sector Register	Section 1.14.14.12	
20h	Z1_EXEONLYRAMR	Zone 1 RAM Execute_Only Block Register	Section 1.14.14.13	

1.14.14.1 Z1_LINKPOINTER Register (offset = 0h) [reset = E0000000h]

Z1_LINKPOINTER is shown in [Figure 1-204](#) and described in [Table 1-207](#).

Zone 1 Link Pointer

Figure 1-204. Z1_LINKPOINTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		LINKPOINTER													
R-7h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINKPOINTER								R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-207. Z1_LINKPOINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	7h	Reserved
28-0	LINKPOINTER	R	0h	This is resolved Link-Pointer value which is generated by looking at the three physical Link-Pointer values loaded from OTP.

1.14.14.2 Z1 OTPSECLOCK Register (offset = 2h) [reset = FFFh]

Z1 OTPSECLOCK is shown in [Figure 1-205](#) and described in [Table 1-208](#).

Zone 1 OTP Secure JTAG lock

Figure 1-205. Z1 OTPSECLOCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CRCLOCK				PSWDLOCK				RESERVED			
R-0h				R-Fh				R-Fh				R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-208. Z1 OTPSECLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	RESERVED	R	0h	Reserved
11-8	CRCLOCK	R	Fh	Value in this field gets loaded from Z1_CRCLOCK[11:8] when a read is issued to address location of Z1_CRCLOCK in OTP. 1111 : VCU has ability to calculate CRC on secure memories. Other Value : VCU doesn't have ability to calculate CRC on secure memories.
7-4	PSWDLOCK	R	Fh	Value in this field gets loaded from Z1_PSWDLOCK[7:4] when a read is issued to address location of Z1_PSWDLOCK in OTP. 1111 : CSM password locations in OTP are not protected and can be read from debugger as well as code running from anywhere. Other Value : CSM password locations in OTP are protected and can't be read without unlocking CSM of that zone.
3-0	RESERVED	R	0h	Reserved

1.14.14.3 Z1_BOOTCTRL Register (offset = 4h) [reset = 0h]

Z1_BOOTCTRL is shown in [Figure 1-206](#) and described in [Table 1-209](#).

Boot Mode

Figure 1-206. Z1_BOOTCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTPIN1						BOOTPIN0						BMODE						KEY													
R-0h						R-0h						R-0h						R-0h													

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-209. Z1_BOOTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BOOTPIN1	R	0h	This field gets loaded with Z1_BOOTCTRL[31:24] when a dummy read is issued to address location of Z1_BOOTCTRL in OTP. This assigns the pin to be used as BOOTPIN1. 0 : Pick default bootmode pin. 1 : Pick GPIO0 as BOOTPIN1. 2 : Pick GPIO1 as BOOTPIN1. n : Pick GPIOn-1 as BOOTPIN1.
23-16	BOOTPIN0	R	0h	This field gets loaded with Z1_BOOTCTRL[23:16] when a dummy read is issued to address location of Z1_BOOTCTRL in OTP. This assigns the pin to be used as BOOTPIN1. 0 : Pick default bootmode pin. 1 : Pick GPIO0 as BOOTPIN1. 2 : Pick GPIO1 as BOOTPIN1. n : Pick GPIOn-1 as BOOTPIN1.
15-8	BMODE	R	0h	This field gets loaded with Z1_BOOTCTRL[16:8] when a dummy read is issued to address location of Z1_BOOTCTRL in OTP.
7-0	KEY	R	0h	This field gets loaded with Z1_BOOTCTRL[7:0] when a dummy read is issued to address location of Z1_BOOTCTRL in OTP.

1.14.14.4 Z1_LINKPOINTERERR Register (offset = 6h) [reset = FFFFFFFFh]

Z1_LINKPOINTERERR is shown in [Figure 1-207](#) and described in [Table 1-210](#).

Link Pointer Error

Figure 1-207. Z1_LINKPOINTERERR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1_LINKPOINTERERR																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-210. Z1_LINKPOINTERERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1_LINKPOINTERERR	R	FFFFFFFh	<p>These bits indicate errors during formation of the resolved Link-Pointer value after the three physical Link-Pointer values loaded of OTP.</p> <p>0 : No Error.</p> <p>Other : Error on bit positions which is set to 1.</p>

1.14.14.5 Z1_CSMKEY0 Register (offset = 10h) [reset = 0h]

Z1_CSMKEY0 is shown in [Figure 1-208](#) and described in [Table 1-211](#).

Zone 1 CSM Key 0

Figure 1-208. Z1_CSMKEY0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1_CSMKEY0																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-211. Z1_CSMKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1_CSMKEY0	R	0h	To unlock Zone1, user needs to write this register with exact value as Z1_CSMPSWD0, programmed in OTP (zone gets unlock only if 128 bit password in OTP match with value written in four CSMKEY registers.)

1.14.14.6 Z1_CSMKEY1 Register (offset = 12h) [reset = 0h]

Z1_CSMKEY1 is shown in [Figure 1-209](#) and described in [Table 1-212](#).

Zone 1 CSM Key 1

Figure 1-209. Z1_CSMKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1_CSMKEY1																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-212. Z1_CSMKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1_CSMKEY1	R	0h	To unlock Zone1, user needs to write this register with exact value as Z1_CSMPSWD1, programmed in OTP (zone gets unlock only if 128 bit password in OTP match with value written in four CSMKEY registers.)

1.14.14.7 Z1_CSMKEY2 Register (offset = 14h) [reset = 0h]

Z1_CSMKEY2 is shown in [Figure 1-210](#) and described in [Table 1-213](#).

Zone 1 CSM Key 2

Figure 1-210. Z1_CSMKEY2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1_CSMKEY2																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-213. Z1_CSMKEY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1_CSMKEY2	R	0h	To unlock Zone1, user needs to write this register with exact value as Z1_CSMPWD2, programmed in OTP (zone gets unlock only if 128 bit password in OTP match with value written in four CSMKEY registers.)

1.14.14.8 Z1_CSMKEY3 Register (offset = 16h) [reset = 0h]

Z1_CSMKEY3 is shown in [Figure 1-211](#) and described in [Table 1-214](#).

Zone 1 CSM Key 3

Figure 1-211. Z1_CSMKEY3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z1_CSMKEY3																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-214. Z1_CSMKEY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z1_CSMKEY3	R	0h	To unlock Zone1, user needs to write this register with exact value as Z1_CSMPSWD3, programmed in OTP (zone gets unlock only if 128 bit password in OTP match with value written in four CSMKEY registers.)

1.14.14.9 Z1_CR Register (offset = 19h) [reset = 8h]

Z1_CR is shown in [Figure 1-212](#) and described in [Table 1-215](#).

Zone 1 CSM Control Register

Figure 1-212. Z1_CR Register

15	14	13	12	11	10	9	8
FORCESEC	RESERVED						
R=0/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED	ARMED	UNSECURE	ALLONE	ALLZERO	RESERVED		
R-0h	R-0h	R-0h	R-0h	R-1h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-215. Z1_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FORCESEC	R=0/W	0h	A write '1' to this field resets the state of zone. If zone is unlocked, it'll lock(secure) the zone and also resets all the bits in this register.
14-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	ARMED	R	0h	0 : Dummy read to CSM Password locations in OTP hasn't been performed. 1 : Dummy read to CSM Password locations in OTP has been performed.
5	UNSECURE	R	0h	Indicates the state of Zone. 0 : Zone is in lock(secure) state. 1 : Zone is in unlock(unsecure) state.
4	ALLONE	R	0h	Indicates the state of CSM passwords. 0 : CSM Passwords are not all ones. 1 : CSM Passwords are all ones and zone is in unlock state.
3	ALLZERO	R	1h	Indicates the state of CSM passwords. 0 : CSM Passwords are not all zeros. 1 : CSM Passwords are all zero and device is permanently locked.
2-0	RESERVED	R	0h	Reserved

1.14.14.10 Z1_GRABSECTR Register (offset = 1Ah) [reset = 0h]

Z1_GRABSECTR is shown in [Figure 1-213](#) and described in [Table 1-216](#).

Zone 1 Grab Flash Sectors Register

Figure 1-213. Z1_GRABSECTR Register

31	30	29	28	27	26	25	24
RESERVED		GRAB_BANK2		GRAB_SECTN		GRAB_SECTM	
R-0h		R-0h		R-0h		R-0h	
23	22	21	20	19	18	17	16
GRAB_SECTL		GRAB_SECTK		GRAB_SECTJ		GRAB_SECTI	
R-0h		R-0h		R-0h		R-0h	
15	14	13	12	11	10	9	8
GRAB_SECTH		GRAB_SECTG		GRAB_SECTF		GRAB_SECTE	
R-0h		R-0h		R-0h		R-0h	
7	6	5	4	3	2	1	0
GRAB_SECTD		GRAB_SECTC		GRAB_SECTB		GRAB_SECTA	
R-0h		R-0h		R-0h		R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-216. Z1_GRABSECTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	GRAB_BANK2	R	0h	Value in this field gets loaded from Z1_GRABSECT[29:28] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash BANK2 J is inaccessible. 01 : Request to allocate Flash BANK2 to Zone1. 10 : Request to allocate Flash BANK2 to Zone2. 11 : Request to make Flash sector BANK2 Non-Secure.
27-26	GRAB_SECTN	R	0h	Value in this field gets loaded from Z1_GRABSECT[27:26] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector N is inaccessible. 01 : Request to allocate Flash Sector N to Zone1. 10 : Request to allocate Flash Sector N to Zone2. 11 : Request to make Flash sector N Non-Secure.
25-24	GRAB_SECTM	R	0h	Value in this field gets loaded from Z1_GRABSECT[25:24] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector M is inaccessible. 01 : Request to allocate Flash Sector M to Zone1. 10 : Request to allocate Flash Sector M to Zone2. 11 : Request to make Flash sector M Non-Secure.
23-22	GRAB_SECTL	R	0h	Value in this field gets loaded from Z1_GRABSECT[23:22] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector L is inaccessible. 01 : Request to allocate Flash Sector L to Zone1. 10 : Request to allocate Flash Sector L to Zone2. 11 : Request to make Flash sector L Non-Secure.

Table 1-216. Z1_GRABSECTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	GRAB_SECTK	R	0h	Value in this field gets loaded from Z1_GRABSECT[21:20] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector K is inaccessible. 01 : Request to allocate Flash Sector K to Zone1. 10 : Request to allocate Flash Sector K to Zone2. 11 : Request to make Flash sector K Non-Secure.
19-18	GRAB_SECTJ	R	0h	Value in this field gets loaded from Z1_GRABSECT[19:18] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector J is inaccessible. 01 : Request to allocate Flash Sector J to Zone1. 10 : Request to allocate Flash Sector J to Zone2. 11 : Request to make Flash sector J Non-Secure.
17-16	GRAB_SECTI	R	0h	Value in this field gets loaded from Z1_GRABSECT[17:16] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector I is inaccessible. 01 : Request to allocate Flash Sector I to Zone1. 10 : Request to allocate Flash Sector I to Zone2. 11 : Request to make Flash sector I Non-Secure.
15-14	GRAB_SECTH	R	0h	Value in this field gets loaded from Z1_GRABSECT[15:14] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector H is inaccessible. 01 : Request to allocate Flash Sector H to Zone1. 10 : Request to allocate Flash Sector H to Zone2. 11 : Request to make Flash sector H Non-Secure.
13-12	GRAB_SECTG	R	0h	Value in this field gets loaded from Z1_GRABSECT[13:12] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector G is inaccessible. 01 : Request to allocate Flash Sector G to Zone1. 10 : Request to allocate Flash Sector G to Zone2. 11 : Request to make Flash sector G Non-Secure.
11-10	GRAB_SECTF	R	0h	Value in this field gets loaded from Z1_GRABSECT[11:10] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector F is inaccessible. 01 : Request to allocate Flash Sector F to Zone1. 10 : Request to allocate Flash Sector F to Zone2. 11 : Request to make Flash sector F Non-Secure.
9-8	GRAB_SECTE	R	0h	Value in this field gets loaded from Z1_GRABSECT[9:8] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector E is inaccessible. 01 : Request to allocate Flash Sector E to Zone1. 10 : Request to allocate Flash Sector E to Zone2. 11 : Request to make Flash sector E Non-Secure.
7-6	GRAB_SECTD	R	0h	Value in this field gets loaded from Z1_GRABSECT[7:6] when a read is issued to address location of Z1_GRABSECT in OTP. 00 : Invalid. Flash Sector D is inaccessible. 01 : Request to allocate Flash Sector D to Zone1. 10 : Request to allocate Flash Sector D to Zone2. 11 : Request to make Flash sector D Non-Secure.

Table 1-216. Z1_GRABSECTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	GRAB_SECTC	R	0h	<p>Value in this field gets loaded from Z1_GRABSECT[5:4] when a read is issued to address location of Z1_GRABSECT in OTP.</p> <p>00 : Invalid. Flash Sector C is inaccessible.</p> <p>01 : Request to allocate Flash Sector C to Zone1.</p> <p>10 : Request to allocate Flash Sector C to Zone2.</p> <p>11 : Request to make Flash sector C Non-Secure.</p>
3-2	GRAB_SECTB	R	0h	<p>Value in this field gets loaded from Z1_GRABSECT[3:2] when a read is issued to address location of Z1_GRABSECT in OTP.</p> <p>00 : Invalid. Flash Sector B is inaccessible.</p> <p>01 : Request to allocate Flash Sector B to Zone1.</p> <p>10 : Request to allocate Flash Sector B to Zone2.</p> <p>11 : Request to make Flash sector B Non-Secure.</p>
1-0	GRAB_SECTA	R	0h	<p>Value in this field gets loaded from Z1_GRABSECT[1:0] when a read is issued to address location of Z1_GRABSECT in OTP.</p> <p>00 : Invalid. Flash Sector A is inaccessible.</p> <p>01 : Request to allocate Flash Sector A to Zone1.</p> <p>10 : Request to allocate Flash Sector A to Zone2.</p> <p>11 : Request to make Flash sector A Non-Secure.</p>

1.14.14.11 Z1_GRABRAMR Register (offset = 1Ch) [reset = 0h]

Z1_GRABRAMR is shown in Figure 1-214 and described in Table 1-217.

Zone 1 Grab RAM Blocks Register

Figure 1-214. Z1_GRABRAMR Register

31	30	29	28	27	26	25	24
RESERVED		GRAB_CLA1		RESERVED		RESERVED	
R-0h		R-0h		R-0h		R-0h	
23	22	21	20	19	18	17	16
RESERVED		RESERVED		RESERVED		RESERVED	
R-0h		R-0h		R-0h		R-0h	
15	14	13	12	11	10	9	8
GRAB_RAM7		GRAB_RAM6		GRAB_RAM5		GRAB_RAM4	
R-0h		R-0h		R-0h		R-0h	
7	6	5	4	3	2	1	0
GRAB_RAM3		GRAB_RAM2		GRAB_RAM1		GRAB_RAM0	
R-0h		R-0h		R-0h		R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-217. Z1_GRABRAMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	GRAB_CLA1	R	0h	Value in this field gets loaded from Z1_GRABRAM[29:28] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. CLA1 is inaccessible. 01 : Request to allocate CLA1 to Zone1. 10 : Request to allocate CLA1 to Zone2. 11 : Request to make CLA1 Non-Secure.
27-16	RESERVED	R	0h	Reserved
15-14	GRAB_RAM7	R	0h	Value in this field gets loaded from Z1_GRABRAM[15:14] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. D1 RAM is inaccessible. 01 : Request to allocate D1 RAM to Zone1. 10 : Request to allocate D1 RAM to Zone2. 11 : Request to make D1 RAM Non-Secure.
13-12	GRAB_RAM6	R	0h	Value in this field gets loaded from Z1_GRABRAM[13:12] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. D0 RAM is inaccessible. 01 : Request to allocate D0 RAM to Zone1. 10 : Request to allocate D0 RAM to Zone2. 11 : Request to make D0 RAM Non-Secure.
11-10	GRAB_RAM5	R	0h	Value in this field gets loaded from Z1_GRABRAM[11:10] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. LS5 RAM is inaccessible. 01 : Request to allocate LS5 RAM to Zone1. 10 : Request to allocate LS5 RAM to Zone2. 11 : Request to make LS5 RAM Non-Secure.

Table 1-217. Z1_GRABRAMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	GRAB_RAM4	R	0h	Value in this field gets loaded from Z1_GRABRAM[9:8] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. LS4 RAM is inaccessible. 01 : Request to allocate LS4 RAM to Zone1. 10 : Request to allocate LS4 RAM to Zone2. 11 : Request to make LS4 RAM Non-Secure.
7-6	GRAB_RAM3	R	0h	Value in this field gets loaded from Z1_GRABRAM[7:6] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. LS3 RAM is inaccessible. 01 : Request to allocate LS3 RAM to Zone1. 10 : Request to allocate LS3 RAM to Zone2. 11 : Request to make LS3 RAM Non-Secure.
5-4	GRAB_RAM2	R	0h	Value in this field gets loaded from Z1_GRABRAM[5:4] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. LS2 RAM is inaccessible. 01 : Request to allocate LS2 RAM to Zone1. 10 : Request to allocate LS2 RAM to Zone2. 11 : Request to make LS2 RAM Non-Secure.
3-2	GRAB_RAM1	R	0h	Value in this field gets loaded from Z1_GRABRAM[3:2] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. LS1 RAM is inaccessible. 01 : Request to allocate LS1 RAM to Zone1. 10 : Request to allocate LS1 RAM to Zone2. 11 : Request to make LS1 RAM Non-Secure.
1-0	GRAB_RAM0	R	0h	Value in this field gets loaded from Z1_GRABRAM[1:0] when a read is issued to address location of Z1_GRABRAM in OTP. 00 : Invalid. LS0 RAM is inaccessible. 01 : Request to allocate LS0 RAM to Zone1. 10 : Request to allocate LS0 RAM to Zone2. 11 : Request to make LS0 RAM Non-Secure.

1.14.14.12 Z1_EXEONLYSECTR Register (offset = 1Eh) [reset = 0h]

Z1_EXEONLYSECTR is shown in [Figure 1-215](#) and described in [Table 1-218](#).

Zone 1 Flash Execute_Only Sector Register

Figure 1-215. Z1_EXEONLYSECTR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	EXEONLY_BA NK2	EXEONLY_SE CTN	EXEONLY_SE CTM	EXEONLY_SE CTL	EXEONLY_SE CTK	EXEONLY_SE CTJ	EXEONLY_SE CTI
R-0h							
7	6	5	4	3	2	1	0
EXEONLY_SE CTH	EXEONLY_SE CTG	EXEONLY_SE CTF	EXEONLY_SE CTE	EXEONLY_SE CTD	EXEONLY_SE CTC	EXEONLY_SE CTB	EXEONLY_SE CTA
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-218. Z1_EXEONLYSECTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	EXEONLY_BANK2	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYSECT[14:14] when a read is issued to Z1_EXEONLYSECT address location in OTP.</p> <p>0 : Execute-Only protection is enabled for Flash BANK2 (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for Flash BANK2 (only if it's allocated to Zone1)</p>
13	EXEONLY_SECTN	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYSECT[13:13] when a read is issued to Z1_EXEONLYSECT address location in OTP.</p> <p>0 : Execute-Only protection is enabled for Flash Sector N (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for Flash Sector N (only if it's allocated to Zone1)</p>
12	EXEONLY_SECTM	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYSECT[12:12] when a read is issued to Z1_EXEONLYSECT address location in OTP.</p> <p>0 : Execute-Only protection is enabled for Flash Sector M (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for Flash Sector M (only if it's allocated to Zone1)</p>
11	EXEONLY_SECTL	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYSECT[11:11] when a read is issued to Z1_EXEONLYSECT address location in OTP.</p> <p>0 : Execute-Only protection is enabled for Flash Sector L (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for Flash Sector L (only if it's allocated to Zone1)</p>

Table 1-218. Z1_EXEONLYSECTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	EXEONLY_SECTK	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[10:10] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector K (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector K (only if it's allocated to Zone1)
9	EXEONLY_SECTJ	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[9:9] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector J (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector J (only if it's allocated to Zone1)
8	EXEONLY_SECTI	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[8:8] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector I (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector I (only if it's allocated to Zone1)
7	EXEONLY_SECTH	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[7:7] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector H (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector H (only if it's allocated to Zone1)
6	EXEONLY_SECTG	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[6:6] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector G (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector G (only if it's allocated to Zone1)
5	EXEONLY_SECTF	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[5:5] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector F (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector F (only if it's allocated to Zone1)
4	EXEONLY_SECTE	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[4:4] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector E (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector E (only if it's allocated to Zone1)
3	EXEONLY_SECTD	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[3:3] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector D (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector D (only if it's allocated to Zone1)
2	EXEONLY_SECTC	R	0h	Value in this field gets loaded from Z1_EXEONLYSECT[2:2] when a read is issued to Z1_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector C (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for Flash Sector C (only if it's allocated to Zone1)

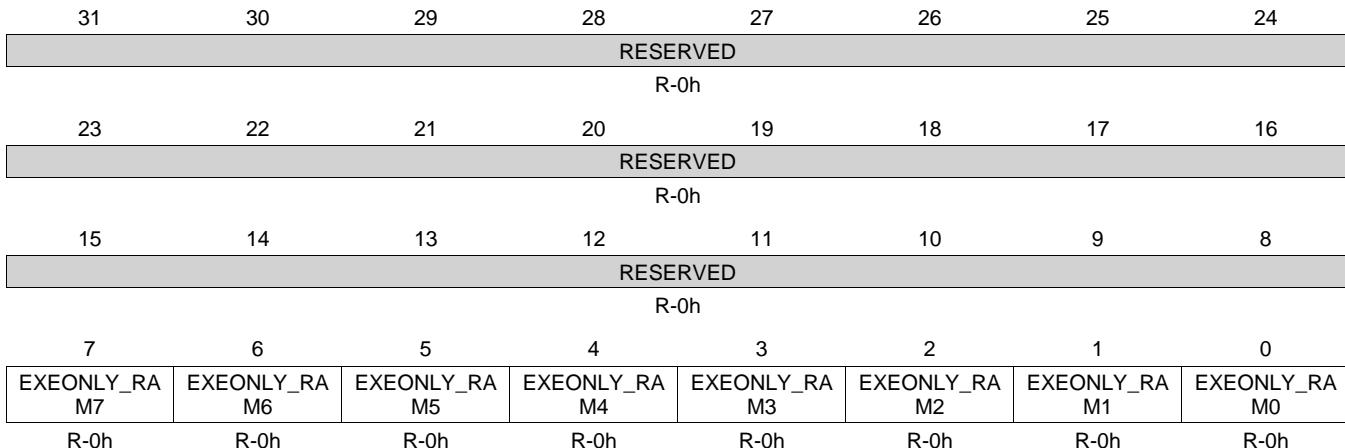
Table 1-218. Z1_EXEONLYSECTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EXEONLY_SECTB	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYSECT[1:1] when a read is issued to Z1_EXEONLYSECT address location in OTP.</p> <p>0 : Execute-Only protection is enabled for Flash Sector B (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for Flash Sector B (only if it's allocated to Zone1)</p>
0	EXEONLY_SECTA	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYSECT[0:0] when a read is issued to Z1_EXEONLYSECT address location in OTP.</p> <p>0 : Execute-Only protection is enabled for Flash Sector A (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for Flash Sector A (only if it's allocated to Zone1)</p>

1.14.14.13 Z1_EXEONLYRAMR Register (offset = 20h) [reset = 0h]

Z1_EXEONLYRAMR is shown in [Figure 1-216](#) and described in [Table 1-219](#).

Zone 1 RAM Execute_Only Block Register

Figure 1-216. Z1_EXEONLYRAMR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-219. Z1_EXEONLYRAMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	RESERVED	R	0h	Reserved
7	EXEONLY_RAM7	R	0h	Value in this field gets loaded from Z1_EXEONLYRAM[7:7] when a read is issued to Z1_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for D1 RAM (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for D1 RAM (only if it's allocated to Zone1)
6	EXEONLY_RAM6	R	0h	Value in this field gets loaded from Z1_EXEONLYRAM[6:6] when a read is issued to Z1_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for D0 RAM (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for D0 RAM (only if it's allocated to Zone1)
5	EXEONLY_RAM5	R	0h	Value in this field gets loaded from Z1_EXEONLYRAM[5:5] when a read is issued to Z1_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for LS5 RAM (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for LS5 RAM (only if it's allocated to Zone1)
4	EXEONLY_RAM4	R	0h	Value in this field gets loaded from Z1_EXEONLYRAM[4:4] when a read is issued to Z1_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for LS4 RAM (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for LS4 RAM (only if it's allocated to Zone1)
3	EXEONLY_RAM3	R	0h	Value in this field gets loaded from Z1_EXEONLYRAM[3:3] when a read is issued to Z1_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for LS3 RAM (only if it's allocated to Zone1) 1 : Execute-Only protection is disabled for LS3 RAM (only if it's allocated to Zone1)

Table 1-219. Z1_EXEONLYRAMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EXEONLY_RAM2	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYRAM[2:2] when a read is issued to Z1_EXEONLYRAM address location in OTP.</p> <p>0 : Execute-Only protection is enabled for LS2 RAM (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for LS2 RAM (only if it's allocated to Zone1)</p>
1	EXEONLY_RAM1	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYRAM[1:1] when a read is issued to Z1_EXEONLYRAM address location in OTP.</p> <p>0 : Execute-Only protection is enabled for LS1 RAM (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for LS1 RAM (only if it's allocated to Zone1)</p>
0	EXEONLY_RAM0	R	0h	<p>Value in this field gets loaded from Z1_EXEONLYRAM[0:0] when a read is issued to Z1_EXEONLYRAM address location in OTP.</p> <p>0 : Execute-Only protection is enabled for LS0 RAM (only if it's allocated to Zone1)</p> <p>1 : Execute-Only protection is disabled for LS0 RAM (only if it's allocated to Zone1)</p>

1.14.15 DCSM_Z2_REGS Registers

Table 1-220 lists the memory-mapped registers for the DCSM_Z2_REGS. All register offset addresses not listed in Table 1-220 should be considered as reserved locations and the register contents should not be modified.

Table 1-220. DCSM_Z2_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	Z2_LINKPOINTER	Zone 2 Link Pointer	Section 1.14.15.1	
2h	Z2 OTPSECLOCK	Zone 2 OTP Secure JTAG lock	Section 1.14.15.2	
4h	Z2_BOOTCTRL	Boot Mode	Section 1.14.15.3	
6h	Z2_LINKPOINTERR	Link Pointer Error	Section 1.14.15.4	
10h	Z2_CSMKEY0	Zone 2 CSM Key 0	Section 1.14.15.5	
12h	Z2_CSMKEY1	Zone 2 CSM Key 1	Section 1.14.15.6	
14h	Z2_CSMKEY2	Zone 2 CSM Key 2	Section 1.14.15.7	
16h	Z2_CSMKEY3	Zone 2 CSM Key 3	Section 1.14.15.8	
19h	Z2_CR	Zone 2 CSM Control Register	Section 1.14.15.9	
1Ah	Z2_GRABSECTR	Zone 2 Grab Flash Sectors Register	Section 1.14.15.10	
1Ch	Z2_GRABRAMR	Zone 2 Grab RAM Blocks Register	Section 1.14.15.11	
1Eh	Z2_EXEONLYSECTR	Zone 2 Flash Execute_Only Sector Register	Section 1.14.15.12	
20h	Z2_EXEONLYRAMR	Zone 2 RAM Execute_Only Block Register	Section 1.14.15.13	

1.14.15.1 Z2_LINKPOINTER Register (offset = 0h) [reset = E0000000h]Z2_LINKPOINTER is shown in [Figure 1-217](#) and described in [Table 1-221](#).

Zone 2 Link Pointer

Figure 1-217. Z2_LINKPOINTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		LINKPOINTER													
R-7h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINKPOINTER								R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-221. Z2_LINKPOINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	7h	Reserved
28-0	LINKPOINTER	R	0h	This is the Resolved Link-Pointer value which is generated by looking at the three physical Link-Pointer values loaded from OTP.

1.14.15.2 Z2 OTPSECLOCK Register (offset = 2h) [reset = FFFh]

Z2 OTPSECLOCK is shown in [Figure 1-218](#) and described in [Table 1-222](#).

Zone 2 OTP Secure JTAG lock

Figure 1-218. Z2 OTPSECLOCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CRCLOCK				PSWDLOCK				RESERVED			
R-0h				R-Fh				R-Fh				R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-222. Z2 OTPSECLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	RESERVED	R	0h	Reserved
11-8	CRCLOCK	R	Fh	<p>Value in this field gets loaded from Z2_CRCLOCK[11:8] when a read is issued to address location of Z2_CRCLOCK in OTP.</p> <p>1111 : VCU has ability to calculate CRC on secure memories.</p> <p>Other Value : VCU doesn't have ability to calculate CRC on secure memories.</p>
7-4	PSWDLOCK	R	Fh	<p>Value in this field gets loaded from Z2_PSWDLOCK[7:4] when a read is issued to address location of Z2_PSWDLOCK in OTP.</p> <p>1111 : CSM password locations in OTP are not protected and can be read from debugger as well as code running from anywhere.</p> <p>Other Value : CSM password locations in OTP are protected and can't be read without unlocking CSM of that zone.</p>
3-0	RESERVED	R	0h	Reserved

1.14.15.3 Z2_BOOTCTRL Register (offset = 4h) [reset = 0h]

Z2_BOOTCTRL is shown in [Figure 1-219](#) and described in [Table 1-223](#).

Boot Mode

Figure 1-219. Z2_BOOTCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTPIN1						BOOTPIN0						BMODE						KEY													
R-0h						R-0h						R-0h						R-0h													

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-223. Z2_BOOTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BOOTPIN1	R	0h	This field gets loaded with Z2_BOOTCTRL[31:24] when a dummy read is issued to address location of Z2_BOOTCTRL in OTP. This assigns the pin to be used as BOOTPIN1. 0 : Pick default bootmode pin. 1 : Pick GPIO0 as BOOTPIN1. 2 : Pick GPIO1 as BOOTPIN1. n : Pick GPIOn-1 as BOOTPIN1.
23-16	BOOTPIN0	R	0h	This field gets loaded with Z2_BOOTCTRL[23:16] when a dummy read is issued to address location of Z2_BOOTCTRL in OTP. This assigns the pin to be used as BOOTPIN1. 0 : Pick default bootmode pin. 1 : Pick GPIO0 as BOOTPIN1. 2 : Pick GPIO1 as BOOTPIN1. n : Pick GPIOn-1 as BOOTPIN1.
15-8	BMODE	R	0h	This field gets loaded with Z2_BOOTCTRL[16:8] when a dummy read is issued to address location of Z2_BOOTCTRL in OTP.
7-0	KEY	R	0h	This field gets loaded with Z2_BOOTCTRL[7:0] when a dummy read is issued to address location of Z2_BOOTCTRL in OTP.

1.14.15.4 Z2_LINKPOINTERERR Register (offset = 6h) [reset = FFFFFFFFh]

Z2_LINKPOINTERERR is shown in [Figure 1-220](#) and described in [Table 1-224](#).

Link Pointer Error

Figure 1-220. Z2_LINKPOINTERERR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2_LINKPOINTERERR																															
R-FFFFFFFh																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-224. Z2_LINKPOINTERERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2_LINKPOINTERERR	R	FFFFFFFh	<p>These bits indicate errors during formation of the resolved Link-Pointer value after the three physical Link-Pointer values loaded of OTP.</p> <p>0 : No Error.</p> <p>Other : Error on bit positions which is set to 1.</p>

1.14.15.5 Z2_CSMKEY0 Register (offset = 10h) [reset = 0h]

Z2_CSMKEY0 is shown in [Figure 1-221](#) and described in [Table 1-225](#).

Zone 2 CSM Key 0

Figure 1-221. Z2_CSMKEY0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2_CSMKEY0																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-225. Z2_CSMKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2_CSMKEY0	R	0h	To unlock Zone2, user needs to write this register with exact value as Z2_CSMPSWD0, programmed in OTP (zone gets unlock only if 128 bit password in OTP match with value written in four CSMKEY registers.)

1.14.15.6 Z2_CSMKEY1 Register (offset = 12h) [reset = 0h]

Z2_CSMKEY1 is shown in [Figure 1-222](#) and described in [Table 1-226](#).

Zone 2 CSM Key 1

Figure 1-222. Z2_CSMKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2_CSMKEY1																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-226. Z2_CSMKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2_CSMKEY1	R	0h	To unlock Zone2, user needs to write this register with exact value as Z2_CSMPSWD1, programmed in OTP (zone gets unlock only if 128 bit password in OTP match with value written in four CSMKEY registers.)

1.14.15.7 Z2_CSMKEY2 Register (offset = 14h) [reset = 0h]Z2_CSMKEY2 is shown in [Figure 1-223](#) and described in [Table 1-227](#).

Zone 2 CSM Key 2

Figure 1-223. Z2_CSMKEY2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2_CSMKEY2																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-227. Z2_CSMKEY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2_CSMKEY2	R	0h	To unlock Zone2, user needs to write this register with exact value as Z2_CSMPWD2, programmed in OTP (zone gets unlock only if 128 bit password in OTP match with value written in four CSMKEY registers.)

1.14.15.8 Z2_CSMKEY3 Register (offset = 16h) [reset = 0h]

Z2_CSMKEY3 is shown in [Figure 1-224](#) and described in [Table 1-228](#).

Zone 2 CSM Key 3

Figure 1-224. Z2_CSMKEY3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z2_CSMKEY3																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-228. Z2_CSMKEY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z2_CSMKEY3	R	0h	To unlock Zone2, user needs to write this register with exact value as Z2_CSMPWD3, programmed in OTP (zone gets unlock only if 128 bit password in OTP match with value written in four CSMKEY registers.)

1.14.15.9 Z2_CR Register (offset = 19h) [reset = 8h]

Z2_CR is shown in [Figure 1-225](#) and described in [Table 1-229](#).

Zone 2 CSM Control Register

Figure 1-225. Z2_CR Register

15	14	13	12	11	10	9	8
FORCESEC	RESERVED						
R=0/W-0h	R=0-0h						
7	6	5	4	3	2	1	0
RESERVED	ARMED	UNSECURE	ALLONE	ALLZERO	RESERVED		
R-0h	R-0h	R-0h	R-0h	R-1h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-229. Z2_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FORCESEC	R=0/W	0h	A write '1' to this field resets the state of zone. If zone is unlocked, it'll lock(secure) the zone and also resets all the bits in this register.
14-8	RESERVED	R=0	0h	Reserved
7	RESERVED	R	0h	Reserved
6	ARMED	R	0h	0 : Dummy read to CSM Password locations in OTP hasn't been performed. 1 : Dummy read to CSM Password locations in OTP has been performed.
5	UNSECURE	R	0h	Indicates the state of Zone. 0 : Zone is in lock(secure) state. 1 : Zone is in unlock(unsecure) state.
4	ALLONE	R	0h	Indicates the state of CSM passwords. 0 : CSM Passwords are not all ones. 1 : CSM Passwords are all ones and zone is in unlock state.
3	ALLZERO	R	1h	Indicates the state of CSM passwords. 0 : CSM Passwords are not all zeros. 1 : CSM Passwords are all zero and device is permanently locked.
2-0	RESERVED	R	0h	Reserved

1.14.15.10 Z2_GRABSECTR Register (offset = 1Ah) [reset = 0h]

Z2_GRABSECTR is shown in [Figure 1-226](#) and described in [Table 1-230](#).

Zone 2 Grab Flash Sectors Register

Figure 1-226. Z2_GRABSECTR Register

31	30	29	28	27	26	25	24
RESERVED		GRAB_BANK2		GRAB_SECTN		GRAB_SECTM	
R-0h		R-0h		R-0h		R-0h	
23	22	21	20	19	18	17	16
GRAB_SECTL		GRAB_SECTK		GRAB_SECTJ		GRAB_SECTI	
R-0h		R-0h		R-0h		R-0h	
15	14	13	12	11	10	9	8
GRAB_SECTH		GRAB_SECTG		GRAB_SECTF		GRAB_SECTE	
R-0h		R-0h		R-0h		R-0h	
7	6	5	4	3	2	1	0
GRAB_SECTD		GRAB_SECTC		GRAB_SECTB		GRAB_SECTA	
R-0h		R-0h		R-0h		R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-230. Z2_GRABSECTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	GRAB_BANK2	R	0h	Value in this field gets loaded from Z2_GRABSECT[29:28] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash BANK2 J is inaccessible. 01 : Request to allocate Flash BANK2 to Zone2. 10 : Request to allocate Flash BANK2 to Zone2. 11 : Request to make Flash sector BANK2 Non-Secure.
27-26	GRAB_SECTN	R	0h	Value in this field gets loaded from Z2_GRABSECT[27:26] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector N is inaccessible. 01 : Request to allocate Flash Sector N to Zone2. 10 : Request to allocate Flash Sector N to Zone2. 11 : Request to make Flash sector N Non-Secure.
25-24	GRAB_SECTM	R	0h	Value in this field gets loaded from Z2_GRABSECT[25:24] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector M is inaccessible. 01 : Request to allocate Flash Sector M to Zone2. 10 : Request to allocate Flash Sector M to Zone2. 11 : Request to make Flash sector M Non-Secure.
23-22	GRAB_SECTL	R	0h	Value in this field gets loaded from Z2_GRABSECT[23:22] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector L is inaccessible. 01 : Request to allocate Flash Sector L to Zone2. 10 : Request to allocate Flash Sector L to Zone2. 11 : Request to make Flash sector L Non-Secure.

Table 1-230. Z2_GRABSECTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	GRAB_SECTK	R	0h	Value in this field gets loaded from Z2_GRABSECT[21:20] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector K is inaccessible. 01 : Request to allocate Flash Sector K to Zone2. 10 : Request to allocate Flash Sector K to Zone2. 11 : Request to make Flash sector K Non-Secure.
19-18	GRAB_SECTJ	R	0h	Value in this field gets loaded from Z2_GRABSECT[19:18] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector J is inaccessible. 01 : Request to allocate Flash Sector J to Zone2. 10 : Request to allocate Flash Sector J to Zone2. 11 : Request to make Flash sector J Non-Secure.
17-16	GRAB_SECTI	R	0h	Value in this field gets loaded from Z2_GRABSECT[17:16] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector I is inaccessible. 01 : Request to allocate Flash Sector I to Zone2. 10 : Request to allocate Flash Sector I to Zone2. 11 : Request to make Flash sector I Non-Secure.
15-14	GRAB_SECTH	R	0h	Value in this field gets loaded from Z2_GRABSECT[15:14] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector H is inaccessible. 01 : Request to allocate Flash Sector H to Zone2. 10 : Request to allocate Flash Sector H to Zone2. 11 : Request to make Flash sector H Non-Secure.
13-12	GRAB_SECTG	R	0h	Value in this field gets loaded from Z2_GRABSECT[13:12] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector G is inaccessible. 01 : Request to allocate Flash Sector G to Zone2. 10 : Request to allocate Flash Sector G to Zone2. 11 : Request to make Flash sector G Non-Secure.
11-10	GRAB_SECTF	R	0h	Value in this field gets loaded from Z2_GRABSECT[11:10] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector F is inaccessible. 01 : Request to allocate Flash Sector F to Zone2. 10 : Request to allocate Flash Sector F to Zone2. 11 : Request to make Flash sector F Non-Secure.
9-8	GRAB_SECTE	R	0h	Value in this field gets loaded from Z2_GRABSECT[9:8] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector E is inaccessible. 01 : Request to allocate Flash Sector E to Zone2. 10 : Request to allocate Flash Sector E to Zone2. 11 : Request to make Flash sector E Non-Secure.
7-6	GRAB_SECTD	R	0h	Value in this field gets loaded from Z2_GRABSECT[7:6] when a read is issued to address location of Z2_GRABSECT in OTP. 00 : Invalid. Flash Sector D is inaccessible. 01 : Request to allocate Flash Sector D to Zone2. 10 : Request to allocate Flash Sector D to Zone2. 11 : Request to make Flash sector D Non-Secure.

Table 1-230. Z2_GRABSECTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	GRAB_SECTC	R	0h	<p>Value in this field gets loaded from Z2_GRABSECT[5:4] when a read is issued to address location of Z2_GRABSECT in OTP.</p> <p>00 : Invalid. Flash Sector C is inaccessible.</p> <p>01 : Request to allocate Flash Sector C to Zone2.</p> <p>10 : Request to allocate Flash Sector C to Zone2.</p> <p>11 : Request to make Flash sector C Non-Secure.</p>
3-2	GRAB_SECTB	R	0h	<p>Value in this field gets loaded from Z2_GRABSECT[3:2] when a read is issued to address location of Z2_GRABSECT in OTP.</p> <p>00 : Invalid. Flash Sector B is inaccessible.</p> <p>01 : Request to allocate Flash Sector B to Zone2.</p> <p>10 : Request to allocate Flash Sector B to Zone2.</p> <p>11 : Request to make Flash sector B Non-Secure.</p>
1-0	GRAB_SECTA	R	0h	<p>Value in this field gets loaded from Z2_GRABSECT[1:0] when a read is issued to address location of Z2_GRABSECT in OTP.</p> <p>00 : Invalid. Flash Sector A is inaccessible.</p> <p>01 : Request to allocate Flash Sector A to Zone2.</p> <p>10 : Request to allocate Flash Sector A to Zone2.</p> <p>11 : Request to make Flash sector A Non-Secure.</p>

1.14.15.11 Z2_GRABRAMR Register (offset = 1Ch) [reset = 0h]

Z2_GRABRAMR is shown in Figure 1-227 and described in Table 1-231.

Zone 2 Grab RAM Blocks Register

Figure 1-227. Z2_GRABRAMR Register

31	30	29	28	27	26	25	24
RESERVED		GRAB_CLA1		RESERVED			
R-0h		R-0h		R-0h			
23	22	21	20	19	18	17	16
RESERVED				R-0h			
15	14	13	12	11	10	9	8
GRAB_RAM7		GRAB_RAM6		GRAB_RAM5		GRAB_RAM4	
R-0h		R-0h		R-0h		R-0h	
7	6	5	4	3	2	1	0
GRAB_RAM3		GRAB_RAM2		GRAB_RAM1		GRAB_RAM0	
R-0h		R-0h		R-0h		R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-231. Z2_GRABRAMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	GRAB_CLA1	R	0h	Value in this field gets loaded from Z2_GRABRAM[29:28] when a read is issued to address location of Z2_GRABRAM in OTP. 00 : Invalid. CLA1 is inaccessible. 01 : Request to allocate CLA1 to Zone2. 10 : Request to allocate CLA1 to Zone2. 11 : Request to make CLA1 Non-Secure.
27-16	RESERVED	R	0h	Reserved
15-14	GRAB_RAM7	R	0h	Value in this field gets loaded from Z2_GRABRAM[15:14] when a read is issued to address location of Z2_GRABRAM in OTP. 00 : Invalid. D1 RAM is inaccessible. 01 : Request to allocate D1 RAM to Zone2. 10 : Request to allocate D1 RAM to Zone2. 11 : Request to make D1 RAM Non-Secure.
13-12	GRAB_RAM6	R	0h	Value in this field gets loaded from Z2_GRABRAM[13:12] when a read is issued to address location of Z2_GRABRAM in OTP. 00 : Invalid. D0 RAM is inaccessible. 01 : Request to allocate D0 RAM to Zone2. 10 : Request to allocate D0 RAM to Zone2. 11 : Request to make D0 RAM Non-Secure.
11-10	GRAB_RAM5	R	0h	Value in this field gets loaded from Z2_GRABRAM[11:10] when a read is issued to address location of Z2_GRABRAM in OTP. 00 : Invalid. LS5 RAM is inaccessible. 01 : Request to allocate LS5 RAM to Zone2. 10 : Request to allocate LS5 RAM to Zone2. 11 : Request to make LS5 RAM Non-Secure.

Table 1-231. Z2_GRABRAMR Register Field Descriptions (continued)

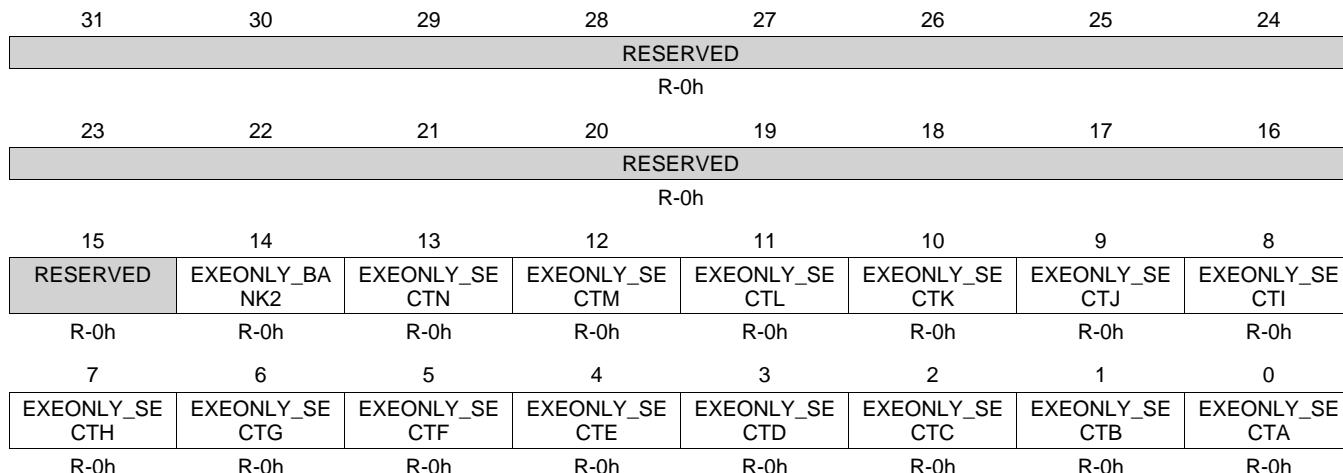
Bit	Field	Type	Reset	Description
9-8	GRAB_RAM4	R	0h	<p>Value in this field gets loaded from Z2_GRABRAM[9:8] when a read is issued to address location of Z2_GRABRAM in OTP.</p> <p>00 : Invalid. LS4 RAM is inaccessible.</p> <p>01 : Request to allocate LS4 RAM to Zone2.</p> <p>10 : Request to allocate LS4 RAM to Zone2.</p> <p>11 : Request to make LS4 RAM Non-Secure.</p>
7-6	GRAB_RAM3	R	0h	<p>Value in this field gets loaded from Z2_GRABRAM[7:6] when a read is issued to address location of Z2_GRABRAM in OTP.</p> <p>00 : Invalid. LS3 RAM is inaccessible.</p> <p>01 : Request to allocate LS3 RAM to Zone2.</p> <p>10 : Request to allocate LS3 RAM to Zone2.</p> <p>11 : Request to make LS3 RAM Non-Secure.</p>
5-4	GRAB_RAM2	R	0h	<p>Value in this field gets loaded from Z2_GRABRAM[5:4] when a read is issued to address location of Z2_GRABRAM in OTP.</p> <p>00 : Invalid. LS2 RAM is inaccessible.</p> <p>01 : Request to allocate LS2 RAM to Zone2.</p> <p>10 : Request to allocate LS2 RAM to Zone2.</p> <p>11 : Request to make LS2 RAM Non-Secure.</p>
3-2	GRAB_RAM1	R	0h	<p>Value in this field gets loaded from Z2_GRABRAM[3:2] when a read is issued to address location of Z2_GRABRAM in OTP.</p> <p>00 : Invalid. LS1 RAM is inaccessible.</p> <p>01 : Request to allocate LS1 RAM to Zone2.</p> <p>10 : Request to allocate LS1 RAM to Zone2.</p> <p>11 : Request to make LS1 RAM Non-Secure.</p>
1-0	GRAB_RAM0	R	0h	<p>Value in this field gets loaded from Z2_GRABRAM[1:0] when a read is issued to address location of Z2_GRABRAM in OTP.</p> <p>00 : Invalid. LS0 RAM is inaccessible.</p> <p>01 : Request to allocate LS0 RAM to Zone2.</p> <p>10 : Request to allocate LS0 RAM to Zone2.</p> <p>11 : Request to make LS0 RAM Non-Secure.</p>

1.14.15.12 Z2_EXEONLYSECTR Register (offset = 1Eh) [reset = 0h]

Z2_EXEONLYSECTR is shown in [Figure 1-228](#) and described in [Table 1-232](#).

Zone 2 Flash Execute_Only Sector Register

Figure 1-228. Z2_EXEONLYSECTR Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-232. Z2_EXEONLYSECTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	EXEONLY_BANK2	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[14:14] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash BANK2 (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash BANK2 (only if it's allocated to Zone2)
13	EXEONLY_SECTN	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[13:13] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector N (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector N (only if it's allocated to Zone2)
12	EXEONLY_SECTM	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[12:12] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector M (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector M (only if it's allocated to Zone2)
11	EXEONLY_SECTL	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[11:11] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector L (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector L (only if it's allocated to Zone2)

Table 1-232. Z2_EXEONLYSECTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	EXEONLY_SECTK	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[10:10] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector K (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector K (only if it's allocated to Zone2)
9	EXEONLY_SECTJ	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[9:9] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector J (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector J (only if it's allocated to Zone2)
8	EXEONLY_SECTI	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[8:8] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector I (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector I (only if it's allocated to Zone2)
7	EXEONLY_SECTH	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[7:7] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector H (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector H (only if it's allocated to Zone2)
6	EXEONLY_SECTG	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[6:6] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector G (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector G (only if it's allocated to Zone2)
5	EXEONLY_SECTF	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[5:5] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector F (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector F (only if it's allocated to Zone2)
4	EXEONLY_SECTE	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[4:4] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector E (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector E (only if it's allocated to Zone2)
3	EXEONLY_SECTD	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[3:3] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector D (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector D (only if it's allocated to Zone2)
2	EXEONLY_SECTC	R	0h	Value in this field gets loaded from Z2_EXEONLYSECT[2:2] when a read is issued to Z2_EXEONLYSECT address location in OTP. 0 : Execute-Only protection is enabled for Flash Sector C (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for Flash Sector C (only if it's allocated to Zone2)

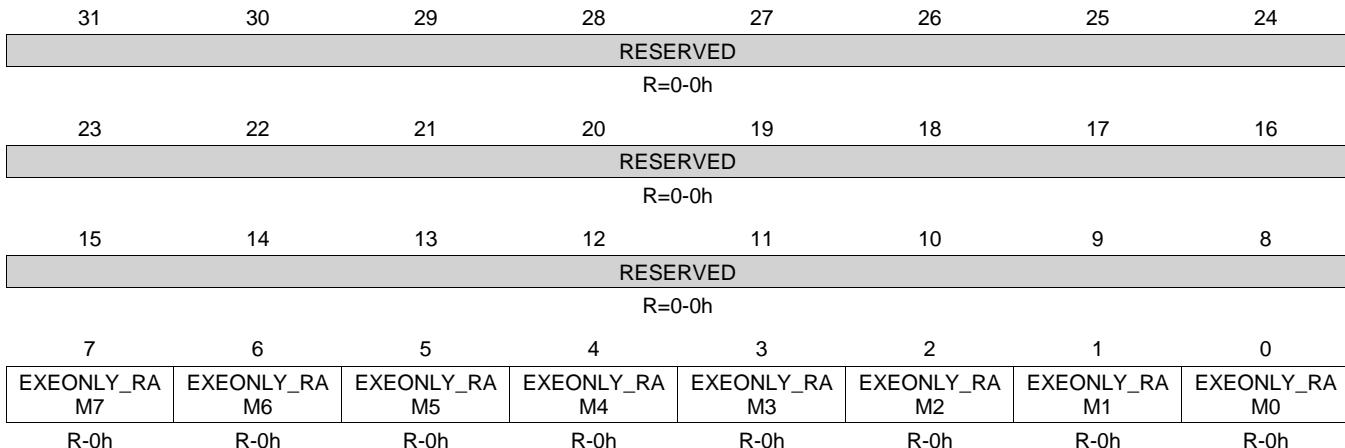
Table 1-232. Z2_EXEONLYSECTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EXEONLY_SECTB	R	0h	<p>Value in this field gets loaded from Z2_EXEONLYSECT[1:1] when a read is issued to Z2_EXEONLYSECT address location in OTP.</p> <p>0 : Execute-Only protection is enabled for Flash Sector B (only if it's allocated to Zone2)</p> <p>1 : Execute-Only protection is disabled for Flash Sector B (only if it's allocated to Zone2)</p>
0	EXEONLY_SECTA	R	0h	<p>Value in this field gets loaded from Z2_EXEONLYSECT[0:0] when a read is issued to Z2_EXEONLYSECT address location in OTP.</p> <p>0 : Execute-Only protection is enabled for Flash Sector A (only if it's allocated to Zone2)</p> <p>1 : Execute-Only protection is disabled for Flash Sector A (only if it's allocated to Zone2)</p>

1.14.15.13 Z2_EXEONLYRAMR Register (offset = 20h) [reset = 0h]

Z2_EXEONLYRAMR is shown in [Figure 1-229](#) and described in [Table 1-233](#).

Zone 2 RAM Execute_Only Block Register

Figure 1-229. Z2_EXEONLYRAMR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-233. Z2_EXEONLYRAMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	EXEONLY_RAM7	R	0h	Value in this field gets loaded from Z2_EXEONLYRAM[7:7] when a read is issued to Z2_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for D1 RAM (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for D1 RAM (only if it's allocated to Zone2)
6	EXEONLY_RAM6	R	0h	Value in this field gets loaded from Z2_EXEONLYRAM[6:6] when a read is issued to Z2_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for D0 RAM (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for D0 RAM (only if it's allocated to Zone2)
5	EXEONLY_RAM5	R	0h	Value in this field gets loaded from Z2_EXEONLYRAM[5:5] when a read is issued to Z2_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for LS5 RAM (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for LS5 RAM (only if it's allocated to Zone2)
4	EXEONLY_RAM4	R	0h	Value in this field gets loaded from Z2_EXEONLYRAM[4:4] when a read is issued to Z2_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for LS4 RAM (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for LS4 RAM (only if it's allocated to Zone2)
3	EXEONLY_RAM3	R	0h	Value in this field gets loaded from Z2_EXEONLYRAM[3:3] when a read is issued to Z2_EXEONLYRAM address location in OTP. 0 : Execute-Only protection is enabled for LS3 RAM (only if it's allocated to Zone2) 1 : Execute-Only protection is disabled for LS3 RAM (only if it's allocated to Zone2)

Table 1-233. Z2_EXEONLYRAMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EXEONLY_RAM2	R	0h	<p>Value in this field gets loaded from Z2_EXEONLYRAM[2:2] when a read is issued to Z2_EXEONLYRAM address location in OTP.</p> <p>0 : Execute-Only protection is enabled for LS2 RAM (only if it's allocated to Zone2)</p> <p>1 : Execute-Only protection is disabled for LS2 RAM (only if it's allocated to Zone2)</p>
1	EXEONLY_RAM1	R	0h	<p>Value in this field gets loaded from Z2_EXEONLYRAM[1:1] when a read is issued to Z2_EXEONLYRAM address location in OTP.</p> <p>0 : Execute-Only protection is enabled for LS1 RAM (only if it's allocated to Zone2)</p> <p>1 : Execute-Only protection is disabled for LS1 RAM (only if it's allocated to Zone2)</p>
0	EXEONLY_RAM0	R	0h	<p>Value in this field gets loaded from Z2_EXEONLYRAM[0:0] when a read is issued to Z2_EXEONLYRAM address location in OTP.</p> <p>0 : Execute-Only protection is enabled for LS0 RAM (only if it's allocated to Zone2)</p> <p>1 : Execute-Only protection is disabled for LS0 RAM (only if it's allocated to Zone2)</p>

1.14.16 DCSM_COMMON_REGS Registers

[Table 1-234](#) lists the memory-mapped registers for the DCSM_COMMON_REGS. All register offset addresses not listed in [Table 1-234](#) should be considered as reserved locations and the register contents should not be modified.

Table 1-234. DCSM_COMMON_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	FLSEM	Flash Wrapper Semaphore Register	Section 1.14.16.1	
2h	SECTSTAT	Sectors Status Register	Section 1.14.16.2	
4h	RAMSTAT	RAM Status Register	Section 1.14.16.3	

1.14.16.1 FLSEM Register (offset = 0h) [reset = 0h]

FLSEM is shown in [Figure 1-230](#) and described in [Table 1-235](#).

Flash Wrapper Semaphore Register

Figure 1-230. FLSEM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY								RESERVED							
R=0/W-0h								R-0h							
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-235. FLSEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	KEY	R=0/W	0h	Writing a value 0xA5 into this field will allow the writing of the SEM bits, else writes are ignored. Reads will return 0.
7-2	RESERVED	R	0h	Reserved
1-0	SEM	R/W	0h	00 : C28X Flash Wrapper registers can be written by code running from anywhere without any restriction. 01 : Flash Wrapper registers can be written by code running from Zone1 security zone. 10 : C28X Flash Wrapper registers can be written by code running from Zone2 security zone 11 : C28X Flash Wrapper registers can be written by code running from anywhere without any restriction Allowed State Transitions in this field. 00 TO 11 : Code running from anywhere. 11 TO 00 : Not allowed. 00/11 TO 01 : Code running from Zone1 only can perform this transition. 01 TO 00/11 : Code running from Zone1 only can perform this transition. 00/11 TO 10 : Code running from Zone2 only can perform this transition. 10 TO 00/11 : Code running from Zone2 can perform this transition

1.14.16.2 SECTSTAT Register (offset = 2h) [reset = 0h]

SECTSTAT is shown in [Figure 1-231](#) and described in [Table 1-236](#).

Sectors Status Register

Figure 1-231. SECTSTAT Register

31	30	29	28	27	26	25	24
RESERVED		STATUS_BANK2		STATUS_SECTN		STATUS_SECTM	
R-0h		R-0h		R-0h		R-0h	
23	22	21	20	19	18	17	16
STATUS_SECTL		STATUS_SECTK		STATUS_SECTJ		STATUS_SECTI	
R-0h		R-0h		R-0h		R-0h	
15	14	13	12	11	10	9	8
STATUS_SECTH		STATUS_SECTG		STATUS_SECTF		STATUS_SECTE	
R-0h		R-0h		R-0h		R-0h	
7	6	5	4	3	2	1	0
STATUS_SECTD		STATUS_SECTC		STATUS_SECTB		STATUS_SECTA	
R-0h		R-0h		R-0h		R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-236. SECTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	STATUS_BANK2	R	0h	Reflects the status of flash BANK2. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
27-26	STATUS_SECTN	R	0h	Reflects the status of flash sector N. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
25-24	STATUS_SECTM	R	0h	Reflects the status of flash sector M. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
23-22	STATUS_SECTL	R	0h	Reflects the status of flash sector L. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.

Table 1-236. SECTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	STATUS_SECTK	R	0h	Reflects the status of flash sector K. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
19-18	STATUS_SECTJ	R	0h	Reflects the status of flash sector J. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
17-16	STATUS_SECTI	R	0h	Reflects the status of flash sector I. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
15-14	STATUS_SECTH	R	0h	Reflects the status of flash sector H. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
13-12	STATUS_SECTG	R	0h	Reflects the status of flash sector G. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
11-10	STATUS_SECTF	R	0h	Reflects the status of flash sector F. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
9-8	STATUS_SECTE	R	0h	Reflects the status of flash sector E. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
7-6	STATUS_SECTD	R	0h	Reflects the status of flash sector D. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.

Table 1-236. SECTSTAT Register Field Descriptions (continued)

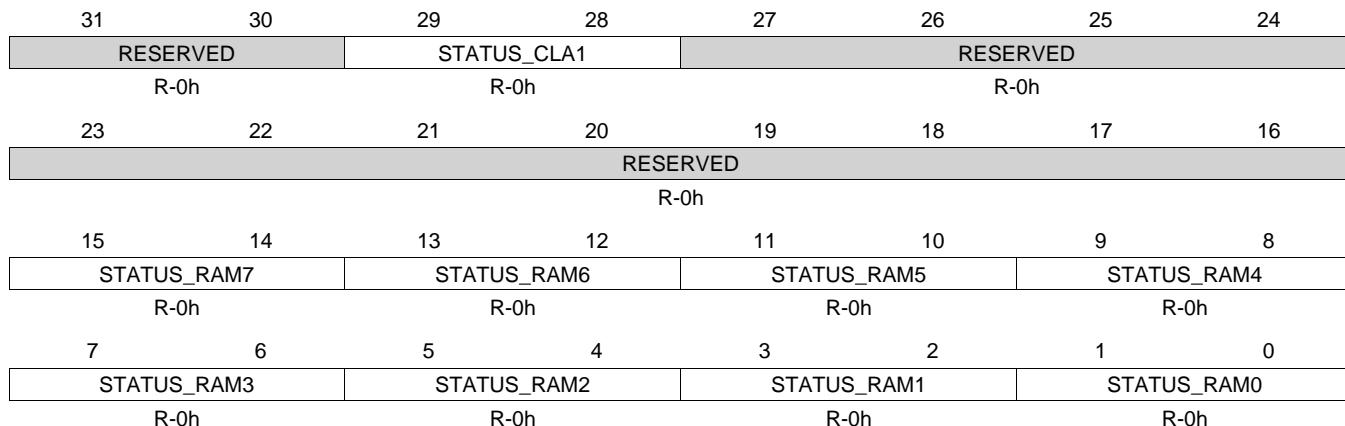
Bit	Field	Type	Reset	Description
5-4	STATUS_SECTC	R	0h	Reflects the status of flash sector C. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
3-2	STATUS_SECTB	R	0h	Reflects the status of flash sector B. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.
1-0	STATUS_SECTA	R	0h	Reflects the status of flash sector A. 00 : Sector is in-accessible 01 : Sector belongs to Zone1. 10 : Sector belongs to Zone2. 11: Sector is un-secure and code running in both zone have full access to it.

1.14.16.3 RAMSTAT Register (offset = 4h) [reset = 0h]

RAMSTAT is shown in [Figure 1-232](#) and described in [Table 1-237](#).

RAM Status Register

Figure 1-232. RAMSTAT Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-237. RAMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	STATUS_CLA1	R	0h	Reflects the status of CLA1. 00 : CLA is in-accessible 01 : CLA belongs to Zone1. 10 : CLA belongs to Zone2. 11: CLA is un-secure and code running in both zone have full access to it.
27-16	RESERVED	R	0h	Reserved
15-14	STATUS_RAM7	R	0h	Reflects the status of D1 RAM. 00 : RAM is in-accessible 01 : RAM belongs to Zone1. 10 : RAM belongs to Zone2. 11: RAM is un-secure and code running in both zone have full access to it.
13-12	STATUS_RAM6	R	0h	Reflects the status of D0 RAM. 00 : RAM is in-accessible 01 : RAM belongs to Zone1. 10 : RAM belongs to Zone2. 11: RAM is un-secure and code running in both zone have full access to it.
11-10	STATUS_RAM5	R	0h	Reflects the status of LS5 RAM. 00 : RAM is in-accessible 01 : RAM belongs to Zone1. 10 : RAM belongs to Zone2. 11: RAM is un-secure and code running in both zone have full access to it.

Table 1-237. RAMSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	STATUS_RAM4	R	0h	Reflects the status of LS4 RAM. 00 : RAM is in-accessible 01 : RAM belongs to Zone1. 10 : RAM belongs to Zone2. 11: RAM is un-secure and code running in both zone have full access to it.
7-6	STATUS_RAM3	R	0h	Reflects the status of LS3 RAM. 00 : RAM is in-accessible 01 : RAM belongs to Zone1. 10 : RAM belongs to Zone2. 11: RAM is un-secure and code running in both zone have full access to it.
5-4	STATUS_RAM2	R	0h	Reflects the status of LS2 RAM. 00 : RAM is in-accessible 01 : RAM belongs to Zone1. 10 : RAM belongs to Zone2. 11: RAM is un-secure and code running in both zone have full access to it.
3-2	STATUS_RAM1	R	0h	Reflects the status of LS1 RAM. 00 : RAM is in-accessible 01 : RAM belongs to Zone1. 10 : RAM belongs to Zone2. 11: RAM is un-secure and code running in both zone have full access to it.
1-0	STATUS_RAM0	R	0h	Reflects the status of LS0 RAM. 00 : RAM is in-accessible 01 : RAM belongs to Zone1. 10 : RAM belongs to Zone2. 11: RAM is un-secure and code running in both zone have full access to it.

1.14.17 MEM_CFG_REGS Registers

Table 1-238 lists the memory-mapped registers for the MEM_CFG_REGS. All register offset addresses not listed in **Table 1-238** should be considered as reserved locations and the register contents should not be modified.

Table 1-238. MEM_CFG_REGS REGISTERS

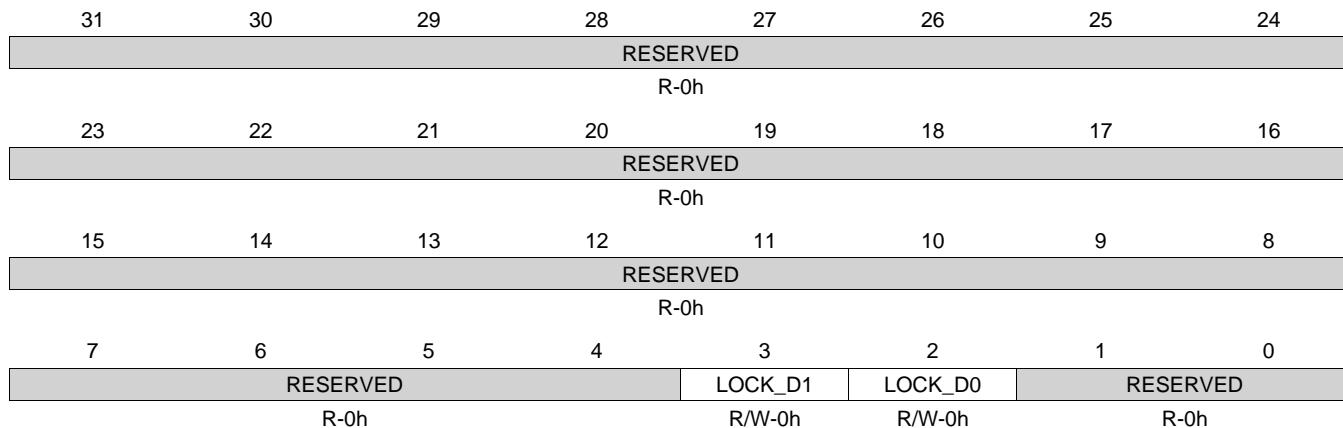
Offset	Acronym	Register Name	Section	Write Protection
0h	DxLOCK	Dedicated RAM Config Lock Register	Section 1.14.17.1	EALLOW
2h	DxCOMMIT	Dedicated RAM Config Lock Commit Register	Section 1.14.17.2	EALLOW
8h	DxACCPROT0	Dedicated RAM Config Register	Section 1.14.17.3	EALLOW
10h	DxTEST	Dedicated RAM TEST Register	Section 1.14.17.4	EALLOW
12h	DxINIT	Dedicated RAM Init Register	Section 1.14.17.5	EALLOW
14h	DxINITDONE	Dedicated RAM InitDone Status Register	Section 1.14.17.6	
20h	LSxLOCK	Local Shared RAM Config Lock Register	Section 1.14.17.7	EALLOW
22h	LSxCOMMIT	Local Shared RAM Config Lock Commit Register	Section 1.14.17.8	EALLOW
24h	LSxMSEL	Local Shared RAM Master Sel Register	Section 1.14.17.9	EALLOW
26h	LSxCLAPGM	Local Shared RAM Prog/Exe control Register	Section 1.14.17.10	EALLOW
28h	LSxACCPROT0	Local Shared RAM Config Register 0	Section 1.14.17.11	EALLOW
2Ah	LSxACCPROT1	Local Shared RAM Config Register 1	Section 1.14.17.12	EALLOW
30h	LSxTEST	Local Shared RAM TEST Register	Section 1.14.17.13	EALLOW
32h	LSxINIT	Local Shared RAM Init Register	Section 1.14.17.14	EALLOW
34h	LSxINITDONE	Local Shared RAM InitDone Status Register	Section 1.14.17.15	
40h	GSxLOCK	Global Shared RAM Config Lock Register	Section 1.14.17.16	EALLOW
42h	GSxCOMMIT	Global Shared RAM Config Lock Commit Register	Section 1.14.17.17	EALLOW
44h	GSxMSEL	Global Shared RAM Master Sel Register	Section 1.14.17.18	EALLOW
48h	GSxACCPROT0	Global Shared RAM Config Register 0	Section 1.14.17.19	EALLOW
4Ah	GSxACCPROT1	Global Shared RAM Config Register 1	Section 1.14.17.20	EALLOW
4Ch	GSxACCPROT2	Global Shared RAM Config Register 2	Section 1.14.17.21	EALLOW
4Eh	GSxACCPROT3	Global Shared RAM Config Register 3	Section 1.14.17.22	EALLOW
50h	GSxTEST	Global Shared RAM TEST Register	Section 1.14.17.23	EALLOW
52h	GSxINIT	Global Shared RAM Init Register	Section 1.14.17.24	EALLOW
54h	GSxINITDONE	Global Shared RAM InitDone Status Register	Section 1.14.17.25	

Table 1-238. MEM_CFG_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
70h	MSGxTEST	Message RAM TEST Register	Section 1.14.17.26	EALLOW
72h	MSGxINIT	Message RAM Init Register	Section 1.14.17.27	EALLOW
74h	MSGxINITDONE	Message RAM InitDone Status Register	Section 1.14.17.28	

1.14.17.1 DxLOCK Register (offset = 0h) [reset = 0h]DxLOCK is shown in [Figure 1-233](#) and described in [Table 1-239](#).

Dedicated RAM Config Lock Register

Figure 1-233. DxLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

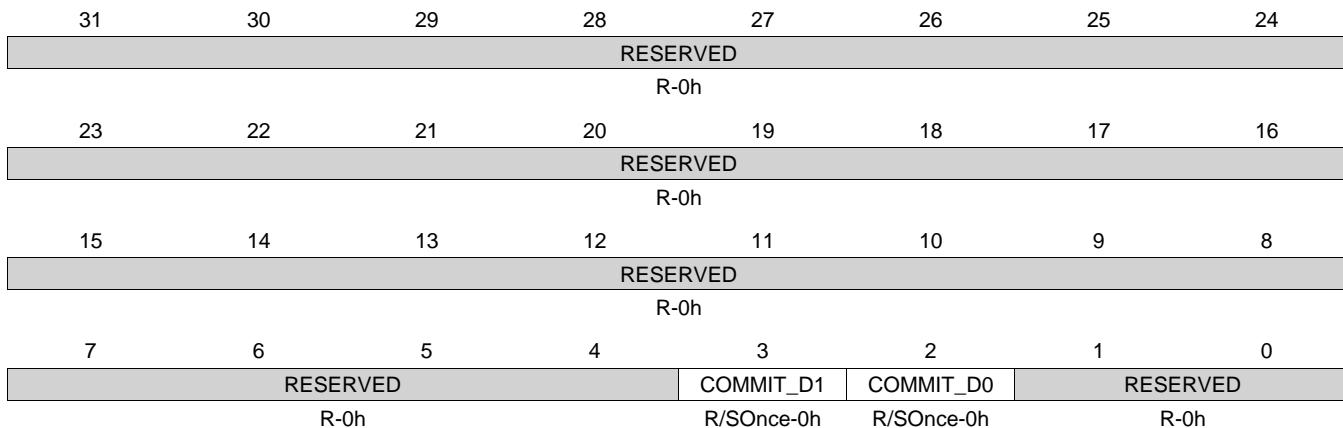
Table 1-239. DxLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	LOCK_D1	R/W	0h	Locks the write to access protection and master select fields for D1 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
2	LOCK_D0	R/W	0h	Locks the write to access protection and master select fields for D0 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
1-0	RESERVED	R	0h	Reserved

1.14.17.2 DxCOMMIT Register (offset = 2h) [reset = 0h]

DxCOMMIT is shown in [Figure 1-234](#) and described in [Table 1-240](#).

Dedicated RAM Config Lock Commit Register

Figure 1-234. DxCOMMIT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

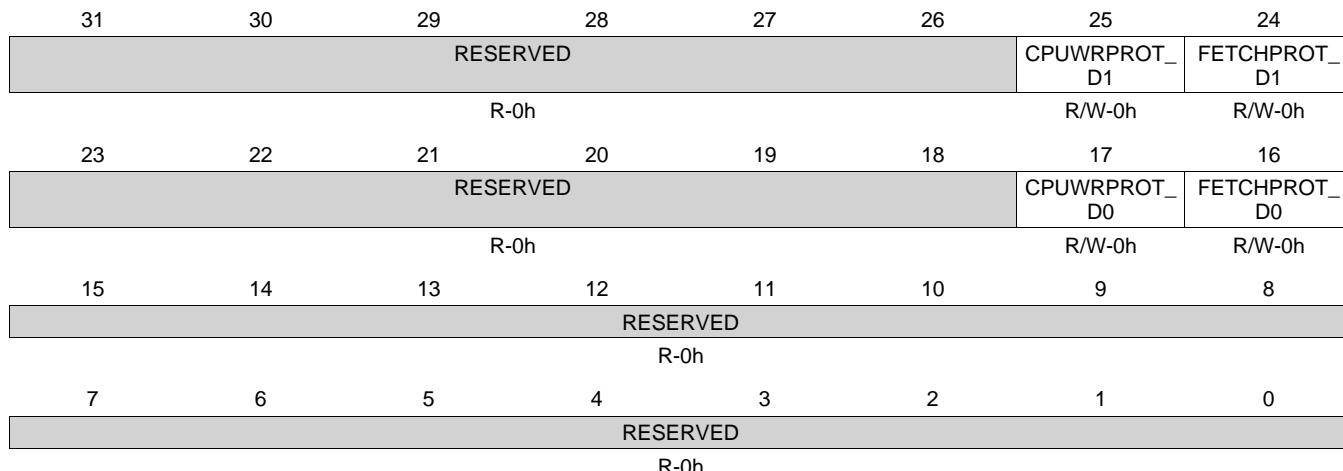
Table 1-240. DxCOMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	COMMIT_D1	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for D1 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in DxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
2	COMMIT_D0	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for D0 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in DxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
1-0	RESERVED	R	0h	Reserved

1.14.17.3 DxACCPROT0 Register (offset = 8h) [reset = 0h]

DxACCPROT0 is shown in [Figure 1-235](#) and described in [Table 1-241](#).

Dedicated RAM Config Register

Figure 1-235. DxACCPROT0 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

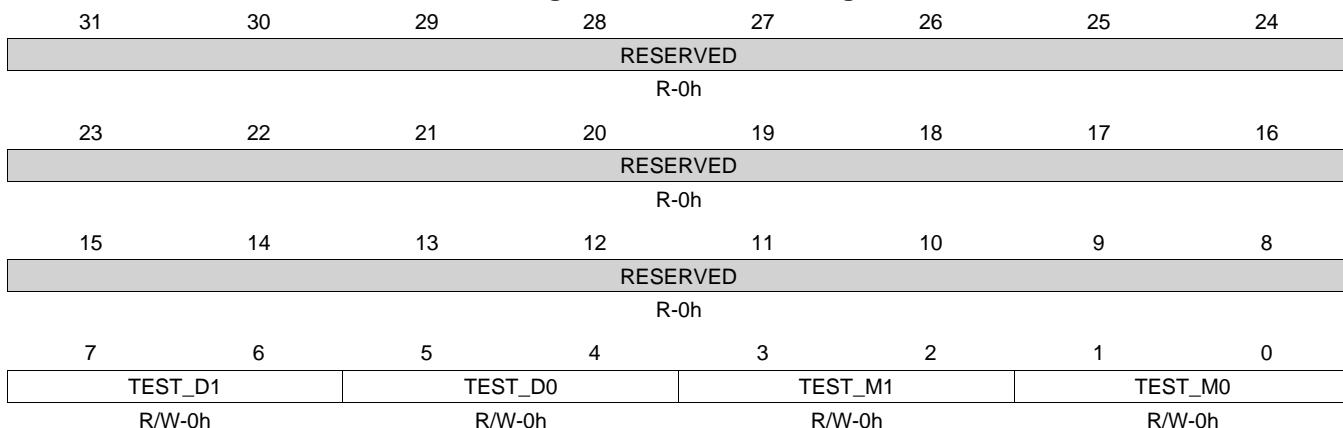
Table 1-241. DxACCPROT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	CPUWRPROT_D1	R/W	0h	CPU WR Protection For D1 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
24	FETCHPROT_D1	R/W	0h	Fetch Protection For D1 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
23-18	RESERVED	R	0h	Reserved
17	CPUWRPROT_D0	R/W	0h	CPU WR Protection For D0 RAM: 0: CPU Writes are allowed. 1: CPU Writes are block.
16	FETCHPROT_D0	R/W	0h	Fetch Protection For D0 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
15-0	RESERVED	R	0h	Reserved

1.14.17.4 DxTEST Register (offset = 10h) [reset = 0h]

DxTEST is shown in [Figure 1-236](#) and described in [Table 1-242](#).

Dedicated RAM TEST Register

Figure 1-236. DxTEST Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

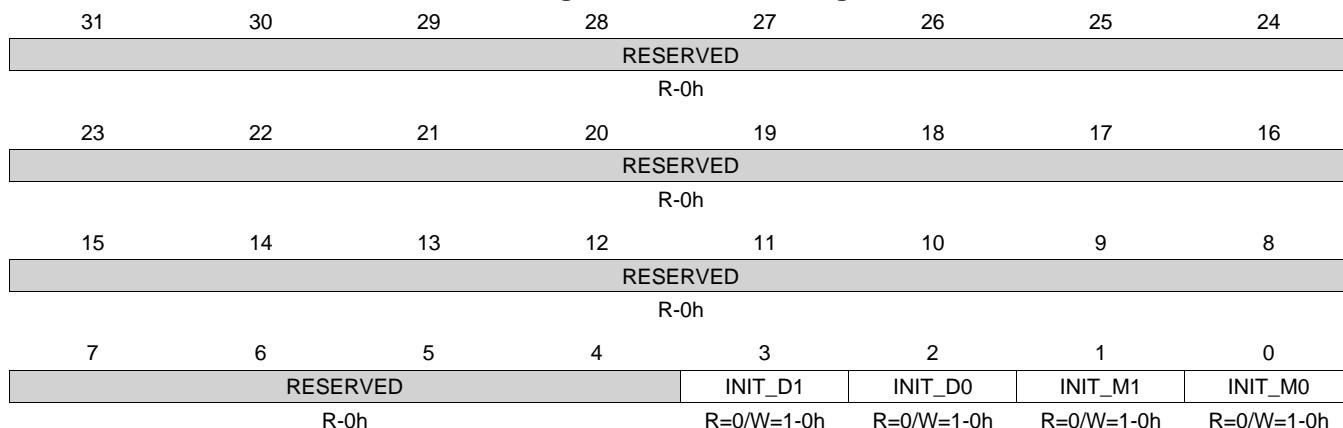
Table 1-242. DxTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	RESERVED	R	0h	Reserved
7-6	TEST_D1	R/W	0h	Selects the different modes for D1 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to ECC bits. 10: Writes are allowed to ECC bits only. No write to data bits. 11: Functional Mode.
5-4	TEST_D0	R/W	0h	Selects the different modes for D0 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to ECC bits. 10: Writes are allowed to ECC bits only. No write to data bits. 11: Functional Mode.
3-2	TEST_M1	R/W	0h	Selects the different modes for M1 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to ECC bits. 10: Writes are allowed to ECC bits only. No write to data bits. 11: Functional Mode.
1-0	TEST_M0	R/W	0h	Selects the different modes for M0 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to ECC bits. 10: Writes are allowed to ECC bits only. No write to data bits. 11: Functional Mode.

1.14.17.5 DxINIT Register (offset = 12h) [reset = 0h]

DxINIT is shown in [Figure 1-237](#) and described in [Table 1-243](#).

Dedicated RAM Init Register

Figure 1-237. DxINIT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

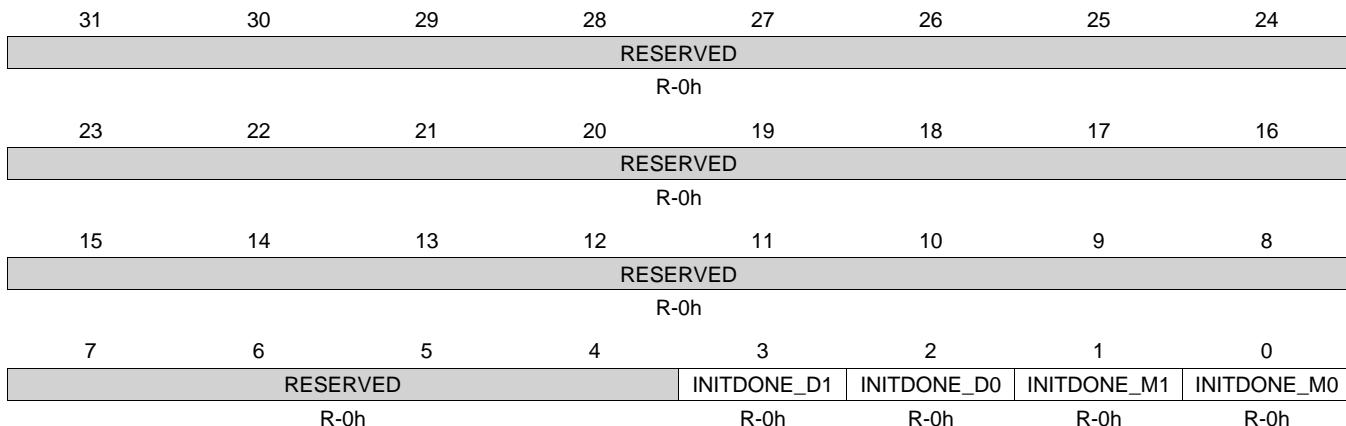
Table 1-243. DxINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	INIT_D1	R=0/W=1	0h	RAM Initialization control for D1 RAM: 0: None. 1: Start RAM Initialization.
2	INIT_D0	R=0/W=1	0h	RAM Initialization control for D0 RAM: 0: None. 1: Start RAM Initialization.
1	INIT_M1	R=0/W=1	0h	RAM Initialization control for M1 RAM: 0: None. 1: Start RAM Initialization.
0	INIT_M0	R=0/W=1	0h	RAM Initialization control for M0 RAM: 0: None. 1: Start RAM Initialization.

1.14.17.6 DxINITDONE Register (offset = 14h) [reset = 0h]

DxINITDONE is shown in [Figure 1-238](#) and described in [Table 1-244](#).

Dedicated RAM InitDone Status Register

Figure 1-238. DxINITDONE Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

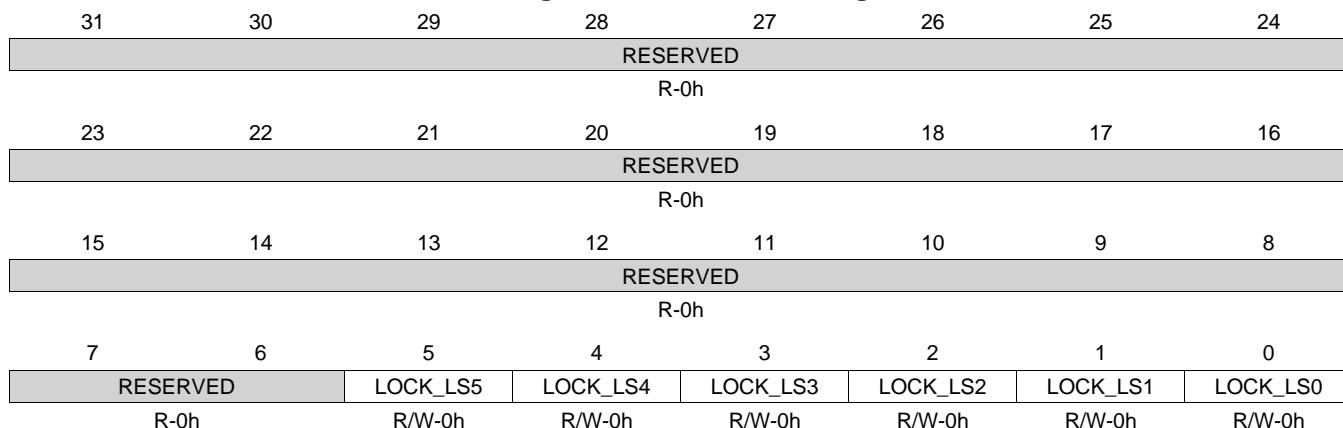
Table 1-244. DxINITDONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	INITDONE_D1	R	0h	RAM Initialization status for D1 RAM: 0: RAM Initialization has completed. 1: RAM Initialization has completed.
2	INITDONE_D0	R	0h	RAM Initialization status for D0 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
1	INITDONE_M1	R	0h	RAM Initialization status for M1 RAM: 0: RAM Initialization has completed. 1: RAM Initialization has completed.
0	INITDONE_M0	R	0h	RAM Initialization status for M0 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.

1.14.17.7 LSxLOCK Register (offset = 20h) [reset = 0h]

LSxLOCK is shown in [Figure 1-239](#) and described in [Table 1-245](#).

Local Shared RAM Config Lock Register

Figure 1-239. LSxLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

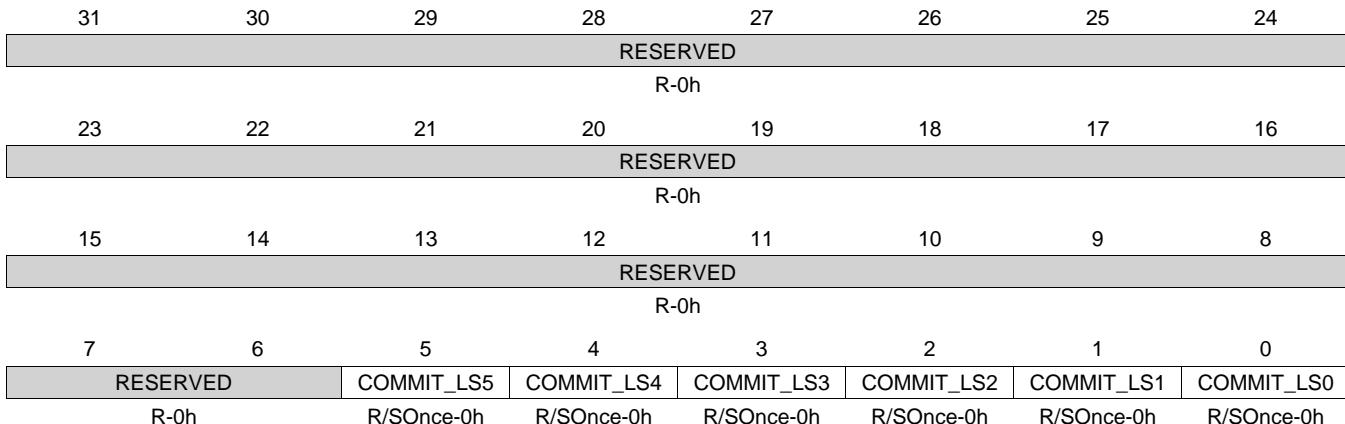
Table 1-245. LSxLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5	LOCK_LS5	R/W	0h	Locks the write to access protection and master select fields for LS5 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
4	LOCK_LS4	R/W	0h	Locks the write to access protection and master select fields for LS4 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
3	LOCK_LS3	R/W	0h	Locks the write to access protection and master select fields for LS3 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
2	LOCK_LS2	R/W	0h	Locks the write to access protection and master select fields for LS2 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
1	LOCK_LS1	R/W	0h	Locks the write to access protection and master select fields for LS1 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
0	LOCK_LS0	R/W	0h	Locks the write to access protection and master select fields for LS0 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.

1.14.17.8 LSxCOMMIT Register (offset = 22h) [reset = 0h]

LSxCOMMIT is shown in [Figure 1-240](#) and described in [Table 1-246](#).

Local Shared RAM Config Lock Commit Register

Figure 1-240. LSxCOMMIT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 1-246. LSxCOMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5	COMMIT_LS5	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for LS5 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in LSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
4	COMMIT_LS4	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for LS4 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in LSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
3	COMMIT_LS3	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for LS3 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in LSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
2	COMMIT_LS2	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for LS2 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in LSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
1	COMMIT_LS1	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for LS1 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in LSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.

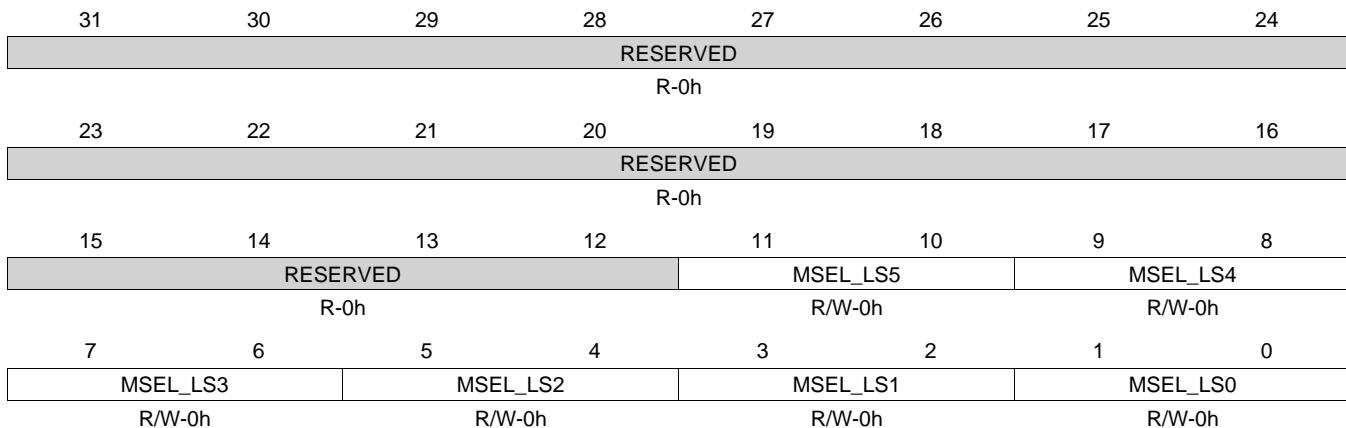
Table 1-246. LSxCOMMIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COMMIT_LS0	R/SOnce	0h	<p>Permanently Locks the write to access protection and master select fields for LS0 RAM:</p> <p>0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in LSxLOCK register.</p> <p>1: Write to ACCPROT and Mselect fields are permanently blocked.</p>

1.14.17.9 LSxMSEL Register (offset = 24h) [reset = 0h]

LSxMSEL is shown in [Figure 1-241](#) and described in [Table 1-247](#).

Local Shared RAM Master Sel Register

Figure 1-241. LSxMSEL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-247. LSxMSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	RESERVED	R	0h	Reserved
11-10	MSEL_LS5	R/W	0h	Master Select for LS5 RAM: 00: Memory is dedicated to CPU. 01: Memory is shared between CPU and CLA1. 10: Reserved. 11: Reserved.
9-8	MSEL_LS4	R/W	0h	Master Select for LS4 RAM: 00: Memory is dedicated to CPU. 01: Memory is shared between CPU and CLA1. 10: Reserved. 11: Reserved.
7-6	MSEL_LS3	R/W	0h	Master Select for LS3 RAM: 00: Memory is dedicated to CPU. 01: Memory is shared between CPU and CLA1. 10: Reserved. 11: Reserved.
5-4	MSEL_LS2	R/W	0h	Master Select for LS2 RAM: 00: Memory is dedicated to CPU. 01: Memory is shared between CPU and CLA1. 10: Reserved. 11: Reserved.
3-2	MSEL_LS1	R/W	0h	Master Select for LS1 RAM: 00: Memory is dedicated to CPU. 01: Memory is shared between CPU and CLA1. 10: Reserved. 11: Reserved.

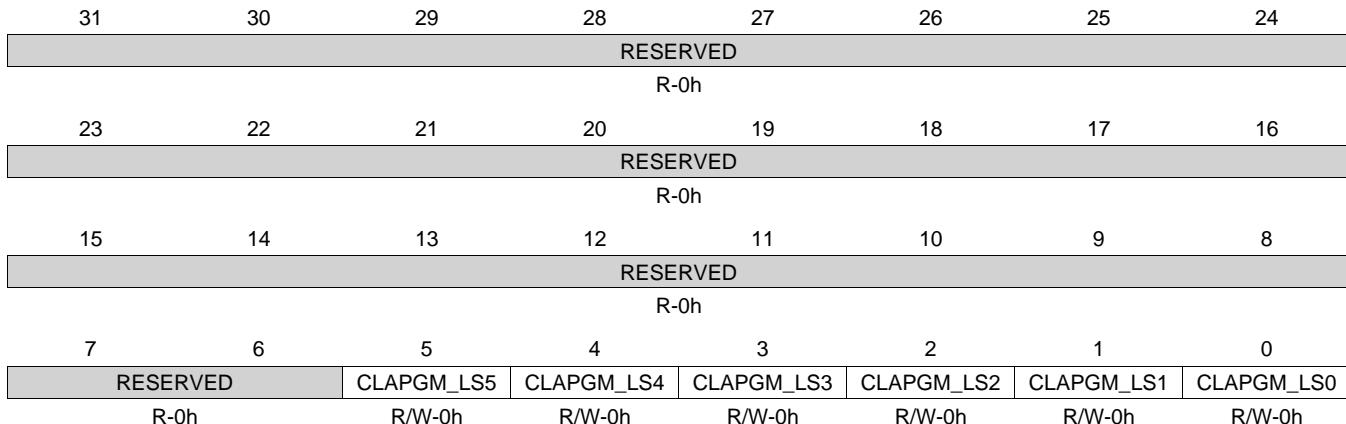
Table 1-247. LSxMSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	MSEL_LS0	R/W	0h	Master Select for LS0 RAM: 00: Memory is dedicated to CPU. 01: Memory is shared between CPU and CLA1. 10: Reserved. 11: Reserved.

1.14.17.10 LSxCLAPGM Register (offset = 26h) [reset = 0h]

LSxCLAPGM is shown in [Figure 1-242](#) and described in [Table 1-248](#).

Local Shared RAM Prog/Exe control Register

Figure 1-242. LSxCLAPGM Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-248. LSxCLAPGM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5	CLAPGM_LS5	R/W	0h	Selects LS5 RAM as program vs data memory for CLA: 0: CLA Data memory. 1: CLA Program memory.
4	CLAPGM_LS4	R/W	0h	Selects LS4 RAM as program vs data memory for CLA: 0: CLA Data memory. 1: CLA Program memory.
3	CLAPGM_LS3	R/W	0h	Selects LS3 RAM as program vs data memory for CLA: 0: CLA Data memory. 1: CLA Program memory.
2	CLAPGM_LS2	R/W	0h	Selects LS2 RAM as program vs data memory for CLA: 0: CLA Data memory. 1: CLA Program memory.
1	CLAPGM_LS1	R/W	0h	Selects LS1 RAM as program vs data memory for CLA: 0: CLA Data memory. 1: CLA Program memory.
0	CLAPGM_LS0	R/W	0h	Selects LS0 RAM as program vs data memory for CLA: 0: CLA Data memory. 1: CLA Program memory.

1.14.17.11 LSxACCPROT0 Register (offset = 28h) [reset = 0h]

LSxACCPROT0 is shown in [Figure 1-243](#) and described in [Table 1-249](#).

Local Shared RAM Config Register 0

Figure 1-243. LSxACCPROT0 Register

31	30	29	28	27	26	25	24
RESERVED					CPUWRPROT_ LS3	FETCHPROT_ LS3	
R-0h					R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
RESERVED					CPUWRPROT_ LS2	FETCHPROT_ LS2	
R-0h					R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
RESERVED					CPUWRPROT_ LS1	FETCHPROT_ LS1	
R-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RESERVED					CPUWRPROT_ LS0	FETCHPROT_ LS0	
R-0h					R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-249. LSxACCPROT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	CPUWRPROT_LS3	R/W	0h	CPU WR Protection For LS3 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
24	FETCHPROT_LS3	R/W	0h	Fetch Protection For LS3 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
23-18	RESERVED	R	0h	Reserved
17	CPUWRPROT_LS2	R/W	0h	CPU WR Protection For LS2 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
16	FETCHPROT_LS2	R/W	0h	Fetch Protection For LS2 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
15-10	RESERVED	R	0h	Reserved
9	CPUWRPROT_LS1	R/W	0h	CPU WR Protection For LS1 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
8	FETCHPROT_LS1	R/W	0h	Fetch Protection For LS1 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
7-2	RESERVED	R	0h	Reserved

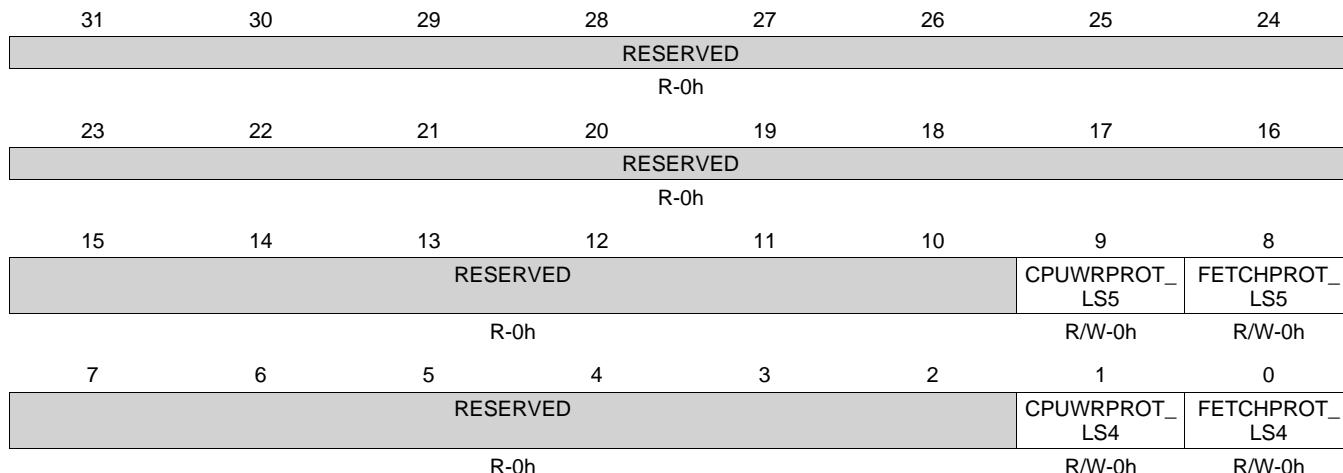
Table 1-249. LSxACCPROT0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CPUWRPROT_LS0	R/W	0h	CPU WR Protection For LS0 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
0	FETCHPROT_LS0	R/W	0h	Fetch Protection For LS0 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.

1.14.17.12 LSxACCPROT1 Register (offset = 2Ah) [reset = 0h]

LSxACCPROT1 is shown in [Figure 1-244](#) and described in [Table 1-250](#).

Local Shared RAM Config Register 1

Figure 1-244. LSxACCPROT1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

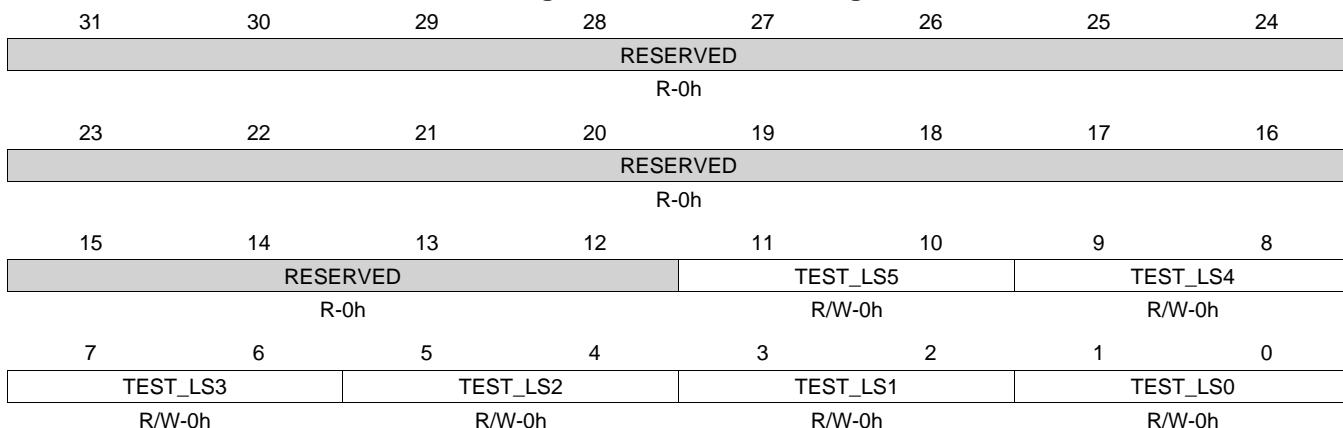
Table 1-250. LSxACCPROT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-10	RESERVED	R	0h	Reserved
9	CPUWRPROT_LS5	R/W	0h	CPU WR Protection For LS5 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
8	FETCHPROT_LS5	R/W	0h	Fetch Protection For LS5 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
7-2	RESERVED	R	0h	Reserved
1	CPUWRPROT_LS4	R/W	0h	CPU WR Protection For LS4 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
0	FETCHPROT_LS4	R/W	0h	Fetch Protection For LS4 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.

1.14.17.13 LSxTEST Register (offset = 30h) [reset = 0h]

LSxTEST is shown in [Figure 1-245](#) and described in [Table 1-251](#).

Local Shared RAM TEST Register

Figure 1-245. LSxTEST Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-251. LSxTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	RESERVED	R	0h	Reserved
11-10	TEST_LS5	R/W	0h	Selects the different modes for LS5 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
9-8	TEST_LS4	R/W	0h	Selects the different modes for LS4 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
7-6	TEST_LS3	R/W	0h	Selects the different modes for LS3 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
5-4	TEST_LS2	R/W	0h	Selects the different modes for LS2 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
3-2	TEST_LS1	R/W	0h	Selects the different modes for LS1 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.

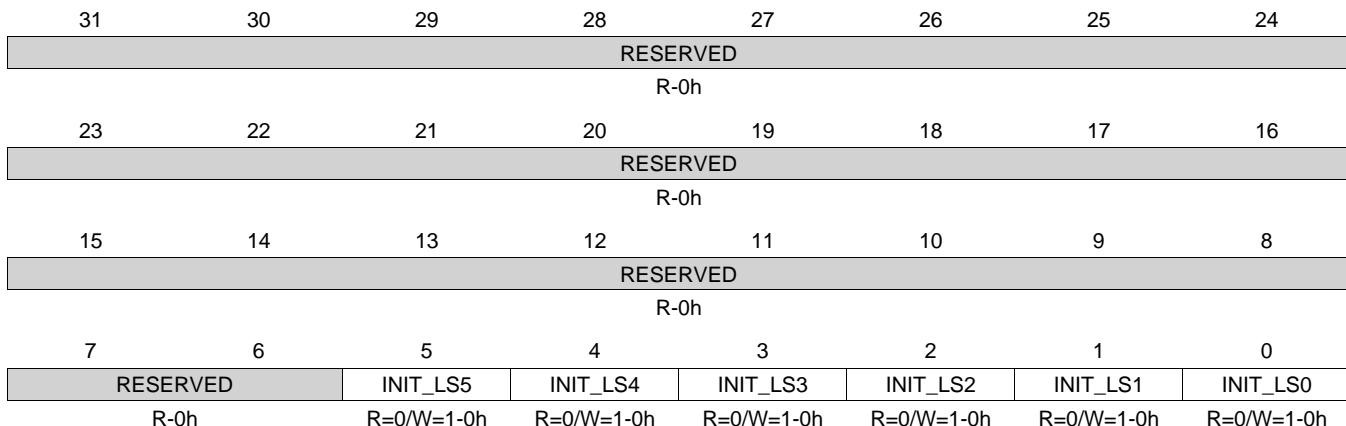
Table 1-251. LSxTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	TEST_LS0	R/W	0h	Selects the different modes for LS0 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.

1.14.17.14 LSxINIT Register (offset = 32h) [reset = 0h]

LSxINIT is shown in [Figure 1-246](#) and described in [Table 1-252](#).

Local Shared RAM Init Register

Figure 1-246. LSxINIT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

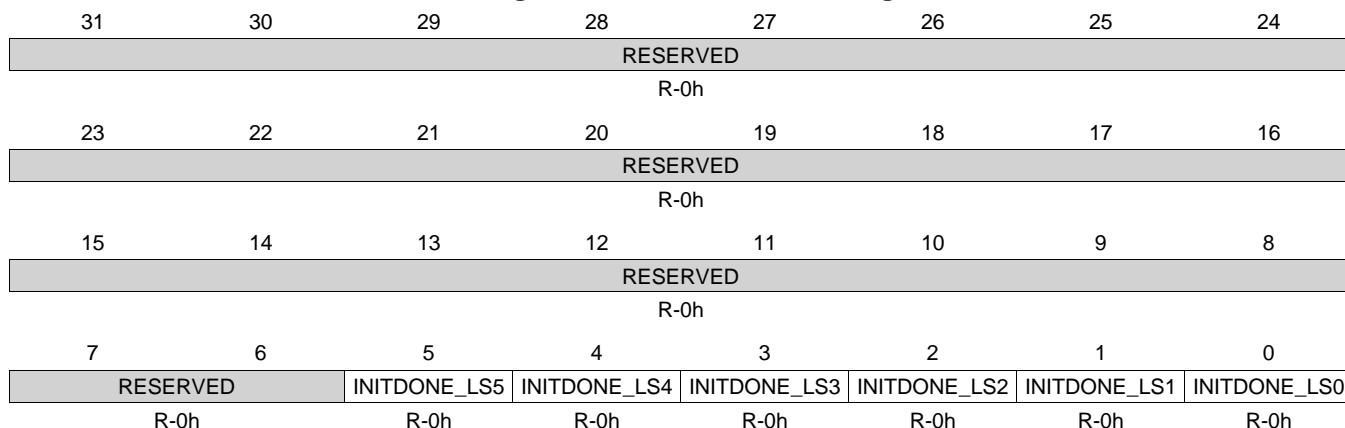
Table 1-252. LSxINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5	INIT_LS5	R=0/W=1	0h	RAM Initialization control for LS5 RAM: 0: None. 1: Start RAM Initialization.
4	INIT_LS4	R=0/W=1	0h	RAM Initialization control for LS4 RAM: 0: None. 1: Start RAM Initialization.
3	INIT_LS3	R=0/W=1	0h	RAM Initialization control for LS3 RAM: 0: None. 1: Start RAM Initialization.
2	INIT_LS2	R=0/W=1	0h	RAM Initialization control for LS2 RAM: 0: None. 1: Start RAM Initialization.
1	INIT_LS1	R=0/W=1	0h	RAM Initialization control for LS1 RAM: 0: None. 1: Start RAM Initialization.
0	INIT_LS0	R=0/W=1	0h	RAM Initialization control for LS0 RAM: 0: None. 1: Start RAM Initialization.

1.14.17.15 LSxINITDONE Register (offset = 34h) [reset = 0h]

LSxINITDONE is shown in [Figure 1-247](#) and described in [Table 1-253](#).

Local Shared RAM InitDone Status Register

Figure 1-247. LSxINITDONE Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-253. LSxINITDONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5	INITDONE_LS5	R	0h	RAM Initialization status for LS5 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
4	INITDONE_LS4	R	0h	RAM Initialization status for LS4 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
3	INITDONE_LS3	R	0h	RAM Initialization status for LS3 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
2	INITDONE_LS2	R	0h	RAM Initialization status for LS2 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
1	INITDONE_LS1	R	0h	RAM Initialization status for LS1 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
0	INITDONE_LS0	R	0h	RAM Initialization status for LS0 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.

1.14.17.16 GSxLOCK Register (offset = 40h) [reset = 0h]

GSxLOCK is shown in [Figure 1-248](#) and described in [Table 1-254](#).

Global Shared RAM Config Lock Register

Figure 1-248. GSxLOCK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
LOCK_GS15	LOCK_GS14	LOCK_GS13	LOCK_GS12	LOCK_GS11	LOCK_GS10	LOCK_GS9	LOCK_GS8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
LOCK_GS7	LOCK_GS6	LOCK_GS5	LOCK_GS4	LOCK_GS3	LOCK_GS2	LOCK_GS1	LOCK_GS0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-254. GSxLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	LOCK_GS15	R/W	0h	Locks the write to access protection and master select fields for GS15 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
14	LOCK_GS14	R/W	0h	Locks the write to access protection and master select fields for GS14 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
13	LOCK_GS13	R/W	0h	Locks the write to access protection and master select fields for GS13 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
12	LOCK_GS12	R/W	0h	Locks the write to access protection and master select fields for GS12 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
11	LOCK_GS11	R/W	0h	Locks the write to access protection and master select fields for GS11 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
10	LOCK_GS10	R/W	0h	Locks the write to access protection and master select fields for GS10 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
9	LOCK_GS9	R/W	0h	Locks the write to access protection and master select fields for GS9 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.

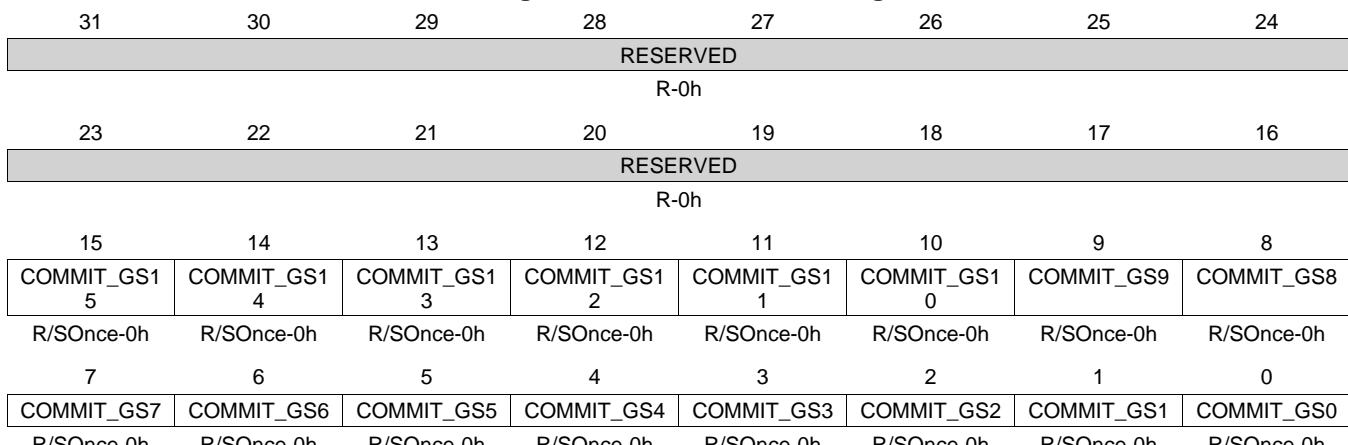
Table 1-254. GSxLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	LOCK_GS8	R/W	0h	Locks the write to access protection and master select fields for GS8 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
7	LOCK_GS7	R/W	0h	Locks the write to access protection and master select fields for GS7 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
6	LOCK_GS6	R/W	0h	Locks the write to access protection and master select fields for GS6 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
5	LOCK_GS5	R/W	0h	Locks the write to access protection and master select fields for GS5 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
4	LOCK_GS4	R/W	0h	Locks the write to access protection and master select fields for GS4 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
3	LOCK_GS3	R/W	0h	Locks the write to access protection and master select fields for GS3 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
2	LOCK_GS2	R/W	0h	Locks the write to access protection and master select fields for GS2 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
1	LOCK_GS1	R/W	0h	Locks the write to access protection and master select fields for GS1 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.
0	LOCK_GS0	R/W	0h	Locks the write to access protection and master select fields for GS0 RAM: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.

1.14.17.17 GSxCOMMIT Register (offset = 42h) [reset = 0h]

GSxCOMMIT is shown in [Figure 1-249](#) and described in [Table 1-255](#).

Global Shared RAM Config Lock Commit Register

Figure 1-249. GSxCOMMIT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-255. GSxCOMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	COMMIT_GS15	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS15 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
14	COMMIT_GS14	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS14 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
13	COMMIT_GS13	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS13 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
12	COMMIT_GS12	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS12 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
11	COMMIT_GS11	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS11 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.

Table 1-255. GSxCOMMIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	COMMIT_GS10	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS10 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
9	COMMIT_GS9	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS9 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
8	COMMIT_GS8	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS2 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
7	COMMIT_GS7	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS7 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
6	COMMIT_GS6	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS6 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
5	COMMIT_GS5	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS5 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
4	COMMIT_GS4	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS4 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
3	COMMIT_GS3	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS3 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
2	COMMIT_GS2	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS2 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.
1	COMMIT_GS1	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for GS1 RAM: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.

Table 1-255. GSxCOMMIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COMMIT_GS0	R/SOnce	0h	<p>Permanently Locks the write to access protection and master select fields for GS0 RAM:</p> <p>0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in GSxLOCK register.</p> <p>1: Write to ACCPROT and Mselect fields are permanently blocked.</p>

1.14.17.18 GSxMSEL Register (offset = 44h) [reset = 0h]

GSxMSEL is shown in [Figure 1-250](#) and described in [Table 1-256](#).

Global Shared RAM Master Sel Register

Figure 1-250. GSxMSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
MSEL_GS15	MSEL_GS14	MSEL_GS13	MSEL_GS12	MSEL_GS11	MSEL_GS10	MSEL_GS9	MSEL_GS8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
MSEL_GS7	MSEL_GS6	MSEL_GS5	MSEL_GS4	MSEL_GS3	MSEL_GS2	MSEL_GS1	MSEL_GS0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-256. GSxMSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	MSEL_GS15	R/W	0h	Master Select for GS15 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
14	MSEL_GS14	R/W	0h	Master Select for GS14 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
13	MSEL_GS13	R/W	0h	Master Select for GS13 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
12	MSEL_GS12	R/W	0h	Master Select for GS12 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
11	MSEL_GS11	R/W	0h	Master Select for GS11 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
10	MSEL_GS10	R/W	0h	Master Select for GS10 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
9	MSEL_GS9	R/W	0h	Master Select for GS9 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
8	MSEL_GS8	R/W	0h	Master Select for GS8 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.

Table 1-256. GSxMSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	MSEL_GS7	R/W	0h	Master Select for GS7 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
6	MSEL_GS6	R/W	0h	Master Select for GS6 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
5	MSEL_GS5	R/W	0h	Master Select for GS5 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
4	MSEL_GS4	R/W	0h	Master Select for GS4 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
3	MSEL_GS3	R/W	0h	Master Select for GS3 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
2	MSEL_GS2	R/W	0h	Master Select for GS2 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
1	MSEL_GS1	R/W	0h	Master Select for GS1 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.
0	MSEL_GS0	R/W	0h	Master Select for GS0 RAM: 0: CPU1 is master for this memory. 1: CPU2 is master for this memory.

1.14.17.19 GSxACCPROT0 Register (offset = 48h) [reset = 0h]

GSxACCPROT0 is shown in [Figure 1-251](#) and described in [Table 1-257](#).

Global Shared RAM Config Register 0

Figure 1-251. GSxACCPROT0 Register

31	30	29	28	27	26	25	24
RESERVED				DMAWRPROT_GS3	CPUWRPROT_GS3	FETCHPROT_GS3	
		R-0h				R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				DMAWRPROT_GS2	CPUWRPROT_GS2	FETCHPROT_GS2	
		R-0h				R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED				DMAWRPROT_GS1	CPUWRPROT_GS1	FETCHPROT_GS1	
		R-0h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				DMAWRPROT_GS0	CPUWRPROT_GS0	FETCHPROT_GS0	
		R-0h				R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-257. GSxACCPROT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	DMAWRPROT_GS3	R/W	0h	DMA WR Protection For GS3 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
25	CPUWRPROT_GS3	R/W	0h	CPU WR Protection For GS3 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
24	FETCHPROT_GS3	R/W	0h	Fetch Protection For GS3 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
23-19	RESERVED	R	0h	Reserved
18	DMAWRPROT_GS2	R/W	0h	DMA WR Protection For GS2 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
17	CPUWRPROT_GS2	R/W	0h	CPU WR Protection For GS2 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
16	FETCHPROT_GS2	R/W	0h	Fetch Protection For GS2 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
15-11	RESERVED	R	0h	Reserved
10	DMAWRPROT_GS1	R/W	0h	DMA WR Protection For GS1 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.

Table 1-257. GSxACCPROT0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CPUWRPROT_GS1	R/W	0h	CPU WR Protection For GS1 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
8	FETCHPROT_GS1	R/W	0h	Fetch Protection For GS1 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
7-3	RESERVED	R	0h	Reserved
2	DMAWRPROT_GS0	R/W	0h	DMA WR Protection For GS0 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
1	CPUWRPROT_GS0	R/W	0h	CPU WR Protection For GS0 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
0	FETCHPROT_GS0	R/W	0h	Fetch Protection For GS0 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.

1.14.17.20 GSxACCPROT1 Register (offset = 4Ah) [reset = 0h]

GSxACCPROT1 is shown in [Figure 1-252](#) and described in [Table 1-258](#).

Global Shared RAM Config Register 1

Figure 1-252. GSxACCPROT1 Register

31	30	29	28	27	26	25	24
RESERVED				DMAWRPROT_GS7	CPUWRPROT_GS7	FETCHPROT_GS7	
		R-0h				R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				DMAWRPROT_GS6	CPUWRPROT_GS6	FETCHPROT_GS6	
		R-0h				R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED				DMAWRPROT_GS5	CPUWRPROT_GS5	FETCHPROT_GS5	
		R-0h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				DMAWRPROT_GS4	CPUWRPROT_GS4	FETCHPROT_GS4	
		R-0h				R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-258. GSxACCPROT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	DMAWRPROT_GS7	R/W	0h	DMA WR Protection For GS7 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
25	CPUWRPROT_GS7	R/W	0h	CPU WR Protection For GS7 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
24	FETCHPROT_GS7	R/W	0h	Fetch Protection For GS7 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
23-19	RESERVED	R	0h	Reserved
18	DMAWRPROT_GS6	R/W	0h	DMA WR Protection For GS6 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
17	CPUWRPROT_GS6	R/W	0h	CPU WR Protection For GS6 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
16	FETCHPROT_GS6	R/W	0h	Fetch Protection For GS6 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
15-11	RESERVED	R	0h	Reserved
10	DMAWRPROT_GS5	R/W	0h	DMA WR Protection For GS5 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.

Table 1-258. GSxACCPROT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CPUWRPROT_GS5	R/W	0h	CPU WR Protection For GS5 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
8	FETCHPROT_GS5	R/W	0h	Fetch Protection For GS5 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
7-3	RESERVED	R	0h	Reserved
2	DMAWRPROT_GS4	R/W	0h	DMA WR Protection For GS4 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
1	CPUWRPROT_GS4	R/W	0h	CPU WR Protection For GS4 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
0	FETCHPROT_GS4	R/W	0h	Fetch Protection For GS4 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.

1.14.17.21 GSxACCPROT2 Register (offset = 4Ch) [reset = 0h]

GSxACCPROT2 is shown in [Figure 1-253](#) and described in [Table 1-259](#).

Global Shared RAM Config Register 2

Figure 1-253. GSxACCPROT2 Register

31	30	29	28	27	26	25	24
RESERVED				DMAWRPROT_GS11	CPUWRPROT_GS11	FETCHPROT_GS11	
			R-0h		R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				DMAWRPROT_GS10	CPUWRPROT_GS10	FETCHPROT_GS10	
			R-0h		R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED				DMAWRPROT_GS9	CPUWRPROT_GS9	FETCHPROT_GS9	
			R-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				DMAWRPROT_GS8	CPUWRPROT_GS8	FETCHPROT_GS8	
			R-0h		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-259. GSxACCPROT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	DMAWRPROT_GS11	R/W	0h	DMA WR Protection For GS11 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
25	CPUWRPROT_GS11	R/W	0h	CPU WR Protection For GS11 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
24	FETCHPROT_GS11	R/W	0h	Fetch Protection For GS11 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
23-19	RESERVED	R	0h	Reserved
18	DMAWRPROT_GS10	R/W	0h	DMA WR Protection For GS10 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
17	CPUWRPROT_GS10	R/W	0h	CPU WR Protection For GS10 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
16	FETCHPROT_GS10	R/W	0h	Fetch Protection For GS10 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
15-11	RESERVED	R	0h	Reserved
10	DMAWRPROT_GS9	R/W	0h	DMA WR Protection For GS9 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.

Table 1-259. GSxACCPROT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CPUWRPROT_GS9	R/W	0h	CPU WR Protection For GS9 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
8	FETCHPROT_GS9	R/W	0h	Fetch Protection For GS9 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
7-3	RESERVED	R	0h	Reserved
2	DMAWRPROT_GS8	R/W	0h	DMA WR Protection For GS8 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
1	CPUWRPROT_GS8	R/W	0h	CPU WR Protection For GS8 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
0	FETCHPROT_GS8	R/W	0h	Fetch Protection For GS8 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.

1.14.17.22 GSxACCPROT3 Register (offset = 4Eh) [reset = 0h]

GSxACCPROT3 is shown in [Figure 1-254](#) and described in [Table 1-260](#).

Global Shared RAM Config Register 3

Figure 1-254. GSxACCPROT3 Register

31	30	29	28	27	26	25	24
RESERVED				DMAWRPROT_GS15	CPUWRPROT_GS15	FETCHPROT_GS15	
			R-0h		R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				DMAWRPROT_GS14	CPUWRPROT_GS14	FETCHPROT_GS14	
			R-0h		R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED				DMAWRPROT_GS13	CPUWRPROT_GS13	FETCHPROT_GS13	
			R-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				DMAWRPROT_GS12	CPUWRPROT_GS12	FETCHPROT_GS12	
			R-0h		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-260. GSxACCPROT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	DMAWRPROT_GS15	R/W	0h	DMA WR Protection For GS15 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
25	CPUWRPROT_GS15	R/W	0h	CPU WR Protection For GS15 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
24	FETCHPROT_GS15	R/W	0h	Fetch Protection For GS15 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
23-19	RESERVED	R	0h	Reserved
18	DMAWRPROT_GS14	R/W	0h	DMA WR Protection For GS14 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
17	CPUWRPROT_GS14	R/W	0h	CPU WR Protection For GS14 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
16	FETCHPROT_GS14	R/W	0h	Fetch Protection For GS14 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
15-11	RESERVED	R	0h	Reserved
10	DMAWRPROT_GS13	R/W	0h	DMA WR Protection For GS13 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.

Table 1-260. GSxACCPROT3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CPUWRPROT_GS13	R/W	0h	CPU WR Protection For GS13 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
8	FETCHPROT_GS13	R/W	0h	Fetch Protection For GS13 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.
7-3	RESERVED	R	0h	Reserved
2	DMAWRPROT_GS12	R/W	0h	DMA WR Protection For GS12 RAM: 0: DMA Writes are allowed. 1: DMA Writes are blocked.
1	CPUWRPROT_GS12	R/W	0h	CPU WR Protection For GS12 RAM: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
0	FETCHPROT_GS12	R/W	0h	Fetch Protection For GS12 RAM: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.

1.14.17.23 GSxTEST Register (offset = 50h) [reset = 0h]

GSxTEST is shown in [Figure 1-255](#) and described in [Table 1-261](#).

Global Shared RAM TEST Register

Figure 1-255. GSxTEST Register

31	30	29	28	27	26	25	24
TEST_GS15		TEST_GS14		TEST_GS13		TEST_GS12	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
TEST_GS11		TEST_GS10		TEST_GS9		TEST_GS8	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
TEST_GS7		TEST_GS6		TEST_GS5		TEST_GS4	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
TEST_GS3		TEST_GS2		TEST_GS1		TEST_GS0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-261. GSxTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	TEST_GS15	R/W	0h	Selects the different modes for GS15 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
29-28	TEST_GS14	R/W	0h	Selects the different modes for GS14 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
27-26	TEST_GS13	R/W	0h	Selects the different modes for GS13 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
25-24	TEST_GS12	R/W	0h	Selects the different modes for GS12 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
23-22	TEST_GS11	R/W	0h	Selects the different modes for GS11 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.

Table 1-261. GSxTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	TEST_GS10	R/W	0h	Selects the different modes for GS10 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
19-18	TEST_GS9	R/W	0h	Selects the different modes for GS9 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
17-16	TEST_GS8	R/W	0h	Selects the different modes for GS8 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
15-14	TEST_GS7	R/W	0h	Selects the different modes for GS7 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
13-12	TEST_GS6	R/W	0h	Selects the different modes for GS6 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
11-10	TEST_GS5	R/W	0h	Selects the different modes for GS5 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
9-8	TEST_GS4	R/W	0h	Selects the different modes for GS4 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
7-6	TEST_GS3	R/W	0h	Selects the different modes for GS3 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
5-4	TEST_GS2	R/W	0h	Selects the different modes for GS2 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.

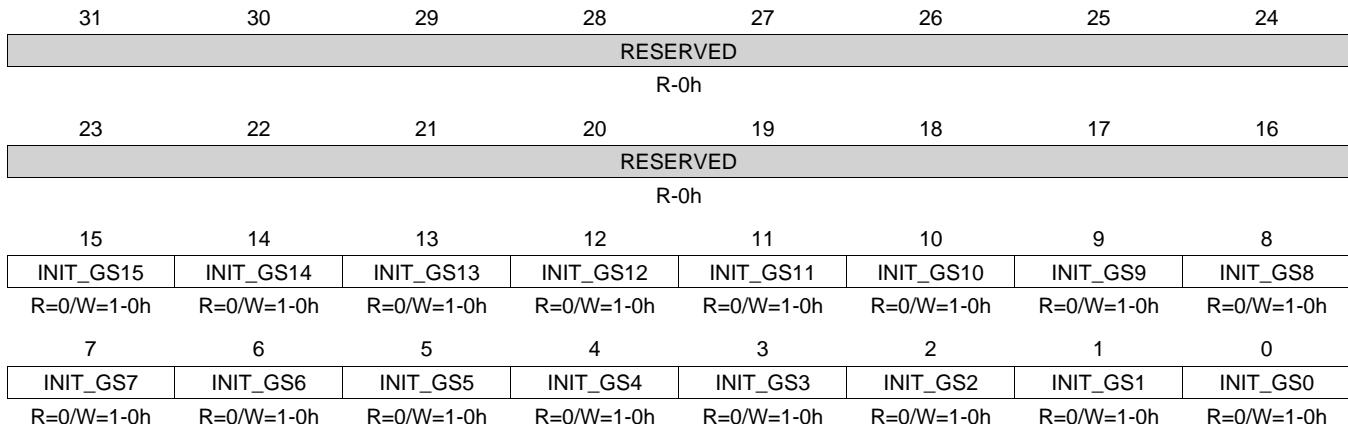
Table 1-261. GSxTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	TEST_GS1	R/W	0h	Selects the defferent modes for GS1 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
1-0	TEST_GS0	R/W	0h	Selects the defferent modes for GS0 RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.

1.14.17.24 GSxINIT Register (offset = 52h) [reset = 0h]

GSxINIT is shown in [Figure 1-256](#) and described in [Table 1-262](#).

Global Shared RAM Init Register

Figure 1-256. GSxINIT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-262. GSxINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	INIT_GS15	R=0/W=1	0h	RAM Initialization control for GS15 RAM: 0: None. 1: Start RAM Initialization.
14	INIT_GS14	R=0/W=1	0h	RAM Initialization control for GS14 RAM: 0: None. 1: Start RAM Initialization.
13	INIT_GS13	R=0/W=1	0h	RAM Initialization control for GS13 RAM: 0: None. 1: Start RAM Initialization.
12	INIT_GS12	R=0/W=1	0h	RAM Initialization control for GS12 RAM: 0: None. 1: Start RAM Initialization.
11	INIT_GS11	R=0/W=1	0h	RAM Initialization control for GS11 RAM: 0: None. 1: Start RAM Initialization.
10	INIT_GS10	R=0/W=1	0h	RAM Initialization control for GS10 RAM: 0: None. 1: Start RAM Initialization.
9	INIT_GS9	R=0/W=1	0h	RAM Initialization control for GS9 RAM: 0: None. 1: Start RAM Initialization.
8	INIT_GS8	R=0/W=1	0h	RAM Initialization control for GS8 RAM: 0: None. 1: Start RAM Initialization.

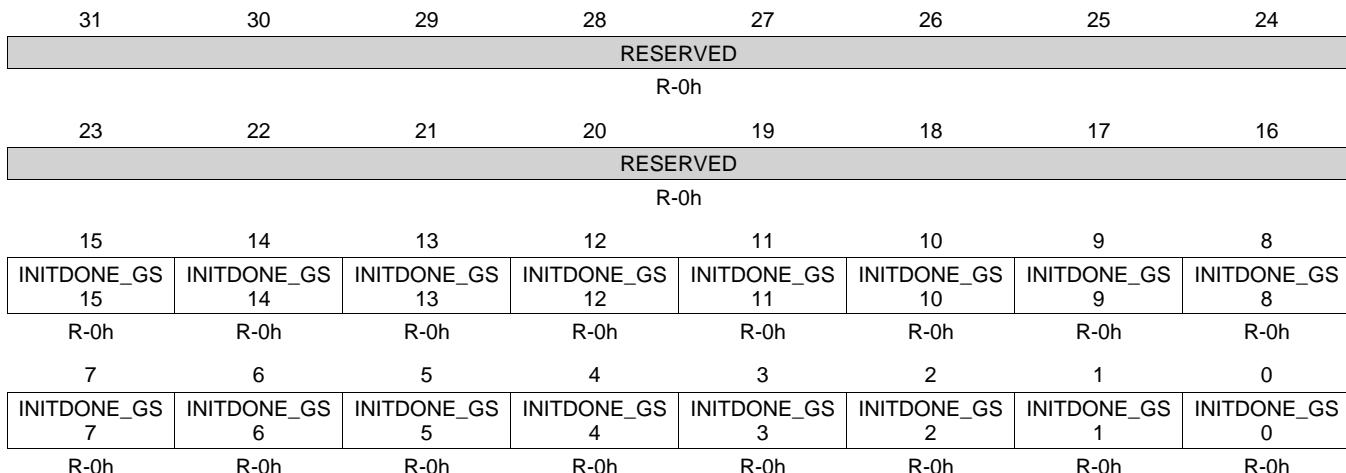
Table 1-262. GSxINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	INIT_GS7	R=0/W=1	0h	RAM Initialization control for GS7 RAM: 0: None. 1: Start RAM Initialization.
6	INIT_GS6	R=0/W=1	0h	RAM Initialization control for GS6 RAM: 0: None. 1: Start RAM Initialization.
5	INIT_GS5	R=0/W=1	0h	RAM Initialization control for GS5 RAM: 0: None. 1: Start RAM Initialization.
4	INIT_GS4	R=0/W=1	0h	RAM Initialization control for GS4 RAM: 0: None. 1: Start RAM Initialization.
3	INIT_GS3	R=0/W=1	0h	RAM Initialization control for GS3 RAM: 0: None. 1: Start RAM Initialization.
2	INIT_GS2	R=0/W=1	0h	RAM Initialization control for GS2 RAM: 0: None. 1: Start RAM Initialization.
1	INIT_GS1	R=0/W=1	0h	RAM Initialization control for GS1 RAM: 0: None. 1: Start RAM Initialization.
0	INIT_GS0	R=0/W=1	0h	RAM Initialization control for GS0 RAM: 0: None. 1: Start RAM Initialization.

1.14.17.25 GSxINITDONE Register (offset = 54h) [reset = 0h]

GSxINITDONE is shown in [Figure 1-257](#) and described in [Table 1-263](#).

Global Shared RAM InitDone Status Register

Figure 1-257. GSxINITDONE Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-263. GSxINITDONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	INITDONE_GS15	R	0h	RAM Initialization status for GS15 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
14	INITDONE_GS14	R	0h	RAM Initialization status for GS14 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
13	INITDONE_GS13	R	0h	RAM Initialization status for GS13 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
12	INITDONE_GS12	R	0h	RAM Initialization status for GS12 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
11	INITDONE_GS11	R	0h	RAM Initialization status for GS11 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
10	INITDONE_GS10	R	0h	RAM Initialization status for GS10 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
9	INITDONE_GS9	R	0h	RAM Initialization status for GS9 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
8	INITDONE_GS8	R	0h	RAM Initialization status for GS8 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.

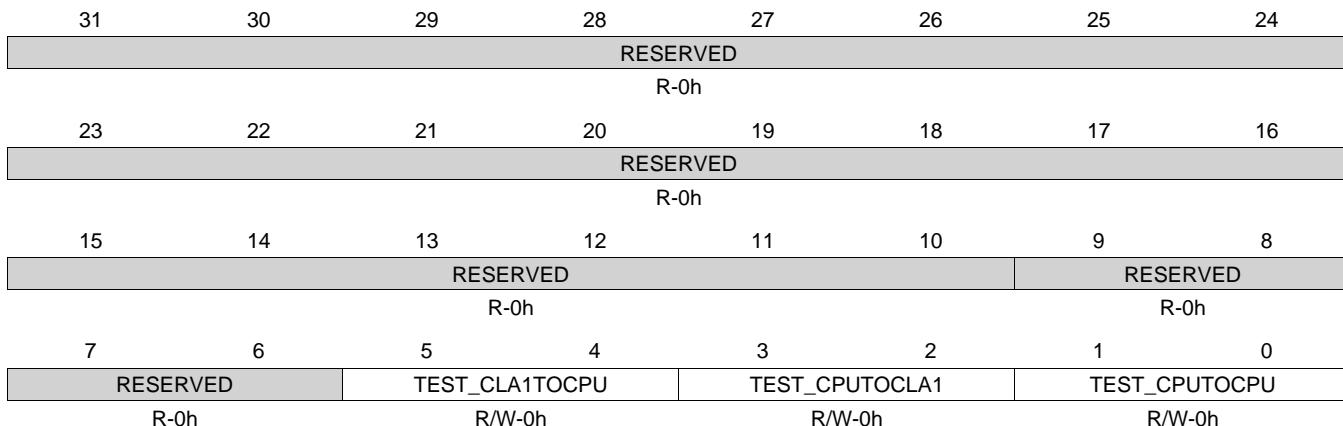
Table 1-263. GSxINITDONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	INITDONE_GS7	R	0h	RAM Initialization status for GS7 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
6	INITDONE_GS6	R	0h	RAM Initialization status for GS6 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
5	INITDONE_GS5	R	0h	RAM Initialization status for GS5 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
4	INITDONE_GS4	R	0h	RAM Initialization status for GS4 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
3	INITDONE_GS3	R	0h	RAM Initialization status for GS3 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
2	INITDONE_GS2	R	0h	RAM Initialization status for GS2 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
1	INITDONE_GS1	R	0h	RAM Initialization status for GS1 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
0	INITDONE_GS0	R	0h	RAM Initialization status for GS0 RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.

1.14.17.26 MSGxTEST Register (offset = 70h) [reset = 0h]

MSGxTEST is shown in [Figure 1-258](#) and described in [Table 1-264](#).

Message RAM TEST Register

Figure 1-258. MSGxTEST Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

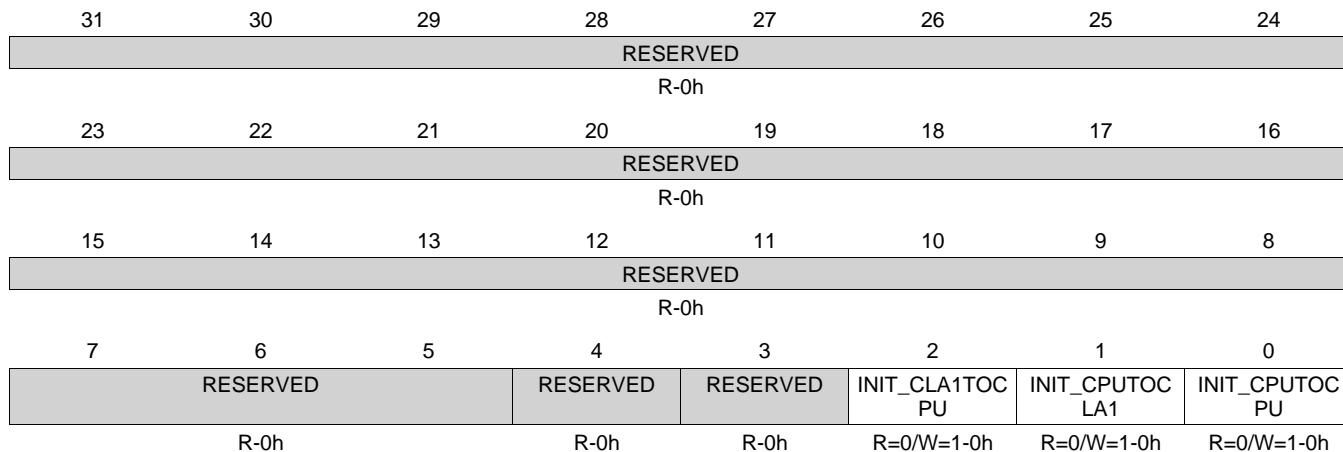
Table 1-264. MSGxTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-10	RESERVED	R	0h	Reserved
9-8	RESERVED	R	0h	Reserved
7-6	RESERVED	R	0h	Reserved
5-4	TEST_CLA1TOCPU	R/W	0h	Selects the different modes for CLA1TOCPU MSG RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
3-2	TEST_CPUOTOCLA1	R/W	0h	Selects the different modes for CPUOTOCLA1 MSG RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.
1-0	TEST_CPUOTOCPU	R/W	0h	Selects the different modes for CPUOTOCPU MSG RAM: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Functional Mode.

1.14.17.27 MSGxINIT Register (offset = 72h) [reset = 0h]

MSGxINIT is shown in [Figure 1-259](#) and described in [Table 1-265](#).

Message RAM Init Register

Figure 1-259. MSGxINIT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

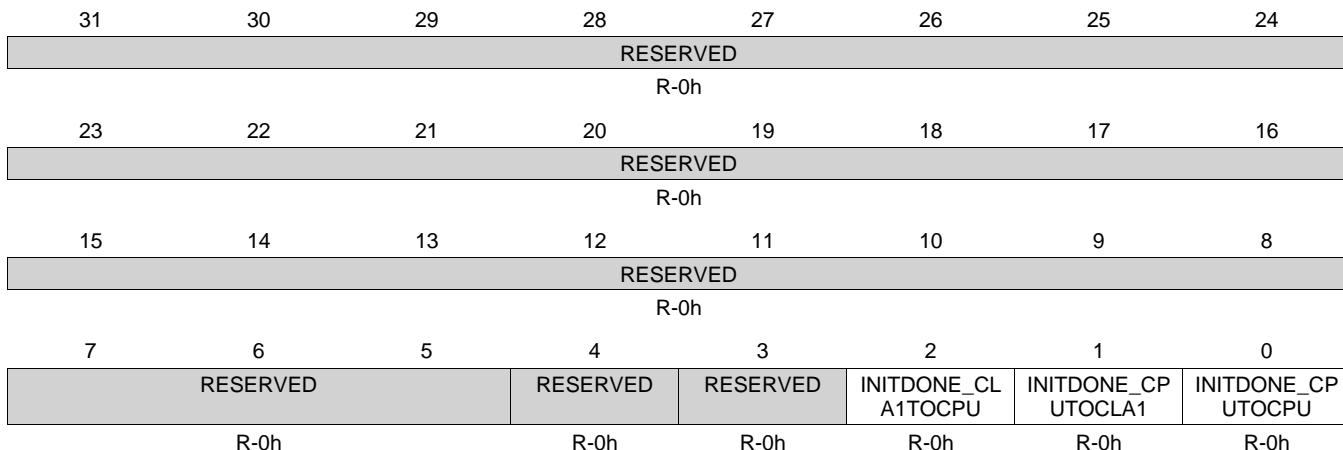
Table 1-265. MSGxINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	INIT_CLA1TOCPU	R=0/W=1	0h	RAM Initialization control for CLA1TOCPU MSG RAM: 0: None. 1: Start RAM Initialization.
1	INIT_CPUOTOC LA1	R=0/W=1	0h	RAM Initialization control for CPUOTOC LA1 MSG RAM: 0: None. 1: Start RAM Initialization.
0	INIT_CPUOTOC PU	R=0/W=1	0h	RAM Initialization control for CPUOTOC PU MSG RAM: 0: None. 1: Start RAM Initialization.

1.14.17.28 MSGxINITDONE Register (offset = 74h) [reset = 0h]

MSGxINITDONE is shown in [Figure 1-260](#) and described in [Table 1-266](#).

Message RAM InitDone Status Register

Figure 1-260. MSGxINITDONE Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-266. MSGxINITDONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	INITDONE_CLA1TOCPU	R	0h	RAM Initialization status for CLA1TOCPU MSG RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
1	INITDONE_CPUTOCLA1	R	0h	RAM Initialization status for CPUTOCLA1 MSG RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.
0	INITDONE_CPUTOCPU	R	0h	RAM Initialization status for CPUTOCPU MSG RAM: 0: RAM Initialization is not done. 1: RAM Initialization is done.

1.14.18 ACCESS_PROTECTION_REGS Registers

Table 1-267 lists the memory-mapped registers for the ACCESS_PROTECTION_REGS. All register offset addresses not listed in **Table 1-267** should be considered as reserved locations and the register contents should not be modified.

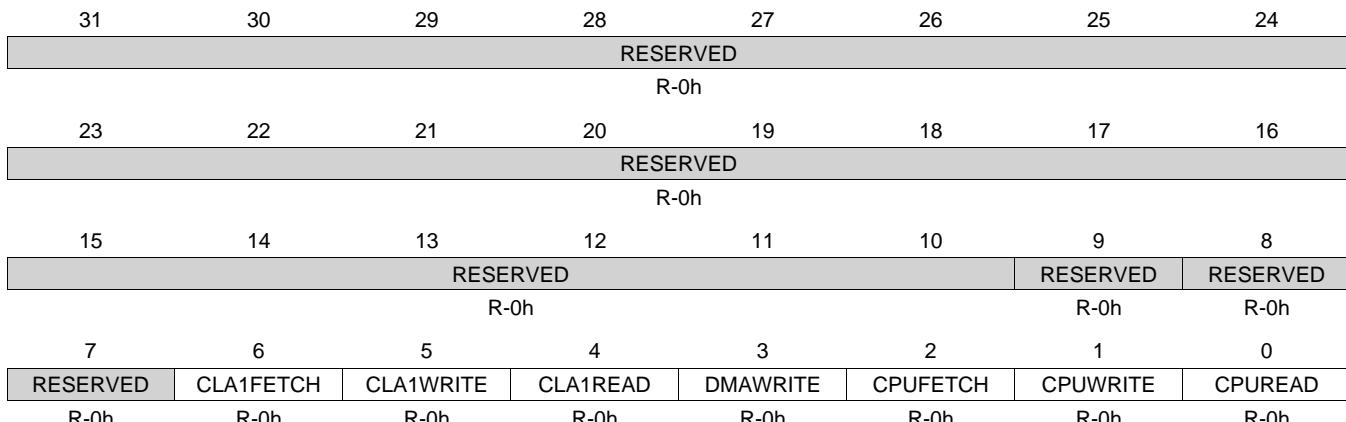
Table 1-267. ACCESS_PROTECTION_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	NMAVFLG	Non-Master Access Violation Flag Register	Section 1.14.18.1	
2h	NMAVSET	Non-Master Access Violation Flag Set Register	Section 1.14.18.2	EALLOW
4h	NMAVCLR	Non-Master Access Violation Flag Clear Register	Section 1.14.18.3	EALLOW
6h	NMAVINTEN	Non-Master Access Violation Interrupt Enable Register	Section 1.14.18.4	EALLOW
8h	NMCPURDAVADDR	Non-Master CPU Read Access Violation Address	Section 1.14.18.5	
Ah	NMCPUWRRAVADDR	Non-Master CPU Write Access Violation Address	Section 1.14.18.6	
Ch	NMCPUFAVADDR	Non-Master CPU Fetch Access Violation Address	Section 1.14.18.7	
Eh	NMDMAWRRAVADDR	Non-Master DMA Write Access Violation Address	Section 1.14.18.8	
10h	NMCLA1RDAVADDR	Non-Master CLA1 Read Access Violation Address	Section 1.14.18.9	
12h	NMCLA1WRRAVADDR	Non-Master CLA1 Write Access Violation Address	Section 1.14.18.10	
14h	NMCLA1FAVADDR	Non-Master CLA1 Fetch Access Violation Address	Section 1.14.18.11	
20h	MAVFLG	Master Access Violation Flag Register	Section 1.14.18.12	
22h	MAVSET	Master Access Violation Flag Set Register	Section 1.14.18.13	EALLOW
24h	MAVCLR	Master Access Violation Flag Clear Register	Section 1.14.18.14	EALLOW
26h	MAVINTEN	Master Access Violation Interrupt Enable Register	Section 1.14.18.15	EALLOW
28h	MCPUFAVADDR	Master CPU Fetch Access Violation Address	Section 1.14.18.16	
2Ah	MCPUWRRAVADDR	Master CPU Write Access Violation Address	Section 1.14.18.17	
2Ch	MDMAWRRAVADDR	Master DMA Write Access Violation Address	Section 1.14.18.18	

1.14.18.1 NMAVFLG Register (offset = 0h) [reset = 0h]

NMAVFLG is shown in [Figure 1-261](#) and described in [Table 1-268](#).

Non-Master Access Violation Flag Register

Figure 1-261. NMAVFLG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

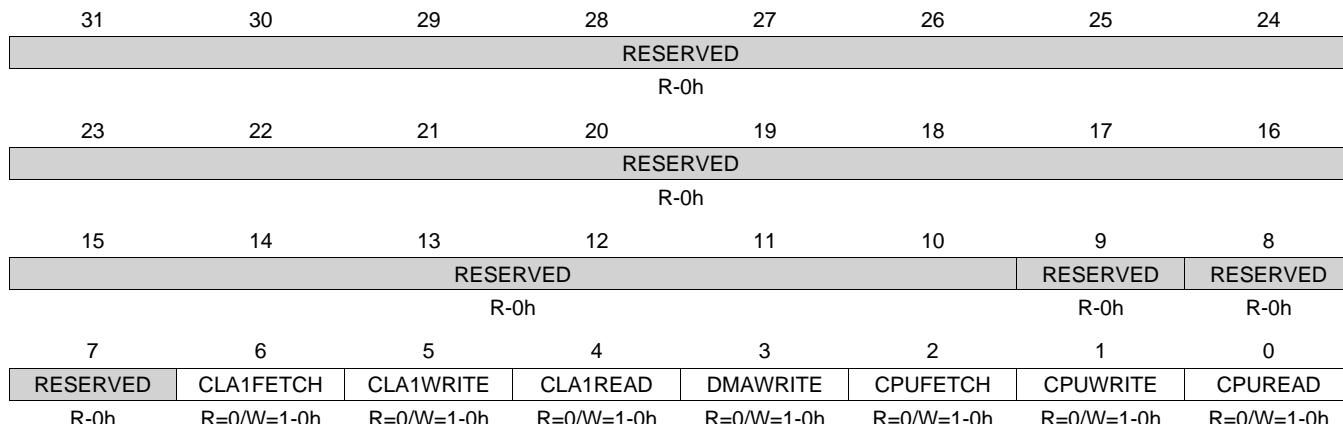
Table 1-268. NMAVFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	CLA1FETCH	R	0h	Non Master CLA1 Fetch Access Violation Flag: 0: No violation. 1: Access violation occurred.
5	CLA1WRITE	R	0h	Non Master CLA1 Write Access Violation Flag: 0: No violation. 1: Access violation occurred.
4	CLA1READ	R	0h	Non Master CLA1 Read Access Violation Flag: 0: No violation. 1: Access violation occurred.
3	DMAWRITE	R	0h	Non Master DMA Write Access Violation Flag: 0: No violation. 1: Access violation occurred.
2	CPUFETCH	R	0h	Non Master CPU Fetch Access Violation Flag: 0: No violation. 1: Access violation occurred.
1	CPUWRITE	R	0h	Non Master CPU Write Access Violation Flag: 0: No violation. 1: Access violation occurred.
0	CPUREAD	R	0h	Non Master CPU Read Access Violation Flag: 0: No violation. 1: Access violation occurred.

1.14.18.2 NMAVSET Register (offset = 2h) [reset = 0h]

NMAVSET is shown in [Figure 1-262](#) and described in [Table 1-269](#).

Non-Master Access Violation Flag Set Register

Figure 1-262. NMAVSET Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-269. NMAVSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	CLA1FETCH	R=0/W=1	0h	0: No action. 1: CLA1 Fetch Access Violation Flag in NMAVFLG register will be set and interrupt will be generated if enabled..
5	CLA1WRITE	R=0/W=1	0h	0: No action. 1: CLA1 Write Access Violation Flag in NMAVFLG register will be set and interrupt will be generated if enabled..
4	CLA1READ	R=0/W=1	0h	0: No action. 1: CLA1 Read Access Violation Flag in NMAVFLG register will be set and interrupt will be generated if enabled..
3	DMAWRITE	R=0/W=1	0h	0: No action. 1: DMA Write Access Violation Flag in NMAVFLG register will be set and interrupt will be generated if enabled..
2	CPUFETCH	R=0/W=1	0h	0: No action. 1: CPU Fetch Access Violation Flag in NMAVFLG register will be set and interrupt will be generated if enabled..
1	CPUWRITE	R=0/W=1	0h	0: No action. 1: CPU Write Access Violation Flag in NMAVFLG register will be set and interrupt will be generated if enabled..
0	CPUREAD	R=0/W=1	0h	0: No action. 1: CPU Read Access Violation Flag in NMAVFLG register will be set and interrupt will be generated if enabled..

1.14.18.3 NMAVCLR Register (offset = 4h) [reset = 0h]

NMAVCLR is shown in [Figure 1-263](#) and described in [Table 1-270](#).

Non-Master Access Violation Flag Clear Register

Figure 1-263. NMAVCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						RESERVED	RESERVED
R-0h						R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	CLA1FETCH	CLA1WRITE	CLA1READ	DMAWRITE	CPUFETCH	CPUWRITE	CPUREAD
R-0h	R=0/W=1-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

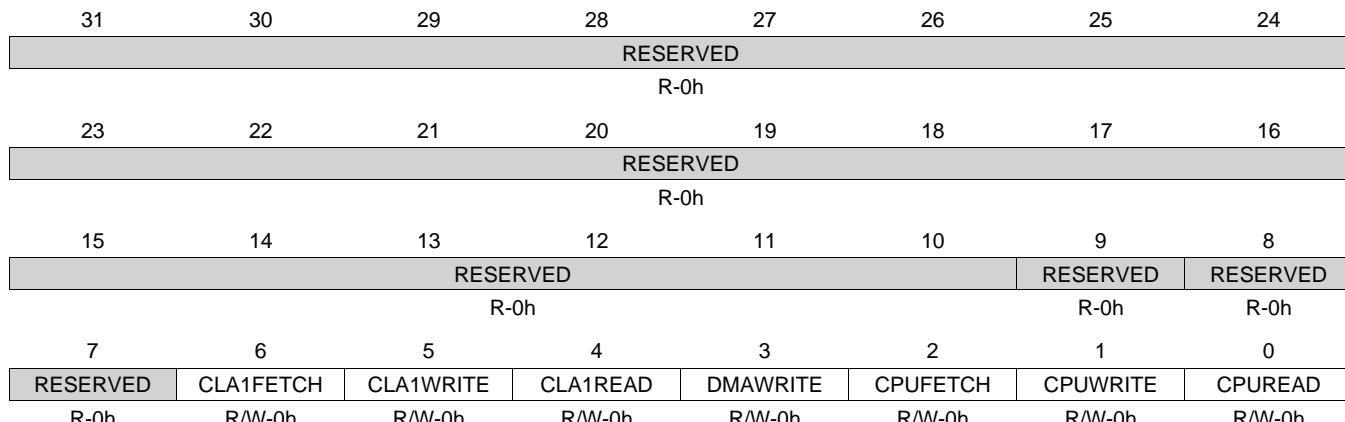
Table 1-270. NMAVCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	CLA1FETCH	R=0/W=1	0h	0: No action. 1: CLA1 Fetch Access Violation Flag in NMAVFLG register will be cleared.
5	CLA1WRITE	R=0/W=1	0h	0: No action. 1: CLA1 Write Access Violation Flag in NMAVFLG register will be cleared.
4	CLA1READ	R=0/W=1	0h	0: No action. 1: CLA1 Read Access Violation Flag in NMAVFLG register will be cleared.
3	DMAWRITE	R=0/W=1	0h	0: No action. 1: DMA Write Access Violation Flag in NMAVFLG register will be cleared.
2	CPUFETCH	R=0/W=1	0h	0: No action. 1: CPU Fetch Access Violation Flag in NMAVFLG register will be cleared.
1	CPUWRITE	R=0/W=1	0h	0: No action. 1: CPU Write Access Violation Flag in NMAVFLG register will be cleared.
0	CPUREAD	R=0/W=1	0h	0: No action. 1: CPU Read Access Violation Flag in NMAVFLG register will be cleared.

1.14.18.4 NMAVINTEN Register (offset = 6h) [reset = 0h]

NMAVINTEN is shown in [Figure 1-264](#) and described in [Table 1-271](#).

Non-Master Access Violation Interrupt Enable Register

Figure 1-264. NMAVINTEN Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-271. NMAVINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	CLA1FETCH	R/W	0h	0: CLA1 Non Master Fetch Access Violation Interrupt is disabled. 1: CLA1 Non Master Fetch Access Violation Interrupt is enabled.
5	CLA1WRITE	R/W	0h	0: CLA1 Non Master Write Access Violation Interrupt is disabled. 1: CLA1 Non Master Write Access Violation Interrupt is enabled.
4	CLA1READ	R/W	0h	0: CLA1 Non Master Read Access Violation Interrupt is disabled. 1: CLA1 Non Master Read Access Violation Interrupt is enabled.
3	DMAWRITE	R/W	0h	0: DMA Non Master Write Access Violation Interrupt is disabled. 1: DMA Non Master Write Access Violation Interrupt is enabled.
2	CPUFETCH	R/W	0h	0: CPU Non Master Fetch Access Violation Interrupt is disabled. 1: CPU Non Master Fetch Access Violation Interrupt is enabled.
1	CPUWRITE	R/W	0h	0: CPU Non Master Write Access Violation Interrupt is disabled. 1: CPU Non Master Write Access Violation Interrupt is enabled.
0	CPUREAD	R/W	0h	0: CPU Non Master Read Access Violation Interrupt is disabled. 1: CPU Non Master Read Access Violation Interrupt is enabled.

1.14.18.5 NMCPURDAVADDR Register (offset = 8h) [reset = 0h]

NMCPURDAVADDR is shown in [Figure 1-265](#) and described in [Table 1-272](#).

Non-Master CPU Read Access Violation Address

Figure 1-265. NMCPURDAVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NMCPURDAVADDR																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-272. NMCPURDAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NMCPURDAVADDR	R	0h	This register captures the address location for which non master CPU read access violation occurred.

1.14.18.6 NMCPUWRAVADDR Register (offset = Ah) [reset = 0h]NMCPUWRAVADDR is shown in [Figure 1-266](#) and described in [Table 1-273](#).

Non-Master CPU Write Access Violation Address

Figure 1-266. NMCPUWRAVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NMCPUWRAVADDR																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-273. NMCPUWRAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NMCPUWRAVADDR	R	0h	This register captures the address location for which non master CPU write access violation occurred.

1.14.18.7 NMCPUFAVADDR Register (offset = Ch) [reset = 0h]

NMCPUFAVADDR is shown in [Figure 1-267](#) and described in [Table 1-274](#).

Non-Master CPU Fetch Access Violation Address

Figure 1-267. NMCPUFAVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NMCPUFAVADDR																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-274. NMCPUFAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NMCPUFAVADDR	R	0h	This register captures the address location for which non master CPU fetch access violation occurred.

1.14.18.8 NMDMAWRAVADDR Register (offset = Eh) [reset = 0h]NMDMAWRAVADDR is shown in [Figure 1-268](#) and described in [Table 1-275](#).

Non-Master DMA Write Access Violation Address

Figure 1-268. NMDMAWRAVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NMDMAWRAVADDR																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

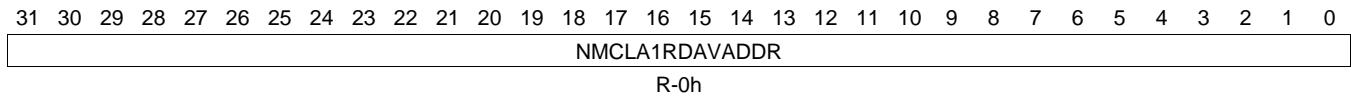
Table 1-275. NMDMAWRAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NMDMAWRAVADDR	R	0h	This register captures the address location for which non master DMA write access violation occurred.

1.14.18.9 NMCLA1RDAVADDR Register (offset = 10h) [reset = 0h]

NMCLA1RDAVADDR is shown in [Figure 1-269](#) and described in [Table 1-276](#).

Non-Master CLA1 Read Access Violation Address

Figure 1-269. NMCLA1RDAVADDR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-276. NMCLA1RDAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NMCLA1RDAVADDR	R	0h	This register captures the address location for which non master CLA1 read access violation occurred.

1.14.18.10 NMCLA1WRAVADDR Register (offset = 12h) [reset = 0h]NMCLA1WRAVADDR is shown in [Figure 1-270](#) and described in [Table 1-277](#).

Non-Master CLA1 Write Access Violation Address

Figure 1-270. NMCLA1WRAVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NMCLA1WRAVADDR																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-277. NMCLA1WRAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NMCLA1WRAVADDR	R	0h	This register captures the address location for which non master CLA1 write access violation occurred.

1.14.18.11 NMCLA1FAVADDR Register (offset = 14h) [reset = 0h]

NMCLA1FAVADDR is shown in [Figure 1-271](#) and described in [Table 1-278](#).

Non-Master CLA1 Fetch Access Violation Address

Figure 1-271. NMCLA1FAVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NMCLA1FAVADDR																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

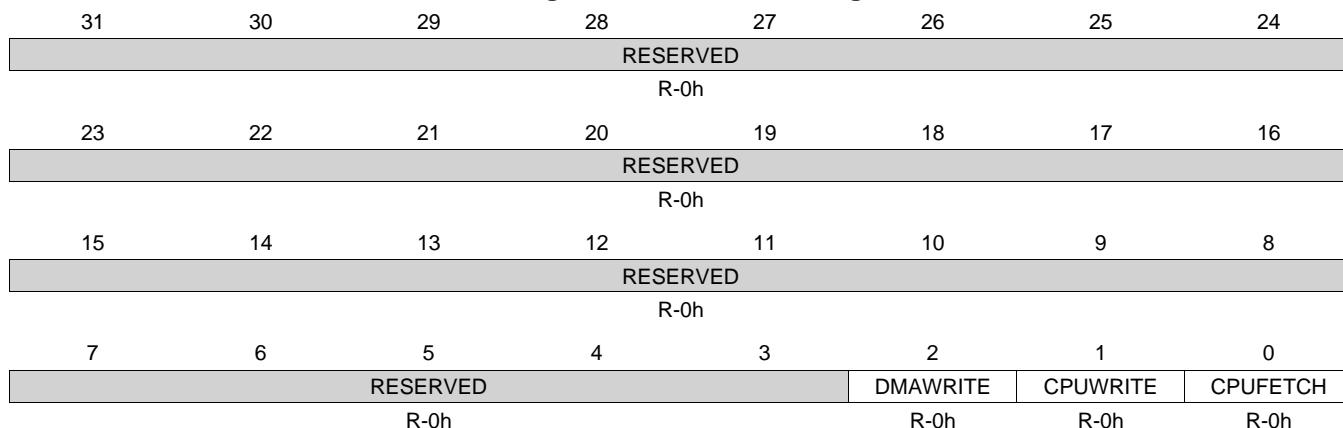
Table 1-278. NMCLA1FAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NMCLA1FAVADDR	R	0h	This register captures the address location for which non master CLA1 fetch access violation occurred.

1.14.18.12 MAVFLG Register (offset = 20h) [reset = 0h]

MAVFLG is shown in [Figure 1-272](#) and described in [Table 1-279](#).

Master Access Violation Flag Register

Figure 1-272. MAVFLG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

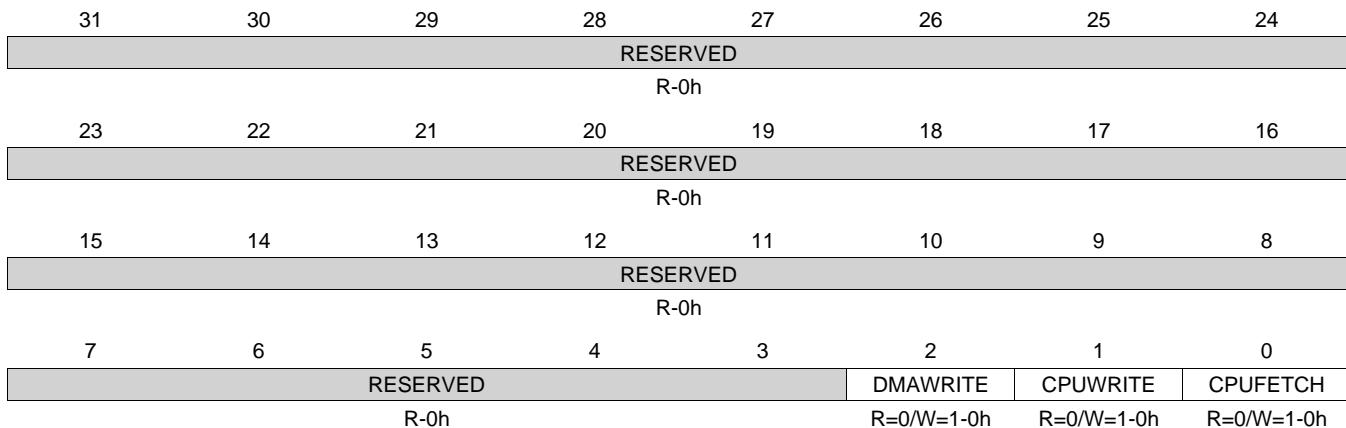
Table 1-279. MAVFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-3	RESERVED	R	0h	Reserved
2	DMAWRITE	R	0h	Master DMA Write Access Violation Flag: 0: No violation. 1: Access violation occurred.
1	CPUWRITE	R	0h	Master CPU Write Access Violation Flag: 0: No violation. 1: Access violation occurred.
0	CPUFETCH	R	0h	Master CPU Fetch Access Violation Flag: 0: No violation. 1: Access violation occurred.

1.14.18.13 MAVSET Register (offset = 22h) [reset = 0h]

MAVSET is shown in [Figure 1-273](#) and described in [Table 1-280](#).

Master Access Violation Flag Set Register

Figure 1-273. MAVSET Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

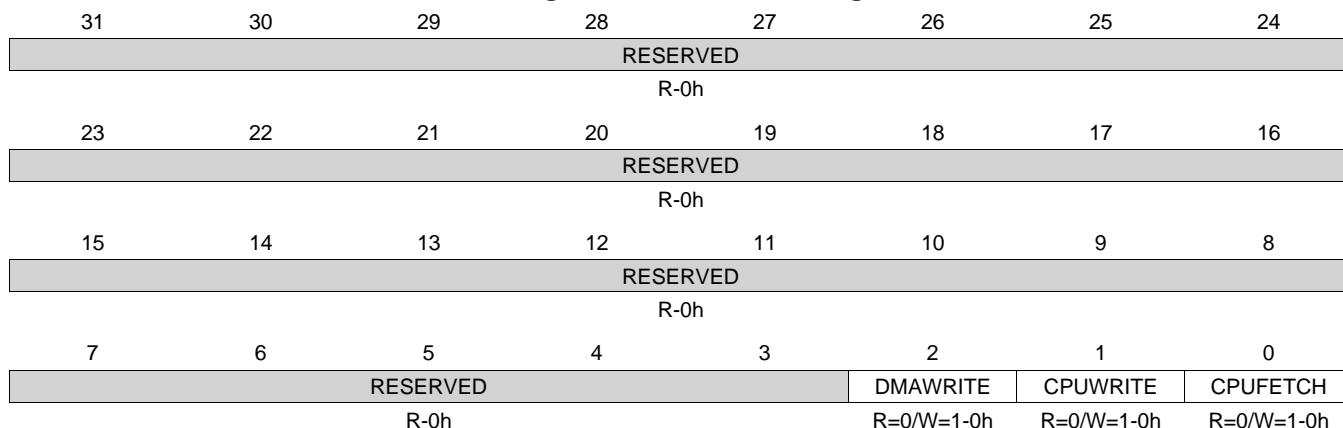
Table 1-280. MAVSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-3	RESERVED	R	0h	Reserved
2	DMAWRITE	R=0/W=1	0h	0: No action. 1: DMA Write Access Violation Flag in MAVFLG register will be set and interrupt will be generated if enabled..
1	CPUWRITE	R=0/W=1	0h	0: No action. 1: CPU Write Access Violation Flag in MAVFLG register will be set and interrupt will be generated if enabled..
0	CPUFETCH	R=0/W=1	0h	0: No action. 1: CPU Fetch Access Violation Flag in MAVFLG register will be set and interrupt will be generated if enabled..

1.14.18.14 MAVCLR Register (offset = 24h) [reset = 0h]

MAVCLR is shown in [Figure 1-274](#) and described in [Table 1-281](#).

Master Access Violation Flag Clear Register

Figure 1-274. MAVCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

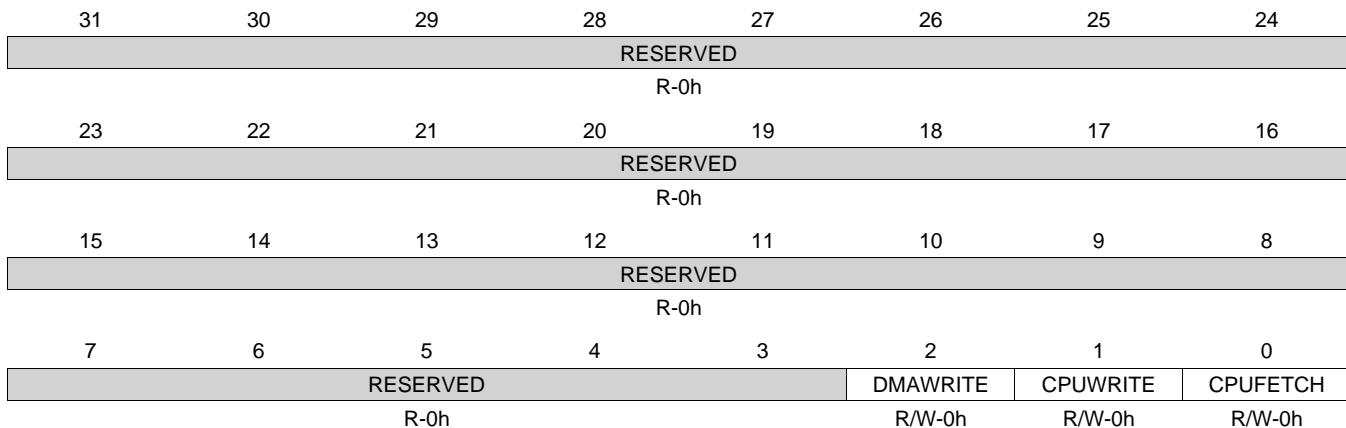
Table 1-281. MAVCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-3	RESERVED	R	0h	Reserved
2	DMAWRITE	R=0/W=1	0h	0: No action. 1: DMA Write Access Violation Flag in MAVFLG register will be cleared.
1	CPUWRITE	R=0/W=1	0h	0: No action. 1: CPU Write Access Violation Flag in MAVFLG register will be cleared.
0	CPUFETCH	R=0/W=1	0h	0: No action. 1: CPU Fetch Access Violation Flag in MAVFLG register will be cleared.

1.14.18.15 MAVINTEN Register (offset = 26h) [reset = 0h]

MAVINTEN is shown in [Figure 1-275](#) and described in [Table 1-282](#).

Master Access Violation Interrupt Enable Register

Figure 1-275. MAVINTEN Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-282. MAVINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-3	RESERVED	R	0h	Reserved
2	DMAWRITE	R/W	0h	0: DMA Write Access Violation Interrupt is disabled. 1: DMA Write Access Violation Interrupt is enabled.
1	CPUWRITE	R/W	0h	0: CPU Write Access Violation Interrupt is disabled. 1: CPU Write Access Violation Interrupt is enabled.
0	CPUFETCH	R/W	0h	0: CPU Fetch Access Violation Interrupt is disabled. 1: CPU Fetch Access Violation Interrupt is enabled.

1.14.18.16 MCPUFAVADDR Register (offset = 28h) [reset = 0h]MCPUFAVADDR is shown in [Figure 1-276](#) and described in [Table 1-283](#).

Master CPU Fetch Access Violation Address

Figure 1-276. MCPUFAVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCPUFAVADDR																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-283. MCPUFAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MCPUFAVADDR	R	0h	This register captures the address location for which master CPU fetch access violation occurred.

1.14.18.17 MCPUWRAVADDR Register (offset = 2Ah) [reset = 0h]

MCPUWRAVADDR is shown in [Figure 1-277](#) and described in [Table 1-284](#).

Master CPU Write Access Violation Address

Figure 1-277. MCPUWRAVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCPUWRAVADDR																															
R-0h																															

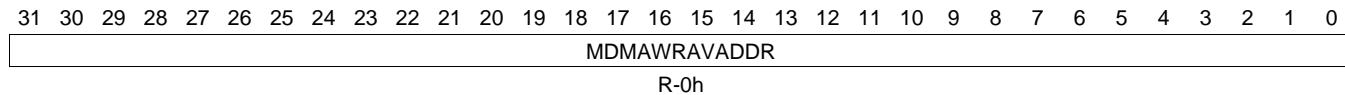
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-284. MCPUWRAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MCPUWRAVADDR	R	0h	This register captures the address location for which master CPU write access violation occurred.

1.14.18.18 MDMAWRAVADDR Register (offset = 2Ch) [reset = 0h]MDMAWRAVADDR is shown in [Figure 1-278](#) and described in [Table 1-285](#).

Master DMA Write Access Violation Address

Figure 1-278. MDMAWRAVADDR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-285. MDMAWRAVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MDMAWRAVADDR	R	0h	This register captures the address location for which master DMA write access violation occurred.

1.14.19 MEMORY_ERROR_REGS Registers

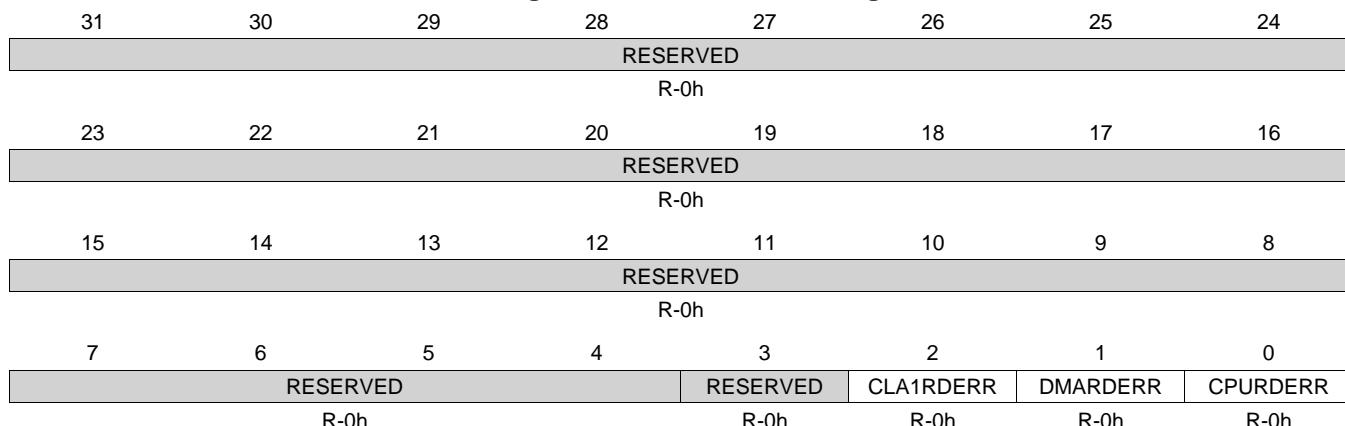
Table 1-286 lists the memory-mapped registers for the MEMORY_ERROR_REGS. All register offset addresses not listed in Table 1-286 should be considered as reserved locations and the register contents should not be modified.

Table 1-286. MEMORY_ERROR_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	UCERRFLG	Uncorrectable Error Flag Register	Section 1.14.19.1	
2h	UCERRSET	Uncorrectable Error Flag Set Register	Section 1.14.19.2	EALLOW
4h	UCERRCLR	Uncorrectable Error Flag Clear Register	Section 1.14.19.3	EALLOW
6h	UCCPUREADDR	Uncorrectable CPU Read Error Address	Section 1.14.19.4	
8h	UCDMAREADDR	Uncorrectable DMA Read Error Address	Section 1.14.19.5	
Ah	UCCLA1READDR	Uncorrectable CLA1 Read Error Address	Section 1.14.19.6	
20h	CERRFLG	Correctable Error Flag Register	Section 1.14.19.7	
22h	CERRSET	Correctable Error Flag Set Register	Section 1.14.19.8	EALLOW
24h	CERRCLR	Correctable Error Flag Clear Register	Section 1.14.19.9	EALLOW
26h	CCPUREADDR	Correctable CPU Read Error Address	Section 1.14.19.10	
2Eh	CERRCNT	Correctable Error Count Register	Section 1.14.19.11	
30h	CERRTHRES	Correctable Error Threshold Value Register	Section 1.14.19.12	EALLOW
32h	CEINTFLG	Correctable Error Interrupt Flag Status Register	Section 1.14.19.13	
34h	CEINTCLR	Correctable Error Interrupt Flag Clear Register	Section 1.14.19.14	EALLOW
36h	CEINTSET	Correctable Error Interrupt Flag Set Register	Section 1.14.19.15	EALLOW
38h	CEINTEN	Correctable Error Interrupt Enable Register	Section 1.14.19.16	EALLOW

1.14.19.1 UCERRFLG Register (offset = 0h) [reset = 0h]UCERRFLG is shown in [Figure 1-279](#) and described in [Table 1-287](#).

Uncorrectable Error Flag Register

Figure 1-279. UCERRFLG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-287. UCERRFLG Register Field Descriptions

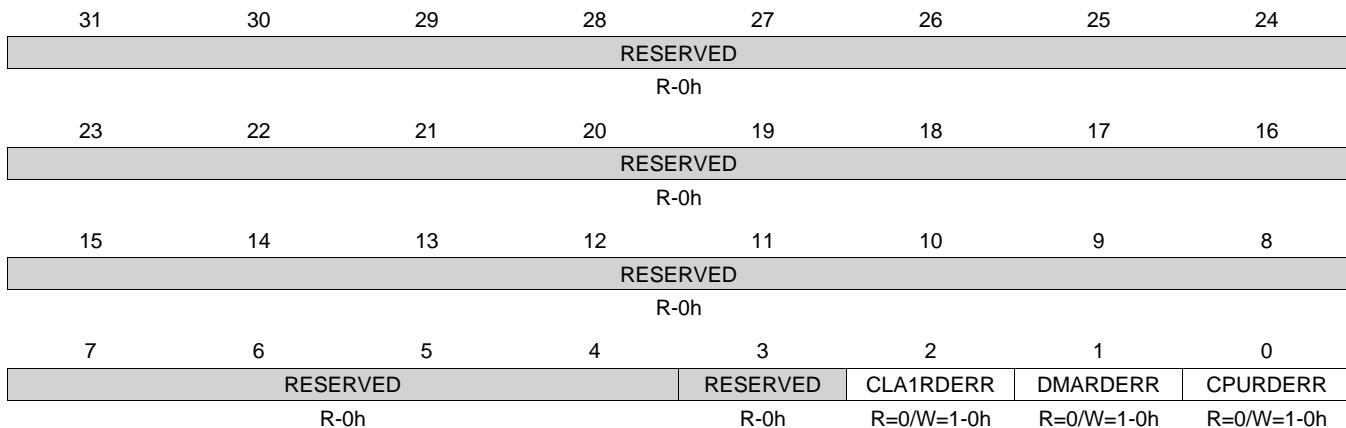
Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	CLA1RDERR	R	0h	CLA1 Uncorrectable Read Error Flag 0: No Error. 1: Uncorrectable error occurred during CLA1 read.
1	DMARDERR	R	0h	DMA Uncorrectable Read Error Flag 0: No Error. 1: Uncorrectable error occurred during DMA read.
0	CPURDERR	R	0h	CPU Uncorrectable Read Error Flag 0: No Error. 1: Uncorrectable error occurred during CPU read.

1.14.19.2 UCERRSET Register (offset = 2h) [reset = 0h]

UCERRSET is shown in [Figure 1-280](#) and described in [Table 1-288](#).

Uncorrectable Error Flag Set Register

Figure 1-280. UCERRSET Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

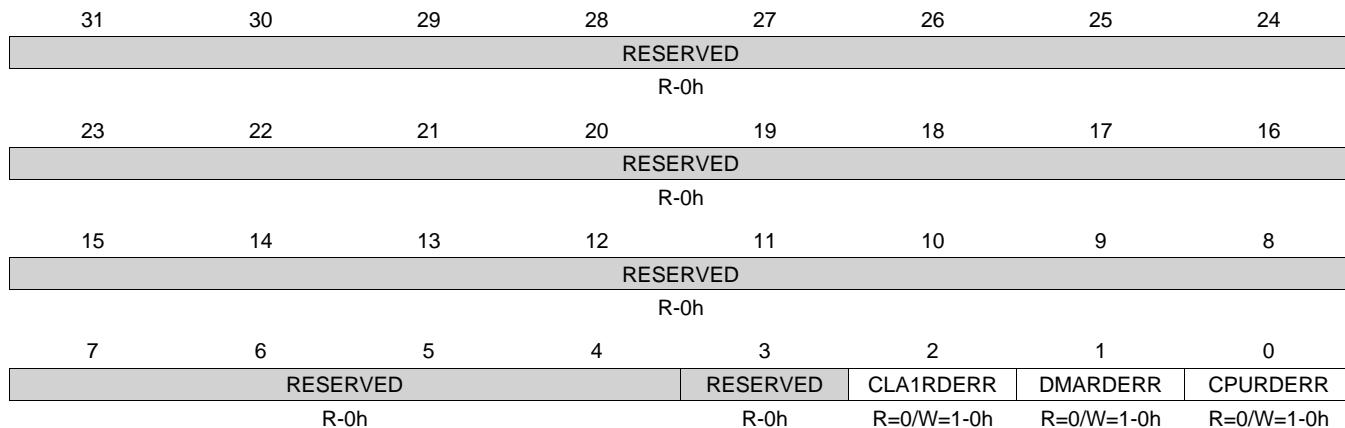
Table 1-288. UCERRSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	CLA1RDERR	R=0/W=1	0h	0: No action. 1: CLA1 Read Error Flag in UCERRFLG register will be set and interrupt will be generated if enabled..
1	DMARDERR	R=0/W=1	0h	0: No action. 1: DMA Read Error Flag in UCERRFLG register will be set and interrupt will be generated if enabled..
0	CPURDERR	R=0/W=1	0h	0: No action. 1: CPU Read Error Flag in UCERRFLG register will be set and interrupt will be generated if enabled..

1.14.19.3 UCERRCLR Register (offset = 4h) [reset = 0h]

UCERRCLR is shown in [Figure 1-281](#) and described in [Table 1-289](#).

Uncorrectable Error Flag Clear Register

Figure 1-281. UCERRCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-289. UCERRCLR Register Field Descriptions

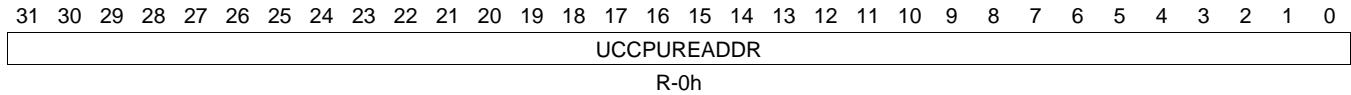
Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	CLA1RDERR	R=0/W=1	0h	0: No action. 1: CLA1 Read Error Flag in UCERRFLG register will be cleared.
1	DMARDERR	R=0/W=1	0h	0: No action. 1: DMA Read Error Flag in UCERRFLG register will be cleared .
0	CPURDERR	R=0/W=1	0h	0: No action. 1: CPU Read Error Flag in UCERRFLG register will be cleared.

1.14.19.4 UCCPUREADDR Register (offset = 6h) [reset = 0h]

UCCPUREADDR is shown in [Figure 1-282](#) and described in [Table 1-290](#).

Uncorrectable CPU Read Error Address

Figure 1-282. UCCPUREADDR Register



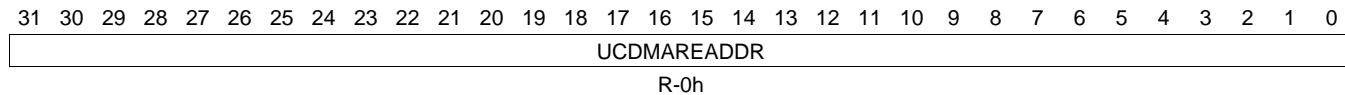
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-290. UCCPUREADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UCCPUREADDR	R	0h	This register captures the address location for which CPU read/fetch access resulted in uncorrectable ECC/Parity error.

1.14.19.5 UCDMAREADDR Register (offset = 8h) [reset = 0h]UCDMAREADDR is shown in [Figure 1-283](#) and described in [Table 1-291](#).

Uncorrectable DMA Read Error Address

Figure 1-283. UCDMAREADDR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

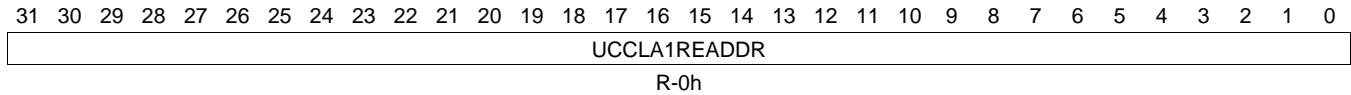
Table 1-291. UCDMAREADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UCDMAREADDR	R	0h	This register captures the address location for which DMA read access resulted in uncorrectable ECC/Parity error.

1.14.19.6 UCCLA1READDR Register (offset = Ah) [reset = 0h]

UCCLA1READDR is shown in [Figure 1-284](#) and described in [Table 1-292](#).

Uncorrectable CLA1 Read Error Address

Figure 1-284. UCCLA1READDR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

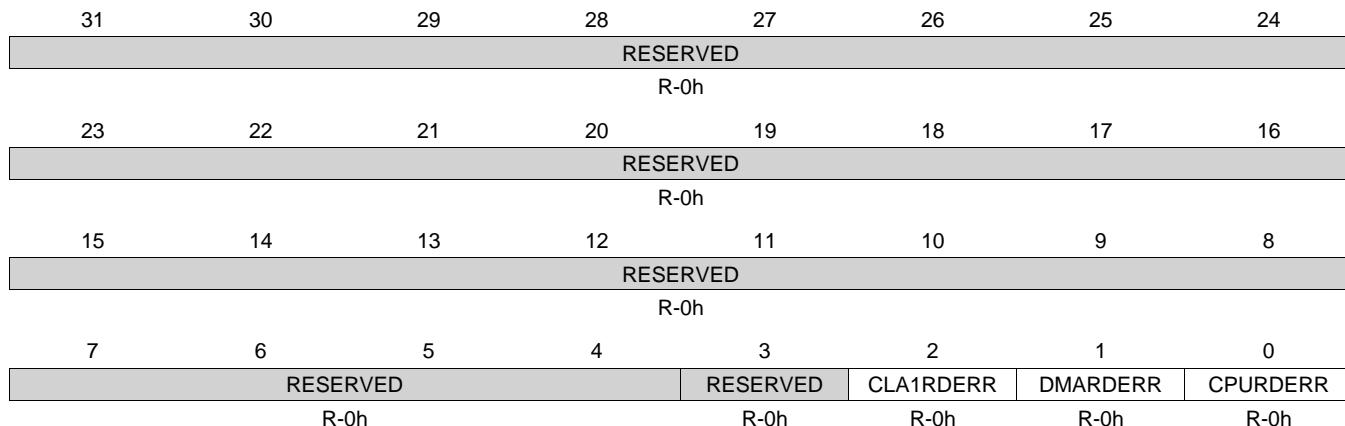
Table 1-292. UCCLA1READDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UCCLA1READDR	R	0h	This register captures the address location for which CLA1 read/fetch access resulted in uncorrectable ECC/Parity error.

1.14.19.7 CERRFLG Register (offset = 20h) [reset = 0h]

CERRFLG is shown in [Figure 1-285](#) and described in [Table 1-293](#).

Correctable Error Flag Register

Figure 1-285. CERRFLG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

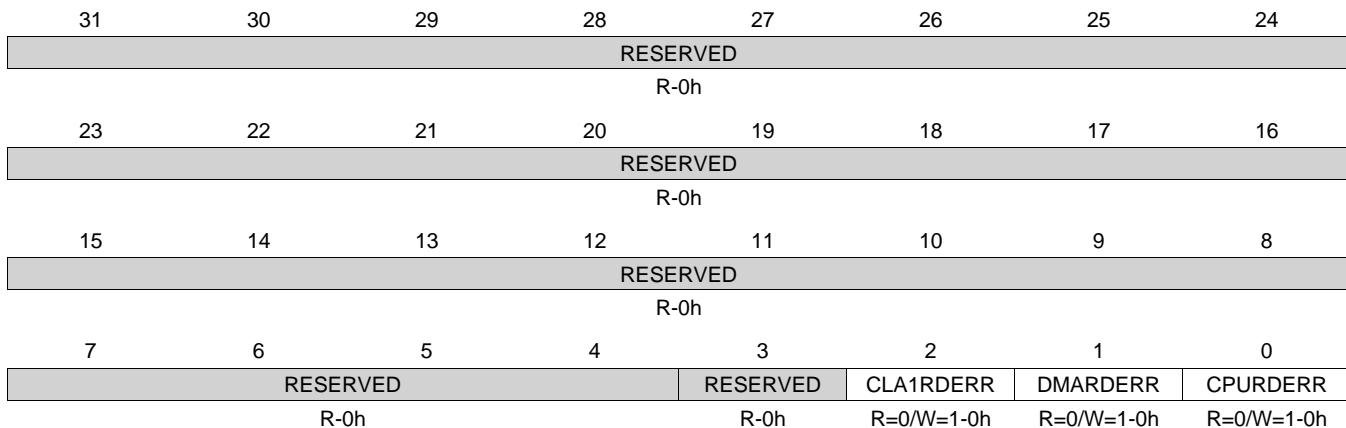
Table 1-293. CERRFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	CLA1RDERR	R	0h	CLA1 Correctable Read Error Flag 0: No Error. 1: Correctable error occurred during CLA1 read.
1	DMARDERR	R	0h	DMA Correctable Read Error Flag 0: No Error. 1: Correctable error occurred during DMA read.
0	CPURDERR	R	0h	CPU Correctable Read Error Flag 0: No Error. 1: Correctable error occurred during CPU read.

1.14.19.8 CERRSET Register (offset = 22h) [reset = 0h]

CERRSET is shown in [Figure 1-286](#) and described in [Table 1-294](#).

Correctable Error Flag Set Register

Figure 1-286. CERRSET Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

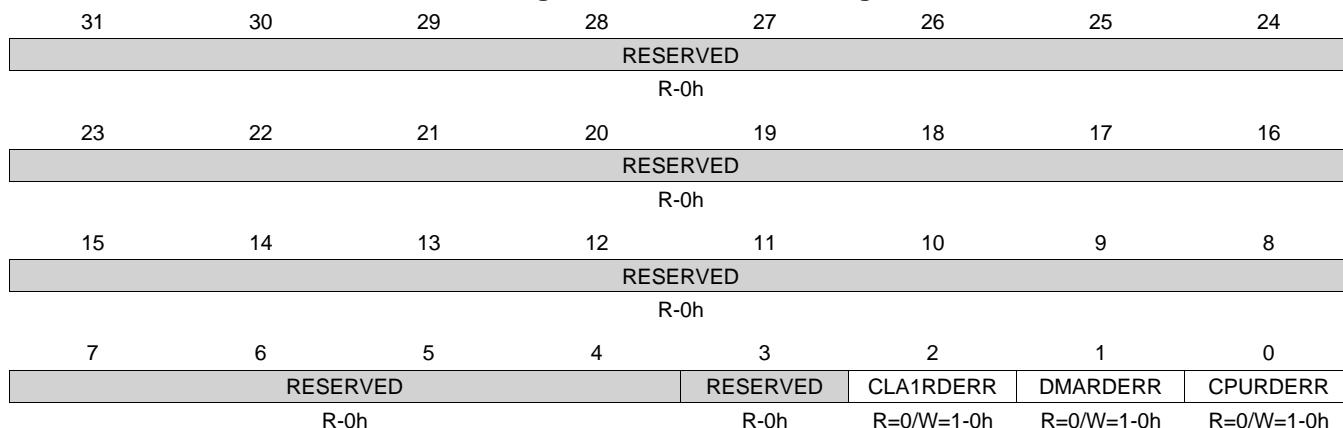
Table 1-294. CERRSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	CLA1RDERR	R=0/W=1	0h	0: No action. 1: CLA1 Read Error Flag in CERRFLG register will be set and interrupt will be generated if enabled..
1	DMARDERR	R=0/W=1	0h	0: No action. 1: DMA Read Error Flag in CERRFLG register will be set and interrupt will be generated if enabled..
0	CPURDERR	R=0/W=1	0h	0: No action. 1: CPU Read Error Flag in CERRFLG register will be set and interrupt will be generated if enabled..

1.14.19.9 CERRCLR Register (offset = 24h) [reset = 0h]

CERRCLR is shown in [Figure 1-287](#) and described in [Table 1-295](#).

Correctable Error Flag Clear Register

Figure 1-287. CERRCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

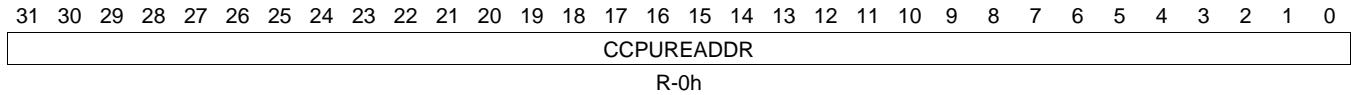
Table 1-295. CERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	CLA1RDERR	R=0/W=1	0h	0: No action. 1: CLA1 Read Error Flag in CERRFLG register will be cleared.
1	DMARDERR	R=0/W=1	0h	0: No action. 1: DMA Read Error Flag in CERRFLG register will be cleared .
0	CPURDERR	R=0/W=1	0h	0: No action. 1: CPU Read Error Flag in CERRFLG register will be cleared.

1.14.19.10 CCPUREADDR Register (offset = 26h) [reset = 0h]

CCPUREADDR is shown in [Figure 1-288](#) and described in [Table 1-296](#).

Correctable CPU Read Error Address

Figure 1-288. CCPUREADDR Register

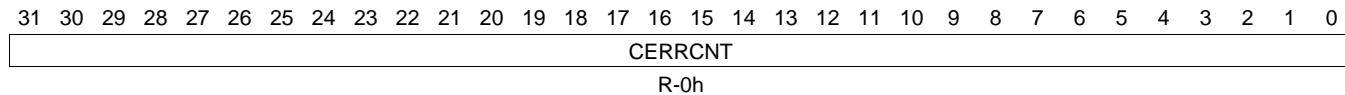
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-296. CCPUREADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCPUREADDR	R	0h	This register captures the address location for which CPU read/fetch access resulted in correctable ECC error.

1.14.19.11 CERRCNT Register (offset = 2Eh) [reset = 0h]CERRCNT is shown in [Figure 1-289](#) and described in [Table 1-297](#).

Correctable Error Count Register

Figure 1-289. CERRCNT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-297. CERRCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CERRCNT	R	0h	This register holds the count of how many times correctable error occurred.

1.14.19.12 CERRTHRES Register (offset = 30h) [reset = 0h]

CERRTHRES is shown in [Figure 1-290](#) and described in [Table 1-298](#).

Correctable Error Threshold Value Register

Figure 1-290. CERRTHRES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CERRTHRES																															
R/W-0h																															

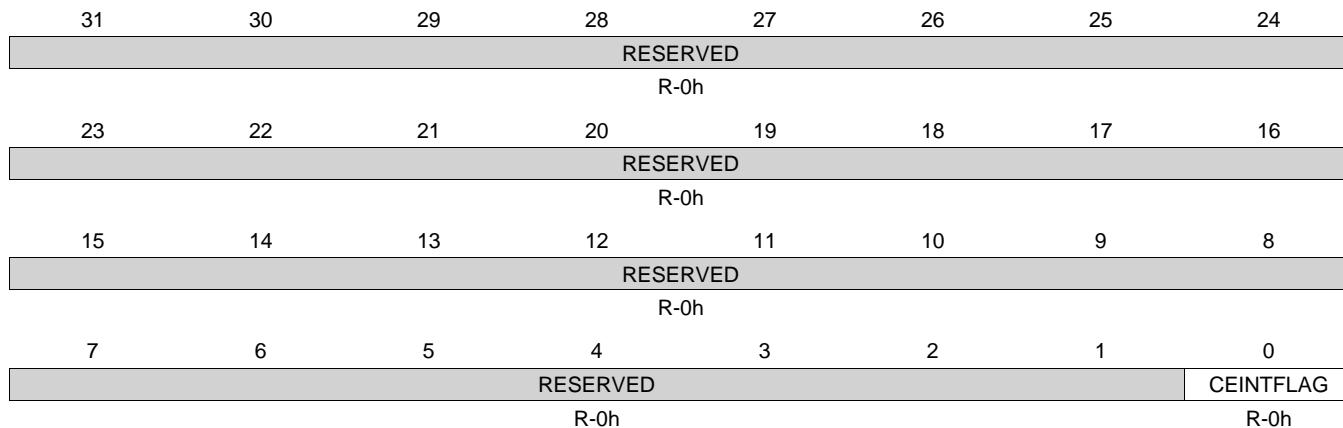
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-298. CERRTHRES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CERRTHRES	R/W	0h	When value in CERRCNT register is greater than value configured in this register, correctable interrupt gets generated, if enabled.

1.14.19.13 CEINTFLG Register (offset = 32h) [reset = 0h]CEINTFLG is shown in [Figure 1-291](#) and described in [Table 1-299](#).

Correctable Error Interrupt Flag Status Register

Figure 1-291. CEINTFLG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

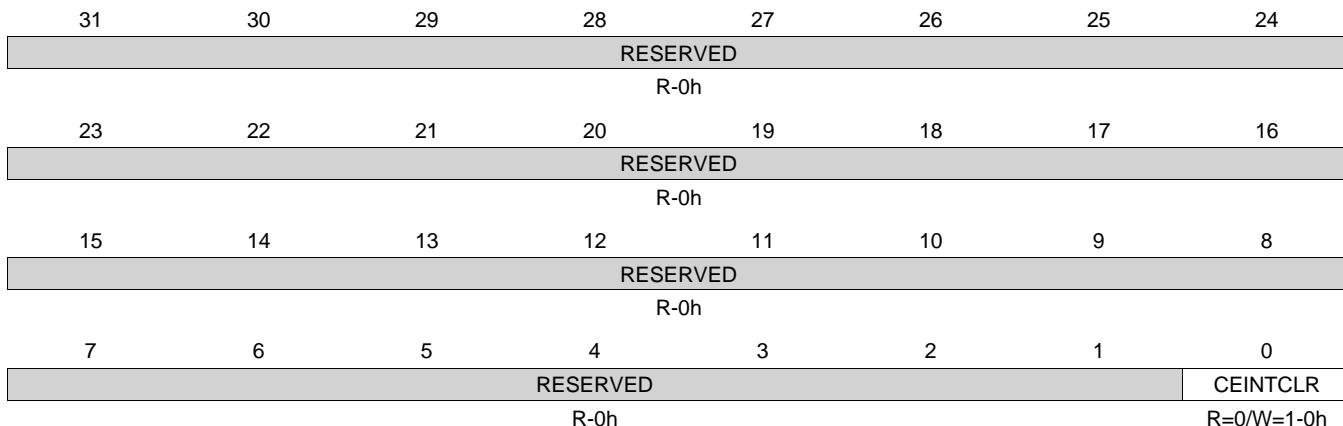
Table 1-299. CEINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	CEINTFLAG	R	0h	Total corrected error count exceeded threshold Flag 0: Total correctable errors < Threshold value configured in CERRTHRES register. 1: Total correctable errors >= Threshold value configured in CERRTHRES register.

1.14.19.14 CEINTCLR Register (offset = 34h) [reset = 0h]

CEINTCLR is shown in [Figure 1-292](#) and described in [Table 1-300](#).

Correctable Error Interrupt Flag Clear Register

Figure 1-292. CEINTCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

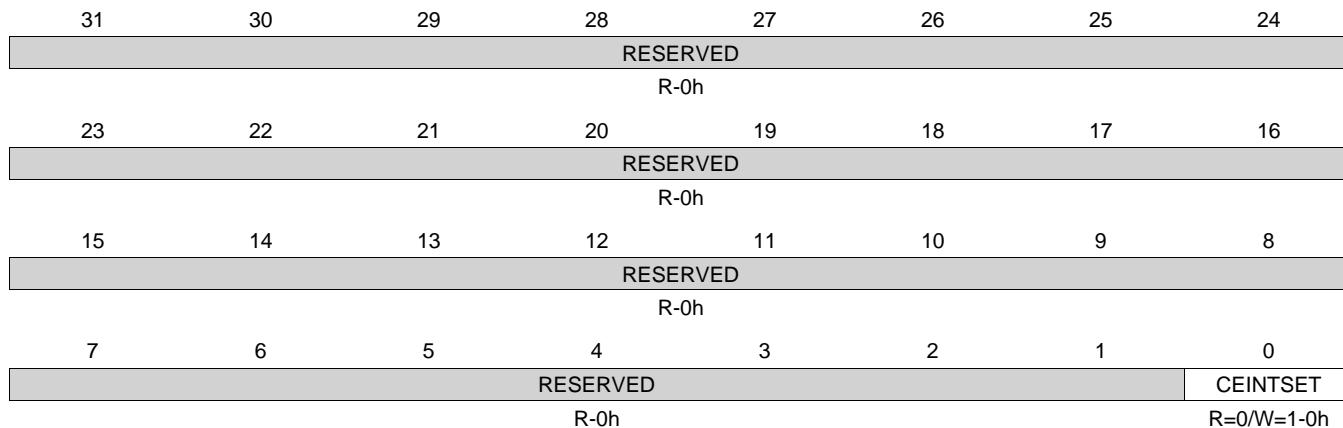
Table 1-300. CEINTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	CEINTCLR	R=0/W=1	0h	0: No action. 1: Total corrected error count exceeded flag in CEINTFLG register will be cleared.

1.14.19.15 CEINTSET Register (offset = 36h) [reset = 0h]

CEINTSET is shown in [Figure 1-293](#) and described in [Table 1-301](#).

Correctable Error Interrupt Flag Set Register

Figure 1-293. CEINTSET Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

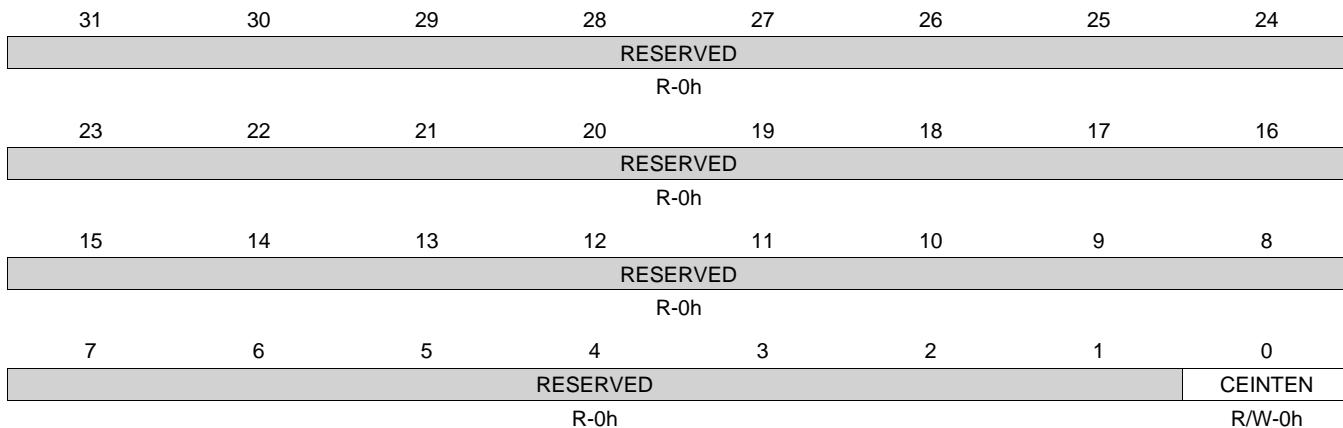
Table 1-301. CEINTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	CEINTSET	R=0/W=1	0h	0: No action. 1: Total corrected error count exceeded flag in CEINTFLG register will be set and interrupt will be generated if enabled.

1.14.19.16 CEINTEN Register (offset = 38h) [reset = 0h]

CEINTEN is shown in [Figure 1-294](#) and described in [Table 1-302](#).

Correctable Error Interrupt Enable Register

Figure 1-294. CEINTEN Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-302. CEINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	CEINTEN	R/W	0h	0: Correctable Error Interrupt is disabled. 1: Correctable Error Interrupt is enabled.

1.14.20 ROM_WAIT_STATE_REGS Registers

Table 1-303 lists the memory-mapped registers for the ROM_WAIT_STATE_REGS. All register offset addresses not listed in Table 1-303 should be considered as reserved locations and the register contents should not be modified.

Table 1-303. ROM_WAIT_STATE_REGS REGISTERS

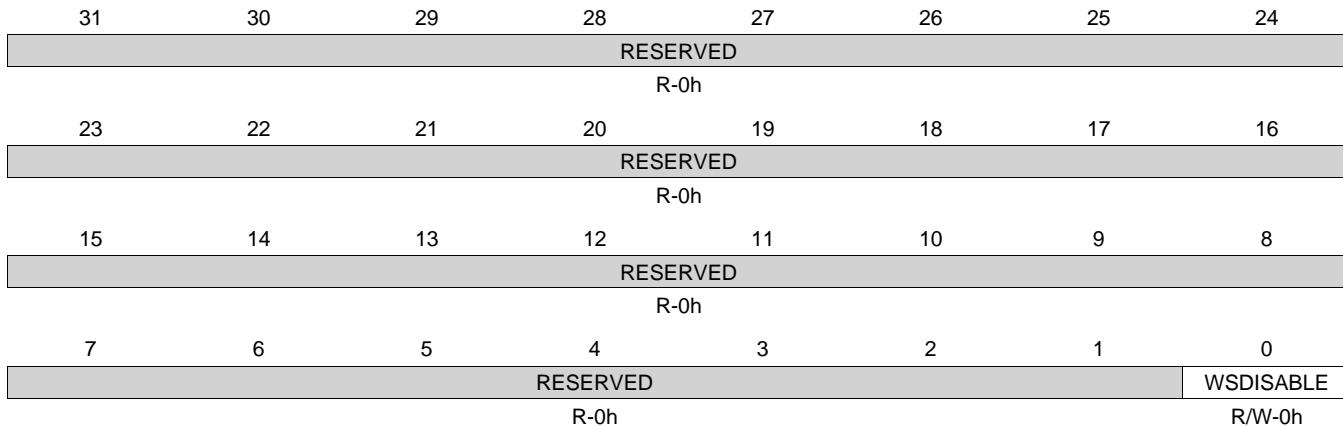
Offset	Acronym	Register Name	Section	Write Protection
0h	ROMWAITSTATE	ROM Wait State Configuration Register	Section 1.14.20.1	EALLOW

1.14.20.1 ROMWAITSTATE Register (offset = 0h) [reset = 0h]

ROMWAITSTATE is shown in [Figure 1-295](#) and described in [Table 1-304](#).

ROM Wait State Configuration Register

Figure 1-295. ROMWAITSTATE Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-304. ROMWAITSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	WSDISABLE	R/W	0h	0: ROM Wait State is enabled. CPU accesses to ROM are 1-wait. 1: ROM Wait State is disabled. CPU accesses to ROM are 0-wait.

1.14.21 FLASH_CTRL_REGS Registers

Table 1-305 lists the memory-mapped registers for the FLASH_CTRL_REGS. All register offset addresses not listed in Table 1-305 should be considered as reserved locations and the register contents should not be modified.

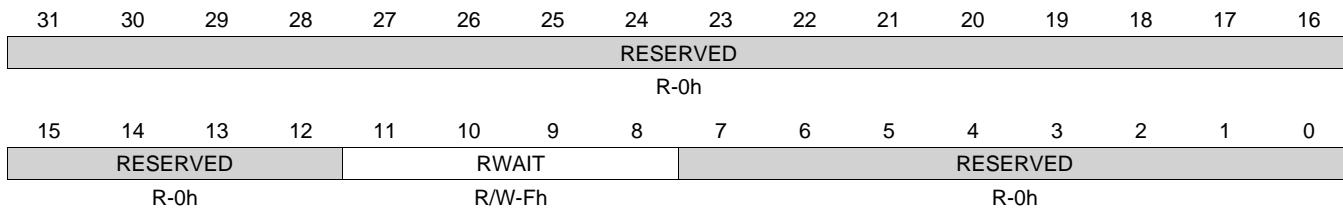
Table 1-305. FLASH_CTRL_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	FRDCNTL	Flash Read Control Register	Section 1.14.21.1	
2h	FSPRD	Flash Read Margin Control Register	Section 1.14.21.2	
1Eh	FBAC	Flash Bank Access Control Register	Section 1.14.21.3	
20h	FBFALLBACK	Flash Bank Fallback Power Register	Section 1.14.21.4	
22h	FBPRDY	Flash Bank Pump Ready Register	Section 1.14.21.5	
24h	FPAC1	Flash Pump Access Control Register 1	Section 1.14.21.6	
26h	FPAC2	Flash Pump Access Control Register 2	Section 1.14.21.7	
28h	FMAC	Flash Module Access Control Register	Section 1.14.21.8	
2Ah	FMSTAT	Flash Module Status Register	Section 1.14.21.9	
180h	FRD_INTF_CTRL	Flash Read Interface Control Register	Section 1.14.21.10	

1.14.21.1 FRDCNTL Register (offset = 0h) [reset = F00h]

FRDCNTL is shown in [Figure 1-296](#) and described in [Table 1-306](#).

Flash Read Control Register

Figure 1-296. FRDCNTL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-306. FRDCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	RESERVED	R	0h	Reserved
11-8	RWAIT	R/W	Fh	<p>Random read waitstate</p> <p>These bits indicate how many waitstates are added to a flash read access. The RWAIT value can be set anywhere from 0 to 0xF. For a flash access, data is returned in RWAIT+1 C28 SYSCLK cycles.</p> <p>Note: The required wait states for each SYSCLK frequency can be found in the device data manual.</p>
7-0	RESERVED	R	0h	Reserved

1.14.21.2 FSPRD Register (offset = 2h) [reset = 0h]

FSPRD is shown in [Figure 1-297](#) and described in [Table 1-307](#).

Flash Read Margin Control Register

Figure 1-297. FSPRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R-0h															
														R/W- 0h	R/W- 0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-307. FSPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	RESERVED	R	0h	Reserved
1	RM1	R/W	0h	0 Read Margin 1 mode is disabled 1 Read Margin 1 mode is enabled
0	RM0	R/W	0h	0 Read Margin 0 mode is disabled 1 Read Margin 0 mode is enabled

1.14.21.3 FBAC Register (offset = 1Eh) [reset = Fh]

FBAC is shown in [Figure 1-298](#) and described in [Table 1-308](#).

Flash Bank Access Control Register

Figure 1-298. FBAC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BAGP		VREADST					
R-0h																								R/W-0h		R/W-Fh					

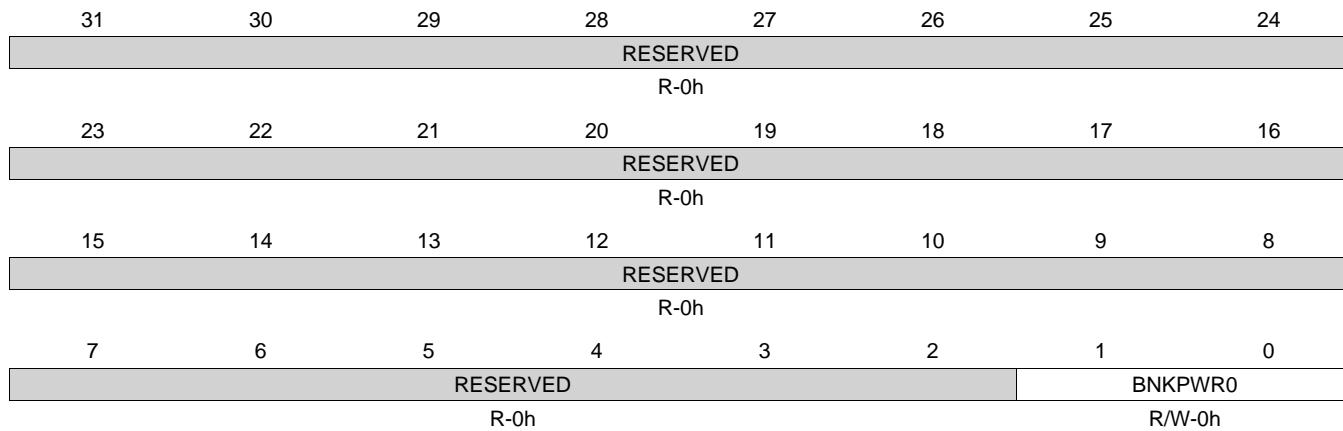
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-308. FBAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	BAGP	R/W	0h	Bank Active Grace Period. These bits contain the starting count value for the BAGP down counter. Any access to a given bank causes its BAGP counter to reload the BAGP value for that bank. After the last access to this flash bank, the down counter delays from 0 to 255 prescaled SYSCLK clock cycles before putting the bank into one of the fallback power modes as determined by the FBFAULTBACK register. This value must be greater than 1 when the fallback mode is not ACTIVE. Note: The prescaled clock used for the BAGP down counter is a clock divided by 16 from input SYSCLK.
7-0	VREADST	R/W	Fh	VREAD setup. VREAD is generated by the flash pump and used for flash read operation. The bank power up sequencing starts VREADST HCLK cycles after VREAD power supply becomes stable.

1.14.21.4 FBFALLBACK Register (offset = 20h) [reset = 0h]FBFALLBACK is shown in [Figure 1-299](#) and described in [Table 1-309](#).

Flash Bank Fallback Power Register

Figure 1-299. FBFALLBACK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

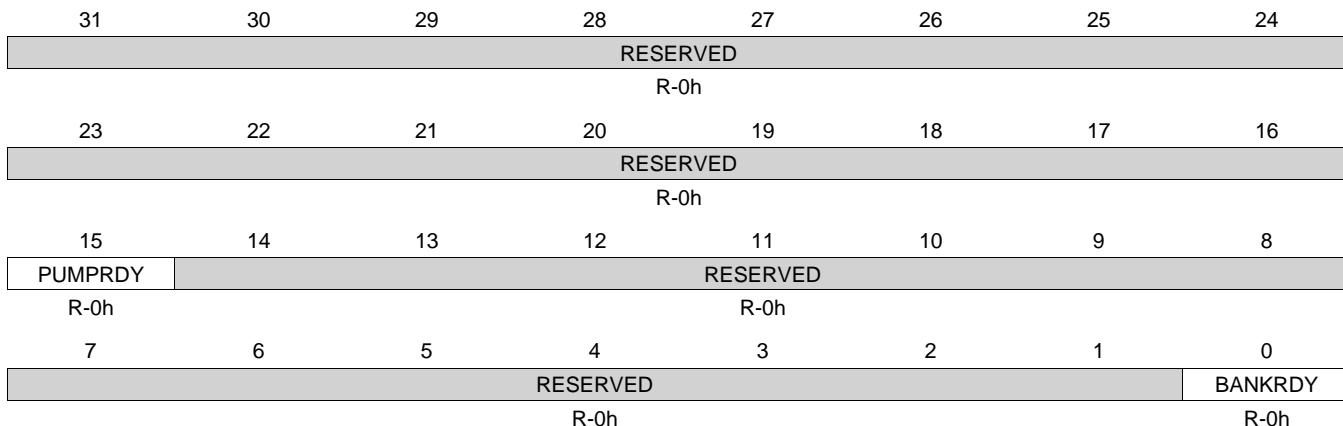
Table 1-309. FBFALLBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	RESERVED	R	0h	Reserved
1-0	BNKPWR0	R/W	0h	Fall Back power mode 00 Sleep (Sense amplifiers and sense reference disabled) 01 Standby (Sense amplifiers disabled, but sense reference enabled) 10 Reserved 11 Active (Both sense amplifiers and sense reference enabled) Note: If the bank and pump are not in active mode and an access is made, the value of this register is automatically changed to active.

1.14.21.5 FBPRDY Register (offset = 22h) [reset = 0h]

FBPRDY is shown in [Figure 1-300](#) and described in [Table 1-310](#).

Flash Bank Pump Ready Register

Figure 1-300. FBPRDY Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-310. FBPRDY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	PUMPRDY	R	0h	Pump Ready. This is a read-only bit which allows software to determine if the pump is ready for flash access before attempting the actual access. If an access is made to a bank when the pump is not ready, wait states are asserted until it becomes ready. 0 Pump is not ready. 1 Pump is ready, in active power state.
14-1	RESERVED	R	0h	Reserved
0	BANKRDY	R	0h	Bank Ready. This is a read-only register which allows software to determine if the bank is ready for Flash access before the access is attempted. Note: The user should wait for both the pump and the bank to be ready before attempting an access. 0 Bank is not ready. 1 Bank is in active power mode and is ready for access.

1.14.21.6 FPAC1 Register (offset = 24h) [reset = 640000h]

FPAC1 is shown in [Figure 1-301](#) and described in [Table 1-311](#).

Flash Pump Access Control Register 1

Figure 1-301. FPAC1 Register

31	30	29	28	27	26	25	24
RESERVED						PSLEEP	
R-0h						R/W-64h	
23	22	21	20	19	18	17	16
RESERVED						PSLEEP	
R-0h						R/W-64h	
15	14	13	12	11	10	9	8
RESERVED						R-0h	
7	6	5	4	3	2	1	0
RESERVED						PMPPWR	
R-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-311. FPAC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-16	PSLEEP	R/W	64h	Pump sleep. These bits contain the starting count value for the charge pump sleep down counter. While the charge pump is in sleep mode, the power mode management logic holds the charge pump sleep counter at this value. When the charge pump exits sleep power mode, the down counter delays from 0 to PSLEEP prescaled SYSCLK clock cycles before putting the charge pump into active power mode. Note: The pump sleep down counter uses the same prescaled clock as Bank sleep down counter which is divided by 2 of input SYSCLK.
15-1	RESERVED	R	0h	Reserved
0	PMPPWR	R/W	0h	Flash Charge Pump Fallback Power Mode. This bit selects what power mode the charge pump enters after the pump active grace period (PAGP) counter has timed out. 0 Sleep (all pump circuits disabled) 1 Active (all pump circuits active) Note: As the pump is shared between both CPU1 and CPU2 banks, if an access is made either to the CPU1 bank or CPU2 bank, the value of this bit changes to 1 (active).

1.14.21.7 FPAC2 Register (offset = 26h) [reset = 0h]

FPAC2 is shown in [Figure 1-302](#) and described in [Table 1-312](#).

Flash Pump Access Control Register 2

Figure 1-302. FPAC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PAGP															

R-0h

R/W-0h

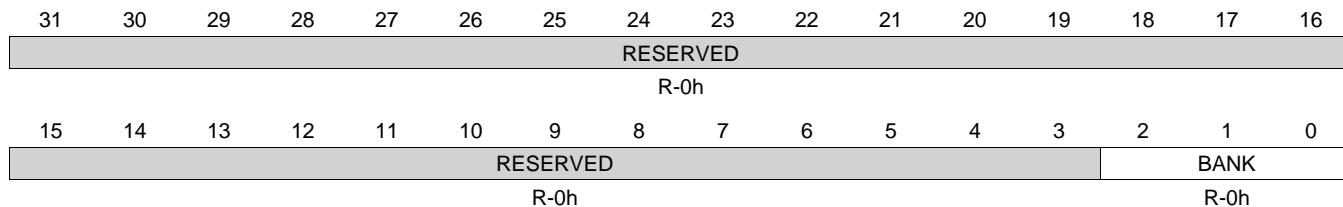
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-312. FPAC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PAGP	R/W	0h	<p>Pump Active Grace Period. This register contains the starting count value for the PAGP mode down counter. Any access to flash memory causes the counter to reload with the PAGP value. After the last access to flash memory, the down counter delays from 0 to 65535 prescaled SYSCLK clock cycles before entering one of the charge pump fallback power modes as determined by PUMPPWR in the FPAC1 register.</p> <p>Note: The PAGP down counter is clocked by the same prescaled clock as the BAGP down counter which is divided by 16 of input SYSCLK.</p>

1.14.21.8 FMAC Register (offset = 28h) [reset = 0h]FMAC is shown in [Figure 1-303](#) and described in [Table 1-313](#).

Flash Module Access Control Register

Figure 1-303. FMAC Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-313. FMAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-3	RESERVED	R	0h	Reserved
2-0	BANK	R	0h	0 BANKID. Controls the bank on which the Flash FSM operations will be performed. For these devices, the value of this field will be 0 as there is only one bank for each CPU.

1.14.21.9 FMSTAT Register (offset = 2Ah) [reset = 0h]

FMSTAT is shown in [Figure 1-304](#) and described in [Table 1-314](#).

Flash Module Status Register

Figure 1-304. FMSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	ILA	RESERVED	PGV	RESERVED	EV	RESERVED	BUSY
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
ERS	PGM	INVDAT	CSTAT	VOLTSTAT	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-314. FMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	ILA	R	0h	Illegal Address When set, indicates that an illegal address is detected. Three conditions can set illegal address flag. - Writing to a hole (un-implemented logical address space) within a flash bank. - Writing to an address location to an un-implemented flash space. - Input address for write is decoded to select a different bank from the bank ID register. - The address range does not match the type of FSM command.
13	RESERVED	R	0h	Reserved
12	PGV	R	0h	Program verify When set, indicates that a word is not successfully programmed after the maximum allowed number of program pulses are given for program operation.
11	RESERVED	R	0h	Reserved
10	EV	R	0h	Erase verify When set, indicates that a sector is not successfully erased after the maximum allowed number of erase pulses are given for erase operation.
9	RESERVED	R	0h	Reserved
8	BUSY	R	0h	When set, this bit indicates that a program, erase, or suspend operation is being processed.
7	ERS	R	0h	Erase Active. When set, this bit indicates that the flash module is actively performing an erase operation. This bit is set when erasing starts and is cleared when erasing is complete. It is also cleared when the erase is suspended and set when the erase resumes.

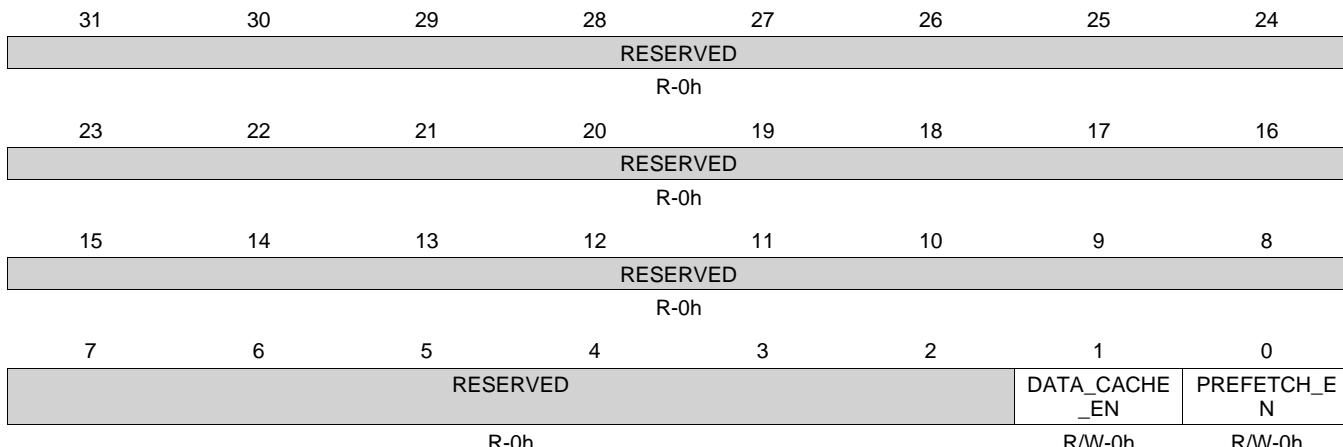
Table 1-314. FMSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PGM	R	0h	Program Active. When set, this bit indicates that the flash module is currently performing a program operation. This bit is set when programming starts and is cleared when programming is complete. It is also cleared when programming is suspended and set when programming resumes.
5	INVDAT	R	0h	Invalid Data. When set, this bit indicates that the user attempted to program a "1" where a "0" was already present.
4	CSTAT	R	0h	Command Status. Once the FSM starts any failure will set this bit. When set, this bit informs the host that the program, erase, or validate sector command failed and the command was stopped. This bit is cleared by the Clear Status command. For some errors, this will be the only indication of an FSM error because the cause does not fall within the other error bit types.
3	VOLTSTAT	R	0h	Core Voltage Status. When set, this bit indicates that the core voltage generator of the pump power supply dipped below the lower limit allowable during a program or erase operation.
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

1.14.21.10 FRD_INTF_CTRL Register (offset = 180h) [reset = 0h]

FRD_INTF_CTRL is shown in [Figure 1-305](#) and described in [Table 1-315](#).

Flash Read Interface Control Register

Figure 1-305. FRD_INTF_CTRL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-315. FRD_INTF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	RESERVED	R	0h	Reserved
1	DATA_CACHE_EN	R/W	0h	Data cache enable. 0 A value of 0 disables the data cache. 1 A value of 1 enables the data cache.
0	PREFETCH_EN	R/W	0h	Prefetch enable. 0 A value of 0 disables program cache and prefetch mechanism. 1 A value of 1 enables program cache and pre-fetch mechanism.

1.14.22 FLASH_ECC_REGS Registers

Table 1-316 lists the memory-mapped registers for the FLASH_ECC_REGS. All register offset addresses not listed in **Table 1-316** should be considered as reserved locations and the register contents should not be modified.

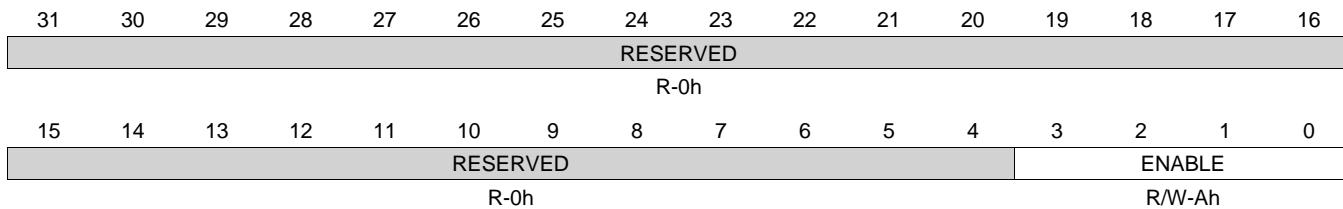
Table 1-316. FLASH_ECC_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	ECC_ENABLE	ECC Enable	Section 1.14.22.1	
2h	SINGLE_ERR_ADDR_LOW	Single Error Address Low	Section 1.14.22.2	
4h	SINGLE_ERR_ADDR_HIGH	Single Error Address High	Section 1.14.22.3	
6h	UNC_ERR_ADDR_LOW	Uncorrectable Error Address Low	Section 1.14.22.4	
8h	UNC_ERR_ADDR_HIGH	Uncorrectable Error Address High	Section 1.14.22.5	
Ah	ERR_STATUS	Error Status	Section 1.14.22.6	
Ch	ERR_POS	Error Position	Section 1.14.22.7	
Eh	ERR_STATUS_CLR	Error Status Clear	Section 1.14.22.8	
10h	ERR_CNT	Error Control	Section 1.14.22.9	
12h	ERR_THRESHOLD	Error Threshold	Section 1.14.22.10	
14h	ERR_INTFLG	Error Interrupt Flag	Section 1.14.22.11	
16h	ERR_INTCLR	Error Interrupt Flag Clear	Section 1.14.22.12	
18h	FDATAH_TEST	Data High Test	Section 1.14.22.13	
1Ah	FDATA_L_TEST	Data Low Test	Section 1.14.22.14	
1Ch	FADDR_TEST	ECC Test Address	Section 1.14.22.15	
1Eh	FECC_TEST	ECC Test Address	Section 1.14.22.16	
20h	FECC_CTRL	ECC Control	Section 1.14.22.17	
22h	FOUTH_TEST	Test Data Out High	Section 1.14.22.18	
24h	FOUTL_TEST	Test Data Out Low	Section 1.14.22.19	
26h	FECC_STATUS	ECC Status	Section 1.14.22.20	

1.14.22.1 ECC_ENABLE Register (offset = 0h) [reset = Ah]

ECC_ENABLE is shown in [Figure 1-306](#) and described in [Table 1-317](#).

ECC Enable

Figure 1-306. ECC_ENABLE Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-317. ECC_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	RESERVED	R	0h	Reserved
3-0	ENABLE	R/W	Ah	ECC enable. A value of 0xA would enable ECC. Any other value would disable ECC.

1.14.22.2 SINGLE_ERR_ADDR_LOW Register (offset = 2h) [reset = 0h]SINGLE_ERR_ADDR_LOW is shown in [Figure 1-307](#) and described in [Table 1-318](#).

Single Error Address Low

Figure 1-307. SINGLE_ERR_ADDR_LOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_ADDR_L																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-318. SINGLE_ERR_ADDR_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ERR_ADDR_L	R/W	0h	64-bit aligned address at which a single bit error occurred in the lower 64-bits of a 128-bit aligned memory.

1.14.22.3 SINGLE_ERR_ADDR_HIGH Register (offset = 4h) [reset = 0h]

SINGLE_ERR_ADDR_HIGH is shown in [Figure 1-308](#) and described in [Table 1-319](#).

Single Error Address High

Figure 1-308. SINGLE_ERR_ADDR_HIGH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_ADDR_H																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-319. SINGLE_ERR_ADDR_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ERR_ADDR_H	R/W	0h	64-bit aligned address at which a single bit error occurred in the upper 64-bits of a 128-bit aligned memory.

1.14.22.4 UNC_ERR_ADDR_LOW Register (offset = 6h) [reset = 0h]UNC_ERR_ADDR_LOW is shown in [Figure 1-309](#) and described in [Table 1-320](#).

Uncorrectable Error Address Low

Figure 1-309. UNC_ERR_ADDR_LOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNC_ERR_ADDR_L																															

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-320. UNC_ERR_ADDR_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UNC_ERR_ADDR_L	R/W	0h	64-bit aligned address at which an uncorrectable error occurred in the lower 64-bits of a 128-bit aligned memory.

1.14.22.5 UNC_ERR_ADDR_HIGH Register (offset = 8h) [reset = 0h]

UNC_ERR_ADDR_HIGH is shown in [Figure 1-310](#) and described in [Table 1-321](#).

Uncorrectable Error Address High

Figure 1-310. UNC_ERR_ADDR_HIGH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNC_ERR_ADDR_H																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

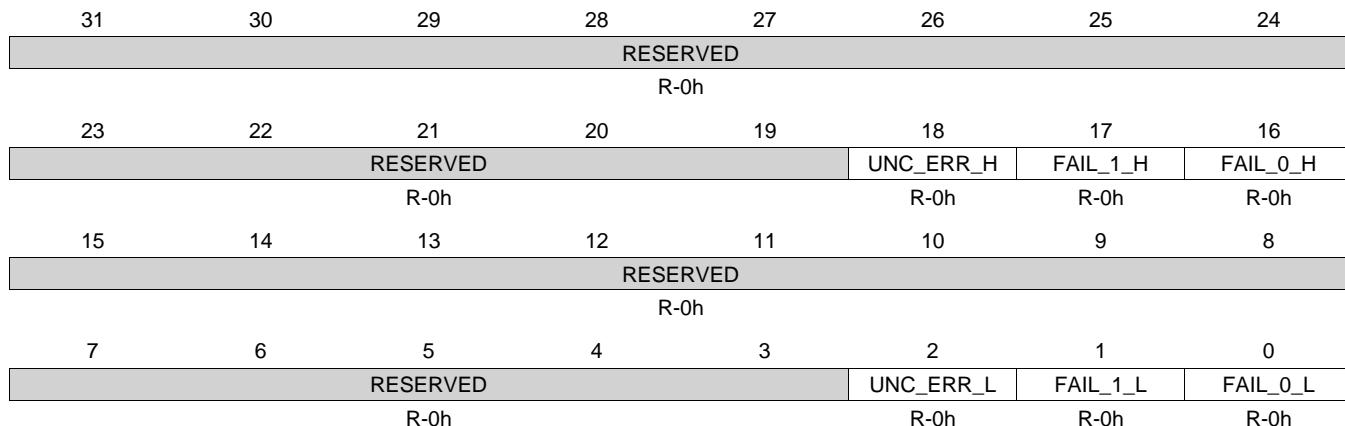
Table 1-321. UNC_ERR_ADDR_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UNC_ERR_ADDR_H	R/W	0h	64-bit aligned address at which an uncorrectable error occurred in the upper 64-bits of a 128-bit aligned memory.

1.14.22.6 ERR_STATUS Register (offset = Ah) [reset = 0h]

ERR_STATUS is shown in [Figure 1-311](#) and described in [Table 1-322](#).

Error Status

Figure 1-311. ERR_STATUS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-322. ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	UNC_ERR_H	R	0h	Uncorrectable error. A value of 1 indicates that an un-correctable error occurred in upper 64bits of a 128-bit aligned address. Cleared by writing a 1 to UNC_ERR_H_CLR bit of ERR_STATUS_CLR register.
17	FAIL_1_H	R	0h	<p>Fail on 1.</p> <p>0 Fail on 1 single bit error did not occur in upper 64bits of a 128-bit aligned address.</p> <p>1 A value of 1 would indicate that a single bit error occurred in upper 64bits of a 128-bit aligned address and the corrected value was 1. Cleared by writing a 1 to FAIL_1_H_CLR bit of ERR_STATUS_CLR register.</p>
16	FAIL_0_H	R	0h	<p>Fail on 0.</p> <p>0 Fail on 0 single bit error did not occur in lower 64bits of a 128-bit aligned address.</p> <p>1 A value of 1 would indicate that a single bit error occurred in lower 64bits of a 128-bit aligned address and the corrected value was 0. Cleared by writing a 1 to FAIL_0_H_CLR bit of ERR_STATUS_CLR register.</p>
15-3	RESERVED	R	0h	Reserved
2	UNC_ERR_L	R	0h	Uncorrectable error. A value of 1 indicates that an un-correctable error occurred in lower 64bits of a 128-bit aligned address. Cleared by writing a 1 to UNC_ERR_L_CLR bit of ERR_STATUS_CLR register.
1	FAIL_1_L	R	0h	<p>Fail on 1.</p> <p>0 Fail on 1 single bit error did not occur in lower 64bits of a 128-bit aligned address.</p> <p>1 A value of 1 would indicate that a single bit error occurred in lower 64bits of a 128-bit aligned address and the corrected value was 1. Cleared by writing a 1 to FAIL_1_L_CLR bit of ERR_STATUS_CLR register.</p>

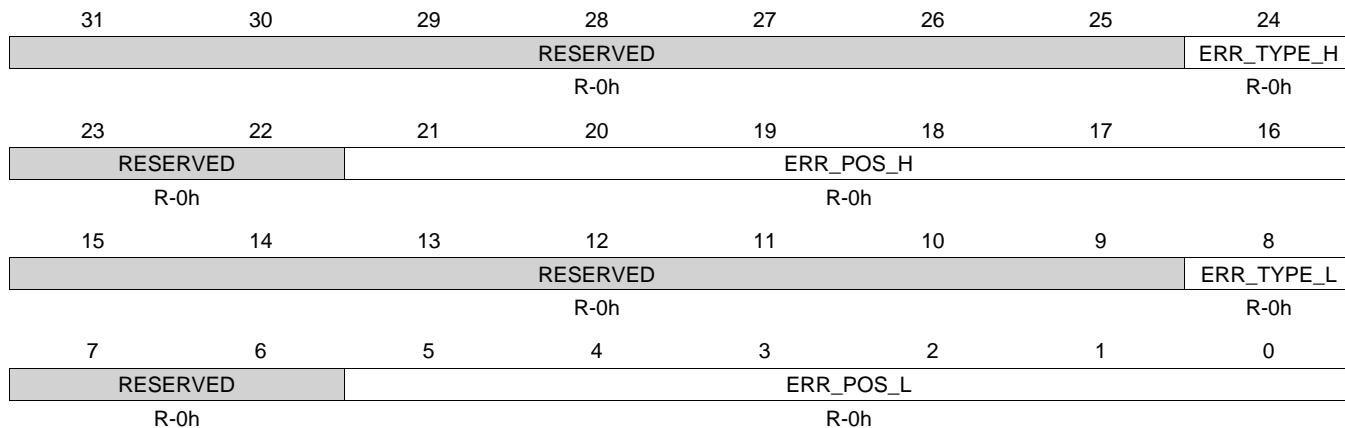
Table 1-322. ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FAIL_0_L	R	0h	<p>Fail on 0.</p> <p>0 Fail on 0 single bit error did not occur in lower 64bits of a 128-bit aligned address.</p> <p>1 A value of 1 would indicate that a single bit error occurred in lower 64bits of a 128-bit aligned address and the corrected value was 0. Cleared by writing a 1 to FAIL_0_L_CLR bit of ERR_STATUS_CLR register.</p>

1.14.22.7 ERR_POS Register (offset = Ch) [reset = 0h]

ERR_POS is shown in [Figure 1-312](#) and described in [Table 1-323](#).

Error Position

Figure 1-312. ERR_POS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

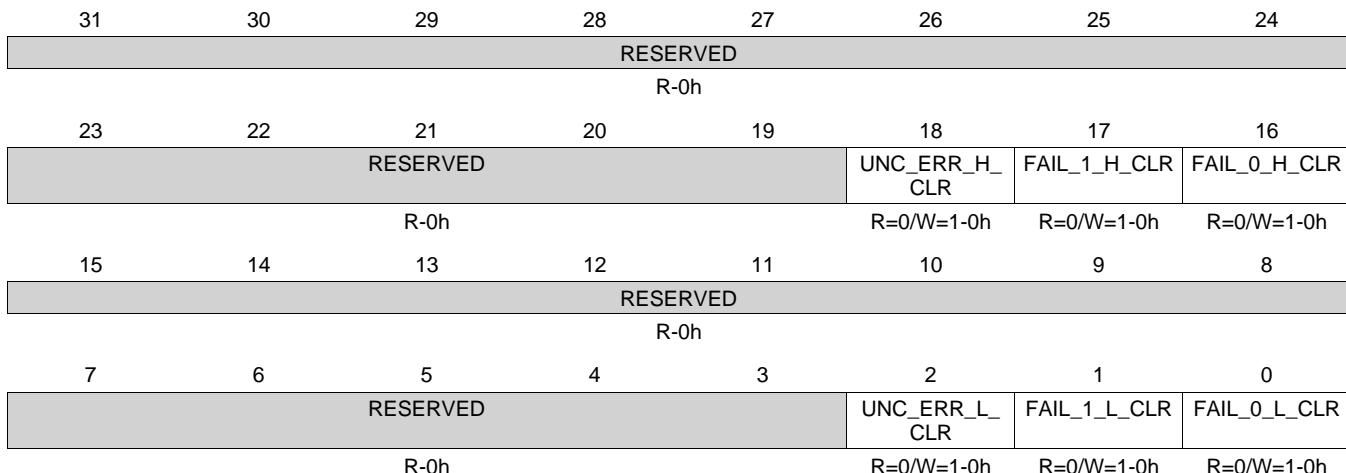
Table 1-323. ERR_POS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	ERR_TYPE_H	R	0h	<p>Error type</p> <p>0 Indicates that a single bit error occurred in upper 64 data bits of a 128-bit aligned address.</p> <p>1 Indicates that a single bit error occurred in ECC check bits of upper 64bits of a 128-bit aligned address.</p>
23-22	RESERVED	R	0h	Reserved
21-16	ERR_POS_H	R	0h	<p>Error position. Bit position of the single bit error in upper 64bits of a 128-bit aligned address. The position is interpreted depending on whether the ERR_TYPE bit indicates a check bit or a data bit. If ERR_TYPE indicates a check bit error, the error position could range from 0 to 7, else it could range from 0 to 63.</p>
15-9	RESERVED	R	0h	Reserved
8	ERR_TYPE_L	R	0h	<p>Error type</p> <p>0 Indicates that a single bit error occurred in lower 64 data bits of a 128-bit aligned address.</p> <p>1 Indicates that a single bit error occurred in ECC check bits of lower 64bits of a 128-bit aligned address.</p>
7-6	RESERVED	R	0h	Reserved
5-0	ERR_POS_L	R	0h	<p>Error position. Bit position of the single bit error in lower 64bits of a 128-bit aligned address. The position is interpreted depending on whether the ERR_TYPE bit indicates a check bit or a data bit. If ERR_TYPE indicates a check bit error, the error position could range from 0 to 7, else it could range from 0 to 63.</p>

1.14.22.8 ERR_STATUS_CLR Register (offset = Eh) [reset = 0h]

ERR_STATUS_CLR is shown in [Figure 1-313](#) and described in [Table 1-324](#).

Error Status Clear

Figure 1-313. ERR_STATUS_CLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-324. ERR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	UNC_ERR_H_CLR	R=0/W=1	0h	Uncorrectable error clear. Writing a 1 to this bit will clear the UNC_ERR_H bit of ERR_STATUS register. Writes of 0 have no effect. Read returns 0.
17	FAIL_1_H_CLR	R=0/W=1	0h	Fail on 1 clear. Writing a 1 to this bit will clear the FAIL_1_H bit of ERR_STATUS register. Writes of 0 have no effect. Read returns 0.
16	FAIL_0_H_CLR	R=0/W=1	0h	Fail on 0 clear. Writing a 1 to this bit will clear the FAIL_0_H bit of ERR_STATUS register. Writes of 0 have no effect. Read returns 0.
15-3	RESERVED	R	0h	Reserved
2	UNC_ERR_L_CLR	R=0/W=1	0h	Uncorrectable error clear. Writing a 1 to this bit will clear the UNC_ERR_L bit of ERR_STATUS register. Writes of 0 have no effect. Read returns 0.
1	FAIL_1_L_CLR	R=0/W=1	0h	Fail on 1 clear. Writing a 1 to this bit will clear the FAIL_1_L bit of ERR_STATUS register. Writes of 0 have no effect. Read returns 0.
0	FAIL_0_L_CLR	R=0/W=1	0h	Fail on 0 clear. Writing a 1 to this bit will clear the FAIL_0_L bit of ERR_STATUS register. Writes of 0 have no effect. Read returns 0.

1.14.22.9 ERR_CNT Register (offset = 10h) [reset = 0h]ERR_CNT is shown in [Figure 1-314](#) and described in [Table 1-325](#).

Error Control

Figure 1-314. ERR_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERR_CNT															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-325. ERR_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ERR_CNT	R/W	0h	Single bit error count. This counter increments with every single bit ECC error occurrence. Upon reaching the threshold value counter stops counting on single bit errors. ERR_CNT can be cleared (irrespective of whether threshold is met or not) using "Single Err Int Clear" bit. This is applicable for ECC logic test mode and normal operational mode. In ECC logic test mode, ERR_CNT will keep incrementing for every cycle after a single bit error occurrence. So, in order to clear ERR_CNT in ECC logic test mode, ECC logic test mode has to be disabled prior to clearing the ERR_CNT using "Single Err Int Clear" bit.

1.14.22.10 ERR_THRESHOLD Register (offset = 12h) [reset = 0h]

ERR_THRESHOLD is shown in [Figure 1-315](#) and described in [Table 1-326](#).

Error Threshold

Figure 1-315. ERR_THRESHOLD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERR_THRESHOLD															

R-0h

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-326. ERR_THRESHOLD Register Field Descriptions

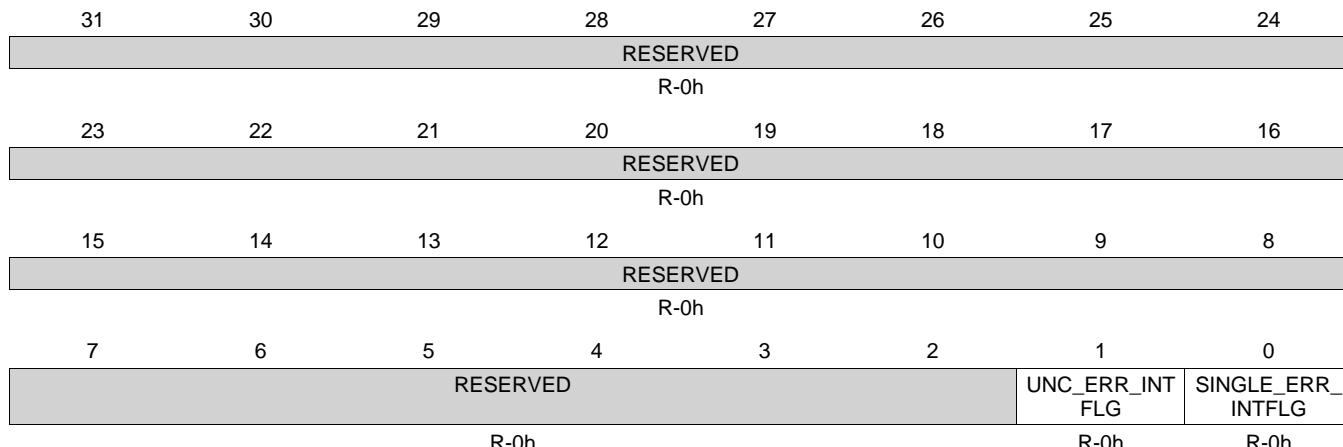
Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ERR_THRESHOLD	R/W	0h	Single bit error threshold. Sets the threshold for single bit errors. When the ERR_CNT value equals the THRESHOLD value and a single bit error occurs, SINGLE_ERR_INT flag is set, and an interrupt is fired.

1.14.22.11 ERR_INTFLG Register (offset = 14h) [reset = 0h]

ERR_INTFLG is shown in [Figure 1-316](#) and described in [Table 1-327](#).

Error Interrupt Flag

Figure 1-316. ERR_INTFLG Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

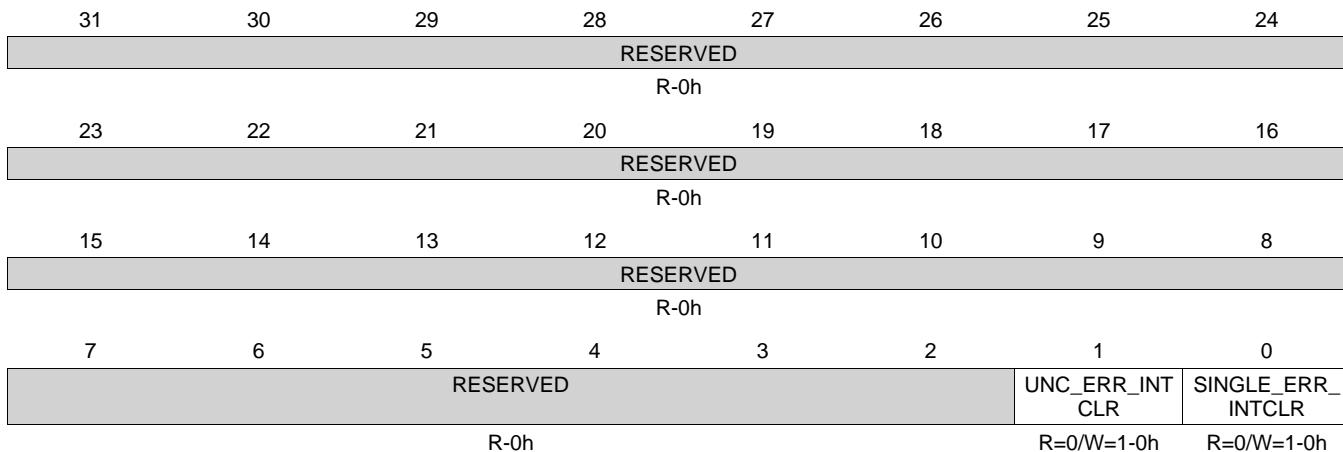
Table 1-327. ERR_INTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	RESERVED	R	0h	Reserved
1	UNC_ERR_INTFLG	R	0h	Uncorrectable bit error interrupt flag. When a Un-correctable error occurs, this bit is set and the UNC_ERR_INT interrupt is fired. When UNC_ERR_INTCLR bit of ERR_INTCLR register is written a value of 1 this bit is cleared.
0	SINGLE_ERR_INTFLG	R	0h	Single bit error interrupt flag. When the ERR_CNT value equals the ERR_THRESHOLD value and a single bit error occurs then SINGLE_ERR_INT flag is set and SINGLE_ERR_INT interrupt is fired. When SINGLE_ERR_INTCLR bit of ERR_INTCLR register is written a value of 1 this bit is cleared.

1.14.22.12 ERR_INTCLR Register (offset = 16h) [reset = 0h]

ERR_INTCLR is shown in [Figure 1-317](#) and described in [Table 1-328](#).

Error Interrupt Flag Clear

Figure 1-317. ERR_INTCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-328. ERR_INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	RESERVED	R	0h	Reserved
1	UNC_ERR_INTCLR	R=0/W=1	0h	Uncorrectable bit error interrupt flag clear. Writing a 1 to this bit will clear UNC_ERR_INT_FLG. Writes of 0 have no effect.
0	SINGLE_ERR_INTCLR	R=0/W=1	0h	Single bit error interrupt flag clear. Writing a 1 to this bit will clear SINGLE_ERR_INT_FLG. Writes of 0 have no effect.

1.14.22.13 FDATAH_TEST Register (offset = 18h) [reset = 0h]

FDATAH_TEST is shown in [Figure 1-318](#) and described in [Table 1-329](#).

Data High Test

Figure 1-318. FDATAH_TEST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDATAH																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-329. FDATAH_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FDATAH	R/W	0h	High double word of selected 64-bit data. User-configurable bits 63:32 of the selected data blocks in ECC test mode.

1.14.22.14 FDATAL_TEST Register (offset = 1Ah) [reset = 0h]

FDATAL_TEST is shown in [Figure 1-319](#) and described in [Table 1-330](#).

Data Low Test

Figure 1-319. FDATAL_TEST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDATAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-330. FDATAL_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FDATAL	R/W	0h	Low double word of selected 64-bit data. User-configurable bits 31:0 of the selected data blocks in ECC test mode.

1.14.22.15 FADDR_TEST Register (offset = 1Ch) [reset = 0h]

FADDR_TEST is shown in [Figure 1-320](#) and described in [Table 1-331](#).

ECC Test Address

Figure 1-320. FADDR_TEST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ADDRH			
R-0h												R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRL												RESERVED			
R/W-0h												R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-331. FADDR_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21-16	ADDRH	R/W	0h	Address for selected 64-bit data. User-configurable address bits of the selected data in ECC test mode. Left-shift the address by one bit (to provide byte address) and ignore the three least significant bits of the address and write the bits 21:16 in remaining address bits in this field.
15-3	ADDRL	R/W	0h	Address for selected 64-bit data. User-configurable address bits of the selected data in ECC test mode. Left-shift the address by one bit (to provide byte address) and ignore the three least significant bits of the address and write the bits 15:3 in remaining address bits in this field.
2-0	RESERVED	R	0h	Reserved

1.14.22.16 FECC_TEST Register (offset = 1Eh) [reset = 0h]

FECC_TEST is shown in [Figure 1-321](#) and described in [Table 1-332](#).

ECC Test Address

Figure 1-321. FECC_TEST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED		ECC					
R-0h																								R-0h		R/W-0h					

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

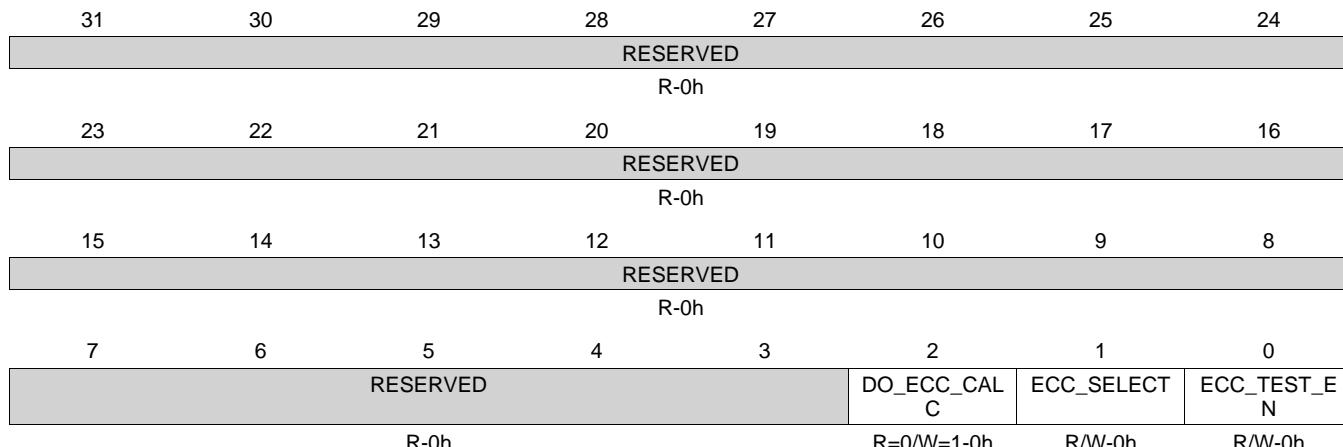
Table 1-332. FECC_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	RESERVED	R	0h	Reserved
7-0	ECC	R/W	0h	8-bit ECC for selected 64-bit data. User-configurable ECC bits of the selected 64-bit data block in ECC test mode.

1.14.22.17 FECC_CTRL Register (offset = 20h) [reset = 0h]

FECC_CTRL is shown in [Figure 1-322](#) and described in [Table 1-333](#).

ECC Control

Figure 1-322. FECC_CTRL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

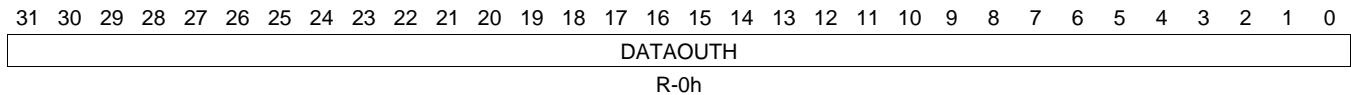
Table 1-333. FECC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-3	RESERVED	R	0h	Reserved
2	DO_ECC_CALC	R=0/W=1	0h	Enable ECC calculation. ECC logic will calculate ECC in one cycle for the data and address written in ECC test registers when ECC test logic is enabled by setting ECC_TEST_EN.
1	ECC_SELECT	R/W	0h	ECC block select. 0 Selects the ECC block on bits [63:0] of bank data. 1 Selects the ECC block on bits [127:64] of bank data.
0	ECC_TEST_EN	R/W	0h	ECC test mode enable. 0 ECC test mode disabled 1 ECC test mode enabled

1.14.22.18 FOUTH_TEST Register (offset = 22h) [reset = 0h]

FOUTH_TEST is shown in [Figure 1-323](#) and described in [Table 1-334](#).

Test Data Out High

Figure 1-323. FOUTH_TEST Register

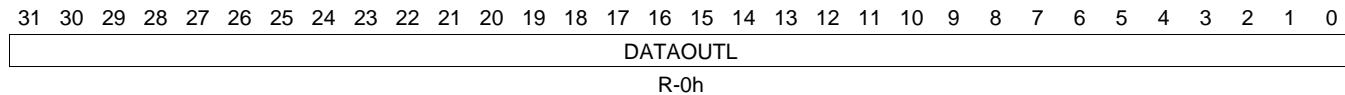
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-334. FOUTH_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATAOUTH	R	0h	High double word test data out. Holds bits 63:32 of the data out of the selected ECC block.

1.14.22.19 FOUTL_TEST Register (offset = 24h) [reset = 0h]FOUTL_TEST is shown in [Figure 1-324](#) and described in [Table 1-335](#).

Test Data Out Low

Figure 1-324. FOUTL_TEST Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

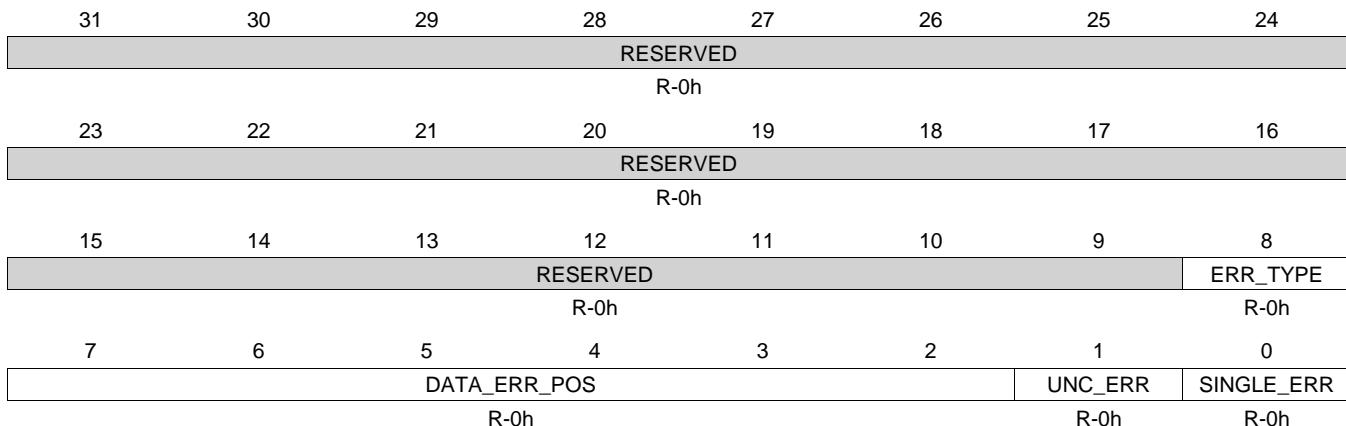
Table 1-335. FOUTL_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATAOUTL	R	0h	Low double word test data out. Holds bits 31:0 of the data out of the selected ECC block.

1.14.22.20 FECC_STATUS Register (offset = 26h) [reset = 0h]

FECC_STATUS is shown in [Figure 1-325](#) and described in [Table 1-336](#).

ECC Status

Figure 1-325. FECC_STATUS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 1-336. FECC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-9	RESERVED	R	0h	Reserved
8	ERR_TYPE	R	0h	Test mode ECC single bit error indicator. When 1, indicates that the single bit error is in check bits. When 0, indicates that the single bit error is in data bits (If SINGLE_ERR field is also set).
7-2	DATA_ERR_POS	R	0h	<p>Test mode single bit error position. Holds the bit position where the single bit error occurred.</p> <p>The position is interpreted depending on whether the CHK_ERR bit indicates a check bit or a data bit. If CHK_ERR indicates a check bit error, the error position could range from 0 to 7, or it could range from 0 to 63.</p>
1	UNC_ERR	R	0h	Test mode ECC double bit error. When 1 indicates that the ECC test resulted in an uncorrectable bit error.
0	SINGLE_ERR	R	0h	Test mode ECC single bit error. When 1 indicates that the ECC test resulted in a single bit error.

ROM Code and Peripheral Booting

This chapter describes the booting functionality of the 2837xD subsystems.

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2.1 Introduction

The purpose of this document is to mainly state the functions and features of boot ROM code and also define the contents and allocated memory map of other ROM(s) in the device.

2.2 Device Boot Philosophy

The system state after an external reset, power up or watchdog reset is as follows:

- CPU1 starts execution from CPU1-Boot ROM
- CPU2 is held in reset

The CPU1 will be the master controller and will also control the boot process. The CPU2 will go through its own boot procedure, but under the control of the CPU1 except when CPU2 is set to boot-to-flash.

Below are the resources used during the boot process:

CPU1-Boot ROM	Code execution starts from this ROM after reset.
CPU1 OTP	This OTP contains the device configuration; security configuration and analog trim information that is used during boot process.
CPU2 OTP	This OTP contains device calibration stuff for CPU2
CPU BOOT ROM	Code execution starts from this ROM for the CPU2 after being released from reset by the CPU1.
C1toC and C2toC1 IPC	Registers used by CPU1 to communicate to CPU2 during boot process and vice-versa

The CPU1 has no direct access to registers on the CPU2 side. Therefore, IPC registers are used to allow CPU1 to communicate to the CPU2 during boot process.

Each core polls for IPC commands that it supports and performs simple actions as indicated below. IPC commands supported by each core will be explained in detail later in this document.

- Perform 8/16/32-bit read, write, read-modify-write operations to specified address locations
- Branch to specified address and does not return (supported only on CPU2).
- Call a function and return (supported only on CPU2)

In the IPC, a command (xIPCCOM), address (xIPCAADDR), data write (xIPCDATAW) and data read (xIPCDATAR) register is provided that is initialized by the CPUx before starting a communication.

In addition, the xBOOTSTS and xBOOTMODE registers are used by the CPU1 and CPU2 to determine the current state and also synchronize actions during the boot process.

2.3 Device Clocking on Power-up and Boot Time

Device (both CPU1 and CPU2) boots up with INTOSC2 as the default clock source unless there is a missing clock detected at power up or right after device reset, in which case device will boot up with INTOSC1 as the clock source.

2.4 Clock Configurations in Boot ROM

This section describes the clock configurations done in boot ROM. All the below configurations are done only for a POR or XRSn or HIBRESETn reset types. For all other resets boot ROM starts executing with the clocks that are already setup before reset.

2.4.1 CPU1-Boot ROM Clocking Configuration

PLL is bypassed by default on POR or XRSn or HIBRESETn and default SYSDIVSEL is set to /4 by design.

Boot ROM does the following things to assist fast boot time response.

- Set the SYSDIVSEL divider to a /1
- Power up PLL and set an integer multiplier. Configure flash wrapper for faster flash power-up (see [Section 2.5](#))

- Check PLL Lock status and put PLL output in clock path

PLL multiplier and divider decisions are based on the below reasoning:

- Need to use PLL for better boot time response
- PLL Fout range is 150-550 MHz, the multiplier chosen should make sure of that by taking the max/min clock frequency that could be available during worst case and best case.

Note that CPU1-Boot ROM writes to the PLL multiplier and enables PLL before accessing Flash, the PLL lock time of 125uS is more than the Flash wake up time, so by the time Flash is powered up and ready PLL would have locked. After Flash is powered up CPU1-Boot ROM looks at PLL LOCK Status and puts the PLLOUTPUT in clock path, else PLLOUTPUT is not used in clock path.

NOTE: PLL if used during boot process, will be bypassed by bootROM before branching to the application.

2.4.2 CPU2-Boot ROM Clocking Configuration

There is no clock configuration done in CPU2-Boot ROM.

2.5 Faster Flash Power Up

This section describes the optimizations done in boot ROM for RWAIT and PSLEEP values in Flash wrapper for faster Flash power up during boot. The modifications/optimizations are done only for POR, XRSn or HIBRESETn reset types.

The first access to Flash after POR/XRSn/HIBRESETn will wake up the Flash and until Flash wakes up or is ready, CPU will stall.

CPU1-Boot ROM modifies PSLEEP to 0x120 and RWAIT to 0x3 before accessing Flash. After Flash is powered up the RWAIT is set back to 0xF and PSLEEP to 0x860.

CPU2-Boot ROM – the RWAIT is modified to 0x3 before accessing Flash and set back to 0xF after the bank powers up. PSLEEP is not modified because by the time CPU2-Boot ROM accesses its own Flash bank the pump is already powered up by CPU1-Boot ROM. So there is no need of modifying PSLEEP.

2.6 Boot ROM DCSM init Sequence

2.6.1 CPU1 DCSM init Sequence

As per the device DCSM spec:

- Read triple link pointers
- Decode link pointer
- Read Zx BOOT MODE
- Read SECDC
- Read the Zx DCSM block

2.6.2 CPU2 DCSM init Sequence

As per the device DCSM spec:

- Read triple link pointers
- Decode link pointer
- Read Zx BOOT MODE
- Read SECDC
- Read the Zx DCSM block

2.7 Device Calibration on CPU1

This applies to CPU1 only.

Below are the analog modules that needs trimming.

- PMM
- OSC
- ADC
- COMP

All the TRIMS are reset by XRSn, so each time device boot ROM is executed after an XRSn the TRIMS are supposed to be loaded.

After a HIBRESETn, the device will be running on previously loaded TRIMS until RESC.HIBRESETn is cleared even after OTP TRIMs are loaded by boot ROM.

ADC and COMP TRIMS are loaded by the DEVICECAL function. This function executes from TI-OTP.

PMM and OSC TRIMs, however, are to be loaded by boot code. Before loading PMM and OSC TRIMs, boot ROM checks for specific keys in TI-OTP and loads the TRIMs only if the KEY matches the expected value.

PMM TRIM load code:

```
#define TI OTP_PMM_LC_TRIM_KEY           (Uint16)(*(volatile Uint16 *)(Uint32)(0x70274))

{
    if(TI OTP_PMM_LC_TRIM_KEY != 0x5A5A)
        return;

    EALLOW;
    AnalogSubsysRegs.PMMREFTRIM.all = TI OTP_PMM_LC_BGSLOPE_VAL_IREF_TRIM;
    AnalogSubsysRegs.PMMVREGTRIM.all = TI OTP_PMM_LC_VREG_TRIM;          //this loads both VSINK
and VREG and VREG2 TRIM
    AnalogSubsysRegs.PMMVMONTRIM.all = TI OTP_PMM_LC_VMON_TRIM;
    EDIS;

}
```

OSC TRIM load code:-

```
#define TI OTP_OSC_TRIM_KEY           (Uint16)(*(volatile Uint16 *)(Uint32)(0x70275))

{
    if(TI OTP_OSC_TRIM_KEY != 0x5A5A)
        return;

    EALLOW;
    AnalogSubsysRegs.OSCREFTRIM.all = TI OTP_OSC_REF_TRIM;
    AnalogSubsysRegs.INTOSC1TRIM.all = TI OTP_OSC1_TRIM;
    AnalogSubsysRegs.INTOSC2TRIM.all = TI OTP_OSC2_TRIM;
    EDIS;
```

2.8 CPU1-Boot ROM Procedure

CPU1-Boot ROM is executed each time CPU1 core is reset. CPU1 acts as master system in the device controlling the overall boot process on CPU2 system. If booting from one of the bootable peripherals then CPU1-Boot ROM gets the application code to be run on CPU1 and loads into device RAMs (M0, M1, LS0-LS5, D0, D1, and GS0-GS15 shared RAM) and starts the CPU1 application. It is the responsibility of CPU1 user application to either move the code from CPU1 RAMs to CPU2 RAM(s) or kick start its own peripheral loaders using CPU2-Boot ROM IPC.

- CPU1-Boot ROM will program device configuration registers on the device from OTP as define in OTP spec.
- CPU1-Boot ROM will execute DCSM and OTPJTAGLOCK sequences as specified in device DCSM

spec

- CPU1-Boot ROM will check for FUSEERR register to check for any errors, and take appropriate action.
- CPU1-Boot ROM will do RAM-INIT of all CPU1 RAM(s) to initialize ECC/PARITY on the POR or after the HIBERNATE Reset.
- CPU1-Boot ROM will handle the exceptions/NMI which are enabled by default on reset. How CPU1-Boot ROM handles these is explained later in the document.
- CPU1-Boot ROM should bring CPU2 out of RESET as part of device initialization process and irrespective of whether it is booting from Flash or not.
- CPU1-Boot ROM after system initialization polls BOOTMODE GPIO to boot from Flash/SRAM/peripherals.
- CPU1-Boot ROM will update the boot status of core to application a specific RAM location. CPU1 applications can read this RAM location and find out more about device boot status or health status, description of boot status to app is explained later in this document.
- If device is set to boot from Flash, then CPU1-Boot ROM just starts the application in CPU1 Flash. It is the responsibility of application in Flash to program/start CPU1 core. CPU1-Boot ROM just does the needful to make sure both CPU2-Boot ROM is ready to accept BOOTMODE commands and IPC commands from Master system.
- CPU1-Boot ROM will not try to start any application on CPU2 system. Only CPU1 application is allowed to start the application on CPU2 system.
- CPU1-Boot ROM when in WAIT BOOT MODE supports predefined IPC commands to allow for easier test application development on CPU2.

2.9 CPU2-Boot ROM Procedure

On Power up CPU2 system will be held in reset until CPU1-Boot ROM brings it out of reset, when CPU2 is out of reset it will start executing code from CPU2-Boot ROM memory. Each time CPU2 is reset CPU2-Boot ROM is executed and depending on the reset cause CPU2-Boot ROM will take actions as explained in further below in this document.

- CPU2-Boot ROM on start up initializes CPU2 sub system, performs RAM-INIT as per the RESC, installs PIE interrupt handlers to serve IPC commands from Master system and goes to IDLE mode.
- CPU2-Boot ROM is allowed to boot to Flash when boot mode is set to boot-to-flash, to allow Checker Micro kind of applications on CPU2.
- CPU2-Boot ROM is allowed to boot to Flash when boot mode is set to boot-to-flash, to allow Checker Micro kind of applications on CPU2.
- CPU1 application before starting CPU2 peripheral boot, is supposed to configure all the IOs and the peripheral ownership after checking if the peripheral is existing in the current device part number (DCx register check). CPU2 cannot read any of these status so it will simply try to boot from the peripheral or IO.

Please refer to the flow chart for the CPU2-Boot ROM procedure.

2.10 Boot Modes Supported on CPU1

Device allows users to download their application on to RAM using the following boot mode configurations. Boot loader uses boot mode GPIO to know from which peripheral to boot from.

CPU1-Boot ROM is responsible to decode the boot mode by reading the boot mode GPIO as defined in the below table. After CPU1-Boot ROM loads/starts CPU1-Application in CPU1-Flash/RAM it is the responsibility of the application to start the user application on CPU2. CPU2-Boot ROM supported both peripheral boot loading and boot from Flash options using IPC commands.

CPU1-Boot ROM boot loader supports booting from:

- CPU1 Flash
- SCI
- SPI
- I2C

- CPU1-RAM
- CAN
- USB

Note: All the peripheral boots supported on CPU1/CPU2 are on primary peripherals (SCIA, SPIA, I2CA, CANA, and so on). So whenever SCIBOOT is referred to in this chapter, it actually means SCIA Boot or Boot on SCIA port. The same is applied for other peripheral boots as well.

Peripheral boot loading will be supported on CPU2-Boot ROM but CPU1 application will have to configure the peripheral and IOs appropriately before sending the boot mode IPC command.

Table 2-1. Device Boot Mode – Decoded by CPU1

Mode No	CPU1 Boot Mode	CPU2 Boot Mode	TRSTn	GPIO72 (boot mode pin 1)	GPIO84 (boot mode pin 0)	Supported in Version 1.0
0	Parallel IO	Boot from Master	0	0	0	Yes
1	SCI Mode	Boot from Master	0	0	1	Yes
2	Wait Boot Mode	Boot from master	0	1	0	Yes
3	Get Mode	Boot from Master	0	1	1	Yes
4-7	EMU Boot Mode (Emulator Connected)	Boot from Master	1	X	X	Yes

Booting from device COM peripherals will follow the same format and protocol as supported in Piccolo class devices.

- Mode EMU (modes 4 thru 7): When TRSTn is HIGH, debugger is connected and the boot ROM determines the boot mode from the first two locations (reset vector) in the PIE vector table.

The definition of EMU_BMODE and EMU_KEY is as below:- 32 bits from 0xD00. This definition is similar to the Zx-BOOTCTRL register definition in OTP and the reason for defining this similar to the Zx-BOOTCTRL is to allow users emulate the device boot with debugger connected before they go ahead and program the OTP with final values.

Table 2-2. EMU_BOOTCTRL Definition: - @ 0xD00 for CPU1 (32 bit word)

Bits	Name	Type	Reset	Description
7:0	EMU_KEY	R/W	X	Use 0x5A to indicate validity of this location values.
15:8	EMU_BMODE	R/W	X	Use this field to define up to 256 boot modes
23:16	EMU_BOOTPIN0	R/W	X	0 -> Pick the default boot pin-0 1 -> Pick GPIO0 as boot pin-0 2 -> Pick GPIO1 as boot pin-0 255 -> Pick GPIO255 as boot pin-0
31:24	EMU_BOOTPIN1	R/W	X	0 -> Pick the default boot pin-1 1 -> Pick GPIO0 as boot pin-1 2 -> Pick GPIO1 as boot pin-1 255 -> Pick GPIO255 as boot pin-1

EMU_BMODE/EMU_KEY will be populated with the boot mode by the boot ROM when powering up with TRSTn = 0.

Above locations can also be initialized manually by the user through the debugger. The value in EMU_KEY must also be initialized to indicate EMU_BMODE is valid. To do this, the boot ROM, or user, will write 0x5A to EMU_KEY. This is to help avoid treating random data in EMU_BMODE as a boot mode. An invalid key or mode will result in “wait” which is the safest mode.

The EMU_BOOTPIN0 and EMU_BOOTPIN1 are provided for users to emulate the device behavior with debugger connected before programming the OTP with final values in case they are choosing a different boot mode pins other than the factory chosen ones. If a customer is choosing the factory default ones then they can leave EMU_BOOTPIN0 and EMU_BOOTPIN1 un-programmed, the boot ROM decides whether to look at these values or not based on the EMU_BMODE value as per the table given below.

Table 2-3. Emulation Boot (TRSTn == 1)

EMU_KEY	EMU_BMODE	EMU_BOOTPIN1	EMU_BOOTPIN0	Realized Boot Mode	CPU1/CPU2	
!= 0x5A	Don't Care	Don't Care	Don't Care	WAIT BOOT	Both	
0x5A	0xFE	Valid (pin decode as per table 13-2)	Valid (pin decode as per table 13-2)	Boot as per EMU_BOOTPIN0 and EMU_BOOTPIN1	CPU1 only	
		0	0	Parallel BOOT		
		0	1	SCI BOOT0		
		1	0	WAIT BOOT		
		1	1	GET MODE (read OTP Zx-BOOTCTRL)		
	0xFF	Don't Care	Don't Care	Emulate CPU1 Stand alone boot (TRSTn == 0)	Both	
		0x00	Don't Care	Don't Care	Parallel BOOT	Both
		0x01	Don't Care	Don't Care	SCI BOOT0	Both
		0x02	Don't Care	Don't Care	WAIT BOOT	Both
		0x03	Don't Care	Don't Care	GET MODE (read OTP Zx-BOOTCTRL)	Both
		0x04	Don't Care	Don't Care	SPI BOOT0	Both
		0x05	Don't Care	Don't Care	I2C BOOT0	Both
		0x07	Don't Care	Don't Care	CAN BOOT0	Both
		0x0A	Don't Care	Don't Care	RAM BOOT	Both
		0x0B	Don't Care	Don't Care	FLASH BOOT	Both
		0x0C	Don't Care	Don't Care	USB BOOT	CPU1 ONLY
0x81		Don't Care	Don't Care	SCI BOOT1	CPU1 ONLY	
0x84		Don't Care	Don't Care	SPI BOOT1	CPU1 ONLY	
0x85		Don't Care	Don't Care	I2C BOOT1	CPU1 ONLY	
0x87		Don't Care	Don't Care	CAN BOOT1	CPU1 ONLY	
0x47	Don't Care	Don't Care	CAN BOOT TEST MODE0	Both		
0xC7	Don't Care	Don't Care	CAN BOOT TEST MODE1	CPU1 ONLY		
Other	Don't Care	Don't Care	WAIT BOOT	Both		

The customer can modify EMU_KEY and EMU_BMODE to change the boot mode via the debugger. A typical debug sequence would be:

1. Power the device, TRSTn = 0.

Configure the chosen boot mode pins for mode 0 – “wait”. This mode emulates a wait-in-reset mode. The boot ROM will loop, allowing the debugger a chance to connect without the eCSL tripping. This will also keep any application code from starting. During this time, the boot ROM will also populate EMU_KEY with 0x5A and EMU_BMODE with WAIT_BOOT.

2. Connect the debugger, TRSTn goes high.

Via the debugger change EMU_BMODE to the desired boot mode. For example, during debug you may want to use “boot to RAM”. To achieve this, load EMU_BMODE with 0x000A.

The EMU_KEY should already be initialized by the boot ROM to 0x5A.

NOTE: TI will be updating the header file peripheral examples that run from SARAM to load EMU_BMODE with "RAM_BOOT" when the code is loaded. In this case, step 2 will simply be to load the code.

3. Perform a debugger reset and run.
 4. The boot ROM will detect TRSTn high and will use EMU_KEY and EMU_BMODE to determine the boot mode.
- If either EMU_KEY or EMU_BMODE is invalid, then the mode will be 'wait'.

NOTE: The behavior of emulators with regards to TRSTn differs. This must be documented clearly.

Some emulators will pull TRSTn high only when Code Composer Studio™ is in a connected state. For these emulators, if Code Composer Studio is disconnected, TRSTn will return to a low state. With Code Composer Studio disconnected, boot mode 0 and boot mode 1 pins (ref. to above boot mode table) will be used to determine the boot mode. On these emulators, this is true even if the emulator pod is physically connected.

Some emulators will pull TRSTn high when Code Composer Studio connects and leave it high as long as the power sense pin is active. TRSTn will remain high even after CCS disconnects. For these emulators, the EMU mode stored in RAM will be used unless the target is power cycled, causing the state of TRSTn to reset back to a low state.

The following modes are available when TRSTn = 0.

In this case the boot mode pins are used to determine the boot mode of the device. The factory default boot mode pins are GPIO84 (boot mode pin 0) and GPIO 72 (boot mode pin 1). You are allowed to choose a different boot mode pin combination by programming the Zx-BOOTCTRL register as shown in [Table 2-4](#).

Table 2-4. BOOTCTRL Register Bit Definition for CPU1⁽¹⁾

Bits	Name	Type	Reset	Description
7:0	OTP_KEY	R	0	Use 0x5A to indicate validity of this register.
15:8	OTP_BMODE	R	0	Use this field to define up to 256 boot modes
23:16	OTP_BOOTPIN0	R	0	0 -> Pick the default boot pin-0 1 -> Pick GPIO0 as boot pin-0 2 -> Pick GPIO1 as boot pin-0 255 -> Pick GPIO255 as boot pin-0
31:24	OTP_BOOTPIN1	R	0	0 -> Pick the default boot pin-1 1 -> Pick GPIO0 as boot pin-1 2 -> Pick GPIO1 as boot pin-1 255 -> Pick GPIO255 as boot pin-1

⁽¹⁾ Refer to the DCSM chapter for the address of this location in the user OTP.

Table 2-5. BOOTCTRL Register Bit Definition for CPU2⁽¹⁾

Bits	Name	Type	Reset	Description
7:0	OTP_KEY	R	0	Use 0x5A to indicate validity of this register.
15:8	OTP_BMODE	R	0	Use this field to define up to 256 boot modes
23:16	Reserved	R	0	Reserved for future use

⁽¹⁾ Refer to the DCSM chapter for the address of this location in the user OTP.

Table 2-5. BOOTCTRL Register Bit Definition for CPU2⁽¹⁾ (continued)

Bits	Name	Type	Reset	Description
31:2 4	Reserved	R	0	Reserved for future use

- Mode 2: “wait” This is to emulate a wait-in-reset mode. This is used when bringing up a debugger on a device with the CSM passwords programmed. This mode writes WAIT_BOOT to EMU_BMODE. This mode enables the PIE on CPU1 and installs C2toC1IPC interrupt handler and loops infinitely.

NOTE: CPU1 WAIT_BOOT mode has a hidden feature where in by configuring OTP_BOOT_CONFIGURE_WORD properly TI could tell it to enable C2toC1IPC handler to let CPU2 application code send IPC commands to CPU1 asking it to configure.

- Mode 1: SCI – a common method for programming fresh devices and the System Apps group uses it for interacting with the device during demonstrations. This mode writes SCI_BOOT to the EMU_BMODE.
- Mode 0: Parallel I/O 8-bit. This will be used by production programmers. For example, Data I/O and BP use this mode. This mode writes PARALLEL_IO_BOOT to EMU_BMODE.
- Mode 3: Get Mode. On a fresh, un-programmed, device this mode will always boot to Flash. On a programmed device, the user can program the values into Zx-BOOTCTRL location in the user OTP to change the behavior. This mode writes GET_BOOT to EMU_BMODE.

The values used by the Get_mode() function are as follows:

Note that GETMODE can be entered when emulator is connected as well as will be shown further below in the document. The boot mode decoding for Get Mode when emulator is connected is as shown below.

Table 2-6. Get Mode Decoding on CPU1

OTP_KEY	OTP_BMODE	Realized Boot Mode When TRSTn == 0	Realized Boot Mode When TRSTn == 1
!= 0X5A	Don't Care	FLASH BOOT	FLASH BOOT
0x5A	0x00	Parallel BOOT	Parallel BOOT
	0x01	SCI BOOT0	SCI BOOT0
	0x02	WAIT BOOT	WAIT BOOT
	0x04	SPI BOOT	SPI BOOT0
	0x05	I2C BOOT	I2C BOOT0
	0x07	CAN BOOT	CAN BOOT0
	0x0A	RAM BOOT	RAM BOOT
	0x0B	FLASH BOOT	FLASH BOOT
	0x0C	USB BOOT	USB BOOT
	0x81	SCI BOOT1	SCI BOOT1
	0x84	SPI BOOT1	SPI BOOT1
	0x85	I2C BOOT1	I2C BOOT1
	0x87	CAN BOOT1	CAN BOOT1
	0x47	CAN BOOT TEST0 IOs (special mode which tx frames for bit rate sync up)	CAN BOOT TEST1 (special mode which tx frames for bit rate sync up)
	0xC7	CAN BOOT TEST1 (special mode which tx frames for bit rate sync up)	CAN BOOT TEST1 (special mode which tx frames for bit rate sync up)
	Other	FLASH BOOT	WAIT BOOT

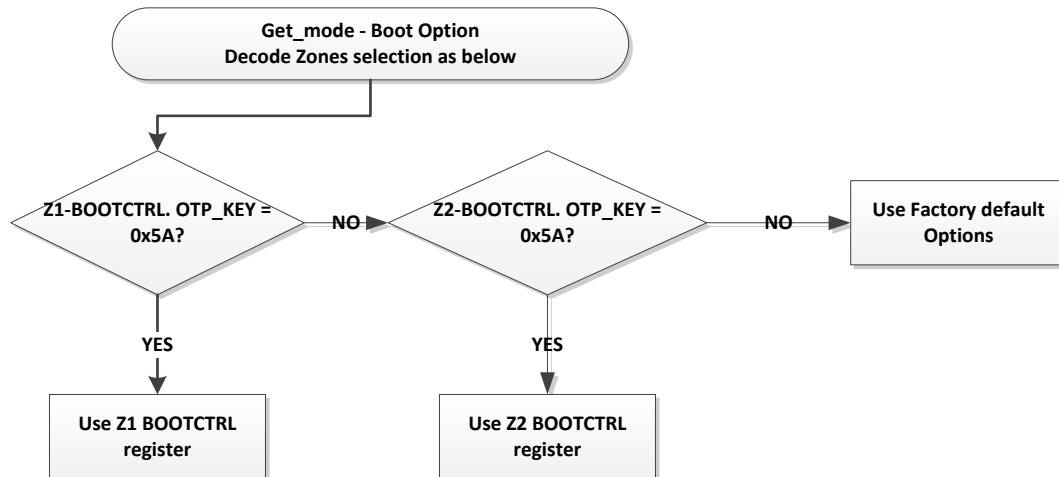
Table 2-7. Get Mode Decoding on CPU2

OTP_KEY	OTP_BMODE	Realized Boot Mode When TRSTn == 0	Realized Boot Mode When TRSTn == 1	Special Cases?
!= 0X5A	Don't Care	WAIT BOOT	WAIT BOOT	N/A

Table 2-7. Get Mode Decoding on CPU2 (continued)

OTP_KEY	OTP_BMODE	Realized Boot Mode When TRSTn == 0	Realized Boot Mode When TRSTn == 1	Special Cases?
0x5A	0x0A	RAM BOOT	RAM BOOT	Only in HIBRESC case, all other reset causes this will default to WAIT BOOT
	0x0B	FLASH BOOT	FLASH BOOT	N/A
	Other	WAIT BOOT	WAIT BOOT	N/A

On this device there are two CSM Zones, Z1 and Z2 each with their own copy of Zx-BOOTCTRL register, boot ROM uses below procedure to identify which one to choose. By default if Z1 is programmed then Z1 is given preference, else Z2. If neither are programmed then factory default options are chosen.

Figure 2-1. BOOTCTRL Selection (applies to both the CPUs)

Mode 0, 1, 2 and 3 result in the following boot modes when TRSTn = 0:

Table 2-8. Stand Alone Boot Modes With TRSTn = 0 (on CPU1)

TRSTn	EMU_BOOTCTRL	OTP_KEY	OTP_BOOTPIN1	OTP_BOOTPIN0	OTP_BMODE	Boot Mode
0	Don't care	!=0x5A	default GPIO72	default GPIO84		
			0	0	Don't care	PARALLEL BOOT
			0	1	Don't care	SCI BOOT
			1	0	Don't care	WAIT BOOT
			1	1	Don't care (no key match)	GET BOOT → FLASH BOOT
		0x5A	User Chosen Boot Pin 1	User Chosen Boot pin 0		
			0	0	Don't care	PARALLEL BOOT
			0	1	Don't care	SCI BOOT
			1	0	Don't care	WAIT BOOT
			1	1	GET MODE (as per Table 2-6) ⁽¹⁾	

⁽¹⁾ Get Mode indicates the boot mode was derived from the values programmed in the OTP_KEY and OTP_BMODE locations, read by boot ROM init process and loaded into BOOTMODE register.

2.11 Boot Modes Supported on CPU2

On CPU2, both EMU-BOOT mode ($\text{TRSTn} == 1$) and stand-alone boot modes ($\text{TRSTn} == 0$) are supported similar to CPU1 except that CPU2 doesn't support decoding of any boot mode GPIO pins and instead reads the OTP Zx-BOOTCTRL register to see if boot-to-flash is selected and if not selected then IPC interrupt is enabled and CPU is put to IDLE mode.

When CPU2-Boot ROM is run with emulator connected, similar to CPU1, the EMUBOOTCTRL location (0xD00 – 32 bits) is used to by boot ROM to know how to boot.

Table 2-9. EMU_BOOTCTRL Definition: - @ 0xD00 for CPU2

Bits	Name	Type	Reset	Description
7:0	EMU_KEY	R	0	Use 0x5A to indicate validity of this register.
15:8	EMu_BMODE	R	0	Use this field to define up to 256 boot modes
23:1 6	Reserved	R	0	0 -> Pick the default boot pin-0
31:2 4	Reserved	R	0	0 -> Pick the default boot pin-1

Below are the EMU Boot modes supported by CPU2, note that there is no USB boot support on CPU2.

Table 2-10. Emulation Boot ($\text{TRSTn} == 1$) – CPU2

EMU_KEY	EMU_BMODE	EMU_BOOTPIN1	EMU_BOOTPINO	Realized Boot Mode
!= 0X5A	Don't Care	Don't Care	Don't Care	WAIT BOOT
0x5A	0xFF	Don't Care	Don't Care	Emulate CPU2 Stand alone boot ($\text{TRSTn} == 0$)
	0x00	Don't Care	Don't Care	Parallel BOOT
	0x01	Don't Care	Don't Care	SCI BOOT
	0x02	Don't Care	Don't Care	WAIT BOOT
	0x03	Don't Care	Don't Care	GET MODE (as shown in Table 2-7)
	0x04	Don't Care	Don't Care	SPI BOOT
	0x05	Don't Care	Don't Care	I2C BOOT
	0x06	Don't Care	Don't Care	WAIT BOOT
	0x07	Don't Care	Don't Care	CAN BOOT
	0x0A	Don't Care	Don't Care	RAM BOOT
	0x0B	Don't Care	Don't Care	FLASH BOOT
	Other	Don't Care	Don't Care	WAIT BOOT

Stand alone boot on CPU2 support is shown in [Table 2-11](#).

Table 2-11. Stand Alone Boot Options on CPU2

TRSTn	EMU_BOOTCT RL	OTP_KEY	OTP_BMODE	Realized Boot Mode
0	Don't care	!=0x5A	Don't care	WAIT BOOT
		0x5A	XXXX	As shown in GET MODE Table 2-7

WAIT MODE on CPU2:

Enable C1 to C2 PIE interrupt handler and enter IDLE mode with WDOG disabled.

2.12 CPU1-Boot ROM Flow Chart

Figure 2-2. Flow Chart (part 1)

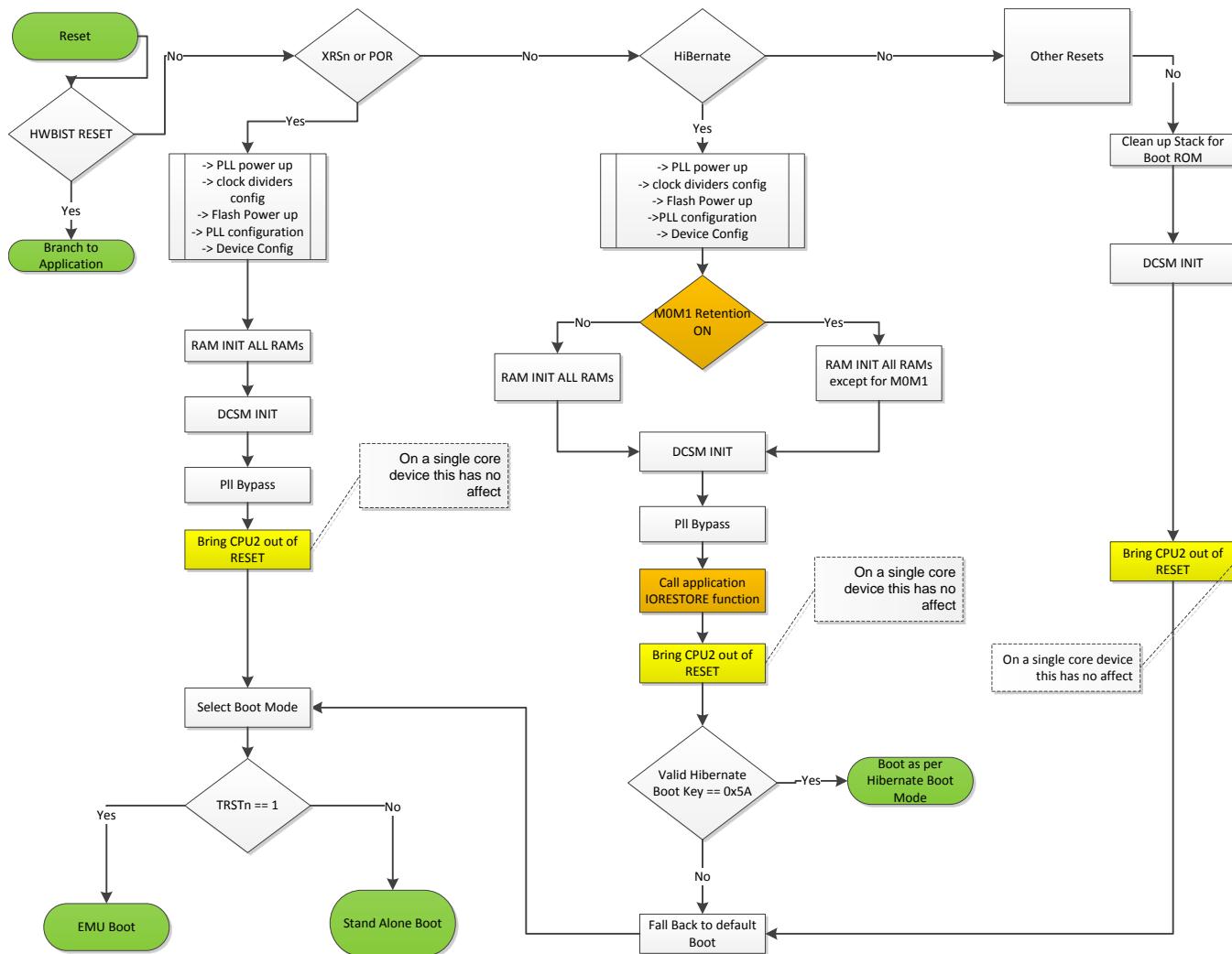


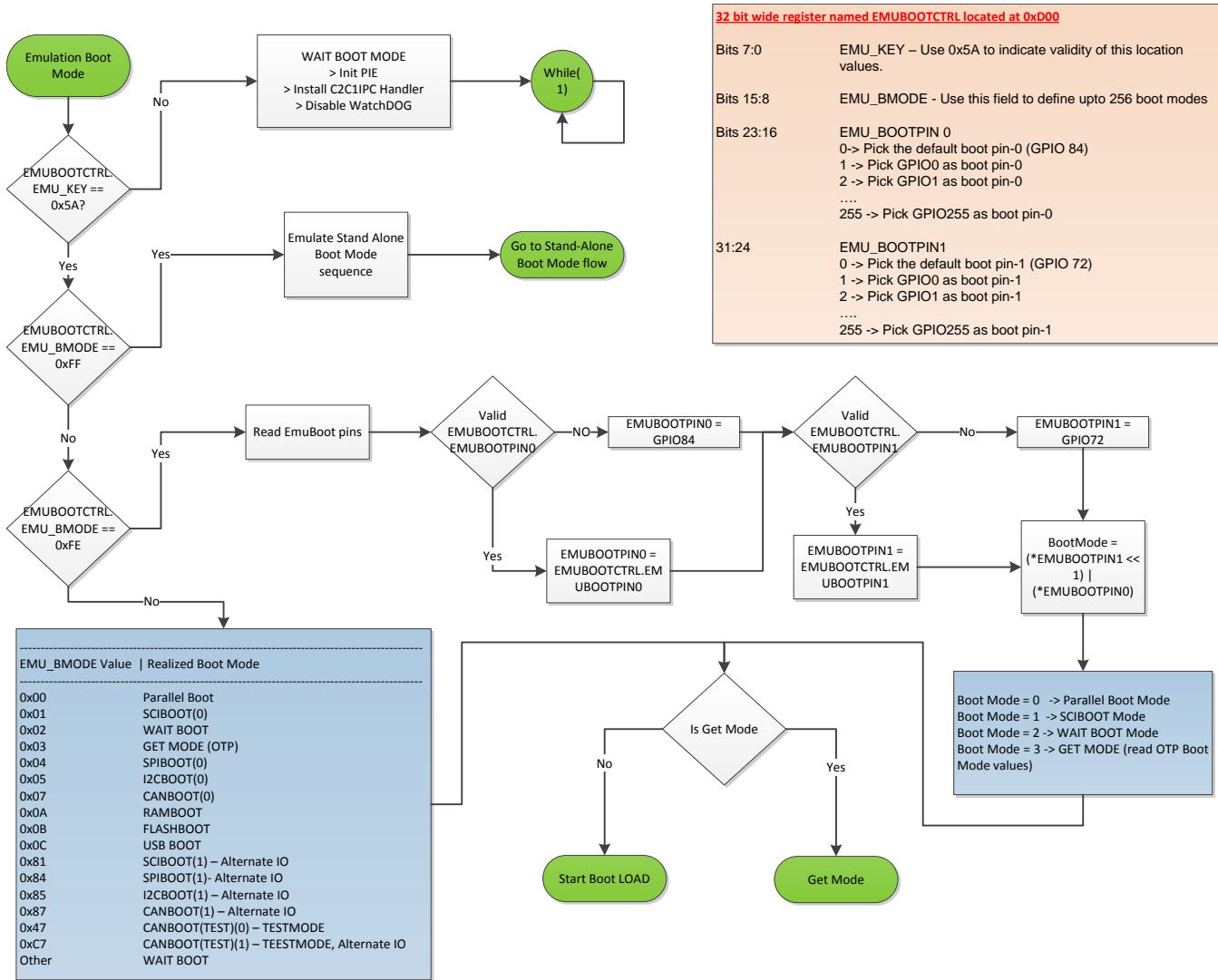
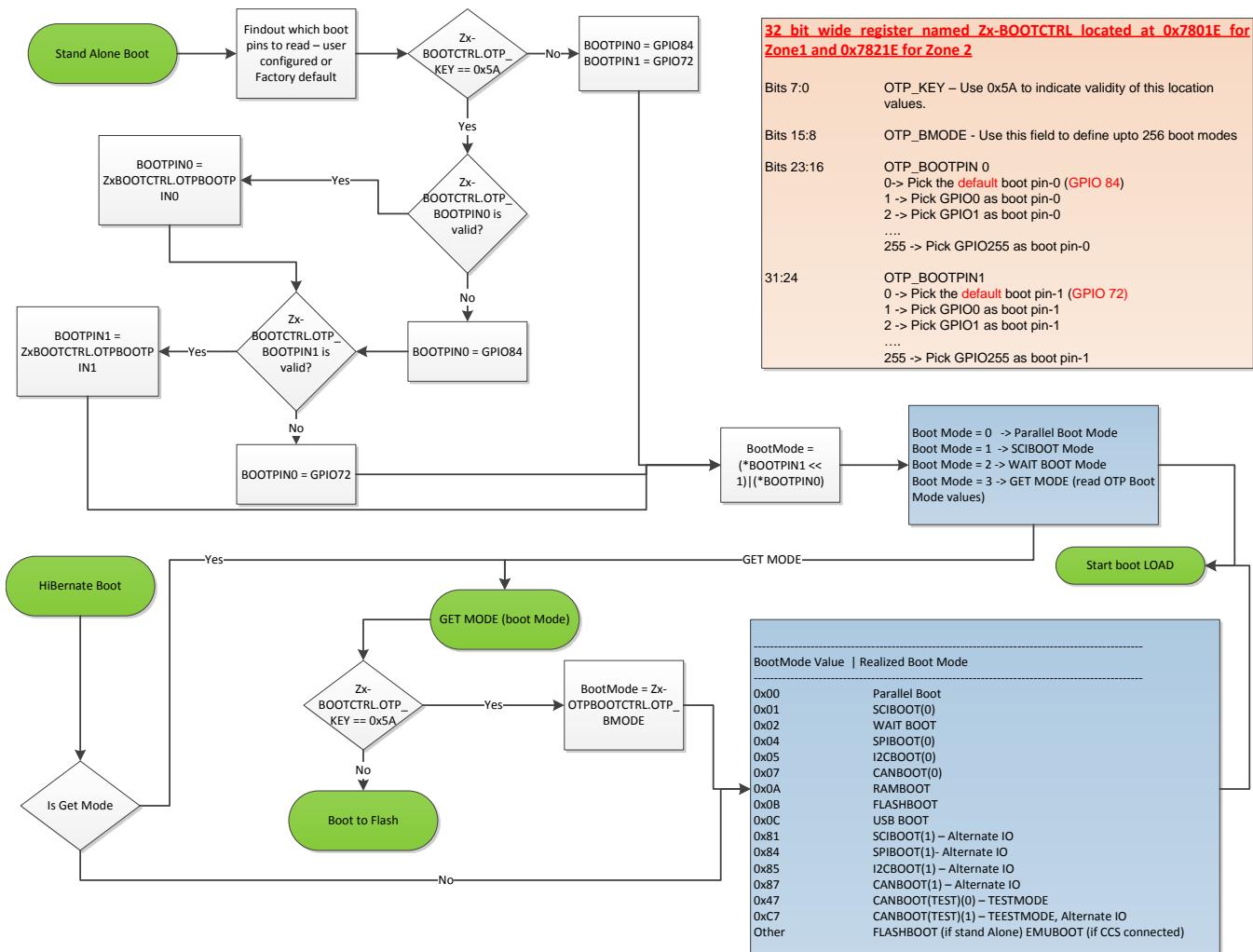
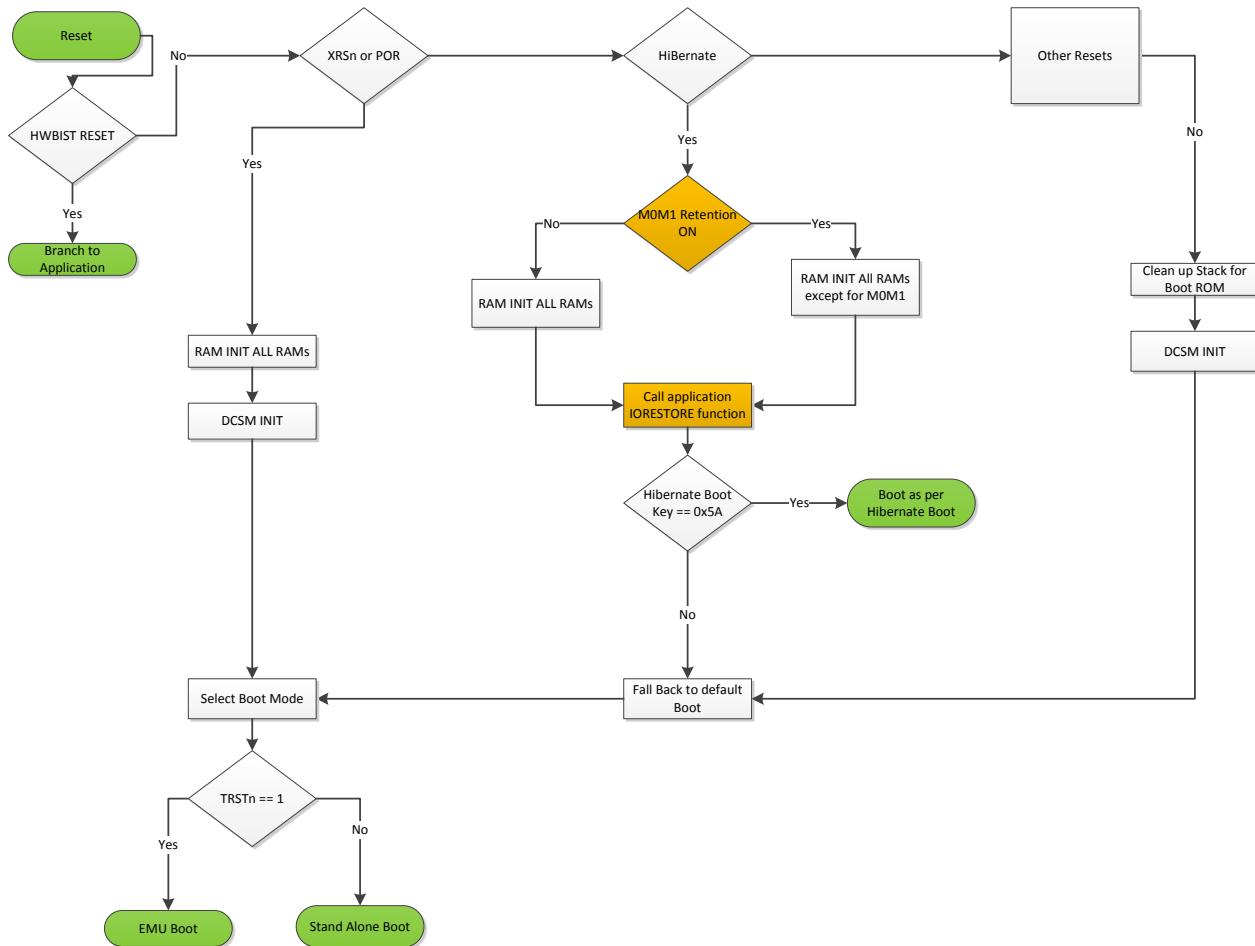
Figure 2-3. CPU1 Part 2


Figure 2-4. CPU1 Part 3

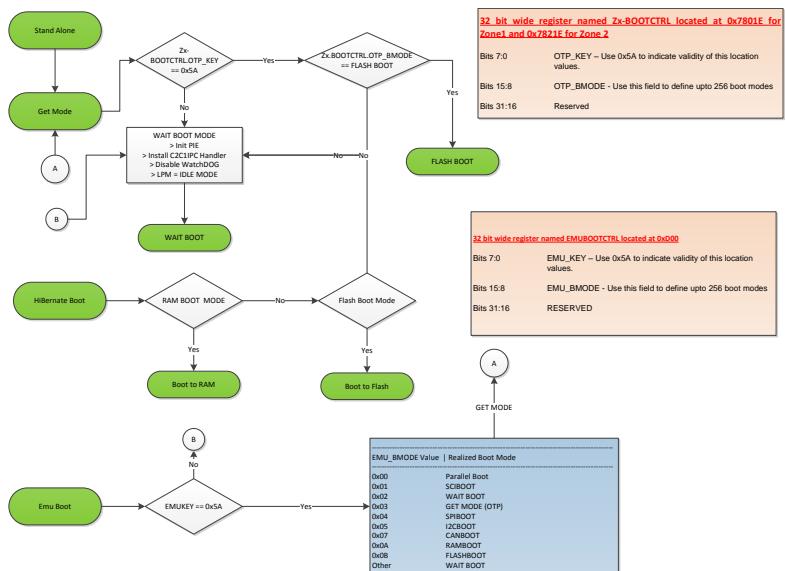


2.13 CPU2-Boot ROM Flow Chart

Figure 2-5. CPU2 Flow Chart (part 1)



CPU2 Flow Chart (part 2)



2.14 BootROM Reset Causes and Handling

BootROM checks the cause of reset every time device is reset and takes appropriate action as needed.

[Table 2-12](#) shows the reset causes on this device.

Table 2-12. Reset Causes

Reset Source	CPU1 Core Reset	CPU1 Subsystem Reset	CPU2 Held Under Reset	CPU2 Core Reset	CPU2 Subsystem Reset	IO Buffers in Reset State	CPU1-Boot ROM Action	CPU2-Boot ROM Action
1 POR	Yes	Yes	Yes	Yes	Yes	yes	Default boot flow, change CLK dividers to /1 and RAM-INIT	Default boot flow
2 XRSn	Yes	Yes	Yes	Yes	Yes	Yes	Default boot flow, change CLK dividers to /1 and RAM-INIT	Default boot flow
3 CPU1.WDRSn	Yes	Yes	Yes	Yes	Yes	Yes	Default boot flow, change CLK dividers to /1 and RAM-INIT	Default boot flow
4 CPU1.NMIWDRSn	Yes	Yes	Yes	Yes	Yes	Yes	Default boot flow, change CLK dividers to /1 and RAM-INIT	Default boot flow
12 CPU2.NMIWDRSn	No	No	No	Yes	Yes	No	Exception handled by CPU1	Default boot flow
13 CPU2.WDRSn	No	No	No	Yes	Yes	No	Exception handled by CPU1	Default boot flow

2.15 Exceptions and Interrupts handling

[Table 2-13](#) defines boot ROM action in case these exceptions occur during boot. The philosophy on CPU1-Boot ROM is to try and start the application and on CPU2-Boot ROM is to send an IPC to CPU1 and wait in loop.

Table 2-13. Exceptions Handling by Boot ROM

Exception source/type		Description	CPU1-Boot ROM Action	CPU2-Boot ROM Action
1	EFUSE-ERR Single bit	Single bit error in FUSEERR	Ignore and continue to boot	Ignore continue to boot
2	EFUSE-ERR Double bit	Not a single bit error in FUSEERR	Use CPU1.WD to reset the device (use counter overflow instead of BADKEY) – ERRORSTS pin set	DON'T CARE for CPU2
3	CLOCKFAIL	System will switch to INTOSC1	Clear the NMI, log the error and continue to boot	Clear, log and continue
4	RAMUNCERR	Double bit ECC error from RAM	Reset the device....because this error should not happen during boot as we took care of RAM-INITS	Send IPC to CPU1 and clear NMIFLG and wait forever.
5	FLUNCERR	Double bit error on FLASH	Reset the device....because this error should not happen during boot	Send IPC to CPU1 and clear NMIFLG and wait forever.
8	PIEVECTERR		Ignore, log and continue to boot	Ignore, log and continue to boot
10	RLNMI		Ignore, log and continue to boot	Send IPC to CPU1 and clear NMIFLG and continue boot.
11	CPU2WDRSn		Ignore, log and continue to boot	XXXX
12	CPU2NMIWDRSn		Ignore, log and continue to boot	XXXX
13	Unsupported PIE interrupts		Ignore and continue to boot	Send IPC to CPU1 and clear NMIFLG and continue to boot.

NOTE: Above NMI ERRORS will be logged into a RAM variable for application to read it when it starts. The location and format of this RAM variable is explained below.

2.16 CPU1 OTP Boot Configure Word

The below location is used in TI OTP to configure the behavior of boot ROM at production flow in the factory.

```
// bit 1,0 = 01 means enable PLL, else don't
// bit 7:2 = PLL divider to use - default will be all 1's, but PLL wont be used when default
// bit 9,8 = 01 means, ENABLE IPC in WAIT boot mode, else nope.
// bits 31:24 = 0x5A means the WORD is good/valid else not valid or not good
```

```
#define OTP_BOOT_CONFIGURE_WORD          (Uint32)(*(volatile Uint32 *)(Uint32)(0x703EE))
```

2.17 Boot ROM Status information

2.17.1 Boot ROM Health and Status

For lack of better location CPU1-Boot ROM stores the boot/health status in a RAM location in the EBSS section allocated for boot ROM.

C1BROM STATUS – at location
0x0000002C.

CPU1 application/user can look at this location during debug or at the start of the application to check what went on during the device boot up.

The below values can be set in C1BROM STATUS[31:80].

```
#define C1_BOOTROM_START_BOOT          0x000000100          //set during the initialization
phase of bootROM
#define C1_BOOTROM_IN_FLASH_BOOT       0x000000200          //set if boot to Flash is
detected
#define C1_BOOTROM_DCSM_INIT_DONE      0x000000400          //set after DCSM is initialized
#define C1_BOOTROM_RESC_HANDLED        0x000000800          //set after all RESC is handled
#define C1_BOOTROM_HANDLED_HIBRESET    0x00001000           //set if HIB reset is detected

#define C1_BOOTROM_HANDLED_XRSN        0x00004000           //set if XRSn is detected
#define C1_BOOTROM_HANDLED_POR         0x00008000           //set if POR is serviced
#define C1_BOOTROM_IN_AN_ITRAP         0x00020000           //set if C2-
BootROM detects an iTRAP
#define C1_BOOTROM_IN_C1TOC2_BRANCH    0x00040000           //INVALID - should never be set
#define C1_BOOTROM_GOT_A_PIEMismatch  0x00080000           //set if pie mismatch handler is
called
#define C1_BOOTROM_GOT_A_OVF_NMI       0x00100000           //set if ovf nmi is detected
#define C1_BOOTROM_GOT_A_CPU2NMWDRST_NMI 0x00200000           //set if cpu2nmwdrst nmi is
detected
#define C1_BOOTROM_GOT_A_CPU2WDRST_NMI 0x00400000           //set if cpu2wdrst nmi is detected
#define C1_BOOTROM_GOT_A_RL_NMI        0x00800000           //set if RL NMI is detected
#define C1_BOOTROM_GOT_A_SYSDBG_NMI    0x01000000           //set if sysdbg nmi is detected
#define C1_BOOTROM_GOT_A_PIEVECTERR_NMI 0x02000000           //set if pievect err nmi is
detected
#define C1_BOOTROM_GOT_A_C2BISTERR_NMI 0x04000000           //set if c2-
bist error nmi is detected
#define C1_BOOTROM_GOT_A_C1BISTERR_NMI 0x08000000           //set if c1-
bist error nmi is detected
#define C1_BOOTROM_GOT_A_FLASH_UNCERR_NMI 0x10000000           //set if Flash uncerr nmi is
detected
#define C1_BOOTROM_GOT_A_RAM_UNCERR_NMI 0x20000000           //set if ram uncerr nmi is
detected
#define C1_BOOTROM_GOT_A_MCLK_NMI      0x40000000           //set if missing clock nmi is
detected
#define C1_BOOTROM_BOOT_COMPLETE       0x80000000           //set if C1-
```

BootROM is starting an application after boot

2.17.2 CPU1-Boot ROM IPC NAK Status

If CPU1-Boot ROM IPC command support is enabled, then below are the NAK status that are possibly returned by CPU1-Boot ROM in C2TOC1IPCDATAR[11:0] register. At the time of a NAK, C2TOC1IPCDATAR[31:12] will contain the C1 BOOT ROM BOOT STATUS information as shown above.

```
#define C1BROM_NAK_STATUS_INVALID_VALUE          0x00000000 //invalid value or value
when not set
#define C1BROM_NAK_STATUS_CMD_NOT_SUPPORTED      0x00000001 //NAK STATUS command not
supported
#define C1BROM_NAK_STATUS_CMD_NOT_SET_PROPERLY    0x00000002 //NAK Status command not set
properly , for ex: IPC0 set but IPC31 not set
#define C1BROM_NAK_STATUS_ALREADY_BUSY_WITH_YOUR_CMD 0x00000003 //NAK status when cpu is
trying to send a second command before first one could complete
#define C1BROM_NAK_STATUS_CMD_RESULTED_IN_ERROR    0x00000004 //NAK status command
execution resulted in an error
#define C1BROM_NAK_STATUS_CMD_CANNOT_BE_EXECUTED_NOW 0x00000005 //NAK status -
command cannot be executed now in the current state of bootROM
```

2.17.3 CPU2-Boot ROM Health and Status

The below will be given to you in C1TOC2IPCDATAR[31:12], in case of an IPC NAK and also always in C2TOC1BOOTSTS[31:12], whenever boot status is written.

```
#define C2_BOOTROM_START_BOOT                  0x00000100 //set during the initialization
phase of C2-bootROM
#define C2_BOOTROM_IN_FLASH_BOOT               0x00000200 //set if boot to Flash is detected
#define C2_BOOTROM_DCSM_INIT_DONE              0x00000400 //set after DCSM is initialized
#define C2_BOOTROM_RESC_HANDLED               0x00000800 //set after all RESC is handled
#define C2_BOOTROM_HANDLED_HIBRESET            0x00001000 //set if HIB reset is detected

#define C2_BOOTROM_HANDLED_XRSN                0x00004000 //set if XRSn is detected
#define C2_BOOTROM_HANDLED_POR                 0x00008000 //set if POR is serviced
#define C2_BOOTROM_IN_AN_ITRAP                 0x00020000 //set if C2-
BootROM detects an iTRAP
#define C2_BOOTROM_IN_C1TOC2_BRANCH             0x00040000 //set if C2-
BootROM is doing a mtoc branch
#define C2_BOOTROM_GOT_A_PIEMISMATCH           0x00080000 //set if pie mismatch handler is
called
#define C2_BOOTROM_GOT_A_OVF_NMI                0x00100000 //set if ovf nmi is detected
#define C2_BOOTROM_GOT_A_CPU2NMIWDRST_NMI       0x00200000 // - should never be set
#define C2_BOOTROM_GOT_A_CPU2WDRST_NMI          0x00400000 // - should never be set
#define C2_BOOTROM_GOT_A_RL_NMI                 0x00800000 //set if RL NMI is detected
#define C2_BOOTROM_GOT_A_SYSDBG_NMI              0x01000000 //set if sysdbg nmi is detected
#define C2_BOOTROM_GOT_A_PIEVETERR_NMI           0x02000000 //set if pievect err nmi is
detected
#define C2_BOOTROM_GOT_A_C2BISTERR_NMI           0x04000000 //set if c2-
bist error nmi is detected
#define C2_BOOTROM_GOT_A_C1BISTERR_NMI           0x08000000 //set if c1-
bist error nmi is detected
#define C2_BOOTROM_GOT_A_FLASH_UNCERR_NMI        0x10000000 //set if Flash uncerr nmi is
detected
#define C2_BOOTROM_GOT_A_RAM_UNCERR_NMI          0x20000000 //set if ram uncerr nmi is
detected
#define C2_BOOTROM_GOT_A_MCLK_NMI                0x40000000 //set if missing clock nmi is
detected
#define C2_BOOTROM_BOOT_COMPLETE                 0x80000000 //set if C2-
BootROM is starting an application after boot
```

C2TOC1BOOTSTS[11:0] – these bits will carry the below status information.

```
#define C2_BOOTROM_BOOTSTS_CTOM_IGNORE 0x00000000 //invalid
status - tells that CPU2 has not filled in a valid value yet
#define C2_BOOTROM_BOOTSTS_SYSTEM_START_BOOT 0x00000001 //tells that
CPU2 has started to boot, but not completed the boot process yet
```

```
#define C2_BOOTROM_BOOTSTS_SYSTEM_READY 0x00000002          //tells that
CPU2 has completed the boot and is ready for C1TOC2 IPC commands
#define C2_BOOTROM_BOOTSTS_CTM_BOOT_CMD_ACK 0x00000003        //tells that
CPU2 ACKs the command in C1TOC2BOOTMODE register
#define C2_BOOTROM_BOOTSTS_CTM_BOOT_CMD_NAK_STATUS_NOT_SUPPORTED 0x00000004 //tells CPU2
doesn't support the command in C1TOC2BOOTMODE register
#define C2_BOOTROM_BOOTSTS_CTM_BOOT_CMD_NAK_STATUS_BUSY_WITH_BOOT 0x00000005 //tells that
CPU2 NAKs the current boot command in C1TOC2BOOTMODE register
```

2.17.4 CPU2-Boot ROM IPC NAK status

C1TOC2IPCDATAR[11:0] register values, when CPU2 BootROM system NAK's an IPC Command sent by CPU1 application.

C1TOC2IPCDATAR[31:12] register value stores the C2-BootROM health status as explained in above section

```
#define C2_BOOTROM_NAK_STATUS_INVALID_VALUE      0x00000000 //invalid value or value
when not set
#define C2_BOOTROM_NAK_STATUS_CMD_NOT_SUPPORTED    0x00000001 //NAK STATUS command not
supported
#define C2_BOOTROM_NAK_STATUS_CMD_NOT_SET_PROPERLY 0x00000002 //NAK Status command not
set properly , for ex: IPC0 set but IPC31 not set
#define C2_BOOTROM_NAK_STATUS_ALREADY_BUSY_WITH_YOUR_CMD 0x00000003 //NAK status when master
is trying to send a second command before first one could complete
#define C2_BOOTROM_NAK_STATUS_CMD_RESULTED_IN_ERROR   0x00000004 //NAK status command
execution resulted in an error
#define C2_BOOTROM_NAK_STATUS_CMD_CANNOT_BE_EXECUTED_NOW 0x00000005 //NAK status -
command cannot be executed now in the current state of bootROM
```

2.18 Boot and IPC Commands

2.18.1 BOOTMODE Commands

This section explains the boot mode commands used between CPU1 and CPU2. BootROM running on CPU2 core will decode the boot command from CPU1 system and take appropriate action.

2.18.1.1 C1TOC2BOOTMODE Commands

CPU1-Boot ROM does not communicate with CPU2-Boot ROM, it is the user application running on CPU1 which will talk to CPU2-Boot ROM using C1TOC2BOOTMODE commands. Please refer to the C1TOC2IPC Commands table on the supported IPC boot mode commands by CPU2-Boot ROM.

Before sending the boot mode IPC command to CPU2-Boot ROM, the CPU1 application is supposed to do the needed GPIO mux configurations for the peripheral IO pins and assign the peripheral to CPU2 by appropriately configuring the CPUSEL register.

CPU2 peripheral loaders doesn't configure any of the GPIO mux options but simply configure the peripheral as needed for the application load. The data protocols followed by CPU2 on peripheral loaders are same as in CPU1.

2.18.2 CPU1-Boot ROM Supported IPC Commands

CPU1-Boot ROM supports the following IPC commands. The feature can be used by CPU2 applications to command CPU1-Boot ROM to configure peripherals or IOs. CPU1-Boot ROM in WAIT BOOT MODE supports the below IPC commands. Note that WATCHDOG on CPU1 is disabled in this mode.

2.18.2.1 C2TOC1IPC Commands Table as Decoded by CPU1-Boot ROM

Table 2-14. C2TOC1IPC Commands Table ⁽¹⁾

Value	IPCRECVCOM (CPU2 - R/W, CPU1- R)	IPCRECVADDR (CPU2 - R/W, CPU1- R)	IPCRECVDATA (CPU2 - R/W, CPU1 - R)	IPCLOCALREPLY (CPU2 - R, CPU1 - R/W)	C2TOC1IPCFLG[3 1] = ? C2TOC1IPCFLAG [0] = 0	Description
0	C2C1_BROM_IPC_COMMAND _ILLEGAL	_NOT-USED_	_NOT-USED_	Look at error codes table	0x01	Illegal command
1	C2C1_BROM_IPC_SET_BITS_16	Address of the 16 bit register	Data in C2TOC1IPCDATAW[15:0]	Data read back from address after write	0x00 = Command success	$*(\text{address}) \mid= \text{data};$
2	C2C1_BROM_IPC_SET_BITS_32	Address of the 32 bit register	Data;	Data read back from address after write	Same as above	$*(\text{address}) \mid= \text{data};$
3	C2C1_BROM_IPC_CLEAR_BIT_S_16	Address of the 16 bit register	Data in C2TOC1IPCDATAW[15:0]	Data read back after write	Same as above	$*(\text{address}) \&= \sim \text{data};$
4	C2C1_BROM_IPC_CLEAR_BIT_S_32	Address of the 32 bit register	Data	Data read back after write	Same as above	$*(\text{address}) \&= \sim \text{data};$
5	C2C1_BROM_IPC_DATA_WRITE_16	Address of the 16 bit register	Data in MTOCIPCDATAW[15:0]	Data read back from the address	Same as above	$*(\text{address}) = \text{data};$
6	C2C1_BROM_IPC_DATA_WRITE_32	Address of the 32 bit register	Data	Same as above	Same as above	$*(\text{address}) = \text{data};$
7	C2C1_BROM_IPC_DATA_READ_16	Address of the 16 bit register	--NOT_USED--	Data in C2TOC1IPCDATAR[15:0]	Same as above	C2TOC1IPCDATAR[15:0] = $*(\text{address});$ Only 16 bit read from address
8	C2C1_BROM_IPC_DATA_READ_32	Address of the 32 bit register	Same as above	32 bit data	Same as above	C2TOC1IPCDATAR[31:0] = $*(\text{address});$ 32 bits read from address
9	C2C1_BROM_IPC_SET_BITS_PROTECTED_16	Address of the 16 bit register	Data in C2TOC1IPCDATAW[15:0]	Data read back from address after write	0x00 = Command success	EALLOW; $*(\text{address}) \mid= \text{data};$ EDIS;
10	C2C1_BROM_IPC_SET_BITS_PROTECTED_32	Address of the 32 bit register	Data;	Data read back from address after write	Same as above	EALLOW; $*(\text{address}) \mid= \text{data};$ EDIS;
11	C2C1_BROM_IPC_CLEAR_BIT_S_PROTECTED_16	Address of the 16 bit register	Data in C2TOC1IPCDATAW[15:0]	Data read back after write	Same as above	EALLOW; $*(\text{address}) \&= \sim \text{data};$ EDIS;
12	C2C1_BROM_IPC_CLEAR_BIT_S_PROTECTED_32	Address of the 32 bit register	Data	Data read back after write	Same as above	EALLOW; $*(\text{address}) \&= \sim \text{data};$ EDIS;
13	C2C1_BROM_IPC_DATA_WRITE_E_PROTECTED_16	Address of the 16 bit register	Data in C2TOC1IPCDATAW[15:0]	Data read back from the address	Same as above	EALLOW; $*(\text{address}) \&= \sim \text{data};$ EDIS;
14	C2C1_BROM_IPC_DATA_WRITE_E_PROTECTED_32	Address of the 32 bit register	Data	Same as above	Same as above	EALLOW; $*(\text{address}) \&= \sim \text{data};$ EDIS;
15	C2C1_BROM_IPC_DATA_READ_D_PROTECTED_16	Address of the 32 bit register	--NOT_USED--	Data in C2TOC1IPCDATAR[15:0]	Same as above	EALLOW; C2TOC1IPCDATAR[15:0] = $*(\text{address});$ EDIS; Only 16 bit read from address
16	C2C1_BROM_IPC_DATA_READ_D_PROTECTED_32	Address of the 32 bit register	Data	Same as above	Same as above	EALLOW; C2TOC1IPCDATAR[31:0] = $*(\text{address});$ EDIS; 32 bits read from address

⁽¹⁾ All 32-bit operations are done in little endian format (C28X is 16 bit addressable).

Example: a 32-bit IPC write is handles as below:

- Data[15:0] is written in address
- Data [31:16] is written in address+1

2.18.3 CPU2-Boot ROM Supported IPC Commands

2.18.3.1 C1TOC2IPC Commands Table as Decoded by CPU2-Boot ROM

Table 2-15. C1TOC2IPC Commands Table

Value	IPCRECVCOM (CPU1 - R/W, CPU2 R)	IPCRECVADDR (CPU1 - R/W, BCPU2- R)	IPCRECVDATA (CPU1 - R/W, CPU2- R)	IPCLOCALREPL Y (CPU1 - R, CPU2 - R/W)	C1TOC2IPCFLG [31] = ? C1TOC2IPCFLA G[0] = 0	Description
0	C1C2_BROM_IPC_COMM AND_ILLEGAL	_NOT-USED_	_NOT-USED_	Look at error codes table	0x01	Illegal command
1.	C1C2_BROM_IPC_SET_BI TS_16	Address of the 16 bit register	Data in C1TOC2IPCDATA W[15:0]	Data read back from address after write	0x00 = Command success	*(address) = data;
2.	C1C2_BROM_IPC_SET_BI TS_32	Address of the 32 bit register	Data;	Data read back from address after write	Same as above	*(address) = data;
3.	C1C2_BROM_IPC_CLEAR _BITS_16	Address of the 16 bit register	Data in C1TOC2IPCDATA W[15:0]	Data read back after write	Same as above	*(address) &= ~data;
4.	C1C2_BROM_IPC_CLEAR _BITS_32	Address of the 32 bit register	Data	Data read back after write	Same as above	*(address) &= ~data;
5.	C1C2_BROM_IPC_DATA_ WRITE_16	Address of the 16 bit register	Data in MTOCIPCDATAW [15:0]	Data read back from the address	Same as above	*(address) = data;
6.	C1C2_BROM_IPC_DATA_ WRITE_32	Address of the 32 bit register	Data	Same as above	Same as above	*(address) = data;
7	C1C2_BROM_IPC_DATA_ READ_16	Address of the 16 bit register	--NOT_USED--	Data in C1TOC2IPCDATA R[15:0]	Same as above	C1TOC2IPCDATAR [15:0] = *(address); Only 16 bit read from address
8	C1C2_BROM_IPC_DATA_ READ_32	Address of the 32 bit register	Same as above	32 bit data	Same as above	C1TOC2IPCDATAR [31:0] = *(address); 32 bits read from address
9	C1C2_BROM_IPC_SET_BI TS_ PROTECTED_16	Address of the 16 bit register	Data in C1TOC2IPCDATA W[15:0]	Data read back from address after write	0x00 = Command success	EALLOW; *(address) = data; EDIS;
10	C1C2_BROM_IPC_SET_BI TS_ PROTECTED_32	Address of the 32 bit register	Data;	Data read back from address after write	Same as above	EALLOW; *(address) = data; EDIS;
11	C1C2_BROM_IPC_CLEAR _BITS_ PROTECTED_16	Address of the 16 bit register	Data in C1TOC2IPCDATA W[15:0]	Data read back after write	Same as above	EALLOW; *(address) &= ~data; EDIS;
12	C1C2_BROM_IPC_CLEAR _BITS_ PROTECTED_32	Address of the 32 bit register	Data	Data read back after write	Same as above	EALLOW; *(address) &= ~data; EDIS;
13	C1C2_BROM_IPC_DATA_ WRITE_ PROTECTED_16	Address of the 16 bit register	Data in C1TOC2IPCDATA W[15:0]	Data read back from the address	Same as above	EALLOW; *(address) = data; EDIS;
14	C1C2_BROM_IPC_DATA_ WRITE_ PROTECTED_32	Address of the 32 bit register	Data	Same as above	Same as above	EALLOW; *(address) = data; EDIS;
15	C1C2_BROM_IPC_DATA_ READ_ PROTECTED_16	Address of the 16 bit register	--NOT_USED--	Data in C1TOC2IPCDATA R[15:0]	Same as above	EALLOW; C1TOC2IPCDATAR [15:0] = *(address); Only 16 bit read from address
16	C1C2_BROM_IPC_DATA_ READ_ PROTECTED_32	Address of the 32 bit register	Same as above	32 bit data	Same as above	EALLOW; C1TOC2IPCDATAR [31:0] = *(address); EDIS; 32 bits read from address

Table 2-15. C1TOC2IPC Commands Table (continued)

Value	IPCRECVCOM (CPU1 - R/W, CPU2 R)	IPCRECVADDR (CPU1 - R/W, BCPU2- R)	IPCRECVDATA (CPU1 - R/W, CPU2- R)	IPCLOCALREPL Y (CPU1 - R, CPU2 - R/W)	C1TOC2IPCFLG [31] = ? C1TOC2IPCFLA G[0] = 0	Description
17	C1C2_BROM_IPC_BRANCH_CALL	Address where to branch to	_NOT_USED_BY_BOOTROM (code at the branch can use this though)	NOT_USED_BY_BOOTROM (code at the branch can use this though)	Same as above	C2-BootROM will jump to the address in ADDR register and starts executing the code from that address. PIE will be enabled when this branch occurs, it is upto the application to disable and reload PIE interrupt handlers if it wants to.
18	C1C2_BROM_IPC_FUNCTION_CALL	Address of the function	Parameter for the function call	Result of function call (return value if any from function)	Same as above	C2-BootROM will jump to the address in ADDR register and starts executing the code from that address; Data in DATAW register can be used as parameter to the function call. C-BootROM returns back to where it was after servicing the function call. Function call is performed from inside the interrupt service routine on Aria so user has to keep this in mind.
19	C1C2_BROM_IPC_EXECUTE_TE_BOOTMODE_CMD <ul style="list-style-type: none"> • C1TOC2BOOTMO DE = 0xA, C1C2_BROM_BOOTMODE_BOOT_FROM_RAM • C1TOC2BOOTMO DE = 0xB, C1C2_BROM_BOOTMODE_BOOT_FROM_FLASH • C1TOC2BOOTMO DE = 0x1, C1C2_BROM_BOOTMODE_BOOT_FROM_SCI • C1TOC2BOOTMO DE = 0x4, C1C2_BROM_BOOTMODE_BOOT_FROM_SPI 	--NOT_USED--	--NOT_USED--	--NOT_USED--	Same as above	Execute loaders as per requested value in C1TOC2BOOTMODE register.

Table 2-15. C1TOC2IPC Commands Table (continued)

Value	IPCRECVCOM (CPU1 - R/W, CPU2 R)	IPCRECVADDR (CPU1 - R/W, BCPU2- R)	IPCRECVDATA (CPU1 - R/W, CPU2- R)	IPCLOCALREPL Y (CPU1 - R, CPU2 - R/W)	C1TOC2IPCFLG [31] = ? C1TOC2IPCFLA G[0] = 0	Description	
	<ul style="list-style-type: none"> • C1TOC2BOOTMO DE = 0x5, C1C2_BROM_BO OTMODE_ BOOT_FROM_I2C • C1TOC2BOOTMO DE = 0x0, C1C2_BROM_BO OTMODE_ BOOT_FROM_PA RALLEL • C1TOC2BOOTMO DE = 0x7, C1C2_BROM_BO OTMODE_ BOOT_FROM_CA N 						

2.18.3.2 CPU2-Boot ROM Sent IPC Commands in Case of Errors

CPU2-Boot ROM sends the below IPC commands to CPU1 in case there is an error. If CPU1 application enables C2C1IPCINT1 while CPU2-Boot ROM is running then the C2TOC1IPC COM register values upon receiving an IPC interrupt are as defined below:

```
#define C2_BOOTROM_IPC_CTOM_COMMAND_ILLEGAL          0x00000000 //invalid command value -  
default value when starting boot  
#define C2_BOOTROM_IPC_CTOM_CONTROL_SYSTEM_IN_ITRAP    0xFFFFFFF8 //message tells that CPU2  
has got an iTRAP, address where iTrap occured will be in IPC ADDR register  
#define C2_BOOTROM_IPC_CTOM_PIE_INTERRUPT_NOT_SUPPORTED 0xFFFFFFF9 //message tells that CPU2  
got a spurious PIE interrupt, intr no. will be in IPCDATAW register  
#define C2_BOOTROM_IPC_CTOM_PIE_VECTOR_ADDRESS_MISMATCH 0xFFFFFFF0 //message tells that CPU2  
got a PIE vector mismatch error  
#define C2_BOOTROM_IPC_CTOM_CONTROL_SYSTEM_IN_FLCNCERR   0xFFFFFFF1 //message tells that CPU2  
got a Flash uncorrectable error  
#define C2_BOOTROM_IPC_CTOM_CONTROL_SYSTEM_IN_RAMUNCERR   0xFFFFFFF2 //message tells that CPU2  
got a RAM uncorrectable error
```

2.19 Device Boot Process Timeline Diagram

[Table 2-16](#) gives an overview of synchronization between CPU1 and CPU2 bootROMs.

Table 2-16. Time Diagram

Time Line	CPU1	CPU2
T0	POR indicates that device is not yet fully powered and is in reset	POR indicates that device is not yet fully powered and is in reset

Table 2-16. Time Diagram (continued)

Time Line	CPU1	CPU2
T1	CPU1 System Configuration: <ul style="list-style-type: none"> • RESC cause check • PLL POWER UP • FALSH POWER UP • RAM INITs • DCSM INIT • NMI ENABLE • PLL BYPASS 	• CPU2 is held in reset
T2	Bring CPU1 out of reset	CPU2 System Config: <ul style="list-style-type: none"> • RESC check • RAM INIT • DCSM INIT • NMI ENABLE
T3	EMU BOOT or STANDALONE BOOT or HIB BOOT <ul style="list-style-type: none"> • If WAIT BOOT go to wait boot loop • If boot from peripheral download application code from peripheral and save it in RAM and jump to start of application. • If WAIT BOOT go to wait boot loop 	HIBRESC check READ BOOT MODE BOOT TO RAM/BOOT TO FLASH Init PIE and WAIT BOOT MODE

2.20 BootROM GPIO Configurations:

Default boot mode GPIO pins:

Boot mode pin 0 : GPIO 84

Boot mode pin 1 : GPIO 72

The boot mode pins are configurable by user by programming proper OTPKEY.

SCIBoot – IO Option 1

SCITX: GPIO84

SCIRX: GPIO85

SCIBoot – IO Option 2

SCITX: GPIO28

SCIRX: GPIO29

Bit parallel bootloader GPIO pins

D0 - GPIO65

D1 - GPIO64

D2 - GPIO58

D3 - GPIO59

D4 - GPIO60

D5 - GPIO61

D6 - GPIO62

D7 - GPIO63

HOST_CTRL - GPIO70

DSP_CTRL - GPIO69

CAN Boot – IO Option 1

CAN0_RX - GPIO70

CAN0_TX - GPIO71

CAN Boot – IO Option 2

CAN0_RX - GPIO62
CAN0_TX - GPIO63

I2C Boot - IO Option 1

I2C0_SDAA - GPIO91
I2C0_SCLA - GPIO92

I2C Boot - IO Option 2

I2C0_SDAA - GPIO32
I2C0_SCLA - GPIO33

SPI Boot – IO Option 1

SPISIMOA - GPIO58
SPISOMIA - GPIO59
SPICLKA - GPIO60
SPISTEA - GPIO61

SPI Boot – IO option 2

SPISIMOA - GPIO16
SPISOMIA - GPIO17
SPICLKA - GPIO18
SPISTEA - GPIO19

USB Boot

USB0DM - GPIO42
USB0DP - GPIO43

(the mode implemented is USB device type, Device Firmware Upgrade Class)

2.21 Boot ROM Memory Map

2.21.1 F2837x Memory Map – CPU1

Figure 2-6. F2837x Memory Map – CPU1

```
*****
TMS320C2000 Linker PC v6.1.3
*****
>> Linked Wed Apr 10 21:18:09 2013

OUTPUT FILE NAME: <F2837x_cpu01_bootROM.out>
ENTRY POINT SYMBOL: "_InitBoot" address: 003feac2

MEMORY CONFIGURATION

      name      origin     length    used   unused   attr   fill
-----
PAGE 0:
SYSBIOS_FLASH      00080010  00001ff0  000007be  00001832  RWIX
Z1_SCC_ROM         003f0000  00000800  00000800  00000000  RWIX  ffff
Z2_SCC_ROM         003f0800  00000800  00000800  00000000  RWIX  ffff
TI_RESERVED        003f1000  00000008  00000008  00000000  RWIX  ffff
Z1_SECURE_ROM       003f1008  00006ff8  00006ff8  00000000  RWIX  ffff
ROM_SIGNATURE       003f8000  00000002  00000002  00000000  RWIX  ffff
SYSBIOS_ROM        003f8002  00001e0e  00001e0e  00000000  RWIX
RESERVED           003f9e10  00003a08  00003a08  00000000  RWIX  ffff
BOOT               003fd818  0000271a  0000271a  00000000  RWIX  ffff
CRCTABLE_ROM        003fff32  00000008  00000008  00000000  RWIX  ffff
BIST_SIGNATURE      003fff3a  00000040  00000040  00000000  RWIX
VERSION            003fff7a  00000002  00000002  00000000  RWIX
CHECKSUM           003fff7c  00000042  00000042  00000000  RWIX
VECS               003fffbe  00000042  00000042  00000000  RWIX
```

2.21.2 F2837x Memory Map – CPU2

Figure 2-7. F2837x Memory Map – CPU2

```
*****
TMS320C2000 Linker PC v6.1.3
*****
>> Linked Wed Apr 10 21:23:14 2013

OUTPUT FILE NAME: <F2837x_cpu02_bootROM.out>
ENTRY POINT SYMBOL: "_InitBoot" address: 003fe649

MEMORY CONFIGURATION

      name      origin     length    used   unused   attr   fill
-----+-----+-----+-----+-----+-----+-----+
PAGE 0:
  SYSBIOS_FLASH      00080010  00001ff0  000007be  00001832  RWIX
  Z1_SCC_ROM          003f0000  00000800  00000800  00000000  RWIX  ffff
  Z2_SCC_ROM          003f0800  00000800  00000800  00000000  RWIX  ffff
  TI_RESERVED         003f1000  00000008  00000008  00000000  RWIX  ffff
  Z1_SECURE_ROM        003f1008  00006ff8  00006ff8  00000000  RWIX  ffff
  ROM_SIGNATURE        003f8000  00000002  00000002  00000000  RWIX  ffff
  SYSBIOS_ROM          003f8002  00001e0e  00001e0e  00000000  RWIX
  RESERVED             003f9e10  00003a08  00003a08  00000000  RWIX  ffff
  BOOT                 003fd818  0000271a  0000271a  00000000  RWIX  ffff
  CRCTABLE_ROM         003fff32  00000008  00000008  00000000  RWIX  ffff
  BIST_SIGNATURE        003fff3a  00000040  00000040  00000000  RWIX
  VERSION              003fff7a  00000002  00000002  00000000  RWIX
  CHECKSUM             003fff7c  00000042  00000042  00000000  RWIX
  VECS                 003fffbe  00000042  00000042  00000000  RWIX
```

2.22 Boot ROM Checksum

ROM checksum is internally used by TI to make sure of ROM integrity before shipping the parts.

2.23 CPU1/CPU2 ROM REVISION Information

32 bits from the location 0x003FFF7A stores ROM revision and release date information as shown below:

- CPU1 ROM REVISION is as below starting from 0x003FFF7A location

```
.sect ".Version"
.global _clbrom_version
clbrom_version:
.word 0x0100 ; Boot ROM Version v0.1
.word 0x0413 ; Month/Year: (ex: 0x0109 = 1/09 = Jan 2009)
```

- CPU2 ROM REVISION is as below starting from 0x003FFF7A location

```
.sect ".Version"
.global _c2brom_version
c2brom_version:
.word 0x0100 ; Boot ROM Version v0.1
.word 0x0413 ; Month/Year: (ex: 0x0109 = 1/09 = Jan 2009)
```

In the 16-bit REVISION word at location 0x3FFF7A, LSB 8 bits need to be reserved to store the Secure ROM contents revision. Since Secure ROM is EXEONLY boot ROM revision locations can be read by application to find out the revision of code in secure ROM.

On REV0 of the Silicon there are no Secure ROM libraries, so the revision is 0x0 for this on both CPU1 and CPU2.

2.24 RAM/Flash Usage and Application Entry Points

Below is the RAM memory usage on CPU1-Boot ROM. All the stack memory will be Zeroed out by boot ROM whenever boot ROM is run from start.

The SYSBIOS_RAM is a special section which is used by SYSBIOS in boot ROM. This memory must be reserved by customers application and should not be used by application if they are planning on using SYSBIOS is ROM.

```
EBSS      : origin = 0x002,      length = 0x000040
STACK     : origin = 0x042,      length = 0x0000E0
SYSBIOS_RAM : origin = 0x780,    length = 0x000080
```

2.24.1 Reserved RAM Memory for CPU2-Boot ROM

Below is the RAM memory usage on CPU2-Boot ROM. All the stack memory will be Zeroed out by boot ROM whenever boot ROM is run from start.

The SYSBIOS_RAM is a special section which is used by SYSBIOS in boot ROM. This memory must be reserved by customers application and should not be used by application if they are planning on using SYSBIOS is ROM.

```
EBSS      : origin = 0x002,      length = 0x00001E
STACK     : origin = 0x042,      length = 0x000060
SYSBIOS_RAM : origin = 0x780,    length = 0x000080
```

2.24.2 CPU1/CPU2 RAM Entry Point

RAM Entry point is fixed at 0x0000000000, user applications when using boot-to-ram option are supposed to place their entry point which branches to main() at this location. Boot ROM when set to boot-to-RAM branches to this location.

2.24.3 CPU1/CPU2 Flash Entry Point

Flash entry point is fixed at 0x000080000, user applications when using boot-to-ram option are supposed to place their entry point which branches to main() at this location. Boot ROM when set to boot-to-flash branches to this location.

2.24.4 CPU1/CPU2 Flash Reserved Memory

Below is the Flash memory on CPU1/CPU2 is reserved for SYSBIOS usage if customer is planning on using SYSBIOS libraries in ROM. The below locations in SECTOR-A of Flash memory will be programmed with needed SYSBIOS components linked with application.

If user is not planning on using SYSBIOS in ROM then they are free to use this memory as needed by application. But if user is planning on using SYSBIOS in ROM then this memory is supposed to be reserved and preferably this sector is supposed to be made un-secure or made sure that no secure Zone claims this sector.

```
SYSBIOS_Flash : origin = 0x00080010, length = 0x7BE
```

2.25 ROM Wait States

ROM memory on this device is not ZERO-WAIT STATE by default. ROM memory is supports prefetch enable and disable configuration to support better execution speeds at different clock frequency configurations as shown below.

By default, ROM is 1-Wait State and pre-fetch is disabled, but if the user is executing his application below 180 MHz then Pre-fetch can be enabled and if the user application is running below 150 Mhz then ROM can be configured for 0-WS operation as shown in [ROM Wait States](#).

Table 2-17. ROM Wait States

WAITSTATE Disable Bit (bit 0 at 0x5F540)	Pre-Fetch Enable Bit Bit 0 at address (0x5e608)	ROM Configuration	ROM Access Time
0	0	WS enabled Pre-fetch disabled Max Frequency : 200 MHz	All accesses are 1 WS. This is default state on reset.
0	1	WS enabled Pre-fetch *enabled* Max Frequency : 180 MHz	Same as current spec.
1	x	0-wait Pre-fetch disabled Max Frequency : 150 MHz	Same as current spec.

2.26 Device Boot Modes Description

All the peripheral boot modes except USB on CPU1 support two options per peripheral and each option is configured to work on different set of RX/TX IOs. Depending on the application design user can choose either option.

Peripheral boot modes on CPU2 are supposed to be started by application running on CPU1 and this application is supposed to be configure the peripheral and needed IOs for CPU2 before sending the proper boot mode IPC command to CPU2-Boot ROM.

The boot modes below are the same as they were on the legacy C2000 device.

- SCI Boot Mode
- SPI Boot Mode
- I2C Boot Mode
- Parallel Boot Mode
- DCAN Boot Mode

The following boot mode is new on the device:

- USB Boot Mode

USB Boot Mode implemented supports Device Firmware Upgrade class (DFU) and is the same as the Flash-based USB loader.

The following sections explain each of the supported peripheral boot mode(s) on CPU1/CPU2 Boot ROM, in detail.

The data transfer protocols or stream structures that allow boot data transfer between boot ROM and Host device, are compatible to the respective bootloaders on the Piccolo class of C2000 devices. This allows the user to reuse the same tools used to send boot data to Piccolo(s) to also send boot data to boot ROM.

2.26.1 Boot Data Stream Structure

The following two tables and associated examples show the structure of the data stream incoming to the bootloader. The basic structure is the same for all the bootloaders and is based on the C54x source data stream generated by the C54x hex utility. The C28x hex utility (hex2000.exe) has been updated to support this structure. The hex2000.exe utility is included with the C2000 code generation tools. All values in the data stream structure are in hex.

The first 16-bit word in the data stream is known as the key value. The key value is used to tell the bootloader the width of the incoming stream: 8 or 16 bits. Note that not all bootloaders will accept both 8 and 16-bit streams. Please refer to the detailed information on each loader for the valid data stream width. For an 8-bit data stream, the key value is 0x08AA and for a 16-bit stream it is 0x10AA. If a bootloader receives an invalid key value, then the load is aborted.

The next eight words are used to initialize register values or otherwise enhance the bootloader by passing values to it. If a bootloader does not use these values then they are reserved for future use and the bootloader simply reads the value and then discards it. Currently only the SPI and I2C and parallel XINTF bootloaders use these words to initialize registers.

The tenth and eleventh words comprise the 22-bit entry point address. This address is used to initialize the PC after the boot load is complete. This address is most likely the entry point of the program downloaded by the bootloader.

The twelfth word in the data stream is the size of the first data block to be transferred. The size of the block is defined for both 8-bit and 16-bit data stream formats as the number of 16-bit words in the block. For example, to transfer a block of 20 8-bit data values from an 8-bit data stream, the block size would be 0x000A to indicate 10 16-bit words.

The next two words tell the loader the destination address of the block of data. Following the size and address will be the 16-bit words that make up that block of data.

This pattern of block size/destination address repeats for each block of data to be transferred. Once all the blocks have been transferred, a block size of 0x0000 signals to the loader that the transfer is complete. At this point the loader will return the entry point address to the calling routine which in turn will cleanup and exit. Execution will then continue at the entry point address as determined by the input data stream contents.

Table 2-18. General Structure Of Source Program Data Stream In 16-Bit Mode

Word	Contents
1	10AA (KeyValue for memory width = 16bits)
2	Register initialization value or reserved for future use
3	Register initialization value or reserved for future use
4	Register initialization value or reserved for future use
5	Register initialization value or reserved for future use
6	Register initialization value or reserved for future use
7	Register initialization value or reserved for future use
8	Register initialization value or reserved for future use
9	Register initialization value or reserved for future use
10	Entry point PC[22:16]
11	Entry point PC[15:0]
12	Block size (number of words) of the first block of data to load. If the block size is 0, this indicates the end of the source program. Otherwise another section follows.
13	Destination address of first block Addr[31:16]
14	Destination address of first block Addr[15:0]
15	First word of the first block in the source being loaded
...	...
...	...
.	Last word of the first block of the source being loaded
.	Block size of the 2nd block to load.
.	Destination address of second block Addr[31:16]
.	Destination address of second block Addr[15:0]
.	First word of the second block in the source being loaded
...	...
.	Last word of the second block of the source being loaded
.	Block size of the last block to load
.	Destination address of last block Addr[31:16]
.	Destination address of last block Addr[15:0]
.	First word of the last block in the source being loaded
...	...
...	...
n	Last word of the last block of the source being loaded
n+1	Block size of 0000h - indicates end of the source program

Example 2-1. Data Stream Structure 16-bit

```

10AA          ; 0x10AA 16-bit key value
0000 0000 0000 0000 ; 8 reserved words
0000 0000 0000 0000
003F 8000      ; 0x003F8000 EntryAddr, starting point after boot load completes
0005          ; 0x0005 - First block consists of 5 16-bit words
003F 9010      ; 0x003F9010 - First block will be loaded starting at 0x3F9010
0001 0002 0003 0004 ; Data loaded = 0x0001 0x0002 0x0003 0x0004 0x0005
0005
0002          ; 0x0002 - 2nd block consists of 2 16-bit words
003F 8000      ; 0x003F8000 - 2nd block will be loaded starting at 0x3F8000
7700 7625      ; Data loaded = 0x7700 0x7625
0000          ; 0x0000 - Size of 0 indicates end of data stream
After load has completed the following memory values will have been initialized as follows:
Location      Value
0x3F9010      0x0001
0x3F9011      0x0002
0x3F9012      0x0003
0x3F9013      0x0004
0x3F9014      0x0005
0x3F8000      0x7700
0x3F8001      0x7625
PC Begins execution at 0x3F8000

```

In 8-bit mode, the least significant byte (LSB) of the word is sent first followed by the most significant byte (MSB). For 32-bit values, such as a destination address, the most significant word (MSW) is loaded first, followed by the least significant word (LSW). The bootloaders take this into account when loading an 8-bit data stream.

Table 2-19. LSB/MSB Loading Sequence in 8-Bit Data Stream

Byte		Contents	
		LSB (First Byte of 2)	MSB (Second Byte of 2)
1	2	LSB: AA (KeyValue for memory width = 8 bits)	MSB: 08h (KeyValue for memory width = 8 bits)
3	4	LSB: Register initialization value or reserved	MSB: Register initialization value or reserved
5	6	LSB: Register initialization value or reserved	MSB: Register initialization value or reserved
7	8	LSB: Register initialization value or reserved	MSB: Register initialization value or reserved
...
...
17	18	LSB: Register initialization value or reserved	MSB: Register initialization value or reserved
19	20	LSB: Upper half of Entry point PC[23:16]	MSB: Upper half of entry point PC[31:24] (Always 0x00)
21	22	LSB: Lower half of Entry point PC[7:0]	MSB: Lower half of Entry point PC[15:8]
23	24	LSB: Block size in words of the first block to load. If the block size is 0, this indicates the end of the source program. Otherwise another block follows. For example, a block size of 0x000A would indicate 10 words or 20 bytes in the block.	MSB: block size
25	26	LSB: MSW destination address, first block Addr[23:16]	MSB: MSW destination address, first block Addr[31:24]
27	28	LSB: LSW destination address, first block Addr[7:0]	MSB: LSW destination address, first block Addr[15:8]
29	30	LSB: First word of the first block being loaded	MSB: First word of the first block being loaded
...
...
.	.	LSB: Last word of the first block to load	MSB: Last word of the first block to load
.	.	LSB: Block size of the second block	MSB: Block size of the second block
.	.	LSB: MSW destination address, second block Addr[23:16]	MSB: MSW destination address, second block Addr[31:24]
.	.	LSB: LSW destination address, second block Addr[7:0]	MSB: LSW destination address, second block Addr[15:8]
.	.	LSB: First word of the second block being loaded	MSB: First word of the second block being loaded
...
...
.	.	LSB: Last word of the second block	MSB: Last word of the second block
.	.	LSB: Block size of the last block	MSB: Block size of the last block
.	.	LSB: MSW of destination address of last block Addr[23:16]	MSB: MSW destination address, last block Addr[31:24]
.	.	LSB: LSW destination address, last block Addr[7:0]	MSB: LSW destination address, last block Addr[15:8]
.	.	LSB: First word of the last block being loaded	MSB: First word of the last block being loaded
...
...
.	.	LSB: Last word of the last block	MSB: Last word of the last block
n	n+1	LSB: 00h	MSB: 00h - indicates the end of the source

Example 2-2. Data Stream Structure 8-bit

```

AA 08      ; 0x08AA 8-bit key value
00 00 00 00 ; 8 reserved words
00 00 00 00
00 00 00 00
00 00 00 00
3F 00 00 80 ; 0x003F8000 EntryAddr, starting point after boot load completes
05 00      ; 0x0005 - First block consists of 5 16-bit words
3F 00 10 90 ; 0x003F9010 - First block will be loaded starting at 0x3F9010
01 00      ; Data loaded = 0x0001 0x0002 0x0003 0x0004 0x0005
02 00
03 00
04 00
05 00
02 00      ; 0x0002 - 2nd block consists of 2 16-bit words
3F 00 00 80 ; 0x003F8000 - 2nd block will be loaded starting at 0x3F8000
00 77      ; Data loaded = 0x7700 0x7625
25 76
00 00      ; 0x0000 - Size of 0 indicates end of data stream

```

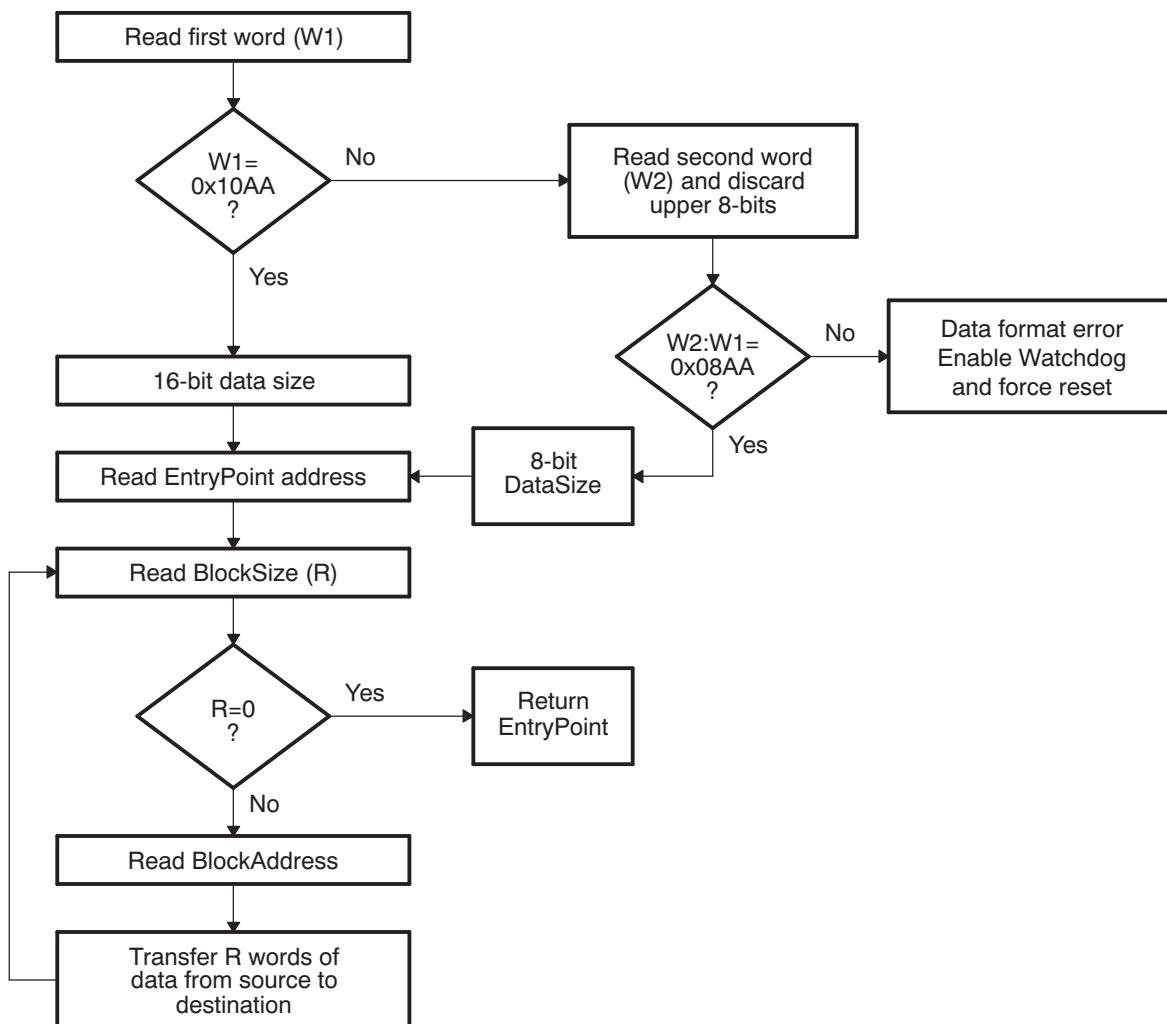
After load has completed the following memory values will have been initialized as follows:

Location	Value
0x3F9010	0x0001
0x3F9011	0x0002
0x3F9012	0x0003
0x3F9013	0x0004
0x3F9014	0x0005
0x3F8000	0x7700
0x3F8001	0x7625
PC Begins execution at	0x3F8000

2.26.2 Basic Data Transfer Procedure

Figure 2-8 illustrates the basic process a bootloader uses to determine whether 8-bit or 16-bit data stream has been selected, transfer that data, and start program execution. This process occurs after the bootloader finds the valid boot mode selected by the state of $\overline{\text{TRST}}$ and GPIO pins.

The loader first compares the first value sent by the host against the 16-bit key value of 0x10AA. If the value fetched does not match then the loader will read a second value. This value will be combined with the first value to form a word. This will then be checked against the 8-bit key value of 0x08AA. If the loader finds that the header does not match either the 8-bit or 16-bit key value, or if the value is not valid for the given boot mode then the load will abort.

Figure 2-8. Bootloader Basic Transfer Procedure


8-bit and 16-bit transfers are not valid for all boot modes. If only one mode is valid, then this decision tree is skipped and the key value is only checked for correctness. See the info specific to a particular bootloader for any limitations.

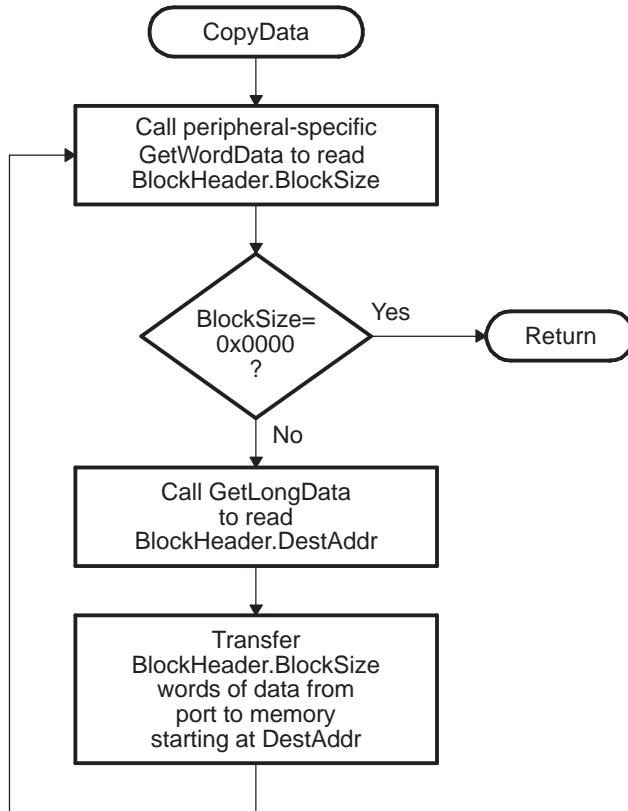
In 8-bit mode, the LSB of the 16-bit word is read first followed by the MSB.

2.26.3 CopyData Function

Each of the bootloaders uses the same function to copy data from the port to the device's SARAM. This function is the CopyData() function. This function uses a pointer to a GetWordData function that is initialized by each of the loaders to properly read data from that port. For example, when the SPI loader is evoked, the GetWordData function pointer is initialized to point to the SPI-specific SPI_GetWordData function. Thus when the CopyData() function is called, the correct port is accessed. The flow of the CopyData function is shown in [Figure 2-9](#).

Note: BlockSize must be less than 0xFFFF for correct operation of the CopyData function. This means the max possible value of BlockSize is 0xFFFE, not 0xFFFF.

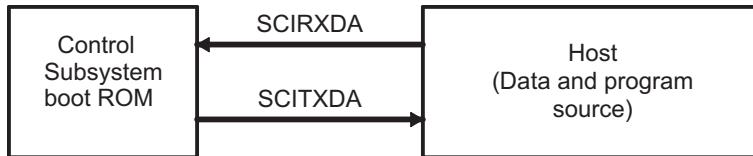
Figure 2-9. Overview of CopyData Function



2.26.4 Boot ROM SCI_Boot Mode

The SCI boot mode asynchronously transfers code from SCI-A to internal memory. This boot mode only supports an incoming 8-bit data stream and follows the same data flow as outlined in [Example 2-2](#).

Figure 2-10. Overview of SCI Bootloader Operation



The device communicates with the external host device by communication through the SCI-A peripheral. The autobaud feature of the SCI port is used to lock baud rates with the host. For this reason the SCI loader is very flexible and you can use a number of different baud rates to communicate with the device.

After each data transfer, the 28x will echo back the 8-bit character received to the host. In this manner, the host can perform checks that each character was received by the 28x.

At higher baud rates, the slew rate of the incoming data bits can be effected by transceiver and connector performance. While normal serial communications may work well, this slew rate may limit reliable auto-baud detection at higher baud rates (typically beyond 100kbaud) and cause the auto-baud lock feature to fail. To avoid this, the following is recommended:

1. Achieve a baud-lock between the host and 28x SCI bootloader using a lower baud rate.
2. Load the incoming 28x application or custom loader at this lower baud rate.
3. The host may then handshake with the loaded 28x application to set the SCI baud rate register to the desired high baud rate.

Figure 2-11. Overview of SCI_Boot Function

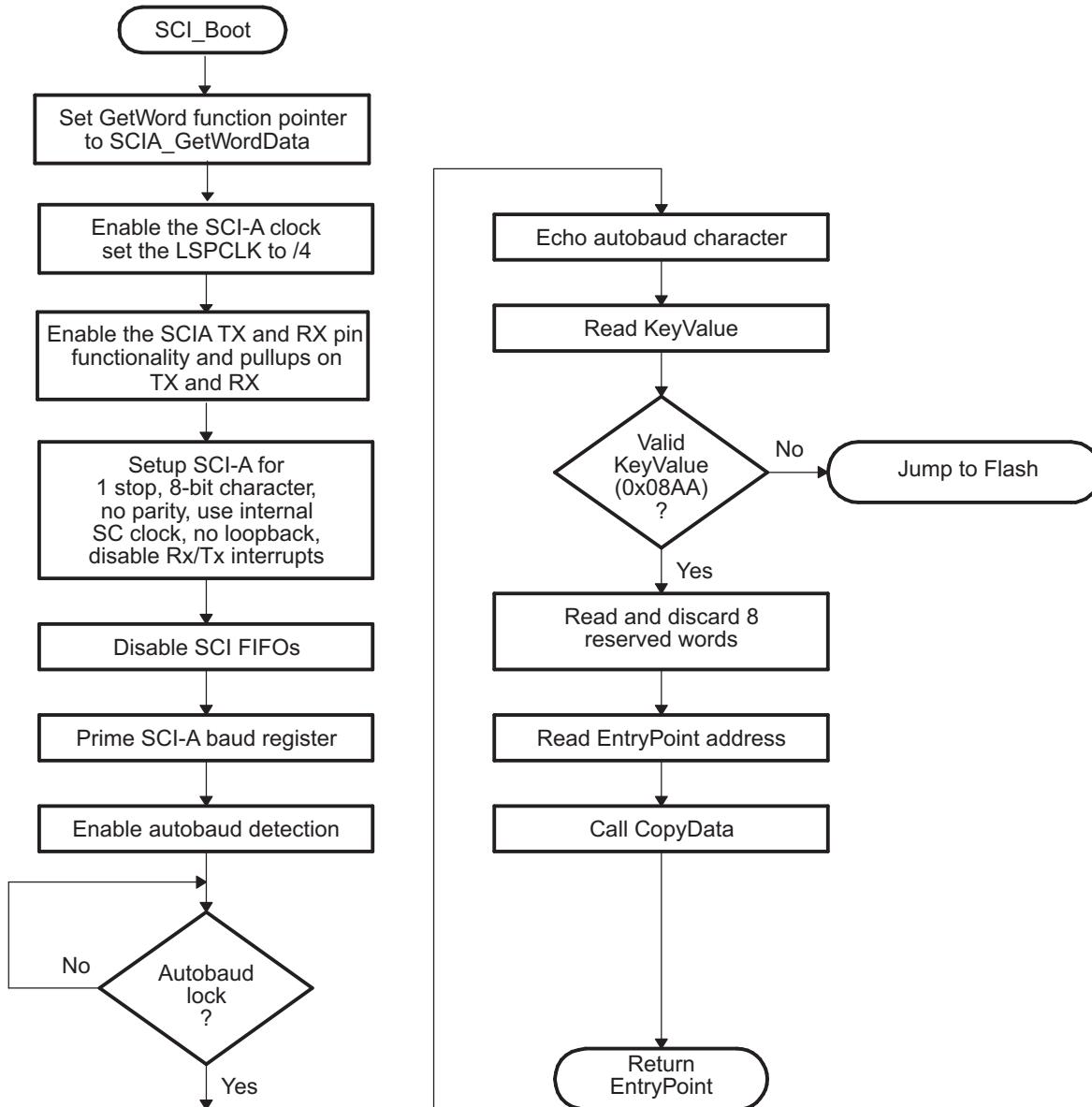
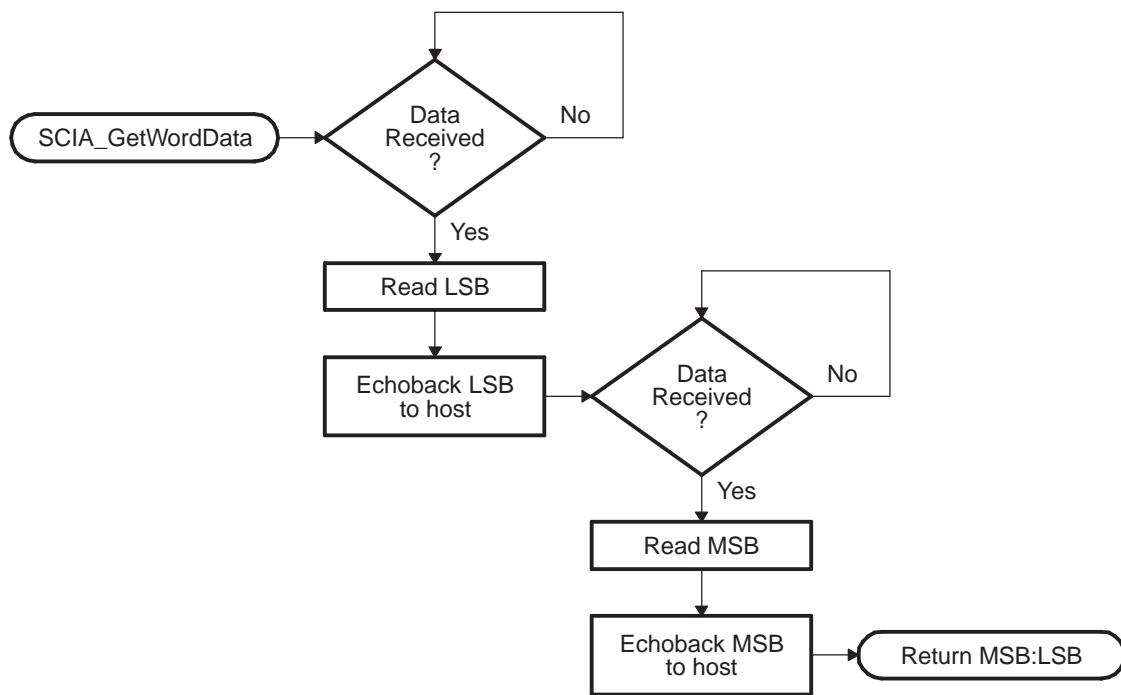


Figure 2-12. Overview of SCI_GetWordData Function

2.26.5 Boot ROM SPI Boot Mode

The SPI loader expects an SPI-compatible 16-bit or 24-bit addressable serial EEPROM or serial flash device to be present on the SPI-A pins as indicated in [Figure 2-13](#). The SPI bootloader supports an 8-bit data stream. It does not support a 16-bit data stream.

Figure 2-13. SPI Loader



The SPI boot ROM loader initializes the SPI module to interface to a serial SPI EEPROM or flash. Devices of this type include, but are not limited to, the Xicor X25320 (4Kx8) and Xicor X25256 (32Kx8) SPI serial SPI EEPROMs and the Atmel AT25F1024A serial flash.

The SPI boot ROM loader initializes the SPI with the following settings: FIFO enabled, 8-bit character, internal SPICLK master mode and talk mode, clock phase = 1, polarity = 0, using the slowest baud rate.

If the download is to be performed from an SPI port on another device, then that device must be setup to operate in the slave mode and mimic a serial SPI EEPROM. Immediately after entering the SPI_Boot function, the pin functions for the SPI pins are set to primary and the SPI is initialized. The initialization is done at the slowest speed possible. Once the SPI is initialized and the key value read, you could specify a change in baud rate or low speed peripheral clock.

Table 2-20. SPI 8-Bit Data Stream

Byte	Contents
1	LSB: AA (KeyValue for memory width = 8-bits)
2	MSB: 08h (KeyValue for memory width = 8-bits)
3	LSB: LOSPCP
4	MSB: SPIBRR
5	LSB: reserved for future use
6	MSB: reserved for future use
...	...
...	Data for this section.
...	...
17	LSB: reserved for future use
18	MSB: reserved for future use
19	LSB: Upper half (MSW) of Entry point PC[23:16]
20	MSB: Upper half (MSW) of Entry point PC[31:24] (Note: Always 0x00)
21	LSB: Lower half (LSW) of Entry point PC[7:0]
22	MSB: Lower half (LSW) of Entry point PC[15:8]
...	...
...	Data for this section.
...	...
...	Blocks of data in the format size/destination address/data as shown in the generic data stream description
...	...
...	Data for this section.
...	...
n	LSB: 00h
n+1	MSB: 00h - indicates the end of the source

The data transfer is done in "burst" mode from the serial SPI EEPROM. The transfer is carried out entirely in byte mode (SPI at 8 bits/character). A step-by-step description of the sequence follows:

- Step 1. The SPI-A port is initialized
- Step 2. The GPIO19 (SPISTE) pin is used as a chip-select for the serial SPI EEPROM or flash
- Step 3. The SPI-A outputs a read command for the serial SPI EEPROM or flash
- Step 4. The SPI-A sends the serial SPI EEPROM an address 0x0000; that is, the host requires that the EEPROM or flash must have the downloadable packet starting at address 0x0000 in the EEPROM or flash. The loader is compatible with both 16-bit addresses and 24-bit addresses.
- Step 5. The next word fetched must match the key value for an 8-bit data stream (0x08AA). The least significant byte of this word is the byte read first and the most significant byte is the next byte fetched. This is true of all word transfers on the SPI. If the key value does not match, then the load is aborted and
- Step 6. The next 2 bytes fetched can be used to change the value of the low speed peripheral clock register (LOSPCP) and the SPI baud rate register (SPIBRR). The first byte read is the LOSPCP value and the second byte read is the SPIBRR value. The next 7 words are reserved for future enhancements. The SPI bootloader reads these 7 words and discards them.
- Step 7. The next 2 words makeup the 32-bit entry point address where execution will continue after the boot load process is complete. This is typically the entry point for the program being downloaded through the SPI port.
- Step 8. Multiple blocks of code and data are then copied into memory from the external serial SPI EEPROM through the SPI port. The blocks of code are organized in the standard data stream structure presented earlier. This is done until a block size of 0x0000 is encountered. At that point in time the entry point address is returned to the calling routine that then exits the bootloader and resumes execution at the address specified.

Figure 2-14. Data Transfer From EEPROM Flow

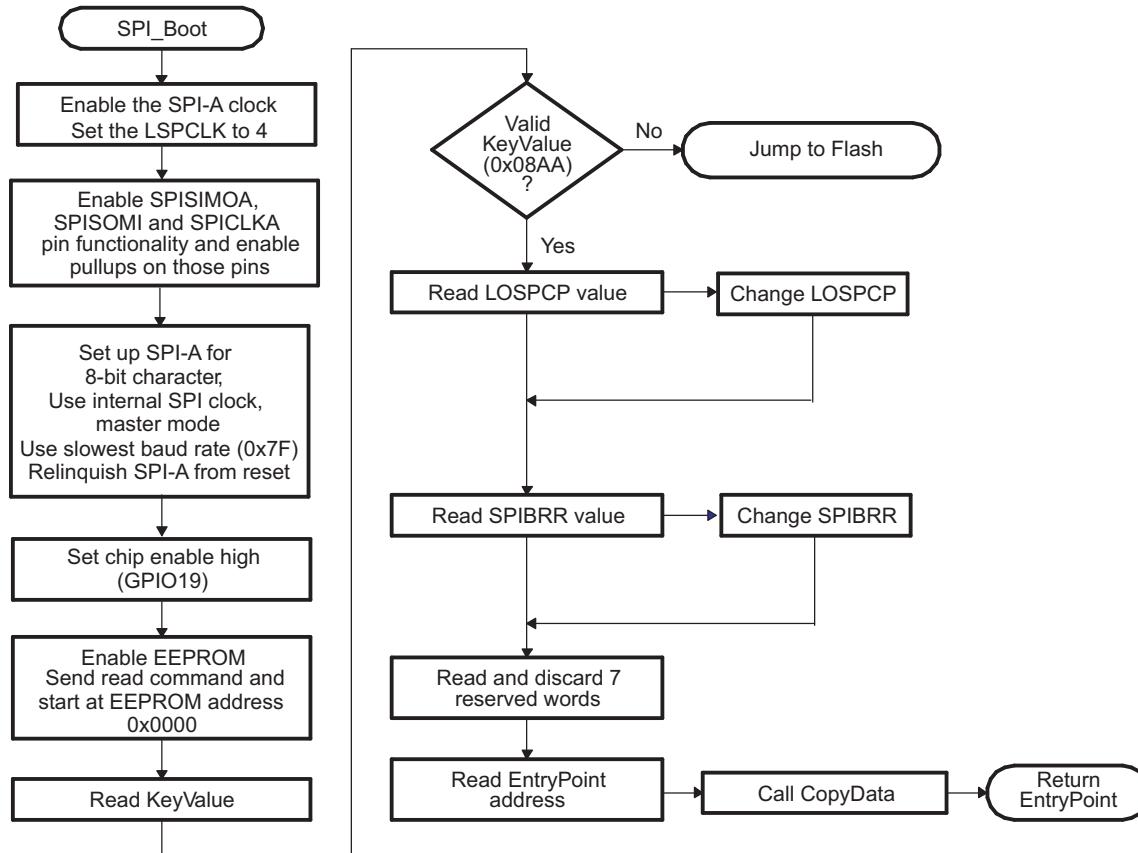
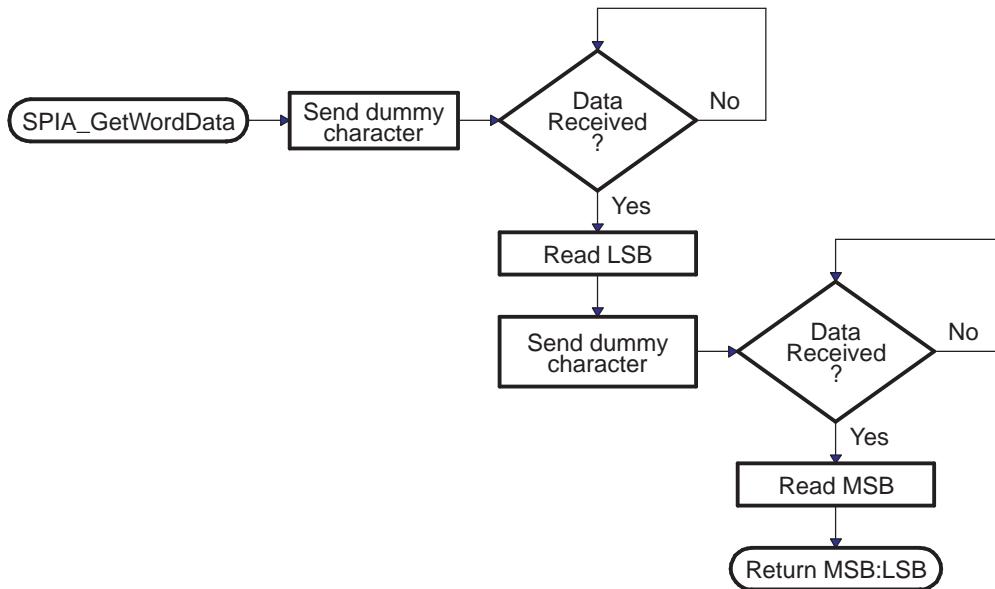


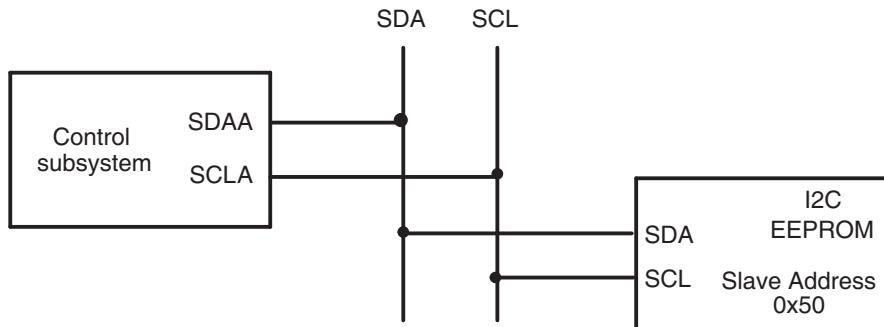
Figure 2-15. Overview of SPIA_GetWordData Function



2.26.6 Boot ROM I2C Boot Mode

The I2C bootloader expects an 8-bit wide I2C-compatible EEPROM device to be present at address 0x50 on the I2C-A bus as indicated in [Figure 2-16](#). The EEPROM must adhere to conventional I2C EEPROM protocol, as described in this section, with a 16-bit base address architecture.

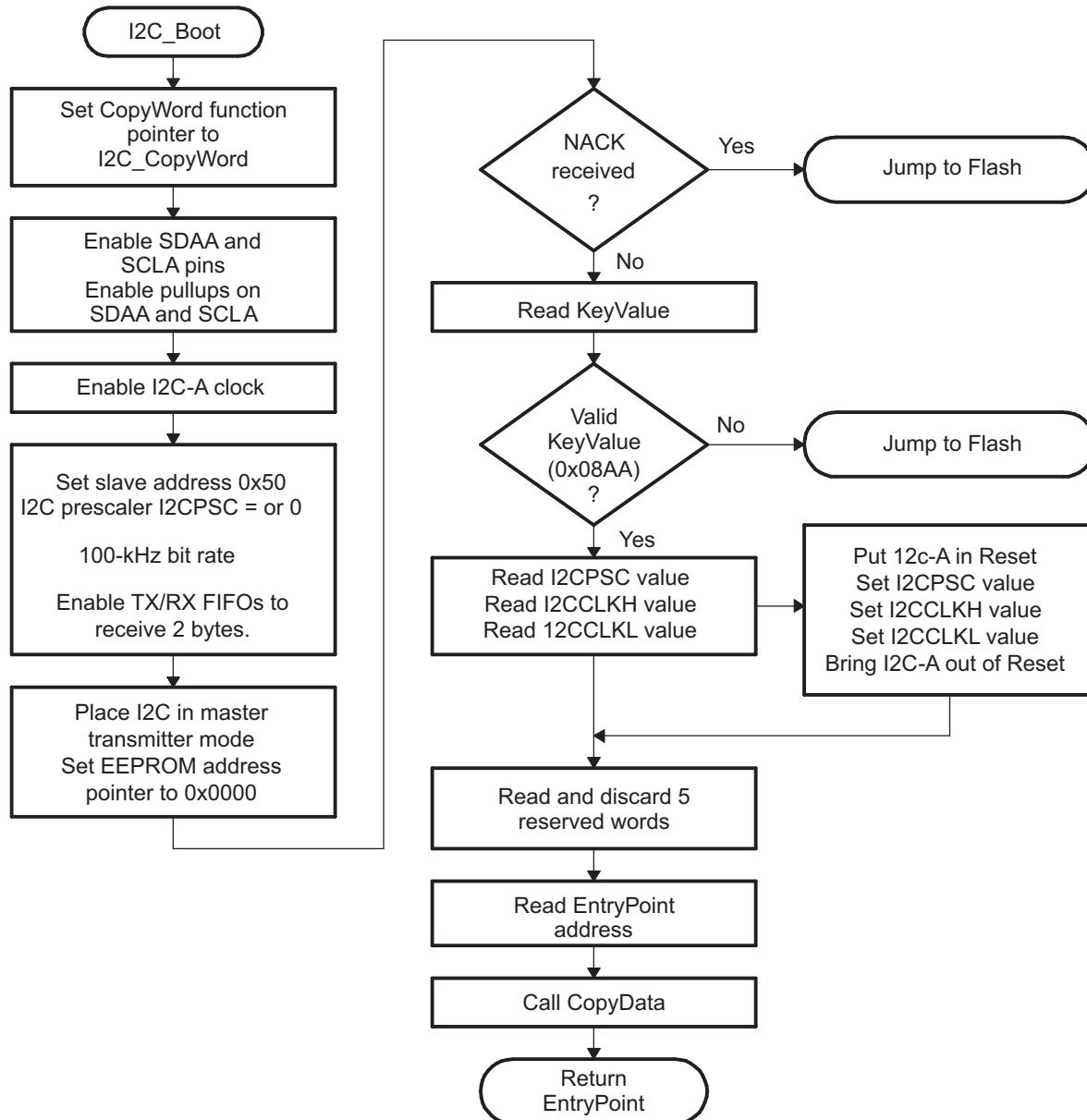
Figure 2-16. EEPROM Device at Address 0x50



If the download is to be performed from a device other than an EEPROM, then that device must be set up to operate in the slave mode and mimic the I2C EEPROM. Immediately after entering the I2C boot function, the GPIO pins are configured for I2C-A operation and the I2C is initialized. The following requirements must be met when booting from the I2C module:

- The input frequency to the device must be in the appropriate range.
- The EEPROM must be at slave address 0x50.

Figure 2-17. Overview of I2C_Boot Function



The bit-period prescalers (I2CCLKH and I2CCLKL) are configured by the bootloader to run the I2C at a 50 percent duty cycle at 100-kHz bit rate (standard I2C mode) when the system clock is 10 MHz. These registers can be modified after receiving the first few bytes from the EEPROM. This allows the communication to be increased up to a 400-kHz bit rate (fast I2C mode) during the remaining data reads.

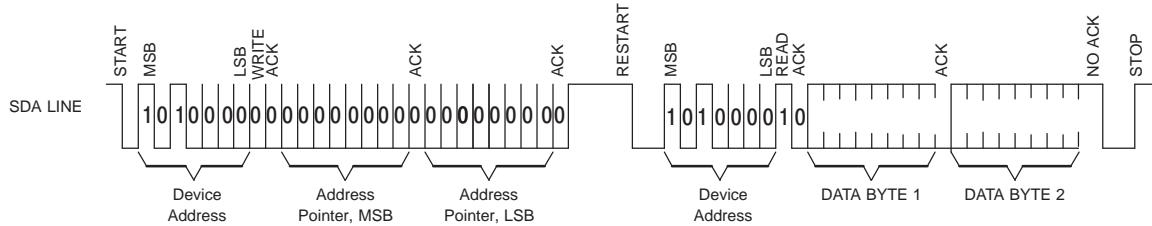
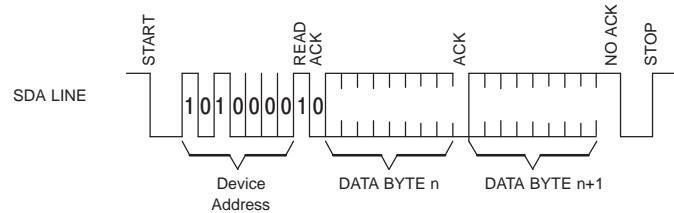
Arbitration, bus busy, and slave signals are not checked. Therefore, no other master is allowed to control the bus during this initialization phase. If the application requires another master during I2C boot mode, that master must be configured to hold off sending any I2C messages until the application software signals that it is past the bootloader portion of initialization.

The non-acknowledgment bit is checked only during the first message sent to initialize the EEPROM base address. This is to make sure that an EEPROM is present at address 0x50 before continuing. If an EEPROM is not present, code will The non-acknowledgment bit is not checked during the address phase of the data read messages (I2C_Get Word). If a non acknowledgment is received during the data read messages, the I2C bus will hang. Table 12-1 shows the 8-bit data stream used by the I2C.

Table 2-21. I2C 8-Bit Data Stream

Byte	Contents
1	LSB: AA (KeyValue for memory width = 8 bits)
2	MSB: 08h (KeyValue for memory width = 8 bits)
3	LSB: I2CPSC[7:0]
4	reserved
5	LSB: I2CCLKH[7:0]
6	MSB: I2CCLKH[15:8]
7	LSB: I2CCLKL[7:0]
8	MSB: I2CCLKL[15:8]
...	...
...	Data for this section.
...	...
17	LSB: Reserved for future use
18	MSB: Reserved for future use
19	LSB: Upper half of entry point PC
20	MSB: Upper half of entry point PC[22:16] (Note: Always 0x00)
21	LSB: Lower half of entry point PC[15:8]
22	MSB: Lower half of entry point PC[7:0]
...	...
...	Data for this section.
...	...
n	LSB: 00h
n+1	MSB: 00h - indicates the end of the source

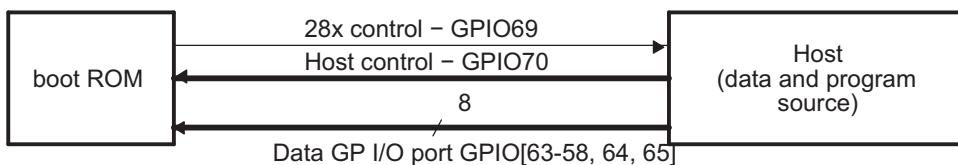
The I2C EEPROM protocol required by the I2C bootloader is shown in [Figure 2-18](#) and [Figure 2-19](#). The first communication, which sets the EEPROM address pointer to 0x0000 and reads the KeyValue (0x08AA) from it, is shown in [Figure 2-18](#). All subsequent reads are shown in [Figure 2-19](#) and are read two bytes at a time.

Figure 2-18. Random Read**Figure 2-19. Sequential Read**

2.26.7 Parallel Boot Mode Protocol

The parallel general purpose I/O (GPIO) boot mode asynchronously transfers code from GPIO0 -GPIO5, GPIO8-GPIO9 to internal memory. Each value is 8 bits long and follows the same data flow as outlined in Figure 2-20.

Figure 2-20. Overview of Parallel GPIO Bootloader Operation



The control subsystem communicates with the external host device by polling/driving the GPIO70 and GPIO69 lines. The handshake protocol shown in Figure 2-21 must be used to successfully transfer each word via GPIO [63-58,64,65]. This protocol is very robust and allows for a slower or faster host to communicate with the master subsystem.

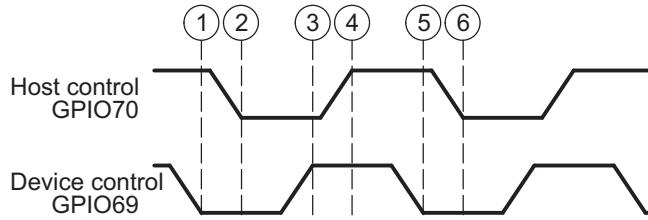
Two consecutive 8-bit words are read to form a single 16-bit word. The most significant byte (MSB) is read first followed by the least significant byte (LSB). In this case, data is read from GPIO[63-58,64,65].

The 8-bit data stream is shown in Table 2-22.

Table 2-22. Parallel GPIO Boot 8-Bit Data Stream

Bytes		GPIO[9,8,5:0] (Byte 1 of 2)	GPIO[9,8,5:0] (Byte 2 of 2)	Description
1	2	AA	08	0x08AA (KeyValue for memory width = 16bits)
3	4	00	00	8 reserved words (words 2 - 9)
...
17	18	00	00	Last reserved word
19	20	BB	00	Entry point PC[22:16]
21	22	DD	CC	Entry point PC[15:0] (PC = 0x00BBCCDD)
23	24	NN	MM	Block size of the first block of data to load = 0xMMNN words
25	26	BB	AA	Destination address of first block Addr[31:16]
27	28	DD	CC	Destination address of first block Addr[15:0] (Addr = 0xAABBCCDD)
29	30	BB	AA	First word of the first block in the source being loaded = 0xAABB
...	Data for this section.
.		BB	AA	Last word of the first block of the source being loaded = 0xAABB
.		NN	MM	Block size of the 2nd block to load = 0xMMNN words
.		BB	AA	Destination address of second block Addr[31:16]
.		DD	CC	Destination address of second block Addr[15:0]
.		BB	AA	First word of the second block in the source being loaded
.		
n	n+1	BB	AA	Last word of the last block of the source being loaded (More sections if required)
n+2	n+3	00	00	Block size of 0000h - indicates end of the source program

The device first signals the host that it is ready to begin data transfer by pulling the GPIO69 pin low. The host load then initiates the data transfer by pulling the GPIO70 pin low. The complete protocol is shown in [Figure 2-21](#):

Figure 2-21. Parallel GPIO Bootloader Handshake Protocol

1. The device indicates it is ready to start receiving data by pulling the GPIO69 pin low.
2. The bootloader waits until the host puts data on GPIO [63-58,64,65]. The host signals to the device that data is ready by pulling the GPIO70 pin low.
3. The device reads the data and signals the host that the read is complete by pulling GPIO69 high.
4. The bootloader waits until the host acknowledges the device by pulling GPIO70 high.
5. The device again indicates it is ready for more data by pulling the GPIO69 pin low.

This process is repeated for each data value to be sent.

[Figure 2-22](#) shows an overview of the Parallel GPIO bootloader flow.

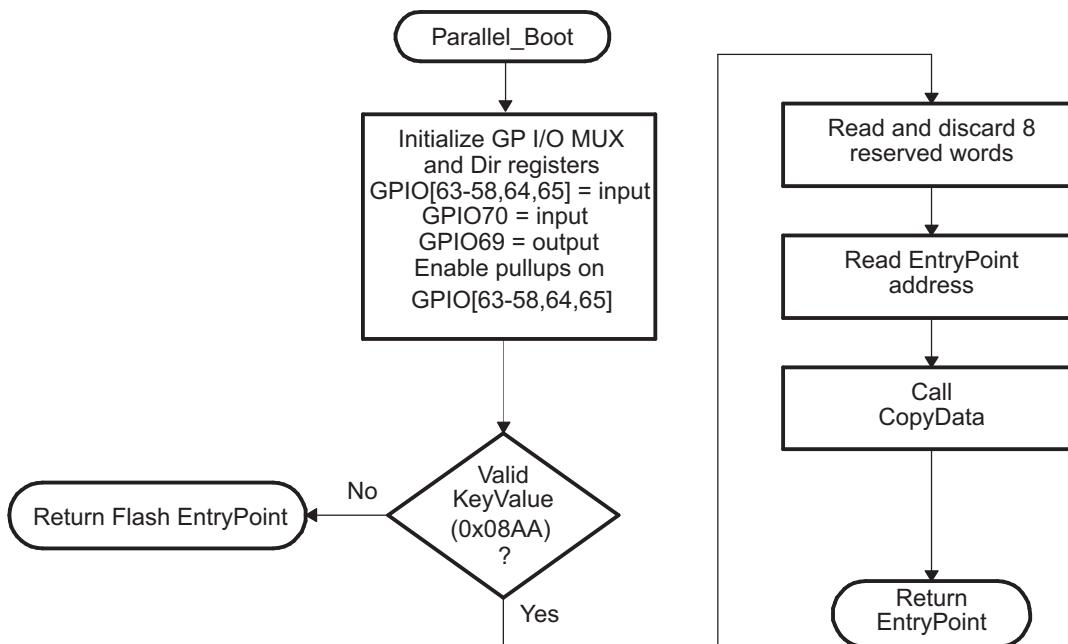
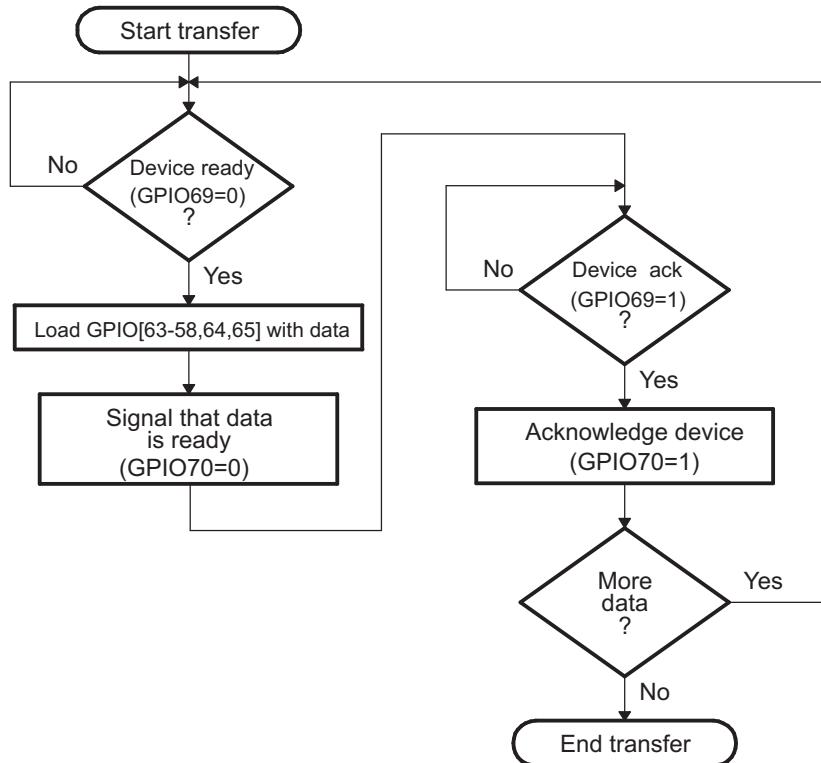
Figure 2-22. Parallel GPIO Mode Overview

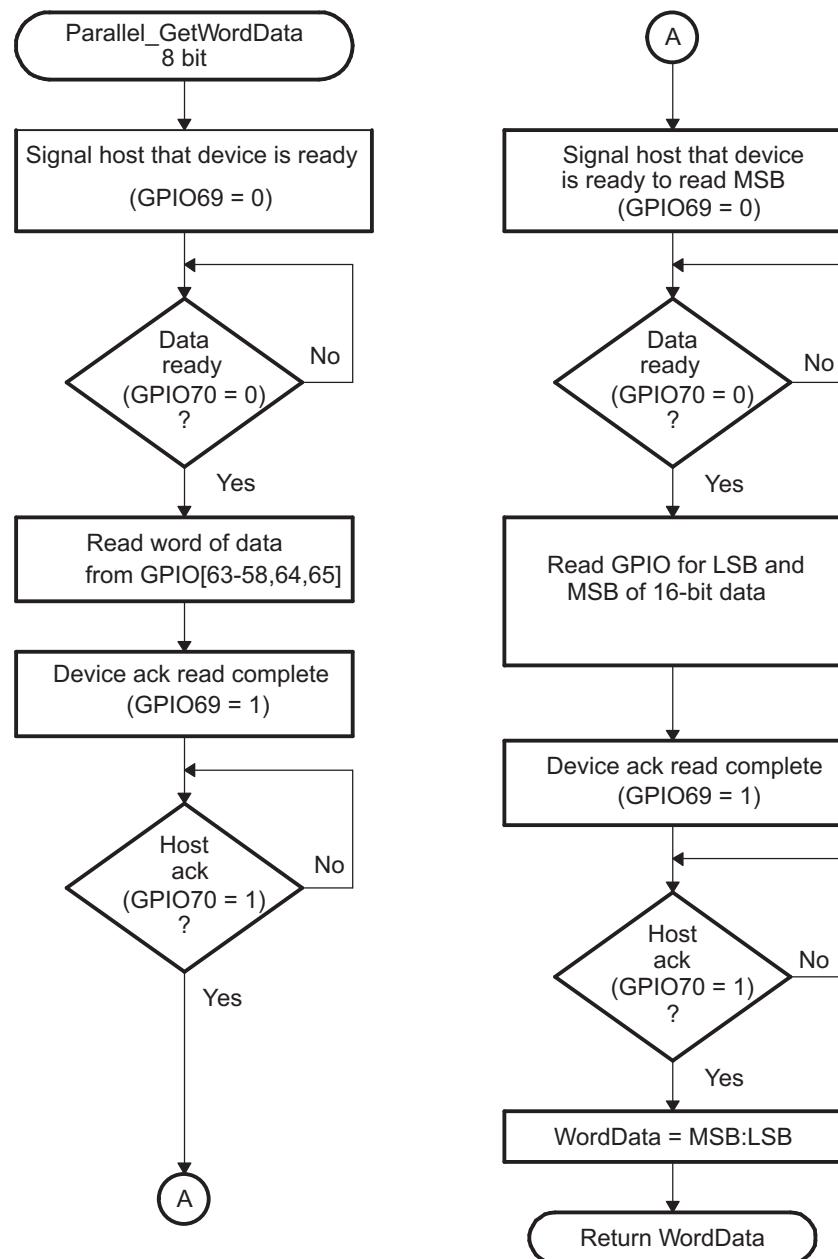
Figure 2-23 shows the transfer flow from the host side. The operating speed of the CPU and host are not critical in this mode as the host will wait for the device and the device will in turn wait for the host. In this manner the protocol will work with both a host running faster and a host running slower than the device.

Figure 2-23. Parallel GPIO Mode - Host Transfer Flow

[Figure 2-24](#) shows the flow used to read a single word of data from the parallel port.

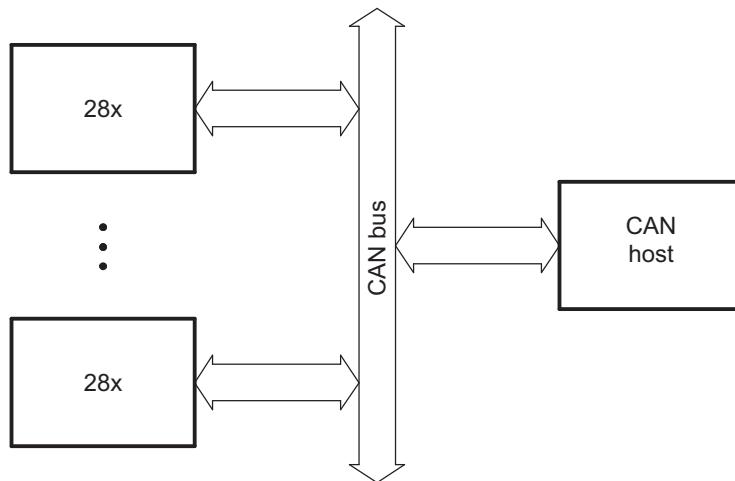
- **8-bit data stream**

The 8-bit routine, shown in [Figure 2-24](#), discards the upper 8 bits of the first read from the port and treats the lower 8 bits masked with GPIO9 in bit position 7 and GPIO8 in bit position 6 as the least significant byte (LSB) of the word to be fetched. The routine will then perform a second read to fetch the most significant byte (MSB). The routine will then perform a second read to fetch the most significant byte (MSB). It then combines the MSB and LSB into a single 16-bit value to be passed back to the calling routine.

Figure 2-24. 8-Bit Parallel GetWord Function

2.26.8 CAN Boot Function

The CAN bootloader asynchronously transfers code from CAN-A to internal memory. The host can be any CAN node. The communication is first done with 11-bit standard identifiers (with a MSGID of 0x1) using two bytes per data frame. The host can download a kernel to reconfigure the CAN if higher data throughput is desired.

Figure 2-25. Overview of CAN-A Bootloader Operation

The bit-timing registers are programmed in such a way that a valid bit-rate is achieved for a 10 MHz internal oscillator frequency as shown in [Table 2-23](#).

Table 2-23. Bit-Rate Value for Internal Oscillators

OSCCLK	SYSCLKOUT	Bit Rate
10 MHz	10 MHz	50 kbps

The SYSCLKOUT values shown are the reset values with the default PLL setting. The BRP and bit-time values are hard-coded to 10 and 20, respectively.

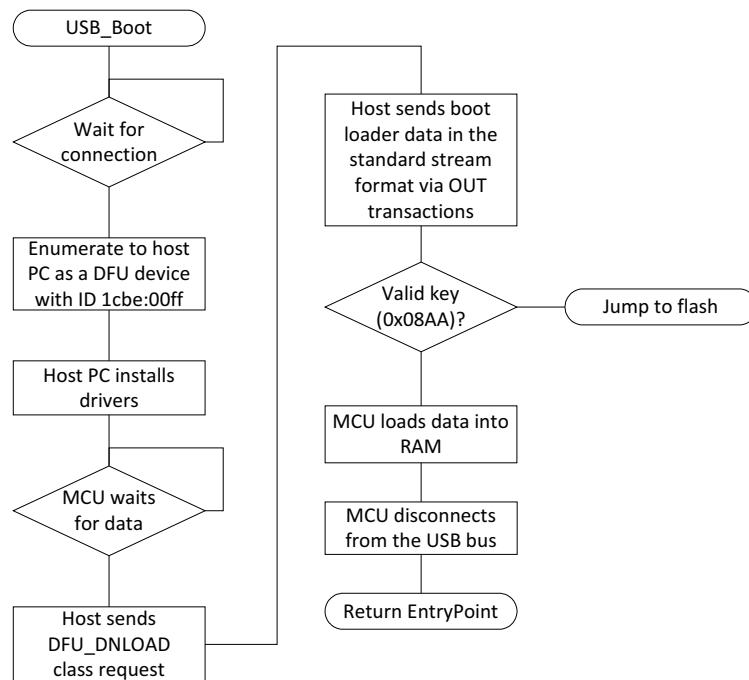
Mailbox 1 is programmed with a standard MSGID of 0x1 for boot-loader communication. The CAN host should transmit only 2 bytes at a time, LSB first and MSB next. For example, to transmit the word 0x08AA to the device, transmit AA first, followed by 08. The program flow of the CAN bootloader is identical to the SCI bootloader. The data sequence for the CAN bootloader is shown in [Table 2-24](#):

Table 2-24. CAN 8-Bit Data Stream

Bytes		Byte 1 of 2	Byte 2 of 2	Description
1	2	AA	08	0x08AA (KeyValue for memory width = 16bits)
3	4	00	00	reserved
5	6	00	00	reserved
7	8	00	00	reserved
9	10	00	00	reserved
11	12	00	00	reserved
13	14	00	00	reserved
15	16	00	00	reserved
17	18	00	00	reserved
19	20	BB	AA	Entry point PC[22:16]
21	22	DD	CC	Entry point PC[15:0] (PC = 0xAABBCCDD)
23	24	NN	MM	Block size of the first block of data to load = 0xMMNN words
25	26	BB	AA	Destination address of first block Addr[31:16]
27	28	DD	CC	Destination address of first block Addr[15:0] (Addr = 0xAABBCCDD)
29	30	BB	AA	First word of the first block in the source being loaded = 0xAABB
...			...	
...				Data for this section.
...				...
.		BB	AA	Last word of the first block of the source being loaded = 0xAABB
.		NN	MM	Block size of the 2nd block to load = 0xMMNN words
.		BB	AA	Destination address of second block Addr[31:16]
.		DD	CC	Destination address of second block Addr[15:0]
.		BB	AA	First word of the second block in the source being loaded
...				...
n	n+1	BB	AA	Last word of the last block of the source being loaded (More sections if required)
n+2	n+3	00	00	Block size of 0000h - indicates end of the source program

2.26.9 USB Boot Mode

In USB boot mode, the device will enumerate as a standard USB Device Firmware Update (DFU) device with vendor ID 0x1cbe and product ID 0x00ff. There is no reconfiguration phase. After enumeration, data can be transferred via DFU_DNLOAD control requests. The data format is the same as in I2C boot mode. Once the data transfer is complete (block size of 0x0000 sent), the device will immediately disconnect from the USB bus, allowing other software to make use of the module if desired. Implementing PC-side USB software is not trivial. It is strongly recommended to use the TI-provided tools and drivers to load data in USB boot mode. If custom software is required, there are third-party libraries that can handle most of the work. One lightweight and easy-to-use option is libusb0x. [Figure 2-26](#) illustrates the flow for USB boot mode.

Figure 2-26. USB Boot Flow

2.27 CLA Data ROM

Both CPU1 and CPU2 on the device support CLA data ROM and this data ROM has some Math tables for CLA application usage. This section provides details about this.

2.27.1 CPU1/CPU2 CLA Data ROM

2.27.1.1 CLA Data ROM Map

```

CLAlmathTables
*      1    01001870  00000784    CLAatanTable.obj (CLAlmathTables)
          01001870  0000018c    CLAasinTable.obj (CLAlmathTables)
          010019fc  0000018a    CLAacosineTable.obj (CLAlmathTables)
          01001b86  00000184    CLASinCosTable.obj (CLAlmathTables)
          01001d0a  00000156    CLAInTable.obj (CLAlmathTables)
          01001e60  000000d2    CLAexpTable.obj (CLAlmathTables)
          01001f32  000000c2

$fill1006  1    01001ff4  00000006    --HOLE-- [fill = ffff]
          01001ff4  00000006

.CROMVersion
*      1    01001ffa  00000002    cla_rom_version.obj (.CROMVersion)
          01001ffa  00000002

$fill1007  1    01001ffc  00000004    --HOLE-- [fill = ffff]
          01001ffc  00000004
  
```

2.27.1.2 CLA Data ROM Tables

Table 2-25. CLA Data ROM Tables

	Start Address From CLA in Hex	Start Address From CPU in Hex
_CLAatan2HalfPITable	F870	01001870
_CLAINV2PI	F874	01001874
_CLAatan2Table	F876	01001876
_CLAasinHalfPITable	F9fc	010019fc
_CLAatan2TableEnd	F9fc	010019fc
_CLAasinTable	Fa00	01001a00
_CLAacosinHalfPITable	Fb86	01001b86
_CLAasinTableEnd	Fb86	01001b86
_CLAacosinTable	Fb8a	01001b8a
_CLAacosinTableEnd	Fd0a	01001d0a
_CLAsinTable	Fd0a	01001d0a
_CLAsincosTable	Fd0a	01001d0a
_CLAsincosTable_Sin0	Fd0a	01001d0a
_CLAcosTable	Fd4a	01001d4a
_CLAsincosTable_Coso	Fd4a	01001d4a
_CLAsinTableEnd	Fe0a	01001e0a
_CLAcosTableEnd	Fe4c	01001e4c
_CLAsincosTable_TABLE_SIZE	Fe4c	01001e4c
_CLAsincosTable_TABLE_SIZEDivTwoPi	Fe4e	01001e4e
_CLAsincosTable_TwoPiDivTABLE_SIZE	Fe50	01001e50
_CLAsincosTable_TABLE_MASK	Fe52	01001e52
_CLAsincosTable_Coef0	Fe54	01001e54
_CLAsincosTable_Coef1	Fe56	01001e56
_CLAsincosTable_Coef1_pos	Fe58	01001e58
_CLAsincosTable_Coef2	Fe5a	01001e5a
_CLAsincosTable_Coef3	Fe5c	01001e5c
_CLAsincosTable_Coef3_neg	Fe5e	01001e5e
_CLALNV2	Fe60	01001e60
_CLAsincosTableEnd	Fe60	01001e60
_CLALNve	Fe62	01001e62
_CLALNV10	Fe64	01001e64
_CLABIAS	Fe66	01001e66
_CLALN_TABLE_MASK1	Fe68	01001e68
_CLALN_TABLE_MASK2	Fe6a	01001e6a
_CLALnTable	Fe6c	01001e6c
_CLAINV1	Ff32	01001f32
_CLALnTableEnd	Ff32	01001f32
_CLAINV2	Ff34	01001f34
_CLAINV3	Ff36	01001f36
_CLAINV4	Ff38	01001f38
_CLAINV5	Ff3a	01001f3a
_CLAINV6	Ff3c	01001f3c
_CLAINV7	Ff3e	01001f3e
_CLALOG10	Ff40	01001f40
_CLAExpTable	Ff42	01001f42
_CLAExpTableEnd	Fff4	01001ff4
CROM VERSION	FFFF	01001FFA (2 16-bit words)

Table 2-25. CLA Data ROM Tables (continued)

	Start Address From CLA in Hex	Start Address From CPU in Hex
		.word 0x0100 ; Boot ROM Version v1.0 .word 0x0413 ; Month/Year: (ex: 0x0109 = 1/09 = Jan 2009)

2.28 Secure ROM Contents

Secure ROM on CPU1/CPU2 has no libraries programmed on REV0 of the devices, but below functions are provided in Zx-SCC sections of secure ROM.

```
Z1_SCC_ROM      : origin = 0x3F0000, length = 0x000800, fill = 0xFFFF    /* Zone 1 Safe-
Copy Code Secure ROM */
Z2_SCC_ROM      : origin = 0x3F0800, length = 0x000800, fill = 0xFFFF    /* Zone 2 Safe-
Copy Code Secure ROM */
Z1_SECURE_ROM   : origin = 0x3F1008, length = 0x006FF8, fill = 0xFFFF    /* Z1 Secure ROM
*/
*/
```

2.28.1 CPU1.Secure ROM

Information to be provided.

2.28.1.1 SafeCopyCode

Information to be provided.

2.28.1.2 SafeCRCCalc

Information to be provided.

2.28.2 CPU2.Secure ROM

Information to be provided.

2.28.2.1 SafeCopyCode

Information to be provided.

2.28.2.2 SafeCRCCalc

Information to be provided.

Direct Memory Access (DMA)

The direct memory access (DMA) module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

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3.8 Register Descriptions	608

3.1 Introduction

The strength of a controller is not measured purely in processor speed, but in total system capabilities. As a part of the equation, any time the CPU bandwidth for a given function can be reduced, the greater the system capabilities. Many times applications spend a significant amount of their bandwidth moving data, whether it is from off-chip memory to on-chip memory, or from a peripheral such as an analog-to-digital converter (ADC) to RAM, or even from one peripheral to another. Furthermore, many times this data comes in a format that is not conducive to the optimum processing powers of the CPU. The DMA module described in this reference guide has the ability to free up CPU bandwidth and rearrange the data into a pattern for more streamlined processing.

The DMA module is an event-based machine, meaning it requires a peripheral or software trigger to start a DMA transfer. Although it can be made into a periodic time-driven machine by configuring a timer as the interrupt trigger source, there is no mechanism within the module itself to start memory transfers periodically. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has the ability to be configured at a higher priority than the others. At the heart of the DMA is a state machine and tightly coupled address control logic. It is this address control logic that allows for rearrangement of the block of data during the transfer as well as the process of ping-ponging data between buffers. Each of these features, along with others, will be discussed in detail in this document.

DMA features include:

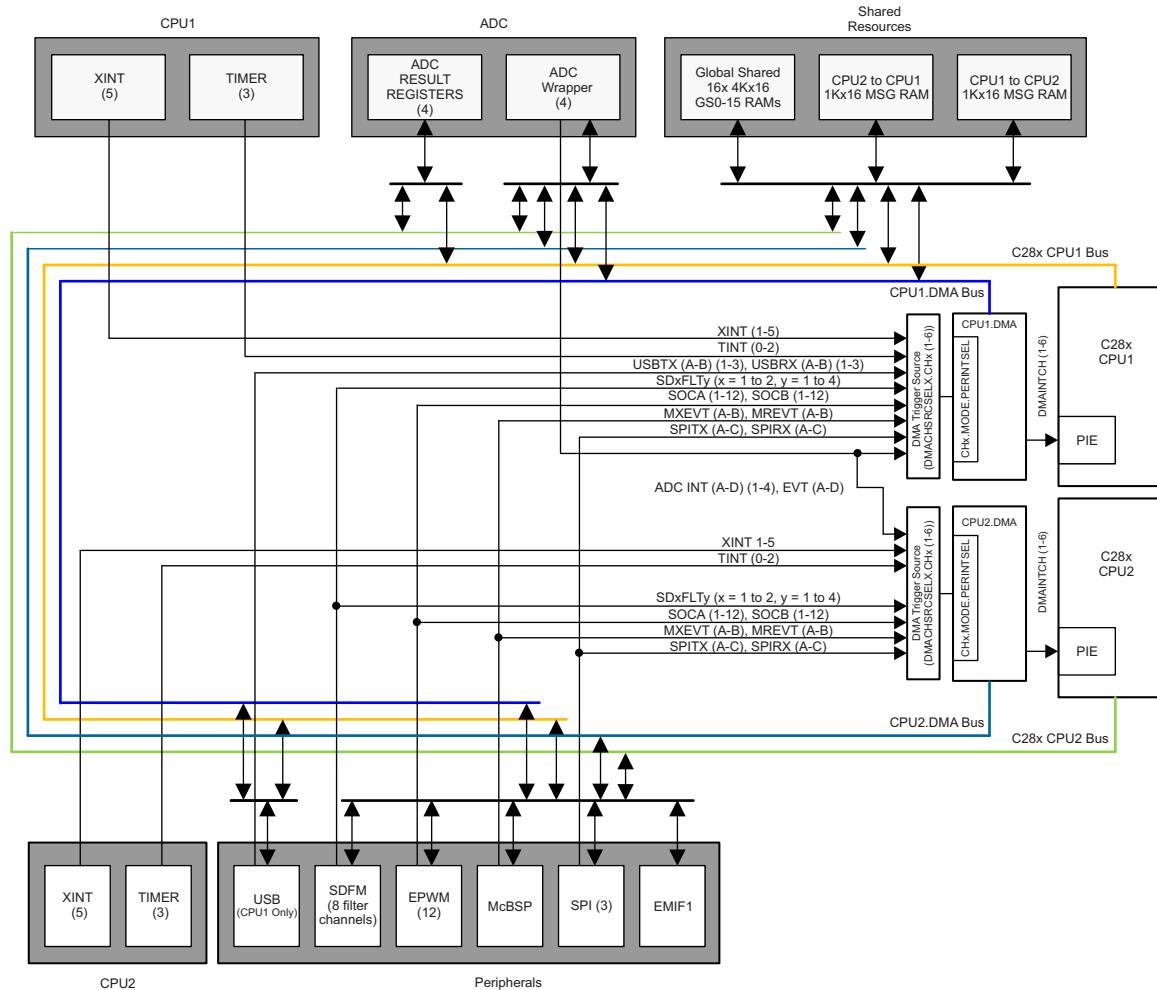
- 6 channels with independent PIE interrupts
- Peripheral interrupt trigger sources
 - ADC interrupts and EVT signals
 - Multichannel buffered serial port transmit and receive
 - External Interrupts
 - CPU Timers
 - EPWMxSOC signals
 - SPI_x transmit and receive
 - USB_x transmit and receive
 - Sigma Delta filter module
 - Software trigger
- Data sources and destinations:
 - GS_x RAM
 - CPU message RAM (IPC RAM)
 - USB RAM
 - ADC memory-bus mapped result registers
 - ePWMx
 - SPI, McBSP, EMIF
- Word Size: 16-bit or 32-bit (SPI and McBSP limited to 16-bit)
- Throughput: 4 cycles/word without arbitration

3.2 Architecture

3.2.1 Block Diagram

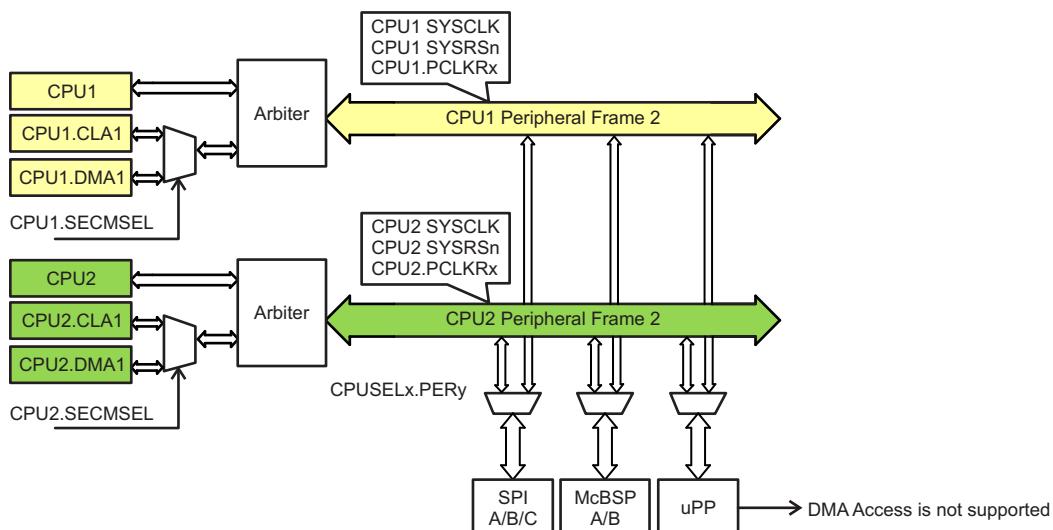
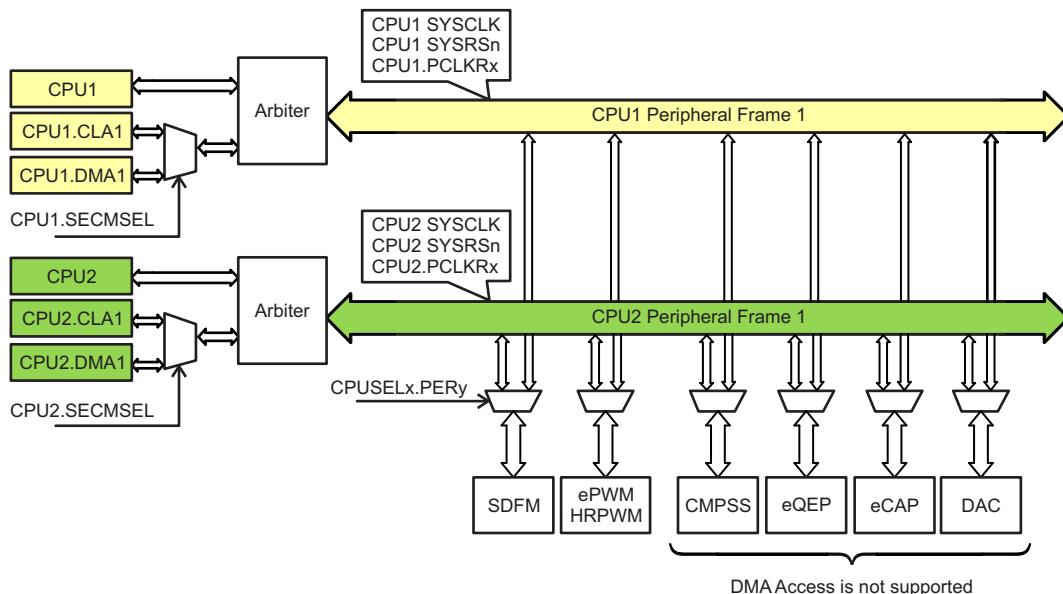
[Figure 3-1](#) shows a device-level block diagram of the DMA.

Figure 3-1. DMA Block Diagram



3.2.2 Common Peripheral Architecture

There are two CPU subsystems; the CPU1 subsystem and CPU2 subsystem, with each containing a CLA and DMA. The architecture allows several peripherals to be common between the two subsystems. Based on application need, these common peripherals can be attached to one of the two subsystems. [Figure 3-2](#) shows how the CPUs and subsystems can be connected to the peripherals on peripheral frames 1 and 2. The clock, clock-enable, and reset muxing for the common peripherals are described in detail in other sections of this document.

Figure 3-2. Common Peripheral Tied to Two CPU Subsystems

A CPUSEL bit associated with each peripheral defines whether the peripheral belongs to the CPU1 or CPU2 subsystem. If a peripheral belongs to a CPU subsystem, it can be accessed by the CPU and one of the secondary masters (DMA1 or CLA1). Refer to CPUSELx register definition for more details. The secondary master is statically selected using the SECSEL register mapped to the respective CPU. Refer to CPUx.SECSEL register definition for more details. If a secondary master is not selected, all writes from that master are ignored and all reads return 0x0 to any of the peripherals.

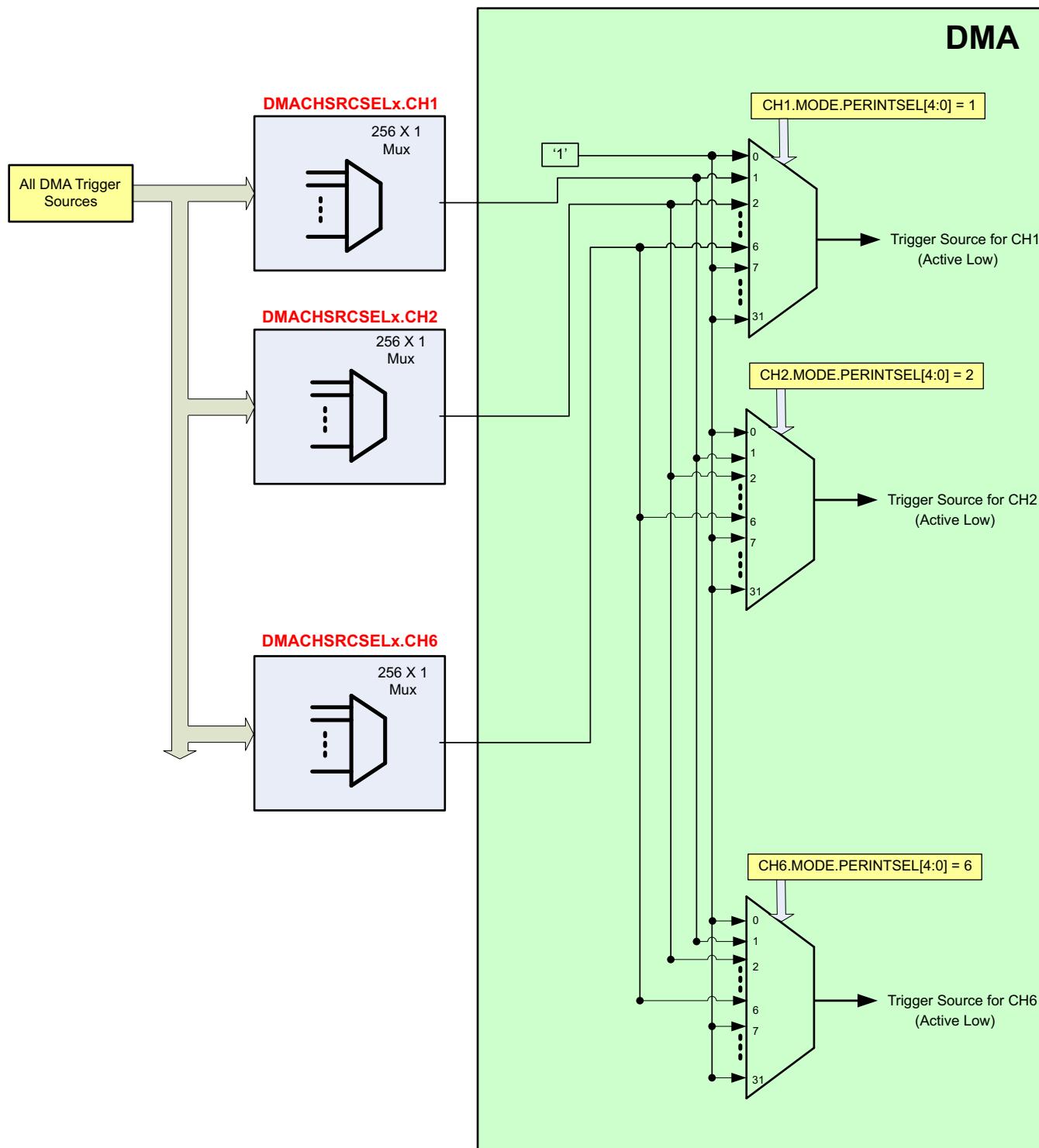
Similarly, if a peripheral does not belong to a CPU subsystem (as defined by the associated CPUSEL bit), all writes to that peripheral are ignored and all reads to that peripheral return 0x0 from any of the masters belonging to the unselected CPU subsystem. Note that since the arbiter has no knowledge regarding the ownership of individual peripherals (as can be seen from [Figure 3-2](#)), arbitration will still happen even if C28x or the selected secondary master tries to access a peripheral which does not belong to its CPU subsystem. See [CPU Arbitration](#) for more information.

Note: If the CPU and DMA make an access to the same peripheral frame in the same cycle, the DMA has priority and the CPU is stalled.

3.2.3 Peripheral Interrupt Event Trigger Sources

As shown in [Figure 3-3](#) the peripheral interrupt event trigger can be independently configured as any of the sources from the DMACHSRCSELx register for each of the six DMA channels. Included in these sources are five external interrupt signals which can be connected to most of the general-purpose input/output (GPIO) pins on the device. This adds significant flexibility to the event trigger capabilities. The DMA trigger source is selected in the DMACHSRCSELx register for each channel. The PERINTSEL in the MODE register of each channel should be set to the channel number (CH2.MODE.PERINTSEL[4:0] = 2). An active peripheral interrupt trigger will be latched into the PERINTFLG bit of the CONTROL register, and if the respective interrupt and DMA channel is enabled (see the MODE.CHx[PERINTE] and CONTROL.CHx[RUNSTS] bits), it will be serviced by the DMA channel. Upon receipt of a peripheral interrupt event signal, the DMA will automatically send a clear signal to the interrupt source so that subsequent interrupt events will occur.

Figure 3-3. DMA Trigger Architecture



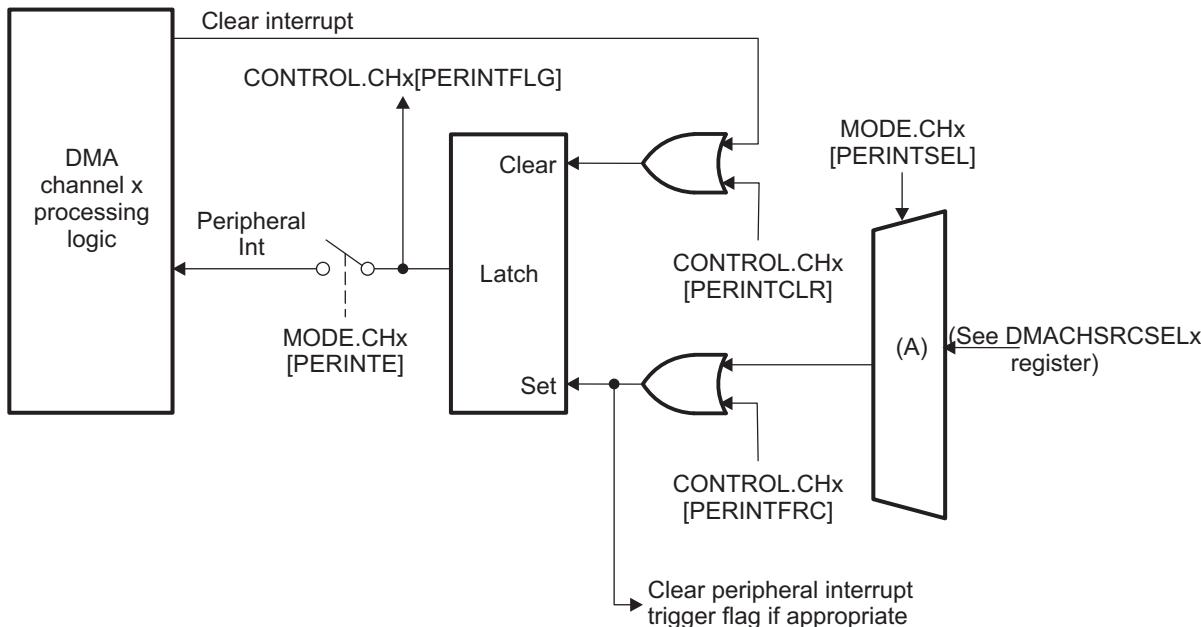
Note: To use the system level DMA Trigger source selection, the DMA internal trigger source selection configuration for each channel should be done using the DMACHSRCSELx register and the CHx.MODE.PERINTSEL register as shown here. See [Table 3-1](#) or the DMACHSRCSELx register definition for a complete list of DMA trigger sources.

Regardless of the value of the MODE.CHx[PERINTSEL] bit field, software can always force a trigger by using the CONTROL.CHx[PERINTFRC] bit. Likewise, software can always clear a pending DMA trigger using the CONTROL.CHx[PERINTCLR] bit.

Once a particular interrupt trigger sets a channel's PERINTFLG bit, the bit stays pending until the priority logic of the state machine starts the burst transfer for that channel. Once the burst transfer starts, the flag is cleared. If a new interrupt trigger is generated while a burst is in progress, the burst will complete before responding to the new interrupt trigger (after proper prioritization). If a third interrupt trigger occurs before the pending interrupt is serviced, an error flag is set in the CONTROL.CHx[OVRFLG] bit. If a peripheral interrupt trigger occurs at the same time as the latched flag is being cleared, the peripheral interrupt trigger has priority and the PERINTFLG will remain set.

Figure 3-4 shows a diagram of the trigger select circuit. See the DMACHSRCSELx register description for the complete list of peripheral interrupt trigger sources.

Figure 3-4. Peripheral Interrupt Trigger Input Diagram



A See [Figure 3-3](#).

Table 3-1 shows the interrupt trigger source options that are available for each channel.

Table 3-1. Peripheral Interrupt Trigger Source Options

Select Value (8-bit)	DMA ChTrigger Source
0	No Peripheral
1	ADCA.1
2	ADCA.2
3	ADCA.3
4	ADCA.4
5	ADCAEVT
6	ADCB.1
7	ADCB.2
8	ADCB.3
9	ADCB.4
10	ADCBEVT
11	ADCC.1
12	ADCC.2
13	ADCC.3
14	ADCC.4
15	ADCCEVT
16	ADCD.1
17	ADCD.2
18	ADCD.3
19	ADCD.4
20	ADCDEVT
21	No Peripheral
22	No Peripheral
23	No Peripheral
24	No Peripheral
25	No Peripheral
26	No Peripheral
27	No Peripheral
28	No Peripheral
29	XINT1
30	XINT2
31	XINT3
32	XINT4
33	XINT5
34	No Peripheral
35	No Peripheral
36	EPWM1.SOCA
37	EPWM1.SOCB
38	EPWM2.SOCA
39	EPWM2.SOCB
40	EPWM3.SOCA
41	EPWM3.SOCB
42	EPWM4.SOCA
43	EPWM4.SOCB
44	EPWM5.SOCA
45	EPWM5.SOCB
46	EPWM6.SOCA
47	EPWM6.SOCB

Table 3-1. Peripheral Interrupt Trigger Source Options (continued)

Select Value (8-bit)	DMA ChTrigger Source
48	EPWM7.SOCA
49	EPWM7.SOCB
50	EPWM8.SOCA
51	EPWM8.SOCB
52	EPWM9.SOCA
53	EPWM9.SOCB
54	EPWM10.SOCA
55	EPWM10.SOCB
56	EPWM11.SOCA
57	EPWM11.SOCB
58	EPWM12.SOCA
59	EPWM12.SOCB
60	No Peripheral
61	No Peripheral
62	No Peripheral
63	No Peripheral
64	No Peripheral
65	No Peripheral
66	No Peripheral
67	No Peripheral
68	TINT0
69	TINT1
70	TINT2
71	MXEVTA
72	MREVTA
73	MXEVTB
74	MREVTB
75	No Peripheral
76	No Peripheral
77	No Peripheral
78	No Peripheral
79	No Peripheral
80	No Peripheral
81	No Peripheral
82	No Peripheral
83	No Peripheral
84	No Peripheral
85	No Peripheral
86	No Peripheral
87	No Peripheral
88	No Peripheral
89	No Peripheral
90	No Peripheral
91	No Peripheral
92	No Peripheral
93	No Peripheral

Table 3-1. Peripheral Interrupt Trigger Source Options (continued)

Select Value (8-bit)	DMA ChTrigger Source
94	No Peripheral
95	SD1FLT1
96	SD1FLT2
97	SD1FLT3
98	SD1FLT4
99	SD2FLT1
100	SD2FLT2
101	SD2FLT3
102	SD2FLT4
103	No Peripheral
104	No Peripheral
105	No Peripheral
106	No Peripheral
107	No Peripheral
108	No Peripheral
109	SPITXDMAA
110	SPIRXDMAA
111	SPITXDMAB
112	SPIRXDMAB
113	SPITXDMAC
114	SPIRXDMAC
115	No Peripheral
116	No Peripheral
117	No Peripheral
118	No Peripheral
119	No Peripheral
120	No Peripheral
121	No Peripheral
122	No Peripheral
123	No Peripheral
124	No Peripheral
125	No Peripheral
126	No Peripheral
127	No Peripheral
128	No Peripheral
129	No Peripheral
130	No Peripheral
131	USBA_EPx_RX1
132	USBA_EPx_TX1
133	USBA_EPx_RX2
134	USBA_EPx_TX2
135	USBA_EPx_RX3
136	USBA_EPx_TX3
137:255	No Peripheral

3.2.4 DMA Bus

The DMA bus architecture consists of a 22-bit address bus, a 32-bit data read bus, and a 32-bit data write bus. Memories and register locations connected to the DMA bus are via interfaces that sometimes share resources with the CPU memory or peripheral bus. Arbitration rules are defined in [Section 3.4](#).

3.3 Pipeline Timing and Throughput

The DMA consists of a 4-stage pipeline as shown in [Figure 3-5](#). The one exception to this is when a DMA channel is configured to have the McBSP as its data source. A read of a McBSP DRR register stalls the DMA bus for one cycle during the read portion of the transfer, as shown in [Figure 3-6](#).

Figure 3-5. 4-Stage Pipeline DMA Transfer

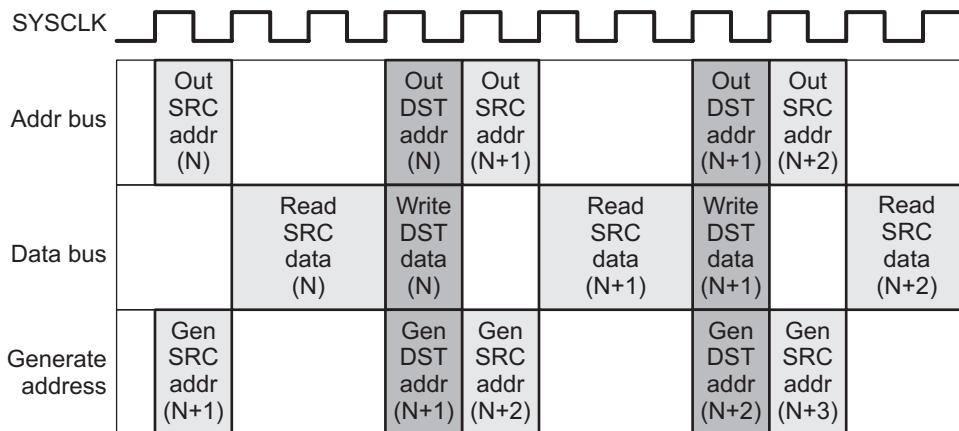
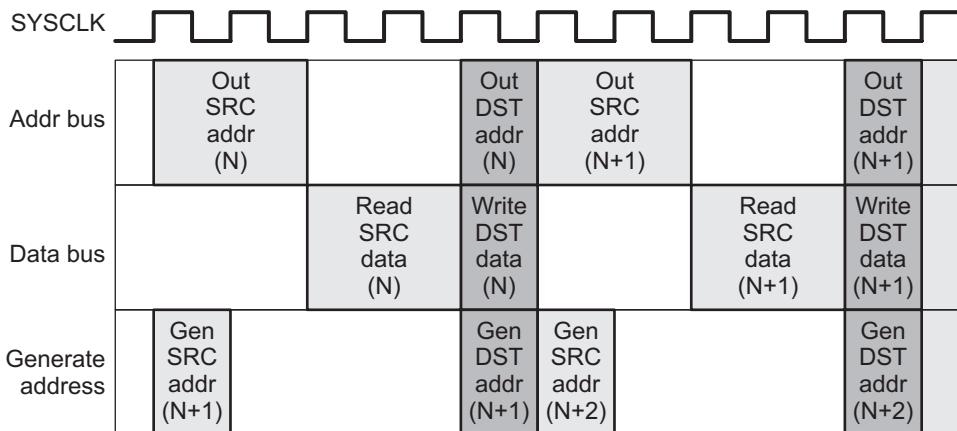


Figure 3-6. 4-Stage Pipeline With One Read Stall (McBSP as source)



In addition to the pipeline there are a few other behaviors of the DMA that affect its total throughput:

- A 1-cycle delay is added at the beginning of each burst
- A 1-cycle delay is added when returning from a CH1 high priority interrupt
- Collisions with the CPU may add delay slots (see [Section 3.4](#))
- 32-bit transfers run at double the speed of a 16-bit transfer (it takes the same amount of time to transfer a 32-bit word as it does a 16-bit word)

For example, to transfer 128 16-bit words from GS0 RAM to GS15 RAM, a channel can be configured to transfer 8 bursts of 16 words/burst. This will give:

$$8 \text{ bursts} * [(4 \text{ cycles/word} * 16 \text{ words/burst}) + 1] = 520 \text{ cycles}$$

If instead the channel were configured to transfer the same amount of data 32 bits at a time (the word size is configured to 32 bits) the transfer would take:

$$8 \text{ bursts} * [(4 \text{ cycles/word} * 8 \text{ words/burst}) + 1] = 264 \text{ cycles}$$

3.4 CPU Arbitration

Typically, DMA activity is independent of the CPU activity. When the DMA and the CPU access a peripheral register within the same peripheral frame concurrently, an arbitration procedure will occur. Any combined accesses between the different interfaces, or where the CPU access is outside of the interface that the DMA is accessing, do not create a conflict.

Conflict Example: the CPU is accessing SPI FIFO while the DMA is simultaneously accessing McBSP, it will create a conflict because both SPI and McBSP reside in a common interface (peripheral frame 2).

Non-conflict Example: the CPU is accessing shared ePWM while the DMA is accessing message McBSP, there will be no conflict, since these two peripherals are located in different interfaces (peripheral frame 1 and peripheral frame 2).

The interfaces which internally contain conflicts are:

- Peripheral frame 1 (Sigma Delta and ePWM / HRPWM)
- Peripheral frame 2 (McBSP, SPI, and uPP)

If the CPU and the DMA make an access to the same peripheral frame in the same cycle, the DMA has priority and the CPU is stalled.

NOTE: If the CPU is performing a read-modify-write operation and the DMA performs a write to the same location, the DMA write may be lost if the operation occurs in between the CPU read and the CPU write. For this reason, it is advised not to mix such CPU accesses with DMA accesses to the same locations.

3.5 Channel Priority

Two priority schemes exist when determining channel priority: Round-robin mode and Channel 1 high-priority mode.

3.5.1 Round-Robin Mode

In this mode, all channels have *equal* priority and each enabled channel is serviced in round-robin fashion as follows:

$$\text{CH1} \rightarrow \text{CH2} \rightarrow \text{CH3} \rightarrow \text{CH4} \rightarrow \text{CH5} \rightarrow \text{CH6} \rightarrow \text{CH1} \rightarrow \text{CH2} \rightarrow \dots$$

In the case above, after each channel has transferred a burst of words, the next channel is serviced. You can specify the size of the burst for each channel. Once CH6 (or the last enabled channel) has been serviced, and no other channels are pending, the round-robin state machine enters an idle state.

From the idle state, channel 1 (if enabled) is always serviced first. However, if the DMA is currently processing another channel x, all other pending channels between x and the end of the round are serviced before CH1. It is in this sense that all the channels are of *equal* priority. For instance, take an example where CH1, CH4, and CH5 are enabled in round-robin mode and CH4 is currently being processed. Then CH1 and CH5 both receive an interrupt trigger from their respective peripherals before CH4 completes. CH1 and CH5 are now both pending. When CH4 completes its burst, CH5 will be serviced next. Only after CH5 completes will CH1 be serviced. Upon completion of CH1, if there are no more channels pending, the round-robin state machine will enter an idle state.

A more complicated example is shown below:

- Assume all channels are enabled, and the DMA is in an idle state,
- Initially a trigger occurs on CH1, CH3, and CH5 on the same cycle,
- When the CH1 burst transfer starts, requests from CH3 and CH5 are pending,
- Before completion of the CH1 burst, the DMA receives a request from CH2. Now the pending requests are from CH2, CH3, and CH5,
- After completing the CH1 burst, CH2 will be serviced since it is next in the round-robin scheme after CH1.
- After the burst from CH2 is finished, the CH3 burst will be serviced, followed by CH5 burst.
- Now while the CH5 burst is being serviced, the DMA receives a request from CH1, CH3, and CH6.
- The burst from CH6 will start after the completion of the CH5 burst since it is the next channel after CH5 in the round-robin scheme.
- This will be followed by the CH1 burst and then the CH3 burst
- After the CH3 burst finishes, assuming no more triggers have occurred, the round-robin state machine will enter an idle state.

The round-robin state machine may be reset to the idle state via the DMACTRL[PRIORITYRESET] bit.

3.5.2 Channel 1 High Priority Mode

In this mode, if a CH1 trigger occurs, the current word transfer on any other channel is completed (not the complete burst), execution is halted, and CH1 is serviced for the complete burst count. When the CH1 burst is complete, execution returns to the channel that was active when the CH1 trigger occurred. All other channels have equal priority and each enabled channel is serviced in round-robin fashion as follows:

Higher Priority: CH1

Lower priority: CH2 → CH3 → CH4 → CH5 → CH6 → CH2 → ...

Given an example where CH1, CH4 and CH5 are enabled in Channel 1 High Priority Mode and CH4 is currently being processed. Then CH1 and CH5 both receive an interrupt trigger from their respective peripherals before CH4 completes. CH1 and CH5 are now both pending. When the current CH4 word transfer is completed, regardless of whether the DMA has completed the entire CH4 burst, CH4 execution will be suspended and CH1 will be serviced. After the CH1 burst completes, CH4 will resume execution.

Upon completion of CH4, CH5 will be serviced. After CH5 completes, if there are no more channels pending, the round-robin state machine will enter an idle state.

Typically Channel 1 would be used in this mode for the ADC, since its data rate is so high. However, Channel 1 High Priority Mode may be used in conjunction with any peripheral.

3.6 Address Pointer and Transfer Control

The DMA state machine is, at its most basic level, two nested loops. The inner loop transfers a burst of data when a peripheral interrupt trigger is received. A burst is the smallest amount of data that can be transferred at one time and its size is defined by the BURST_SIZE register for each channel. The BURST_SIZE register allows a maximum of 32 sixteen-bit words to be transferred in one burst. The outer loop, whose size is set by the TRANSFER_SIZE register for each channel, defines how many bursts are performed in the entire transfer. Since TRANSFER_SIZE is a 16-bit register, the total size of a transfer allowed is well beyond any practical requirement. One CPU interrupt is generated, if enabled, for each transfer. This interrupt can be configured to occur at the beginning or the end of the transfer via the MODE.CHx[CHINTMODE] bit.

In the default setting of the MODE.CHx[ONESHOT] bit, the DMA transfers one burst of data each time a peripheral interrupt trigger is received. After the burst is completed, the state machine moves on to the next pending channel in the priority scheme, even if another trigger for the channel just completed is pending. This feature keeps any single channel from monopolizing the DMA bus. If a transfer of more than the maximum number of words per burst is desired for a single trigger, the MODE.CHx[ONESHOT] bit can be set to complete the entire transfer when triggered. Care is advised when using this mode, since this can create a condition where one trigger uses up the majority of the DMA bandwidth.

Each DMA channel contains a shadowed address pointer for the source and the destination address. These pointers, SRC_ADDR and DST_ADDR, can be independently controlled during the state machine operation. At the beginning of each transfer, the shadowed version of each pointer is copied into its respective active register. During the burst loop, after each word is transferred, the signed value contained in the appropriate source or destination BURST_STEP register is added to the active SRC/DST_ADDR register. During the transfer loop, after each burst is complete, there are two methods that can be used to modify the active address pointer. The first, and default, method is by adding the signed value contained in the SRC/DST_TRANSFER_STEP register to the appropriate pointer. The second is via a process called wrapping, where a wrap address is loaded into the active address pointer. When a wrap procedure occurs, the associated SRC/DST_TRANSFER_STEP register has no effect.

Address wrapping occurs when a number of bursts specified by the appropriate SRC/DST_WRAP_SIZE register completes. Each DMA channel contains two shadowed wrap address pointers, SRC_BEG_ADDR and DST_BEG_ADDR, allowing the source and destination wrapping to be independent of each other. Like the SRC_ADDR and DST_ADDR registers, the active SRC/DST_BEG_ADDR registers are loaded from their shadow counterpart at the beginning of a transfer. When the specified number of bursts has occurred, a two part wrap procedure takes place:

- The appropriate active SRC/DST_BEG_ADDR register is incremented by the signed value contained in the SRC/DST_WRAP_STEP register, then
- The new active SRC/DST_BEG_ADDR register is loaded into the active SRC/DST_ADDR register.

Additionally the wrap counter (SRC/DST_WRAP_COUNT) register is reloaded with the SRC/DST_WRAP_SIZE value to setup the next wrap period. This allows the channel to wrap multiple times within a single transfer. Combined with the first bullet above, this allows the channel to address multiple buffers within a single transfer.

The DMA contains both an active and shadow set of the following address pointers. When a DMA transfer begins, the shadow register set is copied to the active working set of registers. This allows you to program the values of the shadow registers for the next transfer while the DMA works with the active set. It also allows you to implement Ping-Pong buffer schemes without disrupting the DMA channel execution.

Source/Destination Address Pointers (SRC/DST_ADDR)— The value written into the shadow register is the start address of the first location where data is read or written to.

At the beginning of a transfer the shadow register is copied into the active register. The active register performs as the current address pointer.

Source/Destination Begin Address Pointers (SRC/DST_BEG_ADDR)— This is the wrap pointer.

The value written into the shadow register will be loaded into the active register at the start of a transfer. On a wrap condition, the active register will be incremented by the signed value in the appropriate SRC/DST_WRAP_STEP register prior to being loaded into the active SRC/DST_ADDR register.

For each channel, the transfer process can be controlled with the following size values:

Source and Destination Burst Size (BURST_SIZE): — This specifies the number of words to be transferred in a burst.

This value is loaded into the BURST_COUNT register at the beginning of each burst. The BURST_COUNT decrements each word that is transferred and when it reaches a zero value, the burst is complete, indicating that the next channel can be serviced. The behavior of the current channel is defined by the ONE_SHOT bit in the MODE register. The maximum size of the burst is dictated by the type of peripheral. For the ADC, the burst size could be all 16 registers (if all 16 registers are used). For a McBSP peripheral, the burst size is limited to 1 since there is no FIFO and the receive or transmit data register must be loaded or copied every word transferred. For RAM the burst size can be up to the maximum allowed by the BURST_SIZE register, which is 32.

Source and Destination Transfer Size (TRANSFER_SIZE): — This specifies the number of bursts to be transferred before per CPU interrupt (if enabled).

Whether this interrupt is generated at the beginning or the end of the transfer is defined in the CHINTMODE bit in the MODE register. Whether the channel remains enabled or not after the transfer is completed is defined by the CONTINUOUS bit in the MODE register. The TRANSFER_SIZE register is loaded into the TRANSFER_COUNT register at the beginning of each transfer. The TRANSFER_COUNT register keeps track of how many bursts of data the channel has transferred and when it reaches zero, the DMA transfer is complete.

Source/Destination Wrap Size (SRC/DST_WRAP_SIZE): — This specifies the number of bursts to be transferred before the current address pointer wraps around to the beginning.

This feature is used to implement a circular addressing type function. This value is loaded into the appropriate SRC/DST_WRAP_COUNT register at the beginning of each transfer. The SRC/DST_WRAP_COUNT registers keep track of how many bursts of data the channel has transferred and when they reaches zero, the wrap procedure is performed on the appropriate source or destination address pointer. A separate size and count register is allocated for source and destination pointers. To *disable* the wrap function, assign the value of these registers to be larger than the TRANSFER_SIZE.

NOTE: The value written to the SIZE registers is one less than the intended size. So, to transfer three 16-bit words, the value 2 should be placed in the SIZE register.

Regardless of the state of the DATASIZE bit, the value specified in the SIZE registers are for 16-bit addresses. So, to transfer three 32-bit words, the value 5 should be placed in the SIZE register.

For each source/destination pointer, the address changes can be controlled with the following step values:

Source/Destination Burst Step (SRC/DST_BURST_STEP): — Within each burst transfer, the address source and destination step sizes are specified by these registers.

This value is a signed 2's compliment number so that the address pointer can be incremented or decremented as required. If no increment is desired, such as when accessing the McBSP data receive or transmit registers, the value of these registers should be set to zero.

Source/Destination Transfer Step (SRC/DST_TRANSFER_STEP): — This specifies the address offset to start the next burst transfer after completing the current burst transfer.

This is used in cases where registers or data memory locations are spaced at constant intervals. This value is a signed 2's compliment number so that the address pointer can be incremented or decremented as required.

Source/Destination Wrap Step (SRC/DST_WRAP_STEP): — When the wrap counter reaches zero, this value specifies the number of words to add/subtract from the BEG_ADDR pointer and hence sets the new start address.

This implements a circular type of addressing mode, useful in many applications. This value is a signed 2's compliment number so that the address pointer can be incremented or decremented as required.

NOTE: Regardless of the state of the DATASIZE bit, the value specified in the STEP registers are for 16-bit addresses. So, to increment one 32-bit address, a value of 2 should be placed in these registers.

Three modes are provided to control the way the state machine behaves during the burst loop and the transfer loop:

One Shot Mode (ONESHOT): — If one shot mode is enabled when an interrupt event trigger occurs, the DMA will continue transferring data in bursts until TRANSFER_COUNT is zero. If one shot mode is disabled, then an interrupt event trigger is required for each burst transfer and this will continue until TRANSFER_COUNT is zero.

NOTE: When ONESHOT mode is enabled, the DMA will continuously transfer bursts of data on the given channel until the TRANSFER_COUNT value is zero. This could potentially hog the bandwidth of a peripheral and cause long CPU stalls to occur. To avoid this, you could configure a CPU timer (or similar) and disable ONESHOT so as to avoid this situation.

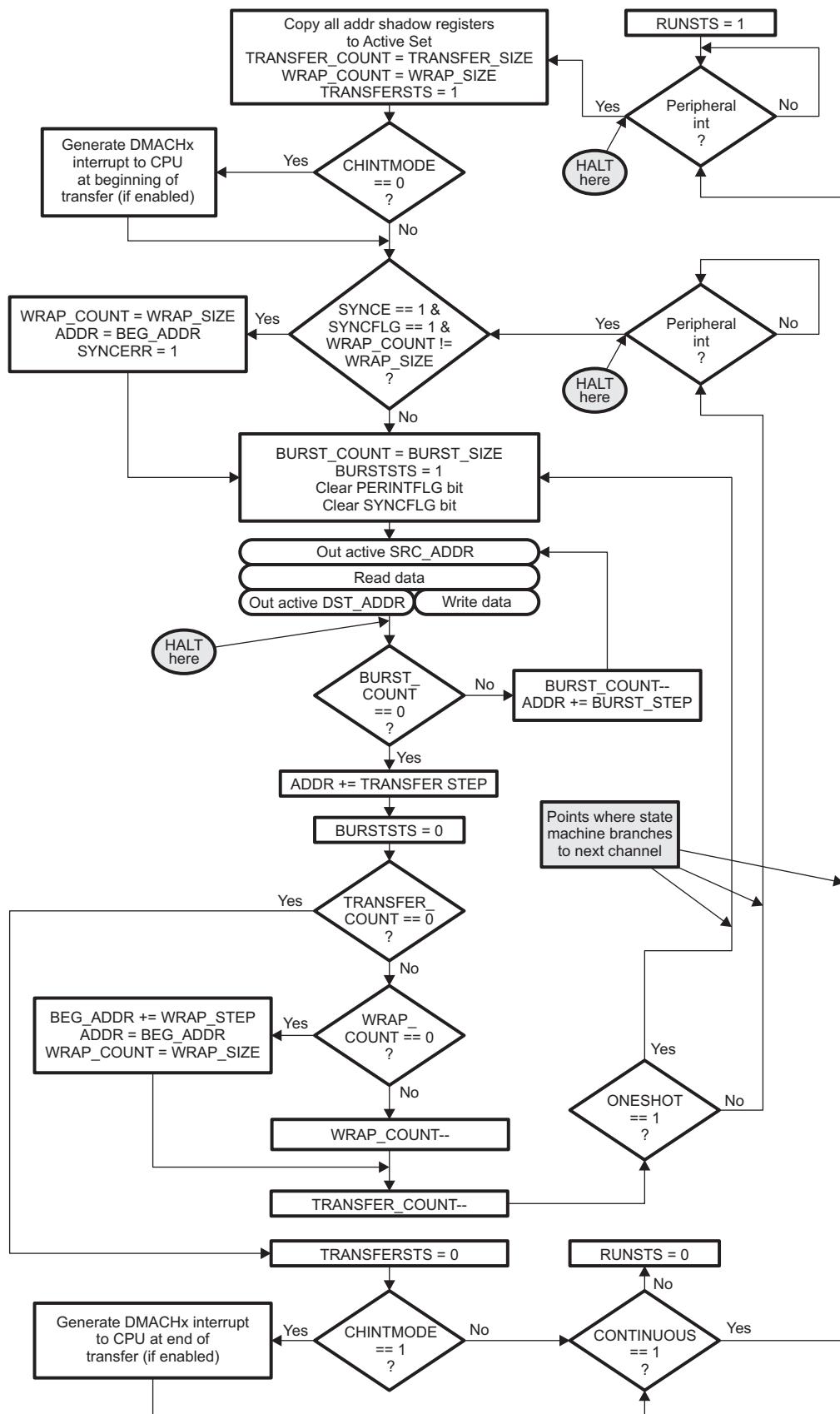
Continuous Mode (CONTINUOUS)— If continuous mode is disabled the RUNSTS bit in the CONTROL register is cleared at the end of the transfer, disabling the DMA channel.

The channel must be re-enabled by setting the RUN bit in the CONTROL register before another transfer can be started on that channel. If the continuous mode is enabled the RUNSTS bit is not cleared at the end of the transfer.

Channel Interrupt Mode (CHINTMODE)— This mode bit selects whether the DMA interrupt from the respective channel is generated at the beginning of a new transfer or at the end of the transfer.

If implementing a ping-pong buffer scheme with continuous mode of operation, then the interrupt would be generated at the beginning, just after the working registers are copied to the shadow set. If the DMA does not operate in continuous mode, then the interrupt is typically generated at the end when the transfer is complete.

All of the above features and modes are shown in [Figure 3-7](#).

Figure 3-7. DMA State Diagram


The following items are in reference to [Figure 3-7](#).

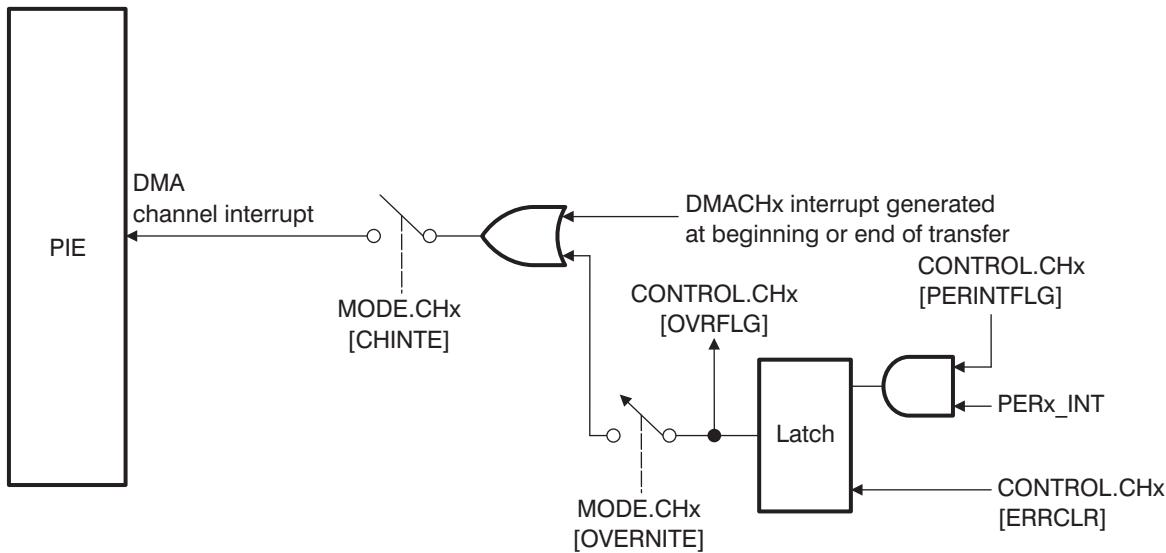
- The *HALT* points represent where the channel halts operation when interrupted by a high priority channel 1 trigger, or when the HALT command is set, or when an emulation halt is issued and the FREE bit is cleared to 0.
- The ADDR registers are not affected by BEG_ADDR at the start of a transfer. BEG_ADDR only affects the ADDR registers on a wrap or sync error. Following is what happens to each of the ADDR registers when a transfer first starts:
 - BEG_ADDR_SHADOW remains unchanged.
 - ADDR_SHADOW remains unchanged.
 - BEG_ADDR = BEG_ADDR_SHADOW
 - ADDR = ADDR_SHADOW
- The active registers get updated when a wrap occurs. The shadow registers remain unchanged. Specifically:
 - BEG_ADDR_SHADOW remains unchanged.
 - ADDR_SHADOW remains unchanged.
 - BEG_ADDR += WRAP_STEP
 - ADDR = BEG_ADDR
- The active registers get updated when a sync error occurs. The shadow registers remain unchanged. Specifically:
 - BEG_ADDR_SHADOW remains unchanged.
 - ADDR_SHADOW remains unchanged.
 - BEG_ADDR remains unchanged.
 - ADDR = BEG_ADDR

Probably the easiest way to remember all this is that:

- The shadow registers never change except by software.
- The active registers never change except by hardware, and a shadow register is only copied into its own active register, never an active register by another name.

3.7 Overrun Detection Feature

The DMA contains overrun detection logic. When a peripheral event trigger is received by the DMA, the PERINTFLG bit in the CONTROL register is set, pending the channel to the DMA state machine. When the burst for that channel is started, the PERINTFLG is cleared. If however, between the time that the PERINTFLG bit is set by an event trigger and cleared by the start of the burst, an additional event trigger arrives, the second trigger will be lost. This condition will set the OVRFLG bit in the CONTROL register as in [Figure 3-8](#). If the overrun interrupt is enabled then the channel interrupt will be generated to the PIE module.

Figure 3-8. Overrun Detection Logic


3.8 Register Descriptions

The complete DMA register set is shown in [Table 3-2](#).

Table 3-2. DMA Register Summary⁽¹⁾

Address	Acronym	Description	Section
DMA Control, Mode and Status Registers			
0x1000	DMACTRL	DMA Control Register	Section 3.8.1
0x1001	DEBUGCTRL	Debug Control Register	Section 3.8.2
0x1002	REVISION	Peripheral Revision Register	Section 3.8.3
0x1003	Reserved	Reserved	
0x1004	PRIORITYCTRL1	Priority Control Register 1	Section 3.8.4
0x1005	Reserved	Reserved	
0x1006	PRIORITYSTAT	Priority Status Register	Table 3-7
0x1007	Reserved	Reserved	
0x101F			
DMA Channel 1 Registers			
0x1020	MODE	Mode Register	Section 3.8.6
0x1021	CONTROL	Control Register	Section 3.8.7
0x1022	BURST_SIZE	Burst Size Register	Section 3.8.8
0x1023	BURST_COUNT	Burst Count Register	Section 3.8.9
0x1024	SRC_BURST_STEP	Source Burst Step Size Register	Section 3.8.10
0x1025	DST_BURST_STEP	Destination Burst Step Size Register	Section 3.8.11
0x1026	TRANSFER_SIZE	Transfer Size Register	Table 3-13
0x1027	TRANSFER_COUNT	Transfer Count Register	Section 3.8.13
0x1028	SRC_TRANSFER_STEP	Source Transfer Step Size Register	Section 3.8.14
0x1029	DST_TRANSFER_STEP	Destination Transfer Step Size Register	Section 3.8.15
0x102A	SRC_WRAP_SIZE	Source Wrap Size Register	Section 3.8.16
0x102B	SRC_WRAP_COUNT	Source Wrap Count Register	Section 3.8.17
0x102C	SRC_WRAP_STEP	Source Wrap Step Size Register	Section 3.8.18
0x102D	DST_WRAP_SIZE	Destination Wrap Size Register	Section 3.8.16
0x102E	DST_WRAP_COUNT	Destination Wrap Count Register	Section 3.8.17
0x102F	DST_WRAP_STEP	Destination Wrap Step Size Register	Section 3.8.18
0x1030	SRC_BEG_ADDR_SHADOW	Shadow Source Begin and Current Address Pointer Registers	Section 3.8.19
0x1032	SRC_ADDR_SHADOW		Section 3.8.19
0x1034	SRC_BEG_ADDR	Active Source Begin and Current Address Pointer Registers	Section 3.8.20
0x1036	SRC_ADDR		Section 3.8.20
0x1038	DST_BEG_ADDR_SHADOW	Shadow Destination Begin and Current Address Pointer Registers	Section 3.8.21
0x103A	DST_ADDR_SHADOW		Section 3.8.21
0x103C	DST_BEG_ADDR	Active Destination Begin and Current Address Pointer Registers	Section 3.8.22
0x103E	DST_ADDR		Section 3.8.22
0x103F	Reserved	Reserved	
DMA Channel 2 Registers			
0x1040	Same as above		
0x105F			
DMA Channel 3 Registers			
0x1060	Same as above		
0x107F			
DMA Channel 4 Registers			

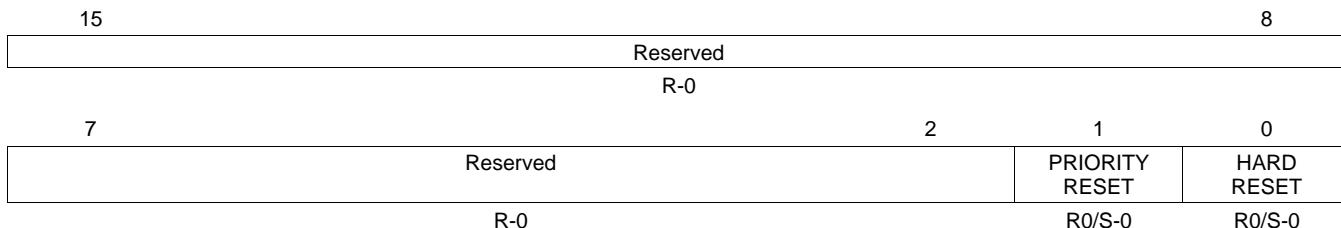
⁽¹⁾ All DMA register writes are EALLOW protected.

Table 3-2. DMA Register Summary⁽¹⁾ (continued)

Address	Acronym	Description	Section
0x1080		Same as above	
0x109F			
DMA Channel 5 Registers			
0x10A0		Same as above	
0x10BF			
DMA Channel 6 Registers			
0x10C0		Same as above	
0x10DF			

3.8.1 DMA Control Register (DMACTRL) — EALLOW Protected

The DMA control register (DMACTRL) is shown in [Figure 3-9](#) and described in [Table 3-3](#).

Figure 3-9. DMA Control Register (DMACTRL)

LEGEND: R0/S = Read 0/Set; R = Read only; -n = value after reset

Table 3-3. DMA Control Register (DMACTRL) Field Descriptions

Bit	Field	Value	Description
15-2	Reserved		Reserved
1	PRIORITYRESET	0	The priority reset bit resets the round-robin state machine when a 1 is written. Service starts from the first enabled channel. Writes of 0 are ignored and this bit always reads back a 0. When a 1 is written to this bit, any pending burst transfer completes before resetting the channel priority machine. If CH1 is configured as a high priority channel, and this bit is written to while CH1 is servicing a burst, the CH1 burst is completed and then any lower priority channel burst is also completed (if CH1 interrupted in the middle of a burst), before the state machine is reset. In case CH1 is high priority, the <i>state machine</i> restarts from CH2 (or the next highest enabled channel).
0	HARDRESET	0	Writing a 1 to the hard reset bit resets the whole DMA and aborts any current access (similar to applying a device reset). Writes of 0 are ignored and this bit always reads back a 0. For a <i>soft</i> reset, a bit is provided for each channel to perform a gentler reset. Refer to the channel control registers. If the DMA was performing an access to the XINTF and the DMA access was stalled (XREADY not responding), then a HARDRESET would abort the access. The XINTF access would only complete if XREADY is released. When writing to this bit, there is a one cycle delay before it takes effect. Hence at least a one cycle delay (i.e., a NOP instruction) after writing to this bit should be introduced before attempting an access to any other DMA register.

3.8.2 Debug Control Register (DEBUGCTRL) — EALLOW Protected

The debug control register (DEBUGCTRL) is shown in [Figure 3-10](#) and described in [Table 3-4](#).

Figure 3-10. Debug Control Register (DEBUGCTRL)

15	14	0
FREE	Reserved	
R/W-0	R-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-4. Debug Control Register (DEBUGCTRL) Field Descriptions

Bit	Field	Value	Description
15	FREE	0	Emulation Control Bit: This bit specifies the action when an emulation halt event occurs. DMA runs until the current DMA read-write access is completed and the current status of a DMA is frozen. See the <i>HALT</i> points in Figure 3-7 for possible halt states.
		1	DMA is unaffected by emulation suspend (run free)
14-0	Reserved		Reserved

3.8.3 Revision Register (REVISION)

The revision register (REVISION) is shown in [Figure 3-11](#) and described in [Table 3-5](#).

Figure 3-11. Revision Register (REVISION)

15	8	7	0
TYPE			REV
R			R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-5. Revision Register (REVISION) Field Descriptions

Bit	Field	Value	Description
15-8	TYPE		DMA Type Bits. A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices which do not affect the basic functionality of the module. These device-specific differences are listed in the <i>TMS320x28xx, 28xxx DSP Peripheral Reference Guide</i> (SPRU566).
		0x0000	This document describes a Type0 DMA.
7-0	REV		DMA Silicon Revision Bits: These bits specify the DMA revision and are changed if any bug fixes are performed.
		0x0000	First release

3.8.4 Priority Control Register 1 (PRIORITYCTRL1) — EALLOW Protected

The priority control register 1 (PRIORITYCTRL1) is shown in [Figure 3-12](#) and described in [Table 3-6](#).

Figure 3-12. Priority Control Register 1 (PRIORITYCTRL1)

15	1	0
Reserved		CH1 PRIORITY
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

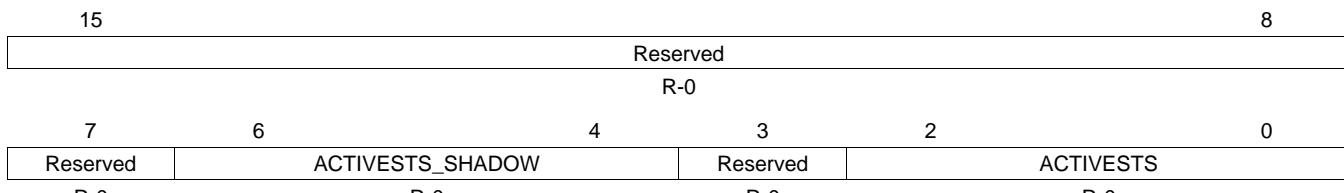
Table 3-6. Priority Control Register 1 (PRIORITYCTRL1) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved		Reserved
0	CH1PRIORITY	0 1	DMA Ch1 Priority: This bit selects whether channel 1 has higher priority or not: Same priority as all other channels Highest priority channel Channel priority can only be changed when all channels are disabled. A priority reset should be performed before restarting channels after changing priority.

3.8.5 Priority Status Register (PRIORITYSTAT)

The priority status register (PRIORITYSTAT) is shown in [Figure 3-13](#) and described in [Table 3-7](#).

Figure 3-13. Priority Status Register (PRIORITYSTAT)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-7. Priority Status Register (PRIORITYSTAT) Field Descriptions

Bit	Field	Value	Description
15-7	Reserved		Reserved
6-4	ACTIVESTS_SHADOW		Active Channel Status Shadow Bits: These bits are only useful when CH1 is enabled as a higher priority channel. When CH1 is serviced, the ACTIVESTS bits are copied to the shadow bits and indicate which channel was interrupted by CH1. When CH1 service is completed, the shadow bits are copied back to the ACTIVESTS bits. If this bit field is zero or the same as the ACTIVESTS bit field, then no channel is pending due to a CH1 interrupt. When CH1 is not a higher priority channel, these bits should be ignored:
	0,0,0	No channel pending	
	0,0,1	CH 1	
	0,1,0	CH 2	
	0,1,1	CH 3	
	1,0,0	CH 4	
	1,0,1	CH 5	
	1,1,0	CH 6	
3	Reserved		Reserved
2-0	ACTIVESTS		Active Channel Status Bits: These bits indicate which channel is currently active or performing a transfer:
	0,0,0	no channel active	
	0,0,1	CH 1	
	0,1,0	CH 2	
	0,1,1	CH 3	
	1,0,0	CH 4	
	1,0,1	CH 5	
	1,1,0	CH 6	

3.8.6 Mode Register (MODE) — EALLOW Protected

The mode register (MODE) is shown in [Figure 3-14](#) and described in [Table 3-8](#).

Figure 3-14. Mode Register (MODE)

15	14	13	12	11	10	9	8
CHINTE	DATASIZE	Reserved		CONTINUOUS	ONESHOT	CHINTMODE	PERINTE
R/W-0	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4				0
OVRINTE	Reserved			PERINTSEL			
R/W-0	R-0			R/W-0			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-8. Mode Register (MODE) Field Descriptions

Bit	Field	Value	Description
15	CHINTE	0 1	Channel Interrupt Enable Bit: This bit enables/disables the respective DMA channel interrupt to the CPU (via the PIE). 0: Interrupt disabled 1: Interrupt enabled
14	DATASIZE	0 1	Data Size Mode Bit: This bit selects if the DMA channel transfers 16-bits or 32-bits of data at a time. 0: 16-bit data transfer size 1: 32-bit data transfer size NOTE: Regardless of the value of this bit all of the registers in the DMA refer to 16-bit words. The only effect this bit causes is whether the databus width is 16 or 32 bits. It is up to you to configure the pointer step increment and size to accommodate 32-bit data transfers. See section Section 3.6 for details.
13-12	Reserved		Reserved
11	CONTINUOUS		Continuous Mode Bit: If this bit is set to 1, then DMA re-initializes when TRANSFER_COUNT is zero and waits for the next interrupt event trigger. If this bit is 0, then the DMA stops and clears the RUNSTS bit to 0.
10	ONESHOT		One Shot Mode Bit: If this bit is set to 1, then subsequent burst transfers occur without additional event triggers after the first event trigger. If this bit is 0 then only one burst transfer is performed per event trigger.
9	CHINTMODE	0 1	Channel Interrupt Generation Mode Bit: This bit specifies when the respective DMA channel interrupt should be generated to the CPU (via the PIE). 0: Generate interrupt at beginning of new transfer 1: Generate interrupt at end of transfer.
8	PERINTE	0 1	Peripheral Interrupt Trigger Enable Bit: This bit enables/disables the selected peripheral interrupt trigger to the DMA. 0: Interrupt trigger disabled. Neither the selected peripheral nor software can start a DMA burst. 1: Interrupt trigger enabled.
7	OVRINTE	0 1	Overflow Interrupt Enable: This bit when set to 1 enables the DMA to generate an interrupt when an overflow event is detected. 0: Overflow interrupt disabled 1: Overflow interrupt enabled An overflow interrupt is generated when the PERINTFLG is set and another interrupt event occurs. The PERINTFLG being set indicates a previous peripheral event is latched and has not been serviced by the DMA.
6-5	Reserved		Reserved

Table 3-8. Mode Register (MODE) Field Descriptions (continued)

Bit	Field	Value	Description
4-0	PERINTSEL		The Peripheral Interrupt Source Select Bits: These bits should be set to the channel number (i.e. CH2.MODE.PERINTSEL[4:0] = 2).

3.8.7 Control Register (CONTROL) — EALLOW Protected

The control register (CONTROL) is shown in [Figure 3-15](#) and described in [Table 3-9](#).

Figure 3-15. Control Register (CONTROL)

15	14	13	12	11	10	9	8
Reserved	OVRFLG	RUNSTS	BURSTSTS	TRANSFERSTS	Reserved	Reserved	PERINTFLG
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
ERRCLR	Reserved	PERINTCLR	PERINTFRC	SOFTRESET	HALT	RUN	
R0/S-0	R-0	R0/S-0	R0/S-0	R0/S-0	R0/S-0	R0/S-0	R0/S-0

LEGEND: R0/S = Read 0/Set; R = Read only; -n = value after reset

Table 3-9. Control Register (CONTROL) Field Descriptions

Bit	Field	Value	Description
15	Reserved		Reserved
14	OVRFLG	0	Overflow Flag Bit: This bit indicates if a peripheral interrupt event trigger is received from the selected peripheral and the PERINTFLG is already set.
			No overflow event
			Overflow event
13	RUNSTS		The ERRCLR bit can be used to clear the state of this bit to 0. The OVRFGL bit is not affected by the PERINTFRC event.
			Run Status Bit: This bit is set to 1 when the RUN bit is written to with a 1. This indicates the DMA channel is now ready to process peripheral interrupt event triggers. This bit is cleared to 0 when TRANSFER_COUNT reaches zero and CONTINUOUS mode bit is set to 0. This bit is also cleared to 0 when either the HARDRESET bit, the SOFTRESET bit, or the HALT bit is activated.
			0 Channel is disabled.
			1 Channel is enabled.
12	BURSTSTS	0	Burst Status Bit: This bit is set to 1 when a DMA burst transfer begins and the BURST_COUNT is initialized with the BURST_SIZE. This bit is cleared to zero when BURST_COUNT reaches zero. This bit is also cleared to 0 when either the HARDRESET or the SOFTRESET bit is activated.
			No burst activity
			1 The DMA is currently servicing or suspending a burst transfer from this channel.
11	TRANSFERSTS	0	Transfer Status Bit: This bit is set to 1 when a DMA transfer begins and the address registers are copied to the shadow set and the TRANSFER_COUNT is initialized with the TRANSFER_SIZE. This bit is cleared to zero when TRANSFER_COUNT reaches zero. This bit is also cleared to 0 when either the HARDRESET or the SOFTRESET bit is activated.
			No transfer activity
			1 The channel is currently in the middle of a transfer regardless of whether a burst of data is actively being transferred or not.
10-9	Reserved		Reserved
8	PERINTFLG	0	Peripheral Interrupt Trigger Flag Bit: This bit indicates if a peripheral interrupt event trigger has occurred. This flag is automatically cleared when the first burst transfer begins.
			No interrupt event trigger
			1 Interrupt event trigger
The PERINTFRC bit can be used to set the state of this bit to 1 and force a software DMA event. The PERINTCLR bit can be used to clear the state of this bit to 0.			
7	ERRCLR	0	Error Clear Bit: Writing a 1 to this bit will clear any latched sync error event and clear the SYNCERR bit. This bit will also clear the OVRFGL bit. This bit would normally be used when initializing the DMA for the first time or if an overflow condition is detected. If an ADCSYNC error event or overflow event occurs at the same time as writing to this bit, the ADC or overrun has priority and the SYNCERR or OVRFGL bit is set.
			Reserved

Table 3-9. Control Register (CONTROL) Field Descriptions (continued)

Bit	Field	Value	Description
4	PERINTCLR	0	Peripheral Interrupt Clear Bit: Writing a 1 to this bit clears any latched peripheral interrupt event and clears the PERINTFLG bit. This bit would normally be used when initializing the DMA for the first time. If a peripheral event occurs at the same time as writing to this bit, the peripheral has priority and the PERINTFLG bit is set.
3	PERINTFRC	0	Peripheral Interrupt Force Bit: Writing a 1 to this bit latches a peripheral interrupt event trigger and sets the PERINTFLG bit. If the PERINTE bit is set, this bit can be used like a software force for a DMA burst transfer.
2	SOFTRESET	0	<p>Channel Soft Reset Bit: Writing a 1 to this bit completes current read-write access and places the channel into a default state as follows:</p> <p>RUNSTS = 0 TRANSFERSTS = 0 BURSTSTS = 0 BURST_COUNT = 0 TRANSFER_COUNT = 0 SRC_WRAP_COUNT = 0 DST_WRAP_COUNT = 0</p> <p>This is a <i>soft</i> reset that basically allows the DMA to complete the current read-write access and then places the DMA channel into the default reset state.</p>
1	HALT	0	Channel Halt Bit: Writing a 1 to this bit halts the DMA at the current state and any current read-write access is completed. See Figure 3-7 for the various positions the state machine can be at when HALTED. The RUNSTS bit is set to 0. To take the device out of HALT, the RUN bit needs to be activated.
0	RUN	0	<p>Channel Run Bit: Writing a 1 to this bit starts the DMA channel. The RUNSTS bit is set to 1. This bit is also used to take the device out of HALT.</p> <p>The RUN bit is typically used to start the DMA running after you have configured the DMA. It will then wait for the first interrupt event (PERINTFLG == 1) to start operation. The RUN bit can also be used to take the DMA channel out of a HALT condition. See Figure 3-7 for the various positions the state machine can be at when HALTED.</p>

3.8.8 Burst Size Register (BURST_SIZE) — EALLOW Protected

The burst size register (BURST_SIZE) is shown in [Figure 3-16](#) and described in [Table 3-10](#).

Figure 3-16. Burst Size Register (BURST_SIZE)

15	5	4	0
Reserved			BURTSIZE
R-0			R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-10. Burst Size Register (BURST_SIZE) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved		Reserved
4-0	BURTSIZE	0 1 ... 31	These bits specify the burst transfer size: Transfer 1 word in a burst Transfer 2 words in a burst ... Transfer 32 words in a burst

3.8.9 BURST_COUNT Register

The burst count register (BURST_COUNT) is shown in [Figure 3-17](#) and described in [Table 3-11](#).

Figure 3-17. Burst Count Register (BURST_COUNT)

15	5	4	0
Reserved			BURSTCOUNT
R-0			R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-11. Burst Count Register (BURST_COUNT) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved		Reserved
4-0	BURSTCOUNT	0 1 2 ... 31	These bits indicate the current burst counter value: 0 word left in a burst 1 word left in a burst 2 words left in a burst ... 31 words left in a burst The above values represent the state of the counter at the HALT conditions.

3.8.10 Source Burst Step Register Size (SRC_BURST_STEP) — EALLOW Protected

The source burst step size register (SRC_BURST_STEP) is shown in [Figure 3-18](#) and described in [Table 3-12](#).

Figure 3-18. Source Burst Step Size Register (SRC_BURST_STEP)

15	SRCBURSTSTEP	0
	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-12. Source Burst Step Size Register (SRC_BURST_STEP) Field Descriptions

Bit	Field	Value	Description																		
15-0	SRCBURSTSTEP		<p>These bits specify the source address post-increment/decrement step size while processing a burst of data:</p> <table> <tr> <td>0x0FFF</td> <td>Add 4095 to address</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0x0002</td> <td>Add 2 to address</td> </tr> <tr> <td>0x0001</td> <td>Add 1 to address</td> </tr> <tr> <td>0x0000</td> <td>No address change</td> </tr> <tr> <td>0xFFFF</td> <td>Sub 1 from address</td> </tr> <tr> <td>0xFFFE</td> <td>Sub 2 from address</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0xF000</td> <td>Sub 4096 from address</td> </tr> </table> <p>Only values from -4096 to 4095 are valid.</p>	0x0FFF	Add 4095 to address	0x0002	Add 2 to address	0x0001	Add 1 to address	0x0000	No address change	0xFFFF	Sub 1 from address	0xFFFE	Sub 2 from address	0xF000	Sub 4096 from address
0x0FFF	Add 4095 to address																				
...	...																				
0x0002	Add 2 to address																				
0x0001	Add 1 to address																				
0x0000	No address change																				
0xFFFF	Sub 1 from address																				
0xFFFE	Sub 2 from address																				
...	...																				
0xF000	Sub 4096 from address																				

3.8.11 Destination Burst Step Register Size (DST_BURST_STEP) — EALLOW Protected

The destination burst step register size (DST_BURST_STEP) is shown in [Figure 3-19](#) and described in [Table 3-13](#).

Figure 3-19. Destination Burst Step Register Size (DST_BURST_STEP)

15	0
DSTBURSTSTEP	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-13. Destination Burst Step Register Size (DST_BURST_STEP) Field Descriptions

Bit	Field	Value	Description
15-0	DSTBURSTSTEP	0x0FFF ... 0x0002 0x0001 0x0000 0xFFFF 0xFFFE ... 0xF000	These bits specify the destination address post-increment/decrement step size while processing a burst of data: Add 4095 to address ... Add 2 to address Add 1 to address No address change Sub 1 from address Sub 2 from address ... Sub 4096 from address Only values from -4096 to 4095 are valid.

3.8.12 Transfer Size Register (TRANSFER_SIZE) — EALLOW Protected

The transfer size register (TRANSFER_SIZE) is shown in [Figure 3-20](#) and described in [Table 3-14](#).

Figure 3-20. Transfer Size Register (TRANSFER_SIZE)

15	0
TRANSFERSIZE	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-14. Transfer Size Register (TRANSFER_SIZE) Field Descriptions

Bit	Field	Value	Description
15-0	TRANSFERSIZE	0x0000 0x0001 0x0002 ... 0xFFFF	These bits specify the number of bursts to transfer: Transfer 1 burst Transfer 2 bursts Transfer 3 bursts ... Transfer 65536 bursts

3.8.13 Transfer Count Register (TRANSFER_COUNT)

The transfer count register (TRANSFER_COUNT) is shown in [Figure 3-21](#) and described in [Table 3-15](#).

Figure 3-21. Transfer Count Register (TRANSFER_COUNT)

15	TRANSFERCOUNT	0
R/W-0		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-15. Transfer Count Register (TRANSFER_COUNT) Field Descriptions

Bit	Field	Value	Description
15-0	TRANSFERCOUNT	0x0000 0x0001 0x0002 ... 0xFFFF	These bits specify the current transfer counter value: 0 bursts left to transfer 1 burst left to transfer 2 bursts left to transfer ... 65535 bursts left to transfer The above values represent the state of the counter at the HALT conditions.

3.8.14 Source Transfer Step Size Register (SRC_TRANSFER_STEP) — EALLOW Protected

The source transfer step size register (SRC_TRANSFER_STEP) is shown in [Figure 3-22](#) and described in [Table 3-16](#).

Figure 3-22. Source Transfer Step Size Register (SRC_TRANSFER_STEP)

15	SRCTRANSFERSTEP	0
R/W-0		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-16. Source Transfer Step Size Register (SRC_TRANSFER_STEP) Field Descriptions

Bit	Field	Value	Description
15-0	SRCTRANSFERSTEP	0x0FFF ... 0x0002 0x0001 0x0000 0xFFFF 0xFFFE ... 0xF000	These bits specify the source address pointer post-increment/decrement step size after processing a burst of data: Add 4095 to address ... Add 2 to address Add 1 to address No address change Sub 1 from address Sub 2 from address ... Sub 4096 from address Only values from -4096 to 4095 are valid.

3.8.15 Destination Transfer Step Size Register (DST_TRANSFER_STEP) — EALLOW Protected

The destination transfer step size register (DST_TRANSFER_STEP) is shown in [Figure 3-23](#) and described in [Table 3-17](#).

Figure 3-23. Destination Transfer Step Size Register (DST_TRANSFER_STEP)

15	0
DSTTRANSFERSTEP	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-17. Destination Transfer Step Size Register (DST_TRANSFER_STEP) Field Descriptions

Bit	Field	Value	Description
15-0	DSTTRANSFERSTEP	0x0FFF ... 0x0002 0x0001 0x0000 0xFFFF 0xFFFE ... 0xF000	These bits specify the destination address pointer post-increment/decrement step size after processing a burst of data: Add 4095 to address ... Add 2 to address Add 1 to address No address change Sub 1 from address Sub 2 from address ... Sub 4096 from address Only values from -4096 to 4095 are valid.

3.8.16 Source/Destination Wrap Size Register (SRC/DST_WRAP_SIZE) — EALLOW protected)

The source/destination wrap size register is shown in [Figure 3-24](#) and described in [Table 3-18](#).

Figure 3-24. Source/Destination Wrap Size Register (SRC/DST_WRAP_SIZE)

15	0
WRAPSIZE	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-18. Source/Destination Wrap Size Register (SRC/DST_WRAP_SIZE) Field Descriptions

Bit	Field	Value	Description
15-0	WRAPSIZE	0x0000 0x0001 0x0002 ... 0xFFFF	These bits specify the number of bursts to transfer before wrapping back to begin address pointer: Wrap after 1 burst Wrap after 2 bursts Wrap after 3 bursts ... Wrap after 65536 bursts To disable the wrap function, set the WRAPSIZE bit field to a number larger than the TRANSFERSIZE bit field.

3.8.17 Source/Destination Wrap Count Register (SCR/DST_WRAP_COUNT)

The source/destination wrap count register (SCR/DST_WRAP_COUNT) is shown in [Figure 3-25](#) and described in [Table 3-19](#).

Figure 3-25. Source/Destination Wrap Count Register (SCR/DST_WRAP_COUNT)

15	WRAPCOUNT	0
	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-19. Source/Destination Wrap Count Register (SCR/DST_WRAP_COUNT) Field Descriptions

Bit	Field	Value	Description
15-0	WRAPCOUNT	0x0000 0x0001 0x0002 ... 0xFFFF	These bits indicate the current wrap counter value: Wrap complete 1 burst left 2 burst left ... 65535 burst left The above values represent the state of the counter at the HALT conditions.

3.8.18 Source/Destination Wrap Step Size Registers (SRC/DST_WRAP_STEP) — EALLOW Protected

The source/destination wrap step size register (SRC/DST_WRAP_STEP) are shown in [Figure 3-26](#) and described in [Table 3-20](#).

Figure 3-26. Source/Destination Wrap Step Size Registers (SRC/DST_WRAP_STEP)

15	WRAPSTEP	0
	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-20. Source/Destination Wrap Step Size Registers (SRC/DST_WRAP_STEP) Field Descriptions

Bit	Field	Value	Description
15-0	WRAPSTEP	0x0FFF ... 0x0002 0x0001 0x0000 0xFFFF 0xFFFFE ... 0xF000	These bits specify the source begin address pointer post-increment/decrement step size after wrap counter expires: Add 4095 to address ... Add 2 to address Add 1 to address No address change Sub 1 from address Sub 2 from address ... Sub 4096 from address Only values from -4096 to 4095 are valid.

3.8.19 Shadow Source Begin and Current Address Pointer Registers (SRC_BEG_ADDR_SHADOW/DST_BEG_ADDR_SHADOW) — All EALLOW Protected

The shadow source begin and current address pointer registers (SRC_BEG_ADDR_SHADOW/DST_BEG_ADDR_SHADOW) are shown in [Figure 3-27](#) and described in [Table 3-21](#).

**Figure 3-27. Shadow Source Begin and Current Address Pointer Registers
(SRC_BEG_ADDR_SHADOW/DST_BEG_ADDR_SHADOW)**

31	22	21	0
Reserved		BEGADDR	
R-0			R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 3-21. Shadow Source Begin and Current Address Pointer Registers
(SRC_BEG_ADDR_SHADOW/DST_BEG_ADDR_SHADOW) Field Descriptions**

Bit	Field	Value	Description
31-22	Reserved		Reserved
21-0	BEGADDR		22-bit address value

3.8.20 Active Source Begin and Current Address Pointer Registers (SRC_BEG_ADDR/DST_BEG_ADDR)

The active source begin and current address pointer registers (SRC_BEG_ADDR/DST_BEG_ADDR) are shown in [Figure 3-28](#) and described in [Table 3-22](#).

**Figure 3-28. Active Source Begin and Current Address Pointer Registers
(SRC_BEG_ADDR/DST_BEG_ADDR)**

31	22	21	0
Reserved		BEGADDR	
R-0			R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 3-22. Active Source Begin and Current Address Pointer Registers
(SRC_BEG_ADDR/DST_BEG_ADDR) Field Descriptions**

Bit	Field	Value	Description
31-22	Reserved		Reserved
21-0	BEGADDR		22-bit address value

3.8.21 Shadow Destination Begin and Current Address Pointer Registers (SRC_ADDR_SHADOW/DST_ADDR_SHADOW) — All EALLOW Protected

The shadow destination begin and current address pointer registers (SRC_ADDR_SHADOW/DST_ADDR_SHADOW) are shown in [Figure 3-29](#) and described in [Table 3-23](#).

**Figure 3-29. Shadow Destination Begin and Current Address Pointer Registers
(SRC_ADDR_SHADOW/DST_ADDR_SHADOW)**

31	22	21	0
Reserved		ADDR	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 3-23. Shadow Destination Begin and Current Address Pointer Registers
(SRC_ADDR_SHADOW/DST_ADDR_SHADOW) Field Descriptions**

Bit	Field	Value	Description
31-22	Reserved		Reserved
21-0	ADDR		22-bit address value

3.8.22 Active Destination Begin and Current Address Pointer Registers (SRC_ADDR/DST_ADDR)

The active destination begin and current address pointer registers (SRC_ADDR/DST_ADDR) are shown in [Figure 3-30](#) and described in [Table 3-24](#).

**Figure 3-30. Active Destination Begin and Current Address Pointer Registers
(SRC_ADDR/DST_ADDR)**

31	22	21	0
Reserved		ADDR	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 3-24. Active Destination Begin and Current Address Pointer Registers
(SRC_ADDR/DST_ADDR) Field Descriptions**

Bit	Field	Value	Description
31-22	Reserved		Reserved
21-0	ADDR		22-bit address value

Control Law Accelerator (CLA)

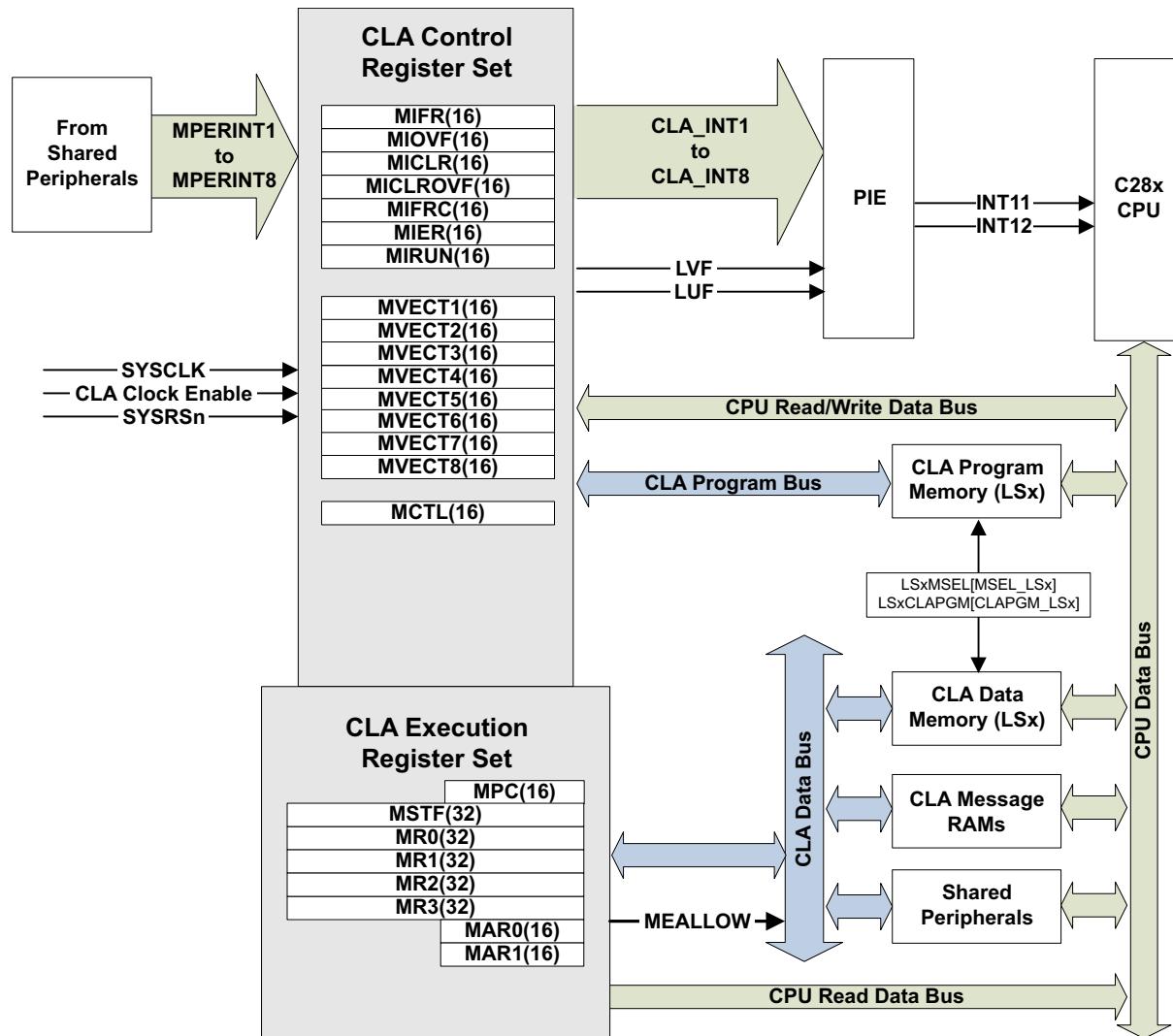
The control law accelerator (CLA) Type-1 is an independent, fully-programmable, 32-bit floating-point math processor that brings concurrent control-loop execution to the C28x family. The low interrupt-latency of the CLA allows it to read ADC samples "just-in-time." This significantly reduces the ADC sample to output delay to enable faster system response and higher MHz control loops. By using the CLA to service time-critical control loops, the main CPU is free to perform other system tasks such as communications and diagnostics. This chapter provides an overview of the architectural structure and components of the control law accelerator.

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4.1 Control Law Accelerator (CLA) Overview

The control law accelerator extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Utilizing the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurrently. The following is a list of major features of the CLA.

- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
 - Complete bus architecture:
 - Program address bus and program data bus
 - Data address bus, data read bus and data write bus
 - Independent eight stage pipeline.
 - 16-bit program counter (MPC)
 - Four 32-bit result registers (MR0-MR3)
 - Two 16-bit auxiliary registers (MAR0, MAR1)
 - Status register (MSTF)
- Instruction set includes:
 - IEEE single-precision (32-bit) floating point math operations
 - Floating-point math with parallel load or store
 - Floating-point multiply with parallel add or subtract
 - 1/X and 1/sqrt(X) estimations
 - Data type conversions.
 - Conditional branch and call
 - Data load/store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines.
 - The start address of each task is specified by the MVECT registers.
 - No limit on task size as long as the tasks fit within the configurable CLA program memory space.
 - One task is serviced at a time through to completion. There is no nesting of tasks.
 - Upon task completion a task-specific interrupt is flagged within the PIE.
 - When a task finishes the next highest-priority pending task is automatically started.
- Task trigger mechanisms:
 - C28x CPU via the IACK instruction
 - Task1 to Task8: up to 256 possible trigger sources from peripherals connected to the shared bus on which the CLA assumes secondary ownership.
- Memory and Shared Peripherals:
 - Two dedicated message RAMs for communication between the CLA and the main CPU.
 - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.
 - The CLA, on reset, is the secondary master for all peripherals which can have either the CLA or DMA as their secondary master.

Figure 4-1. CLA Block Diagram


4.2 CLA Interface

This chapter describes how the C28x main CPU can interface to the CLA and vice versa.

4.2.1 CLA Memory

The CLA can access three types of memory: program, data and message RAMs. The behavior and arbitration for each type of memory is described in detail below.

- **CLA Program Memory**

The CLA program can be loaded to any of the local shared memories (LSxRAM) on the core that it is tied to. At reset, all memory blocks are mapped to the master CPU. While mapped to the CPU space, the CPU can copy the CLA program code into the memory block(s). During debug, the block(s) can also be loaded directly by Code Composer Studio™.

Once the memory is initialized with CLA code, the master CPU maps it to the CLA program space by:

1. Assigning ownership of the memory block to the CLA by writing a 1 to the memory block's MemCfgRegs.LSxMSEL[MSEL_LSx] bit.
2. Specifying the memory block as a code block for the CLA by writing a 1 to the MemCfgRegs.LSxCLAPGM[CLAPGM_LSx] bit.

When an LSx memory is configured as CLA program memory, only debug accesses are allowed on cycles that the CLA is not fetching a new instruction. A detailed explanation of the memory configurations and access arbitration (CPU/CLA/DEBUG) process can be found in the *Memory Controller* chapter of this manual.

All CLA program fetches are performed as 32-bit read operations and all opcodes must be aligned to an even address. Since all CLA opcodes are 32-bits, this alignment naturally occurs.

- **CLA Data Memory**

Any of the device's LSxRAMs can serve as data memory blocks to the CLA. At reset, all blocks are mapped to the master CPU memory space, whereby the master can initialize the memory with data tables, coefficients, and so on, for the CLA to use.

Once the memory is initialized with CLA data, the master CPU maps it to the CLA data space by :

1. Assigning ownership of the memory block to the CLA by writing a 1 to the memory block's MemCfgRegs.LSxMSEL[MSEL_LSx] bit.
2. Specifying the memory block as a data block for the CLA by writing a 0 to the MemCfgRegs.LSxCLAPGM[CLAPGM_LSx] bit. The value of this bit at reset is 0.

When an LSx memory is configured as a CLA data memory, the CLA read/write access are arbitrated along with CPU accesses. The user has the option of turning on CPU fetch or write protection to the memory by writing to the appropriate bits of the MemCfgRegs.LSxACCPROT_x registers. A detailed explanation of the memory configurations and access arbitration (CPU/CLA/DEBUG) process can be found in the *Memory Controller* chapter of this manual.

The CLA RAMs and registers are protected by the security module. Refer to the *DCSM* chapter of this manual for more details on the security scheme.

- **CLA Shared Message RAMs**

There are two small memory blocks for data sharing and communication between the CLA and the master CPU on each CPU subsystem. The message RAMs are always mapped to both CPU and CLA memory spaces and are protected by the DCSM. The message RAMs allow data accesses only; no program fetches can be performed.

- **CLA to CPU Message RAM**

The CLA can use this block to pass data to the master CPU. This block is both readable and writable by the CLA. This block is also readable by the master CPU but writes by the master CPU are ignored.

- **CPU to CLA Message RAM**

The master CPU can use this block to pass data and messages to the CLA. This message RAM is both readable and writable by the master CPU. The CLA can perform reads but writes by the CLA are ignored.

4.2.2 CLA Memory Bus

The CLA has dedicated bus architecture similar to that of the C28x CPU where there is a program read, data read, and data write bus. Thus, there can be simultaneous instruction fetch, data read, and data write in a single cycle. Like the C28x CPU, the CLA expects memory logic to align any 32-bit read or write to an even address. If the address-generation logic generates an odd address, the CLA will begin reading or writing at the previous even address. This alignment does not affect the address values generated by the address-generation logic.

- **CLA Program Bus**

The CLA program bus has a access range of 32K 32-bit instructions. Since all CLA instructions are 32 bits, this bus always fetches 32 bits at a time and the opcodes must be even-word aligned. The amount of program space available for the CLA is limited to the number of available LSxRAM blocks. This number is device-dependent and will be described in the device-specific data manual.

- **CLA Data Read Bus**

The CLA data read bus has a 64K x 16 address range. The bus can perform 16 or 32-bit reads and will automatically stall if there are memory access conflicts. The data read bus has access to both the message RAMs, CLA data memory, and the shared peripherals.

- **CLA Data Write Bus**

The CLA data write bus has a 64K x 16 address range. This bus can perform 16 or 32-bit writes. The bus will automatically stall if there are memory access conflicts. The data write bus has access to the CLA to CPU message RAM, CLA data memory, and the shared peripherals.

4.2.3 Shared Peripherals and EALLOW Protection

For a given CPU subsystem, the CLA and DMA share secondary access to some peripherals. The secondary ownership of the bus is determined by the CpuSysRegs.SECMSEL[VBUS32_X] bit. If it is set to 0, the CLA is the secondary owner. If it is set to 1, the DMA is the secondary owner. By default, at reset, the CLA is given the secondary ownership of the bus and, therefore, can access all the peripherals connected to it.

Note: The CLA read access time to the bus is 2-wait states while write access is 0-wait.

Refer to the device datasheet for the list of peripherals connected to the bus.

Several peripheral control registers are protected from spurious 28x CPU writes by the EALLOW protection mechanism. These same registers are also protected from spurious CLA writes. The EALLOW bit in the main CPU status register 1 (ST1) indicates the state of protection for the main CPU. Likewise the MEALLOW bit in the CLA status register (MSTF) indicates the state of write protection for the CLA. The MEALLOW CLA instruction enables write access by the CLA to EALLOW protected registers. Likewise the MEDIS CLA instruction will disable write access. This way the CLA can enable/disable write access independent of the main CPU.

The ADC offers the option to generate an early interrupt pulse at the start of a sample conversion. If this option is used to start an ADC-triggered CLA task, then the 8th instruction can read the result as soon as the conversion completes. The CLA pipeline activity for this scenario is shown in [Section 4.4](#).

4.2.4 CLA Tasks and Interrupt Vectors

The CLA program code is divided up into tasks or interrupt service routines. Tasks do not have a fixed starting location or length. The CLA program memory can be divided up as desired. The CLA knows where a task begins by the content of the associated interrupt vector (MVECT1 to MVECT8) and the end is indicated by the MSTOP instruction.

The CLA supports eight tasks. Task 1 has the highest priority and task 8 has the lowest priority. A task can be requested by a peripheral interrupt or by software:

- **Peripheral interrupt trigger**

Each task can be triggered by up to 256 interrupt sources. The trigger for each task is defined by writing an appropriate value to the DmaClaSrcSelRegs.CLA1TASKSRCSELx[TASKx] bit field. Each of the possible 256 values specifies an interrupt source from a specific peripheral on the shared bus. The configuration options are listed in [Table 4-1](#).

Table 4-1. Configuration Options

Select Value (8-bit)	CLA Trigger Source
0	No Peripheral
1	ADCAINT1
2	ADCAINT2
3	ADCAINT3
4	ADCAINT4
5	ADCAEVT
6	ADCBINT1
7	ADCBINT2
8	ADCBINT3
9	ADCBINT4
10	ADCBEVT
11	ADCCINT1
12	ADCCINT2
13	ADCCINT3
14	ADCCINT4
15	ADCCEVT
16	ADCDINT1
17	ADCDINT2
18	ADCDINT3
19	ADCDINT4
20	ADCDEVT
28:21	Reserved
29	XINT1
30	XINT2
31	XINT3
32	XINT4
33	XINT5
34	Reserved
35	Reserved
36	EPWM1INT
37	EPWM2INT
38	EPWM3INT
39	EPWM4INT
40	EPWM5INT
41	EPWM6INT

Table 4-1. Configuration Options (continued)

Select Value (8-bit)	CLA Trigger Source
42	EPWM7INT
43	EPWM8INT
44	EPWM9INT
45	EPWM10INT
46	EPWM11INT
47	EPWM12INT
67:48	Reserved
68	TINT0
69	TINT1
70	TINT2
71	MXEVTAA
72	MREVTA
73	MXEVTB
74	MREVTB
75	ECAP1INT
76	ECAP2INT
77	ECAP3INT
78	ECAP4INT
79	ECAP5INT
80	ECAP6INT
81	Reserved
82	Reserved
83	EQEP1INT
84	EQEP2INT
85	EQEP3INT
86	Reserved
87	HRCAP1INT
88	HRCAP2INT
94:89	Reserved
95	SD1INT
96	SD2INT
106:97	Reserved
107	UPP1INT
108	Reserved
109	SPITXINTA
110	SPIRXINTA
111	SPITXINTB
112	SPIRXINTB
113	SPITXINTC
114	SPIRXINTC
255:115	Reserved

For example, task 1 (MVECT1) can be set to trigger on EPWMINT1 by writing 36 to DmaClaSrcSelRegs.CLA1TASKSRCSEL1.bit.TASK1. To disable the triggering of a task by a peripheral, the user must set the DmaClaSrcSelRegs.CLA1TASKSRCSELx[TASKx] bit field to 0. It should be noted that a CLA task only triggers on a level transition (an edge) of the configured interrupt source.

- **Software Trigger**

Tasks can also be started by the main CPU software writing to the MIFRC register or by the IACK instruction. Using the IACK instruction is more efficient because it does not require you to issue an EALLOW to set MIFR bits. Set the MCTL[IACKE] bit to enable the IACK feature. Each bit in the operand of the IACK instruction corresponds to a task. For example IACK #0x0001 will set bit 0 in the MIFR register to start task 1. Likewise IACK #0x0003 will set bits 0 and 1 in the MIFR register to start task 1 and task 2.

The CLA has its own fetch mechanism and can run and execute a task independent of the main CPU. Only one task is serviced at a time; there is no nesting of tasks. The task currently running is indicated in the MIRUN register. Interrupts that have been received but not yet serviced are indicated in the flag register (MIFR). If an interrupt request from a peripheral is received and that same task is already flagged, then the overflow flag bit is set. Overflow flags will remain set until they are cleared by the main CPU.

If the CLA is idle (no task is currently running) then the highest priority interrupt request that is both flagged (MIFR) and enabled (MIER) will start. The flow is as follows:

1. The associated RUN register bit is set (MIRUN) and the flag bit (MIFR) is cleared.
2. The CLA begins execution at the location indicated by the associated interrupt vector (MVECT_x). MVECT contains the absolute 16-bit address of the task in the lower 64K memory space.
3. The CLA executes instructions until the MSTOP instruction is found. This indicates the end of the task.
4. The MIRUN bit is cleared.
5. The task-specific interrupt to the PIE is issued. This informs the main CPU that the task has completed.
6. The CLA returns to idle.

Once a task completes the next highest-priority pending task is automatically serviced and this sequence repeats.

4.3 CLA Configuration and Debug

This section discusses the steps necessary to configure and debug the CLA.

4.3.1 Building a CLA Application

The control law accelerator can be programmed in either CLA assembly code using the instructions described in [Section 4.5](#) or a reduced subset of the C language. CLA assembly code resides in the same project with C28x code. The only restriction is the CLA code must be in its own assembly section. This can be easily done using the .sect assembly directive. This does not prevent CLA and C28x code from being linked into the same memory region in the linker command file.

System and CLA initialization are performed by the main CPU. This would typically be done in C or C++ but can also include C28x assembly code. The main CPU will also copy the CLA code to the program memory and, if needed, initialize the CLA data RAM(s). Once system initialization is complete and the application begins, the CLA will service its interrupts using the CLA assembly code (or tasks). Concurrently the main CPU can perform other tasks.

The C2000 Codegen tools V5.2.x and higher support CLA instructions when the following switch is set: --cla_support = cla0.

4.3.2 Typical CLA Initialization Sequence

A typical CLA initialization sequence is performed by the main CPU as described in this section.

1. Copy CLA code into the CLA program RAM

The source for the CLA code can initially reside in the flash or a data stream from a communications peripheral or anywhere the main CPU can access it. The debugger can also be used to load code directly to the CLA program RAM during development.

2. Initialize CLA data RAM if necessary

Populate the CLA data RAM with any required data coefficients or constants.

3. Configure the CLA registers

Configure the CLA registers, but keep interrupts disabled until later (leave MIER == 0):

- **Enable the CLA clock in the PCLKCR3 register.**

PCLKCR3 register is defined in the *System Control and Interrupts* chapter.

- **Populate the CLA task interrupt vectors: MVECT1 to MVECT8.**

Each vector needs to be initialized with the start address of the task to be executed when the CLA receives the associated interrupt. This address is the full 16-bit starting address of the task in the lower 64K section of memory.

- **Select the task interrupt sources**

For each task select the interrupt source in the CLA1TASKSRCSELx register. If a task is going to be generated by software, select no interrupt.

- **Enable IACK to start a task from software if desired**

To enable the IACK instruction to start a task set the MCTL[IACKE] bit. Using the IACK instruction avoids having to set and clear the EALLOW bit.

- **Map CLA data RAM(s) to CLA space if necessary**

Map the data RAM to the CLA space by first, assigning ownership of the memory block to the CLA by writing a 1 to the memory block's MemCfgRegs.LSxMSEL[MSEL_LSz] bit and then specifying the memory block as a CLA data block by writing a 0 to the MemCfgRegs.LSxCLAPGM[CLAPGM_LSz] bit. When an LSx memory is configured as a CLA data memory, the CLA read/write access are arbitrated along with CPU accesses. The user has the option of turning on CPU fetch or write protection to the memory by writing to the appropriate bits of the MemCfgRegs. LSxACCPROTx registers.

- **Map CLA program RAM to CLA space**

Map the CLA program RAM to CLA space by first, assigning ownership of the memory block to the CLA by writing a 1 to the memory block's MemCfgRegs.LSxMSEL[MSEL_LSz] bit and then specifying the memory block as CLA code memory by writing a 1 to the

MemCfgRegs.LSxCLAPGM[CLAPGM_LSx] bit. When an LSx memory is configured as CLA program memory, only debug accesses are allowed on cycles that the CLA is not fetching a new instruction.

4. Initialize the PIE vector table and registers

When a CLA task completes the associated interrupt in the PIE will be flagged. The CLA overflow and underflow flags also have associated interrupts within the PIE.

5. Enable CLA tasks/interrupts

Set appropriate bits in the interrupt enable register (MIER) to allow the CLA to service interrupts.

6. Initialize other peripherals

Initialize any peripherals (ePWM, ADC, and others) that will generate an interrupt to the CLA and be serviced by a CLA task.

The CLA is now ready to service interrupts and the message RAMs can be used to pass data between the CPU and the CLA. Typically mapping of the CLA program and data RAMs occurs only during the initialization process. If after some time you want to re-map these memories back to CPU space then disable interrupts and make sure all tasks have completed by checking the MIRUN register.

4.3.3 Debugging CLA Code

Debugging the CLA code is a simple process that occurs independently of the main CPU.

1. Insert a breakpoint in CLA code

Insert a CLA breakpoint (MDEBUGSTOP instruction) into the code where you want the CLA to halt, then rebuild and reload the code. Because the CLA does not flush its pipeline when you single-step, the MDEBUGSTOP instruction must be inserted as part of the code. The debugger cannot insert it as needed.

If CLA breakpoints are not enabled, then the MDEBUGSTOP will be ignored and is treated as a MNOP. The MDEBUGSTOP instruction can be placed anywhere in the CLA code as long as it is not within three instructions of a MBCNDD, MCCNDD, or MRCNDD instruction.

2. Enable CLA breakpoints

First, enable the CLA breakpoints in the debugger. In Code Composer Studio, this is done by connecting the core from the debug perspective. Breakpoints are disabled when the core is disconnected.

3. Start the task

There are three ways to start the task:

- The peripheral can assert an interrupt
- The main CPU can execute an IACK instruction, or
- You can manually write to the MIFRC register in the debugger window

When the task starts, the CLA will execute instructions until the MDEBUGSTOP is in the D2 phase of the pipeline. At this point, the CLA will halt and the pipeline will be frozen. The MPC register will reflect the address of the MDEBUGSTOP instruction.

4. Single-step the CLA code

Once halted, you can single-step the CLA code one cycle at a time. The behavior of a CLA single-step is different than the main C28x. When issuing a CLA single-step, the pipeline is clocked only one cycle and then again frozen. On the 28x CPU, the pipeline is flushed for each single-step.

You can also run to the next MDEBUGSTOP or to the end of the task. If another task is pending, it will automatically start when you run to the end of the task.

NOTE: A CLA fetch has higher priority than CPU debug reads. For this reason, it is possible for the CLA to permanently block CPU debug accesses if the CLA is executing in a loop. This might occur when initially developing CLA code due to a bug that causes an infinite loop. To avoid locking up the main CPU, the program memory will return all 0x0000 for CPU debug reads when the CLA is running. When the CLA is halted or idle then normal CPU debug read and write access to CLA program memory can be performed.

If the CLA gets caught in a infinite loop, you can use a soft or hard reset to exit the condition. A debugger reset will also exit the condition.

There are special cases that can occur when single-stepping a task such that the program counter, MPC, reaches the MSTOP instruction at the end of the task.

- **MPC halts at or after the MSTOP with a task already pending**

If you are single-stepping or halted in "task A" and "task B" comes in before the MPC reaches the MSTOP, then "task B" will start if you continue to step through the MSTOP instruction. Basically if "task B" is pending before the MPC reaches MSTOP in "task A" then there is no issue in "task B" starting and no special action is required.

- **MPC halts at or after the MSTOP with no task pending**

In this case you have single-stepped or halted in "task A" and the MPC has reached the MSTOP with no tasks pending. If "task B" comes in at this point, it will be flagged in the MIFR register but it may or may not start if you continue to single-step through the MSTOP instruction of "task A."

It depends on exactly when the new task comes in. To reliably start "task B" perform a soft reset and reconfigure the MIER bits. Once this is done, you can start single-stepping "task B."

This case can be handled slightly differently if there is control over when "task B" comes in (for

example using the IACK instruction to start the task). In this case you have single-stepped or halted in "task A" and the MPC has reached the MSTOP with no tasks pending. Before forcing "task B," run free to force the CLA out of the debug state. Once this is done you can force "task B" and continue debugging.

5. If desired, disable CLA breakpoints

In Code Composer Studio you can disable the CLA breakpoints by disconnecting the CLA core in the debug perspective. Make sure to first issue a run or reset; otherwise, the CLA will be halted and no other tasks will start.

4.3.4 CLA Illegal Opcode Behavior

If the CLA fetches an opcode that does not correspond to a legal instruction, it will behave as follows:

- The CLA will halt with the illegal opcode in the D2 phase of the pipeline as if it were a breakpoint. This will occur whether CLA breakpoints are enabled or not.
- The CLA will issue the task-specific interrupt to the PIE.
- The MIRUN bit for the task will remain set.

Further single-stepping is ignored once execution halts due to an illegal op-code. To exit this situation, issue either a soft or hard reset of the CLA as described in [Section 4.3.5](#).

4.3.5 Resetting the CLA

There may be times when you need to reset the CLA. For example, during code debug the CLA may enter an infinite loop due to a code bug. The CLA has two types of resets: hard and soft. Both of these resets can be performed by the debugger or by the main CPU.

- **Hard Reset**

Writing a 1 to the MCTL[HARDRESET] bit will perform a hard reset of the CLA. The behavior of a hard reset is the same as a system reset (via \overline{XRS} or the debugger). In this case all CLA configuration and execution registers will be set to their default state and CLA execution will halt.

- **Soft Reset**

Writing a 1 to the MCTL[SOFTRESET] bit performs a soft reset of the CLA. If a task is executing it will halt and the associated MIRUN bit will be cleared. All bits within the interrupt enable (MIER) register will also be cleared so that no new tasks start.

4.4 Pipeline

This section describes the CLA pipeline stages and presents cases where pipeline alignment must be considered.

4.4.1 Pipeline Overview

The CLA pipeline is very similar to the C28x pipeline. The pipeline has eight stages:

- **Fetch 1 (F1)**

During the F1 stage the program read address is placed on the CLA program address bus.

- **Fetch 2 (F2)**

During the F2 stage the instruction is read using the CLA program data bus.

- **Decode 1 (D1)**

During D1 the instruction is decoded.

- **Decode 2 (D2)**

Generate the data read address. Changes to MAR0 and MAR1 due to post-increment using indirect addressing takes place in the D2 phase. Conditional branch decisions are also made at this stage based on the MSTF register flags.

- **Read 1 (R1)**

Place the data read address on the CLA data-read address bus. If a memory conflict exists, the R1 stage will be stalled.

- **Read 2 (R2)**

Read the data value using the CLA data read data bus.

- **Execute (EXE)**

Execute the operation. Changes to MAR0 and MAR1 due to loading an immediate value or value from memory take place in this stage.

- **Write (W)**

Place the write address and write data on the CLA write data bus. If a memory conflict exists, the W stage will be stalled.

4.4.2 CLA Pipeline Alignment

The majority of the CLA instructions do not require any special pipeline considerations. This section lists the few operations that do require special consideration.

- **Write Followed by Read**

In both the C28x and the CLA pipeline the read operation occurs before the write. This means that if a read operation immediately follows a write, then the read will complete first as shown in [Table 4-2](#). In most cases this does not cause a problem since the contents of one memory location does not depend on the state of another. For accesses to peripherals where a write to one location can affect the value in another location the code must wait for the write to complete before issuing the read as shown in [Table 4-3](#).

This behavior is different for the 28x CPU. For the 28x CPU any write followed by read to the same location is protected by what is called write-followed-by-read protection. This protection automatically stalls the pipeline so that the write will complete before the read. In addition some peripheral frames are protected such that a 28x CPU write to one location within the frame will always complete before a read to the frame. The CLA does not have this protection mechanism. Instead the code must wait to perform the read.

Table 4-2. Write Followed by Read - Read Occurs First

Instruction	F1	F2	D1	D2	R1	R2	E	W
I1 MMOV16 @Reg1, MR3	I1							
I2 MMOV16 MR2, @Reg2	I2	I1						
		I2	I1					
			I2	I1				
				I2	I1			
					I2	I1		
						I2	I1	
							I2	I1

Table 4-3. Write Followed by Read - Write Occurs First

Instruction	F1	F2	D1	D2	R1	R2	E	W
I1 MMOV16 @Reg1, MR3	I1							
I2	I2	I1						
I3	I3	I2	I1					
I4	I4	I3	I2	I1				
I5 MMOV16 MR2, @Reg2	I5	I4	I3	I2	I1			
		I5	I4	I3	I2	I1		
			I5	I4	I3	I2	I1	
				I5	I4	I3	I2	I1
					I5	I4	I3	
						I5	I4	
							I5	

- Delayed Conditional instructions: MBCNDD, MCCNDD and MRCNDD**

Referring to [Example 4-1](#), the following applies to delayed conditional instructions:

- **I1**

I1 is the last instruction that can effect the CNDF flags for the branch, call or return instruction. The CNDF flags are tested in the D2 phase of the pipeline. That is, a decision is made whether to branch or not when [MBCNDD](#), [MCCNDD](#) or [MRCNDD](#) is in the D2 phase.

- **I2, I3 and I4**

The three instructions preceding MBCNDD can change MSTF flags but will have no effect on whether the MBCNDD instruction branches or not. This is because the flag modification will occur after the D2 phase of the branch, call or return instruction. These three instructions must not be a [MSTOP](#), [MDEBUGSTOP](#), [MBCNDD](#), [MCCNDD](#) or [MRCNDD](#).

- **I5, I6 and I7**

The three instructions following a branch, call or return are always executed irrespective of whether the condition is true or not. These instructions must not be [MSTOP](#), [MDEBUGSTOP](#), [MBCNDD](#), [MCCNDD](#) or [MRCNDD](#).

For a more detailed description refer to the functional description for [MBCNDD](#), [MCCNDD](#) and [MRCNDD](#).

Example 4-1. Code Fragment For MBCNDD, MCCNDD or MRCNDD

```
<Instruction 1> ; I1 Last instruction that can affect flags for
                  ; the branch, call or return operation

<Instruction 2> ; I2 Cannot be stop, branch, call or return
<Instruction 3> ; I3 Cannot be stop, branch, call or return
<Instruction 4> ; I4 Cannot be stop, branch, call or return

<branch/call/ret> ; MBCNDD, MCCNDD or MRCNDD

                  ; I5-I7: Three instructions after are always
                  ; executed whether the branch/call or return is
                  ; taken or not

<Instruction 5> ; I5 Cannot be stop, branch, call or return
<Instruction 6> ; I6 Cannot be stop, branch, call or return
<Instruction 7> ; I7 Cannot be stop, branch, call or return

<Instruction 8> ; I8
<Instruction 9> ; I9
....
```

- **Stop or Halting a Task: MSTOP and MDEBUGSTOP**

The **MSTOP** and **MDEBUGSTOP** instructions cannot be placed three instructions before or after a conditional branch, call or return instruction (**MBCNDD**, **MCCNDD** or **MRCNDD**). Refer to [Example 4-1](#). To single-step through a branch/call or return, insert the **MDEBUGSTOP** at least four instructions back and step from there.

- **Loading MAR0 or MAR1**

A load of auxiliary register MAR0 or MAR1 will occur in the EXE phase of the pipeline. Any post increment of MAR0 or MAR1 using indirect addressing will occur in the D2 phase of the pipeline. Referring to [Example 4-2](#), the following applies when loading the auxiliary registers:

- **I1 and I2**

The two instructions following the load instruction will use the value in MAR0 or MAR1 before the update occurs.

- **I3**

Loading of an auxiliary register occurs in the EXE phase while updates due to post-increment addressing occur in the D2 phase. Thus I3 cannot use the auxiliary register or there will be a conflict. In the case of a conflict, the update due to address-mode post increment will win and the auxiliary register will not be updated with #_X.

- **I4**

Starting with the 4th instruction MAR0 or MAR1 will have the new value.

Example 4-2. Code Fragment for Loading MAR0 or MAR1

```
; Assume MAR0 is 50 and #_X is 20

MMOV16 MAR0, #_X ; Load MAR0 with address of X (20)
<Instruction 1> ; I1 Will use the old value of MAR0 (50)
<Instruction 2> ; I2 Will use the old value of MAR0 (50)
<Instruction 3> ; I3 Cannot use MAR0
<Instruction 4> ; I4 Will use the new value of MAR0 (20)
<Instruction 5> ; I5 Will use the new value of MAR0 (20)
....
```

4.4.2.1 ADC Early Interrupt to CLA Response

The ADC offers the option to generate an early interrupt pulse when the ADC begins conversion. This option is selected by setting the ADCCTL1[INTPULSEPOS] bit as documented in the Analog-to-Digital Converter and Comparator section in this manual. If this option is used to start a CLA task then the CLA will be able to read the result as soon as the conversion completes and the ADC result register updates. This just-in-time sampling along with the low interrupt response of the CLA enable faster system response and higher frequency control loops.

The timing for the ADC conversion is shown in the ADC Reference Guide timing diagrams. From a CLA perspective, the pipeline activity is shown in [Table 4-4](#). The 8th instruction is in the R2 phase just in time to read the result register. While the first seven (7) instructions in the task (I1 to I7) will enter the R2 phase of the pipeline too soon to read the conversion, they can be efficiently used for pre-processing calculations needed by the task.

Table 4-4. ADC to CLA Early Interrupt Response

ADC Activity	CLA Activity	F1	F2	D1	D2	R1	R2	E	W
Sample									
Sample									
...									
Sample									
Conversion (1)	Interrupt Received								
Conversion (2)	Task Startup								
Conversion (3)	Task Startup								
Conversion (4)	I1	I1							
Conversion (5)	I2	I2	I1						
Conversion (6)	I3	I3	I2	I1					
Conversion (7)	I4	I4	I3	I2	I1				
Conversion (8)	I5	I5	I4	I3	I2	I1			
Conversion (9)	I6	I6	I5	I4	I3	I2	I1		
Conversion (10)	I7	I7	I6	I5	I4	I3	I2		
Conversion (11)	I8 Read ADC RESULT	I8	I7	I6	I5	I4	I3		
Conversion (12)		I8	I7	I6	I5	I4	I2		
Conversion (13)			I8	I7	I6	I5	I1		
Conversion Complete				I8	I7	I6	I1		
RESULT Latched					I8	I7	I1		
RESULT Available						I8			

4.4.3 Parallel Instructions

Parallel instructions are single opcodes that perform two operations in parallel. The following types of parallel instructions are available: math operation in parallel with a move operation, or two math operations in parallel. Both operations complete in a single cycle and there are no special pipeline alignment requirements.

Example 4-3. Math Operation with Parallel Load

```
; MADDF32 || MMOV32 instruction: 32-bit floating-point add with parallel move
; MADDF32 is a 1 cycle operation
; MMOV32 is a 1 cycle operation
    MADDF32    MR0, MR1, #2      ; MR0 = MR1 + 2,
|| MMOV32    MR1, @Val        ; MR1 gets the contents of Val
                                ; <-- MMOV32 completes here (MR1 is valid)
                                ; <-- DDF32 completes here (MR0 is valid)
MMPYF32    MR0, MR0, MR1     ; Any instruction, can use MR1 and/or MR0
```

Example 4-4. Multiply with Parallel Add

```
; MMPYF32 || MADDF32 instruction: 32-bit floating-point multiply with parallel add
; MMPYF32 is a 1 cycle operation
; MADDF32 is a 1 cycle operation
    MMPYF32 MR0, MR1, MR3          ; MR0 = MR1 * MR3
||  MADDF32 MR1, MR2, MR0          ; MR1 = MR2 + MR0 (Uses value of MR0 before MMPYF32)
                                ; <-- MMPYF32 and MADDF32 complete here (MR0 and MR1 are valid)
    MMPYF32 MR1, MR1, MR0          ; Any instruction, can use MR1 and/or MR0
```

4.5 Instruction Set

This section describes the assembly language instructions of the control law accelerator. Also described are parallel operations, conditional operations, resource constraints, and addressing modes. The instructions listed here are independent from C28x and C28x+FPU instruction sets.

4.5.1 Instruction Descriptions

This section gives detailed information on the instruction set. Each instruction may present the following information:

- Operands
- Opcode
- Description
- Exceptions
- Pipeline
- Examples
- See also

The example INSTRUCTION is shown to familiarize you with the way each instruction is described. The example describes the kind of information you will find in each part of the individual instruction description and where to obtain more information. CLA instructions follow the same format as the C28x; the source operand(s) are always on the right and the destination operand(s) are on the left.

The explanations for the syntax of the operands used in the instruction descriptions for the C28x CLA are given in [Table 4-5](#).

Table 4-5. Operand Nomenclature

Symbol	Description
#16FHi	16-bit immediate (hex or float) value that represents the upper 16-bits of an IEEE 32-bit floating-point value. Lower 16-bits of the mantissa are assumed to be zero.
#16FHiHex	16-bit immediate hex value that represents the upper 16-bits of an IEEE 32-bit floating-point value. Lower 16-bits of the mantissa are assumed to be zero.
#16FLoHex	A 16-bit immediate hex value that represents the lower 16-bits of an IEEE 32-bit floating-point value
#32Fhex	32-bit immediate value that represents an IEEE 32-bit floating-point value
#32F	Immediate float value represented in floating-point representation
#0.0	Immediate zero
#SHIFT	Immediate value of 1 to 32 used for arithmetic and logical shifts.
addr	Opcode field indicating the addressing mode
CNDF	Condition to test the flags in the MSTF register
FLAG	Selected flags from MSTF register (OR) 8 bit mask indicating which floating-point status flags to change
MAR0	auxiliary register 0
MAR1	auxiliary register 1
MARx	Either MAR0 or MAR1
mem16	16-bit memory location accessed using direct, indirect, or offset addressing modes
mem32	32-bit memory location accessed using direct, indirect, or offset addressing modes
MRa	MR0 to MR3 registers
MRb	MR0 to MR3 registers
MRc	MR0 to MR3 registers
MRd	MR0 to MR3 registers
MRe	MR0 to MR3 registers
MRf	MR0 to MR3 registers
MSTF	CLA Floating-point Status Register
shift	Opcode field indicating the number of bits to shift.
VALUE	Flag value of 0 or 1 for selected flag (OR) 8 bit mask indicating the flag value; 0 or 1

Each instruction has a table that gives a list of the operands and a short description. Instructions always have their destination operand(s) first followed by the source operand(s).

Table 4-6. INSTRUCTION dest, source1, source2 Short Description

	Description
dest1	Description for the 1st operand for the instruction
source1	Description for the 2nd operand for the instruction
source2	Description for the 3rd operand for the instruction
Opcode	This section shows the opcode for the instruction
Description	Detailed description of the instruction execution is described. Any constraints on the operands imposed by the processor or the assembler are discussed.
Restrictions	Any constraints on the operands or use of the instruction imposed by the processor are discussed.
Pipeline	This section describes the instruction in terms of pipeline cycles as described in Section 4.4
Example	Examples of instruction execution. If applicable, register and memory values are given before and after instruction execution. Some examples are code fragments while other examples are full tasks that assume the CLA is correctly configured and the main CPU has passed it data.
Operands	Each instruction has a table that gives a list of the operands and a short description. Instructions always have their destination operand(s) first followed by the source operand(s).

4.5.2 Addressing Modes and Encoding

The CLA uses the same address to access data and registers as the main CPU. For example if the main CPU accesses an ePWM register at address 0x00 6800, then the CLA will access it using address 0x6800. Since all CLA accessible memory and registers are within the low 64k x 16 of memory, only the low 16-bits of the address are used by the CLA.

To address the CLA data memory, message RAMs and shared peripherals, the CLA supports two addressing modes:

- Direct addressing mode: Uses the address of the variable or register directly.
- Indirect addressing with 16-bit post increment. This mode uses either XAR0 or XAR1.

The CLA does not use a data page pointer or a stack pointer. The two addressing modes are encoded as shown [Table 4-7](#).

Table 4-7. Addressing Modes

Addressing Mode	'addr' Opcode Field Encode ⁽¹⁾	Description
@dir	0000	<p>Direct Addressing Mode</p> <p>Example 1: MMOV32 MR1, @_VarA</p> <p>Example 2: MMOV32 MR1, @_EPwm1Regs.CMPA.all</p> <p>In this case the 'mmmm mmmm mmmm mmmm' opcode field will be populated with the 16-bit address of the variable. This is the low 16-bits of the address that you would use to access the variable using the main CPU.</p> <p>For example @_VarA will populate the address of the variable VarA. and @_EPwm1Regs.CMPA.all will populate the address of the CMPA register.</p>
*MAR0[#imm16]++	0001	MAR0 Indirect Addressing with 16-bit Immediate Post Increment
*MAR1[#imm16]++	0010	<p>MAR1 Indirect Addressing with 16-bit Immediate Post Increment</p> <p>addr = MAR0 (or MAR1) Access memory using the address stored in MAR0 (or MAR1). MAR0 (or MAR1) += Then post increment MAR0 (or MAR1) by #imm16. #imm16</p> <p>Example 1: MMOV32 MR0, *MAR0[2]++ Example 2: MMOV32 MR1, *MAR1[-2]++</p> <p>For a post increment of 0 the assembler will accept both *MAR0 and *MAR0[0]++.</p> <p>The 'mmmm mmmm mmmm mmmm' opcode field will be populated with the signed 16-bit pointer offset. For example if #imm16 is 2, then the opcode field will be 0x0002. Likewise if #imm16 is -2, then the opcode field will be 0xFFFF.</p> <p>If addition of the 16-bit immediate causes overflow, then the value will wrap around on a 16-bit boundary.</p>
*MAR0+[#imm16]	0101	MAR0 Offset Addressing with 16-bit Immediate Offset
*MAR1+[#imm16]	0110	<p>MAR1 Offset Addressing with 16-bit Immediate Offset</p> <p>addr = MAR0 Add the offset #imm16 (or MAR1) + #imm16 to address stored in MAR0(MAR1) to access the desired memory location</p> <p>Example 1: MMOV32 MR0, *MAR0+[2] Example 1: MMOV32 MR1, *MAR1+[-2]</p> <p>The 'mmmm mmmm mmmm mmmm' opcode field will be populated with the signed 16-bit pointer offset. For example if #imm16 is 2, then the opcode field will be 0x0002. Likewise if #imm16 is -2, then the opcode field will be 0xFFFF.</p> <p>If the addition of the 16-bit immediate causes overflow, the value will wrap around on a 16-bit boundary.</p>

⁽¹⁾ Values not shown are reserved.

Encoding for the shift fields in the MASR32, MLSR32 and MLSL32 instructions is shown in [Table 4-8](#)

Table 4-8. Shift Field Encoding

Shift Value	'shift' Opcode Field Encode
1	0000
2	0001
3	0010
....
32	1111

Table 4-9 shows the condition field encoding for conditional instructions such as MNEGF, MSWAPF, MBCNDD, MCCNDD, and MRCNDD

Table 4-9. Condition Field Encoding

Encode ⁽¹⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽²⁾	Unconditional with flag modification	None

⁽¹⁾ Values not shown are reserved.

⁽²⁾ This is the default operation if no CNDF field is specified. This condition will allow the ZF and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

4.5.3 Instructions

The instructions are listed alphabetically, preceded by a summary.

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MMABSF32 MRa, MRb 32-Bit Floating-Point Absolute Value**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1110 0010 0000

Description

The absolute value of MRb is loaded into MRa. Only the sign bit of the operand is modified by the MMABSF32 instruction.

```
if (MRb < 0) {MRa = -MRb};  

else {MRa = MRb};
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified as follows:

```
NF = 0;  

ZF = 0;  

if (MRa(30:23) == 0) ZF = 1;
```

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ MRO, #-2.0 ; MRO = -2.0 (0xC0000000)  

MMABSF32 MRO, MRO ; MRO = 2.0 (0x40000000), ZF = NF = 0

MMOVIZ MRO, #5.0 ; MRO = 5.0 (0x40A00000)  

MMABSF32 MRO, MRO ; MRO = 5.0 (0x40A00000), ZF = NF = 0

MMOVIZ MRO, #0.0 ; MRO = 0.0
MMABSF32 MRO, MRO ; MRO = 0.0 ZF = 1, NF = 0
```

See also

[MNEGF32 MRa, MRb {}, CNDF}](#)

MADD32 MRa, MRb, MRc 32-Bit Integer Add

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point destination register (MR0 to MR3)
MRc	CLA floating-point destination register (MR0 to MR3)

Opcode

LSW: 0000 0000 000cc bbaa
 MSW: 0111 1110 1100 0000

Description

32-bit integer addition of MRb and MRc.

MRa(31:0) = MRb(31:0) + MRc(31:0);

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
NF = MRa(31);
ZF = 0;
if(MRa(31:0) == 0) { ZF = 1; };
```

Pipeline

This is a single-cycle instruction.

Example

```
; Given A = (int32)1
;           B = (int32)2
;           C = (int32)-7
;
; Calculate Y2 = A + B + C
;
_Cla1Task1:
    MMOV32 MR0, @_A      ; MR0 = 1 (0x00000001)
    MMOV32 MR1, @_B      ; MR1 = 2 (0x00000002)
    MMOV32 MR2, @_C      ; MR2 = -7 (0xFFFFFFF9)
    MADD32 MR3, MR0, MR1 ; A + B
    MADD32 MR3, MR2, MR3 ; A + B + C = -4 (0xFFFFFFF4)
    MMOV32 @_y2, MR3     ; Store y2
    MSTOP                 ; end of task
```

See also

[MAND32 MRa, MRb, MRc](#)
[MASR32 MRa, #SHIFT](#)
[MLSL32 MRa, #SHIFT](#)
[MLSR32 MRa, #SHIFT](#)
[MOR32 MRa, MRb, MRc](#)
[MXOR32 MRa, MRb, MRc](#)
[MSUB32 MRa, MRb, MRc](#)

MADDF32 MRa, #16FHi, MRb 32-Bit Floating-Point Addition**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: IIII IIII IIII IIII
 MSW: 0111 0111 1100 bbba

Description

Add MRb to the floating-point value represented by the immediate operand. Store the result of the addition in MRa.

#16FHi is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. #16FHi is most useful for representing constants where the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). The assembler will accept either a hex or float as the immediate value. That is, the value -1.5 can be represented as #-1.5 or #0xBFC0.

MRa = MRb + #16FHi:0;

This instruction can also be written as MADDF32 MRa, MRb, #16FHi.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MADDF32 generates an underflow condition.
- LVF = 1 if MADDF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example

```
; Add to MR1 the value 2.0 in 32-bit floating-point format
; Store the result in MR0
MADDF32 MR0, #2.0, MR1      ; MR0 = 2.0 + MR1

; Add to MR3 the value -2.5 in 32-bit floating-point format
; Store the result in MR2
MADDF32 MR2, #-2.5, MR3     ; MR2 = -2.5 + MR3

; Add to MR3 the value 0x3FC00000 (1.5)
; Store the result in MR3
MADDF32 MR3, #0x3FC0, MR3   ; MR3 = 1.5 + MR3
```

See also

[MADDF32 MRa, MRb, #16FHi](#)
[MADDF32 MRa, MRb, MRC](#)
[MADDF32 MRd, MRe, MRf || MMOV32 MRa, mem32](#)
[MADDF32 MRd, MRe, MRf || MMOV32 mem32, MRa](#)
[MMPYF32 MRa, MRb, MRC || MADDF32 MRd, MRe, MRf](#)

MADDF32 MRa, MRb, #16FHi 32-Bit Floating-Point Addition**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.

Opcode

LSW: IIII IIII IIII IIII
 MSW: 0111 0111 1100 bbba

Description

Add MRb to the floating-point value represented by the immediate operand. Store the result of the addition in MRa.

#16FHi is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. #16FHi is most useful for representing constants where the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). The assembler will accept either a hex or float as the immediate value. That is, the value -1.5 can be represented as #-1.5 or #0xBFC0.

MRa = MRb + #16FHi:0;

This instruction can also be written as MADDF32 MRa, #16FHi, MRb.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MADDF32 generates an underflow condition.
- LVF = 1 if MADDF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example 1

```
; X is an array of 32-bit floating-point values
; Find the maximum value in an array X
; and store it in Result
;
_Cla1Task1:
  MMOV16    MAR1,#_X          ; Start address
  MUI16TOF32 MR0, @_len       ; Length of the array
  MNOP
  MNOP
  MMOV32    MR1, *MAR1[2]++   ; MR1 = X0
LOOP
  MMOV32    MR2, *MAR1[2]++   ; MR2 = next element
  MAXF32    MR1, MR2          ; MR1 = MAX(MR1, MR2)
  MADDF32   MR0, MR0, #-1.0   ; Decrement the counter
  MCMPF32   MR0 #0.0          ; Set/clear flags for MBCNDD
  MNOP
  MNOP
  MNOP
  MBCNDD LOOP, NEQ           ; Branch if not equal to zero
  MMOV32 @_Result, MR1        ; Always executed
  MNOP
  MNOP
  MNOP
  MSTOP                         ; End of task
```

Example 2

```

; Show the basic operation of MADDF32
;
; Add to MR1 the value 2.0 in 32-bit floating-point format
; Store the result in MR0
    MADDF32 MR0, MR1, #2.0      ; MR0 = MR1 + 2.0

; Add to MR3 the value -2.5 in 32-bit floating-point format
; Store the result in MR2
    MADDF32 MR2, MR3, #-2.5     ; MR2 = MR3 + (-2.5)

; Add to MR0 the value 0x3FC00000 (1.5)
; Store the result in MR0
    MADDF32 MR0, MR0, #0x3FC0   ; MR0 = MR0 + 1.5

```

See also

[MADDF32 MRa, #16FHi, MRb](#)
[MADDF32 MRa, MRb, MRc](#)
[MADDF32 MRd, MRe, MRf || MMOV32 MRa, mem32](#)
[MADDF32 MRd, MRe, MRf || MMOV32 mem32, MRa](#)
[MMPYF32 MRa, MRb, MRc || MADDF32 MRd, MRe, MRf](#)

MADDF32 MRa, MRb, MRc 32-Bit Floating-Point Addition

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
MRc	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 000 0000 00cc bbaa
 MSW: 0111 1100 0010 0000

Description

Add the contents of MRc to the contents of MRb and load the result into MRa.

MRa = MRb + MRc;

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MADDF32 generates an underflow condition.
- LVF = 1 if MADDF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example

```
; Given M1, X1 and B1 are 32-bit floating point numbers
; Calculate Y1 = M1*X1+B1
;
_Cla1Task1:
    MMOV32 MR0,@M1      ; Load MR0 with M1
    MMOV32 MR1,@X1      ; Load MR1 with X1
    MMPYF32 MR1,MR1,MR0 ; Multiply M1*X1
    || MMOV32 MR0,@B1    ; and in parallel load MR0 with B1
    MADDF32 MR1,MR1,MR0 ; Add M*X1 to B1 and store in MR1
    MMOV32 @Y1,MR1      ; Store the result
    MSTOP                ; end of task
```

See also

[MADDF32 MRa, #16FHi, MRb](#)
[MADDF32 MRa, MRb, #16FHi](#)
[MADDF32 MRd, MRe, MRf || MMOV32 MRa, mem32](#)
[MADDF32 MRd, MRe, MRf || MMOV32 mem32, MRa](#)
[MMPYF32 MRa, MRb, MRc || MADDF32 MRd, MRe, MRf](#)

MADDF32 MRd, MRe, MRf || MMOV32 mem32, MRa 32-Bit Floating-Point Addition with Parallel Move**Operands**

MRd	CLA floating-point destination register for the MADDF32 (MR0 to MR3)
MRe	CLA floating-point source register for the MADDF32 (MR0 to MR3)
MRf	CLA floating-point source register for the MADDF32 (MR0 to MR3)
mem32	32-bit memory location accessed using one of the available addressing modes. This will be the destination of the MMOV32.
MRa	CLA floating-point source register for the MMOV32 (MR0 to MR3)

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0101 ffee ddaa addr

Description

Perform an MADDF32 and a MMOV32 in parallel. Add MRf to the contents of MRe and store the result in MRd. In parallel move the contents of MRa to the 32-bit location mem32.

```
MRd = MRe + MRf;
[mem32] = MRa;
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MADDF32 generates an underflow condition.
- LVF = 1 if MADDF32 generates an overflow condition.

Pipeline

Both MADDF32 and MMOV32 complete in a single cycle.

Example

```
; Given A, B and C are 32-bit floating-point numbers
; Calculate Y2 = (A * B)
;           Y3 = (A * B) + C
;
_Cla1Task2:
    MMOV32    MR0, @_A          ; Load MR0 with A
    MMOV32    MR1, @_B          ; Load MR1 with B
    MMPYF32   MR1, MR1, MR0    ; Multiply A*B
    || MMOV32   MR0, @_C          ;      and in parallel load MR0 with C
    || MADDF32  MR1, MR1, MR0    ; Add (A*B) to C
    || MMOV32   @_Y2, MR1        ;      and in parallel store A*B
    || MMOV32   @_Y3, MR1        ; Store the A*B + C
    MSTOP
```

See also

[MADDF32 MRa, #16FHi, MRb](#)
[MADDF32 MRa, MRb, #16FHi](#)
[MADDF32 MRa, MRb, MRc](#)
[MMPYF32 MRa, MRb, MRc || MADDF32 MRd, MRe, MRf](#)
[MADDF32 MRd, MRe, MRf || MMOV32 MRa, mem32](#)

MADDF32 MRd, MRe, MRf ||MMOV32 MRa, mem32 32-Bit Floating-Point Addition with Parallel Move

Operands

MRd	CLA floating-point destination register for the MADDF32 (MR0 to MR3). MRd cannot be the same register as MRa.
MRe	CLA floating-point source register for the MADDF32 (MR0 to MR3)
MRf	CLA floating-point source register for the MADDF32 (MR0 to MR3)
MRa	CLA floating-point destination register for the MMOV32 (MR0 to MR3). MRa cannot be the same register as MRd.
mem32	32-bit memory location accessed using one of the available addressing modes. This is the source for the MMOV32.

Opcode

LSW: mmmm mmmm mmmm mmmm
MSW: 0001 ffee ddaa addr

Description

Perform an MADDF32 and a MMOV32 operation in parallel. Add MRf to the contents of MRe and store the result in MRd. In parallel move the contents of the 32-bit location mem32 to MRa.

```
MRd = MRe + MRf;
MRa = [mem32];
```

Restrictions

The destination register for the MADDF32 and the MMOV32 must be unique. That is, MRa and MRd cannot be the same register.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MADDF32 generates an underflow condition.
- LVF = 1 if MADDF32 generates an overflow condition.

The MMOV32 Instruction will set the NF and ZF flags as follows:

```
NF = MRa(31);
ZF = 0;
if(MRa(30:23) == 0) { ZF = 1; NF = 0; };
```

Pipeline

The MADDF32 and the MMOV32 both complete in a single cycle.

Example 1

```
; Given A, B and C are 32-bit floating-point numbers
; Calculate Y1 = A + 4B
;           Y2 = A + C
;
_Cla1Task1:
    MMOV32 MR0, @A          ; Load MR0 with A
    MMOV32 MR1, @B          ; Load MR1 with B
    MMPYF32 MR1, MR1, #4.0  ; Multiply 4 * B
    || MMOV32 MR2, @C          and in parallel load C
    MADDF32 MR3, MR0, MR1   ; Add A + 4B
    MADDF32 MR3, MR0, MR2   ; Add A + C
    || MMOV32 @Y1, MR3          and in parallel store A+4B
    MMOV32 @Y2, MR3          ; store A + C MSTOP
                           ; end of task
```

Example 2

```

; Given A, B and C are 32-bit floating-point numbers
; Calculate Y3 = (A + B)
;           Y4 = (A + B) * C
;
_Cla1Task2:
    MMOV32 MR0, @A          ; Load MR0 with A
    MMOV32 MR1, @B          ; Load MR1 with B
    MADDF32 MR1, MR1, MR0   ; Add A+B
|| MMOV32 MR0, @C          ; and in parallel load MR0 with C
    MMPYF32 MR1, MR1, MR0   ; Multiply (A+B) by C
|| MMOV32 @Y3, MR1         ; and in parallel store A+B
    MMOV32 @Y4, MR1         ; Store the (A+B) * C
    MSTOP                   ; end of task

```

See also

[MADDF32 MRa, #16FHi, MRb](#)
[MADDF32 MRa, MRb, #16FHi](#)
[MADDF32 MRa, MRb, MRc](#)
[MADDF32 MRd, MRe, MRf || MMOV32 mem32, MRa](#)
[MMPYF32 MRa, MRb, MRc || MADDF32 MRd, MRe, MRf](#)

MAND32 MRa, MRb, MRc Bitwise AND**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
MRc	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 00cc bbba
 MSW: 0111 1100 0110 0000

Description

Bitwise AND of MRb with MRc.

MRa(31:0) = MRb(31:0) AND MRc(31:0);

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
NF = MRa(31);
ZF = 0;
if(MRa(31:0) == 0) { ZF = 1; }
```

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ    MR0,      #0x5555 ; MR0 = 0x5555AAAA
MMOVXI    MR0,      #0xAAAA

MMOVIZ    MR1,      #0x5432 ; MR1 = 0x5432FEDC
MMOVXI    MR1,      #0xFEDC

; 0101 AND 0101 = 0101 (5)
; 0101 AND 0100 = 0100 (4)
; 0101 AND 0011 = 0001 (1)
; 0101 AND 0010 = 0000 (0)
; 1010 AND 1111 = 1010 (A)
; 1010 AND 1110 = 1010 (A)
; 1010 AND 1101 = 1000 (8)
; 1010 AND 1100 = 1000 (8)

MAND32 MR2, MR1, MR0      ; MR3 = 0x5410AA88
```

See also

[MADD32 MRa, MRb, MRc](#)
[MASR32 MRa, #SHIFT](#)
[MLSL32 MRa, #SHIFT](#)
[MLSR32 MRa, #SHIFT](#)
[MOR32 MRa, MRb, MRc](#)
[MXOR32 MRa, MRb, MRc](#)
[MSUB32 MRa, MRb, MRc](#)

MASR32 MRa, #SHIFT Arithmetic Shift Right**Operands**

MRa	CLA floating-point source/destination register (MR0 to MR3)
#SHIFT	Number of bits to shift (1 to 32)

Opcode

LSW: 0000 0000 0shi ftaa
 MSW: 0111 1011 0100 0000

Description

Arithmetic shift right of MRa by the number of bits indicated. The number of bits can be 1 to 32.

MARa(31:0) = Arithmetic Shift(MARa(31:0) by #SHIFT bits);

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
NF = MRa(31);
ZF = 0;
if(MRa(31:0) == 0) { ZF = 1; }
```

Pipeline

This is a single-cycle instruction.

Example

```
; Given m2 = (int32)32
;           x2 = (int32)64
;           b2 = (int32)-128
;
; Calculate
;           m2 = m2/2
;           x2 = x2/4
;           b2 = b2/8
;
_ClalTask2:
    MMOV32 MR0, @_m2 ; MR0 = 32 (0x00000020)
    MMOV32 MR1, @_x2 ; MR1 = 64 (0x00000040)
    MMOV32 MR2, @_b2 ; MR2 = -128 (0xFFFFFFF80)
    MASR32 MR0, #1   ; MR0 = 16 (0x00000010)
    MASR32 MR1, #2   ; MR1 = 16 (0x00000010)
    MASR32 MR2, #3   ; MR2 = -16 (0xFFFFFFF0)
    MMOV32 @_m2, MR0 ; store results
    MMOV32 @_x2, MR1
    MMOV32 @_b2, MR2
    MSTOP ; end of task
```

See also

[MADD32 MRa, MRb, MRc](#)
[MAND32 MRa, MRb, MRc](#)
[MLSL32 MRa, #SHIFT](#)
[MLSR32 MRa, #SHIFT](#)
[MOR32 MRa, MRb, MRc](#)
[MXOR32 MRa, MRb, MRc](#)
[MSUB32 MRa, MRb, MRc](#)

MBCNDD 16BitDest {, CNDF} Branch Conditional Delayed**Operands**

16BitDest	16-bit destination if condition is true
CNDF	Optional condition tested

Opcode

LSW: dest dest dest dest
 MSW: 0111 1001 1000 cndf

Description

If the specified condition is true, then branch by adding the signed 16BitDest value to the MPC value. Otherwise, continue without branching. If the address overflows, it wraps around. Therefore a value of "0xFFFF" will put the MPC back to the MBCNDD instruction.

Please refer to the pipeline section for important information regarding this instruction.

```
if (CNDF == TRUE) MPC += 16BitDest;
```

CNDF is one of the following conditions:

Encode ⁽¹⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽²⁾	Unconditional with flag modification	None

⁽¹⁾ Values not shown are reserved.

⁽²⁾ This is the default operation if no CNDF field is specified. This condition will allow the ZF and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

Restrictions

The MBCNDD instruction is not allowed three instructions before or after a MBCNDD, MCCNDD or MRCNDD instruction. Refer to the pipeline section for more information.

Flags

This instruction does not modify flags in the MSTF register.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

The MBCNDD instruction by itself is a single-cycle instruction. As shown in [Table 4-11](#) for each branch 6 instruction slots are executed; three before the branch instruction (I2-I4) and three after the branch instruction (I5-I7). The total number of cycles for a branch taken or not taken depends on the usage of these slots. That is, the number of cycles depends on how many slots are filled with a MNOP as well as which slots are filled. The effective number of cycles for a branch can, therefore, range from 1 to 7 cycles. The number of cycles for a branch taken may not be the same as for a branch not taken.

Referring to [Table 4-11](#) and [Table 4-12](#), the instructions before and after MBCNDD have the following properties:

- **I1**
 - I1 is the last instruction that can effect the CNDF flags for the MBCNDD instruction. The CNDF flags are tested in the D2 phase of the pipeline. That is, a decision is made whether to branch or not when MBCNDD is in the D2 phase.
 - There are no restrictions on the type of instruction for I1.
- **I2, I3 and I4**
 - The three instructions proceeding MBCNDD can change MSTF flags but will have no effect on whether the MBCNDD instruction branches or not. This is because the flag modification will occur after the D2 phase of the MBCNDD instruction.
 - These instructions must not be the following: MSTOP, MDEBUGSTOP, MBCNDD, MCCNDD or MRCNDD.
- **I5, I6 and I7**
 - The three instructions following MBCNDD are always executed irrespective of whether the branch is taken or not.
 - These instructions must not be the following: MSTOP, MDEBUGSTOP, MBCNDD, MCCNDD or MRCNDD.

```

<Instruction 1> ; I1 Last instruction that can affect flags for
                  ; the MBCNDD operation
<Instruction 2> ; I2 Cannot be stop, branch, call or return
<Instruction 3> ; I3 Cannot be stop, branch, call or return
<Instruction 4> ; I4 Cannot be stop, branch, call or return
MBCNDD _Skip, NEQ ; Branch to Skip if not equal to zero
                    ; Three instructions after MBCNDD are always
                    ; executed whether the branch is taken or not
<Instruction 5> ; I5 Cannot be stop, branch, call or return
<Instruction 6> ; I6 Cannot be stop, branch, call or return
<Instruction 7> ; I7 Cannot be stop, branch, call or return
<Instruction 8> ; I8
<Instruction 9> ; I9
...
_Skip:
<Destination 1> ; d1 Can be any instruction
<Destination 2> ; d2
<Destination 3> ; d3
...
...
MSTOP
...

```

Table 4-11. Pipeline Activity For MBCNDD, Branch Not Taken

Instruction	F1	F2	D1	D2	R1	R2	E	W
I1	I1							
I2	I2	I1						
I3	I3	I2	I1					
I4	I4	I3	I2	I1				
MBCNDD	MBCNDD	I4	I3	I2	I1			
I5	I5	MBCNDD	I4	I3	I2	I1		
I6	I6	I5	MBCNDD	I4	I3	I2	I1	
I7	I7	I6	I5	MBCNDD	I4	I3	I2	
I8	I8	I7	I6	I5	-	I4	I3	
I9	I9	I8	I7	I6	I5	-	I4	
I10	I10	I9	I8	I7	I6	I5	-	
		I10	I9	I8	I7	I6	I5	
			I10	I9	I8	I7	I6	
				I10	I9	I8	I7	
					I10	I9	I8	
						I10	I9	
							I10	

Table 4-12. Pipeline Activity For MBCNDD, Branch Taken

Instruction	F1	F2	D1	D2	R1	R2	E	W
I1	I1							
I2	I2	I1						
I3	I3	I2	I1					
I4	I4	I3	I2	I1				
MBCNDD	MBCNDD	I4	I3	I2	I1			
I5	I5	MBCNDD	I4	I3	I2	I1		
I6	I6	I5	MBCNDD	I4	I3	I2	I1	
I7	I7	I6	I5	MBCNDD	I4	I3	I2	
d1	d1	I7	I6	I5	-	I4	I3	
d2	d2	d1	I7	I6	I5	-	I4	
d3	d3	d2	d1	I7	I6	I5	-	
		d3	d2	d1	I7	I6	I5	
			d3	d2	d1	I7	I6	
				d3	d2	d1	I7	
					d3	d2	d1	
						d3	d2	
							d3	

Example 1

```

; if (State == 0.1)
; RampState = RampState || RAMPMASK
; else if (State == 0.01)
; CoastState = CoastState || COASTMASK
; else
; SteadyState = SteadyState || STEADYMASK
;
_Cla1Task1:
    MMOV32 MR0, @State
    MCMPF32 MR0, #0.1           ; Affects flags for 1st MBCNDD (A)
    MNOP
    MNOP
    MNOP
    MBCNDD Skip1, NEQ          ; (A) If State != 0.1, go to Skip1
    MNOP ; Always executed
    MNOP ; Always executed
    MNOP ; Always executed
    MMOV32 MR1, @RampState      ; Execute if (A) branch not taken
    MMOVXI MR2, #RAMPMASK       ; Execute if (A) branch not taken
    MOR32 MR1, MR2              ; Execute if (A) branch not taken
    MMOV32 @RampState, MR1      ; Execute if (A) branch not taken
    MSTOP                         ; end of task if (A) branch not taken
Skip1:
    MCMPF32 MR0,#0.01           ; Affects flags for 2nd MBCNDD (B)
    MNOP
    MNOP
    MNOP
    MBCNDD Skip2,NEQ           ; (B) If State != 0.01, go to Skip2
    MNOP ; Always executed
    MNOP ; Always executed
    MNOP ; Always executed
    MMOV32 MR1, @CoastState     ; Execute if (B) branch not taken
    MMOVXI MR2, #COASTMASK      ; Execute if (B) branch not taken
    MOR32 MR1, MR2              ; Execute if (B) branch not taken
    MMOV32 @CoastState, MR1     ; Execute if (B) branch not taken
    MSTOP
Skip2:
    MMOV32 MR3, @SteadyState   ; Executed if (B) branch taken
    MMOVXI MR2, #STEADYMASK     ; Executed if (B) branch taken
    MOR32 MR3, MR2              ; Executed if (B) branch taken
    MMOV32 @SteadyState, MR3    ; Executed if (B) branch taken
    MSTOP

```

Example 2

```
; This example is the same as Example 1, except
; the code is optimized to take advantage of delay slots
;
; if (State == 0.1)
; RampState = RampState || RAMPMASK
; else if (State == 0.01)
; CoastState = CoastState || COASTMASK
; else
; SteadyState = SteadyState || STEADYMASK
;
_Cla1Task2:
    MMOV32 MR0, @State
    MCMPF32 MR0, #0.1           ; Affects flags for 1st MBCNDD (A)
    MCMPF32 MR0, #0.01          ; Check used by 2nd MBCNDD (B)
    MMTESTTF EQ                 ; Store EQ flag in TF for 2nd MBCNDD (B)
    MNOP
    MBCNDD Skip1, NEQ          ; (A) If State != 0.1, go to Skip1
    MMOV32 MR1, @RampState
    MMOVXI MR2, #RAMPMASK
    MOR32 MR1, MR2              ; Always executed
    MMOV32 @RampState, MR1      ; Execute if (A) branch not taken
    MSTOP                         ; end of task if (A) branch not taken

Skip1:
    MMOV32 MR3, @SteadyState
    MMOVXI MR2, #STEADYMASK
    MOR32 MR3, MR2
    MBCNDD Skip2, NTF          ; (B) if State != .01, go to Skip2
    MMOV32 MR1, @CoastState
    MMOVXI MR2, #COASTMASK
    MOR32 MR1, MR2              ; Always executed
    MMOV32 @CoastState, MR1     ; Execute if (B) branch not taken
    MSTOP                         ; end of task if (B) branch not taken

Skip2:
    MMOV32 @SteadyState, MR3    ; Executed if (B) branch taken
    MSTOP
```

See also

[MCCNDD 16BitDest, CNDF](#)
[MRCNDD CNDF](#)

MCCNDD 16BitDest {, CNDF} Call Conditional Delayed**Operands**

16BitDest	16-bit destination if condition is true
CNDF	Optional condition to be tested

Opcode

LSW: dest dest dest dest
 MSW: 0111 1001 1001 cndf

Description

If the specified condition is true, then store the return address in the RPC field of MSTF and make the call by adding the signed 16BitDest value to the MPC value. Otherwise, continue code execution without making the call. If the address overflows, it wraps around. Therefore a value of "0xFFFF" will put the MPC back to the MCCNDD instruction.

Please refer to the pipeline section for important information regarding this instruction.

```
if (CNDF == TRUE)
{
    RPC = return address;
    MPC += 16BitDest;
};
```

CNDF is one of the following conditions:

Encode ⁽³⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽⁴⁾	Unconditional with flag modification	None

⁽³⁾ Values not shown are reserved.

⁽⁴⁾ This is the default operation if no CNDF field is specified. This condition will allow the ZF and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

Restrictions

The MCCNDD instruction is not allowed three instructions before or after a MBCNDD, MCCNDD, or MRCNDD instruction. Refer to the Pipeline section for more details.

Flags

This instruction does not modify flags in the MSTF register.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

The MCCNDD instruction by itself is a single-cycle instruction. As shown in [Table 4-13](#), for each call 6 instruction slots are executed; three before the call instruction (I2-I4) and three after the call instruction (I5-I7). The total number of cycles for a call taken or not taken depends on the usage of these slots. That is, the number of cycles depends on how many slots are filled with a MNOP as well as which slots are filled. The effective number of cycles for a call can, therefore, range from 1 to 7 cycles. The number of cycles for a call taken may not be the same as for a call not taken.

Referring to the following code fragment and the pipeline diagrams in [Table 4-13](#) and [Table 4-14](#), the instructions before and after MCCNDD have the following properties:

- **I1**
 - I1 is the last instruction that can effect the CNDF flags for the MCCNDD instruction. The CNDF flags are tested in the D2 phase of the pipeline. That is, a decision is made whether to branch or not when MCCNDD is in the D2 phase.
 - There are no restrictions on the type of instruction for I1.
- **I2, I3 and I4**
 - The three instructions proceeding MCCNDD can change MSTF flags but will have no effect on whether the MCCNDD instruction makes the call or not. This is because the flag modification will occur after the D2 phase of the MCCNDD instruction.
 - These instructions must not be the following: MSTOP, MDEBUGSTOP, MBCNDD, MCCNDD or MRCNDD.
- **I5, I6 and I7**
 - The three instructions following MBCNDD are always executed irrespective of whether the branch is taken or not.
 - These instructions must not be the following: MSTOP, MDEBUGSTOP, MBCNDD, MCCNDD or MRCNDD.

```

<Instruction 1> ; I1 Last instruction that can affect flags for
                  ; the MCCNDD operation
<Instruction 2> ; I2 Cannot be stop, branch, call or return
<Instruction 3> ; I3 Cannot be stop, branch, call or return
<Instruction 4> ; I4 Cannot be stop, branch, call or return

MCCNDD _func, NEQ ; Call to func if not equal to zero

                  ; Three instructions after MCCNDD are always
                  ; executed whether the call is taken or not

<Instruction 5> ; I5 Cannot be stop, branch, call or return
<Instruction 6> ; I6 Cannot be stop, branch, call or return
<Instruction 7> ; I7 Cannot be stop, branch, call or return
<Instruction 8> ; I8 The address of this instruction is saved
                  ; in the RPC field of the MSTF register.
                  ; Upon return this value is loaded into MPC
                  ; and fetching continues from this point.
<Instruction 9> ; I9
...._func:
<Destination 1> ; d1 Can be any instruction
<Destination 2> ; d2
<Destination 3> ; d3
<Destination 4> ; d4 Last instruction that can affect flags for
                  ; the MRCNDD operation

<Destination 5> ; d5 Cannot be stop, branch, call or return
<Destination 6> ; d6 Cannot be stop, branch, call or return
<Destination 7> ; d7 Cannot be stop, branch, call or return

MRCNDD UNC      ; Return to <Instruction 8>, unconditional

                  ; Three instructions after MRCNDD are always
                  ; executed whether the return is taken or not

<Destination 8> ; d8 Cannot be stop, branch, call or return
<Destination 9> ; d9 Cannot be stop, branch, call or return
<Destination 10> ; d10 Cannot be stop, branch, call or return
<Destination 11> ; d11
....MSTOP

```

Table 4-13. Pipeline Activity For MCCNDD, Call Not Taken

Instruction	F1	F2	D1	D2	R1	R2	E	W
I1		I1						
I2		I2	I1					
I3		I3	I2	I1				
I4		I4	I3	I2	I1			
MCCNDD	MCCNDD	I4	I3	I2	I1			
I5	I5	MCCNDD	I4	I3	I2	I1		
I6	I6	I5	MCCNDD	I4	I3	I2	I1	
I7	I7	I6	I5	MCCNDD	I4	I3	I2	
I8	I8	I7	I6	I5	-	I4	I3	
I9	I9	I8	I7	I6	I5	-	I4	
I10	I10	I9	I8	I7	I6	I5	-	
etc		I10	I9	I8	I7	I6	I5	
....			I10	I9	I8	I7	I6	
....				I10	I9	I8	I7	
....					I10	I9	I8	
						I10	I9	
							I10	

Table 4-14. Pipeline Activity For MCCNDD, Call Taken

Instruction	F1	F2	D1	D2	R1	R2	E	W
I1		I1						
I2		I2	I1					
I3		I3	I2	I1				
I4		I4	I3	I2	I1			
MCCNDD	MCCNDD	I4	I3	I2	I1			
I5	I5	MCCNDD	I4	I3	I2	I1		
I6	I6	I5	MCCNDD	I4	I3	I2	I1	
I7 ⁽¹⁾	I7	I6	I5	MCCNDD	I4	I3	I2	I1
d1	d1	I7	I6	I5	I4	I3	I2	I1
d2	d2	d1	I7	I6	I5	-	I4	I3
d3	d3	d2	d1	I7	I6	I5	-	I4
etc		d3	d2	d1	I7	I6	I5	
....			d3	d2	d1	I7	I6	
....				d3	d2	d1	I7	
....					d3	d2	d1	
						d3	d2	
							d3	

⁽¹⁾ The RPC value in the MSTF register will point to the instruction following I7 (instruction I8).

Example

;

See also

[MBCNDD #16BitDest, CNDF](#)
[MMOV32 mem32, MSTF](#)
[MMOV32 MSTF, mem32](#)
[MRCNDD CNDF](#)

MCMP32 MRa, MRb 32-Bit Integer Compare for Equal, Less Than or Greater Than**Operands**

MRa	CLA floating-point source register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1111 0010 0000

Description Set ZF and NF flags on the result of MRa - MRb where MRa and MRb are 32-bit integers. For a floating point compare refer to [MCMPF32](#).

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
If(MRa == MRb) {ZF=1; NF=0;}
If(MRa > MRb) {ZF=0; NF=0;}
If(MRa < MRb) {ZF=0; NF=1;}
```

Pipeline

This is a single-cycle instruction.

Example

```
; Behavior of ZF and NF flags for different comparisons
;
; Given A = (int32)1
;       B = (int32)2
;       C = (int32)-7
;
      MMOV32 MR0, @_A ; MR0 = 1 (0x00000001)
      MMOV32 MR1, @_B ; MR1 = 2 (0x00000002)
      MMOV32 MR2, @_C ; MR2 = -7 (0xFFFFFFFF9)
      MCMP32 MR2, MR2 ; NF = 0, ZF = 1
      MCMP32 MR0, MR1 ; NF = 1, ZF = 0
      MCMP32 MR1, MR0 ; NF = 0, ZF = 0
```

See also

[MADD32 MRa, MRb, MRc](#)
[MSUB32 MRa, MRb, MRc](#)

MCMPF32 MRa, MRb 32-Bit Floating-Point Compare for Equal, Less Than or Greater Than

Operands

MRa	CLA floating-point source register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1101 0000 0000

Description

Set ZF and NF flags on the result of MRa - MRb. The MCMPF32 instruction is performed as a logical compare operation. This is possible because of the IEEE format offsetting the exponent. Basically the bigger the binary number, the bigger the floating-point value.

Special cases for inputs:

- Negative zero will be treated as positive zero.
- A denormalized value will be treated as positive zero.
- Not-a-Number (NaN) will be treated as infinity.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified as follows:

```
If(MRa == MRb) {ZF=1; NF=0;}
If(MRa > MRb) {ZF=0; NF=0;}
If(MRa < MRb) {ZF=0; NF=1;}
```

Pipeline

This is a single-cycle instruction.

Example

; Behavior of ZF and NF flags for different comparisons

```
MMOVIZ    MR1, #-2.0 ; MR1 = -2.0 (0xC0000000)
MMOVIZ    MR0, #5.0  ; MR0 = 5.0 (0x40A00000)
MCMPF32   MR1, MR0   ; ZF = 0, NF = 1
MCMPF32   MR0, MR1   ; ZF = 0, NF = 0
MCMPF32   MR0, MR0   ; ZF = 1, NF = 0
```

See also

[MCMPF32 MRa, #16FHi](#)
[MMAXF32 MRa, #16FHi](#)
[MMAXF32 MRa, MRb](#)
[MMINF32 MRa, #16FHi](#)
[MMINF32 MRa, MRb](#)

MCMPF32 MRa, #16FHi 32-Bit Floating-Point Compare for Equal, Less Than or Greater Than**Operands**

MRa	CLA floating-point source register (MRO to MR3)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.

Opcode

LSW: IIII IIII IIII IIII
 MSW: 0111 1000 1100 00aa

Description

Compare the value in MRa with the floating-point value represented by the immediate operand. Set the ZF and NF flags on (MRa - #16FHi:0).

#16FHi is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. This addressing mode is most useful for constants where the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). The assembler will accept either a hex or float as the immediate value. That is, -1.5 can be represented as #-1.5 or #0xBFC0.

The MCMPF32 instruction is performed as a logical compare operation. This is possible because of the IEEE floating-point format offsets the exponent. Basically the bigger the binary number, the bigger the floating-point value.

Special cases for inputs:

- Negative zero will be treated as positive zero.
- Denormalized value will be treated as positive zero.
- Not-a-Number (NaN) will be treated as infinity.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified as follows:

```
If(MRa == #16FHi:0) {ZF=1, NF=0;}
If(MRa > #16FHi:0) {ZF=0, NF=0;}
If(MRa < #16FHi:0) {ZF=0, NF=1;}
```

Pipeline

This is a single-cycle instruction

Example 1

; Behavior of ZF and NF flags for different comparisons

```
MMOVIZ      MR1, #-2.0 ; MR1 = -2.0 (0xC0000000)
MMOVIZ      MR0, #5.0  ; MR0 = 5.0 (0x40A00000)
MCMPF32     MR1, #-2.2 ; ZF = 0, NF = 0
MCMPF32     MR0, #6.5  ; ZF = 0, NF = 1
MCMPF32     MR0, #5.0  ; ZF = 1, NF = 0
```

Example 2

```

; X is an array of 32-bit floating-point values
; and has len elements. Find the maximum value in
; the array and store it in Result
;
; Note: MCMPF32 and MSWAPF can be replaced with MMAXF32
;
_Cla1Task1:
    MMOVI16 MAR1,#_X          ; Start address
    MUI16TOF32 MR0, @_len     ; Length of the array
    MNOP                      ; delay for MAR1 load
    MNOP                      ; delay for MAR1 load
    MMOV32 MR1, *MAR1[2]++    ; MR1 = X0

    LOOP
        MMOV32 MR2, *MAR1[2]++ ; MR2 = next element
        MCMPF32 MR2, MR1       ; Compare MR2 with MR1
        MSWAPF MR1, MR2, GT    ; MR1 = MAX(MR1, MR2)
        MADDF32 MR0, MR0, #-1.0 ; Decrement the counter
        MCMPF32 MR0 #0.0        ; Set/clear flags for MBCNDD
        MNOP
        MNOP
        MNOP
        MBCNDD LOOP, NEQ        ; Branch if not equal to zero
        MMOV32 @_Result, MR1    ; Always executed
        MNOP                      ; Always executed
        MNOP                      ; Always executed
        MSTOP                     ; End of task

```

See also

[MCMPF32 MRa, MRb](#)
[MMAXF32 MRa, #16FHi](#)
[MMAXF32 MRa, MRb](#)
[MMINF32 MRa, #16FHi](#)
[MMINF32 MRa, MRb](#)

MDEBUGSTOP***Debug Stop Task*****Operands**

none	This instruction does not have any operands
------	---

Opcode

LSW: 0000 0000 0000 0000
MSW: 0111 1111 0110 0000

Description

When CLA breakpoints are enabled, the MDEBUGSTOP instruction is used to halt a task so that it can be debugged. That is, MDEBUGSTOP is the CLA breakpoint. If CLA breakpoints are not enabled, the MDEBUGSTOP instruction behaves like a MNOP. Unlike the MSTOP, the MIRUN flag is not cleared and an interrupt is not issued. A single-step or run operation will continue execution of the task.

Restrictions

The MDEBUGSTOP instruction cannot be placed 3 instructions before or after a [MBCNDD](#), [MCCNDD](#) or [MRCNDD](#) instruction.

Flags

This instruction does not modify flags in the MSTF register.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

;

See also

[MSTOP](#)

MEALLOW**Enable CLA Write Access to EALLOW Protected Registers****Operands**

none	This instruction does not have any operands
------	---

Opcode

LSW: 0000 0000 0000 0000
MSW: 0111 1111 1001 0000

Description

This instruction sets the MEALLOW bit in the CLA status register MSTF. When this bit is set, the CLA is allowed write access to EALLOW protected registers. To again protect against CLA writes to protected registers, use the MEDIS instruction.

MEALLOW and MEDIS only control CLA write access; reads are allowed even if MEALLOW has not been executed. MEALLOW and MEDIS are also independent from the main CPU's EALLOW/EDIS. This instruction does not modify the EALLOW bit in the main CPU's status register. The MEALLOW bit in MSTF only controls access for the CLA while the EALLOW bit in the ST1 register only controls access for the main CPU.

As with EALLOW, the MEALLOW bit is overridden via the JTAG port, allowing full control of register accesses during debug from Code Composer Studio.

Flags

This instruction does not modify flags in the MSTF register.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; C header file including definition of
; the EPwm1Regs structure
;
; The ePWM TZSEL register is EALLOW protected
;
.cdecls C,LIST,"CLAShared.h"
...
_Cla1Task1:
...
    MEALLOW                                ; Allow CLA write access
    MMOV16 @_EPwm1Regs.TZSEL.all, MR3      ; Write to TZSEL
    MEDIS                                   ; Disallow CLA write access
...
...
MSTOP
```

See also

[MEDIS](#)

MEDIS***Disable CLA Write Access to EALLOW Protected Registers*****Operands**

none	This instruction does not have any operands
------	---

Opcode

LSW: 0000 0000 0000 0000
 MSW: 0111 1111 1011 0000

Description

This instruction clears the MEALLOW bit in the CLA status register MSTF. When this bit is clear, the CLA is not allowed write access to EALLOW-protected registers. To enable CLA writes to protected registers, use the MEALLOW instruction.

MEALLOW and MEDIS only control CLA write access; reads are allowed even if MEALLOW has not been executed. MEALLOW and MEDIS are also independent from the main CPU's EALLOW/EDIS. This instruction does not modify the EALLOW bit in the main CPU's status register. The MEALLOW bit in MSTF only controls access for the CLA while the EALLOW bit in the ST1 register only controls access for the main CPU.

As with EALLOW, the MEALLOW bit is overridden via the JTAG port, allowing full control of register accesses during debug from Code Composer Studio.

Flags

This instruction does not modify flags in the MSTF register.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; C header file including definition of
; the EPwm1Regs structure
;
; The ePWM TZSEL register is EALLOW protected
;
.cdecls C,LIST,"CLAShared.h"
...
_Cla1Task1:
...
    MEALLOW                                ; Allow CLA write access
    MMOV16 @_EPwm1Regs.TZSEL.all, MR3      ; Write to TZSEL
    MEDIS                                  ; Disallow CLA write access
...
...
MSTOP
```

See also

[MEALLOW](#)

MEINVF32 MRa, MRb 32-Bit Floating-Point Reciprocal Approximation

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1111 0000 0000

Description

This operation generates an estimate of 1/X in 32-bit floating-point format accurate to approximately 8 bits. This value can be used in a Newton-Raphson algorithm to get a more accurate answer. That is:

```
Ye = Estimate(1/X);
Ye = Ye*(2.0 - Ye*X);
Ye = Ye*(2.0 - Ye*X);
```

After two iterations of the Newton-Raphson algorithm, you will get an exact answer accurate to the 32-bit floating-point format. On each iteration the mantissa bit accuracy approximately doubles. The MEINVF32 operation will not generate a negative zero, DeNorm or NaN value.

MRa = Estimate of 1/MRb;

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MEINVF32 generates an underflow condition.
- LVF = 1 if MEINVF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example

```
; Calculate Num/Den using a Newton-Raphson algorithm for 1/Den
; Ye = Estimate(1/X)
; Ye = Ye*(2.0 - Ye*X)
; Ye = Ye*(2.0 - Ye*X)
;
_Cla1Task1:
    MMOV32 MR1, @_Den      ; MR1 = Den
    MEINVF32 MR2, MR1       ; MR2 = Ye = Estimate(1/Den)
    MMPYF32 MR3, MR2, MR1   ; MR3 = Ye*Den
    MSUBF32 MR3, #2.0, MR3 ; MR3 = 2.0 - Ye*Den
    MMPYF32 MR2, MR2, MR3   ; MR2 = Ye = Ye*(2.0 - Ye*Den)
    MMPYF32 MR3, MR2, MR1   ; MR3 = Ye*Den
    || MMOV32 MR0, @_Num     ; MR0 = Num
    MSUBF32 MR3, #2.0, MR3 ; MR3 = 2.0 - Ye*Den
    MMPYF32 MR2, MR2, MR3   ; MR2 = Ye = Ye*(2.0 - Ye*Den)
    || MMOV32 MR1, @_Den     ; Reload Den To Set Sign
    MNEGF32 MR0, MR0, EQ    ; if(Den == 0.0) Change Sign Of Num
    MMPYF32 MR0, MR2, MR0    ; MR0 = Y = Ye*Num
    MMOV32 @_Dest, MR0       ; Store result
    MSTOP                   ; end of task
```

See also

[MEISQRTF32 MRa, MRb](#)

MEISQRTF32 MRa, MRb 32-Bit Floating-Point Square-Root Reciprocal Approximation**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1110 0100 0000

Description

This operation generates an estimate of $1/\sqrt{X}$ in 32-bit floating-point format accurate to approximately 8 bits. This value can be used in a Newton-Raphson algorithm to get a more accurate answer. That is:

```
Ye = Estimate(1/sqrt(X));
Ye = Ye*(1.5 - Ye*Ye*X/2.0);
Ye = Ye*(1.5 - Ye*Ye*X/2.0);
```

After 2 iterations of the Newton-Raphson algorithm, you will get an exact answer accurate to the 32-bit floating-point format. On each iteration the mantissa bit accuracy approximately doubles. The MEISQRTF32 operation will not generate a negative zero, DeNorm or NaN value.

MRa = Estimate of $1/\sqrt{X}$ (MRb);

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MEISQRTF32 generates an underflow condition.
- LVF = 1 if MEISQRTF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example

```
; Y = sqrt(X)
; Ye = Estimate(1/sqrt(X));
; Ye = Ye*(1.5 - Ye*Ye*X*0.5)
; Ye = Ye*(1.5 - Ye*Ye*X*0.5)
; Y = X*Ye
;
_Cla1Task3:
  MMOV32 MR0, @_x          ; MR0 = X
  MEISQRTF32 MR1, MR0      ; MR1 = Ye = Estimate(1/sqrt(X))
  MMOV32 MR1, @_x, EQ      ; if(X == 0.0) Ye = 0.0
  MMPYF32 MR3, MR0, #0.5   ; MR3 = X*0.5
  MMPYF32 MR2, MR1, MR3   ; MR2 = Ye*X*0.5
  MMPYF32 MR2, MR1, MR2   ; MR2 = Ye*Ye*X*0.5
  MSUBF32 MR2, #1.5, MR2   ; MR2 = 1.5 - Ye*Ye*X*0.5
  MMPYF32 MR1, MR1, MR2   ; MR1 = Ye = Ye*(1.5 - Ye*Ye*X*0.5)
  MMPYF32 MR2, MR1, MR3   ; MR2 = Ye*X*0.5
  MMPYF32 MR2, MR1, MR2   ; MR2 = Ye*Ye*X*0.5
  MSUBF32 MR2, #1.5, MR2   ; MR2 = 1.5 - Ye*Ye*X*0.5
  MMPYF32 MR1, MR1, MR2   ; MR1 = Ye = Ye*(1.5 - Ye*Ye*X*0.5)
  MMPYF32 MR0, MR1, MR0   ; MR0 = Y = Ye*X
  MMOV32 @_y, MR0          ; Store Y = sqrt(X)
  MSTOP                   ; end of task
```

See also

[MEINVF32 MRa, MRb](#)

MF32TOI16 MRa, MRb Convert 32-Bit Floating-Point Value to 16-Bit Integer

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1101 1110 0000

Description

Convert a 32-bit floating point value in MRb to a 16-bit integer and truncate. The result will be stored in MRa.

```
MRa(15:0) = F32TOI16(MRb);
MRa(31:16) = sign extension of MRa(15);
```

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ      MR0, #5.0      ; MR0          = 5.0 (0x40A00000)
MF32TOI16   MR1, MR0      ; MR1(15:0)    = MF32TOI16(MR0) = 0x0005
              ; MR1(31:16)   = Sign extension of MR1(15) = 0x0000
MMOVIZ      MR2, #-5.0     ; MR2          = -5.0 (0xC0A00000)
MF32TOI16   MR3, MR2      ; MR3(15:0)    = MF32TOI16(MR2) = -5 (0xFFFF)
              ; MR3(31:16)   = Sign extension of MR3(15) = 0xFFFF
```

See also

[MF32TOI16R MRa, MRb](#)
[MF32TOUI16 MRa, MRb](#)
[MF32TOUI16R MRa, MRb](#)
[MI16TOF32 MRa, MRb](#)
[MI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, MRb](#)

MF32TOI16R MRa, MRb Convert 32-Bit Floating-Point Value to 16-Bit Integer and Round**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1110 0110 0000

Description

Convert the 32-bit floating point value in MRb to a 16-bit integer and round to the nearest even value. The result is stored in MRa.

```
MRa(15:0) = F32TOI16round(MRb);
MRa(31:16) = sign extension of MRa(15);
```

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ MR0, #0x3FD9 ; MR0(31:16) = 0x3FD9
MMOVXI MR0, #0x999A ; MR0(15:0) = 0x999A
; MR0 = 1.7 (0x3FD9999A)
MF32TOI16R MR1, MR0 ; MR1(15:0) = MF32TOI16round (MR0) = 2 (0x0002)
; MR1(31:16) = Sign extension of MR1(15) = 0x0000
MMOVF32 MR2, #-1.7 ; MR2 = -1.7 (0xBFD9999A)
MF32TOI16R MR3, MR2 ; MR3(15:0) = MF32TOI16round (MR2) = -2 (0xFFFF)
; MR3(31:16) = Sign extension of MR2(15) = 0xFFFF
```

See also

[MF32TOI16 MRa, MRb](#)
[MF32TOUI16 MRa, MRb](#)
[MF32TOUI16R MRa, MRb](#)
[MI16TOF32 MRa, MRb](#)
[MI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, MRb](#)

MF32TOI32 MRa, MRb Convert 32-Bit Floating-Point Value to 32-Bit Integer**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1101 0110 0000

Description Convert the 32-bit floating-point value in MRb to a 32-bit integer value and truncate.
 Store the result in MRa.

MRa = F32TOI32(MRb);

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example 1

```
MMOVF32    MR2, #11204005.0 ; MR2 = 11204005.0 (0x4B2AF5A5)
MF32TOI32  MR3, MR2        ; MR3 = MF32TOI32(MR2) = 11204005 (0x00AAF5A5)
MMOVF32    MR0, #-11204005.0; MR0 = -11204005.0 (0xCB2AF5A5)
MF32TOI32  MR1, MR0        ; MR1 = MF32TOI32(MR0) = -11204005 (0xFF550A5B)
```

Example 2

```
; Given X, M and B are IQ24 numbers:
; X = IQ24(+2.5) = 0x02800000
; M = IQ24(+1.5) = 0x01800000
; B = IQ24(-0.5) = 0xFF800000
;
; Calculate Y = X * M + B
;
; Convert M, X and B from IQ24 to float
;
_ClalTask2:
  MI32TOF32 MR0, @_M          ; MR0 = 0x4BC00000
  MI32TOF32 MR1, @_X          ; MR1 = 0x4C200000
  MI32TOF32 MR2, @_B          ; MR2 = 0xCB000000
  MMPYF32   MR0, MR0, #0x3380 ; M = 1/(1*2^24) * iqm = 1.5 (0x3FC00000)
  MMPYF32   MR1, MR1, #0x3380 ; X = 1/(1*2^24) * iqx = 2.5 (0x40200000)
  MMPYF32   MR2, MR2, #0x3380 ; B = 1/(1*2^24) * iqb = -.5 (0xBF000000)
  MMPYF32   MR3, MR0, MR1     ; M*X
  MADDF32   MR2, MR2, MR3     ; Y=MX+B = 3.25 (0x40500000)

; Convert Y from float32 to IQ24
  MMPYF32 MR2, MR2, #0x4B80   ; Y * 1*2^24
  MF32TOI32 MR2, MR2          ; IQ24(Y) = 0x03400000
  MMOV32 @_Y, MR2             ; store result
  MSTOP                      ; end of task
```

See also

[MF32TOUI32 MRa, MRb](#)
[MI32TOF32 MRa, MRb](#)
[MI32TOF32 MRa, mem32](#)
[MUI32TOF32 MRa, MRb](#)
[MUI32TOF32 MRa, mem32](#)

MF32TOUI16 MRa, MRb Convert 32-Bit Floating-Point Value to 16-bit Unsigned Integer**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1110 1010 0000

Description

Convert the 32-bit floating point value in MRb to an unsigned 16-bit integer value and truncate to zero. The result will be stored in MRa. To instead round the integer to the nearest even value use the MF32TOUI16R instruction.

MRa(15:0) = F32TOUI16(MRb);
 MRa(31:16) = 0x0000;

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```

MMOVIZ      MR0, #9.0      ; MR0 = 9.0 (0x41100000)
MF32TOUI16  MR1, MR0      ; MR1(15:0) = MF32TOUI16(MR0) = 9 (0x0009)
                  ; MR1(31:16) = 0x0000
MMOVIZ      MR2, #-9.0     ; MR2 = -9.0 (0xC1100000)
MF32TOUI16  MR3, MR2      ; MR3(15:0) = MF32TOUI16(MR2) = 0 (0x0000)
                  ; MR3(31:16) = 0x0000

```

See also

[MF32TOI16 MRa, MRb](#)
[MF32TOUI16 MRa, MRb](#)
[MF32TOUI16R MRa, MRb](#)
[MI16TOF32 MRa, MRb](#)
[MI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, MRb](#)

MF32TOUI16R MRa, MRb Convert 32-Bit Floating-Point Value to 16-bit Unsigned Integer and Round

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1110 1100 0000

Description

Convert the 32-bit floating-point value in MRb to an unsigned 16-bit integer and round to the closest even value. The result will be stored in MRa. To instead truncate the converted value, use the MF32TOUI16 instruction.

```
MRa(15:0) = MF32TOUI16round(MRb);
MRa(31:16) = 0x0000;
```

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ      MR0, #0x412C      ; MR0 = 0x412C
MMOVXI      MR0, #0xCCCCD     ; MR0 = 0xCCCCD ; MR0 = 10.8 (0x412CCCCD)
MF32TOUI16R MR1, MR0        ; MR1(15:0) = MF32TOUI16round(MR0) = 11 (0x000B)
                           ; MR1(31:16) = 0x0000
MMOVF32     MR2, #-10.8       ; MR2 = -10.8 (0x0xC12CCCCD)
MF32TOUI16R MR3, MR2        ; MR3(15:0) = MF32TOUI16round(MR2) = 0 (0x0000)
                           ; MR3(31:16) = 0x0000
```

See also

[MF32TOI16 MRa, MRb](#)
[MF32TOI16R MRa, MRb](#)
[MF32TOUI16 MRa, MRb](#)
[MI16TOF32 MRa, MRb](#)
[MI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, MRb](#)

MF32TOUI32 MRa, MRb Convert 32-Bit Floating-Point Value to 32-Bit Unsigned Integer**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1101 1010 0000

Description Convert the 32-bit floating-point value in MRb to an unsigned 32-bit integer and store the result in MRa.

MRa = F32TOUI32(MRb);

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```

MMOVIZ      MRO, #12.5    ; MRO = 12.5 (0x41480000)
MF32TOUI32  MRO, MRO     ; MRO = MF32TOUI32 (MRO) = 12 (0x0000000C)
MMOVIZ      MR1, #-6.5    ; MR1 = -6.5 (0xC0D00000)
MF32TOUI32  MR2, MR1     ; MR2 = MF32TOUI32 (MR1) = 0.0 (0x00000000)
  
```

See also

[MF32TOI32 MRa, MRb](#)
[MI32TOF32 MRa, MRb](#)
[MI32TOF32 MRa, mem32](#)
[MUI32TOF32 MRa, MRb](#)
[MUI32TOF32 MRa, mem32](#)

MFRACF32 MRa, MRb *Fractional Portion of a 32-Bit Floating-Point Value*

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1110 0000 0000

Description

Returns in MRa the fractional portion of the 32-bit floating-point value in MRb

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ      MR2, #19.625 ; MR2 = 19.625 (0x419D0000)
MFRACF32   MR3, MR2      ; MR3 = MFRACF32(MR2) = 0.625 (0x3F200000)0
```

See also

MI16TOF32 MRa, MRb Convert 16-Bit Integer to 32-Bit Floating-Point Value**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1110 1000 0000

Description

Convert the 16-bit signed integer in MRb to a 32-bit floating point value and store the result in MRa.

MRa = MI16TOF32(MRb);

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```

MMOVIZ      MRO, #0x0000      ; MRO(31:16) = 0.0 (0x0000)
MMOVXI      MRO, #0x0004      ; MRO(15:0) = 4.0 (0x0004)
MI16TOF32   MR1, MRO         ; MR1 = MI16TOF32 (MRO) = 4.0 (0x40800000)

MMOVIZ      MR2, #0x0000      ; MR2(31:16) = 0.0 (0x0000)
MMOVXI      MR2, #0xFFFFC     ; MR2(15:0) = -4.0 (0xFFFFC)
MI16TOF32   MR3, MR2         ; MR3 = MI16TOF32 (MR2) = -4.0 (0xC0800000)
MSTOP
  
```

See also

[MF32TOI16 MRa, MRb](#)
[MF32TOI16R MRa, MRb](#)
[MF32TOUI16 MRa, MRb](#)
[MF32TOUI16R MRa, MRb](#)
[MI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, MRb](#)

MI16TOF32 MRa, mem16 Convert 16-Bit Integer to 32-Bit Floating-Point Value

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
mem16	16-bit source memory location to be converted

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0101 00aa addr

Description

Convert the 16-bit signed integer indicated by the mem16 pointer to a 32-bit floating-point value and store the result in MRa.

MRa = MI16TOF32[mem16];

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction:

Example

```
; Assume A = 4 (0x0004)
;           B = -4 (0xFFFFC)
```

```
MI16TOF32 MR0, @_A ; MR0 = MI16TOF32(A) = 4.0 (0x40800000)
MI16TOF32 MR1, @_B ; MR1 = MI16TOF32(B) = -4.0 (0xC0800000)
```

See also

[MF32TOI16 MRa, MRb](#)
[MF32TOI16R MRa, MRb](#)
[MF32TOUI16 MRa, MRb](#)
[MF32TOUI16R MRa, MRb](#)
[MI16TOF32 MRa, MRb](#)
[MUI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, MRb](#)

MI32TOF32 MRa, mem32 Convert 32-Bit Integer to 32-Bit Floating-Point Value**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
mem32	32-bit memory source for the MMOV32 operation.

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0100 01aa addr

Description

Convert the 32-bit signed integer indicated by mem32 to a 32-bit floating point value and store the result in MRa.

MRa = MI32TOF32[mem32];

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; Given X, M and B are IQ24 numbers:  

; X = IQ24(+2.5) = 0x02800000  

; M = IQ24(+1.5) = 0x01800000  

; B = IQ24(-0.5) = 0xFF800000  

;  

; Calculate Y = X * M + B  

;  

; Convert M, X and B from IQ24 to float  

;  

_Cla1Task3:  

  MI32TOF32 MR0, @_M          ; MR0 = 0x4BC00000  

  MI32TOF32 MR1, @_X          ; MR1 = 0x4C200000  

  MI32TOF32 MR2, @_B          ; MR2 = 0xCB000000  

  MMPYF32 MR0, MR0, #0x3380   ; M = 1/(1*2^24) * iqm = 1.5 (0x3FC00000)  

  MMPYF32 MR1, MR1, #0x3380   ; X = 1/(1*2^24) * iqx = 2.5 (0x40200000)  

  MMPYF32 MR2, MR2, #0x3380   ; B = 1/(1*2^24) * iqb = -.5 (0xBF000000)  

  MMPYF32 MR3, MR0, MR1       ; M*X  

  MADDF32 MR2, MR2, MR3       ; Y=MX+B = 3.25 (0x40500000)  

;  

; Convert Y from float32 to IQ24  

  MMPYF32 MR2, MR2, #0x4B80   ; Y * 1*2^24  

  MF32TOI32 MR2, MR2          ; IQ24(Y) = 0x03400000  

  MMOV32 @_Y, MR2             ; store result  

  MSTOP                      ; end of task
```

See also

[MF32TOI32 MRa, MRb](#)
[MF32TOU132 MRa, MRb](#)
[MI32TOF32 MRa, MRb](#)
[MUI32TOF32 MRa, MRb](#)
[MUI32TOF32 MRa, mem32](#)

MI32TOF32 MRa, MRb Convert 32-Bit Integer to 32-Bit Floating-Point Value

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1101 1000 0000

Description

Convert the signed 32-bit integer in MRb to a 32-bit floating-point value and store the result in MRa.

MRa = MI32TOF32(MRb);

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; Example1:  

;  

    MMOVIZ      MR2, #0x1111 ; MR2(31:16) = 4369 (0x1111)  

    MMOVXI      MR2, #0x1111 ; MR2(15:0) = 4369 (0x1111)  

                ; MR2 = +286331153 (0x11111111)  

    MI32TOF32  MR3, MR2      ; MR3 = MI32TOF32 (MR2) = 286331153.0 (0x4D888888)
```

See also

[MF32TOI32 MRa, MRb](#)
[MF32TOU132 MRa, MRb](#)
[MI32TOF32 MRa, mem32](#)
[MUI32TOF32 MRa, MRb](#)
[MUI32TOF32 MRa, mem32](#)

MLSL32 MRa, #SHIFT Logical Shift Left**Operands**

MRa	CLA floating-point source/destination register (MR0 to MR3)
#SHIFT	Number of bits to shift (1 to 32)

Opcode

LSW: 0000 0000 0shi ftaa
 MSW: 0111 1011 1100 0000

Description

Logical shift left of MRa by the number of bits indicated. The number of bits can be 1 to 32.

```
MRa(31:0) = Logical Shift Left(MRa(31:0) by #SHIFT bits);
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
NF = MRa(31);
ZF = 0;
if(MRa(31:0) == 0) { ZF = 1; }
```

Pipeline

This is a single-cycle instruction.

Example

```
; Given m2 = (int32)32
;           x2 = (int32)64
;           b2 = (int32)-128
;
; Calculate:
;           m2 = m2*2
;           x2 = x2*4
;           b2 = b2*8
;
_Cla1Task3:
    MMOV32 MR0, @_m2      ; MR0 = 32 (0x00000020)
    MMOV32 MR1, @_x2      ; MR1 = 64 (0x00000040)
    MMOV32 MR2, @_b2      ; MR2 = -128 (0xFFFFFFF80)
    MLSL32 MR0, #1        ; MR0 = 64 (0x00000040)
    MLSL32 MR1, #2        ; MR1 = 256 (0x00000100)
    MLSL32 MR2, #3        ; MR2 = -1024 (0xFFFFFC00)
    MMOV32 @_m2, MR0      ; Store results
    MMOV32 @_x2, MR1
    MMOV32 @_b2, MR2
    MSTOP                  ; end of task
```

See also

[MADD32 MRa, MRb, MRc](#)
[MASR32 MRa, #SHIFT](#)
[MAND32 MRa, MRb, MRc](#)
[MLSR32 MRa, #SHIFT](#)
[MOR32 MRa, MRb, MRc](#)
[MXOR32 MRa, MRb, MRc](#)
[MSUB32 MRa, MRb, MRc](#)

MLSR32 MRa, #SHIFT Logical Shift Right**Operands**

MRa	CLA floating-point source/destination register (MR0 to MR3)
#SHIFT	Number of bits to shift (1 to 32)

Opcode

LSW: 0000 0000 0shi ftaa
 MSW: 0111 1011 1000 0000

Description

Logical shift right of MRa by the number of bits indicated. The number of bits can be 1 to 32. Unlike the arithmetic shift (MASR32), the logical shift does not preserve the number's sign bit. Every bit in the operand is moved the specified number of bit positions, and the vacant bit-positions are filled in with zeros

MARa(31:0) = Logical Shift Right(MARa(31:0) by #SHIFT bits);

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
NF = MARa(31);
ZF = 0;
if(MARa(31:0) == 0) { ZF = 1; }
```

Pipeline

This is a single-cycle instruction.

Example

```
; Illustrate the difference between MASR32 and MLSR32

MMOVIZ MR0, #0xAAAA      ; MR0 = 0xAAAA5555
MMOVXI MR0, #0x5555

MMOV32 MR1, MR0          ; MR1 = 0xAAAA5555
MMOV32 MR2, MR0          ; MR2 = 0xAAAA5555

MASR32 MR1, #1           ; MR1 = 0xD5552AAA
MLSR32 MR2, #1           ; MR2 = 0x55552AAA

MASR32 MR1, #1           ; MR1 = 0xEAAA9555
MLSR32 MR2, #1           ; MR2 = 0x2AAA9555

MASR32 MR1, #6           ; MR1 = 0xFFAAAA55
MLSR32 MR2, #6           ; MR2 = 0x00AAAA55
```

See also

[MADD32 MRa, MRb, MRc](#)
[MASR32 MRa, #SHIFT](#)
[MAND32 MRa, MRb, MRc](#)
[MLSL32 MRa, #SHIFT](#)
[MOR32 MRa, MRb, MRc](#)
[MXOR32 MRa, MRb, MRc](#)
[MSUB32 MRa, MRb, MRc](#)

MMACF32 MR3, MR2, MRd, MRe, MRf ||MMOV32 MRa, mem32 32-Bit Floating-Point Multiply and Accumulate with Parallel Move

Operands

MR3	floating-point destination/source register MR3 for the add operation
MR2	CLA floating-point source register MR2 for the add operation
MRd	CLA floating-point destination register (MR0 to MR3) for the multiply operation MRd cannot be the same register as MRa
MRe	CLA floating-point source register (MR0 to MR3) for the multiply operation
MRf	CLA floating-point source register (MR0 to MR3) for the multiply operation
MRa	CLA floating-point destination register for the MMOV32 operation (MR0 to MR3). MRa cannot be MR3 or the same register as MRd.
mem32	32-bit source for the MMOV32 operation

Opcode

LSW: mmmm mmmm mmmm mmmm
MSW: 0011 ffee ddaa addr

Description

Multiply and accumulate the contents of floating-point registers and move from register to memory. The destination register for the MMOV32 cannot be the same as the destination registers for the MMACF32.

```
MR3 = MR3 + MR2;
MRd = MRe * MRf;
MRa = [mem32];
```

Restrictions

The destination registers for the MMACF32 and the MMOV32 must be unique. That is, MRa cannot be MR3 and MRa cannot be the same register as MRd.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MMACF32 (add or multiply) generates an underflow condition.
- LVF = 1 if MMACF32 (add or multiply) generates an overflow condition.

MMOV32 sets the NF and ZF flags as follows:

```
NF = MRa(31);
ZF = 0;
if(MRa(30:23) == 0) { ZF = 1; NF = 0; }
```

Pipeline

MMACF32 and MMOV32 complete in a single cycle.

Example 1

```

; Perform 5 multiply and accumulate operations:
;
; X and Y are 32-bit floating point arrays
;
; 1st multiply: A = X0 * Y0
; 2nd multiply: B = X1 * Y1
; 3rd multiply: C = X2 * Y2
; 4th multiply: D = X3 * Y3
; 5th multiply: E = X3 * Y3
;
; Result = A + B + C + D + E
;
_Cla1Task1:
    MMOV16 MAR0, #_X           ; MAR0 points to X array
    MMOV16 MAR1, #_Y           ; MAR1 points to Y array
    MNOP                      ; Delay for MAR0, MAR1 load
    MNOP                      ; Delay for MAR0, MAR1 load
    ; <-- MAR0 valid
    MMOV32 MR0, *MAR0[2]++     ; MR0 = X0, MAR0 += 2
    ; <-- MAR1 valid
    MMOV32 MR1, *MAR1[2]++     ; MR1 = Y0, MAR1 += 2

    MMPYF32 MR2, MR0, MR1      ; MR2 = A = X0 * Y0
|| MMOV32 MR0, *MAR0[2]++      ; In parallel MR0 = X1, MAR0 += 2
|| MMOV32 MR1, *MAR1[2]++      ; MR1 = Y1, MAR1 += 2

    MMPYF32 MR3, MR0, MR1      ; MR3 = B = X1 * Y1
|| MMOV32 MR0, *MAR0[2]++      ; In parallel MR0 = X2, MAR0 += 2
|| MMOV32 MR1, *MAR1[2]++      ; MR1 = Y2, MAR2 += 2

    MMACF32 MR3, MR2, MR2, MR0, MR1 ; MR3 = A + B, MR2 = C = X2 * Y2
|| MMOV32 MR0, *MAR0[2]++      ; In parallel MR0 = X3
|| MMOV32 MR1, *MAR1[2]++      ; MR1 = Y3 M

    MACF32 MR3, MR2, MR2, MR0, MR1 ; MR3 = (A + B) + C, MR2 = D = X3 * Y3
|| MMOV32 MR0, *MAR0[2]++      ; In parallel MR0 = X4
|| MMOV32 MR1, *MAR1[2]++      ; MR1 = Y4

    MMPYF32 MR2, MR0, MR1      ; MR2 = E = X4 * Y4
|| MADDF32 MR3, MR3, MR2      ; in parallel MR3 = (A + B + C) + D

    MADDF32 MR3, MR3, MR2      ; MR3 = (A + B + C + D) + E
    MMOV32 @_Result, MR3       ; Store the result
    MSTOP                      ; end of task

```

Example 2

```

; sum = X0*B0 + X1*B1 + X2*B2 + Y1*A1 + Y2*B2
;
;      X2 = X1
;      X1 = X0
;      Y2 = Y1 ; Y1 = sum
;
_ClaTask2:
    MMOV32     MR0, @_B2          ; MR0 = B2
    MMOV32     MR1, @_X2          ; MR1 = X2
    MMPYF32    MR2, MR1, MR0    ; MR2 = X2*B2
|| MMOV32    MR0, @_B1          ; MR0 = B1
    MMOVD32   MR1, @_X1          ; MR1 = X1, X2 = X1
    MMPYF32    MR3, MR1, MR0    ; MR3 = X1*B1
|| MMOV32    MR0, @_B0          ; MR0 = B0
    MMOVD32   MR1, @_X0          ; MR1 = X0, X1 = X0

; MR3 = X1*B1 + X2*B2, MR2 = X0*B0
; MR0 = A2
    MMACF32  MR3, MR2, MR2, MR1, MR0
|| MMOV32  MR0, @_A2 M

    MOV32  MR1, @_Y2            ; MR1 = Y2

; MR3 = X0*B0 + X1*B1 + X2*B2, MR2 = Y2*A2
; MR0 = A1
    MMACF32  MR3, MR2, MR2, MR1, MR0
|| MMOV32  MR0, @_A1

    MMOVD32 MR1,@_Y1            ; MR1 = Y1, Y2 = Y1
    MADDF32  MR3, MR3, MR2      ; MR3 = Y2*A2 + X0*B0 + X1*B1 + X2*B2
|| MMPYF32  MR2, MR1, MR0      ; MR2 = Y1*A1
    MADDF32  MR3, MR3, MR2      ; MR3 = Y1*A1 + Y2*A2 + X0*B0 + X1*B1 + X2*B2
    MMOV32 @_Y1, MR3            ; Y1 = MR3
    MSTOP                         ; end of task

```

See also
[MMPYF32 MRa, MRb, MRc || MADDF32 MRd, MRe, MRf](#)

MMAXF32 MRa, MRb 32-Bit Floating-Point Maximum

Operands

MRa	CLA floating-point source/destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1101 0010 0000

Description

`if(MRa < MRb) MRa = MRb;`

Special cases for the output from the MMAXF32 operation:

- NaN output will be converted to infinity
- A denormalized output will be converted to positive zero.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The ZF and NF flags are configured on the result of the operation, not the result stored in the destination register.

```
if(MRa == MRb) {ZF=1; NF=0;}
if(MRa > MRb) {ZF=0; NF=0;}
if(MRa < MRb) {ZF=0; NF=1;}
```

Pipeline

This is a single-cycle instruction.

Example 1

```
MMOVIZ  MR0, #5.0 ; MR0 = 5.0 (0x40A00000)
MMOVIZ  MR1, #-2.0 ; MR1 = -2.0 (0xC0000000)
MMOVIZ  MR2, #-1.5 ; MR2 = -1.5 (0xBFC00000)
MMAXF32  MR2, MR1 ; MR2 = -1.5, ZF = NF = 0
MMAXF32  MR1, MR2 ; MR1 = -1.5, ZF = 0, NF = 1
MMAXF32  MR2, MR0 ; MR2 = 5.0, ZF = 0, NF = 1
MAXF32  MR0, MR2 ; MR2 = 5.0, ZF = 1, NF = 0
```

Example 2

```
; X is an array of 32-bit floating-point values
; Find the maximum value in an array X
; and store it in Result
;
_Cla1Task1:
    MMOV16    MAR1,#_X          ; Start address
    MUI16TOF32 MR0, @_len       ; Length of the array
    MNOP
    MNOP
    MMOV32    MR1, *MAR1[2]++   ; MR1 = X0
LOOP
    MMOV32    MR2, *MAR1[2]++   ; MR2 = next element
    MMAXF32  MR1, MR2          ; MR1 = MAX(MR1, MR2)
    MADDF32  MR0, MR0, #-1.0   ; Decrement the counter
    MCMPF32  MR0 #0.0          ; Set/clear flags for MBCNDD
    MNOP
    MNOP
    MNOP
    MBCNDD    LOOP, NEQ         ; Branch if not equal to zero
    MMOV32    @_Result, MR1     ; Always executed
    MNOP
    MNOP
    MNOP
    MSTOP
```

See also

[MCMPF32 MRa, MRb](#)
[MCMPF32 MRa, #16FH](#)
[MMAXF32 MRa, #16FH](#)

MMINF32 MRa, MRb
MMINF32 MRa, #16FHi

MMAXF32 MRa, #16FHi 32-Bit Floating-Point Maximum

Operands

MRa	CLA floating-point source/destination register (MR0 to MR3)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.

Opcode

LSW: IIII IIII IIII IIII
 MSW: 0111 1001 0000 00aa

Description

Compare MRa with the floating-point value represented by the immediate operand. If the immediate value is larger, then load it into MRa.

```
if(MRa < #16FHi:0) MRa = #16FHi:0;
```

#16FHi is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. This addressing mode is most useful for constants where the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). The assembler will accept either a hex or float as the immediate value. That is, -1.5 can be represented as #-1.5 or #0xBFC0.

Special cases for the output from the MMAXF32 operation:

- NaN output will be converted to infinity
- A denormalized output will be converted to positive zero.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The ZF and NF flags are configured on the result of the operation, not the result stored in the destination register.

```
if(MRa == #16FHi:0) {ZF=1; NF=0;}
if(MRa > #16FHi:0) {ZF=0; NF=0;}
if(MRa < #16FHi:0) {ZF=0; NF=1;}
```

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ    MR0, #5.0 ; MR0 = 5.0 (0x40A00000)
MMOVIZ    MR1, #4.0 ; MR1 = 4.0 (0x40800000)
MMOVIZ    MR2, #-1.5 ; MR2 = -1.5 (0xBFC00000)
MMAXF32   MR0, #5.5 ; MR0 = 5.5, ZF = 0, NF = 1
MMAXF32   MR1, #2.5 ; MR1 = 4.0, ZF = 0, NF = 0
MMAXF32   MR2, #-1.0 ; MR2 = -1.0, ZF = 0, NF = 1
MMAXF32   MR2, #-1.0 ; MR2 = -1.5, ZF = 1, NF = 0
```

See also

[MMAXF32 MRa, MRb](#)
[MMINF32 MRa, MRb](#)
[MMINF32 MRa, #16FHi](#)

MMINF32 MRa, MRb 32-Bit Floating-Point Minimum**Operands**

MRa	CLA floating-point source/destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1101 0100 0000

Description

if(MRa > MRb) MRa = MRb;

Special cases for the output from the MMINF32 operation:

- NaN output will be converted to infinity
- A denormalized output will be converted to positive zero.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The ZF and NF flags are configured on the result of the operation, not the result stored in the destination register.

```
if(MRa == MRb) {ZF=1; NF=0;}
if(MRa > MRb) {ZF=0; NF=0;}
if(MRa < MRb) {ZF=0; NF=1;}
```

Pipeline

This is a single-cycle instruction.

Example 1

```
MMOVIZ MR0, #5.0 ; MR0 = 5.0 (0x40A00000)
MMOVIZ MR1, #4.0 ; MR1 = 4.0 (0x40800000)
MMOVIZ MR2, #-1.5 ; MR2 = -1.5 (0xBFC00000)
MMINF32 MR0, MR1 ; MR0 = 4.0, ZF = 0, NF = 0
MMINF32 MR1, MR2 ; MR1 = -1.5, ZF = 0, NF = 0
MMINF32 MR2, MR1 ; MR2 = -1.5, ZF = 1, NF = 0
MMINF32 MR1, MR0 ; MR2 = -1.5, ZF = 0, NF = 1
```

Example 2

```
; X is an array of 32-bit floating-point values
; Find the minimum value in an array X
; and store it in Result
;

_Cla1Task1:
MMOVI16    MAR1,#_X          ; Start address
MUI16TOF32 MR0, @_len        ; Length of the array
MNOP
MNOP
MMOV32     MR1, *MAR1[2]++   ; MR1 = X0
LOOP
MMOV32     MR2, *MAR1[2]++   ; MR2 = next element
MMINF32    MR1, MR2         ; MR1 = MAX(MR1, MR2)
MADD32     MR0, MR0, #-1.0   ; Decrement the counter
MCMPF32    MR0 #0.0         ; Set/clear flags for MBCNDD
MNOP
MNOP
MNOP
MBCNDD    LOOP, NEQ         ; Branch if not equal to zero
MMOV32    @_Result, MR1      ; Always executed
MNOP
MNOP
MSTOP
```

See also

[MMAXF32 MRa, MRb](#)

MMAXF32 MRa, #16FHi
MMINF32 MRa, #16FHi

MMINF32 MRa, #16FHi 32-Bit Floating-Point Minimum**Operands**

MRa	floating-point source/destination register (MR0 to MR3)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.

Opcode

LSW: IIII IIII IIII IIII
 MSW: 0111 1001 0100 00aa

Description

Compare MRa with the floating-point value represented by the immediate operand. If the immediate value is smaller, then load it into MRa.

```
if(MRa > #16FHi:0) MRa = #16FHi:0;
```

#16FHi is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. This addressing mode is most useful for constants where the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). The assembler will accept either a hex or float as the immediate value. That is, -1.5 can be represented as #-1.5 or #0xBFC0.

Special cases for the output from the MMINF32 operation:

- NaN output will be converted to infinity
- A denormalized output will be converted to positive zero.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The ZF and NF flags are configured on the result of the operation, not the result stored in the destination register.

```
if(MRa == #16FHi:0) {ZF=1; NF=0;}
if(MRa > #16FHi:0) {ZF=0; NF=0;}
if(MRa < #16FHi:0) {ZF=0; NF=1;}
```

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ  MR0, #5.0    ; MR0 = 5.0  (0x40A00000)
MMOVIZ  MR1, #4.0    ; MR1 = 4.0  (0x40800000)
MMOVIZ  MR2, #-1.5   ; MR2 = -1.5 (0xBFC00000)
MMINF32 MR0, #5.5    ; MR0 = 5.0, ZF = 0, NF = 1
MMINF32 MR1, #2.5    ; MR1 = 2.5, ZF = 0, NF = 0
MMINF32 MR2, #-1.0   ; MR2 = -1.5, ZF = 0, NF = 1
MMINF32 MR2, #-1.5   ; MR2 = -1.5, ZF = 1, NF = 0
```

See also

[MMAXF32 MRa, #16FHi](#)
[MMAXF32 MRa, MRb](#)
[MMINF32 MRa, MRb](#)

MMOV16 MARx, MRa, #16I Load the Auxiliary Register with MRa + 16-bit Immediate Value
Operands

MARx	Auxiliary register MAR0 or MAR1
MRa	CLA Floating-point register (MR0 to MR3)
#16I	16-bit immediate value

Opcode

LSW: IIII IIII IIII IIII (opcode of MMOV16 MAR0, MRa, #16I)
 MSW: 0111 1111 1101 00AA

LSW: IIII IIII IIII IIII (opcode of MMOV16 MAR1, MRa, #16I)
 MSW: 0111 1111 1111 00AA

Description

Load the auxiliary register, MAR0 or MAR1, with MRa(15:0) + 16-bit immediate value.
 Refer to the pipeline section for important information regarding this instruction.

MARx = MRa(15:0) + #16I;

Flags

This instruction does not modify flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction. The load of MAR0 or MAR1 will occur in the EXE phase of the pipeline. Any post increment of MAR0 or MAR1 using indirect addressing will occur in the D2 phase of the pipeline. Therefore the following applies when loading the auxiliary registers:

- **I1 and I2**

The two instructions following MMOV16 will use MAR0/MAR1 before the update occurs. Thus these two instructions will use the old value of MAR0 or MAR1.

- **I3**

Loading of an auxiliary register occurs in the EXE phase while updates due to post-increment addressing occur in the D2 phase. Thus I3 cannot use the auxiliary register or there will be a conflict. In the case of a conflict, the update due to address-mode post increment will win and the auxiliary register will not be updated with #_X.

- **I4**

Starting with the 4th instruction MAR0 or MAR1 will be the new value loaded with MMOV16.

; Assume MAR0 is 50, MR0 is 10, and #_X is 20

```

MMOV16 MAR0, MR0, #_X      ; Load MAR0 with address of X (20) + MR0 (10)
<Instruction 1>          ; I1 Will use the old value of MAR0 (50)
<Instruction 2>          ; I2 Will use the old value of MAR0 (50)
<Instruction 3>          ; I3 Cannot use MAR0
<Instruction 4>          ; I4 Will use the new value of MAR0 (30)
<Instruction 5>          ; I5

```

Table 4-15. Pipeline Activity For MMOV16 MARx, MRa , #16I

Instruction	F1	F2	D1	D2	R1	R2	E	W
MMOV16 MAR0, MR0, #_X	MMOV16							
I1	I1	MMOV16						
I2	I2	I1	MMOV16					
I3	I3	I2	I1	MMOV16				
I4	I4	I3	I2	I1	MMOV16			
I5	I5	I4	I3	I2	I1	MMOV16		
I6	I6	I5	I4	I3	I2	I1	MMOV16	6

Example 1

```

; Calculate an offset into a sin/cos table
;
_Cla1Task1:
    MMOV32 MR0,@_rad           ; MR0 = rad
    MMOV32 MR1,@_TABLE_SIZEDivTwoPi ; MR1 = TABLE_SIZE/(2*Pi)
    MMPYF32 MR1,MR0,MR1          ; MR1 = rad* TABLE_SIZE/(2*Pi)
||| MMOV32 MR2,@_TABLE_MASK      ; MR2 = TABLE_MASK
    MF32TOI32 MR3,MR1          ; MR3 = K=int(rad*TABLE_SIZE/(2*Pi))
    MAND32 MR3,MR3,MR2          ; MR3 = K & TABLE_MASK
    MLSL32 MR3,#1              ; MR3 = K * 2

    MMOV16 MAR0,MR3,#_Cos0       ; MAR0 K*2+addr of table.Cos0
    MFRACF32 MR1,MR1            ; I1
    MMOV32 MR0,@_TwoPiDivTABLE_SIZE ; I2
    MMPYF32 MR1,MR1,MR0          ; I3
||| MMOV32 MR0,@_Coef3

    MMOV32 MR2,*MAR0[ #-64]++     ; MR2 = *MAR0, MAR0 += (-64)
    ...
    ...
    MSTOP ; end of task

```

Example 2

```

; This task logs the last NUM_DATA_POINTS
; ADCRESULT1 values in the array VoltageCLA
;
; When the last element in the array has been
; filled, the task will go back to the
; the first element.
;
; Before starting the ADC conversions, force
; Task 8 to initialize the ConversionCount to zero
;
_Cla1Task2:
    MMOVZ16    MR0, @_ConversionCount   ; I1 Current Conversion
    MMOV16    MAR1, MR0, #_VoltageCLA    ; I2 Next array location
    MUI16TOF32 MR0, MR0                ; I3 Convert count to float32
    MADDF32   MR0, MR0, #1.0            ; I4 Add 1 to conversion count
    MCMPF32   MR0, #NUM_DATA_POINTS.0  ; I5 Compare count to max
    MF32TOUI16 MR0, MR0                ; I6 Convert count to Uint16
    MNOP
    MNOP
    MMOVZ16    MR2, @_AdcResult.ADCRESULT1 ; I8 Read ADCRESULT1
    MMOV16    *MAR1, MR2                ; Store ADCRESULT1
    MBCNDD    _RestartCount, GEQ        ; If count >= NUM_DATA_POINTS
    MMOVIZ    MR1, #0.0                ; Always executed: MR1=0
    MNOP
    MNOP
    MMOV16    @_ConversionCount, MR0    ; If branch not taken
    MSTOP
    ;
    _RestartCount
        MMOV16    @_ConversionCount, MR1    ; If branch taken, restart count
        MSTOP
        ;
        ; end of task

; This task initializes the ConversionCount
; to zero
;
_Cla1Task8:
    MMOVIZ MR0, #0.0
    MMOV16 @_ConversionCount, MR0
    MSTOP
_ClaT8End:

```

See also

MMOV16 MARx, mem16 Load MAR1 with 16-bit Value

Operands

MARx	CLA auxiliary register MAR0 or MAR1
mem16	16-bit destination memory accessed using one of the available addressing modes

Opcode

LSW: mmmm mmmm mmmm mmmm (Opcode for MMOV16 MAR0, mem16)
 MSW: 0111 0110 0000 addr

LSW: mmmm mmmm mmmm mmmm (Opcode for MMOV16 MAR1, mem16)
 MSW: 0111 0110 0100 addr

Description

Load MAR0 or MAR1 with the 16-bit value pointed to by mem16. Refer to the pipeline section for important information regarding this instruction.

MAR1 = [mem16];

Flags

No flags MSTF flags are affected.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction. The load of MAR0 or MAR1 will occur in the EXE phase of the pipeline. Any post increment of MAR0 or MAR1 using indirect addressing will occur in the D2 phase of the pipeline. Therefore the following applies when loading the auxiliary registers:

- I1 and I2**

The two instructions following MMOV16 will use MAR0/MAR1 before the update occurs. Thus these two instructions will use the old value of MAR0 or MAR1.

- I3**

Loading of an auxiliary register occurs in the EXE phase while updates due to post-increment addressing occur in the D2 phase. Thus I3 cannot use the auxiliary register or there will be a conflict. In the case of a conflict, the update due to address-mode post increment will win send the auxiliary register will not be updated with #_X.

- I4**

Starting with the 4th instruction MAR0 or MAR1 will be the new value loaded with MMOV16.

; Assume MAR0 is 50 and @_X is 20

```

MMOV16 MAR0, @_X      ; Load MAR0 with the contents of X (20)
<Instruction 1>      ; I1 Will use the old value of MAR0 (50)
<Instruction 2>      ; I2 Will use the old value of MAR0 (50)
<Instruction 3>      ; I3 Cannot use MAR0
<Instruction 4>      ; I4 Will use the new value of MAR0 (20)
<Instruction 5>      ; I5
....
```

Table 4-16. Pipeline Activity For MMOV16 MAR0/MAR1, mem16

Instruction	F1	F2	D1	D2	R1	R2	E	W
MMOV16 MAR0, @_X	MMOV16							
I1	I1	MMOV16						
I2	I2	I1	MMOV16					
I3	I3	I2	I1	MMOV16				
I4	I4	I3	I2	I1	MMOV16			
I5	I5	I4	I3	I2	I1	MMOV16		
I6	I6	I5	I4	I3	I2	I1	MMOV16	

Example

```

; This task logs the last NUM_DATA_POINTS
; ADCRESULT1 values in the array VoltageCLA
;
; When the last element in the array has been
; filled, the task will go back to the
; the first element.
;
; Before starting the ADC conversions, force
; Task 8 to initialize the ConversionCount to zero
;
_Cla1Task2:
    MMOVZ16      MR0, @_ConversionCount      ;I1 Current Conversion
    MMOV16       MAR1, MR0, #_VoltageCLA      ;I2 Next array location
    MUI16TOF32   MR0, MR0                  ;I3 Convert count to float32
    MADDF32     MR0, MR0, #1.0              ;I4 Add 1 to conversion count
    MCMPF32     MR0, #NUM_DATA_POINTS.0    ;I5 Compare count to max
    MF32TOUI16   MR0, MR0                  ;I6 Convert count to Uint16
    MNOP
    MMOVZ16      MR2, @_AdcResult.ADCRESULT1 ;I8 Read ADCRESULT1
    MMOV16       *MAR1, MR2                ; Store ADCRESULT1
    MBCNDD      _RestartCount, GEQ        ; If count >= NUM_DATA_POINTS
    MMOVIZ      MR1, #0.0                 ; Always executed: MR1=0
    MNOP
    MNOP
    MMOV16      @_ConversionCount, MR0      ; If branch not taken MSTOP
                                              ; store current count
_RestartCount
    MMOV16      @_ConversionCount, MR1      ; If branch taken, restart count
    MSTOP
                                              ; end of task

; This task initializes the ConversionCount
; to zero
;
_Cla1Task8:
    MMOVIZ      MR0, #0.0
    MMOV16      @_ConversionCount, MR0
    MSTOP

_ClaT8End:

```

See also

MMOV16 mem16, MARx Move 16-Bit Auxiliary Register Contents to Memory

Operands

mem16	16-bit destination memory accessed using one of the available addressing modes
MARx	CLA auxiliary register MAR0 or MAR1

Opcode

LSW: mmmm mmmm mmmm mmmm (Opcode for MMOV16 mem16, MAR0)
 MSW: 0111 0110 1000 addr

LSW: mmmm mmmm mmmm mmmm (Opcode for MMOV16 mem16, MAR1)
 MSW: 0111 0110 1100 addr

Description

Store the contents of MAR0 or MAR1 in the 16-bit memory location pointed to by mem16.

[mem16] = MAR0 ;

Flags

No flags MSTF flags are affected.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example
See also

MMOV16 mem16, MRa Move 16-Bit Floating-Point Register Contents to Memory**Operands**

mem16	16-bit destination memory accessed using one of the available addressing modes
MRa	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0101 11aa addr

Description

Move 16-bit value from the lower 16-bits of the floating-point register (MRa(15:0)) to the location pointed to by mem16.
 $[mem16] = MRa(15:0);$

Flags

No flags MSTF flags are affected.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; This task logs the last NUM_DATA_POINTS
; ADCRESULT1 values in the array VoltageCLA
;
; When the last element in the array has been
; filled, the task will go back to the
; the first element.
;
; Before starting the ADC conversions, force
; Task 8 to initialize the ConversionCount to zero
;
_Cla1Task2:
  MMOVZ16      MR0, @_ConversionCount    ;I1 Current Conversion
  MMOV16       MAR1, MR0, #_VoltageCLA   ;I2 Next array location
  MUI16TOF32   MR0, MR0                 ;I3 Convert count to float32
  MADDF32     MR0, MR0, #1.0            ;I4 Add 1 to conversion count
  MCMPF32     MR0, #NUM_DATA_POINTS.0  ;I5 Compare count to max
  MF32TOUI16   MR0, MR0                 ;I6 Convert count to Uint16
  MNOP
  MNOP
  MMOV16      @_ConversionCount, MR0    ; If branch not taken MSTOP
                                         ; store current count
_RestartCount
  MMOV16      @_ConversionCount, MR1    ; If branch taken, restart count
  MSTOP
                                         ; end of task

; This task initializes the ConversionCount
; to zero
;
_Cla1Task8:
  MMOVIZ MR0, #0.0
  MMOV16 @_ConversionCount, MR0
  MSTOP
_ClaT8End:
```

See also

[MMOVIZ MRa, #16FHi](#)
[MMOVXI MRa, #16FLoHex](#)

MMOV32 mem32, MRa Move 32-Bit Floating-Point Register Contents to Memory**Operands**

MRa	floating-point register (MR0 to MR3)
mem32	32-bit destination memory accessed using one of the available addressing modes

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0100 11aa addr

Description

Move from MRa to 32-bit memory location indicated by mem32.

[mem32] = MRa;

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

No flags affected.

Pipeline

This is a single-cycle instruction.

Example

```
; Perform 5 multiply and accumulate operations:
;
; X and Y are 32-bit floating point arrays;
; 1st multiply: A = X0 * Y0
; 2nd multiply: B = X1 * Y1
; 3rd multiply: C = X2 * Y2
; 4th multiply: D = X3 * Y3
; 5th multiply: E = X3 * Y3;
; Result = A + B + C + D + E
;

_Cal1Task1:
    MMOV16      MAR0, #_X          ; MAR0 points to X array
    MMOV16      MAR1, #_Y          ; MAR1 points to Y array
    MNOP
    MNOP
    MMOV32      MR0, *MAR0[2]++   ; MR0 = X0, MAR0 += 2
                                ; <-- MAR0 valid
    MMOV32      MR1, *MAR1[2]++   ; MR1 = Y0, MAR1 += 2
    MMPYF32     MR2, MR0, MR1    ; MR2 = A = X0 * Y0
    || MMOV32     MR0, *MAR0[2]++   ; In parallel MR0 = X1, MAR0 += 2
    || MMOV32     MR1, *MAR1[2]++   ; MR1 = Y1, MAR1 += 2
    MMPYF32     MR3, MR0, MR1    ; MR3 = B = X1 * Y1
    || MMOV32     MR0, *MAR0[2]++   ; In parallel MR0 = X2, MAR0 += 2
    || MMOV32     MR1, *MAR1[2]++   ; MR1 = Y2, MAR2 += 2
    MMACF32     MR3, MR2, MR2, MR0, MR1 ; MR3 = A + B, MR2 = C = X2 * Y2
    || MMOV32     MR0, *MAR0[2]++   ; In parallel MR0 = X3
    || MMOV32     MR1, *MAR1[2]++   ; MR1 = Y3
    MMACF32     MR3, MR2, MR2, MR0, MR1 ; MR3 = (A + B) + C, MR2 = D = X3 * Y3
    || MMOV32     MR0, *MAR0[2]++   ; In parallel MR0 = X4
    || MMOV32     MR1, *MAR1[2]++   ; MR1 = Y4
    MMPYF32     MR2, MR0, MR1    ; MR2 = E = X4 * Y4
    || MADDF32    MR3, MR3, MR2    ; in parallel MR3 = (A + B + C) + D
    || MADDF32    MR3, MR3, MR2    ; MR3 = (A + B + C + D) + E
    MMOV32      @_Result, MR3    ; Store the result MSTOP ; end of task
```

See also

[MMOV32 mem32, MSTF](#)

MMOV32 mem32, MSTF Move 32-Bit MSTF Register to Memory**Operands**

MSTF	floating-point status register
mem32	32-bit destination memory

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0111 0100 addr

Description

Copy the CLA's floating-point status register, MSTF, to memory.
 [mem32] = MSTF;

Flags

This instruction does not modify flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

[MMOV32 mem32, MRA](#)

See also

MMOV32 MRa, mem32 {, CNDF} Conditional 32-Bit Move
Operands

MRa	CLA floating-point destination register (MR0 to MR3)
mem32	32-bit memory location accessed using one of the available addressing modes
CNDF	optional condition.

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 00cn dfaa addr

Description

If the condition is true, then move the 32-bit value referenced by mem32 to the floating-point register indicated by MRa.

`if (CNDF == TRUE) MRa = [mem32];`

CNDF is one of the following conditions:

Encode ⁽¹⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽²⁾	Unconditional with flag modification	None

⁽¹⁾ Values not shown are reserved.

⁽²⁾ This is the default operation if no CNDF field is specified. This condition will allow the ZF and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

```
if(CNDF == UNCF)
{
    NF = MRa(31);
    ZF = 0;
    if(MRa(30:23) == 0) { ZF = 1; NF = 0; }
}
else No flags modified;
```

Pipeline

This is a single-cycle instruction.

Example

```
; Given A, B, X, M1 and M2 are 32-bit floating-point
; numbers
;
; if(A == B) calculate Y = X*M1
; if(A! = B) calculate Y = X*M2
;
_Cla1Task5:
    MMOV32    MR0, @_A
    MMOV32    MR1, @_B
    MCMPF32   MR0, MR1
    MMOV32    MR2, @_M1, EQ ; if A == B, MR2 = M1
                    ;      Y = M1*X
    MMOV32    MR2, @_M2, NEQ ; if A! = B, MR2 = M2
                    ;      Y = M2*X
    MMOV32    MR3, @_X
    MMPYF32   MR3, MR2, MR3 ; Calculate Y
    MMOV32    @_Y, MR3       ; Store Y
    MSTOP
```

; end of task

See also

[MMOV32 MRa, MRb {, CNDF}](#)
[MMOVD32 MRa, mem32](#)

MMOV32 MRa, MRb {, CNDF} Conditional 32-Bit Move
Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
CNDF	optional condition.

Opcode

LSW: 0000 0000 cndf bbba
 MSW: 0111 1010 1100 0000

Description

If the condition is true, then move the 32-bit value in MRb to the floating-point register indicated by MRa.

```
if (CNDF == TRUE) MRa = MRb;
```

CNDF is one of the following conditions:

Encode ⁽³⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽⁴⁾	Unconditional with flag modification	None

(3) Values not shown are reserved.

(4) This is the default operation if no CNDF field is specified. This condition will allow the ZF, and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

```
if(CNDF == UNCF)
{
    NF = MRa(31); ZF = 0;
    if(MRa(30:23) == 0) {ZF = 1; NF = 0;}
}
else No flags modified;
```

Pipeline

This is a single-cycle instruction.

Example

```
; Given: X = 8.0
;          Y = 7.0
;          A = 2.0
;          B = 5.0
; _ClaTask1
    MMOV32    MR3, @_X      ; MR3 = X = 8.0
    MMOV32    MR0, @_Y      ; MR0 = Y = 7.0
    MMAXF32   MR3, MR0     ; ZF = 0, NF = 0, MR3 = 8.0
    MMOV32    MR1, @_A, GT  ; true, MR1 = A = 2.0
    MMOV32    MR1, @_B, LT  ; false, does not load MR1
    MMOV32    MR2, MR1, GT  ; true, MR2 = MR1 = 2.0
    MMOV32    MR2, MR0, LT  ; false, does not load MR2
    MSTOP
```

See also

[MMOV32 MRa, mem32 {,CNDF}](#)

MMOV32 MSTF, mem32 Move 32-Bit Value from Memory to the MSTF Register

Operands

MSTF	CLA status register
mem32	32-bit source memory location

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0111 0000 addr

Description

Move from memory to the CLA's status register MSTF. This instruction is most useful when nesting function calls (via MCCNDD).

MSTF = [mem32];

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	Yes	Yes	Yes	Yes	Yes

Loading the status register will overwrite all flags and the RPC field. The MEALLOW field is not affected.

Pipeline

This is a single-cycle instruction.

Example

See also [MMOV32 mem32, MSTF](#)

MMOVD32 MRa, mem32 Move 32-Bit Value from Memory with Data Copy**Operands**

MRa	CLA floating-point register (MR0 to MR3)
mem32	32-bit memory location accessed using one of the available addressing modes

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0100 00aa addr

Description

Move the 32-bit value referenced by mem32 to the floating-point register indicated by MRa.

```
MRa = [mem32];
[mem32+2] = [mem32];
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

```
NF = MRa(31);
ZF = 0;
if(MRa(30:23) == 0){ ZF = 1; NF = 0; }
```

Pipeline

This is a single-cycle instruction.

Example

```
; sum = X0*B0 + X1*B1 + X2*B2 + Y1*A1 + Y2*B2
;
; X2 = X1
; X1 = X0
; Y2 = Y1
; Y1 = sum
;

_Cla1Task2:
  MMOV32 MR0, @_B2      ; MR0 = B2
  MMOV32 MR1, @_X2      ; MR1 = X2
  MMPLYF32 MR2, MR1, MR0 ; MR2 = X2*B2
|| MMOV32 MR0, @_B1      ; MR0 = B1
  MMOV32 MR1, @_X1      ; MR1 = X1, X2 = X1
  MMPLYF32 MR3, MR1, MR0 ; MR3 = X1*B1
|| MMOV32 MR0, @_B0      ; MR0 = B0
  MMOV32 MR1, @_X0      ; MR1 = X0, X1 = X0

; MR3 = X1*B1 + X2*B2, MR2 = X0*B0
; MR0 = A2
  MMACF32 MR3, MR2, MR2, MR1, MR0
|| MMOV32 MR0, @_A2

  MMOV32 MR1, @_Y2      ; MR1 = Y2

; MR3 = X0*B0 + X1*B1 + X2*B2, MR2 = Y2*A2
; MR0 = A1
  MMACF32 MR3, MR2, MR2, MR1, MR0
|| MMOV32 MR0, @_A1

  MMOV32 MR1, @_Y1      ; MR1 = Y1, Y2 = Y1
  MADD32 MR3, MR3, MR2   ; MR3 = Y2*A2 + X0*B0 + X1*B1 + X2*B2
|| MMPLYF32 MR2, MR1, MR0 ; MR2 = Y1*A1
  MADD32 MR3, MR3, MR2   ; MR3 = Y1*A1 + Y2*A2 + X0*B0 + X1*B1 + X2*B2
  MMOV32 @_Y1, MR3       ; Y1 = MR3
  MSTOP                  ; end of task
```

See also

[MMOV32 MRa, mem32 {,CNDF}](#)

MMOVF32 MRa, #32F Load the 32-Bits of a 32-Bit Floating-Point Register

Operands	This instruction is an alias for MMOVIZ and MMOVXI instructions. The second operand is translated by the assembler such that the instruction becomes: MMOVIZ MRa, #16FHiHex MMOVXI MRa, #16FLoHex MRa CLA floating-point destination register (MR0 to MR3) #32F immediate float value represented in floating-point representation												
Opcode	LSW: IIII IIII IIII IIII (opcode of MMOVIZ MRa, #16FHiHex) MSW: 0111 1000 0100 00aa LSW: IIII IIII IIII IIII (opcode of MMOVXI MRa, #16FLoHex) MSW: 0111 1000 1000 00aa												
Description	Note: This instruction accepts the immediate operand only in floating-point representation. To specify the immediate value as a hex value (IEEE 32-bit floating-point format) use the MOVI32 MRa, #32FHex instruction. Load the 32-bits of MRa with the immediate float value represented by #32F. #32F is a float value represented in floating-point representation. The assembler will only accept a float value represented in floating-point representation. That is, 3.0 can only be represented as #3.0. #0x40400000 will result in an error. MRa = #32F;												
Flags	This instruction modifies the following flags in the MSTF register:												
	<table border="1"> <thead> <tr> <th>Flag</th><th>TF</th><th>ZF</th><th>NF</th><th>LUF</th><th>LVF</th></tr> </thead> <tbody> <tr> <td>Modified</td><td>No</td><td>No</td><td>No</td><td>No</td><td>No</td></tr> </tbody> </table>	Flag	TF	ZF	NF	LUF	LVF	Modified	No	No	No	No	No
Flag	TF	ZF	NF	LUF	LVF								
Modified	No	No	No	No	No								
Pipeline	Depending on #32FH, this instruction takes one or two cycles. If all of the lower 16-bits of the IEEE 32-bit floating-point format of #32F are zeros, then the assembler will convert MMOVF32 into only MMOVIZ instruction. If the lower 16-bits of the IEEE 32-bit floating-point format of #32F are not zeros, then the assembler will convert MMOVF32 into MMOVIZ and MMOVXI instructions.												
Example	<pre> MMOVF32 MR1, #3.0 ; MR1 = 3.0 (0x40400000) ; Assembler converts this instruction as ; MMOVIZ MR1, #0x4040 MMOVF32 MR2, #0.0 ; MR2 = 0.0 (0x00000000) ; Assembler converts this instruction as ; MMOVIZ MR2, #0x0 MMOVF32 MR3, #12.265 ; MR3 = 12.625 (0x41443D71) ; Assembler converts this instruction as ; MMOVIZ MR3, #0x4144 ; MMOVXI MR3, #0x3D71 </pre>												
See also	MMOVIZ MRa, #16FHi MMOVXI MRa, #16FLoHex MOVI32 MRa, #32FHex												

MMOVI16 MARx, #16I Load the Auxiliary Register with the 16-Bit Immediate Value**Operands**

MARx	Auxiliary register MAR0 or MAR1
#16I	16-bit immediate value

Opcode

LSW: IIII IIII IIII IIII (opcode of MMOVI16 MAR0, #16I)
 MSW: 0111 1111 1100 0000

LSW: IIII IIII IIII IIII (opcode of MMOVI16 MAR1, #16I)
 MSW: 0111 1111 1110 0000

Description

Load the auxiliary register, MAR0 or MAR1, with a 16-bit immediate value. Refer to the pipeline section for important information regarding this instruction.

MARx = #16I;

Flags

This instruction does not modify flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction. The immediate load of MAR0 or MAR1 will occur in the EXE phase of the pipeline. Any post increment of MAR0 or MAR1 using indirect addressing will occur in the D2 phase of the pipeline. Therefore the following applies when loading the auxiliary registers:

- I1 and I2**

The two instructions following MMOVI16 will use MAR0/MAR1 before the update occurs. Thus these two instructions will use the old value of MAR0 or MAR1.

- I3**

Loading of an auxiliary register occurs in the EXE phase while updates due to post-increment addressing occur in the D2 phase. Thus I3 cannot use the auxiliary register or there will be a conflict. In the case of a conflict, the update due to address-mode post increment will win and the auxiliary register will not be updated with #_X.

- I4**

Starting with the 4th instruction MAR0 or MAR1 will be the new value loaded with MMOVI16.

; Assume MAR0 is 50 and #_X is 20

```
MMOVI16 MAR0, #_X          ; Load MAR0 with address of X (20)
<Instruction 1>           ; I1 Will use the old value of MAR0 (50)
<Instruction 2>           ; I2 Will use the old value of MAR0 (50)
<Instruction 3>           ; I3 Cannot use MAR0
<Instruction 4>           ; I4 Will use the new value of MAR0 (20)
<Instruction 5>           ; I5
....
```

Table 4-17. Pipeline Activity For MMOVI16 MAR0/MAR1, #16I

Instruction	F1	F2	D1	D2	R1	R2	E	W
MMOVI16 MAR0, #_X	MMOVI16							
I1	I1	MMOVI16						
I2	I2	I1	MMOVI16					
I3	I3	I2	I1	MMOVI16				
I4	I4	I3	I2	I1	MMOVI16			
I5	I5	I4	I3	I2	I1	MMOVI16		
I6	I6	I5	I4	I3	I2	I1	MMOVI16	

MMOV132 MRa, #32FHex Load the 32-Bits of a 32-Bit Floating-Point Register with the Immediate

Operands

MRa	floating-point register (MR0 to MR3)
#32FHex	A 32-bit immediate value that represents an IEEE 32-bit floating-point value.

This instruction is an alias for MMOVIZ and MMOVXI instructions. The second operand is translated by the assembler such that the instruction becomes:

```
MMOVIZ MRa, #16FHiHex
MMOVXI MRa, #16FLoHex
```

Opcode

LSW: IIII IIII IIII IIII (opcode of MMOVIZ MRa, #16FHiHex)
MSW: 0111 1000 0100 00aa

LSW: IIII IIII IIII IIII (opcode of MMOVXI MRa, #16FLoHex)
MSW: 0111 1000 1000 00aa

Description

Note: This instruction only accepts a hex value as the immediate operand. To specify the immediate value with a floating-point representation use the MMOVF32 MRa, #32F instruction.

Load the 32-bits of MRa with the immediate 32-bit hex value represented by #32FHex.

#32FHex is a 32-bit immediate hex value that represents the IEEE 32-bit floating-point value of a floating-point number. The assembler will only accept a hex immediate value. That is, 3.0 can only be represented as #0x40400000. #3.0 will result in an error.

```
MRa = #32FHex;
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

Depending on #32FHex, this instruction takes one or two cycles. If all of the lower 16-bits of #32FHex are zeros, then assembler will convert MOVI32 to the MMOVIZ instruction. If the lower 16-bits of #32FHex are not zeros, then assembler will convert MOVI32 to a MMOVIZ and a MMOVXI instruction.

Example

```
MOVI32 MR1, #0x40400000 ; MR1 = 0x40400000
; Assembler converts this instruction as
; MMOVIZ MR1, #0x4040

MOVI32 MR2, #0x00000000 ; MR2 = 0x00000000
; Assembler converts this instruction as
; MMOVIZ MR2, #0x0

MOVI32 MR3, #0x40004001 ; MR3 = 0x40004001
; Assembler converts this instruction as
; MMOVIZ MR3, #0x4000
; MMOVXI MR3, #0x4001

MOVI32 MRO, #0x00004040 ; MRO = 0x00004040
; Assembler converts this instruction as
; MMOVIZ MRO, #0x0000
; MMOVXI MRO, #0x4040
```

See also

[MMOVIZ MRa, #16FHi](#)
[MMOVXI MRa, #16FLoHex](#)
[MMOVF32 MRa, #32F](#)

MMOVIZ MRa, #16FHi Load the Upper 16-Bits of a 32-Bit Floating-Point Register**Operands**

MRa	floating-point register (MR0 to MR3)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.

Opcode

LSW: IIII IIII IIII IIII
 MSW: 0111 1000 0100 00aa

Description

Load the upper 16-bits of MRa with the immediate value #16FHi and clear the low 16-bits of MRa.

#16FHiHex is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. The assembler will only accept a decimal or hex immediate value. That is, -1.5 can be represented as #-1.5 or #0xBFC0.

By itself, MMOVIZ is useful for loading a floating-point register with a constant in which the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). If a constant requires all 32-bits of a floating-point register to be initialized, then use MMOVIZ along with the MMOVXI instruction.

```
MRa(31:16) = #16FHi;
MRa(15:0) = 0;
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; Load MR0 and MR1 with -1.5 (0xBFC00000)
      MMOVIZ    MR0, #0xBFC0          ; MR0 = 0xBFC00000 (1.5)
      MMOVIZ    MR1, #-1.5           ; MR1 = -1.5 (0xBFC00000)

; Load MR2 with pi = 3.141593 (0x40490FDB)
      MMOVIZ    MR2, #0x4049          ; MR2 = 0x40490000
      MMOVXI    MR2, #0x0FDB         ; MR2 = 0x40490FDB
```

See also

[MMOVF32 MRa, #32F](#)
[MMOVI32 MRa, #32FHex](#)
[MMOVXI MRa, #16FLoHex](#)

MMOVZ16 MRa, mem16 *Load MRx With 16-bit Value*

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
mem16	16-bit source memory location

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0101 10aa addr

Description

Move the 16-bit value referenced by mem16 to the floating-point register indicated by MRa.

```
MRa(31:16) = 0;  

MRa(15:0) = [mem16];
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
NF = 0;  

if (MRa(31:0)== 0) { ZF = 1; }
```

Pipeline

This is a single-cycle instruction.

MMOVXI MRa, #16FLoHex Move Immediate to the Low 16-Bits of a Floating-Point Register**Operands**

MRa	CLA floating-point register (MR0 to MR3)
#16FLoHex	A 16-bit immediate hex value that represents the lower 16-bits of an IEEE 32-bit floating-point value. The upper 16-bits will not be modified.

Opcode

LSW: IIII IIII IIII IIII
 MSW: 0111 1000 1000 00aa

Description

Load the low 16-bits of MRa with the immediate value #16FLoHex. #16FLoHex represents the lower 16-bits of an IEEE 32-bit floating-point value. The upper 16-bits of MRa will not be modified. MMOVXI can be combined with the MMOVIZ instruction to initialize all 32-bits of a MRa register.

MRa(15:0) = #16FLoHex;
 MRa(31:16) = Unchanged;

Flags

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; Load MR0 with pi = 3.141593 (0x40490FDB)
MMOVIZ      MR0,#0x4049          ; MR0 = 0x40490000
MMOVXI      MR0,#0x0FDB        ; MR0 = 0x40490FDB
```

See also

[MMOVIZ MRa, #16FHi](#)

MMPYF32 MRa, MRb, MRc 32-Bit Floating-Point Multiply

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
MRc	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 00cc bbba
 MSW: 0111 1100 0000 0000

Description

Multiply the contents of two floating-point registers.

MRa = MRb * MRc;

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MMPYF32 generates an underflow condition.
- LVF = 1 if MMPYF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example

```
; Calculate Num/Den using a Newton-Raphson algorithm for 1/Den
; Ye = Estimate(1/X)
; Ye = Ye*(2.0 - Ye*X)
; Ye = Ye*(2.0 - Ye*X)
;
_ClalTask1:
    MMOV32    MR1, @_Den      ; MR1 = Den
    MEINVF32  MR2, MR1       ; MR2 = Ye = Estimate(1/Den)
    MMPYF32   MR3, MR2, MR1  ; MR3 = Ye*Den
    MSUBF32   MR3, #2.0, MR3 ; MR3 = 2.0 - Ye*Den
    MMPYF32   MR2, MR3, MR3  ; MR2 = Ye = Ye*(2.0 - Ye*Den)
    MMPYF32   MR3, MR2, MR1  ; MR3 = Ye*Den
|| MMOV32    MR0, @_Num      ; MR0 = Num
    MSUBF32   MR3, #2.0, MR3 ; MR3 = 2.0 - Ye*Den
    MMPYF32   MR2, MR3, MR3  ; MR2 = Ye = Ye*(2.0 - Ye*Den)
|| MMOV32    MR1, @_Den      ; Reload Den To Set Sign
    MNEGF32   MR0, MR0, EQ    ; if(Den == 0.0) Change Sign Of Num
    MMPYF32   MR0, MR2, MR0   ; MR0 = Y = Ye*Num
    MMOV32    @_Dest, MR0     ; Store result
    MSTOP
; end of task
```

See also

[MMPYF32 MRa, #16FHi, MRb](#)
[MMPYF32 MRa, MRb, MRc || MADDF32 MRd, MRe, MRF](#)
[MMPYF32 MRd, MRe, MRF || MMOV32 MRa, mem32](#)
[MMPYF32 MRd, MRe, MRF || MMOV32 mem32, MRa](#)
[MMPYF32 MRa, MRb, MRc || MSUBF32 MRd, MRe, MRF](#)
[MMACF32 MR3, MR2, MRd, MRe, MRF || MMOV32 MRa, mem32](#)

MMPYF32 MRa, #16FHi, MRb 32-Bit Floating-Point Multiply**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.
MRc	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: IIII IIII IIII IIII
MSW: 0111 0111 1000 baaa

Description

Multiply MRb with the floating-point value represented by the immediate operand. Store the result of the addition in MRa.

#16FHi is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. #16FHi is most useful for representing constants where the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). The assembler will accept either a hex or float as the immediate value. That is, the value -1.5 can be represented as #-1.5 or #0xBFC0.

MRa = MRb * #16FHi:0;

This instruction can also be written as MMPYF32 MRa, MRb, #16FHi.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MMPYF32 generates an underflow condition.
- LVF = 1 if MMPYF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example 1

```
; Same as example 2 but #16FHi is represented in float
    MMOVIZ    MR3, #2.0      ; MR3 = 2.0 (0x40000000)
    MMPYF32   MR0, #3.0, MR3 ; MR0 = 3.0 * MR3 = 6.0 (0x40C00000)
    MMOV32    @_X, MR0       ; Save the result in variable X
```

Example 2

```
; Same as example 1 but #16FHi is represented in Hex
    MMOVIZ    MR3, #2.0      ; MR3 = 2.0 (0x40000000)
    MMPYF32   MR0, #0x4040, MR3 ; MR0 = 0x4040 * MR3 = 6.0 (0x40C00000)
    MMOV32    @_X, MR0       ; Save the result in variable X
```

Example 3

```

; Given X, M and B are IQ24 numbers:
; X = IQ24(+2.5) = 0x02800000
; M = IQ24(+1.5) = 0x01800000
; B = IQ24(-0.5) = 0xFF800000
;
; Calculate Y = X * M + B
;
;
_Cla1Task2:
;
; Convert M, X and B from IQ24 to float
    MI32TOF32    MR0, @_M           ; MR0 = 0x4BC00000
    MI32TOF32    MR1, @_X           ; MR1 = 0x4C200000
    MI32TOF32    MR2, @_B           ; MR2 = 0xCB000000
    MMPYF32      MR0, MR0, #0x3380 ; M = 1/(1*2^24) * iqm = 1.5 (0x3FC00000)
    MMPYF32      MR1, MR1, #0x3380 ; X = 1/(1*2^24) * iqx = 2.5 (0x40200000)
    MMPYF32      MR2, MR2, #0x3380 ; B = 1/(1*2^24) * iqb = -.5 (0xBF000000)
    MMPYF32      MR3, MR0, MR1     ; M*X
    MADDF32      MR2, MR2, MR3     ; Y=MX+B = 3.25 (0x40500000)
; Convert Y from float32 to IQ24
    MMPYF32      MR2, MR2, #0x4B80 ; Y * 1*2^24
    MF32TOI32    MR2, MR2         ; IQ24(Y) = 0x03400000
    MMOV32 @_Y, MR2                ; store result
    MSTOP          ; end of task

```

See also

[MMPYF32 MRa, MRb, #16FHi](#)
[MMPYF32 MRa, MRb, MRc](#)
[MMPYF32 MRa, MRb, MRc || MADDF32 MRd, MRe, MRF](#)

MMPYF32 MRa, MRb, #16FHi 32-Bit Floating-Point Multiply**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.

Opcode

LSW: IIII IIII IIII IIII
MSW: 0111 0111 1000 baaa

Description

Multiply MRb with the floating-point value represented by the immediate operand. Store the result of the addition in MRa.

#16FHi is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. #16FHi is most useful for representing constants where the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). The assembler will accept either a hex or float as the immediate value. That is, the value -1.5 can be represented as #-1.5 or #0xBFC0.

MRa = MRb * #16FHi:0;

This instruction can also be written as MMPYF32 MRa, #16FHi, MRb.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MMPYF32 generates an underflow condition.
- LVF = 1 if MMPYF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example 1

```
; Same as example 2 but #16FHi is represented in float
    MMOVIZ    MR3, #2.0          ; MR3 = 2.0 (0x40000000)
    MMPYF32   MR0, MR3, #3.0    ; MR0 = MR3 * 3.0 = 6.0 (0x40C00000)
    MMOV32    @_X, MR0          ; Save the result in variable X
```

Example 2

```
; Same as above example but #16FHi is represented in Hex
    MMOVIZ    MR3, #2.0          ; MR3 = 2.0 (0x40000000)
    MMPYF32   MR0, MR3, #0x4040 ; MR0 = MR3 * 0x4040 = 6.0 (0x40C00000)
    MMOV32    @_X, MR0          ; Save the result in variable X
```

Example 3

```

; Given X, M and B are IQ24 numbers:
; X = IQ24(+2.5) = 0x02800000
; M = IQ24(+1.5) = 0x01800000
; B = IQ24(-0.5) = 0xFF800000
;
; Calculate Y = X * M + B
;
_Cla1Task2:
;
; Convert M, X and B from IQ24 to float
    MI32TOF32    MR0, @_M          ; MR0 = 0x4BC00000
    MI32TOF32    MR1, @_X          ; MR1 = 0x4C200000
    MI32TOF32    MR2, @_B          ; MR2 = 0xCB000000
    MMPYF32      MR0, #0x3380, MR0 ; M = 1/(1*2^24) * iqM = 1.5 (0x3FC00000)
    MMPYF32      MR1, #0x3380, MR1 ; X = 1/(1*2^24) * iqX = 2.5 (0x40200000)
    MMPYF32      MR2, #0x3380, MR2 ; B = 1/(1*2^24) * iqB = -.5 (0xBF000000)
    MADDF32     MR3, MR0, MR1    ; M*X
    MADDF32     MR2, MR2, MR3    ; Y=MX+B = 3.25 (0x40500000)

; Convert Y from float32 to IQ24
    MMPYF32     MR2, #0x4B80, MR2 ; Y * 1*2^24
    MF32TOI32    MR2, MR2        ; IQ24(Y) = 0x03400000
    MMOV32      @_Y, MR2         ; store result
    MSTOP          ; end of task

```

See also

[MMPYF32 MRa, #16FHi, MRb](#)
[MMPYF32 MRa, MRb, MRc](#)

MMPYF32 MRa, MRb, MRc||MADDF32 MRd, MRe, MRf 32-Bit Floating-Point Multiply with Parallel Add

Operands

MRa	CLA floating-point destination register for MMPYF32 (MR0 to MR3) MRa cannot be the same register as MRd
MRb	CLA floating-point source register for MMPYF32 (MR0 to MR3)
MRc	CLA floating-point source register for MMPYF32 (MR0 to MR3)
MRd	CLA floating-point destination register for MADDF32 (MR0 to MR3) MRd cannot be the same register as MRa
MRe	CLA floating-point source register for MADDF32 (MR0 to MR3)
MRf	CLA floating-point source register for MADDF32 (MR0 to MR3)

Opcode

LSW: 0000 ffee ddcc bbaa
MSW: 0111 1010 0000 0000

Description

Multiply the contents of two floating-point registers with parallel addition of two registers.
 $MRa = MRb * MRc;$
 $MRd = MRe + MRf;$

Restrictions

The destination register for the MMPYF32 and the MADDF32 must be unique. That is, MRa cannot be the same register as MRd.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MMPYF32 or MADDF32 generates an underflow condition.
- LVF = 1 if MMPYF32 or MADDF32 generates an overflow condition.

Pipeline

Both MMPYF32 and MADDF32 complete in a single cycle.

Example

```

; Perform 5 multiply and accumulate operations:
;
; X and Y are 32-bit floating point arrays
;
; 1st multiply: A = X0 * Y0
; 2nd multiply: B = X1 * Y1
; 3rd multiply: C = X2 * Y2
; 4th multiply: D = X3 * Y3
; 5th multiply: E = X3 * Y3
;
; Result = A + B + C + D + E
;
_Cla1Task1:
    MMOV16    MAR0, #_X          ; MAR0 points to X array
    MMOV16    MAR1, #_Y          ; MAR1 points to Y array
    MNOP
    MNOP
    ; Delay for MAR0, MAR1 load
    ; Delay for MAR0, MAR1 load
    ; <-- MAR0 valid
    MMOV32    MR0, *MAR0[2]++    ; MR0 = X0, MAR0 += 2
    ; <-- MAR1 valid
    MMOV32    MR1, *MAR1[2]++    ; MR1 = Y0, MAR1 += 2

    MMPYF32   MR2, MR0, MR1      ; MR2 = A = X0 * Y0
|| MMOV32    MR0, *MAR0[2]++    ; In parallel MR0 = X1, MAR0 += 2
|| MMOV32    MR1, *MAR1[2]++    ; MR1 = Y1, MAR1 += 2

    MMPYF32   MR3, MR0, MR1      ; MR3 = B = X1 * Y1
|| MMOV32    MR0, *MAR0[2]++    ; In parallel MR0 = X2, MAR0 += 2
|| MMOV32    MR1, *MAR1[2]++    ; MR1 = Y2, MAR2 += 2

    MMACF32   MR3, MR2, MR2, MR0, MR1 ; MR3 = A + B, MR2 = C = X2 * Y2
|| MMOV32    MR0, *MAR0[2]++    ; In parallel MR0 = X3
|| MMOV32    MR1, *MAR1[2]++    ; MR1 = Y3

    MMACF32   MR3, MR2, MR2, MR0, MR1 ; MR3 = (A + B) + C, MR2 = D = X3 * Y3
|| MMOV32    MR0, *MAR0          ; In parallel MR0 = X4
|| MMOV32    MR1, *MAR1          ; MR1 = Y4

    MMPYF32   MR2, MR0, MR1      ; MR2 = E = X4 * Y4
|| MADDF32   MR3, MR3, MR2      ; in parallel MR3 = (A + B + C) + D

    MADDF32   MR3, MR3, MR2      ; MR3 = (A + B + C + D) + E
    MMOV32    @_Result, MR3       ; Store the result
    MSTOP
    ; end of task

```

See also

[MMACF32 MR3, MR2, MRd, MRe, MRf || MMOV32 MRa, mem32](#)

MMPYF32 MRd, MRe, MRf ||MMOV32 MRa, mem32 32-Bit Floating-Point Multiply with Parallel Move**Operands**

MRd	CLA floating-point destination register for the MMPYF32 (MR0 to MR3) MRd cannot be the same register as MRa
MRe	CLA floating-point source register for the MMPYF32 (MR0 to MR3)
MRf	CLA floating-point source register for the MMPYF32 (MR0 to MR3)
MRa	CLA floating-point destination register for the MMOV32 (MR0 to MR3) MRa cannot be the same register as MRd
mem32	32-bit memory location accessed using one of the available addressing modes. This will be the source of the MMOV32.

Opcode

LSW: mmmm mmmm mmmm mmmm
MSW: 0000 ffee ddaa addr

Description

Multiply the contents of two floating-point registers and load another.

```
MRd = MRe * MRf;
MRa = [mem32];
```

Restrictions

The destination register for the MMPYF32 and the MMOV32 must be unique. That is, MRa cannot be the same register as MRd.

Flags

This instruction modifies the following flags in the MSTF register::

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MMPYF32 generates an underflow condition.
- LVF = 1 if MMPYF32 generates an overflow condition.

The MMOV32 Instruction will set the NF and ZF flags as follows:

```
NF = MRa(31);
ZF = 0;
if(MRa(30:23) == 0) { ZF = 1; NF = 0; }
```

Pipeline

Both MMPYF32 and MMOV32 complete in a single cycle.

Example 1

```
; Given M1, X1 and B1 are 32-bit floating point
; Calculate Y1 = M1*X1+B1
;
_Cla1Task1:
    MMOV32    MR0, @M1      ; Load MR0 with M1
    MMOV32    MR1, @X1      ; Load MR1 with X1
    MMPYF32   MR1, MR1, MR0 ; Multiply M1*X1
|| MMOV32    MR0, @B1      ; and in parallel load MR0 with B1
    MADDF32   MR1, MR1, MR0 ; Add M*X1 to B1 and store in MR1
    MMOV32    @Y1, MR1      ; Store the result
    MSTOP
```

Example 2

```

; Given A, B and C are 32-bit floating-point numbers
; Calculate Y2 = (A * B)
;           Y3 = (A * B) * C
;
_Cla1Task2:
    MMOV32    MR0, @A          ; Load MR0 with A
    MMOV32    MR1, @B          ; Load MR1 with B
    MMPYF32   MR1, MR1, MR0   ; Multiply A*B
|| MMOV32    MR0, @C          ; and in parallel load MR0 with C
|| MMPYF32   MR1, MR1, MR0   ; Multiply (A*B) by C
|| MMOV32    @Y2, MR1         ; and in parallel store A*B
    MMOV32    @Y3, MR1         ; Store the result
    MSTOP
;
```

See also

[MMPYF32 MRd, MRe, MRf || MMOV32 mem32, MRa](#)
[MMACF32 MR3, MR2, MRd, MRe, MRf || MMOV32 MRe, mem32](#)

MMPYF32 MRd, MRe, MRf || MMOV32 mem32, MRa 32-Bit Floating-Point Multiply with Parallel Move**Operands**

MRd	CLA floating-point destination register for the MMPYF32 (MR0 to MR3)
MRe	CLA floating-point source register for the MMPYF32 (MR0 to MR3)
MRf	CLA floating-point source register for the MMPYF32 (MR0 to MR3)
mem32	32-bit memory location accessed using one of the available addressing modes. This will be the destination of the MMOV32.
MRa	CLA floating-point source register for the MMOV32 (MR0 to MR3)

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0100 ffee ddaa addr

Description

Multiply the contents of two floating-point registers and move from memory to register.

MRd = MRe * MRf;
 [mem32] = MRa;

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MMPYF32 generates an underflow condition.
- LVF = 1 if MMPYF32 generates an overflow condition.

Pipeline

MMPYF32 and MMOV32 both complete in a single cycle.

Example

```
; Given A, B and C are 32-bit floating-point numbers
; Calculate Y2 = (A * B)
;           Y3 = (A * B) * C
;
_Cla1Task2:
    MMOV32    MR0, @A          ; Load MR0 with A
    MMOV32    MR1, @B          ; Load MR1 with B
    MMPYF32   MR1, MR1, MR0   ; Multiply A*B
||    MMOV32    MR0, @C          ; and in parallel load MR0 with C
    MMPYF32   MR1, MR1, MR0   ; Multiply (A*B) by C
||    MMOV32    @Y2, MR1        ; and in parallel store A*B
    MMOV32    @Y3, MR1        ; Store the result
    MSTOP                                ; end of task
```

See also

[MMPYF32 MRd, MRe, MRf || MMOV32 MRa, mem32](#)
[MMACF32 MR3, MR2, MRd, MRe, MRf || MMOV32 MRa, mem32](#)

MMPYF32 MRa, MRb, MRc || MSUBF32 MRd, MRe, MRf 32-Bit Floating-Point Multiply with Parallel Subtract

Operands

MRa	CLA floating-point destination register for MMPYF32 (MR0 to MR3) MRa cannot be the same register as MRd
MRb	CLA floating-point source register for MMPYF32 (MR0 to MR3)
MRc	CLA floating-point source register for MMPYF32 (MR0 to MR3)
MRd	CLA floating-point destination register for MSUBF32 (MR0 to MR3) MRd cannot be the same register as MRa
MRe	CLA floating-point source register for MSUBF32 (MR0 to MR3)
MRf	CLA floating-point source register for MSUBF32 (MR0 to MR3)

Opcode

LSW: 0000 ffee ddcc bbaa
MSW: 0111 1010 0100 0000

Description

Multiply the contents of two floating-point registers with parallel subtraction of two registers.

```
MRa = MRb * MRc;
MRd = MRe - MRf;
```

Restrictions

The destination register for the MMPYF32 and the MSUBF32 must be unique. That is, MRa cannot be the same register as MRd.

Flags

This instruction modifies the following flags in the MSTF register::

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MMPYF32 or MSUBF32 generates an underflow condition.
- LVF = 1 if MMPYF32 or MSUBF32 generates an overflow condition.

Pipeline

MMPYF32 and MSUBF32 both complete in a single cycle.

Example

```
; Given A, B and C are 32-bit floating-point numbers
; Calculate Y2 = (A * B)
;           Y3 = (A - B)
;
_Cla1Task2:
    MMOV32    MR0, @A          ; Load MR0 with A
    MMOV32    MR1, @B          ; Load MR1 with B
    MMPYF32   MR2, MR0, MR1   ; Multiply (A*B)
|| MSUBF32  MR3, MR0, MR1   ; and in parallel Sub (A-B)
    MMOV32    @Y2, MR2        ; Store A*B
    MMOV32    @Y3, MR3        ; Store A-B
    MSTOP                                ; end of task
```

See also

[MSUBF32 MRa, MRb, MRc](#)
[MSUBF32 MRd, MRe, MRf || MMOV32 MRa, mem32](#)
[MSUBF32 MRd, MRe, MRf || MMOV32 mem32, MRa](#)

MNEGF32 MRa, MRb{, CNDF} Conditional Negation**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
CNDF	condition tested

Opcode

LSW: 0000 0000 cndf bbba
 MSW: 0111 1010 1000 0000

Description

```
if (CNDF == true) {MRa = - MRb; }
else {MRa = MRb; }
```

CNDF is one of the following conditions:

Encode ⁽⁵⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽⁶⁾	Unconditional with flag modification	None

⁽⁵⁾ Values not shown are reserved.

⁽⁶⁾ This is the default operation if no CNDF field is specified. This condition will allow the ZF, and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

Pipeline

This is a single-cycle instruction.

Example 1

```
; Show the basic operation of MNEGF32
;
  MMOVIZ    MR0, #5.0      ; MR0 = 5.0 (0x40A00000)
  MMOVIZ    MR1, #4.0      ; MR1 = 4.0 (0x40800000)
  MMOVIZ    MR2, #-1.5     ; MR2 = -1.5 (0xBFC00000)
  MMPYF32   MR3, MR1, MR2 ; MR3 = -6.0
  MMPYF32   MR0, MR0, MR1 ; MR0 = 20.0
  MMOVIZ    MR1, #0.0
  MCMPF32   MR3, MR1      ; NF = 1
  MNEGF32   MR3, MR3, LT   ; if NF = 1, MR3 = 6.0
  MCMPF32   MR0, MR1      ; NF = 0
  MNEGF32   MR0, MR0, GEQ  ; if NF = 0, MR0 = -20.0
```

Example 2

```

; Calculate Num/Den using a Newton-Raphson algorithm for 1/Den
; Ye = Estimate(1/X)
; Ye = Ye*(2.0 - Ye*X)
; Ye = Ye*(2.0 - Ye*X)
;
_Cla1Task1:
    MMOV32    MR1, @_Den      ; MR1 = Den
    MEINVF32  MR2, MR1       ; MR2 = Ye = Estimate(1/Den)
    MMPYF32   MR3, MR2, MR1  ; MR3 = Ye*Den
    MSUBF32   MR3, #2.0, MR3 ; MR3 = 2.0 - Ye*Den
    MMPYF32   MR2, MR2, MR3  ; MR2 = Ye = Ye*(2.0 - Ye*Den)
    MMPYF32   MR3, MR2, MR1  ; MR3 = Ye*Den
|| MMOV32    MR0, @_Num      ; MR0 = Num
    MSUBF32   MR3, #2.0, MR3 ; MR3 = 2.0 - Ye*Den
    MMPYF32   MR2, MR2, MR3  ; MR2 = Ye = Ye*(2.0 - Ye*Den)
|| MMOV32    MR1, @_Den      ; Reload Den To Set Sign
    MNEGF32   MR0, MR0, EQ    ; if(Den == 0.0) Change Sign Of Num
    MMPYF32   MR0, MR2, MR0    ; MR0 = Y = Ye*Num
    MMOV32    @_Dest, MR0      ; Store result
    MSTOP          ; end of task

```

See also
[MABSF32](#) [MRa](#), [MRb](#)

MNOP**No Operation****Operands**

none	This instruction does not have any operands
------	---

Opcode

LSW: 0000 0000 0000 0000
MSW: 0111 1111 1010 0000

Description

Do nothing. This instruction is used to fill required pipeline delay slots when other instructions are not available to fill the slots.

Flags

This instruction does not modify flags in the MSTF register.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; X is an array of 32-bit floating-point values
; Find the maximum value in an array X
; and store it in Result
;
_Cla1Task1:
    MMOV16    MAR1, #_X          ; Start address
    MUI16TOF32 MR0, @_len        ; Length of the array
    MNOP                  ; delay for MAR1 load
    MNOP                  ; delay for MAR1 load
    MMOV32    MR1, *MAR1[2]++   ; MR1 = X0
LOOP
    MMOV32    MR2, *MAR1[2]++   ; MR2 = next element
    MMAXF32   MR1, MR2         ; MR1 = MAX(MR1, MR2)
    MADDF32   MR0, MR0, #-1.0  ; Decrement the counter
    MCMPF32   MR0 #0.0         ; Set/clear flags for MBCNDD
    MNOP                  ; Too late to affect MBCNDD
    MNOP                  ; Too late to affect MBCNDD
    MNOP                  ; Too late to affect MBCNDD
    MBCNDD    LOOP, NEQ        ; Branch if not equal to zero
    MMOV32    @_Result, MR1     ; Always executed
    MNOP                  ; Pad to separate MBCNDD and MSTOP
    MNOP                  ; Pad to separate MBCNDD and MSTOP
    MSTOP                 ; End of task
```

See also

MOR32 MRa, MRb, MRc Bitwise OR

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
MRc	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 00cc bbba
 MSW: 0111 1100 1000 0000

Description

Bitwise OR of MRb with MRc.

`MARa(31:0) = MARb(31:0) OR MARc(31:0);`

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
NF = MARa(31);
ZF = 0;
if(MARa(31:0) == 0) { ZF = 1; }
```

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ      MR0, #0x5555 ; MR0 = 0x5555AAAA
MMOVXI      MR0, #0xAAAA

MMOVIZ      MR1, #0x5432 ; MR1 = 0x5432FEDC
MMOVXI      MR1, #0xFEDC

; 0101 OR 0101 = 0101 (5)
; 0101 OR 0100 = 0101 (5)
; 0101 OR 0011 = 0111 (7)
; 0101 OR 0010 = 0111 (7)
; 1010 OR 1111 = 1111 (F)
; 1010 OR 1110 = 1110 (E)
; 1010 OR 1101 = 1111 (F)
; 1010 OR 1100 = 1110 (E)
MOR32 MR2, MR1, MR0      ; MR3 = 0x5555FEFE
```

See also

[MAND32 MRa, MRb, MRc](#)
[MXOR32 MRa, MRb, MRc](#)

MRCNDD {CNDF} *Return Conditional Delayed***Operands**

CNDF	optional condition.
------	---------------------

Opcode

LSW: 0000 0000 0000 0000
 MSW: 0111 1001 1010 cndf

Description

If the specified condition is true, then the RPC field of MSTF is loaded into MPC and fetching continues from that location. Otherwise program fetches will continue without the return.

Please refer to the pipeline section for important information regarding this instruction.

```
if (CNDF == TRUE) MPC = RPC;
```

CNDF is one of the following conditions:

Encode ⁽⁷⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽⁸⁾	Unconditional with flag modification	None

⁽⁷⁾ Values not shown are reserved.

⁽⁸⁾ This is the default operation if no CNDF field is specified. This condition will allow the ZF and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

Flags

This instruction does not modify flags in the MSTF register.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

The MRCNDD instruction by itself is a single-cycle instruction. As shown in [Table 4-18](#), for each return 6 instruction slots are executed; three before the return instruction (d5-d7) and three after the return instruction (d8-d10). The total number of cycles for a return taken or not taken depends on the usage of these slots. That is, the number of cycles depends on how many slots are filled with a MNOP as well as which slots are filled. The effective number of cycles for a return can, therefore, range from 1 to 7 cycles. The number of cycles for a return taken may not be the same as for a return not taken.

Referring to the following code fragment and the pipeline diagrams in [Table 4-18](#) and [Table 4-19](#), the instructions before and after MRCNDD have the following properties:

```

;
;
<Instruction 1>      ; I1 Last instruction that can affect flags for
                      ; the MCCNDD operation
<Instruction 2>      ; I2 Cannot be stop, branch, call or return
<Instruction 3>      ; I3 Cannot be stop, branch, call or return
<Instruction 4>      ; I4 Cannot be stop, branch, call or return

MCCNDD _func, NEQ    ; Call to func if not equal to zero
                      ; Three instructions after MCCNDD are always
                      ; executed whether the call is taken or not
<Instruction 5>      ; I5 Cannot be stop, branch, call or return
<Instruction 6>      ; I6 Cannot be stop, branch, call or return
<Instruction 7>      ; I7 Cannot be stop, branch, call or return
<Instruction 8>      ; I8 The address of this instruction is saved
                      ; in the RPC field of the MSTF register.
                      ; Upon return this value is loaded into MPC
                      ; and fetching continues from this point.
<Instruction 9>      ; I9
<Instruction 10>     ; I10
.....
.....
_func:
<Destination 1>     ; d1 Can be any instruction
<Destination 2>     ; d2
<Destination 3>     ; d3
<Destination 4>     ; d4 Last instruction that can affect flags for
                      ; the MRCNDD operation
<Destination 5>     ; d5 Cannot be stop, branch, call or return
<Destination 6>     ; d6 Cannot be stop, branch, call or return
<Destination 7>     ; d7 Cannot be stop, branch, call or return

MRCNDD NEQ          ; Return to <Instruction 8> if not equal to zero
                      ; Three instructions after MRCNDD are always
                      ; executed whether the return is taken or not
<Destination 8>     ; d8 Cannot be stop, branch, call or return
<Destination 9>     ; d9 Cannot be stop, branch, call or return
<Destination 10>    ; d10 Cannot be stop, branch, call or return
<Destination 11>    ; d11
<Destination 12>    ; d12
.....
.....
MSTOP
.....

```

- **d4**

- d4 is the last instruction that can effect the CNDF flags for the MRCNDD instruction. The CNDF flags are tested in the D2 phase of the pipeline. That is, a decision is made whether to return or not when MRCNDD is in the D2 phase.

- There are no restrictions on the type of instruction for d4.

- **d5, d6 and d7**

- The three instructions proceeding MRCNDD can change MSTF flags but will have no effect on whether the MRCNDD instruction makes the return or not. This is

because the flag modification will occur after the D2 phase of the MRCNDD instruction.

- These instructions must not be the following: MSTOP, MDEBUGSTOP, MBCNDD, MCCNDD or MRCNDD.
- **d8, d9 and d10**
 - The three instructions following MRCNDD are always executed irrespective of whether the return is taken or not.
 - These instructions must not be the following: MSTOP, MDEBUGSTOP, MBCNDD, MCCNDD or MRCNDD.

Table 4-18. Pipeline Activity For MRCNDD, Return Not Taken

Instruction	F1	F2	D1	D2	R1	R2	E	W
d4	d4	d3	d2	d1	I7	I6	I5	
d5	d5	d4	d3	d2	d1	I7	I6	
d6	d6	d5	d4	d3	d2	d1	i7	
d7	d7	d6	d5	d4	d3	d2	d1	
MRCNDD	MRCNDD	d7	d6	d5	d4	d3	d2	
d8	d8	MRCNDD	d7	d6	d5	d4	d3	
d9	d9	d8	MRCNDD	d7	d6	d5	d4	
d10	d10	d9	d8	MRCNDD	d7	d6	d5	
d11	d11	d10	d9	d8	-	d7	d6	
d12	d12	d11	d10	d9	d8	-	d7	
etc....	d12	d11	d10	d9	d8	-	
....	d12	d11	d10	d9	d8	
....	d12	d11	d10	d9	
					d12	d11	d10	
						d12	d11	
							d12	

Table 4-19. Pipeline Activity For MRCNDD, Return Taken

Instruction	F1	F2	D1	D2	R1	R2	E	W
d4	d4	d3	d2	d1	I7	I6	I5	
d5	d5	d4	d3	d2	d1	I7	I6	
d6	d6	d5	d4	d3	d2	d1	i7	
d7	d7	d6	d5	d4	d3	d2	d1	
MRCNDD	MRCNDD	d7	d6	d5	d4	d3	d2	
d8	d8	MRCNDD	d7	d6	d5	d4	d3	
d9	d9	d8	MRCNDD	d7	d6	d5	d4	
d10	d10	d9	d8	MRCNDD	d7	d6	d5	
I8	I8	d10	d9	d8	-	d7	d6	
I9	I9	I8	d10	d9	d8	-	d7	
I10	I10	I9	I8	d10	d9	d8	-	
etc....	I10	I9	I8	d10	d9	d8	
....	I10	I9	I8	d10	d9	
....	I10	I9	I8	d10	
					I10	I9	I8	
						I10	I9	
							I10	

Example

;

See also

MBCNDD #16BitDest, CNDF
MCCNDD 16BitDest, CNDF
MMOV32 mem32, MSTF
MMOV32 MSTF, mem32

MSETFLG FLAG, VALUE Set or Clear Selected Floating-Point Status Flags**Operands**

FLAG	8 bit mask indicating which floating-point status flags to change.
VALUE	8 bit mask indicating the flag value; 0 or 1.

Opcode

LSW: FFFF FFFF VVVV VVVV
 MSW: 0111 1001 1100 0000

Description

The MSETFLG instruction is used to set or clear selected floating-point status flags in the MSTF register. The FLAG field is an 11-bit value that indicates which flags will be changed. That is, if a FLAG bit is set to 1 it indicates that flag will be changed; all other flags will not be modified. The bit mapping of the FLAG field is shown below:

reserved	RNDF32	TF	reserved	reserved	ZF	NF	LUF	LVF
8	7	6	5	4	3	2	1	0

The VALUE field indicates the value the flag should be set to; 0 or 1.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	Yes	Yes	Yes	Yes	Yes

Any flag can be modified by this instruction. The MEALLOW and RPC fields cannot be modified with this instruction.

Pipeline

This is a single-cycle instruction.

Example

To make it easier and legible, the assembler accepts a FLAG=VALUE syntax for the MSETFLG operation as shown below:

```
MSETFLG RNDF32=0, TF=0, NF=1; FLAG = 11000100; VALUE = 00XXX1XX;
```

See also

[MMOV32 mem32, MSTF](#)
[MMOV32 MSTF, mem32](#)

MSTOP
Stop Task
Operands

none	This instruction does not have any operands
------	---

Opcode

LSW: 0000 0000 0000 0000
MSW: 0111 1111 1000 0000

Description

The MSTOP instruction must be placed to indicate the end of each task. In addition, placing MSTOP in unused memory locations within the CLA program RAM can be useful for debugging and preventing run away CLA code. When MSTOP enters the D2 phase of the pipeline, the MIRUN flag for the task is cleared and the associated interrupt is flagged in the PIE vector table.

There are three special cases that can occur when single-stepping a task such that the MPC reaches the MSTOP instruction.

1. If you are single-stepping or halted in "task A" and "task B" comes in before the MPC reaches the MSTOP, then "task B" will start if you continue to step through the MSTOP instruction. Basically if "task B" is pending before the MPC reaches MSTOP in "task A" then there is no issue in "task B" starting and no special action is required.
2. In this case you have single-stepped or halted in "task A" and the MPC has reached the MSTOP with no tasks pending. If "task B" comes in at this point, it will be flagged in the MIFR register but it may or may not start if you continue to single-step through the MSTOP instruction of "task A". It depends on exactly when the new task comes in. To reliably start "task B" perform a soft reset and reconfigure the MIER bits. Once this is done, you can start single-stepping "task B".
3. Case 2 can be handled slightly differently if there is control over when "task B" comes in (for example using the IACK instruction to start the task). In this case you have single-stepped or halted in "task A" and the MPC has reached the MSTOP with no tasks pending. Before forcing "task B", run free to force the CLA out of the debug state. Once this is done you can force "task B" and continue debugging.

Restrictions

The MSTOP instruction cannot be placed 3 instructions before or after a [MBCNDD](#), [MCCNDD](#) or [MRCNDD](#) instruction.

Flags

This instruction does not modify flags in the MSTF register.

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction. [Table 4-20](#) shows the pipeline behavior of the MSTOP instruction. The MSTOP instruction cannot be placed with 3 instructions of a [MBCNDD](#), [MCCNDD](#) or [MRCNDD](#) instruction.

Table 4-20. Pipeline Activity For MSTOP

Instruction	F1	F2	D1	D2	R1	R2	E	W
I1	I1							
I2	I2	I1						
I3	I3	I2	I1					
MSTOP	MSTOP	I3	I2	I1				
I4	I4	MSTOP	I3	I2	I1			
I5	I5	I4	MSTOP	I3	I2	I1		
I6	I6	I5	I4	MSTOP	I3	I2	I1	
New Task Arbitrated and Prioritized	-	-	-	-	-	I3	I2	
New Task Arbitrated and Prioritized	-	-	-	-	-	-	I3	
I1	I1	-	-	-	-	-	-	
I2	I2	I1	-	-	-	-	-	
I3	I3	I2	I1	-	-	-	-	
I4	I4	I3	I2	I1	-	-	-	
I5	I5	I4	I3	I2	I1	-	-	
I6	I6	I5	I4	I3	I2	I1	-	
I7	I7	I6	I5	I4	I3	I2	I1	
etc								

Example

```

; Given A = (int32)1
;      B = (int32)2
;      C = (int32)-7
;
; Calculate Y2 = A - B - C
_Cla1Task3:
    MMOV32    MR0, @_A        ; MR0 = 1 (0x00000001)
    MMOV32    MR1, @_B        ; MR1 = 2 (0x00000002)
    MMOV32    MR2, @_C        ; MR2 = -7 (0xFFFFFFF9)
    MSUB32    MR3, MR0, MR1 ; A + B
    MSUB32    MR3, MR3, MR2 ; A + B + C = 6 (0x00000006)
    MMOV32    @_Y2, MR3       ; Store y2
    MSTOP
                                ; End of task

```

See also[MDEBUGSTOP](#)

MSUB32 MRa, MRb, MRc 32-Bit Integer Subtraction

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point destination register (MR0 to MR3)
MRc	CLA floating-point destination register (MR0 to MR3)

Opcode

LSW: 0000 0000 00cc bbba
 MSW: 0111 1100 1110 0000

Description

32-bit integer addition of MRb and MRc.

`MRA(31:0) = MRB(31:0) - MRC(31:0);`

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified as follows:

```
NF = MRA(31);
ZF = 0;
if(MRA(31:0) == 0) { ZF = 1; }
```

Pipeline

This is a single-cycle instruction.

Example

```
; Given A = (int32)1
;           B = (int32)2
;           C = (int32)-7
;
;
Calculate Y2 = A - B - C
;
_Cla1Task3:
    MMOV32    MR0, @_A          ; MR0 = 1 (0x00000001)
    MMOV32    MR1, @_B          ; MR1 = 2 (0x00000002)
    MMOV32    MR2, @_C          ; MR2 = -7 (0xFFFFFFF9)
    MSUB32    MR3, MR0, MR1    ; A + B
    MSUB32    MR3, MR3, MR2    ; A + B + C = 6 (0x00000006)
    MMOV32    @_y2, MR3        ; Store y2
    MSTOP                                ; End of task
```

See also

[MADD32 MRa, MRb, MRc](#)
[MAND32 MRa, MRb, MRc](#)
[MASR32 MRa, #SHIFT](#)
[MLSL32 MRa, #SHIFT](#)
[MLSR32 MRa, #SHIFT](#)
[MOR32 MRa, MRb, MRc](#)
[MXOR32 MRa, MRb, MRc](#)

MSUBF32 MRa, MRb, MRc 32-Bit Floating-Point Subtraction**Operands**

MRa	CLA floating-point destination register (MR0 to R1)
MRb	CLA floating-point source register (MR0 to R1)
MRc	CLA floating-point source register (MR0 to R1)

Opcode

LSW: 0000 0000 00cc bbba
 MSW: 0111 1100 0100 0000

Description

Subtract the contents of two floating-point registers

MRa = MRb - MRc;

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MSUBF32 generates an underflow condition.
- LVF = 1 if MSUBF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example

```
; Given A, B and C are 32-bit floating-point numbers
; Calculate Y2 = A + B - C
;
_Cla1Task5:
  MMOV32    MR0, @_A      ; Load MR0 with A
  MMOV32    MR1, @_B      ; Load MR1 with B
  MADDF32   MR0, MR1, MR0 ; Add A + B
  || MMOV32    MR1, @_C      ; and in parallel load C
  MSUBF32   MR0, MR0, MR1 ; Subtract C from (A + B)
  MMOV32    @Y, MR0       ; (A+B) - C
  MSTOP                                ; end of task
```

See also

[MSUBF32 MRa, #16FHi, MRb](#)
[MSUBF32 MRd, MRe, MRf || MMOV32 MRa, mem32](#)
[MSUBF32 MRd, MRe, MRf || MMOV32 mem32, MRa](#)
[MMPYF32 MRa, MRb, MRc || MSUBF32 MRd, MRe, MRf](#)

MSUBF32 MRa, #16FHi, MRb 32-Bit Floating-Point Subtraction

Operands

MRa	CLA floating-point destination register (MR0 to R1)
#16FHi	A 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0.
MRb	CLA floating-point source register (MR0 to R1)

Opcode

LSW: IIII IIII IIII IIII
MSW: 0111 1000 0000 baaa

Description

Subtract MRb from the floating-point value represented by the immediate operand. Store the result of the addition in MRa.

#16FHi is a 16-bit immediate value that represents the upper 16-bits of an IEEE 32-bit floating-point value. The low 16-bits of the mantissa are assumed to be all 0. #16FHi is most useful for representing constants where the lowest 16-bits of the mantissa are 0. Some examples are 2.0 (0x40000000), 4.0 (0x40800000), 0.5 (0x3F000000), and -1.5 (0xBFC00000). The assembler will accept either a hex or float as the immediate value. That is, the value -1.5 can be represented as #-1.5 or #0xBFC0.

MRa = #16FHi:0 - MRb;

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MSUBF32 generates an underflow condition.
- LVF = 1 if MSUBF32 generates an overflow condition.

Pipeline

This is a single-cycle instruction.

Example

```
; Y = sqrt(X)
; Ye = Estimate(1/sqrt(X));
; Ye = Ye*(1.5 - Ye*Ye*X*0.5)
; Ye = Ye*(1.5 - Ye*Ye*X*0.5)
; Y = X*Ye
;
_Cla1Task3:
    MMOV32      MR0, @_x           ; MR0 = X
    MEISQRTF32  MR1, MR0          ; MR1 = Ye = Estimate(1/sqrt(X))
    MMOV32      MR1, @_x, EQ       ; if(X == 0.0) Ye = 0.0
    MMPYF32     MR3, MR0, #0.5     ; MR3 = X*0.5
    MMPYF32     MR2, MR1, MR3      ; MR2 = Ye*X*0.5
    MMPYF32     MR2, MR1, MR2      ; MR2 = Ye*Ye*X*0.5
    MSUBF32     MR2, #1.5, MR2     ; MR2 = 1.5 - Ye*Ye*X*0.5
    MMPYF32     MR1, MR1, MR2      ; MR1 = Ye = Ye*(1.5 - Ye*Ye*X*0.5)
    MMPYF32     MR2, MR1, MR3      ; MR2 = Ye*X*0.5
    MMPYF32     MR2, MR1, MR2      ; MR2 = Ye*Ye*X*0.5
    MSUBF32     MR2, #1.5, MR2     ; MR2 = 1.5 - Ye*Ye*X*0.5
    MMPYF32     MR1, MR1, MR2      ; MR1 = Ye = Ye*(1.5 - Ye*Ye*X*0.5)
    MMPYF32     MR0, MR1, MR0      ; MR0 = Y = Ye*X
    MMOV32      @_y, MR0          ; Store Y = sqrt(X)
    MSTOP
```

; end of task

See also

[MSUBF32 MRa, MRb, MRc](#)
[MSUBF32 MRd, MRe, MRF || MMOV32 MRa, mem32](#)
[MSUBF32 MRd, MRe, MRF || MMOV32 mem32, MRa](#)
[MMPYF32 MRa, MRb, MRc || MSUBF32 MRd, MRe, MRF](#)

MSUBF32 MRd, MRe, MRf ||MMOV32 MRa, mem32 32-Bit Floating-Point Subtraction with Parallel Move

Operands

MRd	CLA floating-point destination register (MR0 to MR3) for the MSUBF32 operation MRd cannot be the same register as MRa
MRe	CLA floating-point source register (MR0 to MR3) for the MSUBF32 operation
MRf	CLA floating-point source register (MR0 to MR3) for the MSUBF32 operation
MRa	CLA floating-point destination register (MR0 to MR3) for the MMOV32 operation MRa cannot be the same register as MRd
mem32	32-bit memory location accessed using one of the available addressing modes. Source for the MMOV32 operation.

Opcode

LSW: mmmm mmmm mmmm mmmm
MSW: 0010 ffee ddaa addr

Description

Subtract the contents of two floating-point registers and move from memory to a floating-point register.

```
MRd = MRe - MRf;
MRa = [mem32];
```

Restrictions

The destination register for the MSUBF32 and the MMOV32 must be unique. That is, MRa cannot be the same register as MRd.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MSUBF32 generates an underflow condition.
- LVF = 1 if MSUBF32 generates an overflow condition.

The MMOV32 Instruction will set the NF and ZF flags as follows:

Pipeline

Both MSUBF32 and MMOV32 complete in a single cycle.

Example

```
NF = MRa(31);
ZF = 0;
if(MRa(30:23) == 0) { ZF = 1; NF = 0; }
```

See also

[MSUBF32 MRa, MRb, MRc](#)
[MSUBF32 MRa, #16FHi, MRb](#)
[MMPYF32 MRa, MRb, MRc || MSUBF32 MRd, MRe, MRf](#)

MSUBF32 MRd, MRe, MRf || MMOV32 mem32, MRa 32-Bit Floating-Point Subtraction with Parallel Move

Operands

MRd	CLA floating-point destination register (MR0 to MR3) for the MSUBF32 operation
MRe	CLA floating-point source register (MR0 to MR3) for the MSUBF32 operation
MRf	CLA floating-point source register (MR0 to MR3) for the MSUBF32 operation
mem32	32-bit destination memory location for the MMOV32 operation
MRa	CLA floating-point source register (MR0 to MR3) for the MMOV32 operation

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0110 ffee ddःaddr

Description

Subtract the contents of two floating-point registers and move from a floating-point register to memory.

```
MRd = MRe - MRf ;
[ mem32 ] = MRa ;
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	Yes	Yes

The MSTF register flags are modified as follows:

- LUF = 1 if MSUBF32 generates an underflow condition.
- LVF = 1 if MSUBF32 generates an overflow condition.

Pipeline

Both MSUBF32 and MMOV32 complete in a single cycle.

Example

MSUBF32 MRa, MRb, MRc
 MSUBF32 MRa, #16FHi, MRb

MSUBF32 MRd, MRe, MRf || MMOV32 MRa, mem32
 MMPYF32 MRa, MRb, MRc || MSUBF32 MRd, MRe, MRf

See also

MSWAPF MRa, MRb {, CNDF} Conditional Swap**Operands**

MRa	CLA floating-point register (MR0 to MR3)
MRb	CLA floating-point register (MR0 to MR3)
CNDF	Optional condition tested based on the MSTF flags

Opcode

LSW: 0000 0000 CNDF bbba
 MSW: 0111 1011 0000 0000

Description

Conditional swap of MRa and MRb.

```
if (CNDF == true) swap MRa and MRb;
```

CNDF is one of the following conditions:

Encode ⁽¹⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽²⁾	Unconditional with flag modification	None

⁽¹⁾ Values not shown are reserved.

⁽²⁾ This is the default operation if no CNDF field is specified. This condition will allow the ZF and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

No flags affected

Pipeline

This is a single-cycle instruction.

Example

```
; X is an array of 32-bit floating-point values
; and has len elements. Find the maximum value in
; the array and store it in Result
;
; Note: MCMPF32 and MSWAPF can be replaced by MMAXF32
;
_Cla1Task1:
    MMOVI16    MAR1, #_X          ; Start address
    MUI16TOF32 MR0, @_len        ; Length of the array
    MNOP
    MNOP
    MMOV32     MR1, *MAR1[2]++   ; MR1 = X0
LOOP
    MMOV32     MR2, *MAR1[2]++   ; MR2 = next element
    MCMPF32    MR2, MR1          ; Compare MR2 with MR1
    MSWAPF    MR1, MR2, GT       ; MR1 = MAX(MR1, MR2)
    MADDF32    MR0, MR0, #-1.0   ; Decrement the counter
    MCMPF32    MR0 #0.0         ; Set/clear flags for MBCNDD
    MNOP
    MNOP
    MNOP
    MBCNDD    LOOP, NEQ          ; Branch if not equal to zero
    MMOV32    @_Result, MR1      ; Always executed
    MNOP
    MNOP
    MNOP
    MSTOP      ; End of task
```

See also

MMTESTTF CNDF *Test MSTF Register Flag Condition***Operands**

CNDF	condition to test based on MSTF flags
------	---------------------------------------

Opcode

LSW: 0000 0000 0000 cndf
 MSW: 0111 1111 0100 0000

Description

Test the CLA floating-point condition and if true, set the MSTF[TF] flag. If the condition is false, clear the MSTF[TF] flag. This is useful for temporarily storing a condition for later use.

```
if (CNDF == true) TF = 1;
else TF = 0;
```

CNDF is one of the following conditions:

Encode ⁽³⁾	CNDF	Description	MSTF Flags Tested
0000	NEQ	Not equal to zero	ZF == 0
0001	EQ	Equal to zero	ZF == 1
0010	GT	Greater than zero	ZF == 0 AND NF == 0
0011	GEQ	Greater than or equal to zero	NF == 0
0100	LT	Less than zero	NF == 1
0101	LEQ	Less than or equal to zero	ZF == 1 OR NF == 1
1010	TF	Test flag set	TF == 1
1011	NTF	Test flag not set	TF == 0
1100	LU	Latched underflow	LUF == 1
1101	LV	Latched overflow	LVF == 1
1110	UNC	Unconditional	None
1111	UNCF ⁽⁴⁾	Unconditional with flag modification	None

⁽³⁾ Values not shown are reserved.

⁽⁴⁾ This is the default operation if no CNDF field is specified. This condition will allow the ZF and NF flags to be modified when a conditional operation is executed. All other conditions will not modify these flags.

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	Yes	No	No	No	No

```
TF = 0;
if (CNDF == true) TF = 1;
```

Note: If (CNDF == UNC or UNCF), the TF flag will be set to 1.

Pipeline

This is a single-cycle instruction.

Example

```

; if (State == 0.1)
;   RampState = RampState || RAMPMASK
; else if (State == 0.01)
;   CoastState = CoastState || COASTMASK
; else
;   SteadyState = SteadyState || STEADYMASK
;
_Cla1Task2:
    MMOV32    MR0, @_State
    MCMPF32   MR0, #0.1      ; Affects flags for 1st MBCNDD (A)
    MCMPF32   MR0, #0.01     ; Check used by 2nd MBCNDD (B)
    MMTESTTF  EQ             ; Store EQ flag in TF for 2nd MBCNDD (B)
    MNOP
    MBCNDD    _Skip1, NEQ    ; (A) If State != 0.1, go to Skip1
    MMOV32    MR1, @_RampState ; Always executed
    MMOVXI   MR2, #RAMPMASK  ; Always executed
    MOR32    MR1, MR2        ; Always executed
    MMOV32    @_RampState, MR1 ; Execute if (A) branch not taken
    MSTOP                  ; end of task if (A) branch not taken

_Skip1:
    MMOV32    MR3, @_SteadyState
    MMOVXI   MR2, #STEADYMASK
    MOR32    MR3, MR2
    MBCNDD    _Skip2, NTF    ; (B) if State != .01, go to Skip2
    MMOV32    MR1, @_CoastState ; Always executed
    MMOVXI   MR2, #COASTMASK  ; Always executed
    MOR32    MR1, MR2        ; Always executed
    MMOV32    @_CoastState, MR1 ; Execute if (B) branch not taken
    MSTOP                  ; end of task if (B) branch not taken

_Skip2:
    MMOV32 @_SteadyState, MR3  ; Executed if (B) branch taken
    MSTOP

```

See also

MUI16TOF32 MRa, mem16 Convert Unsigned 16-Bit Integer to 32-Bit Floating-Point Value**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
mem16	16-bit source memory location

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0101 01aa addr

Description

When converting F32 to I16/UI16 data format, the MF32TOI16/UI16 operation truncates to zero while the MF32TOI16R/UI16R operation will round to nearest (even) value.

MRa = UI16TOF32[mem16];

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

[MF32TOI16 MRa, MRb](#)
[MF32TOI16R MRa, MRb](#)
[MF32TOUI16 MRa, MRb](#)
[MF32TOUI16R MRa, MRb](#)
[MI16TOF32 MRa, MRb](#)
[MI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, MRb](#)

See also

MUI16TOF32 MRa, MRb Convert Unsigned 16-Bit Integer to 32-Bit Floating-Point Value

Operands

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
 MSW: 0111 1110 1110 0000

Description

Convert an unsigned 16-bit integer to a 32-bit floating-point value. When converting float32 to I16/UI16 data format, the MF32TOI16/UI16 operation truncates to zero while the MF32TOI16R/UI16R operation will round to nearest (even) value.

MRa = UI16TOF32[MRb];

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
MMOVXI MR1, #0x800F ; MR1(15:0) = 32783 (0x800F)
MUI16TOF32 MR0, MR1 ; MR0 = UI16TOF32 (MR1(15:0))
; = 32783.0 (0x47000F00)
```

See also

[MF32TOI16 MRa, MRb](#)
[MF32TOI16R MRa, MRb](#)
[MF32TOUI16 MRa, MRb](#)
[MF32TOUI16R MRa, MRb](#)
[MI16TOF32 MRa, MRb](#)
[MI16TOF32 MRa, mem16](#)
[MUI16TOF32 MRa, mem16](#)

MUI32TOF32 MRa, mem32 Convert Unsigned 32-Bit Integer to 32-Bit Floating-Point Value**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
mem32	32-bit memory location accessed using one of the available addressing modes

Opcode

LSW: mmmm mmmm mmmm mmmm
 MSW: 0111 0100 10aa addr

Description

MRa = UI32TOF32[mem32];

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
; Given x2, m2 and b2 are Uint32 numbers:  

;  

; x2 = Uint32(2) = 0x00000002  

; m2 = Uint32(1) = 0x00000001  

; b2 = Uint32(3) = 0x00000003  

;  

; Calculate y2 = x2 * m2 + b2  

;  

_ClalTask1:  

  MUI32TOF32  MR0, @_m2      ; MR0 = 1.0 (0x3F800000)  

  MUI32TOF32  MR1, @_x2      ; MR1 = 2.0 (0x40000000)  

  MUI32TOF32  MR2, @_b2      ; MR2 = 3.0 (0x40400000)  

  MMPYF32     MR3, MR0, MR1  ; M*X  

  MADDF32     MR3, MR2, MR3  ; Y=MX+B = 5.0 (0x40A00000)  

  MF32TOUI32   MR3, MR3      ; Y = Uint32(5.0) = 0x00000005  

  MMOV32      @_y2, MR3      ; store result  

  MSTOP          ; end of task
```

See also

[MF32TOI32 MRa, MRb](#)
[MF32TOU32 MRa, MRb](#)
[MI32TOF32 MRa, mem32](#)
[MI32TOF32 MRa, MRb](#)
[MUI32TOF32 MRa, MRb](#)

MUI32TOF32 MRa, MRb Convert Unsigned 32-Bit Integer to 32-Bit Floating-Point Value**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 0000 bbba
MSW: 0111 1101 1100 0000

Description

MRa = UI32TOF32 [MRb];

Flags

This instruction does not affect any flags:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	No	No	No	No

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ      MR3, #0x8000 ; MR3(31:16) = 0x8000
MMOVXI      MR3, #0x1111 ; MR3(15:0) = 0x1111
              ; MR3 = 2147488017
MUI32TOF32  MR3, MR3     ; MR3 = MUI32TOF32 (MR3) = 2147488017.0 (0x4F000011)
```

See also

[MF32TOI32 MRa, MRb](#)
[MF32TOUI32 MRa, MRb](#)
[MI32TOF32 MRa, mem32](#)
[MI32TOF32 MRa, MRb](#)
[MUI32TOF32 MRa, mem32](#)

MXOR32 MRa, MRb, MRc Bitwise Exclusive Or**Operands**

MRa	CLA floating-point destination register (MR0 to MR3)
MRb	CLA floating-point source register (MR0 to MR3)
MRc	CLA floating-point source register (MR0 to MR3)

Opcode

LSW: 0000 0000 00cc bbba
 MSW: 0111 1100 1010 0000

Description

Bitwise XOR of MRb with MRc.

```
MRa(31:0) = MRb(31:0) XOR MRc(31:0);
```

Flags

This instruction modifies the following flags in the MSTF register:

Flag	TF	ZF	NF	LUF	LVF
Modified	No	Yes	Yes	No	No

The MSTF register flags are modified based on the integer results of the operation.

```
NF = MRa(31);
ZF = 0;
if(MRa(31:0) == 0) { ZF = 1; }
```

Pipeline

This is a single-cycle instruction.

Example

```
MMOVIZ MR0, #0x5555      ; MR0 = 0x5555AAAA
MMOVXI MR0, #0xAAAA

MMOVIZ MR1, #0x5432      ; MR1 = 0x5432FEDC
MMOVXI MR1, #0xFEDC

; 0101 XOR 0101 = 0000 (0)
; 0101 XOR 0100 = 0001 (1)
; 0101 XOR 0011 = 0110 (6)
; 0101 XOR 0010 = 0111 (7)
; 1010 XOR 1111 = 0101 (5)
; 1010 XOR 1110 = 0100 (4)
; 1010 XOR 1101 = 0111 (7)
; 1010 XOR 1100 = 0110 (6)

MXOR32 MR2, MR1, MR0    ; MR3 = 0x01675476
```

See also

[MAND32 MRa, MRb, MRc](#)
[MOR32 MRa, MRb, MRc](#)

4.6 Registers

4.6.1 CLA Base Addresses

Table 4-21. CLA Base Address Table

Device Register	Register Name	Start Address	End Address
Cla1Regs	CLA_REGS	0x0000_1400	0x0000_147F

4.6.2 CLA Registers

Table 4-22 lists the memory-mapped registers for the CLA. All register offset addresses not listed in Table 4-22 should be considered as reserved locations and the register contents should not be modified.

Table 4-22. CLA REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	MVECT1	Task Interrupt Vector	Section 4.6.2.1	
1h	MVECT2	Task Interrupt Vector	Section 4.6.2.2	
2h	MVECT3	Task Interrupt Vector	Section 4.6.2.3	
3h	MVECT4	Task Interrupt Vector	Section 4.6.2.4	
4h	MVECT5	Task Interrupt Vector	Section 4.6.2.5	
5h	MVECT6	Task Interrupt Vector	Section 4.6.2.6	
6h	MVECT7	Task Interrupt Vector	Section 4.6.2.7	
7h	MVECT8	Task Interrupt Vector	Section 4.6.2.8	
10h	MCTL	Control Register	Section 4.6.2.9	
20h	MIFR	Interrupt Flag Register	Section 4.6.2.10	
21h	MIOVF	Interrupt Overflow Flag Register	Section 4.6.2.11	
22h	MIFRC	Interrupt Force Register	Section 4.6.2.12	
23h	MICLR	Interrupt Flag Clear Register	Section 4.6.2.13	
24h	MICLROVF	Interrupt Overflow Flag Clear Register	Section 4.6.2.14	
25h	MIER	Interrupt Enable Register	Section 4.6.2.15	
26h	MIRUN	Interrupt Run Status Register	Section 4.6.2.16	
28h	_MPC	CLA Program Counter	Section 4.6.2.17	
2Ah	_MAR0	CLA Auxiliary Register 0	Section 4.6.2.18	
2Bh	_MAR1	CLA Auxiliary Register 1	Section 4.6.2.19	
2Ch	_MSTF	CLA Floating-Point Status Register	Section 4.6.2.20	
2Eh	_MR0	CLA Floating-Point Result Register 0	Section 4.6.2.21	
32h	_MR1	CLA Floating-Point Result Register 1	Section 4.6.2.22	
36h	_MR2	CLA Floating-Point Result Register 2	Section 4.6.2.23	
3Ah	_MR3	CLA Floating-Point Result Register 3	Section 4.6.2.24	

4.6.2.1 MVECT1 Register (offset = 0h) [reset = 0h]

MVECT1 is shown in [Figure 4-2](#) and described in [Table 4-23](#).

Each CLA interrupt has its own interrupt vector (MVECT1 to MVECT8). This interrupt vector points to the first instruction of the associated task. When a task begins, the CLA will start fetching instructions at the location indicated by the appropriate MVECT register .

Figure 4-2. MVECT1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MVECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-23. MVECT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MVECT	R/W	0h	<p>MPC Start Address: These bits specify the start address for the given interrupt (task). The address range of the CLA with a 16-bit MVECT is 64Kx16 words or 32K MCLA instructions.</p> <p>There is one MVECT register per interrupt (task). Interrupt 1 uses MVECT1, interrupt 2 uses MVECT2 and so forth.</p> <p>Note: While the CLA is running or executing a task, the CPU can change the MVECT values..</p>

4.6.2.2 MVECT2 Register (offset = 1h) [reset = 0h]

MVECT2 is shown in [Figure 4-3](#) and described in [Table 4-24](#).

Each CLA interrupt has its own interrupt vector (MVECT1 to MVECT8). This interrupt vector points to the first instruction of the associated task. When a task begins, the CLA will start fetching instructions at the location indicated by the appropriate MVECT register .

Figure 4-3. MVECT2 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MVECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-24. MVECT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MVECT	R/W	0h	<p>MPC Start Address: These bits specify the start address for the given interrupt (task). The address range of the CLA with a 16-bit MVECT is 64Kx16 words or 32K MCLA instructions.</p> <p>There is one MVECT register per interrupt (task). Interrupt 1 uses MVECT1, interrupt 2 uses MVECT2 and so forth.</p> <p>Note: While the CLA is running or executing a task, the CPU can change the MVECT values..</p>

4.6.2.3 MVECT3 Register (offset = 2h) [reset = 0h]

MVECT3 is shown in [Figure 4-4](#) and described in [Table 4-25](#).

Each CLA interrupt has its own interrupt vector (MVECT1 to MVECT8). This interrupt vector points to the first instruction of the associated task. When a task begins, the CLA will start fetching instructions at the location indicated by the appropriate MVECT register .

Figure 4-4. MVECT3 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MVECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-25. MVECT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MVECT	R/W	0h	<p>MPC Start Address: These bits specify the start address for the given interrupt (task). The address range of the CLA with a 16-bit MVECT is 64Kx16 words or 32K MCLA instructions.</p> <p>There is one MVECT register per interrupt (task). Interrupt 1 uses MVECT1, interrupt 2 uses MVECT2 and so forth.</p> <p>Note: While the CLA is running or executing a task, the CPU can change the MVECT values..</p>

4.6.2.4 MVECT4 Register (offset = 3h) [reset = 0h]

MVECT4 is shown in [Figure 4-5](#) and described in [Table 4-26](#).

Each CLA interrupt has its own interrupt vector (MVECT1 to MVECT8). This interrupt vector points to the first instruction of the associated task. When a task begins, the CLA will start fetching instructions at the location indicated by the appropriate MVECT register .

Figure 4-5. MVECT4 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MVECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-26. MVECT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MVECT	R/W	0h	<p>MPC Start Address: These bits specify the start address for the given interrupt (task). The address range of the CLA with a 16-bit MVECT is 64Kx16 words or 32K MCLA instructions.</p> <p>There is one MVECT register per interrupt (task). Interrupt 1 uses MVECT1, interrupt 2 uses MVECT2 and so forth.</p> <p>Note: While the CLA is running or executing a task, the CPU can change the MVECT values..</p>

4.6.2.5 MVECT5 Register (offset = 4h) [reset = 0h]

MVECT5 is shown in [Figure 4-6](#) and described in [Table 4-27](#).

Each CLA interrupt has its own interrupt vector (MVECT1 to MVECT8). This interrupt vector points to the first instruction of the associated task. When a task begins, the CLA will start fetching instructions at the location indicated by the appropriate MVECT register .

Figure 4-6. MVECT5 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MVECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-27. MVECT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MVECT	R/W	0h	<p>MPC Start Address: These bits specify the start address for the given interrupt (task). The address range of the CLA with a 16-bit MVECT is 64Kx16 words or 32K MCLA instructions.</p> <p>There is one MVECT register per interrupt (task). Interrupt 1 uses MVECT1, interrupt 2 uses MVECT2 and so forth.</p> <p>Note: While the CLA is running or executing a task, the CPU can change the MVECT values..</p>

4.6.2.6 MVECT6 Register (offset = 5h) [reset = 0h]

MVECT6 is shown in [Figure 4-7](#) and described in [Table 4-28](#).

Each CLA interrupt has its own interrupt vector (MVECT1 to MVECT8). This interrupt vector points to the first instruction of the associated task. When a task begins, the CLA will start fetching instructions at the location indicated by the appropriate MVECT register .

Figure 4-7. MVECT6 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MVECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-28. MVECT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MVECT	R/W	0h	<p>MPC Start Address: These bits specify the start address for the given interrupt (task). The address range of the CLA with a 16-bit MVECT is 64Kx16 words or 32K MCLA instructions.</p> <p>There is one MVECT register per interrupt (task). Interrupt 1 uses MVECT1, interrupt 2 uses MVECT2 and so forth.</p> <p>Note: While the CLA is running or executing a task, the CPU can change the MVECT values..</p>

4.6.2.7 MVECT7 Register (offset = 6h) [reset = 0h]

MVECT7 is shown in [Figure 4-8](#) and described in [Table 4-29](#).

Each CLA interrupt has its own interrupt vector (MVECT1 to MVECT8). This interrupt vector points to the first instruction of the associated task. When a task begins, the CLA will start fetching instructions at the location indicated by the appropriate MVECT register .

Figure 4-8. MVECT7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MVECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-29. MVECT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MVECT	R/W	0h	<p>MPC Start Address: These bits specify the start address for the given interrupt (task). The address range of the CLA with a 16-bit MVECT is 64Kx16 words or 32K MCLA instructions.</p> <p>There is one MVECT register per interrupt (task). Interrupt 1 uses MVECT1, interrupt 2 uses MVECT2 and so forth.</p> <p>Note: While the CLA is running or executing a task, the CPU can change the MVECT values..</p>

4.6.2.8 MVECT8 Register (offset = 7h) [reset = 0h]

MVECT8 is shown in [Figure 4-9](#) and described in [Table 4-30](#).

Each CLA interrupt has its own interrupt vector (MVECT1 to MVECT8). This interrupt vector points to the first instruction of the associated task. When a task begins, the CLA will start fetching instructions at the location indicated by the appropriate MVECT register .

Figure 4-9. MVECT8 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MVECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-30. MVECT8 Register Field Descriptions

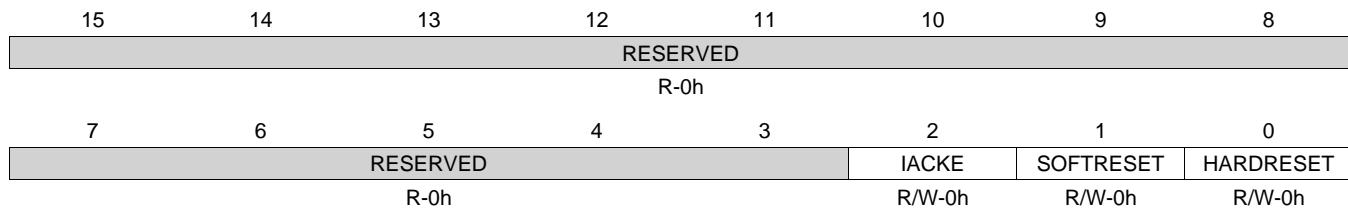
Bit	Field	Type	Reset	Description
15-0	MVECT	R/W	0h	<p>MPC Start Address: These bits specify the start address for the given interrupt (task). The address range of the CLA with a 16-bit MVECT is 64Kx16 words or 32K MCLA instructions.</p> <p>There is one MVECT register per interrupt (task). Interrupt 1 uses MVECT1, interrupt 2 uses MVECT2 and so forth.</p> <p>Note: While the CLA is running or executing a task, the CPU can change the MVECT values..</p>

4.6.2.9 MCTL Register (offset = 10h) [reset = 0h]

MCTL is shown in [Figure 4-10](#) and described in [Table 4-31](#).

Control Register

Figure 4-10. MCTL Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-31. MCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2	IACKE	R/W	0h	<p>IACK enable</p> <p>0h (R/W) = The CLA ignores the IACK instruction. (default)</p> <p>1h (R/W) = Enable the main CPU to use the IACK #16bit instruction to set MIFR bits in the same manner as writing to the MIFRC register. Each bit in the operand, #16bit, corresponds to a bit in the MIFRC register. Using IACK has the advantage of not having to first set the EALLOW bit. This allows the main CPU to efficiently trigger a CLA task through software.</p> <p>Examples IACK #0x0001 Write a 1 to MIFRC bit 0 to force task 1</p> <p>IACK #0x0003 Write a 1 to MIFRC bit 0 and 1 to force task 1 and task 2</p>
1	SOFTRESET	R/W	0h	<p>Soft Reset</p> <p>0h (R/W) = This bit always reads back 0 and writes of 0 are ignored.</p> <p>1h (R/W) = Writing a 1 will cause a soft reset of the CLA. This will stop the current task, clear the MIRUN flag and clear all bits in the MIER register. After a soft reset you must wait at least 1 SYSCLKOUT cycle before reconfiguring the MIER bits. If these two operations are done back-to-back then the MIER bits will not get set.</p>
0	HARDRESET	R/W	0h	<p>Hard Reset</p> <p>0h (R/W) = This bit always reads back 0 and writes of 0 are ignored.</p> <p>1h (R/W) = Writing a 1 will cause a hard reset of the CLA. This will set all CLA registers to their default state.</p>

4.6.2.10 MIFR Register (offset = 20h) [reset = 0h]

MIFR is shown in [Figure 4-11](#) and described in [Table 4-32](#).

Each bit in the interrupt flag register corresponds to a CLA task. The corresponding bit is automatically set when the task request is received from the peripheral interrupt. The bit can also be set by the main CPU writing to the MIFRC register or using the IACK instruction to start the task. To use the IACK instruction to begin a task first enable this feature in the MCTL register. If the bit is already set when a new peripheral interrupt is received, then the corresponding overflow bit will be set in the MIOVF register.

The corresponding MIFR bit is automatically cleared when the task begins execution. This will occur if the interrupt is enabled in the MIER register and no other higher priority task is pending. The bits can also be cleared manually by writing to the MICLR register. Writes to the MIFR register are ignored.

Figure 4-11. MIFR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-32. MIFR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	INT8	R	0h	Task 8 Interrupt Flag 0h (R/W) = TASK_FLAG_DISABLE Task 8 interrupt is currently not flagged (default) 1h (R/W) = TASK_FLAG_ENABLE Task 8 interrupt has been received and is pending execution
6	INT7	R	0h	Task 7 Interrupt Flag 0h (R/W) = TASK_FLAG_DISABLE Task 7 interrupt is currently not flagged (default) 1h (R/W) = TASK_FLAG_ENABLE Task 7 interrupt has been received and is pending execution
5	INT6	R	0h	Task 6 Interrupt Flag 0h (R/W) = TASK_FLAG_DISABLE Task 6 interrupt is currently not flagged (default) 1h (R/W) = TASK_FLAG_ENABLE Task 6 interrupt has been received and is pending execution
4	INT5	R	0h	Task 5 Interrupt Flag 0h (R/W) = TASK_FLAG_DISABLE Task 5 interrupt is currently not flagged (default) 1h (R/W) = TASK_FLAG_ENABLE Task 5 interrupt has been received and is pending execution
3	INT4	R	0h	Task 4 Interrupt Flag 0h (R/W) = TASK_FLAG_DISABLE Task 4 interrupt is currently not flagged (default) 1h (R/W) = TASK_FLAG_ENABLE Task 4 interrupt has been received and is pending execution

Table 4-32. MIFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT3	R	0h	Task 3 Interrupt Flag 0h (R/W) = TASK_FLAG_DISABLE Task 3 interrupt is currently not flagged (default) 1h (R/W) = TASK_FLAG_ENABLE Task 3 interrupt has been received and is pending execution
1	INT2	R	0h	Task 2 Interrupt Flag 0h (R/W) = TASK_FLAG_DISABLE Task 2 interrupt is currently not flagged (default) 1h (R/W) = TASK_FLAG_ENABLE Task 2 interrupt has been received and is pending execution
0	INT1	R	0h	Task 1 Interrupt Flag 0h (R/W) = TASK_FLAG_DISABLE Task 1 interrupt is currently not flagged (default) 1h (R/W) = TASK_FLAG_ENABLE Task 1 interrupt has been received and is pending execution

4.6.2.11 MIOVF Register (offset = 21h) [reset = 0h]

MIOVF is shown in Figure 4-12 and described in Table 4-33.

Each bit in the overflow flag register corresponds to a CLA task. The bit is set when an interrupt overflow event has occurred for the specific task. An overflow event occurs when the MIFR register bit is already set when a new interrupt is received from a peripheral source. The MIOVF bits are only affected by peripheral interrupt events. They do not respond to a task request by the main CPU IACK instruction or by directly setting MIFR bits. The overflow flag will remain latched and can only be cleared by writing to the overflow flag clear (MCLROVF) register. Writes to the MIOVF register are ignored.

Figure 4-12. MIOVF Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-33. MIOVF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	INT8	R	0h	Task 8 Interrupt Overflow Flag 0h (R/W) = A task 8 interrupt overflow has not occurred (default) 1h (R/W) = A task 8 interrupt overflow has occurred
6	INT7	R	0h	Task 7 Interrupt Overflow Flag 0h (R/W) = A task 7 interrupt overflow has not occurred (default) 1h (R/W) = A task 7 interrupt overflow has occurred
5	INT6	R	0h	Task 6 Interrupt Overflow Flag 0h (R/W) = A task 6 interrupt overflow has not occurred (default) 1h (R/W) = A task 6 interrupt overflow has occurred
4	INT5	R	0h	Task 5 Interrupt Overflow Flag 0h (R/W) = A task 5 interrupt overflow has not occurred (default) 1h (R/W) = A task 5 interrupt overflow has occurred
3	INT4	R	0h	Task 4 Interrupt Overflow Flag 0h (R/W) = A task 4 interrupt overflow has not occurred (default) 1h (R/W) = A task 4 interrupt overflow has occurred
2	INT3	R	0h	Task 3 Interrupt Overflow Flag 0h (R/W) = A task 3 interrupt overflow has not occurred (default) 1h (R/W) = A task 3 interrupt overflow has occurred
1	INT2	R	0h	Task 2 Interrupt Overflow Flag 0h (R/W) = A task 2 interrupt overflow has not occurred (default) 1h (R/W) = A task 2 interrupt overflow has occurred
0	INT1	R	0h	Task 1 Interrupt Overflow Flag 0h (R/W) = A task 1 interrupt overflow has not occurred (default) 1h (R/W) = A task 1 interrupt overflow has occurred

4.6.2.12 MIFRC Register (offset = 22h) [reset = 0h]

MIFRC is shown in [Figure 4-13](#) and described in [Table 4-34](#).

The interrupt force register can be used by the main CPU to start tasks through software. Writing a 1 to a MIFRC bit will set the corresponding bit in the MIFR register. Writes of 0 are ignored and reads always return 0. The IACK #16bit operation can also be used to start tasks and has the same effect as the MIFRC register. To enable IACK to set MIFR bits you must first set the MCTL[IACKE] bit. Using IACK has the advantage of not having to first set the EALLOW bit. This allows the main CPU to efficiently trigger CLA tasks through software.

Figure 4-13. MIFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-34. MIFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	INT8	R/W	0h	Task 8 Interrupt Force 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to force the task 8 interrupt
6	INT7	R/W	0h	Task 7 Interrupt Force 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to force the task 7 interrupt
5	INT6	R/W	0h	Task 6 Interrupt Force 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to force the task 6 interrupt
4	INT5	R/W	0h	Task 5 Interrupt Force 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to force the task 5 interrupt
3	INT4	R/W	0h	Task 4 Interrupt Force 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to force the task 4 interrupt
2	INT3	R/W	0h	Task 3 Interrupt Force 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to force the task 3 interrupt
1	INT2	R/W	0h	Task 2 Interrupt Force 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to force the task 2 interrupt
0	INT1	R/W	0h	Task 1 Interrupt Force 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to force the task 1 interrupt

4.6.2.13 MICLR Register (offset = 23h) [reset = 0h]

MICLR is shown in [Figure 4-14](#) and described in [Table 4-35](#).

Normally bits in the MIFR register are automatically cleared when a task begins. The interrupt flag clear register can be used to instead manually clear bits in the interrupt flag (MIFR) register. Writing a 1 to a MICLR bit will clear the corresponding bit in the MIFR register. Writes of 0 are ignored and reads always return 0.

Figure 4-14. MICLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-35. MICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	INT8	R/W	0h	Task 8 Interrupt Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 8 interrupt flag
6	INT7	R/W	0h	Task 7 Interrupt Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 7 interrupt flag
5	INT6	R/W	0h	Task 6 Interrupt Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 6 interrupt flag
4	INT5	R/W	0h	Task 5 Interrupt Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 5 interrupt flag
3	INT4	R/W	0h	Task 4 Interrupt Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 4 interrupt flag
2	INT3	R/W	0h	Task 3 Interrupt Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 3 interrupt flag
1	INT2	R/W	0h	Task 2 Interrupt Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 2 interrupt flag
0	INT1	R/W	0h	Task 1 Interrupt Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 1 interrupt flag

4.6.2.14 MICLROVF Register (offset = 24h) [reset = 0h]

MICLROVF is shown in [Figure 4-15](#) and described in [Table 4-36](#).

Overflow flag bits in the MIOVF register are latched until manually cleared using the MICLROVF register. Writing a 1 to a MICLROVF bit will clear the corresponding bit in the MIOVF register. Writes of 0 are ignored and reads always return 0.

Figure 4-15. MICLROVF Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-36. MICLROVF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	INT8	R/W	0h	Task 8 Interrupt Overflow Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 8 interrupt overflow flag
6	INT7	R/W	0h	Task 7 Interrupt Overflow Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 7 interrupt overflow flag
5	INT6	R/W	0h	Task 6 Interrupt Overflow Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 6 interrupt overflow flag
4	INT5	R/W	0h	Task 5 Interrupt Overflow Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 5 interrupt overflow flag
3	INT4	R/W	0h	Task 4 Interrupt Overflow Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 4 interrupt overflow flag
2	INT3	R/W	0h	Task 3 Interrupt Overflow Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 3 interrupt overflow flag
1	INT2	R/W	0h	Task 2 Interrupt Overflow Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 2 interrupt overflow flag
0	INT1	R/W	0h	Task 1 Interrupt Overflow Flag Clear 0h (R/W) = This bit always reads back 0 and writes of 0 have no effect 1h (R/W) = Write a 1 to clear the task 1 interrupt overflow flag

4.6.2.15 MIER Register (offset = 25h) [reset = 0h]

MIER is shown in [Figure 4-16](#) and described in [Table 4-37](#).

Setting the bits in the interrupt enable register (MIER) allow an incoming interrupt or main CPU software to start the corresponding CLA task. Writing a 0 will block the task, but the interrupt request will still be latched in the flag register (MIFLG). Setting the MIER register bit to 0 while the corresponding task is executing will have no effect on the task. The task will continue to run until it hits the MSTOP instruction. When a soft reset is issued, the MIER bits are cleared. There should always be at least a 1 SYSCLKOUT delay between issuing the soft reset and reconfiguring the MIER bits.

Figure 4-16. MIER Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-37. MIER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	INT8	R	0h	Task 8 Interrupt Enable 0h (R/W) = TASK_INT_DISABLE Task 8 interrupt is disabled (default) 1h (R/W) = TASK_INT_ENABLE Task 8 interrupt is enabled
6	INT7	R	0h	Task 7 Interrupt Enable 0h (R/W) = TASK_INT_DISABLE Task 7 interrupt is disabled (default) 1h (R/W) = TASK_INT_ENABLE Task 7 interrupt is enabled
5	INT6	R	0h	Task 6 Interrupt Enable 0h (R/W) = TASK_INT_DISABLE Task 6 interrupt is disabled (default) 1h (R/W) = TASK_INT_ENABLE Task 6 interrupt is enabled
4	INT5	R	0h	Task 5 Interrupt Enable 0h (R/W) = TASK_INT_DISABLE Task 5 interrupt is disabled (default) 1h (R/W) = TASK_INT_ENABLE Task 5 interrupt is enabled
3	INT4	R	0h	Task 4 Interrupt Enable 0h (R/W) = TASK_INT_DISABLE Task 4 interrupt is disabled (default) 1h (R/W) = TASK_INT_ENABLE Task 4 interrupt is enabled
2	INT3	R	0h	Task 3 Interrupt Enable 0h (R/W) = TASK_INT_DISABLE Task 3 interrupt is disabled (default) 1h (R/W) = TASK_INT_ENABLE Task 3 interrupt is enabled

Table 4-37. MIER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT2	R	0h	Task 2 Interrupt Enable 0h (R/W) = TASK_INT_DISABLE Task 2 interrupt is disabled (default) 1h (R/W) = TASK_INT_ENABLE Task 2 interrupt is enabled
0	INT1	R	0h	Task 1 Interrupt Enable 0h (R/W) = TASK_INT_DISABLE Task 1 interrupt is disabled (default) 1h (R/W) = TASK_INT_ENABLE Task 1 interrupt is enabled

4.6.2.16 MIRUN Register (offset = 26h) [reset = 0h]

MIRUN is shown in [Figure 4-17](#) and described in [Table 4-38](#).

The interrupt run status register (MIRUN) indicates which task is currently executing. Only one MIRUN bit will ever be set to a 1 at any given time. The bit is automatically cleared when the task competes and the respective interrupt is fed to the peripheral interrupt expansion (PIE) block of the device. This lets the main CPU know when a task has completed. The main CPU can stop a currently running task by writing to the MCTL[SOFTRESET] bit. This will clear the MIRUN flag and stop the task. In this case no interrupt will be generated to the PIE.

Figure 4-17. MIRUN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

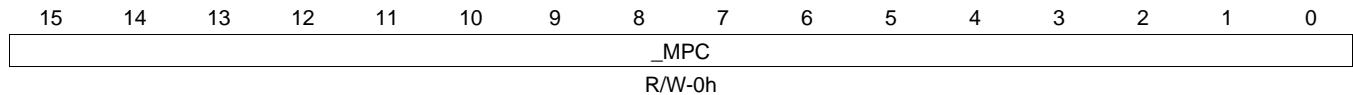
Table 4-38. MIRUN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	INT8	R	0h	Task 8 Run Status 0h (R/W) = Task 8 is not executing (default) 1h (R/W) = Task 8 is executing
6	INT7	R	0h	Task 7 Run Status 0h (R/W) = Task 7 is not executing (default) 1h (R/W) = Task 7 is executing
5	INT6	R	0h	Task 6 Run Status 0h (R/W) = Task 6 is not executing (default) 1h (R/W) = Task 6 is executing
4	INT5	R	0h	Task 5 Run Status 0h (R/W) = Task 5 is not executing (default) 1h (R/W) = Task 5 is executing
3	INT4	R	0h	Task 4 Run Status 0h (R/W) = Task 4 is not executing (default) 1h (R/W) = Task 4 is executing
2	INT3	R	0h	Task 3 Run Status 0h (R/W) = Task 3 is not executing (default) 1h (R/W) = Task 3 is executing
1	INT2	R	0h	Task 2 Run Status 0h (R/W) = Task 2 is not executing (default) 1h (R/W) = Task 2 is executing
0	INT1	R	0h	Task 1 Run Status 0h (R/W) = Task 1 is not executing (default) 1h (R/W) = Task 1 is executing

4.6.2.17 _MPC Register (offset = 28h) [reset = 0h]

_MPC is shown in [Figure 4-18](#) and described in [Table 4-39](#).

CLA Program Counter

Figure 4-18. _MPC Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

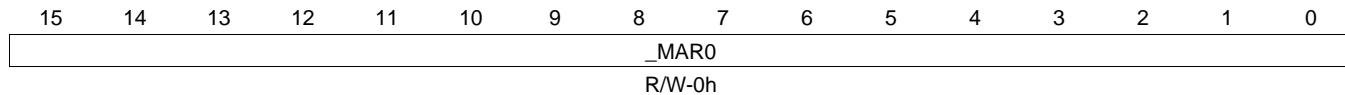
Table 4-39. _MPC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	_MPC	R/W	0h	Points to the instruction currently in the decode 2 phase of the CLA pipeline. The address range of the CLA with a 16-bit MPC is 64K 16-bit words or 32K CLA instructions.

4.6.2.18 _MAR0 Register (offset = 2Ah) [reset = 0h]

_MAR0 is shown in [Figure 4-19](#) and described in [Table 4-40](#).

CLA Auxiliary Register 0

Figure 4-19. _MAR0 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

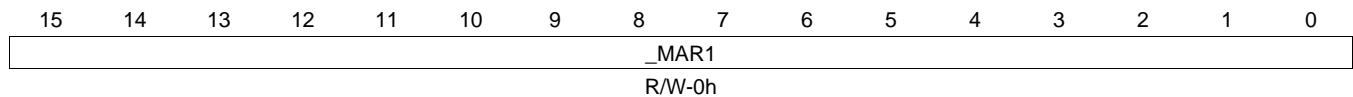
Table 4-40. _MAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	_MAR0	R/W	0h	CLA Auxillary Register 0

4.6.2.19 _MAR1 Register (offset = 2Bh) [reset = 0h]

_MAR1 is shown in [Figure 4-20](#) and described in [Table 4-41](#).

CLA Auxiliary Register 1

Figure 4-20. _MAR1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-41. _MAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	_MAR1	R/W	0h	CLA Auxillary Register 1

4.6.2.20 _MSTF Register (offset = 2Ch) [reset = 0h]

_MSTF is shown in [Figure 4-21](#) and described in [Table 4-42](#).

The CLA status register (MSTF) reflects the results of different operations. These are the basic rules for the flags:

- Zero and negative flags are cleared or set based on:
- floating-point moves to registers
- the result of compare, minimum, maximum, negative and absolute value operations
- the integer result of operations such as MMOV16, MAND32, MOR32, MXOR32, MCMP32, MASR32, MLSR32
- Overflow and underflow flags are set by floating-point math instructions such as multiply, add, subtract and 1/x. These flags may also be connected to the peripheral interrupt expansion (PIE) block on your device. This can be useful for debugging underflow and overflow conditions within an application.

Figure 4-21. _MSTF Register

31	30	29	28	27	26	25	24
RESERVED						RPC	
R-0h						R/W-0h	
23	22	21	20	19	18	17	16
RPC						R/W-0h	
R/W-0h						R-0h	
15	14	13	12	11	10	9	8
RPC				MEALLOW	RESERVED	RNDF32	RESERVED
R/W-0h				R/W-0h	R-0h	R/W-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	TF	RESERVED		ZF	NF	LUF	LVF
R-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-42. _MSTF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-12	RPC	R/W	0h	Return program counter The RPC is used to save and restore the MPC address by the MCCNDD and MRCNDD operations
11	MEALLOW	R/W	0h	MEALLOW Status This bit enables and disables CLA write access to EALLOW protected registers. This is independent of the state of the EALLOW bit in the main CPU status register. This status bit can be saved and restored by the MMOV32 STF, mem32 instruction. 0h (R/W) = The CLA cannot write to EALLOW protected registers. This bit is cleared by the CLA instruction, MEDIS. 1h (R/W) = The CLA is allowed to write to EALLOW protected registers. This bit is set by the CLA instruction, MEALLOW.
10	RESERVED	R	0h	Reserved
9	RNDF32	R/W	0h	Round 32-bit Floating-Point Mode Use the MSETFLG and MMOV32 MSTF, mem32 instructions to change the rounding mode 0h (R/W) = If this bit is zero, the MMPYF32, MADDF32 and MSUBF32 instructions will round to zero (truncate). 1h (R/W) = If this bit is one, the MMPYF32, MADDF32 and MSUBF32 instructions will round to the nearest even value.
8-7	RESERVED	R	0h	Reserved

Table 4-42. _MSTF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TF	R/W	0h	<p>Test Flag</p> <p>The MTESTTF instruction can modify this flag based on the condition tested. The MSETFLG and MMOV32 MSTF, mem32 instructions can also be used to modify this flag.</p> <p>0h (R/W) = The condition tested with the MTESTTF instruction is false.</p> <p>1h (R/W) = The condition tested with the MTESTTF instruction is true.</p>
5-4	RESERVED	R/W	0h	Reserved
3	ZF	R/W	0h	<p>Zero Flag</p> <ul style="list-style-type: none"> - Instructions that modify this flag based on the floating-point value stored in the destination register: <p>MMOV32, MMOVD32, MABSF32, MNEGF32</p> <ul style="list-style-type: none"> - Instructions that modify this flag based on the floating-point result of the operation: <p>MCMPF32, MMAXF32, and MMINF32</p> <ul style="list-style-type: none"> - Instructions that modify this flag based on the integer result of the operation: <p>MMOV16, MAND32, MOR32, MXOR32, MCMP32, MASR32, MLSR32 and MSL32</p> <p>The MSETFLG and MMOV32 MSTF, mem32 instructions can also be used to modify this flag</p> <p>0h (R/W) = The value is not zero</p> <p>1h (R/W) = The value is zero</p>
2	NF	R/W	0h	<p>Negative Flag</p> <ul style="list-style-type: none"> - Instructions that modify this flag based on the floating-point value stored in the destination register: <p>MMOV32, MMOVD32, MABSF32, MNEGF32</p> <ul style="list-style-type: none"> - Instructions that modify this flag based on the floating-point result of the operation: <p>MCMPF32, MMAXF32, and MMINF32</p> <ul style="list-style-type: none"> - Instructions that modify this flag based on the integer result of the operation: <p>MMOV16, MAND32, MOR32, MXOR32, MCMP32, MASR32, MLSR32 and MSL32</p> <p>The MSETFLG and MMOV32 MSTF, mem32 instructions can also be used to modify this flag</p> <p>0h (R/W) = The value is not negative</p> <p>1h (R/W) = The value is negative</p>
1	LUF	R/W	0h	<p>Latched Underflow Flag</p> <p>The following instructions will set this flag to 1 if an underflow occurs:</p> <p>MMPYF32, MADDF32, MSUBF32, MMACF32, MEINV32, MEISQRTF32</p> <p>The MSETFLG and MMOV32 MSTF, mem32 instructions can also be used to modify this flag</p> <p>0h (R/W) = An underflow condition has not been latched</p> <p>1h (R/W) = An underflow condition has been latched</p>

Table 4-42. _MSTF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LVF	R/W	0h	<p>Latched Overflow Flag</p> <p>The following instructions will set this flag to 1 if an overflow occurs: MMPYF32, MADDF32, MSUBF32, MMACF32, MEINV32, MEISQRTF32</p> <p>The MSETFLG and MMOV32 MSTF, mem32 instructions can also be used to modify this flag</p> <p>0h (R/W) = An overflow condition has not been latched 1h (R/W) = An overflow condition has been latched</p>

4.6.2.21 _MR0 Register (offset = 2Eh) [reset = 0h]

_MR0 is shown in [Figure 4-22](#) and described in [Table 4-43](#).

CLA Floating-Point Result Register 0

Figure 4-22. _MR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
i32																															

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-43. _MR0 Register Field Descriptions

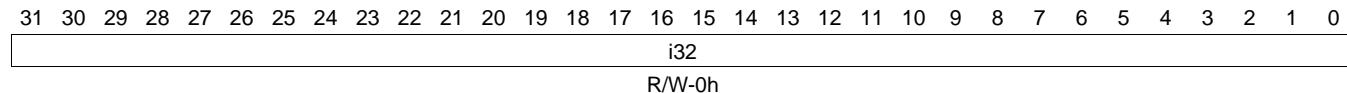
Bit	Field	Type	Reset	Description
31-0	i32	R/W	0h	CLA Result Register 0

4.6.2.22 _MR1 Register (offset = 32h) [reset = 0h]

_MR1 is shown in [Figure 4-23](#) and described in [Table 4-44](#).

CLA Floating-Point Result Register 1

Figure 4-23. _MR1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-44. _MR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	i32	R/W	0h	CLA Result Register 1

4.6.2.23 _MR2 Register (offset = 36h) [reset = 0h]

_MR2 is shown in [Figure 4-24](#) and described in [Table 4-45](#).

CLA Floating-Point Result Register 2

Figure 4-24. _MR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
i32																															

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-45. _MR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	i32	R/W	0h	CLA Result Register 2

4.6.2.24 _MR3 Register (offset = 3Ah) [reset = 0h]

_MR3 is shown in [Figure 4-25](#) and described in [Table 4-46](#).

CLA Floating-Point Result Register 3

Figure 4-25. _MR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
i32 R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 4-46. _MR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	i32	R/W	0h	CLA Result Register 3

Preliminary



Chapter 5

SPRUHM8A—December 2013—Revised March 2014

Inter-Processor Communication (IPC)

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5.1 Inter-Processor Communication

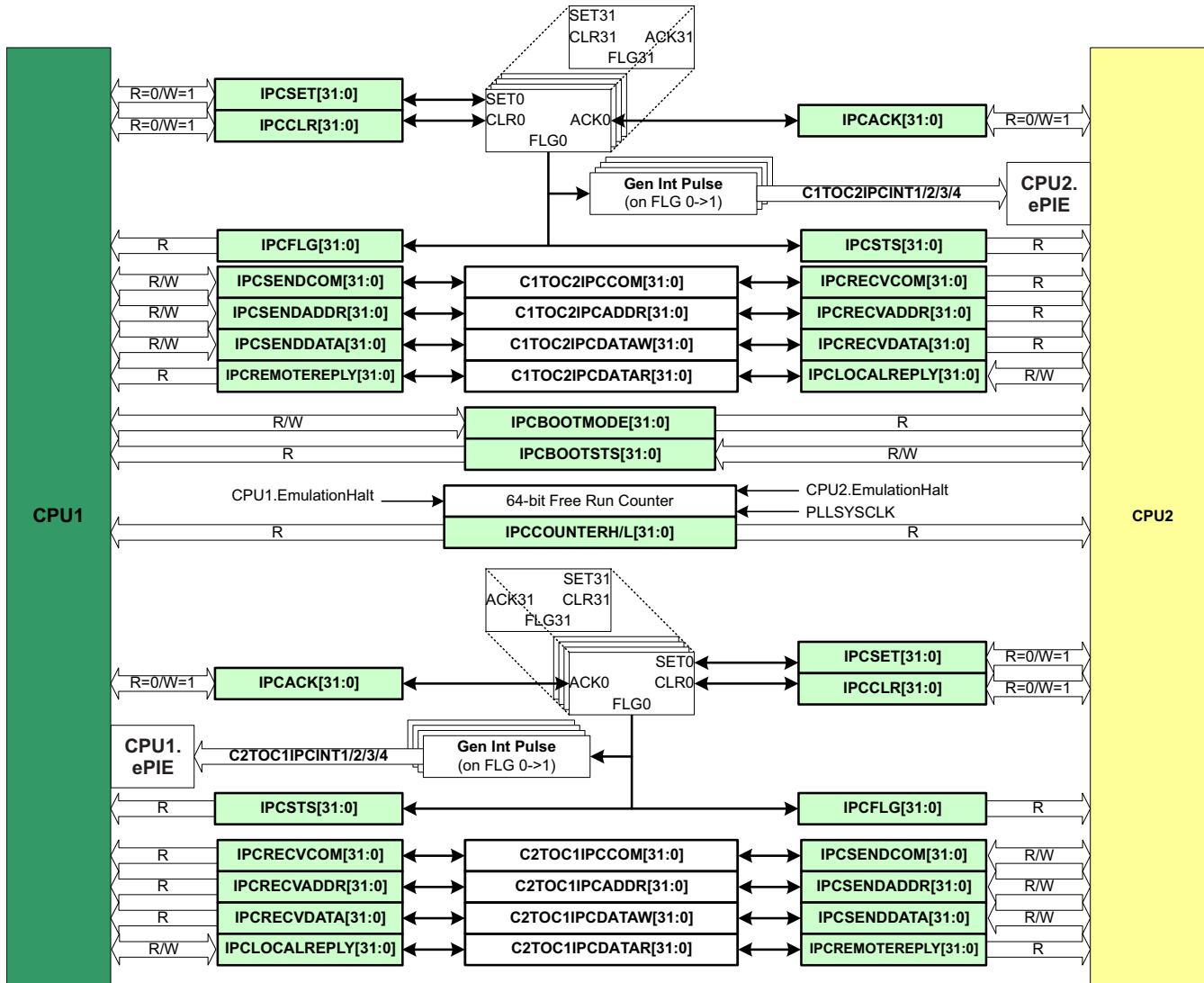
The Inter-Processor Communications (IPC) module allows communication between the two CPU subsystems. This section details the IPC features that each CPU can use to request and share information. The IPC features are:

- Message RAMs
- IPC flags and interrupts
- IPC command registers
- Flash pump semaphore
- Clock configuration semaphore
- Free-running counter

All IPC features are independent of each other, and most do not require any specific data format. There are also two registers for boot mode/status communication. Please refer to the boot ROM chapter for more information on these registers.

Figure 5-1 shows the design structure of the IPC module.

Figure 5-1. IPC Module Architecture



5.1.1 Message RAMs

There are two dedicated 2kB blocks of message RAM. Each CPU and its DMA have read/write access to one RAM and read-only access to the other RAM, as shown in [Table 5-1](#)

Table 5-1. IPC Message RAM Read/Write Access

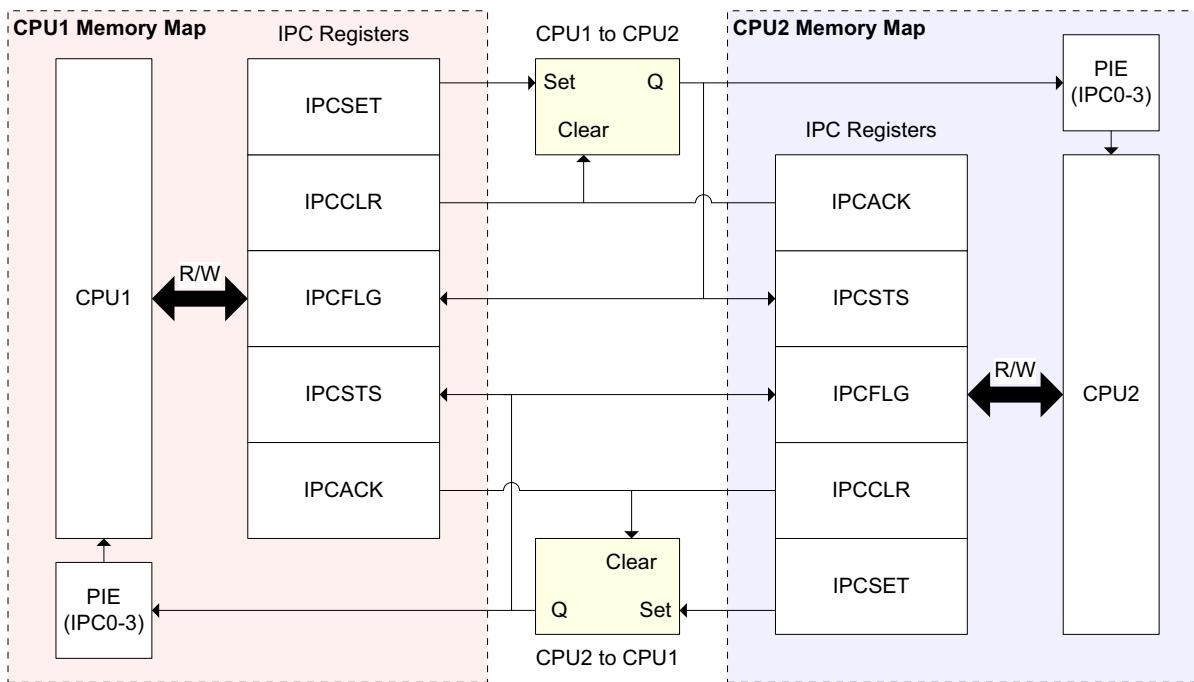
	CPU1	CPU2	CPU1 DMA	CPU2 DMA
CPU1 to CPU2 (2kB, address 0x03FC00)	R/W	R	R/W	R
CPU2 to CPU1 (2kB, address 0x03F800)	R	R/W	R	R/W

Reading or writing a message RAM does not trigger any events on the remote CPU.

5.1.2 IPC Flags and Interrupts

There are 32 IPC event signals from CPU1 to CPU2, and vice-versa. These signals can be used for flag-based event polling. Four of them (IPC0 - IPC3) can be configured to generate IPC interrupts on the remote CPU. [Figure 5-2](#) shows the IPC flag messaging and interrupt system.

Figure 5-2. Messaging with IPC Flags and Interrupts



5.1.3 IPC Command Registers

The IPC command registers provide a simple and flexible way for the two CPUs to exchange more complex messages. Each CPU has eight dedicated registers, four for sending messages and four for receiving messages. The register names were chosen to support a simple command/response protocol, but can be used for any purpose. Only the read/write permissions are determined by hardware; the data format is entirely software-defined.

For sending messages, each CPU has three writable registers and one read-only register. Those same registers are accessible on the remote CPU as three read-only registers and one writable register. [Table 5-2](#) shows the command registers.

Table 5-2. IPC Command Registers

Local Register Name	Local CPU	Remote CPU	Remote Register Name
IPCSENDCOM	R/W	R	IPCRECVCOM
IPCSENDADDR	R/W	R	IPCRECVADDR
IPCSENDDATA	R/W	R	IPCRECVDATA
IPCREMOTEREPLY	R	R/W	IPCLOCALREPLY

5.1.4 Flash Pump and Clock Configuration Semaphores

The semaphore registers allow the two CPUs to manage shared system resources.

5.1.4.1 Flash Pump Semaphore

Each CPU subsystem has its own flash bank, which it can read, program, and erase. Both flash banks share a single charge pump for program and erase operations. Hence, only one CPU can program/erase its flash at any given time. A CPU can read data and execute code from its flash even when the other CPU is programming or erasing. The flash pump semaphore allows one CPU to take control of the pump without being interrupted by the other CPU.

5.1.4.2 Clock Configuration Semaphore

The two CPUs share a common set of PLL and peripheral clock configuration registers. Since each CPU can have its own mix of peripherals, both may access the configuration registers. The clock configuration semaphore allows one CPU to access the registers without being interrupted by the other CPU.

5.1.4.3 Semaphore States

Both the flash pump and the clock configuration semaphores allow the same states and state transitions. The semaphore is implemented as a two-bit field in a register with special write protections. The semaphore registers require a key field to be written at the same time as the semaphore bits. See the PUMPREQUEST and CLKSEM register descriptions for details. The possible semaphore states are:

- | | |
|----------|--|
| 00 or 11 | Either CPU may write to the semaphore. CPU1 has control of the resource by default. 00 is the reset state. |
| 01 | CPU2 has exclusive control of the resource and exclusive write access to the semaphore. |
| 10 | CPU1 has exclusive control of the resource and exclusive write access to the semaphore. |

Each CPU is only allowed to take control of the resource for itself. Direct transfer between the 01 and 10 states is not allowed. However, CPU1 may force both semaphores into the default state (00) at any time by putting CPU2 into reset. [Figure 5-3](#) and [Figure 5-4](#) show the allowed states and state transitions.

Figure 5-3. Flash Pump Semaphore State transitions

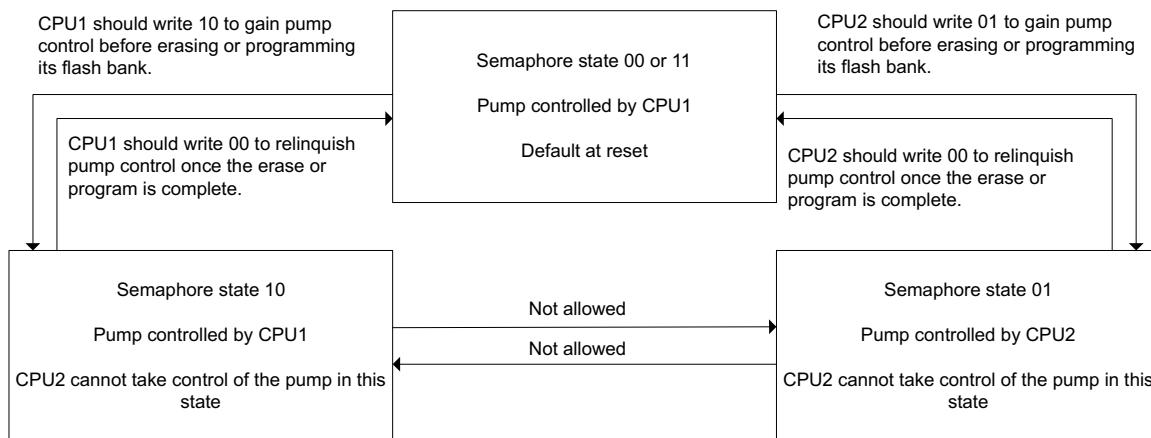
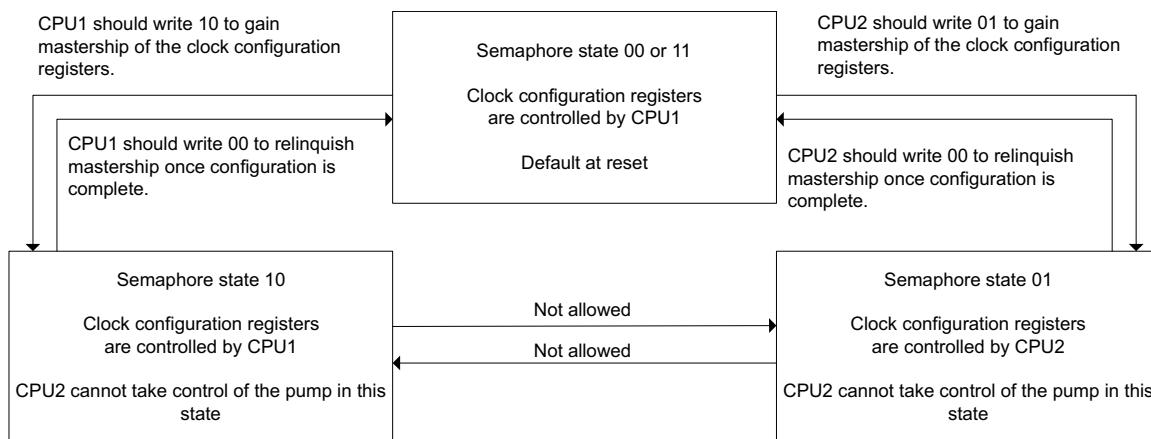


Figure 5-4. Clock Configuration Semaphore State Transitions



5.1.5 Free-Running Counter

A 64-bit free-running counter is present in the device and can be used to timestamp IPC events between processors. The counter is clocked by PLLSYSCLK and reset by SYRSRsN. The counter is implemented as two 32-bit registers, IPCCOUNTERH and IPCCOUNTERL. When IPCCOUNTERL is read, the value of IPCCOUNTERH is saved. A subsequent read to IPCCOUNTERH returns this saved value. This design prevents race conditions due to IPCCOUNTERL overflowing between reads of the two registers.

The free-running counter only stops when both CPUs are in HALT mode. If either core is executing, the counter runs.

5.1.6 IPC Communication Protocol

This section describes the hardware support options for IPC communication between the two CPUs. These options can be used independently or in combination. All flag definitions and data formats are entirely user-defined.

- The flag system supports event-based communication via interrupts and register polling.
 - CPUx can raise an IPC event by writing to any of the 32 bits of its IPCSET register. This sets the corresponding bits in CPUx's IPCFLG register and CPUy's IPCSTS register.
 - CPUy can signal its response to the event by setting the appropriate bit in its IPCACK register. This clears the corresponding bits in CPUx's IPCFLG register and CPUy's IPCSTS register.
 - If CPUx needs to cancel an event, it can set the appropriate bit in its IPCCLR register. This has the same effect as CPUy writing to IPCACK.
 - Flags 0–3 (set via IPCSET[3:0]) fire interrupts to the remote CPU. The remote CPU must configure its ePIE module properly in order to receive an IPC interrupt. Flags 4–31 (set via IPCSET[31:4]) do not produce interrupts. Multiple flags can be set, acknowledged, and cleared simultaneously.
- The command registers support sending several distinct pieces of information. They are named COM, ADDR, DATA, and REPLY for convenience only and can hold whatever data the application needs.
 - CPUx can write data to its IPCSENDCOM, IPCSENDADDR, and IPCSENDDATA registers. CPUy receives these in its IPCRECVCOM, IPCRECVADDR, and IPCRECVDATA registers.
 - CPUy can respond by writing to its IPCLOCALREPLY register. CPUx receives this data in its IPCREMOTEREPLY register.
 - Each CPU can only write to its SEND and LOCALREPLY registers. The RECV and REMOTEREPLY registers are read-only.
- There is an additional pair of command-like registers offered for boot-time IPC or any other convenient use — IPCBOOTMODE and IPCBOOTSTS. Both CPUs can read these registers. CPU1 can only write to IPCBOOTMODE, and CPU2 can only write to IPCBOOTSTS.
- There are two shared memories for passing large amounts of data between the CPUs. Each CPU has a writable memory for sending data and a read-only memory for receiving data.
- Here is an example of how to use these features together. CPUx needs some data from CPUy's LS RAM. The data is at CPUy address 0x9400 and is 0x80 16-bit words long. The protocol could be implemented like this:
 - CPUx writes 0x1 to IPCSENDCOM, defined in software to mean "copy data from address". It writes the address (0x9400) to IPCSENDADDR and the data length (0x80) to IPCSENDDATA.
 - CPUx writes to IPCSET[3] and IPCSET[16]. Here, IPC flag 3 is configured to send an interrupt and IPCSET[16] is defined in software to indicate an incoming command. CPUx begins polling for IPCFLG[3] to go low.
 - CPUy receives the interrupt. In the interrupt handler, it checks IPCSTS, finds that flag 16 is set, and runs a command processor.
 - CPUy reads the command (0x1) from IPCRECVCOM, the address (0x9400) from IPCRECVADDR, and the data length (0x80) from IPCRECVDATA. CPUy then copies the LS RAM data to an empty space in its writable shared memory starting at offset 0x210.
 - CPUy writes the shared memory address (0x210) to its IPCLOCALREPLY register. It then writes to IPCACK[16] and IPCACK[3] to clear the flags and indicate completion of the command. CPUy's work is done.
 - CPUx sees IPCFLG[3] go low. It reads IPCREMOTEREPLY to get the shared memory offset of the copied data (0x210).

5.2 Registers

5.2.1 IPC Base Addresses

Table 5-3. IPC Base Addresses

Device Registers	Register Name	Start Address	End Address
IpcRegs (CPU1)	IPC_REGS_CPU1	0x0005_0000	0x0005_0FFF
IpcRegs (CPU2)	IPC_REGS_CPU2	0x0005_0000	0x0005_0FFF

5.2.2 IPC_REGS_CPU1 Registers

Table 5-4 lists the memory-mapped registers for the IPC_REGS_CPU1. All register offset addresses not listed in Table 5-4 should be considered as reserved locations and the register contents should not be modified.

Table 5-4. IPC_REGS_CPU1 REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	IPCACK	IPC incoming flag clear (acknowledge) register	Section 5.2.3.1	
2h	IPCSTS	IPC incoming flag status register	Section 5.2.3.2	
4h	IPCSET	IPC remote flag set register	Section 5.2.3.3	
6h	IPCCCLR	IPC remote flag clear register	Section 5.2.3.4	
8h	IPCFLG	IPC remote flag status register	Section 5.2.3.5	
Ch	IPCCOUNTERL	IPC Counter Low Register	Section 5.2.3.6	
Eh	IPCCOUNTERH	IPC Counter High Register	Section 5.2.3.7	
10h	IPCSENDCOM	Local to Remote IPC Command Register	Section 5.2.3.12	
12h	IPCSENDADDR	Local to Remote IPC Address Register	Section 5.2.3.13	
14h	IPCSENDDATA	Local to Remote IPC Data Register	Section 5.2.3.14	
16h	IPCREMOTEREPLY	Remote to Local IPC Reply Data Register	Section 5.2.3.15	
18h	IPCRECVCOM	Remote to Local IPC Command Register	Section 5.2.3.8	
1Ah	IPCRECVADDR	Remote to Local IPC Address Register	Section 5.2.3.9	
1Ch	IPCRECVDATA	Remote to Local IPC Data Register	Section 5.2.3.10	
1Eh	IPCLOCALREPLY	Local to Remote IPC Reply Data Register	Section 5.2.3.11	
20h	IPCBOOTSTS	CPU2 to CPU1 IPC Boot Status Register	Section 5.2.3.16	
22h	IPCBOOTMODE	CPU1 to CPU2 IPC Boot Mode Register	Section 5.2.3.17	
24h	PUMPREQUEST	Flash programming semaphore PUMP request register	Section 5.2.3.18	EALLOW

5.2.2.1 IPCACK Register (offset = 0h) [reset = 0h]

IPCACK is shown in [Figure 5-23](#) and described in [Table 5-24](#).

IPC incoming flag clear (acknowledge) register

Figure 5-5. IPCACK Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R=0/W=1-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R=0/W=1-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R=0/W=1-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-5. IPCACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R=0/W=1	0h	Writing 1 to this bit clears the IPC31 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
30	IPC30	R=0/W=1	0h	Writing 1 to this bit clears the IPC30 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
29	IPC29	R=0/W=1	0h	Writing 1 to this bit clears the IPC29 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
28	IPC28	R=0/W=1	0h	Writing 1 to this bit clears the IPC28 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
27	IPC27	R=0/W=1	0h	Writing 1 to this bit clears the IPC27 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
26	IPC26	R=0/W=1	0h	Writing 1 to this bit clears the IPC26 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
25	IPC25	R=0/W=1	0h	Writing 1 to this bit clears the IPC25 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
24	IPC24	R=0/W=1	0h	Writing 1 to this bit clears the IPC24 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
23	IPC23	R=0/W=1	0h	Writing 1 to this bit clears the IPC23 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
22	IPC22	R=0/W=1	0h	Writing 1 to this bit clears the IPC22 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.

Table 5-5. IPCACK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	IPC21	R=0/W=1	0h	Writing 1 to this bit clears the IPC21 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
20	IPC20	R=0/W=1	0h	Writing 1 to this bit clears the IPC20 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
19	IPC19	R=0/W=1	0h	Writing 1 to this bit clears the IPC19 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
18	IPC18	R=0/W=1	0h	Writing 1 to this bit clears the IPC18 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
17	IPC17	R=0/W=1	0h	Writing 1 to this bit clears the IPC17 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
16	IPC16	R=0/W=1	0h	Writing 1 to this bit clears the IPC16 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
15	IPC15	R=0/W=1	0h	Writing 1 to this bit clears the IPC15 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
14	IPC14	R=0/W=1	0h	Writing 1 to this bit clears the IPC14 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
13	IPC13	R=0/W=1	0h	Writing 1 to this bit clears the IPC13 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
12	IPC12	R=0/W=1	0h	Writing 1 to this bit clears the IPC12 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
11	IPC11	R=0/W=1	0h	Writing 1 to this bit clears the IPC11 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
10	IPC10	R=0/W=1	0h	Writing 1 to this bit clears the IPC10 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
9	IPC9	R=0/W=1	0h	Writing 1 to this bit clears the IPC9 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
8	IPC8	R=0/W=1	0h	Writing 1 to this bit clears the IPC8 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
7	IPC7	R=0/W=1	0h	Writing 1 to this bit clears the IPC7 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
6	IPC6	R=0/W=1	0h	Writing 1 to this bit clears the IPC6 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
5	IPC5	R=0/W=1	0h	Writing 1 to this bit clears the IPC5 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.

Table 5-5. IPCACK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IPC4	R=0/W=1	0h	Writing 1 to this bit clears the IPC4 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
3	IPC3	R=0/W=1	0h	Writing 1 to this bit clears the IPC3 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
2	IPC2	R=0/W=1	0h	Writing 1 to this bit clears the IPC2 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
1	IPC1	R=0/W=1	0h	Writing 1 to this bit clears the IPC1 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
0	IPC0	R=0/W=1	0h	Writing 1 to this bit clears the IPC0 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.

5.2.2.2 IPCSTS Register (offset = 2h) [reset = 0h]

IPCSTS is shown in [Figure 5-24](#) and described in [Table 5-25](#).

IPC incoming flag status register

Figure 5-6. IPCSTS Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-6. IPCSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R	0h	Indicates to the local CPU if the IPC31 event flag was set by the remote CPU. 0: No IPC31 event was set by the remote CPU 1: An IPC31 event was set by the remote CPU
30	IPC30	R	0h	Indicates to the local CPU if the IPC30 event flag was set by the remote CPU. 0: No IPC30 event was set by the remote CPU 1: An IPC30 event was set by the remote CPU
29	IPC29	R	0h	Indicates to the local CPU if the IPC29 event flag was set by the remote CPU. 0: No IPC29 event was set by the remote CPU 1: An IPC29 event was set by the remote CPU
28	IPC28	R	0h	Indicates to the local CPU if the IPC28 event flag was set by the remote CPU. 0: No IPC28 event was set by the remote CPU 1: An IPC28 event was set by the remote CPU
27	IPC27	R	0h	Indicates to the local CPU if the IPC27 event flag was set by the remote CPU. 0: No IPC27 event was set by the remote CPU 1: An IPC27 event was set by the remote CPU
26	IPC26	R	0h	Indicates to the local CPU if the IPC26 event flag was set by the remote CPU. 0: No IPC26 event was set by the remote CPU 1: An IPC26 event was set by the remote CPU
25	IPC25	R	0h	Indicates to the local CPU if the IPC25 event flag was set by the remote CPU. 0: No IPC25 event was set by the remote CPU 1: An IPC25 event was set by the remote CPU

Table 5-6. IPCSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	IPC24	R	0h	Indicates to the local CPU if the IPC24 event flag was set by the remote CPU. 0: No IPC24 event was set by the remote CPU 1: An IPC24 event was set by the remote CPU
23	IPC23	R	0h	Indicates to the local CPU if the IPC23 event flag was set by the remote CPU. 0: No IPC23 event was set by the remote CPU 1: An IPC23 event was set by the remote CPU
22	IPC22	R	0h	Indicates to the local CPU if the IPC22 event flag was set by the remote CPU. 0: No IPC22 event was set by the remote CPU 1: An IPC22 event was set by the remote CPU
21	IPC21	R	0h	Indicates to the local CPU if the IPC21 event flag was set by the remote CPU. 0: No IPC21 event was set by the remote CPU 1: An IPC21 event was set by the remote CPU
20	IPC20	R	0h	Indicates to the local CPU if the IPC20 event flag was set by the remote CPU. 0: No IPC20 event was set by the remote CPU 1: An IPC20 event was set by the remote CPU
19	IPC19	R	0h	Indicates to the local CPU if the IPC19 event flag was set by the remote CPU. 0: No IPC19 event was set by the remote CPU 1: An IPC19 event was set by the remote CPU
18	IPC18	R	0h	Indicates to the local CPU if the IPC18 event flag was set by the remote CPU. 0: No IPC18 event was set by the remote CPU 1: An IPC18 event was set by the remote CPU
17	IPC17	R	0h	Indicates to the local CPU if the IPC17 event flag was set by the remote CPU. 0: No IPC17 event was set by the remote CPU 1: An IPC17 event was set by the remote CPU
16	IPC16	R	0h	Indicates to the local CPU if the IPC16 event flag was set by the remote CPU. 0: No IPC16 event was set by the remote CPU 1: An IPC16 event was set by the remote CPU
15	IPC15	R	0h	Indicates to the local CPU if the IPC15 event flag was set by the remote CPU. 0: No IPC15 event was set by the remote CPU 1: An IPC15 event was set by the remote CPU
14	IPC14	R	0h	Indicates to the local CPU if the IPC14 event flag was set by the remote CPU. 0: No IPC14 event was set by the remote CPU 1: An IPC14 event was set by the remote CPU
13	IPC13	R	0h	Indicates to the local CPU if the IPC13 event flag was set by the remote CPU. 0: No IPC13 event was set by the remote CPU 1: An IPC13 event was set by the remote CPU
12	IPC12	R	0h	Indicates to the local CPU if the IPC12 event flag was set by the remote CPU. 0: No IPC12 event was set by the remote CPU 1: An IPC12 event was set by the remote CPU

Table 5-6. IPCSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	IPC11	R	0h	Indicates to the local CPU if the IPC11 event flag was set by the remote CPU. 0: No IPC11 event was set by the remote CPU 1: An IPC11 event was set by the remote CPU
10	IPC10	R	0h	Indicates to the local CPU if the IPC10 event flag was set by the remote CPU. 0: No IPC10 event was set by the remote CPU 1: An IPC10 event was set by the remote CPU
9	IPC9	R	0h	Indicates to the local CPU if the IPC9 event flag was set by the remote CPU. 0: No IPC9 event was set by the remote CPU 1: An IPC9 event was set by the remote CPU
8	IPC8	R	0h	Indicates to the local CPU if the IPC8 event flag was set by the remote CPU. 0: No IPC8 event was set by the remote CPU 1: An IPC8 event was set by the remote CPU
7	IPC7	R	0h	Indicates to the local CPU if the IPC7 event flag was set by the remote CPU. 0: No IPC7 event was set by the remote CPU 1: An IPC7 event was set by the remote CPU
6	IPC6	R	0h	Indicates to the local CPU if the IPC6 event flag was set by the remote CPU. 0: No IPC6 event was set by the remote CPU 1: An IPC6 event was set by the remote CPU
5	IPC5	R	0h	Indicates to the local CPU if the IPC5 event flag was set by the remote CPU. 0: No IPC5 event was set by the remote CPU 1: An IPC5 event was set by the remote CPU
4	IPC4	R	0h	Indicates to the local CPU if the IPC4 event flag was set by the remote CPU. 0: No IPC4 event was set by the remote CPU 1: An IPC4 event was set by the remote CPU
3	IPC3	R	0h	Indicates to the local CPU if the IPC3 event flag was set by the remote CPU. 0: No IPC3 event was set by the remote CPU 1: An IPC3 event was set by the remote CPU Notes [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
2	IPC2	R	0h	Indicates to the local CPU if the IPC2 event flag was set by the remote CPU. 0: No IPC2 event was set by the remote CPU 1: An IPC2 event was set by the remote CPU Notes [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
1	IPC1	R	0h	Indicates to the local CPU if the IPC1 event flag was set by the remote CPU. 0: No IPC1 event was set by the remote CPU 1: An IPC1 event was set by the remote CPU Notes [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.

Table 5-6. IPCSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IPC0	R	0h	<p>Indicates to the local CPU if the IPC0 event flag was set by the remote CPU.</p> <p>0: No IPC0 event was set by the remote CPU</p> <p>1: An IPC0 event was set by the remote CPU</p> <p>Notes</p> <p>[1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.</p>

5.2.2.3 IPCSET Register (offset = 4h) [reset = 0h]

IPCSET is shown in [Figure 5-25](#) and described in [Table 5-26](#).

IPC remote flag set register

Figure 5-7. IPCSET Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R=0/W=1-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R=0/W=1-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R=0/W=1-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-7. IPCSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R=0/W=1	0h	Writing 1 to this bit sets the IPC31 event flag for the remote CPU. Writing 0 has no effect.
30	IPC30	R=0/W=1	0h	Writing 1 to this bit sets the IPC30 event flag for the remote CPU. Writing 0 has no effect.
29	IPC29	R=0/W=1	0h	Writing 1 to this bit sets the IPC29 event flag for the remote CPU. Writing 0 has no effect.
28	IPC28	R=0/W=1	0h	Writing 1 to this bit sets the IPC28 event flag for the remote CPU. Writing 0 has no effect.
27	IPC27	R=0/W=1	0h	Writing 1 to this bit sets the IPC27 event flag for the remote CPU. Writing 0 has no effect.
26	IPC26	R=0/W=1	0h	Writing 1 to this bit sets the IPC26 event flag for the remote CPU. Writing 0 has no effect.
25	IPC25	R=0/W=1	0h	Writing 1 to this bit sets the IPC25 event flag for the remote CPU. Writing 0 has no effect.
24	IPC24	R=0/W=1	0h	Writing 1 to this bit sets the IPC24 event flag for the remote CPU. Writing 0 has no effect.
23	IPC23	R=0/W=1	0h	Writing 1 to this bit sets the IPC23 event flag for the remote CPU. Writing 0 has no effect.
22	IPC22	R=0/W=1	0h	Writing 1 to this bit sets the IPC22 event flag for the remote CPU. Writing 0 has no effect.
21	IPC21	R=0/W=1	0h	Writing 1 to this bit sets the IPC21 event flag for the remote CPU. Writing 0 has no effect.
20	IPC20	R=0/W=1	0h	Writing 1 to this bit sets the IPC20 event flag for the remote CPU. Writing 0 has no effect.
19	IPC19	R=0/W=1	0h	Writing 1 to this bit sets the IPC19 event flag for the remote CPU. Writing 0 has no effect.

Table 5-7. IPCSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	IPC18	R=0/W=1	0h	Writing 1 to this bit sets the IPC18 event flag for the remote CPU. Writing 0 has no effect.
17	IPC17	R=0/W=1	0h	Writing 1 to this bit sets the IPC17 event flag for the remote CPU. Writing 0 has no effect.
16	IPC16	R=0/W=1	0h	Writing 1 to this bit sets the IPC16 event flag for the remote CPU. Writing 0 has no effect.
15	IPC15	R=0/W=1	0h	Writing 1 to this bit sets the IPC15 event flag for the remote CPU. Writing 0 has no effect.
14	IPC14	R=0/W=1	0h	Writing 1 to this bit sets the IPC14 event flag for the remote CPU. Writing 0 has no effect.
13	IPC13	R=0/W=1	0h	Writing 1 to this bit sets the IPC13 event flag for the remote CPU. Writing 0 has no effect.
12	IPC12	R=0/W=1	0h	Writing 1 to this bit sets the IPC12 event flag for the remote CPU. Writing 0 has no effect.
11	IPC11	R=0/W=1	0h	Writing 1 to this bit sets the IPC11 event flag for the remote CPU. Writing 0 has no effect.
10	IPC10	R=0/W=1	0h	Writing 1 to this bit sets the IPC10 event flag for the remote CPU. Writing 0 has no effect.
9	IPC9	R=0/W=1	0h	Writing 1 to this bit sets the IPC9 event flag for the remote CPU. Writing 0 has no effect.
8	IPC8	R=0/W=1	0h	Writing 1 to this bit sets the IPC8 event flag for the remote CPU. Writing 0 has no effect.
7	IPC7	R=0/W=1	0h	Writing 1 to this bit sets the IPC7 event flag for the remote CPU. Writing 0 has no effect.
6	IPC6	R=0/W=1	0h	Writing 1 to this bit sets the IPC6 event flag for the remote CPU. Writing 0 has no effect.
5	IPC5	R=0/W=1	0h	Writing 1 to this bit sets the IPC5 event flag for the remote CPU. Writing 0 has no effect.
4	IPC4	R=0/W=1	0h	Writing 1 to this bit sets the IPC4 event flag for the remote CPU. Writing 0 has no effect.
3	IPC3	R=0/W=1	0h	Writing 1 to this bit sets the IPC3 event flag for the remote CPU. Writing 0 has no effect. Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
2	IPC2	R=0/W=1	0h	Writing 1 to this bit sets the IPC2 event flag for the remote CPU. Writing 0 has no effect. Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
1	IPC1	R=0/W=1	0h	Writing 1 to this bit sets the IPC1 event flag for the remote CPU. Writing 0 has no effect. Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.

Table 5-7. IPCSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IPC0	R=0/W=1	0h	<p>Writing 1 to this bit sets the IPC0 event flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.</p>

5.2.2.4 IPCCLR Register (offset = 6h) [reset = 0h]

IPCCLR is shown in [Figure 5-26](#) and described in [Table 5-27](#).

IPC remote flag clear register

Figure 5-8. IPCCLR Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R=0/W=1-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R=0/W=1-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R=0/W=1-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-8. IPCCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC31 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
30	IPC30	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC30 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
29	IPC29	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC29 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
28	IPC28	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC28 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
27	IPC27	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC27 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>

Table 5-8. IPCCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	IPC26	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC26 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
25	IPC25	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC25 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
24	IPC24	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC24 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
23	IPC23	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC23 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
22	IPC22	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC22 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
21	IPC21	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC21 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
20	IPC20	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC20 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
19	IPC19	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC19 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
18	IPC18	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC18 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>

Table 5-8. IPCCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	IPC17	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC17 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
16	IPC16	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC16 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
15	IPC15	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC15 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
14	IPC14	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC14 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
13	IPC13	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC13 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
12	IPC12	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC12 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
11	IPC11	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC11 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
10	IPC10	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC10 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
9	IPC9	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC9 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>

Table 5-8. IPCCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	IPC8	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC8 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
7	IPC7	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC7 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
6	IPC6	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC6 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
5	IPC5	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC5 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
4	IPC4	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC4 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
3	IPC3	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC3 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
2	IPC2	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC2 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
1	IPC1	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC1 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
0	IPC0	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC0 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>

5.2.2.5 IPCFLG Register (offset = 8h) [reset = 0h]

IPCFLG is shown in [Figure 5-27](#) and described in [Table 5-28](#).

IPC remote flag status register

Figure 5-9. IPCFLG Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-9. IPCFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R	0h	Indicates to the local CPU whether the remote IPC31 event flag is set. 0: The remote IPC31 event flag is not set 1: The remote IPC31 event flag is set
30	IPC30	R	0h	Indicates to the local CPU whether the remote IPC30 event flag is set. 0: The remote IPC30 event flag is not set 1: The remote IPC30 event flag is set
29	IPC29	R	0h	Indicates to the local CPU whether the remote IPC29 event flag is set. 0: The remote IPC29 event flag is not set 1: The remote IPC29 event flag is set
28	IPC28	R	0h	Indicates to the local CPU whether the remote IPC28 event flag is set. 0: The remote IPC28 event flag is not set 1: The remote IPC28 event flag is set
27	IPC27	R	0h	Indicates to the local CPU whether the remote IPC27 event flag is set. 0: The remote IPC27 event flag is not set 1: The remote IPC27 event flag is set
26	IPC26	R	0h	Indicates to the local CPU whether the remote IPC26 event flag is set. 0: The remote IPC26 event flag is not set 1: The remote IPC26 event flag is set
25	IPC25	R	0h	Indicates to the local CPU whether the remote IPC25 event flag is set. 0: The remote IPC25 event flag is not set 1: The remote IPC25 event flag is set

Table 5-9. IPCFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	IPC24	R	0h	Indicates to the local CPU whether the remote IPC24 event flag is set. 0: The remote IPC24 event flag is not set 1: The remote IPC24 event flag is set
23	IPC23	R	0h	Indicates to the local CPU whether the remote IPC23 event flag is set. 0: The remote IPC23 event flag is not set 1: The remote IPC23 event flag is set
22	IPC22	R	0h	Indicates to the local CPU whether the remote IPC22 event flag is set. 0: The remote IPC22 event flag is not set 1: The remote IPC22 event flag is set
21	IPC21	R	0h	Indicates to the local CPU whether the remote IPC21 event flag is set. 0: The remote IPC21 event flag is not set 1: The remote IPC21 event flag is set
20	IPC20	R	0h	Indicates to the local CPU whether the remote IPC20 event flag is set. 0: The remote IPC20 event flag is not set 1: The remote IPC20 event flag is set
19	IPC19	R	0h	Indicates to the local CPU whether the remote IPC19 event flag is set. 0: The remote IPC19 event flag is not set 1: The remote IPC19 event flag is set
18	IPC18	R	0h	Indicates to the local CPU whether the remote IPC18 event flag is set. 0: The remote IPC18 event flag is not set 1: The remote IPC18 event flag is set
17	IPC17	R	0h	Indicates to the local CPU whether the remote IPC17 event flag is set. 0: The remote IPC17 event flag is not set 1: The remote IPC17 event flag is set
16	IPC16	R	0h	Indicates to the local CPU whether the remote IPC16 event flag is set. 0: The remote IPC16 event flag is not set 1: The remote IPC16 event flag is set
15	IPC15	R	0h	Indicates to the local CPU whether the remote IPC15 event flag is set. 0: The remote IPC15 event flag is not set 1: The remote IPC15 event flag is set
14	IPC14	R	0h	Indicates to the local CPU whether the remote IPC14 event flag is set. 0: The remote IPC14 event flag is not set 1: The remote IPC14 event flag is set
13	IPC13	R	0h	Indicates to the local CPU whether the remote IPC13 event flag is set. 0: The remote IPC13 event flag is not set 1: The remote IPC13 event flag is set
12	IPC12	R	0h	Indicates to the local CPU whether the remote IPC12 event flag is set. 0: The remote IPC12 event flag is not set 1: The remote IPC12 event flag is set

Table 5-9. IPCFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	IPC11	R	0h	Indicates to the local CPU whether the remote IPC11 event flag is set. 0: The remote IPC11 event flag is not set 1: The remote IPC11 event flag is set
10	IPC10	R	0h	Indicates to the local CPU whether the remote IPC10 event flag is set. 0: The remote IPC10 event flag is not set 1: The remote IPC10 event flag is set
9	IPC9	R	0h	Indicates to the local CPU whether the remote IPC9 event flag is set. 0: The remote IPC9 event flag is not set 1: The remote IPC9 event flag is set
8	IPC8	R	0h	Indicates to the local CPU whether the remote IPC8 event flag is set. 0: The remote IPC8 event flag is not set 1: The remote IPC8 event flag is set
7	IPC7	R	0h	Indicates to the local CPU whether the remote IPC7 event flag is set. 0: The remote IPC7 event flag is not set 1: The remote IPC7 event flag is set
6	IPC6	R	0h	Indicates to the local CPU whether the remote IPC6 event flag is set. 0: The remote IPC6 event flag is not set 1: The remote IPC6 event flag is set
5	IPC5	R	0h	Indicates to the local CPU whether the remote IPC5 event flag is set. 0: The remote IPC5 event flag is not set 1: The remote IPC5 event flag is set
4	IPC4	R	0h	Indicates to the local CPU whether the remote IPC4 event flag is set. 0: The remote IPC4 event flag is not set 1: The remote IPC4 event flag is set
3	IPC3	R	0h	Indicates to the local CPU whether the remote IPC3 event flag is set. 0: The remote IPC3 event flag is not set 1: The remote IPC3 event flag is set Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
2	IPC2	R	0h	Indicates to the local CPU whether the remote IPC2 event flag is set. 0: The remote IPC2 event flag is not set 1: The remote IPC2 event flag is set Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
1	IPC1	R	0h	Indicates to the local CPU whether the remote IPC1 event flag is set. 0: The remote IPC1 event flag is not set 1: The remote IPC1 event flag is set Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
0	IPC0	R	0h	Indicates to the local CPU whether the remote IPC0 event flag is set. 0: The remote IPC0 event flag is not set 1: The remote IPC0 event flag is set Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.

5.2.2.6 IPCCOUNTERL Register (offset = Ch) [reset = 0h]IPCCOUNTERL is shown in [Figure 5-28](#) and described in [Table 5-29](#).

IPC Counter Low Register

Figure 5-10. IPCCOUNTERL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-10. IPCCOUNTERL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R	0h	This is the lower 32-bits of free running 64 bit timestamp counter clocked by the PLLSYSCLK.

5.2.2.7 IPCCOUNTERH Register (offset = Eh) [reset = 0h]

IPCCOUNTERH is shown in [Figure 5-29](#) and described in [Table 5-30](#).

IPC Counter High Register

Figure 5-11. IPCCOUNTERH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-11. IPCCOUNTERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R	0h	This is the upper 32-bits of free running 64 bit timestamp counter clocked by the PLLSYSCLK.

5.2.2.8 IPCSENDCOM Register (offset = 10h) [reset = 0h]

IPCSENDCOM is shown in [Figure 5-34](#) and described in [Table 5-35](#).

Local to Remote IPC Command Register

Figure 5-12. IPCSENDCOM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-12. IPCSENDCOM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMMAND	R/W	0h	<p>This is a general purpose register used to send software-defined commands to the remote CPU. It can only be written by the local CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCSENDCOM is the same physical register as the remote CPU's IPCRECVCOM, and is located at the same address in both CPUs.</p>

5.2.2.9 IPCSENDADDR Register (offset = 12h) [reset = 0h]

IPCSENDADDR is shown in [Figure 5-35](#) and described in [Table 5-36](#).

Local to Remote IPC Address Register

Figure 5-13. IPCSENDADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-13. IPCSENDADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R/W	0h	<p>This is a general purpose register used to send software-defined addresses to the remote CPU. It can only be written by the local CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCSENDADDR is the same physical register as the remote CPU's IPCRECVDATA, and is located at the same address in both CPUs.</p>

5.2.2.10 IPCSENDDATA Register (offset = 14h) [reset = 0h]

IPCSENDDATA is shown in [Figure 5-36](#) and described in [Table 5-37](#).

Local to Remote IPC Data Register

Figure 5-14. IPCSENDDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-14. IPCSENDDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	WDATA	R/W	0h	<p>This is a general purpose register used to send software-defined data to the remote CPU. It can only be written by the local CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCSENDDATA is the same physical register as the remote CPU's IPCRECVDATA, and is located at the same address in both CPUs.</p>

5.2.2.11 IPCREMOTEREPLY Register (offset = 16h) [reset = 0h]

IPCREMOTEREPLY is shown in [Figure 5-37](#) and described in [Table 5-38](#).

Remote to Local IPC Reply Data Register

Figure 5-15. IPCREMOTEREPLY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-15. IPCREMOTEREPLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R	0h	<p>This is a general purpose register used to receive software-defined data from the remote CPU's response to a command. It can only be written by the remote CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCREMOTEREPLY is the same physical register as the remote CPU's IPCLOCALREPLY, and is located at the same address in both CPUs.</p>

5.2.2.12 IPCRECVCOM Register (offset = 18h) [reset = 0h]IPCRECVCOM is shown in [Figure 5-30](#) and described in [Table 5-31](#).

Remote to Local IPC Command Register

Figure 5-16. IPCRECVCOM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-16. IPCRECVCOM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMMAND	R	0h	<p>This is a general purpose register used to receive software-defined commands from the remote CPU. It can only be written by the remote CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCRECVCOM is the same physical register as the remote CPU's IPCSENDCOM, and is located at the same address in both CPUs.</p>

5.2.2.13 IPCRECVADDR Register (offset = 1Ah) [reset = 0h]

IPCRECVADDR is shown in [Figure 5-31](#) and described in [Table 5-32](#).

Remote to Local IPC Address Register

Figure 5-17. IPCRECVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

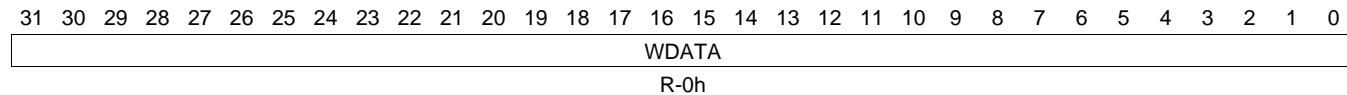
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-17. IPCRECVADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	<p>This is a general purpose register used to receive software-defined addresses from the remote CPU. It can only be written by the remote CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCRECVADDR is the same physical register as the remote CPU's IPCSENDADDR, and is located at the same address in both CPUs.</p>

5.2.2.14 IPCRECVDATA Register (offset = 1Ch) [reset = 0h]IPCRECVDATA is shown in [Figure 5-32](#) and described in [Table 5-33](#).

Remote to Local IPC Data Register

Figure 5-18. IPCRECVDATA Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-18. IPCRECVDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	WDATA	R	0h	<p>This is a general purpose register used to receive software-defined data from the remote CPU. It can only be written by the remote CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCRECVDATA is the same physical register as the remote CPU's IPCSENDDATA, and is located at the same address in both CPUs.</p>

5.2.2.15 IPCLOCALREPLY Register (offset = 1Eh) [reset = 0h]

IPCLOCALREPLY is shown in [Figure 5-33](#) and described in [Table 5-34](#).

Local to Remote IPC Reply Data Register

Figure 5-19. IPCLOCALREPLY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-19. IPCLOCALREPLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R/W	0h	<p>This is a general purpose register used to send software-defined data to the remote CPU in response to a command. It can only be written by the local CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCLOCALREPLY is the same physical register as the remote CPU's IPCREMOTEREPLY, and is located at the same address in both CPUs.</p>

5.2.2.16 IPCBOOTSTS Register (offset = 20h) [reset = 0h]IPCBOOTSTS is shown in [Figure 5-38](#) and described in [Table 5-39](#).

CPU2 to CPU1 IPC Boot Status Register

Figure 5-20. IPCBOOTSTS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTSTS																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-20. IPCBOOTSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BOOTSTS	R/W	0h	This register is used by CPU2 to pass the boot Status to CPU1. The data format is software-defined. It can only be written by CPU2.

5.2.2.17 IPCBOOTMODE Register (offset = 22h) [reset = 0h]

IPCBOOTMODE is shown in [Figure 5-39](#) and described in [Table 5-40](#).

CPU1 to CPU2 IPC Boot Mode Register

Figure 5-21. IPCBOOTMODE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTMODE																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-21. IPCBOOTMODE Register Field Descriptions

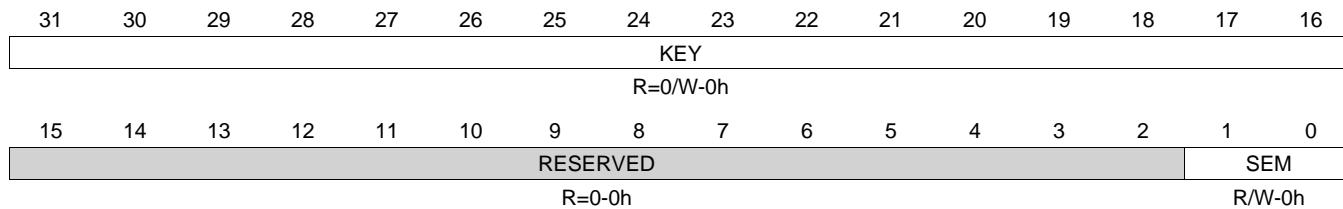
Bit	Field	Type	Reset	Description
31-0	BOOTMODE	R/W	0h	This register is used by CPU1 to pass a boot mode information to CPU2. The data format is software-defined. It can only be written by CPU1.

5.2.2.18 PUMPREQUEST Register (offset = 24h) [reset = 0h]

PUMPREQUEST is shown in [Figure 5-40](#) and described in [Table 5-41](#).

Flash programming semaphore PUMP request register

Figure 5-22. PUMPREQUEST Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-22. PUMPREQUEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R=0/W	0h	In order to write to the semaphore bits, 0x5a5a must be written to these key bits at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every semaphore change.
15-2	RESERVED	R=0	0h	Reserved
1-0	SEM	R/W	0h	These bits decide which CPU has control of the flash pump, which allows write access to the flash memory. The possible values are: 00 or 11: Read-only state. CPU1 has control of the pump, but CPU2 may seize control at any time. 01: CPU2 has exclusive control of the pump and of these semaphore bits. CPU2 can relinquish control by setting the bits back to 00 or 11. 10: CPU1 has exclusive control of the pump and of these semaphore bits. CPU1 can relinquish control by setting the bits back to 00 or 11. Going from 01->10 or 10->01 is not allowed. Going from 00->11 or 11->00 is allowed, but has no effect. The semaphore bits [1:0] must be written along with the correct key in bits [31:16].

5.2.3 IPC_REGS_CPU2 Registers

Table 5-23 lists the memory-mapped registers for the IPC_REGS_CPU2. All register offset addresses not listed in **Table 5-23** should be considered as reserved locations and the register contents should not be modified.

Table 5-23. IPC_REGS_CPU2 REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	IPCACK	IPC incoming flag clear (acknowledge) register	Section 5.2.3.1	
2h	IPCSTS	IPC incoming flag status register	Section 5.2.3.2	
4h	IPCSET	IPC remote flag set register	Section 5.2.3.3	
6h	IPCCCLR	IPC remote flag clear register	Section 5.2.3.4	
8h	IPCFLG	IPC remote flag status register	Section 5.2.3.5	
Ch	IPCCOUNTERL	IPC Counter Low Register	Section 5.2.3.6	
Eh	IPCCOUNTERH	IPC Counter High Register	Section 5.2.3.7	
10h	IPCRECVCOM	Remote to Local IPC Command Register	Section 5.2.3.8	
12h	IPCRECVADDR	Remote to Local IPC Address Register	Section 5.2.3.9	
14h	IPCRECVDATA	Remote to Local IPC Data Register	Section 5.2.3.10	
16h	IPCLOCALREPLY	Local to Remote IPC Reply Data Register	Section 5.2.3.11	
18h	IPCSENDCOM	Local to Remote IPC Command Register	Section 5.2.3.12	
1Ah	IPCSENDADDR	Local to Remote IPC Address Register	Section 5.2.3.13	
1Ch	IPCSENDDATA	Local to Remote IPC Data Register	Section 5.2.3.14	
1Eh	IPCREMOTEREPLY	Remote to Local IPC Reply Data Register	Section 5.2.3.15	
20h	IPCBOOTSTS	CPU2 to CPU1 IPC Boot Status Register	Section 5.2.3.16	
22h	IPCBOOTMODE	CPU1 to CPU2 IPC Boot Mode Register	Section 5.2.3.17	
24h	PUMPREQUEST	Flash programming semaphore PUMP request register	Section 5.2.3.18	EALLOW

5.2.3.1 IPCACK Register (offset = 0h) [reset = 0h]

IPCACK is shown in [Figure 5-23](#) and described in [Table 5-24](#).

IPC incoming flag clear (acknowledge) register

Figure 5-23. IPCACK Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R=0/W=1-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R=0/W=1-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R=0/W=1-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-24. IPCACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R=0/W=1	0h	Writing 1 to this bit clears the IPC31 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
30	IPC30	R=0/W=1	0h	Writing 1 to this bit clears the IPC30 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
29	IPC29	R=0/W=1	0h	Writing 1 to this bit clears the IPC29 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
28	IPC28	R=0/W=1	0h	Writing 1 to this bit clears the IPC28 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
27	IPC27	R=0/W=1	0h	Writing 1 to this bit clears the IPC27 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
26	IPC26	R=0/W=1	0h	Writing 1 to this bit clears the IPC26 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
25	IPC25	R=0/W=1	0h	Writing 1 to this bit clears the IPC25 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
24	IPC24	R=0/W=1	0h	Writing 1 to this bit clears the IPC24 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
23	IPC23	R=0/W=1	0h	Writing 1 to this bit clears the IPC23 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
22	IPC22	R=0/W=1	0h	Writing 1 to this bit clears the IPC22 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.

Table 5-24. IPCACK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	IPC21	R=0/W=1	0h	Writing 1 to this bit clears the IPC21 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
20	IPC20	R=0/W=1	0h	Writing 1 to this bit clears the IPC20 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
19	IPC19	R=0/W=1	0h	Writing 1 to this bit clears the IPC19 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
18	IPC18	R=0/W=1	0h	Writing 1 to this bit clears the IPC18 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
17	IPC17	R=0/W=1	0h	Writing 1 to this bit clears the IPC17 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
16	IPC16	R=0/W=1	0h	Writing 1 to this bit clears the IPC16 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
15	IPC15	R=0/W=1	0h	Writing 1 to this bit clears the IPC15 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
14	IPC14	R=0/W=1	0h	Writing 1 to this bit clears the IPC14 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
13	IPC13	R=0/W=1	0h	Writing 1 to this bit clears the IPC13 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
12	IPC12	R=0/W=1	0h	Writing 1 to this bit clears the IPC12 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
11	IPC11	R=0/W=1	0h	Writing 1 to this bit clears the IPC11 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
10	IPC10	R=0/W=1	0h	Writing 1 to this bit clears the IPC10 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
9	IPC9	R=0/W=1	0h	Writing 1 to this bit clears the IPC9 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
8	IPC8	R=0/W=1	0h	Writing 1 to this bit clears the IPC8 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
7	IPC7	R=0/W=1	0h	Writing 1 to this bit clears the IPC7 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
6	IPC6	R=0/W=1	0h	Writing 1 to this bit clears the IPC6 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
5	IPC5	R=0/W=1	0h	Writing 1 to this bit clears the IPC5 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.

Table 5-24. IPCACK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IPC4	R=0/W=1	0h	Writing 1 to this bit clears the IPC4 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
3	IPC3	R=0/W=1	0h	Writing 1 to this bit clears the IPC3 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
2	IPC2	R=0/W=1	0h	Writing 1 to this bit clears the IPC2 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
1	IPC1	R=0/W=1	0h	Writing 1 to this bit clears the IPC1 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.
0	IPC0	R=0/W=1	0h	Writing 1 to this bit clears the IPC0 event flag which was set by the remote CPU. Writing 0 to this bit has no effect.

5.2.3.2 IPCSTS Register (offset = 2h) [reset = 0h]

IPCSTS is shown in [Figure 5-24](#) and described in [Table 5-25](#).

IPC incoming flag status register

Figure 5-24. IPCSTS Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-25. IPCSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R	0h	Indicates to the local CPU if the IPC31 event flag was set by the remote CPU. 0: No IPC31 event was set by the remote CPU 1: An IPC31 event was set by the remote CPU
30	IPC30	R	0h	Indicates to the local CPU if the IPC30 event flag was set by the remote CPU. 0: No IPC30 event was set by the remote CPU 1: An IPC30 event was set by the remote CPU
29	IPC29	R	0h	Indicates to the local CPU if the IPC29 event flag was set by the remote CPU. 0: No IPC29 event was set by the remote CPU 1: An IPC29 event was set by the remote CPU
28	IPC28	R	0h	Indicates to the local CPU if the IPC28 event flag was set by the remote CPU. 0: No IPC28 event was set by the remote CPU 1: An IPC28 event was set by the remote CPU
27	IPC27	R	0h	Indicates to the local CPU if the IPC27 event flag was set by the remote CPU. 0: No IPC27 event was set by the remote CPU 1: An IPC27 event was set by the remote CPU
26	IPC26	R	0h	Indicates to the local CPU if the IPC26 event flag was set by the remote CPU. 0: No IPC26 event was set by the remote CPU 1: An IPC26 event was set by the remote CPU
25	IPC25	R	0h	Indicates to the local CPU if the IPC25 event flag was set by the remote CPU. 0: No IPC25 event was set by the remote CPU 1: An IPC25 event was set by the remote CPU

Table 5-25. IPCSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	IPC24	R	0h	Indicates to the local CPU if the IPC24 event flag was set by the remote CPU. 0: No IPC24 event was set by the remote CPU 1: An IPC24 event was set by the remote CPU
23	IPC23	R	0h	Indicates to the local CPU if the IPC23 event flag was set by the remote CPU. 0: No IPC23 event was set by the remote CPU 1: An IPC23 event was set by the remote CPU
22	IPC22	R	0h	Indicates to the local CPU if the IPC22 event flag was set by the remote CPU. 0: No IPC22 event was set by the remote CPU 1: An IPC22 event was set by the remote CPU
21	IPC21	R	0h	Indicates to the local CPU if the IPC21 event flag was set by the remote CPU. 0: No IPC21 event was set by the remote CPU 1: An IPC21 event was set by the remote CPU
20	IPC20	R	0h	Indicates to the local CPU if the IPC20 event flag was set by the remote CPU. 0: No IPC20 event was set by the remote CPU 1: An IPC20 event was set by the remote CPU
19	IPC19	R	0h	Indicates to the local CPU if the IPC19 event flag was set by the remote CPU. 0: No IPC19 event was set by the remote CPU 1: An IPC19 event was set by the remote CPU
18	IPC18	R	0h	Indicates to the local CPU if the IPC18 event flag was set by the remote CPU. 0: No IPC18 event was set by the remote CPU 1: An IPC18 event was set by the remote CPU
17	IPC17	R	0h	Indicates to the local CPU if the IPC17 event flag was set by the remote CPU. 0: No IPC17 event was set by the remote CPU 1: An IPC17 event was set by the remote CPU
16	IPC16	R	0h	Indicates to the local CPU if the IPC16 event flag was set by the remote CPU. 0: No IPC16 event was set by the remote CPU 1: An IPC16 event was set by the remote CPU
15	IPC15	R	0h	Indicates to the local CPU if the IPC15 event flag was set by the remote CPU. 0: No IPC15 event was set by the remote CPU 1: An IPC15 event was set by the remote CPU
14	IPC14	R	0h	Indicates to the local CPU if the IPC14 event flag was set by the remote CPU. 0: No IPC14 event was set by the remote CPU 1: An IPC14 event was set by the remote CPU
13	IPC13	R	0h	Indicates to the local CPU if the IPC13 event flag was set by the remote CPU. 0: No IPC13 event was set by the remote CPU 1: An IPC13 event was set by the remote CPU
12	IPC12	R	0h	Indicates to the local CPU if the IPC12 event flag was set by the remote CPU. 0: No IPC12 event was set by the remote CPU 1: An IPC12 event was set by the remote CPU

Table 5-25. IPCSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	IPC11	R	0h	Indicates to the local CPU if the IPC11 event flag was set by the remote CPU. 0: No IPC11 event was set by the remote CPU 1: An IPC11 event was set by the remote CPU
10	IPC10	R	0h	Indicates to the local CPU if the IPC10 event flag was set by the remote CPU. 0: No IPC10 event was set by the remote CPU 1: An IPC10 event was set by the remote CPU
9	IPC9	R	0h	Indicates to the local CPU if the IPC9 event flag was set by the remote CPU. 0: No IPC9 event was set by the remote CPU 1: An IPC9 event was set by the remote CPU
8	IPC8	R	0h	Indicates to the local CPU if the IPC8 event flag was set by the remote CPU. 0: No IPC8 event was set by the remote CPU 1: An IPC8 event was set by the remote CPU
7	IPC7	R	0h	Indicates to the local CPU if the IPC7 event flag was set by the remote CPU. 0: No IPC7 event was set by the remote CPU 1: An IPC7 event was set by the remote CPU
6	IPC6	R	0h	Indicates to the local CPU if the IPC6 event flag was set by the remote CPU. 0: No IPC6 event was set by the remote CPU 1: An IPC6 event was set by the remote CPU
5	IPC5	R	0h	Indicates to the local CPU if the IPC5 event flag was set by the remote CPU. 0: No IPC5 event was set by the remote CPU 1: An IPC5 event was set by the remote CPU
4	IPC4	R	0h	Indicates to the local CPU if the IPC4 event flag was set by the remote CPU. 0: No IPC4 event was set by the remote CPU 1: An IPC4 event was set by the remote CPU
3	IPC3	R	0h	Indicates to the local CPU if the IPC3 event flag was set by the remote CPU. 0: No IPC3 event was set by the remote CPU 1: An IPC3 event was set by the remote CPU Notes [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
2	IPC2	R	0h	Indicates to the local CPU if the IPC2 event flag was set by the remote CPU. 0: No IPC2 event was set by the remote CPU 1: An IPC2 event was set by the remote CPU Notes [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
1	IPC1	R	0h	Indicates to the local CPU if the IPC1 event flag was set by the remote CPU. 0: No IPC1 event was set by the remote CPU 1: An IPC1 event was set by the remote CPU Notes [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.

Table 5-25. IPCSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IPC0	R	0h	<p>Indicates to the local CPU if the IPC0 event flag was set by the remote CPU.</p> <p>0: No IPC0 event was set by the remote CPU</p> <p>1: An IPC0 event was set by the remote CPU</p> <p>Notes</p> <p>[1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.</p>

5.2.3.3 IPCSET Register (offset = 4h) [reset = 0h]

IPCSET is shown in [Figure 5-25](#) and described in [Table 5-26](#).

IPC remote flag set register

Figure 5-25. IPCSET Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R=0/W=1-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R=0/W=1-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R=0/W=1-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-26. IPCSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R=0/W=1	0h	Writing 1 to this bit sets the IPC31 event flag for the remote CPU. Writing 0 has no effect.
30	IPC30	R=0/W=1	0h	Writing 1 to this bit sets the IPC30 event flag for the remote CPU. Writing 0 has no effect.
29	IPC29	R=0/W=1	0h	Writing 1 to this bit sets the IPC29 event flag for the remote CPU. Writing 0 has no effect.
28	IPC28	R=0/W=1	0h	Writing 1 to this bit sets the IPC28 event flag for the remote CPU. Writing 0 has no effect.
27	IPC27	R=0/W=1	0h	Writing 1 to this bit sets the IPC27 event flag for the remote CPU. Writing 0 has no effect.
26	IPC26	R=0/W=1	0h	Writing 1 to this bit sets the IPC26 event flag for the remote CPU. Writing 0 has no effect.
25	IPC25	R=0/W=1	0h	Writing 1 to this bit sets the IPC25 event flag for the remote CPU. Writing 0 has no effect.
24	IPC24	R=0/W=1	0h	Writing 1 to this bit sets the IPC24 event flag for the remote CPU. Writing 0 has no effect.
23	IPC23	R=0/W=1	0h	Writing 1 to this bit sets the IPC23 event flag for the remote CPU. Writing 0 has no effect.
22	IPC22	R=0/W=1	0h	Writing 1 to this bit sets the IPC22 event flag for the remote CPU. Writing 0 has no effect.
21	IPC21	R=0/W=1	0h	Writing 1 to this bit sets the IPC21 event flag for the remote CPU. Writing 0 has no effect.
20	IPC20	R=0/W=1	0h	Writing 1 to this bit sets the IPC20 event flag for the remote CPU. Writing 0 has no effect.
19	IPC19	R=0/W=1	0h	Writing 1 to this bit sets the IPC19 event flag for the remote CPU. Writing 0 has no effect.

Table 5-26. IPCSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	IPC18	R=0/W=1	0h	Writing 1 to this bit sets the IPC18 event flag for the remote CPU. Writing 0 has no effect.
17	IPC17	R=0/W=1	0h	Writing 1 to this bit sets the IPC17 event flag for the remote CPU. Writing 0 has no effect.
16	IPC16	R=0/W=1	0h	Writing 1 to this bit sets the IPC16 event flag for the remote CPU. Writing 0 has no effect.
15	IPC15	R=0/W=1	0h	Writing 1 to this bit sets the IPC15 event flag for the remote CPU. Writing 0 has no effect.
14	IPC14	R=0/W=1	0h	Writing 1 to this bit sets the IPC14 event flag for the remote CPU. Writing 0 has no effect.
13	IPC13	R=0/W=1	0h	Writing 1 to this bit sets the IPC13 event flag for the remote CPU. Writing 0 has no effect.
12	IPC12	R=0/W=1	0h	Writing 1 to this bit sets the IPC12 event flag for the remote CPU. Writing 0 has no effect.
11	IPC11	R=0/W=1	0h	Writing 1 to this bit sets the IPC11 event flag for the remote CPU. Writing 0 has no effect.
10	IPC10	R=0/W=1	0h	Writing 1 to this bit sets the IPC10 event flag for the remote CPU. Writing 0 has no effect.
9	IPC9	R=0/W=1	0h	Writing 1 to this bit sets the IPC9 event flag for the remote CPU. Writing 0 has no effect.
8	IPC8	R=0/W=1	0h	Writing 1 to this bit sets the IPC8 event flag for the remote CPU. Writing 0 has no effect.
7	IPC7	R=0/W=1	0h	Writing 1 to this bit sets the IPC7 event flag for the remote CPU. Writing 0 has no effect.
6	IPC6	R=0/W=1	0h	Writing 1 to this bit sets the IPC6 event flag for the remote CPU. Writing 0 has no effect.
5	IPC5	R=0/W=1	0h	Writing 1 to this bit sets the IPC5 event flag for the remote CPU. Writing 0 has no effect.
4	IPC4	R=0/W=1	0h	Writing 1 to this bit sets the IPC4 event flag for the remote CPU. Writing 0 has no effect.
3	IPC3	R=0/W=1	0h	Writing 1 to this bit sets the IPC3 event flag for the remote CPU. Writing 0 has no effect. Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
2	IPC2	R=0/W=1	0h	Writing 1 to this bit sets the IPC2 event flag for the remote CPU. Writing 0 has no effect. Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
1	IPC1	R=0/W=1	0h	Writing 1 to this bit sets the IPC1 event flag for the remote CPU. Writing 0 has no effect. Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.

Table 5-26. IPCSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IPC0	R=0/W=1	0h	<p>Writing 1 to this bit sets the IPC0 event flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.</p>

5.2.3.4 IPCCLR Register (offset = 6h) [reset = 0h]

IPCCLR is shown in [Figure 5-26](#) and described in [Table 5-27](#).

IPC remote flag clear register

Figure 5-26. IPCCLR Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R=0/W=1-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R=0/W=1-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R=0/W=1-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-27. IPCCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC31 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
30	IPC30	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC30 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
29	IPC29	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC29 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
28	IPC28	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC28 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
27	IPC27	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC27 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>

Table 5-27. IPCCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	IPC26	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC26 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
25	IPC25	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC25 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
24	IPC24	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC24 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
23	IPC23	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC23 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
22	IPC22	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC22 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
21	IPC21	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC21 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
20	IPC20	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC20 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
19	IPC19	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC19 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
18	IPC18	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC18 flag for the remote CPU.</p> <p>Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>

Table 5-27. IPCCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	IPC17	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC17 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
16	IPC16	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC16 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
15	IPC15	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC15 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
14	IPC14	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC14 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
13	IPC13	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC13 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
12	IPC12	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC12 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
11	IPC11	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC11 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
10	IPC10	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC10 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
9	IPC9	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC9 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>

Table 5-27. IPCCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	IPC8	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC8 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
7	IPC7	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC7 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
6	IPC6	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC6 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
5	IPC5	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC5 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
4	IPC4	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC4 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
3	IPC3	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC3 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
2	IPC2	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC2 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
1	IPC1	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC1 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>
0	IPC0	R=0/W=1	0h	<p>Writing 1 to this bit clears the IPC0 flag for the remote CPU. Writing 0 has no effect.</p> <p>Notes:</p> <p>[1] Normally, each CPU will clear (acknowledge) only its own local flags. This mechanism may be useful if the remote CPU is non-responsive.</p>

5.2.3.5 IPCFLG Register (offset = 8h) [reset = 0h]IPCFLG is shown in [Figure 5-27](#) and described in [Table 5-28](#).

IPC remote flag status register

Figure 5-27. IPCFLG Register

31	30	29	28	27	26	25	24
IPC31	IPC30	IPC29	IPC28	IPC27	IPC26	IPC25	IPC24
R-0h							
23	22	21	20	19	18	17	16
IPC23	IPC22	IPC21	IPC20	IPC19	IPC18	IPC17	IPC16
R-0h							
15	14	13	12	11	10	9	8
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8
R-0h							
7	6	5	4	3	2	1	0
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-28. IPCFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPC31	R	0h	Indicates to the local CPU whether the remote IPC31 event flag is set. 0: The remote IPC31 event flag is not set 1: The remote IPC31 event flag is set
30	IPC30	R	0h	Indicates to the local CPU whether the remote IPC30 event flag is set. 0: The remote IPC30 event flag is not set 1: The remote IPC30 event flag is set
29	IPC29	R	0h	Indicates to the local CPU whether the remote IPC29 event flag is set. 0: The remote IPC29 event flag is not set 1: The remote IPC29 event flag is set
28	IPC28	R	0h	Indicates to the local CPU whether the remote IPC28 event flag is set. 0: The remote IPC28 event flag is not set 1: The remote IPC28 event flag is set
27	IPC27	R	0h	Indicates to the local CPU whether the remote IPC27 event flag is set. 0: The remote IPC27 event flag is not set 1: The remote IPC27 event flag is set
26	IPC26	R	0h	Indicates to the local CPU whether the remote IPC26 event flag is set. 0: The remote IPC26 event flag is not set 1: The remote IPC26 event flag is set
25	IPC25	R	0h	Indicates to the local CPU whether the remote IPC25 event flag is set. 0: The remote IPC25 event flag is not set 1: The remote IPC25 event flag is set

Table 5-28. IPCFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	IPC24	R	0h	Indicates to the local CPU whether the remote IPC24 event flag is set. 0: The remote IPC24 event flag is not set 1: The remote IPC24 event flag is set
23	IPC23	R	0h	Indicates to the local CPU whether the remote IPC23 event flag is set. 0: The remote IPC23 event flag is not set 1: The remote IPC23 event flag is set
22	IPC22	R	0h	Indicates to the local CPU whether the remote IPC22 event flag is set. 0: The remote IPC22 event flag is not set 1: The remote IPC22 event flag is set
21	IPC21	R	0h	Indicates to the local CPU whether the remote IPC21 event flag is set. 0: The remote IPC21 event flag is not set 1: The remote IPC21 event flag is set
20	IPC20	R	0h	Indicates to the local CPU whether the remote IPC20 event flag is set. 0: The remote IPC20 event flag is not set 1: The remote IPC20 event flag is set
19	IPC19	R	0h	Indicates to the local CPU whether the remote IPC19 event flag is set. 0: The remote IPC19 event flag is not set 1: The remote IPC19 event flag is set
18	IPC18	R	0h	Indicates to the local CPU whether the remote IPC18 event flag is set. 0: The remote IPC18 event flag is not set 1: The remote IPC18 event flag is set
17	IPC17	R	0h	Indicates to the local CPU whether the remote IPC17 event flag is set. 0: The remote IPC17 event flag is not set 1: The remote IPC17 event flag is set
16	IPC16	R	0h	Indicates to the local CPU whether the remote IPC16 event flag is set. 0: The remote IPC16 event flag is not set 1: The remote IPC16 event flag is set
15	IPC15	R	0h	Indicates to the local CPU whether the remote IPC15 event flag is set. 0: The remote IPC15 event flag is not set 1: The remote IPC15 event flag is set
14	IPC14	R	0h	Indicates to the local CPU whether the remote IPC14 event flag is set. 0: The remote IPC14 event flag is not set 1: The remote IPC14 event flag is set
13	IPC13	R	0h	Indicates to the local CPU whether the remote IPC13 event flag is set. 0: The remote IPC13 event flag is not set 1: The remote IPC13 event flag is set
12	IPC12	R	0h	Indicates to the local CPU whether the remote IPC12 event flag is set. 0: The remote IPC12 event flag is not set 1: The remote IPC12 event flag is set

Table 5-28. IPCFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	IPC11	R	0h	Indicates to the local CPU whether the remote IPC11 event flag is set. 0: The remote IPC11 event flag is not set 1: The remote IPC11 event flag is set
10	IPC10	R	0h	Indicates to the local CPU whether the remote IPC10 event flag is set. 0: The remote IPC10 event flag is not set 1: The remote IPC10 event flag is set
9	IPC9	R	0h	Indicates to the local CPU whether the remote IPC9 event flag is set. 0: The remote IPC9 event flag is not set 1: The remote IPC9 event flag is set
8	IPC8	R	0h	Indicates to the local CPU whether the remote IPC8 event flag is set. 0: The remote IPC8 event flag is not set 1: The remote IPC8 event flag is set
7	IPC7	R	0h	Indicates to the local CPU whether the remote IPC7 event flag is set. 0: The remote IPC7 event flag is not set 1: The remote IPC7 event flag is set
6	IPC6	R	0h	Indicates to the local CPU whether the remote IPC6 event flag is set. 0: The remote IPC6 event flag is not set 1: The remote IPC6 event flag is set
5	IPC5	R	0h	Indicates to the local CPU whether the remote IPC5 event flag is set. 0: The remote IPC5 event flag is not set 1: The remote IPC5 event flag is set
4	IPC4	R	0h	Indicates to the local CPU whether the remote IPC4 event flag is set. 0: The remote IPC4 event flag is not set 1: The remote IPC4 event flag is set
3	IPC3	R	0h	Indicates to the local CPU whether the remote IPC3 event flag is set. 0: The remote IPC3 event flag is not set 1: The remote IPC3 event flag is set Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
2	IPC2	R	0h	Indicates to the local CPU whether the remote IPC2 event flag is set. 0: The remote IPC2 event flag is not set 1: The remote IPC2 event flag is set Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
1	IPC1	R	0h	Indicates to the local CPU whether the remote IPC1 event flag is set. 0: The remote IPC1 event flag is not set 1: The remote IPC1 event flag is set Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.
0	IPC0	R	0h	Indicates to the local CPU whether the remote IPC0 event flag is set. 0: The remote IPC0 event flag is not set 1: The remote IPC0 event flag is set Notes: [1] IPC event flags 0-3 will trigger interrupts in the receiving CPU via the ePIE.

5.2.3.6 IPCCOUNTERL Register (offset = Ch) [reset = 0h]

IPCCOUNTERL is shown in [Figure 5-28](#) and described in [Table 5-29](#).

IPC Counter Low Register

Figure 5-28. IPCCOUNTERL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-29. IPCCOUNTERL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R	0h	This is the lower 32-bits of free running 64 bit timestamp counter clocked by the PLLSYSCLK.

5.2.3.7 IPCCOUNTERH Register (offset = Eh) [reset = 0h]IPCCOUNTERH is shown in [Figure 5-29](#) and described in [Table 5-30](#).

IPC Counter High Register

Figure 5-29. IPCCOUNTERH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-30. IPCCOUNTERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R	0h	This is the upper 32-bits of free running 64 bit timestamp counter clocked by the PLLSYSCLK.

5.2.3.8 IPCRECVCOM Register (offset = 10h) [reset = 0h]

IPCRECVCOM is shown in [Figure 5-30](#) and described in [Table 5-31](#).

Remote to Local IPC Command Register

Figure 5-30. IPCRECVCOM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-31. IPCRECVCOM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMMAND	R	0h	<p>This is a general purpose register used to receive software-defined commands from the remote CPU. It can only be written by the remote CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCRECVCOM is the same physical register as the remote CPU's IPCSENDCOM, and is located at the same address in both CPUs.</p>

5.2.3.9 IPCRECVADDR Register (offset = 12h) [reset = 0h]IPCRECVADDR is shown in [Figure 5-31](#) and described in [Table 5-32](#).

Remote to Local IPC Address Register

Figure 5-31. IPCRECVADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-32. IPCRECVADDR Register Field Descriptions

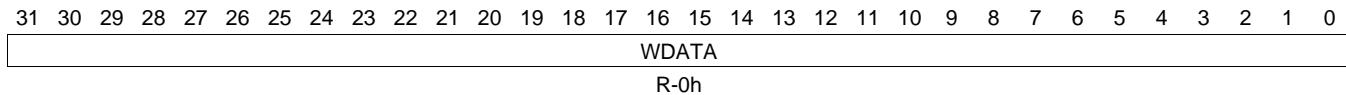
Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	<p>This is a general purpose register used to receive software-defined addresses from the remote CPU. It can only be written by the remote CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCRECVADDR is the same physical register as the remote CPU's IPCSENDADDR, and is located at the same address in both CPUs.</p>

5.2.3.10 IPCRECVDATA Register (offset = 14h) [reset = 0h]

IPCRECVDATA is shown in [Figure 5-32](#) and described in [Table 5-33](#).

Remote to Local IPC Data Register

Figure 5-32. IPCRECVDATA Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-33. IPCRECVDATA Register Field Descriptions

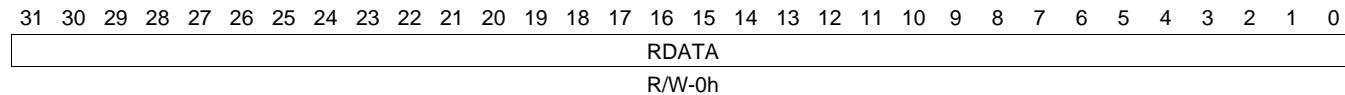
Bit	Field	Type	Reset	Description
31-0	WDATA	R	0h	<p>This is a general purpose register used to receive software-defined data from the remote CPU. It can only be written by the remote CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCRECVDATA is the same physical register as the remote CPU's IPCSENDDATA, and is located at the same address in both CPUs.</p>

5.2.3.11 IPCLOCALREPLY Register (offset = 16h) [reset = 0h]

IPCLOCALREPLY is shown in [Figure 5-33](#) and described in [Table 5-34](#).

Local to Remote IPC Reply Data Register

Figure 5-33. IPCLOCALREPLY Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-34. IPCLOCALREPLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R/W	0h	<p>This is a general purpose register used to send software-defined data to the remote CPU in response to a command. It can only be written by the local CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCLOCALREPLY is the same physical register as the remote CPU's IPCREMOTEREPLY, and is located at the same address in both CPUs.</p>

5.2.3.12 IPCSENDCOM Register (offset = 18h) [reset = 0h]

IPCSENDCOM is shown in [Figure 5-34](#) and described in [Table 5-35](#).

Local to Remote IPC Command Register

Figure 5-34. IPCSENDCOM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-35. IPCSENDCOM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMMAND	R/W	0h	<p>This is a general purpose register used to send software-defined commands to the remote CPU. It can only be written by the local CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCSENDCOM is the same physical register as the remote CPU's IPCRECVCOM, and is located at the same address in both CPUs.</p>

5.2.3.13 IPCSENDADDR Register (offset = 1Ah) [reset = 0h]IPCSENDADDR is shown in [Figure 5-35](#) and described in [Table 5-36](#).

Local to Remote IPC Address Register

Figure 5-35. IPCSENDADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-36. IPCSENDADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R/W	0h	<p>This is a general purpose register used to send software-defined addresses to the remote CPU. It can only be written by the local CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCSENDADDR is the same physical register as the remote CPU's IPCRECVDATA, and is located at the same address in both CPUs.</p>

5.2.3.14 IPCSENDDATA Register (offset = 1Ch) [reset = 0h]

IPCSENDDATA is shown in [Figure 5-36](#) and described in [Table 5-37](#).

Local to Remote IPC Data Register

Figure 5-36. IPCSENDDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-37. IPCSENDDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	WDATA	R/W	0h	<p>This is a general purpose register used to send software-defined data to the remote CPU. It can only be written by the local CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCSENDDATA is the same physical register as the remote CPU's IPCRECVDATA, and is located at the same address in both CPUs.</p>

5.2.3.15 IPCREMOTEREPLY Register (offset = 1Eh) [reset = 0h]IPCREMOTEREPLY is shown in [Figure 5-37](#) and described in [Table 5-38](#).

Remote to Local IPC Reply Data Register

Figure 5-37. IPCREMOTEREPLY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-38. IPCREMOTEREPLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R	0h	<p>This is a general purpose register used to receive software-defined data from the remote CPU's response to a command. It can only be written by the remote CPU.</p> <p>Notes</p> <p>[1] The local CPU's IPCREMOTEREPLY is the same physical register as the remote CPU's IPCLOCALREPLY, and is located at the same address in both CPUs.</p>

5.2.3.16 IPCBOOTSTS Register (offset = 20h) [reset = 0h]

IPCBOOTSTS is shown in [Figure 5-38](#) and described in [Table 5-39](#).

CPU2 to CPU1 IPC Boot Status Register

Figure 5-38. IPCBOOTSTS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTSTS																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-39. IPCBOOTSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BOOTSTS	R/W	0h	This register is used by CPU2 to pass the boot Status to CPU1. The data format is software-defined. It can only be written by CPU2.

5.2.3.17 IPCBOOTMODE Register (offset = 22h) [reset = 0h]IPCBOOTMODE is shown in [Figure 5-39](#) and described in [Table 5-40](#).

CPU1 to CPU2 IPC Boot Mode Register

Figure 5-39. IPCBOOTMODE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTMODE																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-40. IPCBOOTMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BOOTMODE	R/W	0h	This register is used by CPU1 to pass a boot mode information to CPU2. The data format is software-defined. It can only be written by CPU1.

5.2.3.18 PUMPREQUEST Register (offset = 24h) [reset = 0h]

PUMPREQUEST is shown in [Figure 5-40](#) and described in [Table 5-41](#).

Flash programming semaphore PUMP request register

Figure 5-40. PUMPREQUEST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY															
R=0/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SEM
R=0-0h															R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 5-41. PUMPREQUEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R=0/W	0h	In order to write to the semaphore bits, 0x5a5a must be written to these key bits at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every semaphore change.
15-2	RESERVED	R=0	0h	Reserved
1-0	SEM	R/W	0h	These bits decide which CPU has control of the flash pump, which allows write access to the flash memory. The possible values are: 00 or 11: Read-only state. CPU1 has control of the pump, but CPU2 may seize control at any time. 01: CPU2 has exclusive control of the pump and of these semaphore bits. CPU2 can relinquish control by setting the bits back to 00 or 11. 10: CPU1 has exclusive control of the pump and of these semaphore bits. CPU1 can relinquish control by setting the bits back to 00 or 11. Going from 01->10 or 10->01 is not allowed. Going from 00->11 or 11->00 is allowed, but has no effect. The semaphore bits [1:0] must be written along with the correct key in bits [31:16].

General-Purpose Input/Output (GPIO)

The GPIO module provides control over the device's digital I/O MUX, which uses shared pins to maximize application flexibility. The pins are named by their general-purpose I/O name (for example, GPIO0, GPIO25, GPIO58). These pins can be individually selected to operate as digital I/O (also called GPIO mode), or connected to one of several peripheral I/O signals. You can qualify the input signals to remove unwanted noise.

Topic		Page
6.1	GPIO Overview	854
6.2	Output X-BAR	863
6.3	Input X-BAR	865
6.4	Registers	868

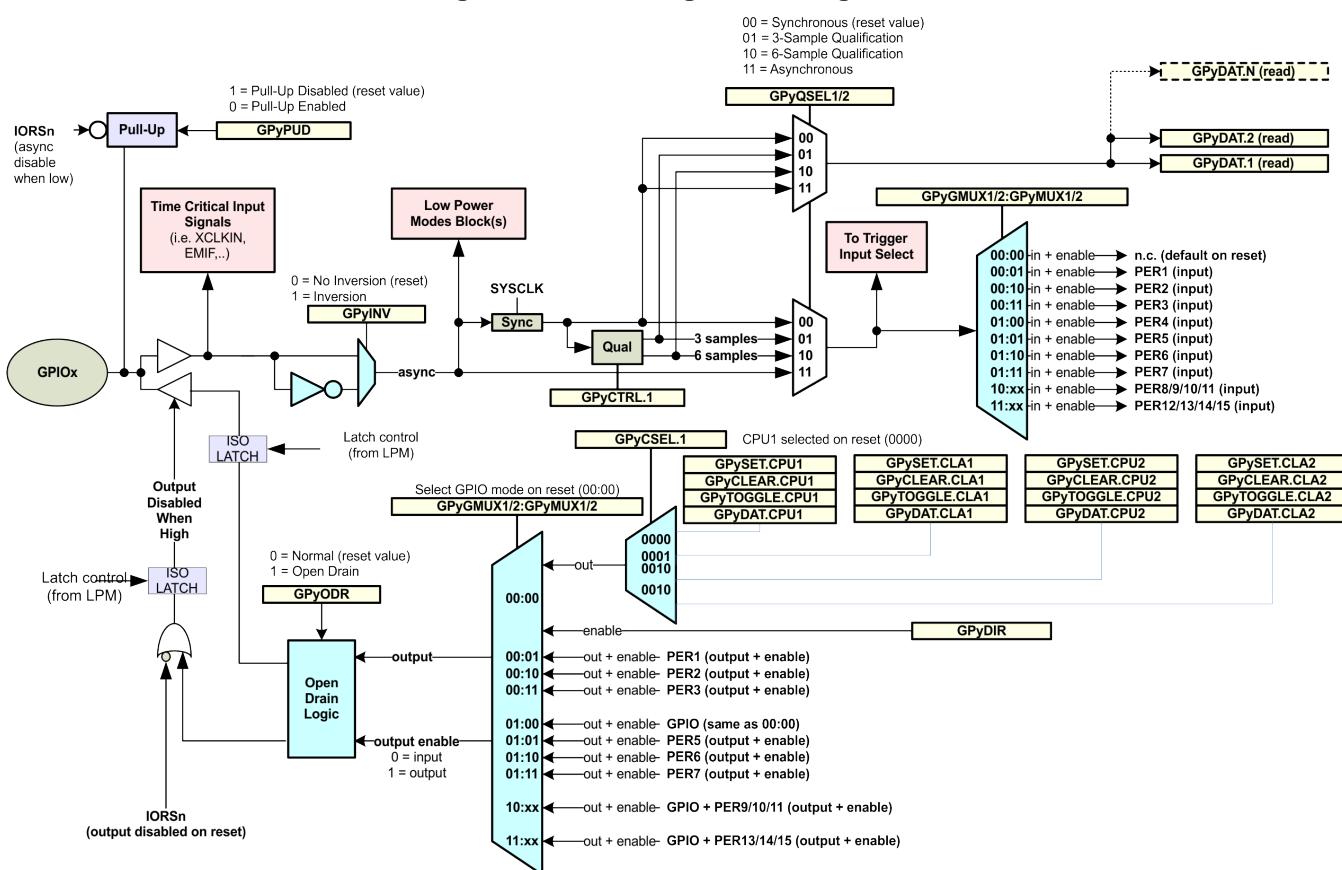
6.1 GPIO Overview

Up to twelve independent peripheral signals are multiplexed on a single GPIO-enabled pin in addition to the CPU-controlled I/O capability. Each pin output can be controlled by either a peripheral or one of the four CPU masters (CPU1, CPU1.CLA, CPU2, or CPU2.CLA). There are six I/O ports:

- Port A consists of GPIO0-GPIO31
- Port B consists of GPIO32-GPIO63
- Port C consists of GPIO64-GPIO95
- Port D consists of GPIO96-GPIO127
- Port E consists of GPIO128-GPIO159
- Port F consists of GPIO160-GPIO168

Figure 6-1 shows the GPIO logic for a single pin.

Figure 6-1. GPIO Logic for a Single Pin



There are two key features to note in this diagram. The first is that the input and output paths are entirely separate, connecting only at the pin. The second is that peripheral muxing takes place far from the pin. As a result, it is always possible for both CPUs and CLAs to read the physical state of the pin independent of CPU mastering and peripheral muxing. Likewise, external interrupts can be generated from peripheral activity. All pin options such as input qualification and open-drain output are valid for all masters and peripherals. However, the peripheral muxing, CPU muxing, and pin options can only be configured by CPU1.

Separate configuration is required for the USB signals. See [Section 6.1.4](#) for details.

6.1.1 Configuration Overview

I/O pin configuration consists of several steps:

1. Plan the device pin-out

Make a list of all required peripherals for the application. Using the peripheral mux information in the device data manual, choose which GPIOs to use for the peripheral signals. Decide which of the remaining GPIOs to use as inputs and outputs for each CPU and CLA. Note that GPIOs 42, 43, 46, and 47 are the only available USB pins. GPIO41 is hard-wired to be the wake-up signal in hibernate mode.

Once the peripheral muxing has been chosen, it should be implemented by writing the appropriate values to the GPyMUX1/2 and GPyGMUX1/2 registers. When changing the GPyGMUX value for a pin, always set the corresponding GPyMUX bits to zero first to avoid glitching in the muxes. By default, all pins are general-purpose I/Os, not peripheral signals.

2. (Optional) Enable internal pullup resistors

To enable or disable the pullup resistors, write to the appropriate bits in the GPIO pullup disable registers (GPyPUD). All pullups are disabled by default. Pullups can be used to keep input pins in a known state when there is no external signal driving them.

3. Select input qualification

If the pin will be used as an input, specify the required input qualification, if any. The input qualification sampling period is selected in the GPyCTRL registers, while the type of qualification is selected in the GPyQSEL1 and GPyQSEL2 registers. By default, all qualification is synchronous with a sampling period equal to PLLSYSCLK. For an explanation of input qualification, see section [Section 6.1.3](#).

4. Select the direction of any general-purpose I/O pins

For each pin configured as a GPIO, specify the direction of the pin as either input or output using the GPyDIR registers. By default, all GPIO pins are inputs. Before changing a pin to an output, load the output latch with the value to be driven by writing that value to the GPySET, GPyCLEAR, or GPyDAT registers. Once the latch is loaded, write to GPyDIR to change the pin direction. By default, all output latches are zero.

5. Select low-power mode wake-up sources

GPIOs 0-63 can be used to wake the system up from Standby or Halt mode. To select one or more GPIOs for wake-up, write to the appropriate bits in the GPIOLOPMSEL0 and GPIOLOPMSEL1 registers. These registers are part of the CPU system register space. In Hibernate mode, GPIO 41 is the only wake-up pin. For more information on low-power modes and GPIO wake-up, see the Low Power Modes section in the *System Control and Interrupts* chapter.

6. Select external interrupt sources

Configuring external interrupts is a two-step process. First, the interrupts themselves must be enabled and their polarity must be configured via the XINTnCR registers. Second, the XINT1-5 GPIO pins must be set by selecting the sources for Input X-BAR signals 4, 5, 6, 13, and 14, respectively. For more information on the Input X-BAR architecture, see the ePWM chapter of this manual.

6.1.2 Digital General-Purpose I/O Control

The values on the pins that are configured as GPIO can be changed by using these registers.

• GPyDAT Registers

Each I/O port has one data register. Each bit in the data register corresponds to one GPIO pin. No matter how the pin is configured (GPIO or peripheral function), the corresponding bit in the data register reflects the current state of the pin after qualification. Writing to the GPyDAT register clears or sets the corresponding output latch and if the pin is enabled as a general purpose output (GPIO output) the pin will also be driven either low or high. If the pin is not configured as a GPIO output then the value will be latched, but the pin will not be driven. Only if the pin is later configured as a GPIO output, will the latched value be driven onto the pin.

When using the GPyDAT register to change the level of an output pin, you should be cautious not to accidentally change the level of another pin. For example, if you mean to change the output latch level of GPIOA1 by writing to the GPADAT register bit 0 using a read-modify-write instruction, a problem can occur if another I/O port A signal changes level between the read and the write stage of the instruction. Following is an analysis of why this happens:

The GPyDAT registers reflect the state of the pin, not the latch. This means the register reflects the

actual pin value. However, there is a lag between when the register is written to when the new pin value is reflected back in the register. This may pose a problem when this register is used in subsequent program statements to alter the state of GPIO pins. An example is shown below where two program statements attempt to drive two different GPIO pins that are currently low to a high state.

If Read-Modify-Write operations are used on the GPyDAT registers, because of the delay between the output and the input of the first instruction (I1), the second instruction (I2) will read the old value and write it back.

```
GpioDataRegs.GPADAT.bit.GPIO1 = 1; //I1 performs read-modify-write of GPADAT
GpioDataRegs.GPADAT.bit.GPIO2 = 1; //I2 also a read-modify-write of GPADAT.
//GPADAT gets the old value of GPIO1 due to the delay
```

The second instruction will wait for the first to finish its write due to the write-followed-by-read protection on this peripheral frame. There will be some lag, however, between the write of (I1) and the GPyDAT bit reflecting the new value (1) on the pin. During this lag, the second instruction will read the old value of GPIO1 (0) and write it back along with the new value of GPIO2 (1). Therefore, GPIO1 pin stays low.

One solution is to put some NOP's between instructions. A better solution is to use the GPySET/GPyCLEAR/GPyTOGGLE registers instead of the GPyDAT registers. These registers always read back a 0 and writes of 0 have no effect. Only bits that need to be changed can be specified without disturbing any other bit(s) that are currently in the process of changing.

- **GPySET Registers**

The set registers are used to drive specified GPIO pins high without disturbing other pins. Each I/O port has one set register and each bit corresponds to one GPIO pin. The set registers always read back 0. If the corresponding pin is configured as an output, then writing a 1 to that bit in the set register will set the output latch high and the corresponding pin will be driven high. If the pin is not configured as a GPIO output, then the value will be latched but the pin will not be driven. Only if the pin is later configured as a GPIO output will the latched value will be driven onto the pin. Writing a 0 to any bit in the set registers has no effect.

- **GPyCLEAR Registers**

The clear registers are used to drive specified GPIO pins low without disturbing other pins. Each I/O port has one clear register. The clear registers always read back 0. If the corresponding pin is configured as a general purpose output, then writing a 1 to the corresponding bit in the clear register will clear the output latch and the pin will be driven low. If the pin is not configured as a GPIO output, then the value will be latched but the pin will not be driven. Only if the pin is later configured as a GPIO output will the latched value will be driven onto the pin. Writing a 0 to any bit in the clear registers has no effect.

- **GPyTOGGLE Registers**

The toggle registers are used to drive specified GPIO pins to the opposite level without disturbing other pins. Each I/O port has one toggle register. The toggle registers always read back 0. If the corresponding pin is configured as an output, then writing a 1 to that bit in the toggle register flips the output latch and pulls the corresponding pin in the opposite direction. That is, if the output pin is driven low, then writing a 1 to the corresponding bit in the toggle register will pull the pin high. Likewise, if the output pin is high, then writing a 1 to the corresponding bit in the toggle register will pull the pin low. If the pin is not configured as a GPIO output, then the value will be latched but the pin will not be driven. Only if the pin is later configured as a GPIO output will the latched value will be driven onto the pin. Writing a 0 to any bit in the toggle registers has no effect.

6.1.3 Input Qualification

The input qualification scheme has been designed to be very flexible. You can select the type of input qualification for each GPIO pin by configuring the GPyQSEL1 and GPyQSEL2 registers. In the case of a GPIO input pin, the qualification can be specified as only synchronize to SYSCLKOUT or qualification by a sampling window. For pins that are configured as peripheral inputs, the input can also be asynchronous in addition to synchronized to SYSCLKOUT or qualified by a sampling window. The remainder of this section describes the options available.

6.1.3.1 No Synchronization (asynchronous input)

This mode is used for peripherals where input synchronization is not required or the peripheral itself performs the synchronization. Examples include communication ports SCI, SPI, and I²C. In addition, it may be desirable to have the ePWM trip zone (TZn) signals function independent of the presence of SYSCLKOUT.

The asynchronous option is not valid if the pin is used as a general purpose digital input pin (GPIO). If the pin is configured as a GPIO input and the asynchronous option is selected then the qualification defaults to synchronization to SYSCLKOUT as described in [Section 6.1.3.2](#).

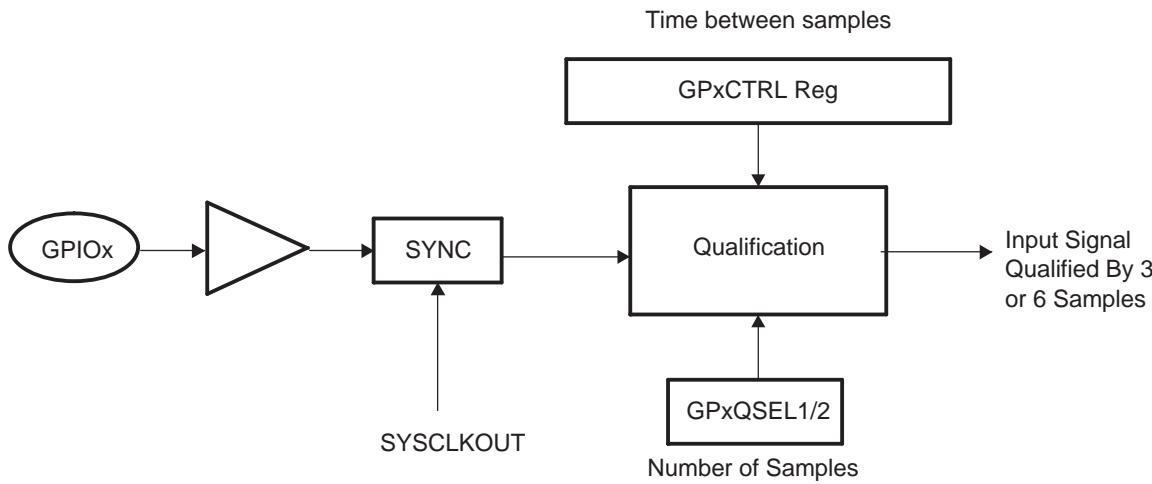
6.1.3.2 Synchronization to SYSCLKOUT Only

This is the default qualification mode of all the pins at reset. In this mode, the input signal is only synchronized to the system clock (SYSCLKOUT). Because the incoming signal is asynchronous, it can take up to a SYSCLKOUT period of delay in order for the input to the MCU to be changed. No further qualification is performed on the signal.

6.1.3.3 Qualification Using a Sampling Window

In this mode, the signal is first synchronized to the system clock (SYSCLKOUT) and then qualified by a specified number of cycles before the input is allowed to change. [Figure 6-2](#) and [Figure 6-3](#) show how the input qualification is performed to eliminate unwanted noise. Two parameters are specified by the user for this type of qualification: 1) the sampling period, or how often the signal is sampled, and 2) the number of samples to be taken.

Figure 6-2. Input Qualification Using a Sampling Window



Time between samples (sampling period):

To qualify the signal, the input signal is sampled at a regular period. The sampling period is specified by the user and determines the time duration between samples, or how often the signal will be sampled, relative to the CPU clock (SYSCLKOUT).

The sampling period is specified by the qualification period (QUALPRDn) bits in the GPxCTRL register. The sampling period is configurable in groups of 8 input signals. For example, GPIO0 to GPIO7 use GPACTRL[QUALPRD0] setting and GPIO8 to GPIO15 use GPACTRL[QUALPRD1]. [Table 6-1](#) and [Table 6-2](#) show the relationship between the sampling period or sampling frequency and the GPxCTRL[QUALPRDn] setting.

Table 6-1. Sampling Period

Sampling Period	
If GPxCTRL[QUALPRDn] = 0	$1 \times T_{SYSCLKOUT}$
If GPxCTRL[QUALPRDn] ≠ 0	$2 \times GPxCTRL[QUALPRDn] \times T_{SYSCLKOUT}$ Where $T_{SYSCLKOUT}$ is the period in time of SYSCLKOUT

Table 6-2. Sampling Frequency

Sampling Frequency	
If GPxCTRL[QUALPRDn] = 0	$f_{SYSCLKOUT}$
If GPxCTRL[QUALPRDn] ≠ 0	$f_{SYSCLKOUT} \times 1 \div (2 \times GPxCTRL[QUALPRDn])$ Where $f_{SYSCLKOUT}$ is the frequency of SYSCLKOUT

From these equations, the minimum and maximum time between samples can be calculated for a given SYSCLKOUT frequency:

Example: Maximum Sampling Frequency:

If $GPxCTRL[QUALPRDn] = 0$

then the sampling frequency is $f_{SYSCLKOUT}$

If, for example, $f_{SYSCLKOUT} = 60$ MHz

then the signal will be sampled at 60 MHz or one sample every 16.67 ns.

Example: Minimum Sampling Frequency:

If $GPxCTRL[QUALPRDn] = 0xFF$ (255)

then the sampling frequency is $f_{SYSCLKOUT} \times 1 \div (2 \times GPxCTRL[QUALPRDn])$

If, for example, $f_{SYSCLKOUT} = 60$ MHz

then the signal will be sampled at 60 MHz $\times 1 \div (2 \times 255)$ or one sample every 8.5 μ s.

Number of samples:

The number of times the signal is sampled is either three samples or six samples as specified in the qualification selection (GPAQSEL1, GPAQSEL2, GPBQSEL1, and GPBQSEL2) registers. When three or six consecutive cycles are the same, then the input change will be passed through to the MCU.

Total Sampling Window Width:

The sampling window is the time during which the input signal will be sampled as shown in [Figure 6-3](#). By using the equation for the sampling period along with the number of samples to be taken, the total width of the window can be determined.

For the input qualifier to detect a change in the input, the level of the signal must be stable for the duration of the sampling window width or longer.

The number of sampling periods within the window is always one less than the number of samples taken. For a three-sample window, the sampling window width is two sampling periods wide where the sampling period is defined in [Table 6-1](#). Likewise, for a six-sample window, the sampling window width is five sampling periods wide. [Table 6-3](#) and [Table 6-4](#) show the calculations that can be used to determine the total sampling window width based on $GPxCTRL[QUALPRDn]$ and the number of samples taken.

Table 6-3. Case 1: Three-Sample Sampling Window Width

Total Sampling Window Width	
If $GPxCTRL[QUALPRDn] = 0$	$2 \times T_{SYSCLKOUT}$
If $GPxCTRL[QUALPRDn] \neq 0$	$2 \times 2 \times GPxCTRL[QUALPRDn] \times T_{SYSCLKOUT}$ Where $T_{SYSCLKOUT}$ is the period in time of SYSCLKOUT

Table 6-4. Case 2: Six-Sample Sampling Window Width

Total Sampling Window Width	
If GPxCTRL[QUALPRDn] = 0	$5 \times T_{SYSCLKOUT}$
If GPxCTRL[QUALPRDn] ≠ 0	$5 \times 2 \times GPxCTRL[QUALPRDn] \times T_{SYSCLKOUT}$
	Where $T_{SYSCLKOUT}$ is the period in time of SYSCLKOUT

NOTE: The external signal change is asynchronous with respect to both the sampling period and SYSCLKOUT. Due to the asynchronous nature of the external signal, the input should be held stable for a time greater than the sampling window width to make sure the logic detects a change in the signal. The extra time required can be up to an additional sampling period + $T_{SYSCLKOUT}$.

The required duration for an input signal to be stable for the qualification logic to detect a change is described in the device-specific data manual.

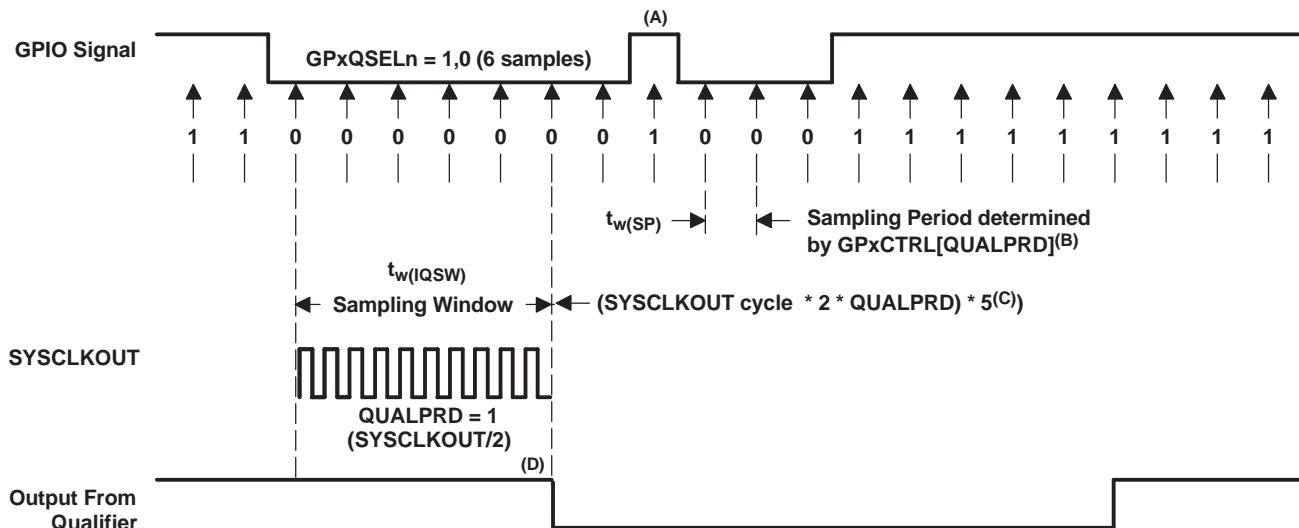
Example Qualification Window:

For the example shown in [Figure 6-3](#), the input qualification has been configured as follows:

- GPxQSEL1/2 = 1,0. This indicates a six-sample qualification.
- GPxCTRL[QUALPRDn] = 1. The sampling period is $t_w(SP) = 2 \times GPxCTRL[QUALPRDn] \times T_{SYSCLKOUT}$.

This configuration results in the following:

- The width of the sampling window is: .
 $t_w(IQSW) = 5 \times t_w(SP) = 5 \times 2 \times GPxCTRL[QUALPRDn] \times T_{SYSCLKOUT}$ or $5 \times 2 \times T_{SYSCLKOUT}$
- If, for example, $T_{SYSCLKOUT} = 16.67$ ns, then the duration of the sampling window is:
 $t_w(IQSW) = 5 \times 2 \times 16.67$ ns = 166.7 ns.
- To account for the asynchronous nature of the input relative to the sampling period and SYSCLKOUT, up to an additional sampling period, $t_w(SP)$, + $T_{SYSCLKOUT}$ may be required to detect a change in the input signal. For this example:
 $t_w(SP) + T_{SYSCLKOUT} = 333.4$ ns + 166.67 ns = 500.1 ns
- In [Figure 6-3](#), the glitch (A) is shorter than the qualification window and will be ignored by the input qualifier.

Figure 6-3. Input Qualifier Clock Cycles

- A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value "n", the qualification sampling period in 2n SYSCLKOUT cycles (i.e., at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled).
- B. The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.
- C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
- D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for $(5 \times \text{QUALPRD} \times 2)$ SYSCLKOUT cycles. That would ensure 5 sampling periods for detection to occur. Since external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

6.1.4 USB Signals

The USB module on this device has an internal physical layer transceiver (PHY). Its I/O signals are not normal digital signals, and as a result, they do not connect to the pins through the normal GPIO mux path. Instead, a special analog mux is used. To connect the USB signals to the device pins, set the GPyAMSEL bits appropriately as shown in [Table 6-5](#). Do not enable pullups or any other special pin option when using the USB signals.

Table 6-5. USB I/O Signal Muxing

Signal	GPIO	AMSEL
USBDM	42	GPBAMSEL[10]
USBDP	43	GPBAMSEL[11]

6.1.5 GPIO and Peripheral Muxing

Up to twelve different peripheral functions are multiplexed to each pin along with a general-purpose input/output (GPIO) function. This allows you to choose the peripheral mix and pinout that will work best for your particular application. Refer to the device datasheet for muxing combinations and definitions.

For example, the multiplexing for the GPIO 6 pin is controlled by writing to GPAGMUX[13:12] and GPAMUX[13:12]. By writing to these bits, GPIO 6 can be configured as either a general-purpose digital I/O or one of four different peripheral functions. Here are the options:

GPAGMUX1[13:12]	GPAMUX1[13:12]	Pin functionality
00	00	GPIO
00	01	EPWM4A
00	10	XTRIPOUT4
00	11	EPWMSYNCO
01	00	GPIO
01	01	EQEP3A
01	10	CANTXB
10	00	GPIO
11	00	GPIO
All others		Reserved

The devices have different multiplexing schemes. If a peripheral is not available on a particular device, that mux selection is reserved on that device and should not be used.

Note: If you select a reserved GPIO mux configuration that is not mapped to either a peripheral or GPIO mode, the state of the pin will be undefined and the pin may be driven. Unimplemented configurations are for future expansion and must not be selected. In the device mux table (see datasheet), these options are indicated as Reserved or left blank.

Some peripherals can be assigned to more than one pin via the mux registers. For example, XTRIPOUT1 can be assigned to GPIOs 2, 24, 34, or 58, depending on individual system requirements:

GMUX Configuration	MUX Configuration	
Choice 1 GPIO2	GPAGMUX1[5:4]=01	GPAMUX1[5:4]=01
or Choice 2 GPIO24	GPAGMUX2[17:16]=00	GPAMUX2[17:16]=01
or Choice 3 GPIO34	GPBGMUX1[5:4]=00	GPBMUX1[5:4]=01
or Choice 4 GPIO58	GPBGMUX2[21:20]=01	GPBMUX2[21:20]=01

If no pin is configured as an input to a peripheral, or if more than one pin is configured to an input for the same peripheral, then that input will be set to a hard-wired default value.

6.1.6 Internal Pullup Configuration Requirements

On reset, GPIOs are in input mode and have the internal pullups disabled. An un-driven input can float to a mid-rail voltage and cause wasted shoot-through current on the input buffer. The user should always put each GPIO in one of these configurations:

- Input mode and driven on the board by another component to a level above V_{ih} or below V_{il}
- Input mode with GPIO internal pullup enabled
- Output mode

On devices in the 176PTP or 100PZP packages, the pullups for any internally unbonded GPIO must be enabled to prevent floating inputs. TI has provided functions in controlSUITE which users can call to enable the pullup on any unbonded GPIO for the package they are using. This function, `GPIO_EnabledUnbondedIOPullups()`, resides in the `(Device)_Sysctrl.c` file and is called by default from `InitSysCtrl()`. The user should take care to avoid disabling these pullups in their application code.

For 176-pin packages, pullup resistors should be enabled on the following GPIOs:

Table 6-6. Pullup Resistors for 175-pin Packages

Unbonded GPIOs on the 176-pin package							
95	106	116	126	137	147	157	167
96	107	117	127	138	148	158	168
97	108	118	128	139	149	159	
98	109	119	129	140	150	160	
100	110	120	130	141	151	161	
101	111	121	131	142	152	162	
102	112	122	132	143	153	163	
103	113	123	134	144	154	164	
104	114	124	135	145	155	165	
105	115	125	136	146	156	166	

For 100-pin packages, pullup resistors should be enabled on the following GPIOs:

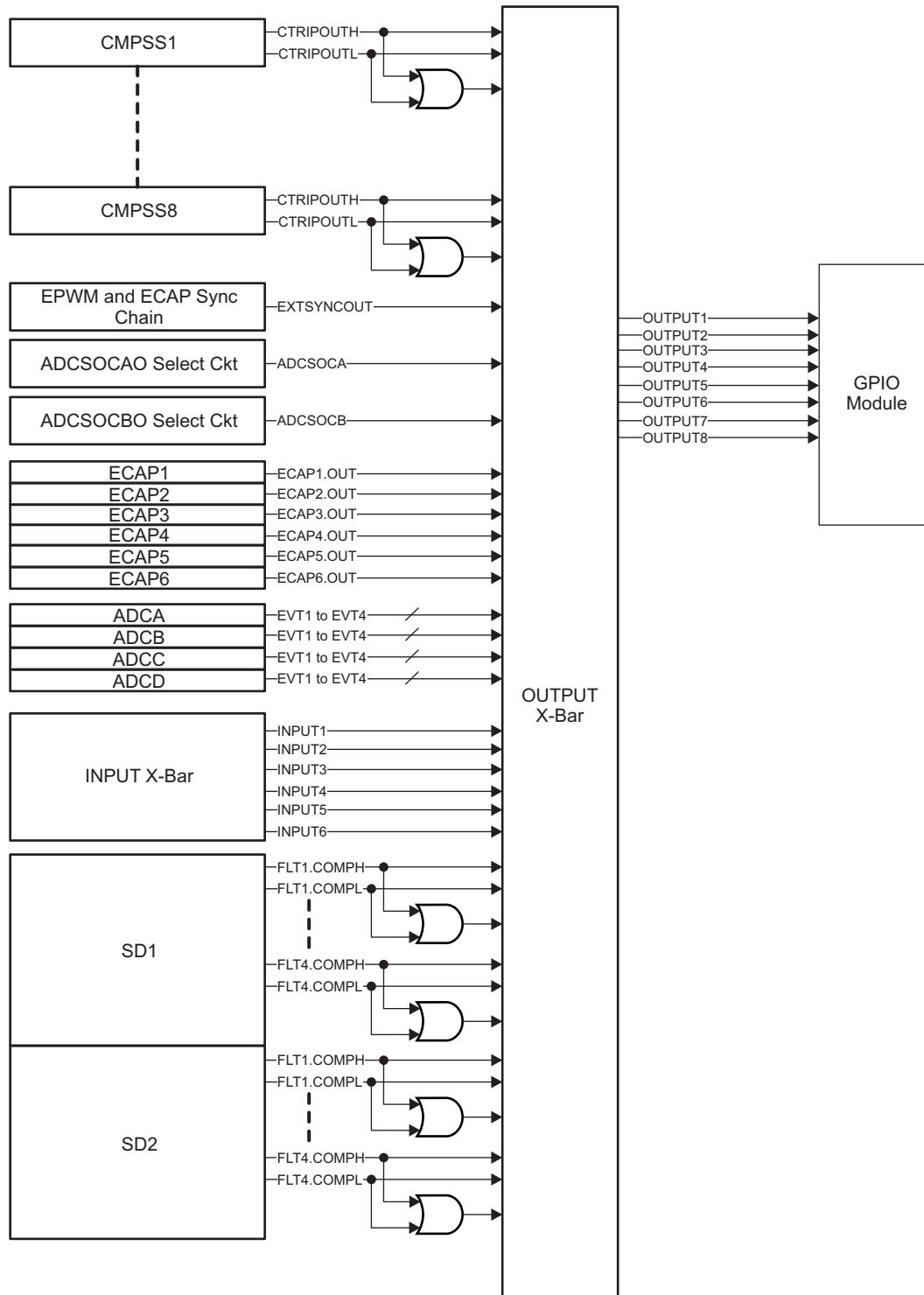
Table 6-7. Pullup Resistors for 100-pin Packages

Unbonded GPIOs on the 100-pin package								
0	30	48	77	101	116	131	146	161
1	31	49	79	102	117	132	147	162
5	32	50	80	103	118	133	148	163
6	33	51	81	104	119	134	149	164
7	34	52	82	105	120	135	150	165
8	35	53	83	106	121	136	151	166
9	36	54	88	107	122	137	152	167
22	37	55	93	108	123	138	153	168
23	38	56	94	109	124	139	154	
24	39	57	95	110	125	140	155	
25	40	67	96	111	126	141	156	
26	44	68	97	112	127	142	157	
27	45	74	98	113	128	143	158	
28	46	75	100	114	129	144	159	
29	47	76	101	115	130	145	160	

6.2 Output X-BAR

The GPIO module contains a X-BAR which allows an assortment of signals to be routed to a GPIO. The signals which are available to bring to the GPIO are listed in [Table 6-8](#). The X-BAR contains eight outputs and each will contain at least one position on the GPIO mux, denoted as OUTPUTXBARx. The X-BAR allows the selection of a single signal or a logical OR of up to 32 signals.

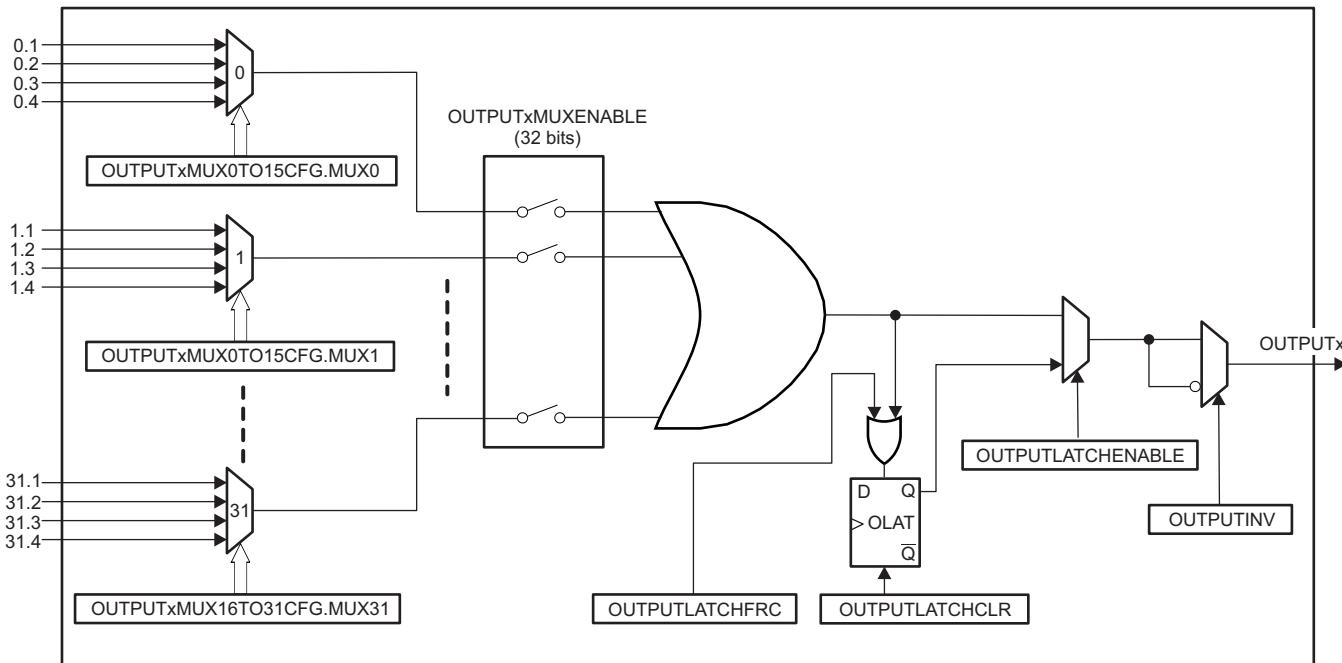
Figure 6-4. OUTPUT X- Bar



6.2.1 Output X-BAR Architecture

The Output X-BAR has eight outputs which are routed to the GPIO module. Figure 6-5 represents the architecture of a single output but it is identical to the architecture of all of the other outputs:

Figure 6-5. Output X-Bar Architecture



First, determine the signal(s) which should be passed to the GPIO by referencing Table 6-8. You may select up to one signal per mux (32 total muxes) for each OUTPUTXBARx output. Select the inputs to each mux via the OUTPUTxMUX0TO15CFG and OUTPUTxMUX16TO31CFG registers.

In order to pass any signal through to the GPIO, you must also enable the mux in the OUTPUTxMUXENABLE register. All muxes which are enabled will be logically OR'd before being passed on to the respective OUTPUTx signal on the GPIO module. You may also optionally invert the signal via the OUTPUTINV register. The signal will only be seen on the GPIO if the proper OUTPUTx muxing options are selected via the GpioCtrlRegs.GPxMUX and GpioCtrlRegs.GPxGMUX registers.

Table 6-8. Output X-BAR Mux Configuration Table

Mux	1	2	3	4
0	CMPSS1.CTRIPOUTH	CMPSS0.CTRIPOUTH_OR_CTRIPOUTL	ADCAEVT1	ECAP1.OUT
1	CMPSS1.CTRIPOUTL	INPUTXBAR1		ADCCEVT1
2	CMPSS2.CTRIPOUTH	CMPSS1.CTRIPOUTH_OR_CTRIPOUTL	ADCAEVT2	ECAP2.OUT
3	CMPSS2.CTRIPOUTL	INPUTXBAR2		ADCCEVT2
4	CMPSS3.CTRIPOUTH	CMPSS2.CTRIPOUTH_OR_CTRIPOUTL	ADCAEVT3	ECAP3.OUT
5	CMPSS3.CTRIPOUTL	INPUTXBAR3		ADCCEVT3
6	CMPSS4.CTRIPOUTH	CMPSS3.CTRIPOUTH_OR_CTRIPOUTL	ADCAEVT4	ECAP4.OUT
7	CMPSS4.CTRIPOUTL	INPUTXBAR4		ADCCEVT4
8	CMPSS5.CTRIPOUTH	CMPSS4.CTRIPOUTH_OR_CTRIPOUTL	ADCBEVT1	ECAP5.OUT
9	CMPSS5.CTRIPOUTL	INPUTXBAR5		ADCDEVT1
10	CMPSS6.CTRIPOUTH	CMPSS5.CTRIPOUTH_OR_CTRIPOUTL	ADCBEVT2	ECAP6.OUT
11	CMPSS6.CTRIPOUTL	INPUTXBAR6		ADCDEVT2
12	CMPSS7.CTRIPOUTH	CMPSS6.CTRIPOUTH_OR_CTRIPOUTL	ADCBEVT3	
13	CMPSS7.CTRIPOUTL	ADCSOCA		ADCDEVT3
14	CMPSS8.CTRIPOUTH	CMPSS7.CTRIPOUTH_OR_CTRIPOUTL	ADCBEVT4	EXTSYNCOUT
15	CMPSS8.CTRIPOUTL	ADCSOCB		ADCDEVT4
16	SD1FLT1.COMPH	SD1FLT1.COMPH_OR_COMPL		
17	SD1FLT1.COMPL			
18	SD1FLT2.COMPH	SD1FLT2.COMPH_OR_COMPL		
19	SD1FLT2.COMPL			
20	SD1FLT3.COMPH	SD1FLT3.COMPH_OR_COMPL		
21	SD1FLT3.COMPL			
22	SD1FLT4.COMPH	SD1FLT4.COMPH_OR_COMPL		
23	SD1FLT4.COMPL			
24	SD2FLT1.COMPH	SD2FLT1.COMPH_OR_COMPL		
25	SD2FLT1.COMPL			
26	SD2FLT2.COMPH	SD2FLT2.COMPH_OR_COMPL		
27	SD2FLT2.COMPL			
28	SD2FLT3.COMPH	SD2FLT3.COMPH_OR_COMPL		
29	SD2FLT3.COMPL			
30	SD2FLT4.COMPH	SD2FLT4.COMPH_OR_COMPL		
31	SD2FLT4.COMPL			

6.3 Input X-BAR

On this device, the Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADC(s), eCAP(s), ePWM(s), and external interrupts. The Input X-BAR has access to every GPIO and can route each signal to any (or multiple) of the IP blocks previously mentioned. This flexibility relieves some of the constraints on peripheral muxing by just requiring any GPIO pin to be available. It is important to note that the function selected on the GPIO mux does not affect the Input-XBAR. The Input X-BAR simply connects the signal on the input buffer to the selected destination. Therefore, you can do things such as route the output of one peripheral to another (that is, measure the output of an ePWM with an eCAP for a frequency test).

The Input X-BAR is configured via the INPUTxSELECT registers. The available IP destination(s) for each INPUTx is shown in [Figure 6-6](#). For more information on configuration, see the TRIG_REGS register definitions at the end of this chapter.

Figure 6-6. GPIO MUX-to-Trip Input Connectivity

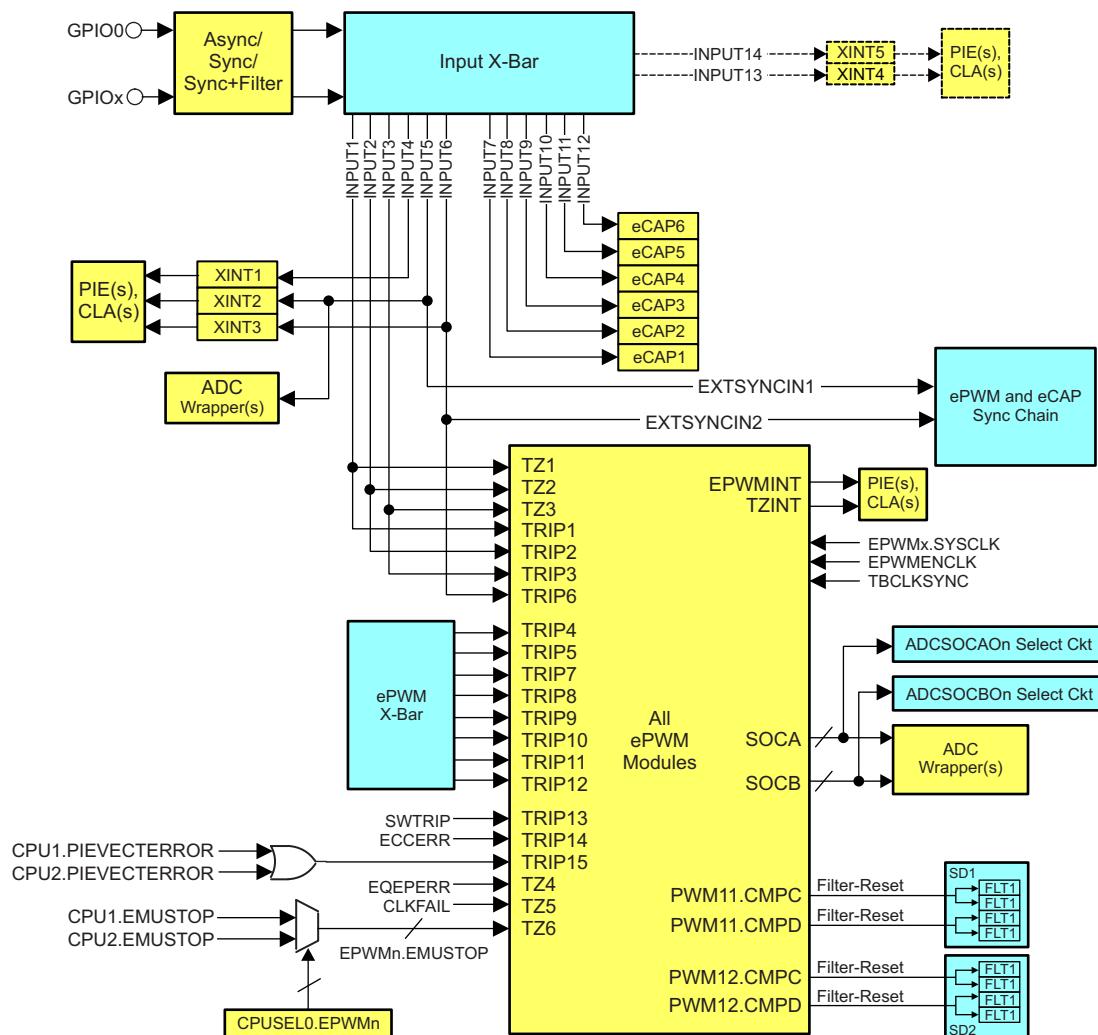


Table 6-9. Input X_BAR Destinations

Input	Destinations
INPUT1	EPWM[TZ1], EPWM[TRIP1], EPWM X-BAR, Output X-BAR
INPUT2	EPWM[TZ2], EPWM[TRIP2], EPWM X-BAR, Output X-BAR
INPUT3	EPWM[TZ3], EPWM[TRIP3], EPWM X-BAR, Output X-BAR
INPUT4	ADC Wrapper(s), EPWM X-BAR, Output X-BAR, XINT1
INPUT5	EXTSYNCIN1, EPWM X-BAR, Output X-BAR, XINT2
INPUT6	EXTSYNCIN2, EPWM[TRIP6], EPWM X-BAR, Output X-BAR, XINT3
INPUT7	ECAP1
INPUT8	ECAP2
INPUT9	ECAP3
INPUT10	ECAP4
INPUT11	ECAP5
INPUT12	ECAP6
INPUT13	XINT4
INPUT14	XINT5

6.4 Registers

6.4.1 GPIO Base Addresses

Table 6-10. GPIO Base Address Table

Device Registers	Register Name	Start Address	End Address
InputXbarRegs ⁽¹⁾	INPUT_XBAR_REGS	0x0000_7900	0x0000_793F
OutputXbarRegs ⁽¹⁾	OUTPUT_XBAR_REGS	0x0000_7A80	0x0000_7ABF
GpioCtrlRegs ⁽¹⁾	GPIO_CTRL_REGS	0x0000_7C00	0x0000_7D7F
GpioDataRegs	GPIO_DATA_REGS	0x0000_7F00	0x0000_7F2F

⁽¹⁾ Only available on CPU1.

6.4.2 INPUT_XBAR_REGS Registers

Table 6-11 lists the memory-mapped registers for the INPUT_XBAR_REGS. All register offset addresses not listed in Table 6-11 should be considered as reserved locations and the register contents should not be modified.

Table 6-11. INPUT_XBAR_REGS REGISTERS

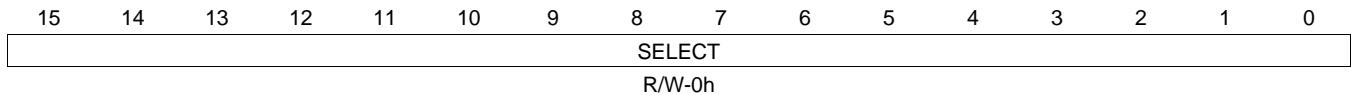
Offset	Acronym	Register Name	Section	Write Protection
0h	INPUT1SELECT	INPUT1 Input Select Register (GPIO0 to x)	Section 6.4.2.1	EALLOW
1h	INPUT2SELECT	INPUT2 Input Select Register (GPIO0 to x)	Section 6.4.2.2	EALLOW
2h	INPUT3SELECT	INPUT3 Input Select Register (GPIO0 to x)	Section 6.4.2.3	EALLOW
3h	INPUT4SELECT	INPUT4 Input Select Register (GPIO0 to x)	Section 6.4.2.4	EALLOW
4h	INPUT5SELECT	INPUT5 Input Select Register (GPIO0 to x)	Section 6.4.2.5	EALLOW
5h	INPUT6SELECT	INPUT6 Input Select Register (GPIO0 to x)	Section 6.4.2.6	EALLOW
6h	INPUT7SELECT	INPUT7 Input Select Register (GPIO0 to x)	Section 6.4.2.7	EALLOW
7h	INPUT8SELECT	INPUT8 Input Select Register (GPIO0 to x)	Section 6.4.2.8	EALLOW
8h	INPUT9SELECT	INPUT9 Input Select Register (GPIO0 to x)	Section 6.4.2.9	EALLOW
9h	INPUT10SELECT	INPUT10 Input Select Register (GPIO0 to x)	Section 6.4.2.10	EALLOW
Ah	INPUT11SELECT	INPUT11 Input Select Register (GPIO0 to x)	Section 6.4.2.11	EALLOW
Bh	INPUT12SELECT	INPUT12 Input Select Register (GPIO0 to x)	Section 6.4.2.12	EALLOW
Ch	INPUT13SELECT	INPUT13 Input Select Register (GPIO0 to x)	Section 6.4.2.13	EALLOW
Dh	INPUT14SELECT	INPUT14 Input Select Register (GPIO0 to x)	Section 6.4.2.14	EALLOW
1Eh	INPUTSELECTLOCK	Input Select Lock Register	Section 6.4.2.15	EALLOW
20h	TRIGLATCH1	X-Bar Input Latch Register 1	Section 6.4.2.16	
22h	TRIGLATCH2	X-Bar Input Latch Register 2	Section 6.4.2.17	
24h	TRIGLATCH3	X-Bar Input Latch Register 3	Section 6.4.2.18	
28h	TRIGLATCHCLR1	X-Bar Input Latch Clear Register 1	Section 6.4.2.19	
2Ah	TRIGLATCHCLR2	X-Bar Input Latch Clear Register 2	Section 6.4.2.20	
2Ch	TRIGLATCHCLR3	X-Bar Input Latch Clear Register 3	Section 6.4.2.21	

6.4.2.1 INPUT1SELECT Register (offset = 0h) [reset = 0h]

INPUT1SELECT is shown in [Figure 6-7](#) and described in [Table 6-12](#).

INPUT1 Input Select Register (GPIO0 to x)

Figure 6-7. INPUT1SELECT Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-12. INPUT1SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT1 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.2 INPUT2SELECT Register (offset = 1h) [reset = 0h]

INPUT2SELECT is shown in [Figure 6-8](#) and described in [Table 6-13](#).

INPUT2 Input Select Register (GPIO0 to x)

Figure 6-8. INPUT2SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-13. INPUT2SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT2 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.3 INPUT3SELECT Register (offset = 2h) [reset = 0h]

INPUT3SELECT is shown in [Figure 6-9](#) and described in [Table 6-14](#).

INPUT3 Input Select Register (GPIO0 to x)

Figure 6-9. INPUT3SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-14. INPUT3SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT3 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.4 INPUT4SELECT Register (offset = 3h) [reset = 0h]

INPUT4SELECT is shown in [Figure 6-10](#) and described in [Table 6-15](#).

INPUT4 Input Select Register (GPIO0 to x)

Figure 6-10. INPUT4SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-15. INPUT4SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT4 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.5 INPUT5SELECT Register (offset = 4h) [reset = 0h]

INPUT5SELECT is shown in [Figure 6-11](#) and described in [Table 6-16](#).

INPUT5 Input Select Register (GPIO0 to x)

Figure 6-11. INPUT5SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-16. INPUT5SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT5 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.6 INPUT6SELECT Register (offset = 5h) [reset = 0h]

INPUT6SELECT is shown in [Figure 6-12](#) and described in [Table 6-17](#).

INPUT6 Input Select Register (GPIO0 to x)

Figure 6-12. INPUT6SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-17. INPUT6SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT6 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.7 INPUT7SELECT Register (offset = 6h) [reset = 0h]

INPUT7SELECT is shown in [Figure 6-13](#) and described in [Table 6-18](#).

INPUT7 Input Select Register (GPIO0 to x)

Figure 6-13. INPUT7SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-18. INPUT7SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT7 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.8 INPUT8SELECT Register (offset = 7h) [reset = 0h]

INPUT8SELECT is shown in [Figure 6-14](#) and described in [Table 6-19](#).

INPUT8 Input Select Register (GPIO0 to x)

Figure 6-14. INPUT8SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-19. INPUT8SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT8 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.9 INPUT9SELECT Register (offset = 8h) [reset = 0h]

INPUT9SELECT is shown in [Figure 6-15](#) and described in [Table 6-20](#).

INPUT9 Input Select Register (GPIO0 to x)

Figure 6-15. INPUT9SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-20. INPUT9SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT9 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.10 INPUT10SELECT Register (offset = 9h) [reset = 0h]INPUT10SELECT is shown in [Figure 6-16](#) and described in [Table 6-21](#).

INPUT10 Input Select Register (GPIO0 to x)

Figure 6-16. INPUT10SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-21. INPUT10SELECT Register Field Descriptions

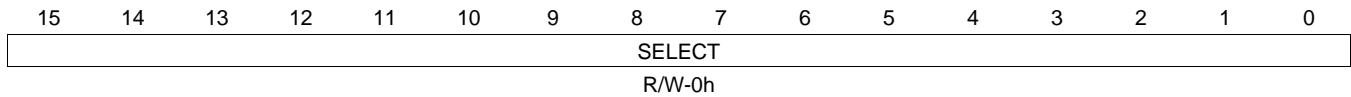
Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT10 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.11 INPUT11SELECT Register (offset = Ah) [reset = 0h]

INPUT11SELECT is shown in [Figure 6-17](#) and described in [Table 6-22](#).

INPUT11 Input Select Register (GPIO0 to x)

Figure 6-17. INPUT11SELECT Register



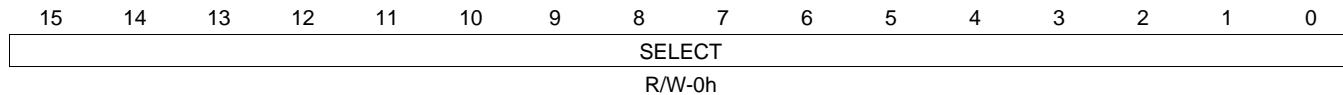
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-22. INPUT11SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT11 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.12 INPUT12SELECT Register (offset = Bh) [reset = 0h]INPUT12SELECT is shown in [Figure 6-18](#) and described in [Table 6-23](#).

INPUT12 Input Select Register (GPIO0 to x)

Figure 6-18. INPUT12SELECT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-23. INPUT12SELECT Register Field Descriptions

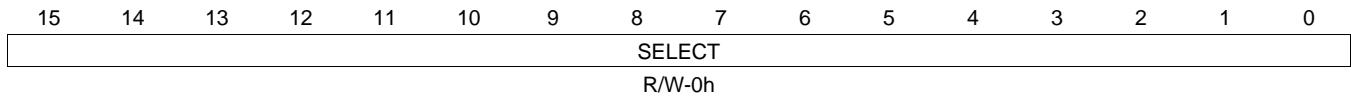
Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT12 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.13 INPUT13SELECT Register (offset = Ch) [reset = 0h]

INPUT13SELECT is shown in [Figure 6-19](#) and described in [Table 6-24](#).

INPUT13 Input Select Register (GPIO0 to x)

Figure 6-19. INPUT13SELECT Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-24. INPUT13SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT13 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.14 INPUT14SELECT Register (offset = Dh) [reset = 0h]INPUT14SELECT is shown in [Figure 6-20](#) and described in [Table 6-25](#).

INPUT14 Input Select Register (GPIO0 to x)

Figure 6-20. INPUT14SELECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-25. INPUT14SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SELECT	R/W	0h	Select GPIO for INPUT14 signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ...

6.4.2.15 INPUTSELECTLOCK Register (offset = 1Eh) [reset = 0h]

INPUTSELECTLOCK is shown in [Figure 6-21](#) and described in [Table 6-26](#).

Input Select Lock Register

Figure 6-21. INPUTSELECTLOCK Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
INPUT16SELE CT	INPUT15SELE CT	INPUT14SELE CT	INPUT13SELE CT	INPUT12SELE CT	INPUT11SELE CT	INPUT10SELE CT	INPUT9SELEC T
R/SOnce-0h	R/SOnce-0h						
7	6	5	4	3	2	1	0
INPUT8SELEC T	INPUT7SELEC T	INPUT6SELEC T	INPUT5SELEC T	INPUT4SELEC T	INPUT3SELEC T	INPUT2SELEC T	INPUT1SELEC T
R/SOnce-0h	R/SOnce-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-26. INPUTSELECTLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15	INPUT16SELECT	R/SOnce	0h	<p>Lock bit for INPUT16SELECT Register: 0: Respective register is not locked 1: Respective register is locked. Any bit in this register, once set can only be cleared through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect Notes: [1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
14	INPUT15SELECT	R/SOnce	0h	<p>Lock bit for INPUT15SELECT Register: 0: Respective register is not locked 1: Respective register is locked. Any bit in this register, once set can only be cleared through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect Notes: [1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
13	INPUT14SELECT	R/SOnce	0h	<p>Lock bit for INPUT14SELECT Register: 0: Respective register is not locked 1: Respective register is locked. Any bit in this register, once set can only be cleared through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect Notes: [1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>

Table 6-26. INPUTSELECTLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	INPUT13SELECT	R/SOnce	0h	<p>Lock bit for INPUT13SELECT Register: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
11	INPUT12SELECT	R/SOnce	0h	<p>Lock bit for INPUT12SELECT Register: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
10	INPUT11SELECT	R/SOnce	0h	<p>Lock bit for INPUT11SELECT Register: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
9	INPUT10SELECT	R/SOnce	0h	<p>Lock bit for INPUT11SELECT Register: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
8	INPUT9SELECT	R/SOnce	0h	<p>Lock bit for INPUT10SELECT Register: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
7	INPUT8SELECT	R/SOnce	0h	<p>Lock bit for INPUT9SELECT Register: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>

Table 6-26. INPUTSELECTLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INPUT7SELECT	R/SOnce	0h	<p>Lock bit for INPUT8SELECT Register:</p> <p>0: Respective register is not locked</p> <p>1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
5	INPUT6SELECT	R/SOnce	0h	<p>Lock bit for INPUT7SELECT Register:</p> <p>0: Respective register is not locked</p> <p>1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
4	INPUT5SELECT	R/SOnce	0h	<p>Lock bit for INPUT5SELECT Register:</p> <p>0: Respective register is not locked</p> <p>1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
3	INPUT4SELECT	R/SOnce	0h	<p>Lock bit for INPUT4SELECT Register:</p> <p>0: Respective register is not locked</p> <p>1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
2	INPUT3SELECT	R/SOnce	0h	<p>Lock bit for INPUT3SELECT Register:</p> <p>0: Respective register is not locked</p> <p>1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>
1	INPUT2SELECT	R/SOnce	0h	<p>Lock bit for INPUT2SELECT Register:</p> <p>0: Respective register is not locked</p> <p>1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>

Table 6-26. INPUTSELECTLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INPUT1SELECT	R/SOnce	0h	<p>Lock bit for INPUT1SELECT Register:</p> <p>0: Respective register is not locked</p> <p>1: Respective register is locked.</p> <p>Any bit in this register, once set can only be created through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect</p> <p>Notes:</p> <p>[1] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed.</p>

6.4.2.16 TRIGLATCH1 Register (offset = 20h) [reset = 0h]

TRIGLATCH1 is shown in [Figure 6-22](#) and described in [Table 6-27](#).

X-Bar Input Latch Register 1

Figure 6-22. TRIGLATCH1 Register

31	30	29	28	27	26	25	24
CMPSS8_CTRI POUTH	CMPSS8_CTRI POUTL	CMPSS7_CTRI POUTH	CMPSS7_CTRI POUTL	CMPSS6_CTRI POUTH	CMPSS6_CTRI POUTL	CMPSS5_CTRI POUTH	CMPSS5_CTRI POUTL
R-0h							
23	22	21	20	19	18	17	16
CMPSS4_CTRI POUTH	CMPSS4_CTRI POUTL	CMPSS3_CTRI POUTH	CMPSS3_CTRI POUTL	CMPSS2_CTRI POUTH	CMPSS2_CTRI POUTL	CMPSS1_CTRI POUTH	CMPSS1_CTRI POUTL
R-0h							
15	14	13	12	11	10	9	8
CMPSS8_CTRI PH	CMPSS8_CTRI PL	CMPSS7_CTRI PH	CMPSS7_CTRI PL	CMPSS6_CTRI PH	CMPSS6_CTRI PL	CMPSS5_CTRI PH	CMPSS5_CTRI PL
R-0h							
7	6	5	4	3	2	1	0
CMPSS4_CTRI PH	CMPSS4_CTRI PL	CMPSS3_CTRI PH	CMPSS3_CTRI PL	CMPSS2_CTRI PH	CMPSS2_CTRI PL	CMPSS1_CTRI PH	CMPSS1_CTRI PL
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-27. TRIGLATCH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMPSS8_CTRIPOUTH	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
30	CMPSS8_CTRIPOUTL	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
29	CMPSS7_CTRIPOUTH	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
28	CMPSS7_CTRIPOUTL	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software

Table 6-27. TRIGLATCH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMPSS6_CTRIPOUTH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
26	CMPSS6_CTRIPOUTL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
25	CMPSS5_CTRIPOUTH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
24	CMPSS5_CTRIPOUTL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
23	CMPSS4_CTRIPOUTH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
22	CMPSS4_CTRIPOUTL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
21	CMPSS3_CTRIPOUTH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
20	CMPSS3_CTRIPOUTL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>

Table 6-27. TRIGLATCH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CMPSS2_CTRIPOUTH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
18	CMPSS2_CTRIPOUTL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
17	CMPSS1_CTRIPOUTH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
16	CMPSS1_CTRIPOUTL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
15	CMPSS8_CTRIPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
14	CMPSS8_CTRIPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
13	CMPSS7_CTRIPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
12	CMPSS7_CTRIPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>

Table 6-27. TRIGLATCH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CMPSS6_CTRIPH	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
10	CMPSS6_CTRIPL	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
9	CMPSS5_CTRIPH	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
8	CMPSS5_CTRIPL	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
7	CMPSS4_CTRIPH	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
6	CMPSS4_CTRIPL	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
5	CMPSS3_CTRIPH	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
4	CMPSS3_CTRIPL	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software

Table 6-27. TRIGLATCH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMPSS2_CTRIPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
2	CMPSS2_CTRIPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
1	CMPSS1_CTRIPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
0	CMPSS1_CTRIPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>

6.4.2.17 TRIGLATCH2 Register (offset = 22h) [reset = 0h]

TRIGLATCH2 is shown in [Figure 6-23](#) and described in [Table 6-28](#).

X-Bar Input Latch Register 2

Figure 6-23. TRIGLATCH2 Register

31	30	29	28	27	26	25	24
ADCCEVT1	ADCBEvt4	ADCBEvt3	ADCBEvt2	ADCBEvt1	ADCAEvt4	ADCAEvt3	ADCAEvt2
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
ADCAEvt1	EXTSYNCOUT	ECAP6_OUT	ECAP5_OUT	ECAP4_OUT	ECAP3_OUT	ECAP2_OUT	ECAP1_OUT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
ADCSOCB	ADCSOCA	INPUT7	INPUT5	INPUT4	INPUT3	INPUT2	INPUT1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-28. TRIGLATCH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ADCCEVT1	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
30	ADCBEvt4	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
29	ADCBEvt3	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
28	ADCBEvt2	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
27	ADCBEvt1	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software

Table 6-28. TRIGLATCH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	ADCAEVT4	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
25	ADCAEVT3	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
24	ADCAEVT2	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
23	ADCAEVT1	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
22	EXTSYNCOUT	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
21	ECAP6_OUT	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
20	ECAP5_OUT	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
19	ECAP4_OUT	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>

Table 6-28. TRIGLATCH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	ECAP3_OUT	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
17	ECAP2_OUT	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
16	ECAP1_OUT	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	ADCSOCB	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
6	ADCSOCA	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
5	INPUT7	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
4	INPUT5	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software

Table 6-28. TRIGLATCH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INPUT4	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
2	INPUT3	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
1	INPUT2	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
0	INPUT1	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>

6.4.2.18 TRIGLATCH3 Register (offset = 24h) [reset = 0h]

TRIGLATCH3 is shown in [Figure 6-24](#) and described in [Table 6-29](#).

X-Bar Input Latch Register 3

Figure 6-24. TRIGLATCH3 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED	SD2FLT4_CO MPH	SD2FLT4_CO MPL	SD2FLT3_CO MPH	SD2FLT3_CO MPL	SD2FLT2_CO MPH	SD2FLT2_CO MPL	SD2FLT1_CO MPH
R=0-0h	R-0h						
15	14	13	12	11	10	9	8
SD2FLT1_CO MPL	SD1FLT4_CO MPH	SD1FLT4_CO MPL	SD1FLT3_CO MPH	SD1FLT3_CO MPL	SD1FLT2_CO MPH	SD1FLT2_CO MPL	SD1FLT1_CO MPH
R-0h							
7	6	5	4	3	2	1	0
SD1FLT1_CO MPL	ADCDEVT4	ADCDEVT3	ADCDEVT2	ADCDEVT1	ADCCEVT4	ADCCEVT3	ADCCEVT2
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-29. TRIGLATCH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R=0	0h	Reserved
22	SD2FLT4_COMPH	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
21	SD2FLT4_COMPL	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
20	SD2FLT3_COMPH	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software
19	SD2FLT3_COMPL	R	0h	This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software

Table 6-29. TRIGLATCH3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	SD2FLT2_COMPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
17	SD2FLT2_COMPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
16	SD2FLT1_COMPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
15	SD2FLT1_COMPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
14	SD1FLT4_COMPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
13	SD1FLT4_COMPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
12	SD1FLT3_COMPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
11	SD1FLT3_COMPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>

Table 6-29. TRIGLATCH3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SD1FLT2_COMPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
9	SD1FLT2_COMPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
8	SD1FLT1_COMPH	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
7	SD1FLT1_COMPL	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
6	ADCDEVT4	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
5	ADCDEVT3	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
4	ADCDEVT2	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
3	ADCDEVT1	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>

Table 6-29. TRIGLATCH3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ADCCEVT4	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
1	ADCCEVT3	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>
0	ADCCEVT2	R	0h	<p>This register is used to latch the inputs of the X-Bars to provide software knowledge of the input sources which got triggered.</p> <p>1: Corresponding Input was triggered 0: Corresponding Input was not triggered</p> <p>Note: [1] setting of this bit has priority over clear by software</p>

6.4.2.19 TRIGLATCHCLR1 Register (offset = 28h) [reset = 0h]

TRIGLATCHCLR1 is shown in [Figure 6-25](#) and described in [Table 6-30](#).

X-Bar Input Latch Clear Register 1

Figure 6-25. TRIGLATCHCLR1 Register

31	30	29	28	27	26	25	24
CMPSS8_CTRI POUTH	CMPSS8_CTRI POUTL	CMPSS7_CTRI POUTH	CMPSS7_CTRI POUTL	CMPSS6_CTRI POUTH	CMPSS6_CTRI POUTL	CMPSS5_CTRI POUTH	CMPSS5_CTRI POUTL
R=0/W=1-0h							
23	22	21	20	19	18	17	16
CMPSS4_CTRI POUTH	CMPSS4_CTRI POUTL	CMPSS3_CTRI POUTH	CMPSS3_CTRI POUTL	CMPSS2_CTRI POUTH	CMPSS2_CTRI POUTL	CMPSS1_CTRI POUTH	CMPSS1_CTRI POUTL
R=0/W=1-0h							
15	14	13	12	11	10	9	8
CMPSS8_CTRI PH	CMPSS8_CTRI PL	CMPSS7_CTRI PH	CMPSS7_CTRI PL	CMPSS6_CTRI PH	CMPSS6_CTRI PL	CMPSS5_CTRI PH	CMPSS5_CTRI PL
R=0/W=1-0h							
7	6	5	4	3	2	1	0
CMPSS4_CTRI PH	CMPSS4_CTRI PL	CMPSS3_CTRI PH	CMPSS3_CTRI PL	CMPSS2_CTRI PH	CMPSS2_CTRI PL	CMPSS1_CTRI PH	CMPSS1_CTRI PL
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-30. TRIGLATCHCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMPSS8_CTRIPOUTH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
30	CMPSS8_CTRIPOUTL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
29	CMPSS7_CTRIPOUTH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
28	CMPSS7_CTRIPOUTL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
27	CMPSS6_CTRIPOUTH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
26	CMPSS6_CTRIPOUTL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
25	CMPSS5_CTRIPOUTH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
24	CMPSS5_CTRIPOUTL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
23	CMPSS4_CTRIPOUTH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect

Table 6-30. TRIGLATCHCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	CMPSS4_CTRIPOUTL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
21	CMPSS3_CTRIPOUTH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
20	CMPSS3_CTRIPOUTL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
19	CMPSS2_CTRIPOUTH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
18	CMPSS2_CTRIPOUTL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
17	CMPSS1_CTRIPOUTH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
16	CMPSS1_CTRIPOUTL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
15	CMPSS8_CTRIPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
14	CMPSS8_CTRIPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
13	CMPSS7_CTRIPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
12	CMPSS7_CTRIPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
11	CMPSS6_CTRIPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
10	CMPSS6_CTRIPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
9	CMPSS5_CTRIPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
8	CMPSS5_CTRIPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
7	CMPSS4_CTRIPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
6	CMPSS4_CTRIPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect

Table 6-30. TRIGLATCHCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CMPSS3_CTRIPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
4	CMPSS3_CTRIPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
3	CMPSS2_CTRIPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
2	CMPSS2_CTRIPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
1	CMPSS1_CTRIPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect
0	CMPSS1_CTRIPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT1 register. Writing 0 has no effect

6.4.2.20 TRIGLATCHCLR2 Register (offset = 2Ah) [reset = 0h]TRIGLATCHCLR2 is shown in [Figure 6-26](#) and described in [Table 6-31](#).

X-Bar Input Latch Clear Register 2

Figure 6-26. TRIGLATCHCLR2 Register

31	30	29	28	27	26	25	24
ADCCEVT1	ADCB EVT4	ADCB EVT3	ADCB EVT2	ADCB EVT1	ADCA EVT4	ADCA EVT3	ADCA EVT2
R=0/W=1-0h							
23	22	21	20	19	18	17	16
ADCA EVT1	EXTSYNCOUT	ECAP6_OUT	ECAP5_OUT	ECAP4_OUT	ECAP3_OUT	ECAP2_OUT	ECAP1_OUT
R=0/W=1-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
ADCSOCB	ADCSOCA	INPUT7	INPUT5	INPUT4	INPUT3	INPUT2	INPUT1
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-31. TRIGLATCHCLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ADCCEVT1	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
30	ADCB EVT4	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
29	ADCB EVT3	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
28	ADCB EVT2	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
27	ADCB EVT1	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
26	ADCA EVT4	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
25	ADCA EVT3	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
24	ADCA EVT2	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
23	ADCA EVT1	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
22	EXTSYNCOUT	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect

Table 6-31. TRIGLATCHCLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ECAP6_OUT	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
20	ECAP5_OUT	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
19	ECAP4_OUT	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
18	ECAP3_OUT	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
17	ECAP2_OUT	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
16	ECAP1_OUT	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	ADCSOCB	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
6	ADCSOCA	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
5	INPUT7	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
4	INPUT5	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
3	INPUT4	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
2	INPUT3	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
1	INPUT2	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect
0	INPUT1	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT2 register. Writing 0 has no effect

6.4.2.21 TRIGLATCHCLR3 Register (offset = 2Ch) [reset = 0h]

TRIGLATCHCLR3 is shown in [Figure 6-27](#) and described in [Table 6-32](#).

X-Bar Input Latch Clear Register 3

Figure 6-27. TRIGLATCHCLR3 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED	SD2FLT4_CO MPH	SD2FLT4_CO MPL	SD2FLT3_CO MPH	SD2FLT3_CO MPL	SD2FLT2_CO MPH	SD2FLT2_CO MPL	SD2FLT1_CO MPH
R=0-0h	R=0/W=1-0h						
15	14	13	12	11	10	9	8
SD2FLT1_CO MPL	SD1FLT4_CO MPH	SD1FLT4_CO MPL	SD1FLT3_CO MPH	SD1FLT3_CO MPL	SD1FLT2_CO MPH	SD1FLT2_CO MPL	SD1FLT1_CO MPH
R=0/W=1-0h							
7	6	5	4	3	2	1	0
SD1FLT1_CO MPL	ADCDEVT4	ADCDEVT3	ADCDEVT2	ADCDEVT1	ADCCEVT4	ADCCEVT3	ADCCEVT2
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-32. TRIGLATCHCLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R=0	0h	Reserved
22	SD2FLT4_COMPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
21	SD2FLT4_COMPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
20	SD2FLT3_COMPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
19	SD2FLT3_COMPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
18	SD2FLT2_COMPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
17	SD2FLT2_COMPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
16	SD2FLT1_COMPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
15	SD2FLT1_COMPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect

Table 6-32. TRIGLATCHCLR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	SD1FLT4_COMPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
13	SD1FLT4_COMPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
12	SD1FLT3_COMPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
11	SD1FLT3_COMPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
10	SD1FLT2_COMPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
9	SD1FLT2_COMPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
8	SD1FLT1_COMPH	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
7	SD1FLT1_COMPL	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
6	ADCDEVT4	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
5	ADCDEVT3	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
4	ADCDEVT2	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
3	ADCDEVT1	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
2	ADCCEVT4	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
1	ADCCEVT3	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect
0	ADCCEVT2	R=0/W=1	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARILAT3 register. Writing 0 has no effect

6.4.3 OUTPUT_XBAR_REGS Registers

Table 6-33 lists the memory-mapped registers for the OUTPUT_XBAR_REGS. All register offset addresses not listed in **Table 6-33** should be considered as reserved locations and the register contents should not be modified.

Table 6-33. OUTPUT_XBAR_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	OUTPUT1MUX0TO15CFG	Output X-BAR Mux Configuration for Output 1	Section 6.4.3.1	EALLOW
2h	OUTPUT1MUX16TO31CFG	Output X-BAR Mux Configuration for Output 1	Section 6.4.3.2	EALLOW
4h	OUTPUT2MUX0TO15CFG	Output X-BAR Mux Configuration for Output 2	Section 6.4.3.3	EALLOW
6h	OUTPUT2MUX16TO31CFG	Output X-BAR Mux Configuration for Output 2	Section 6.4.3.4	EALLOW
8h	OUTPUT3MUX0TO15CFG	Output X-BAR Mux Configuration for Output 3	Section 6.4.3.5	EALLOW
Ah	OUTPUT3MUX16TO31CFG	Output X-BAR Mux Configuration for Output 3	Section 6.4.3.6	EALLOW
Ch	OUTPUT4MUX0TO15CFG	Output X-BAR Mux Configuration for Output 4	Section 6.4.3.7	EALLOW
Eh	OUTPUT4MUX16TO31CFG	Output X-BAR Mux Configuration for Output 4	Section 6.4.3.8	EALLOW
10h	OUTPUT5MUX0TO15CFG	Output X-BAR Mux Configuration for Output 5	Section 6.4.3.9	EALLOW
12h	OUTPUT5MUX16TO31CFG	Output X-BAR Mux Configuration for Output 5	Section 6.4.3.10	EALLOW
14h	OUTPUT6MUX0TO15CFG	Output X-BAR Mux Configuration for Output 6	Section 6.4.3.11	EALLOW
16h	OUTPUT6MUX16TO31CFG	Output X-BAR Mux Configuration for Output 6	Section 6.4.3.12	EALLOW
18h	OUTPUT7MUX0TO15CFG	Output X-BAR Mux Configuration for Output 7	Section 6.4.3.13	EALLOW
1Ah	OUTPUT7MUX16TO31CFG	Output X-BAR Mux Configuration for Output 7	Section 6.4.3.14	EALLOW
1Ch	OUTPUT8MUX0TO15CFG	Output X-BAR Mux Configuration for Output 8	Section 6.4.3.15	EALLOW
1Eh	OUTPUT8MUX16TO31CFG	Output X-BAR Mux Configuration for Output 8	Section 6.4.3.16	EALLOW
20h	OUTPUT1MUXENABLE	Output X-BAR Mux Enable for Output 1	Section 6.4.3.17	EALLOW
22h	OUTPUT2MUXENABLE	Output X-BAR Mux Enable for Output 2	Section 6.4.3.18	EALLOW
24h	OUTPUT3MUXENABLE	Output X-BAR Mux Enable for Output 3	Section 6.4.3.19	EALLOW
26h	OUTPUT4MUXENABLE	Output X-BAR Mux Enable for Output 4	Section 6.4.3.20	EALLOW
28h	OUTPUT5MUXENABLE	Output X-BAR Mux Enable for Output 5	Section 6.4.3.21	EALLOW
2Ah	OUTPUT6MUXENABLE	Output X-BAR Mux Enable for Output 6	Section 6.4.3.22	EALLOW
2Ch	OUTPUT7MUXENABLE	Output X-BAR Mux Enable for Output 7	Section 6.4.3.23	EALLOW
2Eh	OUTPUT8MUXENABLE	Output X-BAR Mux Enable for Output 8	Section 6.4.3.24	EALLOW
30h	OUTPUTLATCH	Output X-BAR Output Latch	Section 6.4.3.25	
32h	OUTPUTLATCHCLR	Output X-BAR Output Latch Clear	Section 6.4.3.26	
34h	OUTPUTLATCHFRC	Output X-BAR Output Latch Clear	Section 6.4.3.27	
36h	OUTPUTLATCHENABLE	Output X-BAR Output Latch Enable	Section 6.4.3.28	EALLOW
38h	OUTPUTINV	Output X-BAR Output Inversion	Section 6.4.3.29	EALLOW
3Eh	OUTPUTLOCK	Output X-BAR Configuration Lock register	Section 6.4.3.30	EALLOW

6.4.3.1 OUTPUT1MUX0TO15CFG Register (offset = 0h) [reset = 0h]

OUTPUT1MUX0TO15CFG is shown in [Figure 6-28](#) and described in [Table 6-34](#).

Output X-BAR Mux Configuration for Output 1

Figure 6-28. OUTPUT1MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-34. OUTPUT1MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the Output X-BAR section of this chapter for more details.

Table 6-34. OUTPUT1MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the Output X-BAR section of this chapter for more details.

Table 6-34. OUTPUT1MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.2 OUTPUT1MUX16TO31CFG Register (offset = 2h) [reset = 0h]

OUTPUT1MUX16TO31CFG is shown in [Figure 6-29](#) and described in [Table 6-35](#).

Output X-BAR Mux Configuration for Output 1

Figure 6-29. OUTPUT1MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-35. OUTPUT1MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the Output X-BAR section of this chapter for more details.

Table 6-35. OUTPUT1MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the Output X-BAR section of this chapter for more details.

Table 6-35. OUTPUT1MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for OUTPUT1 of OUTPUT-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.3 OUTPUT2MUX0TO15CFG Register (offset = 4h) [reset = 0h]

OUTPUT2MUX0TO15CFG is shown in [Figure 6-30](#) and described in [Table 6-36](#).

Output X-BAR Mux Configuration for Output 2

Figure 6-30. OUTPUT2MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-36. OUTPUT2MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the Output X-BAR section of this chapter for more details.

Table 6-36. OUTPUT2MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the Output X-BAR section of this chapter for more details.

Table 6-36. OUTPUT2MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.4 OUTPUT2MUX16TO31CFG Register (offset = 6h) [reset = 0h]

OUTPUT2MUX16TO31CFG is shown in [Figure 6-31](#) and described in [Table 6-37](#).

Output X-BAR Mux Configuration for Output 2

Figure 6-31. OUTPUT2MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-37. OUTPUT2MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the Output X-BAR section of this chapter for more details.

Table 6-37. OUTPUT2MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the Output X-BAR section of this chapter for more details.

Table 6-37. OUTPUT2MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for OUTPUT2 of OUTPUT-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.5 OUTPUT3MUX0TO15CFG Register (offset = 8h) [reset = 0h]

OUTPUT3MUX0TO15CFG is shown in [Figure 6-32](#) and described in [Table 6-38](#).

Output X-BAR Mux Configuration for Output 3

Figure 6-32. OUTPUT3MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-38. OUTPUT3MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the Output X-BAR section of this chapter for more details.

Table 6-38. OUTPUT3MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the Output X-BAR section of this chapter for more details.

Table 6-38. OUTPUT3MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.6 OUTPUT3MUX16TO31CFG Register (offset = Ah) [reset = 0h]

OUTPUT3MUX16TO31CFG is shown in [Figure 6-33](#) and described in [Table 6-39](#).

Output X-BAR Mux Configuration for Output 3

Figure 6-33. OUTPUT3MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-39. OUTPUT3MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the Output X-BAR section of this chapter for more details.

Table 6-39. OUTPUT3MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the Output X-BAR section of this chapter for more details.

Table 6-39. OUTPUT3MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for OUTPUT3 of OUTPUT-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.7 OUTPUT4MUX0TO15CFG Register (offset = Ch) [reset = 0h]

OUTPUT4MUX0TO15CFG is shown in [Figure 6-34](#) and described in [Table 6-40](#).

Output X-BAR Mux Configuration for Output 4

Figure 6-34. OUTPUT4MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-40. OUTPUT4MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the Output X-BAR section of this chapter for more details.

Table 6-40. OUTPUT4MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the Output X-BAR section of this chapter for more details.

Table 6-40. OUTPUT4MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.8 OUTPUT4MUX16TO31CFG Register (offset = Eh) [reset = 0h]

OUTPUT4MUX16TO31CFG is shown in [Figure 6-35](#) and described in [Table 6-41](#).

Output X-BAR Mux Configuration for Output 4

Figure 6-35. OUTPUT4MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-41. OUTPUT4MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the Output X-BAR section of this chapter for more details.

Table 6-41. OUTPUT4MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the Output X-BAR section of this chapter for more details.

Table 6-41. OUTPUT4MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for OUTPUT4 of OUTPUT-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.9 OUTPUT5MUX0TO15CFG Register (offset = 10h) [reset = 0h]

OUTPUT5MUX0TO15CFG is shown in [Figure 6-36](#) and described in [Table 6-42](#).

Output X-BAR Mux Configuration for Output 5

Figure 6-36. OUTPUT5MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15		Mux14		Mux13		Mux12		Mux11		Mux10		Mux9		Mux8	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7		Mux6		Mux5		Mux4		Mux3		Mux2		Mux1		Mux0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-42. OUTPUT5MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the Output X-BAR section of this chapter for more details.

Table 6-42. OUTPUT5MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the Output X-BAR section of this chapter for more details.

Table 6-42. OUTPUT5MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.10 OUTPUT5MUX16TO31CFG Register (offset = 12h) [reset = 0h]

OUTPUT5MUX16TO31CFG is shown in [Figure 6-37](#) and described in [Table 6-43](#).

Output X-BAR Mux Configuration for Output 5

Figure 6-37. OUTPUT5MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-43. OUTPUT5MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the Output X-BAR section of this chapter for more details.

Table 6-43. OUTPUT5MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the Output X-BAR section of this chapter for more details.

Table 6-43. OUTPUT5MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for OUTPUT5 of OUTPUT-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.11 OUTPUT6MUX0TO15CFG Register (offset = 14h) [reset = 0h]

OUTPUT6MUX0TO15CFG is shown in [Figure 6-38](#) and described in [Table 6-44](#).

Output X-BAR Mux Configuration for Output 6

Figure 6-38. OUTPUT6MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-44. OUTPUT6MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the Output X-BAR section of this chapter for more details.

Table 6-44. OUTPUT6MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the Output X-BAR section of this chapter for more details.

Table 6-44. OUTPUT6MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.12 OUTPUT6MUX16TO31CFG Register (offset = 16h) [reset = 0h]

OUTPUT6MUX16TO31CFG is shown in [Figure 6-39](#) and described in [Table 6-45](#).

Output X-BAR Mux Configuration for Output 6

Figure 6-39. OUTPUT6MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-45. OUTPUT6MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the Output X-BAR section of this chapter for more details.

Table 6-45. OUTPUT6MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the Output X-BAR section of this chapter for more details.

Table 6-45. OUTPUT6MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for OUTPUT6 of OUTPUT-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.13 OUTPUT7MUX0TO15CFG Register (offset = 18h) [reset = 0h]

OUTPUT7MUX0TO15CFG is shown in [Figure 6-40](#) and described in [Table 6-46](#).

Output X-BAR Mux Configuration for Output 7

Figure 6-40. OUTPUT7MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-46. OUTPUT7MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the Output X-BAR section of this chapter for more details.

Table 6-46. OUTPUT7MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the Output X-BAR section of this chapter for more details.

Table 6-46. OUTPUT7MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.14 OUTPUT7MUX16TO31CFG Register (offset = 1Ah) [reset = 0h]

OUTPUT7MUX16TO31CFG is shown in [Figure 6-41](#) and described in [Table 6-47](#).

Output X-BAR Mux Configuration for Output 7

Figure 6-41. OUTPUT7MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-47. OUTPUT7MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the Output X-BAR section of this chapter for more details.

Table 6-47. OUTPUT7MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the Output X-BAR section of this chapter for more details.

Table 6-47. OUTPUT7MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for OUTPUT7 of OUTPUT-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.15 OUTPUT8MUX0TO15CFG Register (offset = 1Ch) [reset = 0h]

OUTPUT8MUX0TO15CFG is shown in [Figure 6-42](#) and described in [Table 6-48](#).

Output X-BAR Mux Configuration for Output 8

Figure 6-42. OUTPUT8MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-48. OUTPUT8MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the Output X-BAR section of this chapter for more details.

Table 6-48. OUTPUT8MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the Output X-BAR section of this chapter for more details.

Table 6-48. OUTPUT8MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.16 OUTPUT8MUX16TO31CFG Register (offset = 1Eh) [reset = 0h]

OUTPUT8MUX16TO31CFG is shown in [Figure 6-43](#) and described in [Table 6-49](#).

Output X-BAR Mux Configuration for Output 8

Figure 6-43. OUTPUT8MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-49. OUTPUT8MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the Output X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the Output X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the Output X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the Output X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the Output X-BAR section of this chapter for more details.

Table 6-49. OUTPUT8MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the Output X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the Output X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the Output X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the Output X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the Output X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the Output X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the Output X-BAR section of this chapter for more details.

Table 6-49. OUTPUT8MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the Output X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the Output X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the Output X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for OUTPUT8 of OUTPUT-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the Output X-BAR section of this chapter for more details.

6.4.3.17 OUTPUT1MUXENABLE Register (offset = 20h) [reset = 0h]

OUTPUT1MUXENABLE is shown in [Figure 6-44](#) and described in [Table 6-50](#).

Output X-BAR Mux Enable for Output 1

Figure 6-44. OUTPUT1MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-50. OUTPUT1MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux31 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux31 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux30 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux30 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux29 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux29 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux28 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux28 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux27 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux27 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-50. OUTPUT1MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux26 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux26 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux25 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux25 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux24 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux24 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux23 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux23 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux22 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux22 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux21 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux21 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux20 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux20 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux19 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux19 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux18 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux18 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-50. OUTPUT1MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux17 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux17 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux16 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux16 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux15 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux15 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux14 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux14 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux13 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux13 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux12 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux12 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux11 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux11 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux10 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux10 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux9 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux9 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-50. OUTPUT1MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux8 is enabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux8 is disabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux7 is disabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux7 is enabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux6 is disabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux6 is enabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux5 is disabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux5 is enabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux4 is disabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux4 is enabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux3 is disabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux3 is enabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux2 is disabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux2 is enabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux1 is disabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux1 is enabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive OUTPUT1 of OUTPUT-XBAR 0: Respective output of Mux0 is disabled to drive the OUTPUT1 of OUTPUT-XBAR 1: Respective output of Mux0 is enabled to drive the OUTPUT1 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

6.4.3.18 OUTPUT2MUXENABLE Register (offset = 22h) [reset = 0h]

OUTPUT2MUXENABLE is shown in [Figure 6-45](#) and described in [Table 6-51](#).

Output X-BAR Mux Enable for Output 2

Figure 6-45. OUTPUT2MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-51. OUTPUT2MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux31 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux31 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux30 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux30 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux29 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux29 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux28 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux28 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux27 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux27 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-51. OUTPUT2MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux26 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux26 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux25 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux25 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux24 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux24 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux23 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux23 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux22 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux22 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux21 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux21 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux20 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux20 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux19 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux19 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux18 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux18 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-51. OUTPUT2MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux17 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux17 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux16 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux16 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux15 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux15 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux14 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux14 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux13 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux13 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux12 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux12 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux11 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux11 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux10 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux10 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux9 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux9 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-51. OUTPUT2MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux8 is enabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux8 is disabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux7 is disabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux7 is enabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux6 is disabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux6 is enabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux5 is disabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux5 is enabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux4 is disabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux4 is enabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux3 is disabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux3 is enabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux2 is disabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux2 is enabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux1 is disabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux1 is enabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive OUTPUT2 of OUTPUT-XBAR 0: Respective output of Mux0 is disabled to drive the OUTPUT2 of OUTPUT-XBAR 1: Respective output of Mux0 is enabled to drive the OUTPUT2 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

6.4.3.19 OUTPUT3MUXENABLE Register (offset = 24h) [reset = 0h]

OUTPUT3MUXENABLE is shown in [Figure 6-46](#) and described in [Table 6-52](#).

Output X-BAR Mux Enable for Output 3

Figure 6-46. OUTPUT3MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-52. OUTPUT3MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux31 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux31 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux30 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux30 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux29 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux29 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux28 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux28 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux27 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux27 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-52. OUTPUT3MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux26 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux26 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux25 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux25 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux24 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux24 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux23 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux23 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux22 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux22 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux21 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux21 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux20 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux20 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux19 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux19 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux18 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux18 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-52. OUTPUT3MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux17 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux17 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux16 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux16 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux15 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux15 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux14 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux14 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux13 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux13 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux12 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux12 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux11 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux11 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux10 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux10 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux9 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux9 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-52. OUTPUT3MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux8 is enabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux8 is disabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux7 is disabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux7 is enabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux6 is disabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux6 is enabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux5 is disabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux5 is enabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux4 is disabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux4 is enabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux3 is disabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux3 is enabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux2 is disabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux2 is enabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux1 is disabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux1 is enabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive OUTPUT3 of OUTPUT-XBAR 0: Respective output of Mux0 is disabled to drive the OUTPUT3 of OUTPUT-XBAR 1: Respective output of Mux0 is enabled to drive the OUTPUT3 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

6.4.3.20 OUTPUT4MUXENABLE Register (offset = 26h) [reset = 0h]

OUTPUT4MUXENABLE is shown in [Figure 6-47](#) and described in [Table 6-53](#).

Output X-BAR Mux Enable for Output 4

Figure 6-47. OUTPUT4MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-53. OUTPUT4MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux31 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux31 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux30 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux30 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux29 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux29 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux28 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux28 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux27 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux27 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-53. OUTPUT4MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux26 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux26 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux25 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux25 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux24 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux24 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux23 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux23 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux22 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux22 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux21 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux21 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux20 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux20 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux19 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux19 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux18 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux18 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-53. OUTPUT4MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux17 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux17 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux16 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux16 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux15 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux15 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux14 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux14 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux13 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux13 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux12 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux12 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux11 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux11 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux10 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux10 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux9 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux9 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-53. OUTPUT4MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux8 is enabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux8 is disabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux7 is disabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux7 is enabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux6 is disabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux6 is enabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux5 is disabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux5 is enabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux4 is disabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux4 is enabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux3 is disabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux3 is enabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux2 is disabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux2 is enabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux1 is disabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux1 is enabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive OUTPUT4 of OUTPUT-XBAR 0: Respective output of Mux0 is disabled to drive the OUTPUT4 of OUTPUT-XBAR 1: Respective output of Mux0 is enabled to drive the OUTPUT4 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

6.4.3.21 OUTPUT5MUXENABLE Register (offset = 28h) [reset = 0h]

OUTPUT5MUXENABLE is shown in [Figure 6-48](#) and described in [Table 6-54](#).

Output X-BAR Mux Enable for Output 5

Figure 6-48. OUTPUT5MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-54. OUTPUT5MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux31 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux31 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux30 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux30 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux29 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux29 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux28 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux28 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux27 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux27 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-54. OUTPUT5MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux26 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux26 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux25 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux25 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux24 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux24 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux23 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux23 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux22 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux22 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux21 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux21 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux20 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux20 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux19 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux19 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux18 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux18 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-54. OUTPUT5MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux17 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux17 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux16 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux16 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux15 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux15 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux14 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux14 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux13 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux13 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux12 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux12 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux11 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux11 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux10 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux10 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux9 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux9 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-54. OUTPUT5MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux8 is enabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux8 is disabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux7 is disabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux7 is enabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux6 is disabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux6 is enabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux5 is disabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux5 is enabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux4 is disabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux4 is enabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux3 is disabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux3 is enabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux2 is disabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux2 is enabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux1 is disabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux1 is enabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive OUTPUT5 of OUTPUT-XBAR 0: Respective output of Mux0 is disabled to drive the OUTPUT5 of OUTPUT-XBAR 1: Respective output of Mux0 is enabled to drive the OUTPUT5 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

6.4.3.22 OUTPUT6MUXENABLE Register (offset = 2Ah) [reset = 0h]

OUTPUT6MUXENABLE is shown in [Figure 6-49](#) and described in [Table 6-55](#).

Output X-BAR Mux Enable for Output 6

Figure 6-49. OUTPUT6MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-55. OUTPUT6MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux31 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux31 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux30 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux30 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux29 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux29 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux28 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux28 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux27 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux27 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-55. OUTPUT6MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux26 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux26 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux25 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux25 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux24 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux24 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux23 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux23 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux22 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux22 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux21 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux21 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux20 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux20 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux19 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux19 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux18 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux18 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-55. OUTPUT6MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux17 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux17 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux16 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux16 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux15 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux15 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux14 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux14 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux13 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux13 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux12 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux12 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux11 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux11 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux10 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux10 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux9 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux9 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-55. OUTPUT6MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux8 is enabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux8 is disabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux7 is disabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux7 is enabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux6 is disabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux6 is enabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux5 is disabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux5 is enabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux4 is disabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux4 is enabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux3 is disabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux3 is enabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux2 is disabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux2 is enabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux1 is disabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux1 is enabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive OUTPUT6 of OUTPUT-XBAR 0: Respective output of Mux0 is disabled to drive the OUTPUT6 of OUTPUT-XBAR 1: Respective output of Mux0 is enabled to drive the OUTPUT6 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

6.4.3.23 OUTPUT7MUXENABLE Register (offset = 2Ch) [reset = 0h]

OUTPUT7MUXENABLE is shown in [Figure 6-50](#) and described in [Table 6-56](#).

Output X-BAR Mux Enable for Output 7

Figure 6-50. OUTPUT7MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-56. OUTPUT7MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux31 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux31 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux30 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux30 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux29 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux29 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux28 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux28 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux27 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux27 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-56. OUTPUT7MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux26 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux26 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux25 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux25 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux24 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux24 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux23 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux23 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux22 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux22 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux21 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux21 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux20 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux20 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux19 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux19 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux18 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux18 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-56. OUTPUT7MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux17 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux17 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux16 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux16 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux15 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux15 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux14 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux14 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux13 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux13 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux12 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux12 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux11 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux11 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux10 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux10 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux9 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux9 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-56. OUTPUT7MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux8 is enabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux8 is disabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux7 is disabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux7 is enabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux6 is disabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux6 is enabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux5 is disabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux5 is enabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux4 is disabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux4 is enabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux3 is disabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux3 is enabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux2 is disabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux2 is enabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux1 is disabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux1 is enabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive OUTPUT7 of OUTPUT-XBAR 0: Respective output of Mux0 is disabled to drive the OUTPUT7 of OUTPUT-XBAR 1: Respective output of Mux0 is enabled to drive the OUTPUT7 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

6.4.3.24 OUTPUT8MUXENABLE Register (offset = 2Eh) [reset = 0h]

OUTPUT8MUXENABLE is shown in [Figure 6-51](#) and described in [Table 6-57](#).

Output X-BAR Mux Enable for Output 8

Figure 6-51. OUTPUT8MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-57. OUTPUT8MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux31 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux31 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux30 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux30 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux29 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux29 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux28 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux28 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux27 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux27 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-57. OUTPUT8MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux26 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux26 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux25 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux25 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux24 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux24 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux23 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux23 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux22 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux22 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux21 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux21 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux20 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux20 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux19 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux19 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux18 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux18 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-57. OUTPUT8MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux17 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux17 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux16 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux16 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux15 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux15 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux14 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux14 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux13 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux13 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux12 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux12 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux11 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux11 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux10 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux10 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux9 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux9 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

Table 6-57. OUTPUT8MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux8 is enabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux8 is disabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux7 is disabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux7 is enabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux6 is disabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux6 is enabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux5 is disabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux5 is enabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux4 is disabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux4 is enabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux3 is disabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux3 is enabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux2 is disabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux2 is enabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux1 is disabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux1 is enabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive OUTPUT8 of OUTPUT-XBAR 0: Respective output of Mux0 is disabled to drive the OUTPUT8 of OUTPUT-XBAR 1: Respective output of Mux0 is enabled to drive the OUTPUT8 of OUTPUT-XBAR Refer to the Output X-BAR section of this chapter for more details.

6.4.3.25 OUTPUTLATCH Register (offset = 30h) [reset = 0h]

OUTPUTLATCH is shown in [Figure 6-52](#) and described in [Table 6-58](#).

Output X-BAR Output Latch

Figure 6-52. OUTPUTLATCH Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-58. OUTPUTLATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	OUT7	R	0h	Records the OUTPUT8 of OUTPUT-XBAR. 0: Respective output was not triggered 1: Respective output is triggered Refer to the Output X-BAR section of this chapter for more details. Note: [1] setting of this bit has priority over clear by software
6	OUT6	R	0h	Records the OUTPUT7 of OUTPUT-XBAR. 0: Respective output was not triggered 1: Respective output is triggered Refer to the Output X-BAR section of this chapter for more details. Note: [1] setting of this bit has priority over clear by software
5	OUT5	R	0h	Records the OUTPUT6 of OUTPUT-XBAR. 0: Respective output was not triggered 1: Respective output is triggered Refer to the Output X-BAR section of this chapter for more details. Note: [1] setting of this bit has priority over clear by software
4	OUT4	R	0h	Records the OUTPUT5 of OUTPUT-XBAR. 0: Respective output was not triggered 1: Respective output is triggered Refer to the Output X-BAR section of this chapter for more details. Note: [1] setting of this bit has priority over clear by software

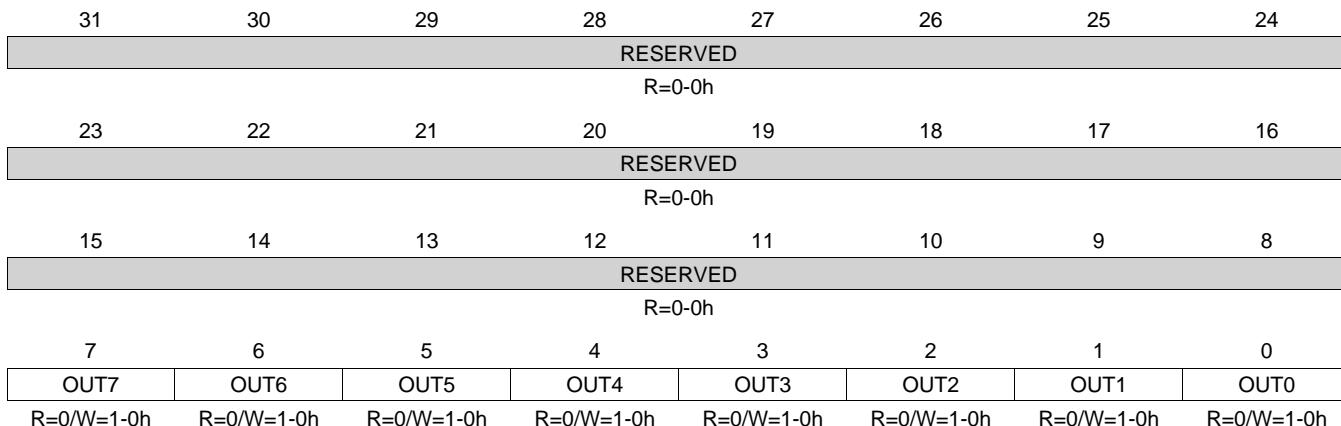
Table 6-58. OUTPUTLATCH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT3	R	0h	Records the OUTPUT4 of OUTPUT-XBAR. 0: Respective output was not triggered 1: Respective output is triggered Refer to the Output X-BAR section of this chapter for more details. Note: [1] setting of this bit has priority over clear by software
2	OUT2	R	0h	Records the OUTPUT3 of OUTPUT-XBAR. 0: Respective output was not triggered 1: Respective output is triggered Refer to the Output X-BAR section of this chapter for more details. Note: [1] setting of this bit has priority over clear by software
1	OUT1	R	0h	Records the OUTPUT2 of OUTPUT-XBAR. 0: Respective output was not triggered 1: Respective output is triggered Refer to the Output X-BAR section of this chapter for more details. Note: [1] setting of this bit has priority over clear by software
0	OUT0	R	0h	Records the OUTPUT1 of OUTPUT-XBAR. 0: Respective output was not triggered 1: Respective output is triggered Refer to the Output X-BAR section of this chapter for more details. Note: [1] setting of this bit has priority over clear by software

6.4.3.26 OUTPUTLATCHCLR Register (offset = 32h) [reset = 0h]

OUTPUTLATCHCLR is shown in [Figure 6-53](#) and described in [Table 6-59](#).

Output X-BAR Output Latch Clear

Figure 6-53. OUTPUTLATCHCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-59. OUTPUTLATCHCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	OUT7	R=0/W=1	0h	Clears the Output-Latch for OUTPUT8 of OUTPUT-XBAR Writing 1 clears the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
6	OUT6	R=0/W=1	0h	Clears the Output-Latch for OUTPUT7 of OUTPUT-XBAR Writing 1 clears the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
5	OUT5	R=0/W=1	0h	Clears the Output-Latch for OUTPUT6 of OUTPUT-XBAR Writing 1 clears the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
4	OUT4	R=0/W=1	0h	Clears the Output-Latch for OUTPUT5 of OUTPUT-XBAR Writing 1 clears the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
3	OUT3	R=0/W=1	0h	Clears the Output-Latch for OUTPUT4 of OUTPUT-XBAR Writing 1 clears the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.

Table 6-59. OUTPUTLATCHCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OUT2	R=0/W=1	0h	<p>Clears the Output-Latch for OUTPUT3 of OUTPUT-XBAR</p> <p>Writing 1 clears the corresponding output latch bit in the OUTPUT-XBAROLAT register</p> <p>Write of 0 has no effect</p> <p>Refer to the Output X-BAR section of this chapter for more details.</p>
1	OUT1	R=0/W=1	0h	<p>Clears the Output-Latch for OUTPUT2 of OUTPUT-XBAR</p> <p>Writing 1 clears the corresponding output latch bit in the OUTPUT-XBAROLAT register</p> <p>Write of 0 has no effect</p> <p>Refer to the Output X-BAR section of this chapter for more details.</p>
0	OUT0	R=0/W=1	0h	<p>Clears the Output-Latch for OUTPUT1 of OUTPUT-XBAR</p> <p>Writing 1 clears the corresponding output latch bit in the OUTPUT-XBAROLAT register</p> <p>Write of 0 has no effect</p> <p>Refer to the Output X-BAR section of this chapter for more details.</p>

6.4.3.27 OUTPUTLATCHFRC Register (offset = 34h) [reset = 0h]

OUTPUTLATCHFRC is shown in [Figure 6-54](#) and described in [Table 6-60](#).

Output X-BAR Output Latch Clear

Figure 6-54. OUTPUTLATCHFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-60. OUTPUTLATCHFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	OUT7	R=0/W=1	0h	Sets the Output-Latch for OUTPUT8 of OUTPUT-XBAR Writing 1 sets the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
6	OUT6	R=0/W=1	0h	Sets the Output-Latch for OUTPUT7 of OUTPUT-XBAR Writing 1 sets the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
5	OUT5	R=0/W=1	0h	Sets the Output-Latch for OUTPUT6 of OUTPUT-XBAR Writing 1 sets the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
4	OUT4	R=0/W=1	0h	Sets the Output-Latch for OUTPUT5 of OUTPUT-XBAR Writing 1 sets the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
3	OUT3	R=0/W=1	0h	Sets the Output-Latch for OUTPUT4 of OUTPUT-XBAR Writing 1 sets the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.

Table 6-60. OUTPUTLATCHFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OUT2	R=0/W=1	0h	Sets the Output-Latch for OUTPUT3 of OUTPUT-XBAR Writing 1 sets the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
1	OUT1	R=0/W=1	0h	Sets the Output-Latch for OUTPUT2 of OUTPUT-XBAR Writing 1 sets the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.
0	OUT0	R=0/W=1	0h	Sets the Output-Latch for OUTPUT1 of OUTPUT-XBAR Writing 1 sets the corresponding output latch bit in the OUTPUT-XBAROLAT register Write of 0 has no effect Refer to the Output X-BAR section of this chapter for more details.

6.4.3.28 OUTPUTLATCHENABLE Register (offset = 36h) [reset = 0h]

OUTPUTLATCHENABLE is shown in [Figure 6-55](#) and described in [Table 6-61](#).

Output X-BAR Output Latch Enable

Figure 6-55. OUTPUTLATCHENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-61. OUTPUTLATCHENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	OUT7	R/W	0h	Selects the output latch to drive output7 for OUTPUT-XBAR 0: Output Latch is not selected to driven the respective output 1: Output Latch is selected to drive the respective output Refer to the Output X-BAR section of this chapter for more details.
6	OUT6	R/W	0h	Selects the output latch to drive output6 for OUTPUT-XBAR 0: Output Latch is not selected to driven the respective output 1: Output Latch is selected to drive the respective output Refer to the Output X-BAR section of this chapter for more details.
5	OUT5	R/W	0h	Selects the output latch to drive output5 for OUTPUT-XBAR 0: Output Latch is not selected to driven the respective output 1: Output Latch is selected to drive the respective output Refer to the Output X-BAR section of this chapter for more details.
4	OUT4	R/W	0h	Selects the output latch to drive output4 for OUTPUT-XBAR 0: Output Latch is not selected to driven the respective output 1: Output Latch is selected to drive the respective output Refer to the Output X-BAR section of this chapter for more details.
3	OUT3	R/W	0h	Selects the output latch to drive output3 for OUTPUT-XBAR 0: Output Latch is not selected to driven the respective output 1: Output Latch is selected to drive the respective output Refer to the Output X-BAR section of this chapter for more details.
2	OUT2	R/W	0h	Selects the output latch to drive output2 for OUTPUT-XBAR 0: Output Latch is not selected to driven the respective output 1: Output Latch is selected to drive the respective output Refer to the Output X-BAR section of this chapter for more details.

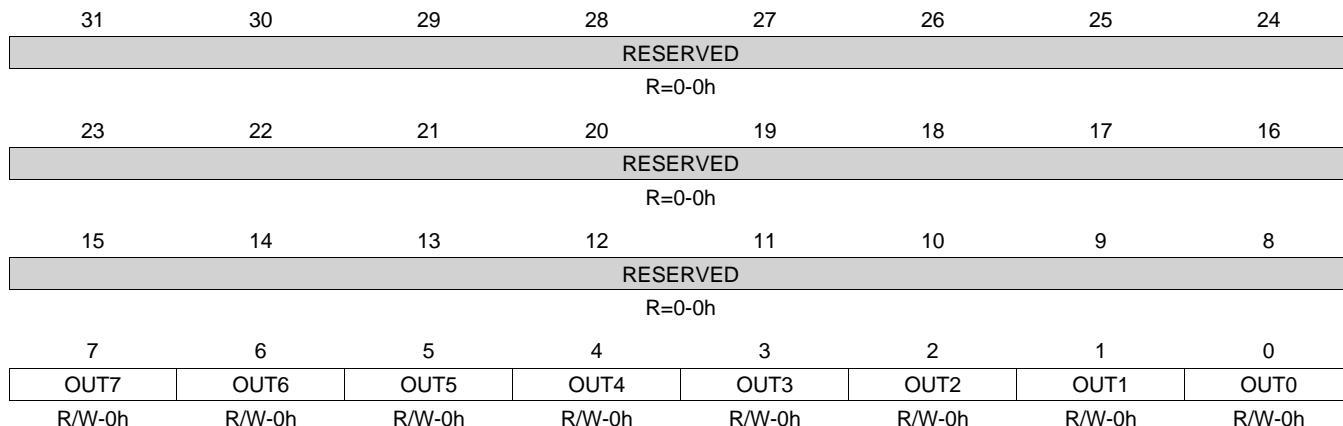
Table 6-61. OUTPUTLATCHENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OUT1	R/W	0h	Selects the output latch to drive output1 for OUTPUT-XBAR 0: Output Latch is not selected to driven the respective output 1: Output Latch is selected to drive the respective output Refer to the Output X-BAR section of this chapter for more details.
0	OUT0	R/W	0h	Selects the output latch to drive OUTPUT1 for OUTPUT-XBAR 0: Output Latch is not selected to driven the respective output 1: Output Latch is selected to drive the respective output Refer to the Output X-BAR section of this chapter for more details.

6.4.3.29 OUTPUTINV Register (offset = 38h) [reset = 0h]

OUTPUTINV is shown in [Figure 6-56](#) and described in [Table 6-62](#).

Output X-BAR Output Inversion

Figure 6-56. OUTPUTINV Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-62. OUTPUTINV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	OUT7	R/W	0h	Selects polarity for OUTPUT8 of OUTPUT-XBAR 0: drives active high output 1: drives active-low output Refer to the Output X-BAR section of this chapter for more details.
6	OUT6	R/W	0h	Selects polarity for OUTPUT7 of OUTPUT-XBAR 0: drives active high output 1: drives active-low output Refer to the Output X-BAR section of this chapter for more details.
5	OUT5	R/W	0h	Selects polarity for OUTPUT6 of OUTPUT-XBAR 0: drives active high output 1: drives active-low output Refer to the Output X-BAR section of this chapter for more details.
4	OUT4	R/W	0h	Selects polarity for OUTPUT5 of OUTPUT-XBAR 0: drives active high output 1: drives active-low output Refer to the Output X-BAR section of this chapter for more details.
3	OUT3	R/W	0h	Selects polarity for OUTPUT4 of OUTPUT-XBAR 0: drives active high output 1: drives active-low output Refer to the Output X-BAR section of this chapter for more details.
2	OUT2	R/W	0h	Selects polarity for OUTPUT3 of OUTPUT-XBAR 0: drives active high output 1: drives active-low output Refer to the Output X-BAR section of this chapter for more details.

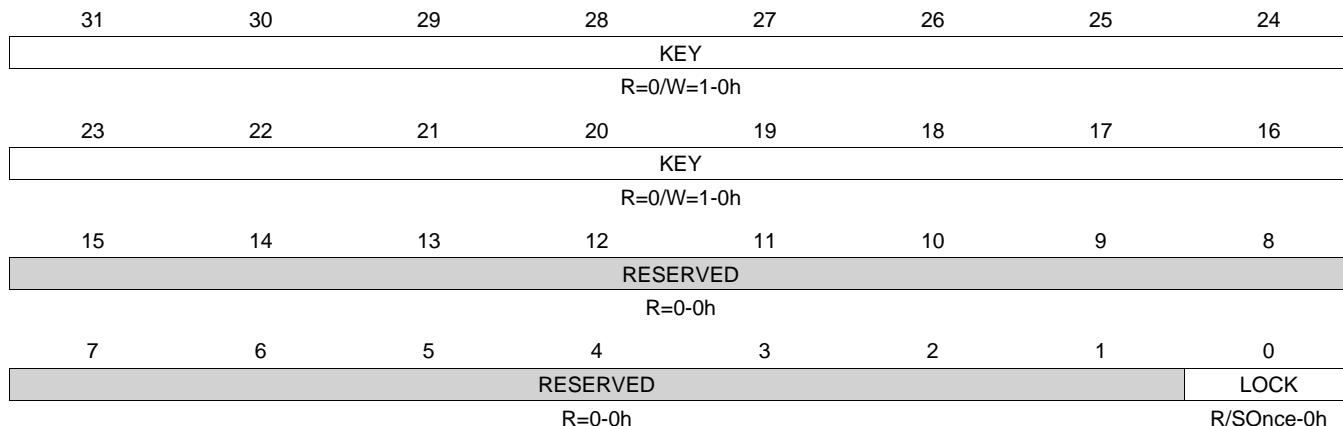
Table 6-62. OUTPUTINV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OUT1	R/W	0h	Selects polarity for OUTPUT2 of OUTPUT-XBAR 0: drives active high output 1: drives active-low output Refer to the Output X-BAR section of this chapter for more details.
0	OUT0	R/W	0h	Selects polarity for OUTPUT1 of OUTPUT-XBAR 0: drives active high output 1: drives active-low output Refer to the Output X-BAR section of this chapter for more details.

6.4.3.30 OUTPUTLOCK Register (offset = 3Eh) [reset = 0h]

OUTPUTLOCK is shown in [Figure 6-57](#) and described in [Table 6-63](#).

Output X-BAR Configuration Lock register

Figure 6-57. OUTPUTLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-63. OUTPUTLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R=0/W=1	0h	Bit-0 of this register can be set only if KEY= 0x5a5a
15-1	RESERVED	R=0	0h	Reserved
0	LOCK	R/SOnce	0h	<p>Locks the configuration for OUTPUT-XBAR. Once the configuration is locked, writes to the below registers for OUTPUT-XBAR is blocked.</p> <p>Registers Affected by the LOCK mechanism:</p> <ul style="list-style-type: none"> OUTPUT-XBAROUTyMUX0TO15CFG OUTPUT-XBAROUTyMUX16TO31CFG OUTPUT-XBAROUTyMUXENABLE OUTPUT-XBAROUTLATEN OUTPUT-XBAROUTINV <p>0: Writes to the above registers are allowed</p> <p>1: Writes to the above registers are blocked</p> <p>Note:</p> <p>[1] LOCK mechanism only applies to writes. Reads are never blocked.</p>

6.4.4 GPIO_CTRL_REGS Registers

Table 6-64 lists the memory-mapped registers for the GPIO_CTRL_REGS. All register offset addresses not listed in [Table 6-64](#) should be considered as reserved locations and the register contents should not be modified.

Table 6-64. GPIO_CTRL_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	GPACTRL	GPIO A Qualification Sampling Period Control (GPIO0 to 31)	Section 6.4.4.1	EALLOW
2h	GPAQSEL1	GPIO A Qualifier Select 1 Register (GPIO0 to 15)	Section 6.4.4.2	EALLOW
4h	GPAQSEL2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)	Section 6.4.4.3	EALLOW
6h	GPAMUX1	GPIO A Mux 1 Register (GPIO0 to 15)	Section 6.4.4.4	EALLOW
8h	GPAMUX2	GPIO A Mux 2 Register (GPIO16 to 31)	Section 6.4.4.5	EALLOW
Ah	GPADIR	GPIO A Direction Register (GPIO0 to 31)	Section 6.4.4.6	EALLOW
Ch	GPAPUD	GPIO A Pull Up Disable Register (GPIO0 to 31)	Section 6.4.4.7	EALLOW
10h	GPAINV	GPIO A Input Polarity Invert Registers (GPIO0 to 31)	Section 6.4.4.8	EALLOW
12h	GPAODR	GPIO A Open Drain Output Register (GPIO0 to GPIO31)	Section 6.4.4.9	EALLOW
20h	GPAGMUX1	GPIO A Peripheral Group Mux (GPIO0 to 15)	Section 6.4.4.10	EALLOW
22h	GPAGMUX2	GPIO A Peripheral Group Mux (GPIO16 to 31)	Section 6.4.4.11	EALLOW
28h	GPACSEL1	GPIO A Core Select Register (GPIO0 to 7)	Section 6.4.4.12	EALLOW
2Ah	GPACSEL2	GPIO A Core Select Register (GPIO8 to 15)	Section 6.4.4.13	EALLOW
2Ch	GPACSEL3	GPIO A Core Select Register (GPIO16 to 23)	Section 6.4.4.14	EALLOW
2Eh	GPACSEL4	GPIO A Core Select Register (GPIO24 to 31)	Section 6.4.4.15	EALLOW
3Ch	GPALOCK	GPIO A Lock Configuration Register (GPIO0 to 31)	Section 6.4.4.16	EALLOW
3Eh	GPACR	GPIO A Lock Commit Register (GPIO0 to 31)	Section 6.4.4.17	EALLOW
40h	GPBCTRL	GPIO B Qualification Sampling Period Control (GPIO32 to 63)	Section 6.4.4.18	EALLOW
42h	GPBQSEL1	GPIO B Qualifier Select 1 Register (GPIO32 to 47)	Section 6.4.4.19	EALLOW
44h	GPBQSEL2	GPIO B Qualifier Select 2 Register (GPIO48 to 63)	Section 6.4.4.20	EALLOW
46h	GPBMUX1	GPIO B Mux 1 Register (GPIO32 to 47)	Section 6.4.4.21	EALLOW
48h	GPBMUX2	GPIO B Mux 2 Register (GPIO48 to 63)	Section 6.4.4.22	EALLOW
4Ah	GPBDIR	GPIO B Direction Register (GPIO32 to 63)	Section 6.4.4.23	EALLOW
4Ch	GPBPUD	GPIO B Pull Up Disable Register (GPIO32 to 63)	Section 6.4.4.24	EALLOW
50h	GPBINV	GPIO B Input Polarity Invert Registers (GPIO32 to 63)	Section 6.4.4.25	EALLOW
52h	GPBODR	GPIO B Open Drain Output Register (GPIO32 to GPIO63)	Section 6.4.4.26	EALLOW
54h	GPBAMSEL	GPIO B Analog Mode Select register (GPIO32 to GPIO63)	Section 6.4.4.27	EALLOW
60h	GPBGMUX1	GPIO B Peripheral Group Mux (GPIO32 to 47)	Section 6.4.4.28	EALLOW
62h	GPBGMUX2	GPIO B Peripheral Group Mux (GPIO48 to 63)	Section 6.4.4.29	EALLOW
68h	GPBCSEL1	GPIO B Core Select Register (GPIO32 to 39)	Section 6.4.4.30	EALLOW
6Ah	GPBCSEL2	GPIO B Core Select Register (GPIO40 to 47)	Section 6.4.4.31	EALLOW

Table 6-64. GPIO_CTRL_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
6Ch	GPBCSEL3	GPIO B Core Select Register (GPIO48 to 55)	Section 6.4.4.32	EALLOW
6Eh	GPBCSEL4	GPIO B Core Select Register (GPIO56 to 63)	Section 6.4.4.33	EALLOW
7Ch	GPBLOCK	GPIO B Lock Configuration Register (GPIO32 to 63)	Section 6.4.4.34	EALLOW
7Eh	GPBCR	GPIO B Lock Commit Register (GPIO32 to 63)	Section 6.4.4.35	EALLOW
80h	GPCCTRL	GPIO C Qualification Sampling Period Control (GPIO64 to 95)	Section 6.4.4.36	EALLOW
82h	GPCQSEL1	GPIO C Qualifier Select 1 Register (GPIO64 to 79)	Section 6.4.4.37	EALLOW
84h	GPCQSEL2	GPIO C Qualifier Select 2 Register (GPIO80 to 95)	Section 6.4.4.38	EALLOW
86h	GPCMUX1	GPIO C Mux 1 Register (GPIO64 to 79)	Section 6.4.4.39	EALLOW
88h	GPCMUX2	GPIO C Mux 2 Register (GPIO80 to 95)	Section 6.4.4.40	EALLOW
8Ah	GPCDIR	GPIO C Direction Register (GPIO64 to 95)	Section 6.4.4.41	EALLOW
8Ch	GPCPUD	GPIO C Pull Up Disable Register (GPIO64 to 95)	Section 6.4.4.42	EALLOW
90h	GPCINV	GPIO C Input Polarity Invert Registers (GPIO64 to 95)	Section 6.4.4.43	EALLOW
92h	GPCODR	GPIO C Open Drain Output Register (GPIO64 to GPIO95)	Section 6.4.4.44	EALLOW
A0h	GPCGMUX1	GPIO C Peripheral Group Mux (GPIO64 to 79)	Section 6.4.4.45	EALLOW
A2h	GPCGMUX2	GPIO C Peripheral Group Mux (GPIO80 to 95)	Section 6.4.4.46	EALLOW
A8h	GPCCSEL1	GPIO C Core Select Register (GPIO64 to 71)	Section 6.4.4.47	EALLOW
AAh	GPCCSEL2	GPIO C Core Select Register (GPIO72 to 79)	Section 6.4.4.48	EALLOW
ACh	GPCCSEL3	GPIO C Core Select Register (GPIO80 to 87)	Section 6.4.4.49	EALLOW
AEh	GPCCSEL4	GPIO C Core Select Register (GPIO88 to 95)	Section 6.4.4.50	EALLOW
BCh	GPCLOCK	GPIO C Lock Configuration Register (GPIO64 to 95)	Section 6.4.4.51	EALLOW
BEh	GPCCR	GPIO C Lock Commit Register (GPIO64 to 95)	Section 6.4.4.52	EALLOW
C0h	GPDCTRL	GPIO D Qualification Sampling Period Control (GPIO96 to 127)	Section 6.4.4.53	EALLOW
C2h	GPDQSEL1	GPIO D Qualifier Select 1 Register (GPIO96 to 111)	Section 6.4.4.54	EALLOW
C4h	GPDQSEL2	GPIO D Qualifier Select 2 Register (GPIO112 to 127)	Section 6.4.4.55	EALLOW
C6h	GPDMUX1	GPIO D Mux 1 Register (GPIO96 to 111)	Section 6.4.4.56	EALLOW
C8h	GPDMUX2	GPIO D Mux 2 Register (GPIO112 to 127)	Section 6.4.4.57	EALLOW
CAh	GPDDIR	GPIO D Direction Register (GPIO96 to 127)	Section 6.4.4.58	EALLOW
CCh	GPDPUD	GPIO D Pull Up Disable Register (GPIO96 to 127)	Section 6.4.4.59	EALLOW
D0h	GPDINV	GPIO D Input Polarity Invert Registers (GPIO96 to 127)	Section 6.4.4.60	EALLOW
D2h	GPDODR	GPIO D Open Drain Output Register (GPIO96 to GPIO127)	Section 6.4.4.61	EALLOW
E0h	GPDGMUX1	GPIO D Peripheral Group Mux (GPIO96 to 111)	Section 6.4.4.62	EALLOW
E2h	GPDGMUX2	GPIO D Peripheral Group Mux (GPIO112 to 127)	Section 6.4.4.63	EALLOW

Table 6-64. GPIO_CTRL_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
E8h	GPDCSEL1	GPIO D Core Select Register (GPIO96 to 103)	Section 6.4.4.64	EALLOW
EAh	GPDCSEL2	GPIO D Core Select Register (GPIO104 to 111)	Section 6.4.4.65	EALLOW
EC _h	GPDCSEL3	GPIO D Core Select Register (GPIO112 to 119)	Section 6.4.4.66	EALLOW
EE _h	GPDCSEL4	GPIO D Core Select Register (GPIO120 to 127)	Section 6.4.4.67	EALLOW
FCh	GPDLOCK	GPIO D Lock Configuration Register (GPIO96 to 127)	Section 6.4.4.68	EALLOW
FE _h	GPDCR	GPIO D Lock Commit Register (GPIO96 to 127)	Section 6.4.4.69	EALLOW
100h	GPECTRL	GPIO E Qualification Sampling Period Control (GPIO128 to 159)	Section 6.4.4.70	EALLOW
102h	GPEQSEL1	GPIO E Qualifier Select 1 Register (GPIO128 to 143)	Section 6.4.4.71	EALLOW
104h	GPEQSEL2	GPIO E Qualifier Select 2 Register (GPIO144 to 159)	Section 6.4.4.72	EALLOW
106h	GPEMUX1	GPIO E Mux 1 Register (GPIO128 to 143)	Section 6.4.4.73	EALLOW
108h	GPEMUX2	GPIO E Mux 2 Register (GPIO144 to 159)	Section 6.4.4.74	EALLOW
10Ah	GPEDIR	GPIO E Direction Register (GPIO128 to 159)	Section 6.4.4.75	EALLOW
10Ch	GPEPUD	GPIO E Pull Up Disable Register (GPIO128 to 159)	Section 6.4.4.76	EALLOW
110h	GPEINV	GPIO E Input Polarity Invert Registers (GPIO128 to 159)	Section 6.4.4.77	EALLOW
112h	GPEODR	GPIO E Open Drain Output Register (GPIO128 to GPIO159)	Section 6.4.4.78	EALLOW
120h	GPEGMUX1	GPIO E Peripheral Group Mux (GPIO128 to 143)	Section 6.4.4.79	EALLOW
122h	GPEGMUX2	GPIO E Peripheral Group Mux (GPIO144 to 159)	Section 6.4.4.80	EALLOW
128h	GPECSEL1	GPIO E Core Select Register (GPIO128 to 135)	Section 6.4.4.81	EALLOW
12Ah	GPECSEL2	GPIO E Core Select Register (GPIO136 to 143)	Section 6.4.4.82	EALLOW
12Ch	GPECSEL3	GPIO E Core Select Register (GPIO144 to 151)	Section 6.4.4.83	EALLOW
12Eh	GPECSEL4	GPIO E Core Select Register (GPIO152 to 159)	Section 6.4.4.84	EALLOW
13Ch	GPELOCK	GPIO E Lock Configuration Register (GPIO128 to 159)	Section 6.4.4.85	EALLOW
13Eh	GPECR	GPIO E Lock Commit Register (GPIO128 to 159)	Section 6.4.4.86	EALLOW
140h	GPFCTRL	GPIO F Qualification Sampling Period Control (GPIO160 to 168)	Section 6.4.4.87	EALLOW
142h	GPFQSEL1	GPIO F Qualifier Select 1 Register (GPIO160 to 168)	Section 6.4.4.88	EALLOW
146h	GPFMUX1	GPIO F Mux 1 Register (GPIO160 to 168)	Section 6.4.4.89	EALLOW
14Ah	GPFDIR	GPIO F Direction Register (GPIO160 to 168)	Section 6.4.4.90	EALLOW
14Ch	GPFPUD	GPIO F Pull Up Disable Register (GPIO160 to 168)	Section 6.4.4.91	EALLOW
150h	GPFINV	GPIO F Input Polarity Invert Registers (GPIO160 to 168)	Section 6.4.4.92	EALLOW
152h	GPFODR	GPIO F Open Drain Output Register (GPIO160 to GPIO168)	Section 6.4.4.93	EALLOW

Table 6-64. GPIO_CTRL_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
160h	GPFGMUX1	GPIO F Peripheral Group Mux (GPIO160 to 168)	Section 6.4.4.94	EALLOW
168h	GPFCSEL1	GPIO F Core Select Register (GPIO160 to 167)	Section 6.4.4.95	EALLOW
16Ah	GPFCSEL2	GPIO F Core Select Register (GPIO168)	Section 6.4.4.96	EALLOW
17Ch	GPFLOCK	GPIO F Lock Configuration Register (GPIO160 to 168)	Section 6.4.4.97	EALLOW
17Eh	GPFCR	GPIO F Lock Commit Register (GPIO160 to 168)	Section 6.4.4.98	EALLOW

6.4.4.1 GPACTRL Register (offset = 0h) [reset = 0h]

GPACTRL is shown in [Figure 6-58](#) and described in [Table 6-65](#).

GPIO A Qualification Sampling Period Control (GPIO0 to 31)

Figure 6-58. GPACTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUALPRD3								QUALPRD2								QUALPRD1				QUALPRD0											
R/W-0h								R/W-0h								R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-65. GPACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	QUALPRD3	R/W	0h	Qualification sampling period for GPIO24 to GPIO31: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
23-16	QUALPRD2	R/W	0h	Qualification sampling period for GPIO16 to GPIO23: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
15-8	QUALPRD1	R/W	0h	Qualification sampling period for GPIO8 to GPIO15: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
7-0	QUALPRD0	R/W	0h	Qualification sampling period for GPIO0 to GPIO7: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510

6.4.4.2 GPAQSEL1 Register (offset = 2h) [reset = 0h]

GPAQSEL1 is shown in [Figure 6-59](#) and described in [Table 6-66](#).

GPIO A Qualifier Select 1 Register (GPIO0 to 15)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-59. GPAQSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO15		GPIO14		GPIO13		GPIO12		GPIO11		GPIO10		GPIO9		GPIO8	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO7		GPIO6		GPIO5		GPIO4		GPIO3		GPIO2		GPIO1		GPIO0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-66. GPAQSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO15	R/W	0h	Input qualification type
29-28	GPIO14	R/W	0h	Input qualification type
27-26	GPIO13	R/W	0h	Input qualification type
25-24	GPIO12	R/W	0h	Input qualification type
23-22	GPIO11	R/W	0h	Input qualification type
21-20	GPIO10	R/W	0h	Input qualification type
19-18	GPIO9	R/W	0h	Input qualification type
17-16	GPIO8	R/W	0h	Input qualification type
15-14	GPIO7	R/W	0h	Input qualification type
13-12	GPIO6	R/W	0h	Input qualification type
11-10	GPIO5	R/W	0h	Input qualification type
9-8	GPIO4	R/W	0h	Input qualification type
7-6	GPIO3	R/W	0h	Input qualification type
5-4	GPIO2	R/W	0h	Input qualification type
3-2	GPIO1	R/W	0h	Input qualification type
1-0	GPIO0	R/W	0h	Input qualification type

6.4.4.3 GPAQSEL2 Register (offset = 4h) [reset = 0h]

GPAQSEL2 is shown in [Figure 6-60](#) and described in [Table 6-67](#).

GPIO A Qualifier Select 2 Register (GPIO16 to 31)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-60. GPAQSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-67. GPAQSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO31	R/W	0h	Input qualification type
29-28	GPIO30	R/W	0h	Input qualification type
27-26	GPIO29	R/W	0h	Input qualification type
25-24	GPIO28	R/W	0h	Input qualification type
23-22	GPIO27	R/W	0h	Input qualification type
21-20	GPIO26	R/W	0h	Input qualification type
19-18	GPIO25	R/W	0h	Input qualification type
17-16	GPIO24	R/W	0h	Input qualification type
15-14	GPIO23	R/W	0h	Input qualification type
13-12	GPIO22	R/W	0h	Input qualification type
11-10	GPIO21	R/W	0h	Input qualification type
9-8	GPIO20	R/W	0h	Input qualification type
7-6	GPIO19	R/W	0h	Input qualification type
5-4	GPIO18	R/W	0h	Input qualification type
3-2	GPIO17	R/W	0h	Input qualification type
1-0	GPIO16	R/W	0h	Input qualification type

6.4.4.4 GPAMUX1 Register (offset = 6h) [reset = 0h]

GPAMUX1 is shown in [Figure 6-61](#) and described in [Table 6-68](#).

GPIO A Mux 1 Register (GPIO0 to 15)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-61. GPAMUX1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO15		GPIO14		GPIO13		GPIO12		GPIO11		GPIO10		GPIO9		GPIO8	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO7		GPIO6		GPIO5		GPIO4		GPIO3		GPIO2		GPIO1		GPIO0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-68. GPAMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO15	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO14	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO13	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO12	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO11	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO10	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO9	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO8	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO7	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO6	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO5	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO4	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO3	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO2	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO1	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO0	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.5 GPAMUX2 Register (offset = 8h) [reset = 0h]

GPAMUX2 is shown in [Figure 6-62](#) and described in [Table 6-69](#).

GPIO A Mux 2 Register (GPIO16 to 31)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-62. GPAMUX2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-69. GPAMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO31	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO30	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO29	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO28	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO27	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO26	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO25	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO24	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO23	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO22	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO21	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO20	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO19	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO18	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO17	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO16	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.6 GPADIR Register (offset = Ah) [reset = 0h]

GPADIR is shown in [Figure 6-63](#) and described in [Table 6-70](#).

GPIO A Direction Register (GPIO0 to 31)

Controls direction of GPIO pins when the specified pin is configured in GPIO mode.

0: Configures pin as input.

1: Configures pin as output.

Reading the register returns the current value of the register setting.

Figure 6-63. GPADIR Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-70. GPADIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Defines direction for this pin in GPIO mode
30	GPIO30	R/W	0h	Defines direction for this pin in GPIO mode
29	GPIO29	R/W	0h	Defines direction for this pin in GPIO mode
28	GPIO28	R/W	0h	Defines direction for this pin in GPIO mode
27	GPIO27	R/W	0h	Defines direction for this pin in GPIO mode
26	GPIO26	R/W	0h	Defines direction for this pin in GPIO mode
25	GPIO25	R/W	0h	Defines direction for this pin in GPIO mode
24	GPIO24	R/W	0h	Defines direction for this pin in GPIO mode
23	GPIO23	R/W	0h	Defines direction for this pin in GPIO mode
22	GPIO22	R/W	0h	Defines direction for this pin in GPIO mode
21	GPIO21	R/W	0h	Defines direction for this pin in GPIO mode
20	GPIO20	R/W	0h	Defines direction for this pin in GPIO mode
19	GPIO19	R/W	0h	Defines direction for this pin in GPIO mode
18	GPIO18	R/W	0h	Defines direction for this pin in GPIO mode
17	GPIO17	R/W	0h	Defines direction for this pin in GPIO mode
16	GPIO16	R/W	0h	Defines direction for this pin in GPIO mode
15	GPIO15	R/W	0h	Defines direction for this pin in GPIO mode
14	GPIO14	R/W	0h	Defines direction for this pin in GPIO mode
13	GPIO13	R/W	0h	Defines direction for this pin in GPIO mode
12	GPIO12	R/W	0h	Defines direction for this pin in GPIO mode

Table 6-70. GPADIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO11	R/W	0h	Defines direction for this pin in GPIO mode
10	GPIO10	R/W	0h	Defines direction for this pin in GPIO mode
9	GPIO9	R/W	0h	Defines direction for this pin in GPIO mode
8	GPIO8	R/W	0h	Defines direction for this pin in GPIO mode
7	GPIO7	R/W	0h	Defines direction for this pin in GPIO mode
6	GPIO6	R/W	0h	Defines direction for this pin in GPIO mode
5	GPIO5	R/W	0h	Defines direction for this pin in GPIO mode
4	GPIO4	R/W	0h	Defines direction for this pin in GPIO mode
3	GPIO3	R/W	0h	Defines direction for this pin in GPIO mode
2	GPIO2	R/W	0h	Defines direction for this pin in GPIO mode
1	GPIO1	R/W	0h	Defines direction for this pin in GPIO mode
0	GPIO0	R/W	0h	Defines direction for this pin in GPIO mode

6.4.4.7 GPAPUD Register (offset = Ch) [reset = FFFFFFFFh]

GPAPUD is shown in [Figure 6-64](#) and described in [Table 6-71](#).

GPIO A Pull Up Disable Register (GPIO0 to 31)

Disables the Pull-Up on GPIO.

0: Enables the Pull-Up.

1: Disables the Pull-Up.

Reading the register returns the current value of the register setting.

Note:

[1] The Pull-Ups on the GPIO pins are disabled asynchronously when IORSn signal is low.

Figure 6-64. GPAPUD Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-1h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-1h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-1h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-71. GPAPUD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	1h	Pull-Up Disable control for this pin
30	GPIO30	R/W	1h	Pull-Up Disable control for this pin
29	GPIO29	R/W	1h	Pull-Up Disable control for this pin
28	GPIO28	R/W	1h	Pull-Up Disable control for this pin
27	GPIO27	R/W	1h	Pull-Up Disable control for this pin
26	GPIO26	R/W	1h	Pull-Up Disable control for this pin
25	GPIO25	R/W	1h	Pull-Up Disable control for this pin
24	GPIO24	R/W	1h	Pull-Up Disable control for this pin
23	GPIO23	R/W	1h	Pull-Up Disable control for this pin
22	GPIO22	R/W	1h	Pull-Up Disable control for this pin
21	GPIO21	R/W	1h	Pull-Up Disable control for this pin
20	GPIO20	R/W	1h	Pull-Up Disable control for this pin
19	GPIO19	R/W	1h	Pull-Up Disable control for this pin
18	GPIO18	R/W	1h	Pull-Up Disable control for this pin
17	GPIO17	R/W	1h	Pull-Up Disable control for this pin
16	GPIO16	R/W	1h	Pull-Up Disable control for this pin
15	GPIO15	R/W	1h	Pull-Up Disable control for this pin
14	GPIO14	R/W	1h	Pull-Up Disable control for this pin
13	GPIO13	R/W	1h	Pull-Up Disable control for this pin

Table 6-71. GPAPUD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	GPIO12	R/W	1h	Pull-Up Disable control for this pin
11	GPIO11	R/W	1h	Pull-Up Disable control for this pin
10	GPIO10	R/W	1h	Pull-Up Disable control for this pin
9	GPIO9	R/W	1h	Pull-Up Disable control for this pin
8	GPIO8	R/W	1h	Pull-Up Disable control for this pin
7	GPIO7	R/W	1h	Pull-Up Disable control for this pin
6	GPIO6	R/W	1h	Pull-Up Disable control for this pin
5	GPIO5	R/W	1h	Pull-Up Disable control for this pin
4	GPIO4	R/W	1h	Pull-Up Disable control for this pin
3	GPIO3	R/W	1h	Pull-Up Disable control for this pin
2	GPIO2	R/W	1h	Pull-Up Disable control for this pin
1	GPIO1	R/W	1h	Pull-Up Disable control for this pin
0	GPIO0	R/W	1h	Pull-Up Disable control for this pin

6.4.4.8 GPAINV Register (offset = 10h) [reset = 0h]

GPAINV is shown in [Figure 6-65](#) and described in [Table 6-72](#).

GPIO A Input Polarity Invert Registers (GPIO0 to 31)

Selects between non-inverted and inverted GPIO input to the device.

0: selects non-inverted GPIO input

1: selects inverted GPIO input

Reading the register returns the current value of the register setting.

Figure 6-65. GPAINV Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-72. GPAINV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Input inversion control for this pin
30	GPIO30	R/W	0h	Input inversion control for this pin
29	GPIO29	R/W	0h	Input inversion control for this pin
28	GPIO28	R/W	0h	Input inversion control for this pin
27	GPIO27	R/W	0h	Input inversion control for this pin
26	GPIO26	R/W	0h	Input inversion control for this pin
25	GPIO25	R/W	0h	Input inversion control for this pin
24	GPIO24	R/W	0h	Input inversion control for this pin
23	GPIO23	R/W	0h	Input inversion control for this pin
22	GPIO22	R/W	0h	Input inversion control for this pin
21	GPIO21	R/W	0h	Input inversion control for this pin
20	GPIO20	R/W	0h	Input inversion control for this pin
19	GPIO19	R/W	0h	Input inversion control for this pin
18	GPIO18	R/W	0h	Input inversion control for this pin
17	GPIO17	R/W	0h	Input inversion control for this pin
16	GPIO16	R/W	0h	Input inversion control for this pin
15	GPIO15	R/W	0h	Input inversion control for this pin
14	GPIO14	R/W	0h	Input inversion control for this pin
13	GPIO13	R/W	0h	Input inversion control for this pin
12	GPIO12	R/W	0h	Input inversion control for this pin

Table 6-72. GPAINV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO11	R/W	0h	Input inversion control for this pin
10	GPIO10	R/W	0h	Input inversion control for this pin
9	GPIO9	R/W	0h	Input inversion control for this pin
8	GPIO8	R/W	0h	Input inversion control for this pin
7	GPIO7	R/W	0h	Input inversion control for this pin
6	GPIO6	R/W	0h	Input inversion control for this pin
5	GPIO5	R/W	0h	Input inversion control for this pin
4	GPIO4	R/W	0h	Input inversion control for this pin
3	GPIO3	R/W	0h	Input inversion control for this pin
2	GPIO2	R/W	0h	Input inversion control for this pin
1	GPIO1	R/W	0h	Input inversion control for this pin
0	GPIO0	R/W	0h	Input inversion control for this pin

6.4.4.9 GPAODR Register (offset = 12h) [reset = 0h]

GPAODR is shown in [Figure 6-66](#) and described in [Table 6-73](#).

GPIO A Open Drain Output Register (GPIO0 to GPIO31)

Selects between normal and open-drain output for the GPIO pin.

0: Normal Output

1: Open Drain Output

Reading the register returns the current value of the register setting.

Note:

[1] In the Open Drain output mode, if the buffer is configured for output mode, a 0 value to be driven out comes out on the on the PAD while a 1 value to be driven out tri-states the buffer.

Figure 6-66. GPAODR Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-73. GPAODR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Output Open-Drain control for this pin
30	GPIO30	R/W	0h	Output Open-Drain control for this pin
29	GPIO29	R/W	0h	Output Open-Drain control for this pin
28	GPIO28	R/W	0h	Output Open-Drain control for this pin
27	GPIO27	R/W	0h	Output Open-Drain control for this pin
26	GPIO26	R/W	0h	Output Open-Drain control for this pin
25	GPIO25	R/W	0h	Output Open-Drain control for this pin
24	GPIO24	R/W	0h	Output Open-Drain control for this pin
23	GPIO23	R/W	0h	Output Open-Drain control for this pin
22	GPIO22	R/W	0h	Output Open-Drain control for this pin
21	GPIO21	R/W	0h	Output Open-Drain control for this pin
20	GPIO20	R/W	0h	Output Open-Drain control for this pin
19	GPIO19	R/W	0h	Output Open-Drain control for this pin
18	GPIO18	R/W	0h	Output Open-Drain control for this pin
17	GPIO17	R/W	0h	Output Open-Drain control for this pin
16	GPIO16	R/W	0h	Output Open-Drain control for this pin
15	GPIO15	R/W	0h	Output Open-Drain control for this pin
14	GPIO14	R/W	0h	Output Open-Drain control for this pin

Table 6-73. GPAODR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO13	R/W	0h	Output Open-Drain control for this pin
12	GPIO12	R/W	0h	Output Open-Drain control for this pin
11	GPIO11	R/W	0h	Output Open-Drain control for this pin
10	GPIO10	R/W	0h	Output Open-Drain control for this pin
9	GPIO9	R/W	0h	Output Open-Drain control for this pin
8	GPIO8	R/W	0h	Output Open-Drain control for this pin
7	GPIO7	R/W	0h	Output Open-Drain control for this pin
6	GPIO6	R/W	0h	Output Open-Drain control for this pin
5	GPIO5	R/W	0h	Output Open-Drain control for this pin
4	GPIO4	R/W	0h	Output Open-Drain control for this pin
3	GPIO3	R/W	0h	Output Open-Drain control for this pin
2	GPIO2	R/W	0h	Output Open-Drain control for this pin
1	GPIO1	R/W	0h	Output Open-Drain control for this pin
0	GPIO0	R/W	0h	Output Open-Drain control for this pin

6.4.4.10 GPAGMUX1 Register (offset = 20h) [reset = 0h]

GPAGMUX1 is shown in [Figure 6-67](#) and described in [Table 6-74](#).

GPIO A Peripheral Group Mux (GPIO0 to 15)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-67. GPAGMUX1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO15		GPIO14		GPIO13		GPIO12		GPIO11		GPIO10		GPIO9		GPIO8	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO7		GPIO6		GPIO5		GPIO4		GPIO3		GPIO2		GPIO1		GPIO0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-74. GPAGMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO15	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO14	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO13	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO12	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO11	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO10	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO9	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO8	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO7	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO6	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO5	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO4	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO3	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO2	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO1	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO0	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.11 GPAGMUX2 Register (offset = 22h) [reset = 0h]

GPAGMUX2 is shown in [Figure 6-68](#) and described in [Table 6-75](#).

GPIO A Peripheral Group Mux (GPIO16 to 31)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-68. GPAGMUX2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-75. GPAGMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO31	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO30	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO29	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO28	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO27	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO26	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO25	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO24	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO23	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO22	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO21	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO20	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO19	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO18	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO17	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO16	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.12 GPACSEL1 Register (offset = 28h) [reset = 0h]

GPACSEL1 is shown in [Figure 6-69](#) and described in [Table 6-76](#).

GPIO A Core Select Register (GPIO0 to 7)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-69. GPACSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO7				GPIO6				GPIO5				GPIO4			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO3				GPIO2				GPIO1				GPIO0			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-76. GPACSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO7	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO6	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO5	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO4	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO3	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO2	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO1	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO0	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.13 GPACSEL2 Register (offset = 2Ah) [reset = 0h]

GPACSEL2 is shown in [Figure 6-70](#) and described in [Table 6-77](#).

GPIO A Core Select Register (GPIO8 to 15)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-70. GPACSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO15				GPIO14				GPIO13				GPIO12			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO11				GPIO10				GPIO9				GPIO8			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-77. GPACSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO15	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO14	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO13	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO12	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO11	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO10	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO9	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO8	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.14 GPACSEL3 Register (offset = 2Ch) [reset = 0h]

GPACSEL3 is shown in [Figure 6-71](#) and described in [Table 6-78](#).

GPIO A Core Select Register (GPIO16 to 23)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-71. GPACSEL3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO23				GPIO22				GPIO21				GPIO20			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO19				GPIO18				GPIO17				GPIO16			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-78. GPACSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO23	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO22	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO21	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO20	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO19	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO18	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO17	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO16	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.15 GPACSEL4 Register (offset = 2Eh) [reset = 0h]

GPACSEL4 is shown in [Figure 6-72](#) and described in [Table 6-79](#).

GPIO A Core Select Register (GPIO24 to 31)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-72. GPACSEL4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO31				GPIO30				GPIO29				GPIO28			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO27				GPIO26				GPIO25				GPIO24			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-79. GPACSEL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO31	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO30	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO29	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO28	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO27	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO26	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO25	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO24	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.16 GPALOCK Register (offset = 3Ch) [reset = 0h]

GPALOCK is shown in [Figure 6-73](#) and described in [Table 6-80](#).

GPIO A Lock Configuration Register (GPIO0 to 31)

GPIO Configuration Lock for GPIO.

0: Bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx register which control the same pin can be changed

1: Locks changes to the bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx registers which control the same pin

Figure 6-73. GPALOCK Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-80. GPALOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Configuration Lock bit for this pin
30	GPIO30	R/W	0h	Configuration Lock bit for this pin
29	GPIO29	R/W	0h	Configuration Lock bit for this pin
28	GPIO28	R/W	0h	Configuration Lock bit for this pin
27	GPIO27	R/W	0h	Configuration Lock bit for this pin
26	GPIO26	R/W	0h	Configuration Lock bit for this pin
25	GPIO25	R/W	0h	Configuration Lock bit for this pin
24	GPIO24	R/W	0h	Configuration Lock bit for this pin
23	GPIO23	R/W	0h	Configuration Lock bit for this pin
22	GPIO22	R/W	0h	Configuration Lock bit for this pin
21	GPIO21	R/W	0h	Configuration Lock bit for this pin
20	GPIO20	R/W	0h	Configuration Lock bit for this pin
19	GPIO19	R/W	0h	Configuration Lock bit for this pin
18	GPIO18	R/W	0h	Configuration Lock bit for this pin
17	GPIO17	R/W	0h	Configuration Lock bit for this pin
16	GPIO16	R/W	0h	Configuration Lock bit for this pin
15	GPIO15	R/W	0h	Configuration Lock bit for this pin
14	GPIO14	R/W	0h	Configuration Lock bit for this pin
13	GPIO13	R/W	0h	Configuration Lock bit for this pin
12	GPIO12	R/W	0h	Configuration Lock bit for this pin

Table 6-80. GPALOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO11	R/W	0h	Configuration Lock bit for this pin
10	GPIO10	R/W	0h	Configuration Lock bit for this pin
9	GPIO9	R/W	0h	Configuration Lock bit for this pin
8	GPIO8	R/W	0h	Configuration Lock bit for this pin
7	GPIO7	R/W	0h	Configuration Lock bit for this pin
6	GPIO6	R/W	0h	Configuration Lock bit for this pin
5	GPIO5	R/W	0h	Configuration Lock bit for this pin
4	GPIO4	R/W	0h	Configuration Lock bit for this pin
3	GPIO3	R/W	0h	Configuration Lock bit for this pin
2	GPIO2	R/W	0h	Configuration Lock bit for this pin
1	GPIO1	R/W	0h	Configuration Lock bit for this pin
0	GPIO0	R/W	0h	Configuration Lock bit for this pin

6.4.4.17 GPACR Register (offset = 3Eh) [reset = 0h]

GPACR is shown in [Figure 6-74](#) and described in [Table 6-81](#).

GPIO A Lock Commit Register (GPIO0 to 31)

GPIO Configuration Lock Commit for GPIO:

1: Locks changes to the bit in GPyLOCK register which controls the same pin

0: Bit in the GPyLOCK register which controls the same pin can be changed

Figure 6-74. GPACR Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-81. GPACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Configuration lock commit bit for this pin
30	GPIO30	R/W	0h	Configuration lock commit bit for this pin
29	GPIO29	R/W	0h	Configuration lock commit bit for this pin
28	GPIO28	R/W	0h	Configuration lock commit bit for this pin
27	GPIO27	R/W	0h	Configuration lock commit bit for this pin
26	GPIO26	R/W	0h	Configuration lock commit bit for this pin
25	GPIO25	R/W	0h	Configuration lock commit bit for this pin
24	GPIO24	R/W	0h	Configuration lock commit bit for this pin
23	GPIO23	R/W	0h	Configuration lock commit bit for this pin
22	GPIO22	R/W	0h	Configuration lock commit bit for this pin
21	GPIO21	R/W	0h	Configuration lock commit bit for this pin
20	GPIO20	R/W	0h	Configuration lock commit bit for this pin
19	GPIO19	R/W	0h	Configuration lock commit bit for this pin
18	GPIO18	R/W	0h	Configuration lock commit bit for this pin
17	GPIO17	R/W	0h	Configuration lock commit bit for this pin
16	GPIO16	R/W	0h	Configuration lock commit bit for this pin
15	GPIO15	R/W	0h	Configuration lock commit bit for this pin
14	GPIO14	R/W	0h	Configuration lock commit bit for this pin
13	GPIO13	R/W	0h	Configuration lock commit bit for this pin
12	GPIO12	R/W	0h	Configuration lock commit bit for this pin
11	GPIO11	R/W	0h	Configuration lock commit bit for this pin

Table 6-81. GPACR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO10	R/W	0h	Configuration lock commit bit for this pin
9	GPIO9	R/W	0h	Configuration lock commit bit for this pin
8	GPIO8	R/W	0h	Configuration lock commit bit for this pin
7	GPIO7	R/W	0h	Configuration lock commit bit for this pin
6	GPIO6	R/W	0h	Configuration lock commit bit for this pin
5	GPIO5	R/W	0h	Configuration lock commit bit for this pin
4	GPIO4	R/W	0h	Configuration lock commit bit for this pin
3	GPIO3	R/W	0h	Configuration lock commit bit for this pin
2	GPIO2	R/W	0h	Configuration lock commit bit for this pin
1	GPIO1	R/W	0h	Configuration lock commit bit for this pin
0	GPIO0	R/W	0h	Configuration lock commit bit for this pin

6.4.4.18 GPBCTRL Register (offset = 40h) [reset = 0h]

GPBCTRL is shown in [Figure 6-75](#) and described in [Table 6-82](#).

GPIO B Qualification Sampling Period Control (GPIO32 to 63)

Figure 6-75. GPBCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUALPRD3								QUALPRD2								QUALPRD1				QUALPRD0											
R/W-0h								R/W-0h								R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-82. GPBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	QUALPRD3	R/W	0h	Qualification sampling period for GPIO56 to GPIO63: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
23-16	QUALPRD2	R/W	0h	Qualification sampling period for GPIO48 to GPIO55: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
15-8	QUALPRD1	R/W	0h	Qualification sampling period for GPIO40 to GPIO47: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
7-0	QUALPRD0	R/W	0h	Qualification sampling period for GPIO32 to GPIO39: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510

6.4.4.19 GPBQSEL1 Register (offset = 42h) [reset = 0h]

GPBQSEL1 is shown in [Figure 6-76](#) and described in [Table 6-83](#).

GPIO B Qualifier Select 1 Register (GPIO32 to 47)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-76. GPBQSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-83. GPBQSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO47	R/W	0h	Input qualification type
29-28	GPIO46	R/W	0h	Input qualification type
27-26	GPIO45	R/W	0h	Input qualification type
25-24	GPIO44	R/W	0h	Input qualification type
23-22	GPIO43	R/W	0h	Input qualification type
21-20	GPIO42	R/W	0h	Input qualification type
19-18	GPIO41	R/W	0h	Input qualification type
17-16	GPIO40	R/W	0h	Input qualification type
15-14	GPIO39	R/W	0h	Input qualification type
13-12	GPIO38	R/W	0h	Input qualification type
11-10	GPIO37	R/W	0h	Input qualification type
9-8	GPIO36	R/W	0h	Input qualification type
7-6	GPIO35	R/W	0h	Input qualification type
5-4	GPIO34	R/W	0h	Input qualification type
3-2	GPIO33	R/W	0h	Input qualification type
1-0	GPIO32	R/W	0h	Input qualification type

6.4.4.20 GPBQSEL2 Register (offset = 44h) [reset = 0h]

GPBQSEL2 is shown in [Figure 6-77](#) and described in [Table 6-84](#).

GPIO B Qualifier Select 2 Register (GPIO48 to 63)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-77. GPBQSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO63		GPIO62		GPIO61		GPIO60		GPIO59		GPIO58		GPIO57		GPIO56	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO55		GPIO54		GPIO53		GPIO52		GPIO51		GPIO50		GPIO49		GPIO48	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-84. GPBQSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO63	R/W	0h	Input qualification type
29-28	GPIO62	R/W	0h	Input qualification type
27-26	GPIO61	R/W	0h	Input qualification type
25-24	GPIO60	R/W	0h	Input qualification type
23-22	GPIO59	R/W	0h	Input qualification type
21-20	GPIO58	R/W	0h	Input qualification type
19-18	GPIO57	R/W	0h	Input qualification type
17-16	GPIO56	R/W	0h	Input qualification type
15-14	GPIO55	R/W	0h	Input qualification type
13-12	GPIO54	R/W	0h	Input qualification type
11-10	GPIO53	R/W	0h	Input qualification type
9-8	GPIO52	R/W	0h	Input qualification type
7-6	GPIO51	R/W	0h	Input qualification type
5-4	GPIO50	R/W	0h	Input qualification type
3-2	GPIO49	R/W	0h	Input qualification type
1-0	GPIO48	R/W	0h	Input qualification type

6.4.4.21 GPBMUX1 Register (offset = 46h) [reset = 0h]

GPBMUX1 is shown in [Figure 6-78](#) and described in [Table 6-85](#).

GPIO B Mux 1 Register (GPIO32 to 47)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-78. GPBMUX1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-85. GPBMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO47	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO46	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO45	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO44	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO43	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO42	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO41	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO40	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO39	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO38	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO37	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO36	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO35	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO34	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO33	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO32	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.22 GPBMUX2 Register (offset = 48h) [reset = 0h]

GPBMUX2 is shown in [Figure 6-79](#) and described in [Table 6-86](#).

GPIO B Mux 2 Register (GPIO48 to 63)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-79. GPBMUX2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-86. GPBMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO63	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO62	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO61	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO60	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO59	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO58	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO57	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO56	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO55	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO54	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO53	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO52	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO51	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO50	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO49	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO48	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.23 GPBDIR Register (offset = 4Ah) [reset = 0h]

GPBDIR is shown in [Figure 6-80](#) and described in [Table 6-87](#).

GPIO B Direction Register (GPIO32 to 63)

Controls direction of GPIO pins when the specified pin is configured in GPIO mode.

0: Configures pin as input.

1: Configures pin as output.

Reading the register returns the current value of the register setting.

Figure 6-80. GPBDIR Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-87. GPBDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Defines direction for this pin in GPIO mode
30	GPIO62	R/W	0h	Defines direction for this pin in GPIO mode
29	GPIO61	R/W	0h	Defines direction for this pin in GPIO mode
28	GPIO60	R/W	0h	Defines direction for this pin in GPIO mode
27	GPIO59	R/W	0h	Defines direction for this pin in GPIO mode
26	GPIO58	R/W	0h	Defines direction for this pin in GPIO mode
25	GPIO57	R/W	0h	Defines direction for this pin in GPIO mode
24	GPIO56	R/W	0h	Defines direction for this pin in GPIO mode
23	GPIO55	R/W	0h	Defines direction for this pin in GPIO mode
22	GPIO54	R/W	0h	Defines direction for this pin in GPIO mode
21	GPIO53	R/W	0h	Defines direction for this pin in GPIO mode
20	GPIO52	R/W	0h	Defines direction for this pin in GPIO mode
19	GPIO51	R/W	0h	Defines direction for this pin in GPIO mode
18	GPIO50	R/W	0h	Defines direction for this pin in GPIO mode
17	GPIO49	R/W	0h	Defines direction for this pin in GPIO mode
16	GPIO48	R/W	0h	Defines direction for this pin in GPIO mode
15	GPIO47	R/W	0h	Defines direction for this pin in GPIO mode
14	GPIO46	R/W	0h	Defines direction for this pin in GPIO mode
13	GPIO45	R/W	0h	Defines direction for this pin in GPIO mode
12	GPIO44	R/W	0h	Defines direction for this pin in GPIO mode

Table 6-87. GPBDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO43	R/W	0h	Defines direction for this pin in GPIO mode
10	GPIO42	R/W	0h	Defines direction for this pin in GPIO mode
9	GPIO41	R/W	0h	Defines direction for this pin in GPIO mode
8	GPIO40	R/W	0h	Defines direction for this pin in GPIO mode
7	GPIO39	R/W	0h	Defines direction for this pin in GPIO mode
6	GPIO38	R/W	0h	Defines direction for this pin in GPIO mode
5	GPIO37	R/W	0h	Defines direction for this pin in GPIO mode
4	GPIO36	R/W	0h	Defines direction for this pin in GPIO mode
3	GPIO35	R/W	0h	Defines direction for this pin in GPIO mode
2	GPIO34	R/W	0h	Defines direction for this pin in GPIO mode
1	GPIO33	R/W	0h	Defines direction for this pin in GPIO mode
0	GPIO32	R/W	0h	Defines direction for this pin in GPIO mode

6.4.4.24 GPBPUD Register (offset = 4Ch) [reset = FFFFFFFFh]

GPBPUD is shown in [Figure 6-81](#) and described in [Table 6-88](#).

GPIO B Pull Up Disable Register (GPIO32 to 63)

Disables the Pull-Up on GPIO.

0: Enables the Pull-Up.

1: Disables the Pull-Up.

Reading the register returns the current value of the register setting.

Note:

[1] The Pull-Ups on the GPIO pins are disabled asynchronously when IORSn signal is low.

Figure 6-81. GPBPUD Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-1h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-1h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-1h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-88. GPBPUD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	1h	Pull-Up Disable control for this pin
30	GPIO62	R/W	1h	Pull-Up Disable control for this pin
29	GPIO61	R/W	1h	Pull-Up Disable control for this pin
28	GPIO60	R/W	1h	Pull-Up Disable control for this pin
27	GPIO59	R/W	1h	Pull-Up Disable control for this pin
26	GPIO58	R/W	1h	Pull-Up Disable control for this pin
25	GPIO57	R/W	1h	Pull-Up Disable control for this pin
24	GPIO56	R/W	1h	Pull-Up Disable control for this pin
23	GPIO55	R/W	1h	Pull-Up Disable control for this pin
22	GPIO54	R/W	1h	Pull-Up Disable control for this pin
21	GPIO53	R/W	1h	Pull-Up Disable control for this pin
20	GPIO52	R/W	1h	Pull-Up Disable control for this pin
19	GPIO51	R/W	1h	Pull-Up Disable control for this pin
18	GPIO50	R/W	1h	Pull-Up Disable control for this pin
17	GPIO49	R/W	1h	Pull-Up Disable control for this pin
16	GPIO48	R/W	1h	Pull-Up Disable control for this pin
15	GPIO47	R/W	1h	Pull-Up Disable control for this pin
14	GPIO46	R/W	1h	Pull-Up Disable control for this pin
13	GPIO45	R/W	1h	Pull-Up Disable control for this pin

Table 6-88. GPBPUD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	GPIO44	R/W	1h	Pull-Up Disable control for this pin
11	GPIO43	R/W	1h	Pull-Up Disable control for this pin
10	GPIO42	R/W	1h	Pull-Up Disable control for this pin
9	GPIO41	R/W	1h	Pull-Up Disable control for this pin
8	GPIO40	R/W	1h	Pull-Up Disable control for this pin
7	GPIO39	R/W	1h	Pull-Up Disable control for this pin
6	GPIO38	R/W	1h	Pull-Up Disable control for this pin
5	GPIO37	R/W	1h	Pull-Up Disable control for this pin
4	GPIO36	R/W	1h	Pull-Up Disable control for this pin
3	GPIO35	R/W	1h	Pull-Up Disable control for this pin
2	GPIO34	R/W	1h	Pull-Up Disable control for this pin
1	GPIO33	R/W	1h	Pull-Up Disable control for this pin
0	GPIO32	R/W	1h	Pull-Up Disable control for this pin

6.4.4.25 GPBINV Register (offset = 50h) [reset = 0h]

GPBINV is shown in [Figure 6-82](#) and described in [Table 6-89](#).

GPIO B Input Polarity Invert Registers (GPIO32 to 63)

Selects between non-inverted and inverted GPIO input to the device.

0: selects non-inverted GPIO input

1: selects inverted GPIO input

Reading the register returns the current value of the register setting.

Figure 6-82. GPBINV Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-89. GPBINV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Input inversion control for this pin
30	GPIO62	R/W	0h	Input inversion control for this pin
29	GPIO61	R/W	0h	Input inversion control for this pin
28	GPIO60	R/W	0h	Input inversion control for this pin
27	GPIO59	R/W	0h	Input inversion control for this pin
26	GPIO58	R/W	0h	Input inversion control for this pin
25	GPIO57	R/W	0h	Input inversion control for this pin
24	GPIO56	R/W	0h	Input inversion control for this pin
23	GPIO55	R/W	0h	Input inversion control for this pin
22	GPIO54	R/W	0h	Input inversion control for this pin
21	GPIO53	R/W	0h	Input inversion control for this pin
20	GPIO52	R/W	0h	Input inversion control for this pin
19	GPIO51	R/W	0h	Input inversion control for this pin
18	GPIO50	R/W	0h	Input inversion control for this pin
17	GPIO49	R/W	0h	Input inversion control for this pin
16	GPIO48	R/W	0h	Input inversion control for this pin
15	GPIO47	R/W	0h	Input inversion control for this pin
14	GPIO46	R/W	0h	Input inversion control for this pin
13	GPIO45	R/W	0h	Input inversion control for this pin
12	GPIO44	R/W	0h	Input inversion control for this pin

Table 6-89. GPBINV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO43	R/W	0h	Input inversion control for this pin
10	GPIO42	R/W	0h	Input inversion control for this pin
9	GPIO41	R/W	0h	Input inversion control for this pin
8	GPIO40	R/W	0h	Input inversion control for this pin
7	GPIO39	R/W	0h	Input inversion control for this pin
6	GPIO38	R/W	0h	Input inversion control for this pin
5	GPIO37	R/W	0h	Input inversion control for this pin
4	GPIO36	R/W	0h	Input inversion control for this pin
3	GPIO35	R/W	0h	Input inversion control for this pin
2	GPIO34	R/W	0h	Input inversion control for this pin
1	GPIO33	R/W	0h	Input inversion control for this pin
0	GPIO32	R/W	0h	Input inversion control for this pin

6.4.4.26 GPBODR Register (offset = 52h) [reset = 0h]

GPBODR is shown in [Figure 6-83](#) and described in [Table 6-90](#).

GPIO B Open Drain Output Register (GPIO32 to GPIO63)

Selects between normal and open-drain output for the GPIO pin.

0: Normal Output

1: Open Drain Output

Reading the register returns the current value of the register setting.

Note:

[1] In the Open Drain output mode, if the buffer is configured for output mode, a 0 value to be driven out comes out on the on the PAD while a 1 value to be driven out tri-states the buffer.

Figure 6-83. GPBODR Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-90. GPBODR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Output Open-Drain control for this pin
30	GPIO62	R/W	0h	Output Open-Drain control for this pin
29	GPIO61	R/W	0h	Output Open-Drain control for this pin
28	GPIO60	R/W	0h	Output Open-Drain control for this pin
27	GPIO59	R/W	0h	Output Open-Drain control for this pin
26	GPIO58	R/W	0h	Output Open-Drain control for this pin
25	GPIO57	R/W	0h	Output Open-Drain control for this pin
24	GPIO56	R/W	0h	Output Open-Drain control for this pin
23	GPIO55	R/W	0h	Output Open-Drain control for this pin
22	GPIO54	R/W	0h	Output Open-Drain control for this pin
21	GPIO53	R/W	0h	Output Open-Drain control for this pin
20	GPIO52	R/W	0h	Output Open-Drain control for this pin
19	GPIO51	R/W	0h	Output Open-Drain control for this pin
18	GPIO50	R/W	0h	Output Open-Drain control for this pin
17	GPIO49	R/W	0h	Output Open-Drain control for this pin
16	GPIO48	R/W	0h	Output Open-Drain control for this pin
15	GPIO47	R/W	0h	Output Open-Drain control for this pin
14	GPIO46	R/W	0h	Output Open-Drain control for this pin

Table 6-90. GPBODR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO45	R/W	0h	Output Open-Drain control for this pin
12	GPIO44	R/W	0h	Output Open-Drain control for this pin
11	GPIO43	R/W	0h	Output Open-Drain control for this pin
10	GPIO42	R/W	0h	Output Open-Drain control for this pin
9	GPIO41	R/W	0h	Output Open-Drain control for this pin
8	GPIO40	R/W	0h	Output Open-Drain control for this pin
7	GPIO39	R/W	0h	Output Open-Drain control for this pin
6	GPIO38	R/W	0h	Output Open-Drain control for this pin
5	GPIO37	R/W	0h	Output Open-Drain control for this pin
4	GPIO36	R/W	0h	Output Open-Drain control for this pin
3	GPIO35	R/W	0h	Output Open-Drain control for this pin
2	GPIO34	R/W	0h	Output Open-Drain control for this pin
1	GPIO33	R/W	0h	Output Open-Drain control for this pin
0	GPIO32	R/W	0h	Output Open-Drain control for this pin

6.4.4.27 GPBAMSEL Register (offset = 54h) [reset = 0h]

GPBAMSEL is shown in [Figure 6-84](#) and described in [Table 6-91](#).

GPIO B Analog Mode Select register (GPIO32 to GPIO63)

Selects between digital and analog functionality for GPIO0 pins.

0: The analog function of the pin is disabled and the pin is capable of digital functions as specified by the other GPIO configuration registers

1: The analog function of the pin is enabled and the pin is capable of analog functions

Reading the register returns the current value of the register setting.

Note:

[1] This register and bits are only valid for GPIO signals that share analog function through a unified I/O pad. For all the IOs, t

Figure 6-84. GPBAMSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	RESERVED	RESERVED	GPIO43	GPIO42	RESERVED	RESERVED
R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-91. GPBAMSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	GPIO47	R/W	0h	Analog Mode select for this pin
14	GPIO46	R/W	0h	Analog Mode select for this pin
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved

Table 6-91. GPBAMSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO43	R/W	0h	Analog Mode select for this pin
10	GPIO42	R/W	0h	Analog Mode select for this pin
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

6.4.4.28 GPBGMUX1 Register (offset = 60h) [reset = 0h]

GPBGMUX1 is shown in [Figure 6-85](#) and described in [Table 6-92](#).

GPIO B Peripheral Group Mux (GPIO32 to 47)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-85. GPBGMUX1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-92. GPBGMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO47	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO46	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO45	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO44	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO43	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO42	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO41	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO40	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO39	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO38	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO37	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO36	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO35	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO34	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO33	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO32	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.29 GPBGMUX2 Register (offset = 62h) [reset = 0h]

GPBGMUX2 is shown in [Figure 6-86](#) and described in [Table 6-93](#).

GPIO B Peripheral Group Mux (GPIO48 to 63)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-86. GPBGMUX2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-93. GPBGMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO63	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO62	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO61	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO60	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO59	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO58	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO57	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO56	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO55	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO54	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO53	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO52	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO51	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO50	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO49	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO48	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.30 GPBCSEL1 Register (offset = 68h) [reset = 0h]

GPBCSEL1 is shown in [Figure 6-87](#) and described in [Table 6-94](#).

GPIO B Core Select Register (GPIO32 to 39)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-87. GPBCSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO39				GPIO38				GPIO37				GPIO36			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO35				GPIO34				GPIO33				GPIO32			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-94. GPBCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO39	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO38	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO37	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO36	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO35	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO34	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO33	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO32	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.31 GPBCSEL2 Register (offset = 6Ah) [reset = 0h]

GPBCSEL2 is shown in [Figure 6-88](#) and described in [Table 6-95](#).

GPIO B Core Select Register (GPIO40 to 47)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-88. GPBCSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO47				GPIO46				GPIO45				GPIO44			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO43				GPIO42				GPIO41				GPIO40			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-95. GPBCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO47	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO46	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO45	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO44	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO43	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO42	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO41	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO40	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.32 GPBCSEL3 Register (offset = 6Ch) [reset = 0h]

GPBCSEL3 is shown in [Figure 6-89](#) and described in [Table 6-96](#).

GPIO B Core Select Register (GPIO48 to 55)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-89. GPBCSEL3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO55				GPIO54				GPIO53				GPIO52			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO51				GPIO50				GPIO49				GPIO48			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-96. GPBCSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO55	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO54	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO53	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO52	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO51	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO50	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO49	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO48	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.33 GPBCSEL4 Register (offset = 6Eh) [reset = 0h]

GPBCSEL4 is shown in [Figure 6-90](#) and described in [Table 6-97](#).

GPIO B Core Select Register (GPIO56 to 63)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-90. GPBCSEL4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO63				GPIO62				GPIO61				GPIO60			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO59				GPIO58				GPIO57				GPIO56			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-97. GPBCSEL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO63	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO62	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO61	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO60	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO59	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO58	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO57	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO56	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.34 GPBLOCK Register (offset = 7Ch) [reset = 0h]

GPBLOCK is shown in [Figure 6-91](#) and described in [Table 6-98](#).

GPIO B Lock Configuration Register (GPIO32 to 63)

GPIO Configuration Lock for GPIO.

0: Bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx register which control the same pin can be changed

1: Locks changes to the bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx registers which control the same pin

Figure 6-91. GPBLOCK Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-98. GPBLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Configuration Lock bit for this pin
30	GPIO62	R/W	0h	Configuration Lock bit for this pin
29	GPIO61	R/W	0h	Configuration Lock bit for this pin
28	GPIO60	R/W	0h	Configuration Lock bit for this pin
27	GPIO59	R/W	0h	Configuration Lock bit for this pin
26	GPIO58	R/W	0h	Configuration Lock bit for this pin
25	GPIO57	R/W	0h	Configuration Lock bit for this pin
24	GPIO56	R/W	0h	Configuration Lock bit for this pin
23	GPIO55	R/W	0h	Configuration Lock bit for this pin
22	GPIO54	R/W	0h	Configuration Lock bit for this pin
21	GPIO53	R/W	0h	Configuration Lock bit for this pin
20	GPIO52	R/W	0h	Configuration Lock bit for this pin
19	GPIO51	R/W	0h	Configuration Lock bit for this pin
18	GPIO50	R/W	0h	Configuration Lock bit for this pin
17	GPIO49	R/W	0h	Configuration Lock bit for this pin
16	GPIO48	R/W	0h	Configuration Lock bit for this pin
15	GPIO47	R/W	0h	Configuration Lock bit for this pin
14	GPIO46	R/W	0h	Configuration Lock bit for this pin
13	GPIO45	R/W	0h	Configuration Lock bit for this pin
12	GPIO44	R/W	0h	Configuration Lock bit for this pin

Table 6-98. GPBLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO43	R/W	0h	Configuration Lock bit for this pin
10	GPIO42	R/W	0h	Configuration Lock bit for this pin
9	GPIO41	R/W	0h	Configuration Lock bit for this pin
8	GPIO40	R/W	0h	Configuration Lock bit for this pin
7	GPIO39	R/W	0h	Configuration Lock bit for this pin
6	GPIO38	R/W	0h	Configuration Lock bit for this pin
5	GPIO37	R/W	0h	Configuration Lock bit for this pin
4	GPIO36	R/W	0h	Configuration Lock bit for this pin
3	GPIO35	R/W	0h	Configuration Lock bit for this pin
2	GPIO34	R/W	0h	Configuration Lock bit for this pin
1	GPIO33	R/W	0h	Configuration Lock bit for this pin
0	GPIO32	R/W	0h	Configuration Lock bit for this pin

6.4.4.35 GPBCR Register (offset = 7Eh) [reset = 0h]

GPBCR is shown in [Figure 6-92](#) and described in [Table 6-99](#).

GPIO B Lock Commit Register (GPIO32 to 63)

GPIO Configuration Lock Commit for GPIO:

1: Locks changes to the bit in GPyLOCK register which controls the same pin

0: Bit in the GPyLOCK register which controls the same pin can be changed

Figure 6-92. GPBCR Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-99. GPBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Configuration lock commit bit for this pin
30	GPIO62	R/W	0h	Configuration lock commit bit for this pin
29	GPIO61	R/W	0h	Configuration lock commit bit for this pin
28	GPIO60	R/W	0h	Configuration lock commit bit for this pin
27	GPIO59	R/W	0h	Configuration lock commit bit for this pin
26	GPIO58	R/W	0h	Configuration lock commit bit for this pin
25	GPIO57	R/W	0h	Configuration lock commit bit for this pin
24	GPIO56	R/W	0h	Configuration lock commit bit for this pin
23	GPIO55	R/W	0h	Configuration lock commit bit for this pin
22	GPIO54	R/W	0h	Configuration lock commit bit for this pin
21	GPIO53	R/W	0h	Configuration lock commit bit for this pin
20	GPIO52	R/W	0h	Configuration lock commit bit for this pin
19	GPIO51	R/W	0h	Configuration lock commit bit for this pin
18	GPIO50	R/W	0h	Configuration lock commit bit for this pin
17	GPIO49	R/W	0h	Configuration lock commit bit for this pin
16	GPIO48	R/W	0h	Configuration lock commit bit for this pin
15	GPIO47	R/W	0h	Configuration lock commit bit for this pin
14	GPIO46	R/W	0h	Configuration lock commit bit for this pin
13	GPIO45	R/W	0h	Configuration lock commit bit for this pin
12	GPIO44	R/W	0h	Configuration lock commit bit for this pin
11	GPIO43	R/W	0h	Configuration lock commit bit for this pin

Table 6-99. GPBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO42	R/W	0h	Configuration lock commit bit for this pin
9	GPIO41	R/W	0h	Configuration lock commit bit for this pin
8	GPIO40	R/W	0h	Configuration lock commit bit for this pin
7	GPIO39	R/W	0h	Configuration lock commit bit for this pin
6	GPIO38	R/W	0h	Configuration lock commit bit for this pin
5	GPIO37	R/W	0h	Configuration lock commit bit for this pin
4	GPIO36	R/W	0h	Configuration lock commit bit for this pin
3	GPIO35	R/W	0h	Configuration lock commit bit for this pin
2	GPIO34	R/W	0h	Configuration lock commit bit for this pin
1	GPIO33	R/W	0h	Configuration lock commit bit for this pin
0	GPIO32	R/W	0h	Configuration lock commit bit for this pin

6.4.4.36 GPCCTRL Register (offset = 80h) [reset = 0h]

GPCCTRL is shown in [Figure 6-93](#) and described in [Table 6-100](#).

GPIO C Qualification Sampling Period Control (GPIO64 to 95)

Figure 6-93. GPCCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUALPRD3								QUALPRD2								QUALPRD1				QUALPRD0											
R/W-0h								R/W-0h								R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-100. GPCCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	QUALPRD3	R/W	0h	Qualification sampling period for GPIO88 to GPIO95: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
23-16	QUALPRD2	R/W	0h	Qualification sampling period for GPIO80 to GPIO87: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
15-8	QUALPRD1	R/W	0h	Qualification sampling period for GPIO72 to GPIO79: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
7-0	QUALPRD0	R/W	0h	Qualification sampling period for GPIO64 to GPIO71: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510

6.4.4.37 GPCQSEL1 Register (offset = 82h) [reset = 0h]

GPCQSEL1 is shown in [Figure 6-94](#) and described in [Table 6-101](#).

GPIO C Qualifier Select 1 Register (GPIO64 to 79)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-94. GPCQSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO79		GPIO78		GPIO77		GPIO76		GPIO75		GPIO74		GPIO73		GPIO72	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO71		GPIO70		GPIO69		GPIO68		GPIO67		GPIO66		GPIO65		GPIO64	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-101. GPCQSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO79	R/W	0h	Input qualification type
29-28	GPIO78	R/W	0h	Input qualification type
27-26	GPIO77	R/W	0h	Input qualification type
25-24	GPIO76	R/W	0h	Input qualification type
23-22	GPIO75	R/W	0h	Input qualification type
21-20	GPIO74	R/W	0h	Input qualification type
19-18	GPIO73	R/W	0h	Input qualification type
17-16	GPIO72	R/W	0h	Input qualification type
15-14	GPIO71	R/W	0h	Input qualification type
13-12	GPIO70	R/W	0h	Input qualification type
11-10	GPIO69	R/W	0h	Input qualification type
9-8	GPIO68	R/W	0h	Input qualification type
7-6	GPIO67	R/W	0h	Input qualification type
5-4	GPIO66	R/W	0h	Input qualification type
3-2	GPIO65	R/W	0h	Input qualification type
1-0	GPIO64	R/W	0h	Input qualification type

6.4.4.38 GPCQSEL2 Register (offset = 84h) [reset = 0h]

GPCQSEL2 is shown in [Figure 6-95](#) and described in [Table 6-102](#).

GPIO C Qualifier Select 2 Register (GPIO80 to 95)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-95. GPCQSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO95		GPIO94		GPIO93		GPIO92		GPIO91		GPIO90		GPIO89		GPIO88	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO87		GPIO86		GPIO85		GPIO84		GPIO83		GPIO82		GPIO81		GPIO80	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-102. GPCQSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO95	R/W	0h	Input qualification type
29-28	GPIO94	R/W	0h	Input qualification type
27-26	GPIO93	R/W	0h	Input qualification type
25-24	GPIO92	R/W	0h	Input qualification type
23-22	GPIO91	R/W	0h	Input qualification type
21-20	GPIO90	R/W	0h	Input qualification type
19-18	GPIO89	R/W	0h	Input qualification type
17-16	GPIO88	R/W	0h	Input qualification type
15-14	GPIO87	R/W	0h	Input qualification type
13-12	GPIO86	R/W	0h	Input qualification type
11-10	GPIO85	R/W	0h	Input qualification type
9-8	GPIO84	R/W	0h	Input qualification type
7-6	GPIO83	R/W	0h	Input qualification type
5-4	GPIO82	R/W	0h	Input qualification type
3-2	GPIO81	R/W	0h	Input qualification type
1-0	GPIO80	R/W	0h	Input qualification type

6.4.4.39 GPCMUX1 Register (offset = 86h) [reset = 0h]

GPCMUX1 is shown in [Figure 6-96](#) and described in [Table 6-103](#).

GPIO C Mux 1 Register (GPIO64 to 79)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPYGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-96. GPCMUX1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO79		GPIO78		GPIO77		GPIO76		GPIO75		GPIO74		GPIO73		GPIO72	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO71		GPIO70		GPIO69		GPIO68		GPIO67		GPIO66		GPIO65		GPIO64	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-103. GPCMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO79	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO78	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO77	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO76	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO75	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO74	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO73	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO72	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO71	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO70	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO69	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO68	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO67	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO66	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO65	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO64	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.40 GPCMUX2 Register (offset = 88h) [reset = 0h]

GPCMUX2 is shown in [Figure 6-97](#) and described in [Table 6-104](#).

GPIO C Mux 2 Register (GPIO80 to 95)
Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-97. GPCMUX2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-104. GPCMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO95	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO94	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO93	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO92	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO91	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO90	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO89	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO88	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO87	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO86	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO85	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO84	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO83	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO82	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO81	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO80	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.41 GPCDIR Register (offset = 8Ah) [reset = 0h]

GPCDIR is shown in [Figure 6-98](#) and described in [Table 6-105](#).

GPIO C Direction Register (GPIO64 to 95)

Controls direction of GPIO pins when the specified pin is configured in GPIO mode.

0: Configures pin as input.

1: Configures pin as output.

Reading the register returns the current value of the register setting.

Figure 6-98. GPCDIR Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-105. GPCDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Defines direction for this pin in GPIO mode
30	GPIO94	R/W	0h	Defines direction for this pin in GPIO mode
29	GPIO93	R/W	0h	Defines direction for this pin in GPIO mode
28	GPIO92	R/W	0h	Defines direction for this pin in GPIO mode
27	GPIO91	R/W	0h	Defines direction for this pin in GPIO mode
26	GPIO90	R/W	0h	Defines direction for this pin in GPIO mode
25	GPIO89	R/W	0h	Defines direction for this pin in GPIO mode
24	GPIO88	R/W	0h	Defines direction for this pin in GPIO mode
23	GPIO87	R/W	0h	Defines direction for this pin in GPIO mode
22	GPIO86	R/W	0h	Defines direction for this pin in GPIO mode
21	GPIO85	R/W	0h	Defines direction for this pin in GPIO mode
20	GPIO84	R/W	0h	Defines direction for this pin in GPIO mode
19	GPIO83	R/W	0h	Defines direction for this pin in GPIO mode
18	GPIO82	R/W	0h	Defines direction for this pin in GPIO mode
17	GPIO81	R/W	0h	Defines direction for this pin in GPIO mode
16	GPIO80	R/W	0h	Defines direction for this pin in GPIO mode
15	GPIO79	R/W	0h	Defines direction for this pin in GPIO mode
14	GPIO78	R/W	0h	Defines direction for this pin in GPIO mode
13	GPIO77	R/W	0h	Defines direction for this pin in GPIO mode
12	GPIO76	R/W	0h	Defines direction for this pin in GPIO mode

Table 6-105. GPCDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO75	R/W	0h	Defines direction for this pin in GPIO mode
10	GPIO74	R/W	0h	Defines direction for this pin in GPIO mode
9	GPIO73	R/W	0h	Defines direction for this pin in GPIO mode
8	GPIO72	R/W	0h	Defines direction for this pin in GPIO mode
7	GPIO71	R/W	0h	Defines direction for this pin in GPIO mode
6	GPIO70	R/W	0h	Defines direction for this pin in GPIO mode
5	GPIO69	R/W	0h	Defines direction for this pin in GPIO mode
4	GPIO68	R/W	0h	Defines direction for this pin in GPIO mode
3	GPIO67	R/W	0h	Defines direction for this pin in GPIO mode
2	GPIO66	R/W	0h	Defines direction for this pin in GPIO mode
1	GPIO65	R/W	0h	Defines direction for this pin in GPIO mode
0	GPIO64	R/W	0h	Defines direction for this pin in GPIO mode

6.4.4.42 GPCPUD Register (offset = 8Ch) [reset = FFFFFFFFh]

GPCPUD is shown in [Figure 6-99](#) and described in [Table 6-106](#).

GPIO C Pull Up Disable Register (GPIO64 to 95)

Disables the Pull-Up on GPIO.

0: Enables the Pull-Up.

1: Disables the Pull-Up.

Reading the register returns the current value of the register setting.

Note:

[1] The Pull-Ups on the GPIO pins are disabled asynchronously when IORSn signal is low.

Figure 6-99. GPCPUD Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-1h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-1h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-1h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-106. GPCPUD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	1h	Pull-Up Disable control for this pin
30	GPIO94	R/W	1h	Pull-Up Disable control for this pin
29	GPIO93	R/W	1h	Pull-Up Disable control for this pin
28	GPIO92	R/W	1h	Pull-Up Disable control for this pin
27	GPIO91	R/W	1h	Pull-Up Disable control for this pin
26	GPIO90	R/W	1h	Pull-Up Disable control for this pin
25	GPIO89	R/W	1h	Pull-Up Disable control for this pin
24	GPIO88	R/W	1h	Pull-Up Disable control for this pin
23	GPIO87	R/W	1h	Pull-Up Disable control for this pin
22	GPIO86	R/W	1h	Pull-Up Disable control for this pin
21	GPIO85	R/W	1h	Pull-Up Disable control for this pin
20	GPIO84	R/W	1h	Pull-Up Disable control for this pin
19	GPIO83	R/W	1h	Pull-Up Disable control for this pin
18	GPIO82	R/W	1h	Pull-Up Disable control for this pin
17	GPIO81	R/W	1h	Pull-Up Disable control for this pin
16	GPIO80	R/W	1h	Pull-Up Disable control for this pin
15	GPIO79	R/W	1h	Pull-Up Disable control for this pin
14	GPIO78	R/W	1h	Pull-Up Disable control for this pin
13	GPIO77	R/W	1h	Pull-Up Disable control for this pin

Table 6-106. GPCPUD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	GPIO76	R/W	1h	Pull-Up Disable control for this pin
11	GPIO75	R/W	1h	Pull-Up Disable control for this pin
10	GPIO74	R/W	1h	Pull-Up Disable control for this pin
9	GPIO73	R/W	1h	Pull-Up Disable control for this pin
8	GPIO72	R/W	1h	Pull-Up Disable control for this pin
7	GPIO71	R/W	1h	Pull-Up Disable control for this pin
6	GPIO70	R/W	1h	Pull-Up Disable control for this pin
5	GPIO69	R/W	1h	Pull-Up Disable control for this pin
4	GPIO68	R/W	1h	Pull-Up Disable control for this pin
3	GPIO67	R/W	1h	Pull-Up Disable control for this pin
2	GPIO66	R/W	1h	Pull-Up Disable control for this pin
1	GPIO65	R/W	1h	Pull-Up Disable control for this pin
0	GPIO64	R/W	1h	Pull-Up Disable control for this pin

6.4.4.43 GPCINV Register (offset = 90h) [reset = 0h]

GPCINV is shown in [Figure 6-100](#) and described in [Table 6-107](#).

GPIO C Input Polarity Invert Registers (GPIO64 to 95)

Selects between non-inverted and inverted GPIO input to the device.

0: selects non-inverted GPIO input

1: selects inverted GPIO input

Reading the register returns the current value of the register setting.

Figure 6-100. GPCINV Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-107. GPCINV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Input inversion control for this pin
30	GPIO94	R/W	0h	Input inversion control for this pin
29	GPIO93	R/W	0h	Input inversion control for this pin
28	GPIO92	R/W	0h	Input inversion control for this pin
27	GPIO91	R/W	0h	Input inversion control for this pin
26	GPIO90	R/W	0h	Input inversion control for this pin
25	GPIO89	R/W	0h	Input inversion control for this pin
24	GPIO88	R/W	0h	Input inversion control for this pin
23	GPIO87	R/W	0h	Input inversion control for this pin
22	GPIO86	R/W	0h	Input inversion control for this pin
21	GPIO85	R/W	0h	Input inversion control for this pin
20	GPIO84	R/W	0h	Input inversion control for this pin
19	GPIO83	R/W	0h	Input inversion control for this pin
18	GPIO82	R/W	0h	Input inversion control for this pin
17	GPIO81	R/W	0h	Input inversion control for this pin
16	GPIO80	R/W	0h	Input inversion control for this pin
15	GPIO79	R/W	0h	Input inversion control for this pin
14	GPIO78	R/W	0h	Input inversion control for this pin
13	GPIO77	R/W	0h	Input inversion control for this pin
12	GPIO76	R/W	0h	Input inversion control for this pin

Table 6-107. GPCINV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO75	R/W	0h	Input inversion control for this pin
10	GPIO74	R/W	0h	Input inversion control for this pin
9	GPIO73	R/W	0h	Input inversion control for this pin
8	GPIO72	R/W	0h	Input inversion control for this pin
7	GPIO71	R/W	0h	Input inversion control for this pin
6	GPIO70	R/W	0h	Input inversion control for this pin
5	GPIO69	R/W	0h	Input inversion control for this pin
4	GPIO68	R/W	0h	Input inversion control for this pin
3	GPIO67	R/W	0h	Input inversion control for this pin
2	GPIO66	R/W	0h	Input inversion control for this pin
1	GPIO65	R/W	0h	Input inversion control for this pin
0	GPIO64	R/W	0h	Input inversion control for this pin

6.4.4.44 GPCODR Register (offset = 92h) [reset = 0h]

GPCODR is shown in [Figure 6-101](#) and described in [Table 6-108](#).

GPIO C Open Drain Output Register (GPIO64 to GPIO95)

Selects between normal and open-drain output for the GPIO pin.

0: Normal Output

1: Open Drain Output

Reading the register returns the current value of the register setting.

Note:

[1] In the Open Drain output mode, if the buffer is configured for output mode, a 0 value to be driven out comes out on the on the PAD while a 1 value to be driven out tri-states the buffer.

Figure 6-101. GPCODR Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-108. GPCODR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Output Open-Drain control for this pin
30	GPIO94	R/W	0h	Output Open-Drain control for this pin
29	GPIO93	R/W	0h	Output Open-Drain control for this pin
28	GPIO92	R/W	0h	Output Open-Drain control for this pin
27	GPIO91	R/W	0h	Output Open-Drain control for this pin
26	GPIO90	R/W	0h	Output Open-Drain control for this pin
25	GPIO89	R/W	0h	Output Open-Drain control for this pin
24	GPIO88	R/W	0h	Output Open-Drain control for this pin
23	GPIO87	R/W	0h	Output Open-Drain control for this pin
22	GPIO86	R/W	0h	Output Open-Drain control for this pin
21	GPIO85	R/W	0h	Output Open-Drain control for this pin
20	GPIO84	R/W	0h	Output Open-Drain control for this pin
19	GPIO83	R/W	0h	Output Open-Drain control for this pin
18	GPIO82	R/W	0h	Output Open-Drain control for this pin
17	GPIO81	R/W	0h	Output Open-Drain control for this pin
16	GPIO80	R/W	0h	Output Open-Drain control for this pin
15	GPIO79	R/W	0h	Output Open-Drain control for this pin
14	GPIO78	R/W	0h	Output Open-Drain control for this pin

Table 6-108. GPCODR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO77	R/W	0h	Output Open-Drain control for this pin
12	GPIO76	R/W	0h	Output Open-Drain control for this pin
11	GPIO75	R/W	0h	Output Open-Drain control for this pin
10	GPIO74	R/W	0h	Output Open-Drain control for this pin
9	GPIO73	R/W	0h	Output Open-Drain control for this pin
8	GPIO72	R/W	0h	Output Open-Drain control for this pin
7	GPIO71	R/W	0h	Output Open-Drain control for this pin
6	GPIO70	R/W	0h	Output Open-Drain control for this pin
5	GPIO69	R/W	0h	Output Open-Drain control for this pin
4	GPIO68	R/W	0h	Output Open-Drain control for this pin
3	GPIO67	R/W	0h	Output Open-Drain control for this pin
2	GPIO66	R/W	0h	Output Open-Drain control for this pin
1	GPIO65	R/W	0h	Output Open-Drain control for this pin
0	GPIO64	R/W	0h	Output Open-Drain control for this pin

6.4.4.45 GPCGMUX1 Register (offset = A0h) [reset = 0h]

GPCGMUX1 is shown in [Figure 6-102](#) and described in [Table 6-109](#).

GPIO C Peripheral Group Mux (GPIO64 to 79)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-102. GPCGMUX1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-109. GPCGMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO79	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO78	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO77	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO76	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO75	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO74	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO73	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO72	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO71	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO70	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO69	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO68	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO67	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO66	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO65	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO64	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.46 GPCGMUX2 Register (offset = A2h) [reset = 0h]

GPCGMUX2 is shown in [Figure 6-103](#) and described in [Table 6-110](#).

GPIO C Peripheral Group Mux (GPIO80 to 95)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-103. GPCGMUX2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-110. GPCGMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO95	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO94	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO93	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO92	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO91	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO90	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO89	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO88	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO87	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO86	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO85	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO84	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO83	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO82	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO81	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO80	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.47 GPCCSEL1 Register (offset = A8h) [reset = 0h]

GPCCSEL1 is shown in [Figure 6-104](#) and described in [Table 6-111](#).

GPIO C Core Select Register (GPIO64 to 71)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-104. GPCCSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO71				GPIO70				GPIO69				GPIO68			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO67				GPIO66				GPIO65				GPIO64			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-111. GPCCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO71	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO70	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO69	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO68	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO67	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO66	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO65	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO64	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.48 GPCCSEL2 Register (offset = AAh) [reset = 0h]

GPCCSEL2 is shown in [Figure 6-105](#) and described in [Table 6-112](#).

GPIO C Core Select Register (GPIO72 to 79)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-105. GPCCSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO79				GPIO78				GPIO77				GPIO76			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO75				GPIO74				GPIO73				GPIO72			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-112. GPCCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO79	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO78	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO77	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO76	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO75	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO74	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO73	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO72	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.49 GPCCSEL3 Register (offset = ACh) [reset = 0h]

GPCCSEL3 is shown in [Figure 6-106](#) and described in [Table 6-113](#).

GPIO C Core Select Register (GPIO80 to 87)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-106. GPCCSEL3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO87				GPIO86				GPIO85				GPIO84			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO83				GPIO82				GPIO81				GPIO80			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-113. GPCCSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO87	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO86	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO85	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO84	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO83	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO82	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO81	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO80	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.50 GPCCSEL4 Register (offset = AEh) [reset = 0h]

GPCCSEL4 is shown in [Figure 6-107](#) and described in [Table 6-114](#).

GPIO C Core Select Register (GPIO88 to 95)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-107. GPCCSEL4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO95				GPIO94				GPIO93				GPIO92			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO91				GPIO90				GPIO89				GPIO88			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-114. GPCCSEL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO95	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO94	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO93	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO92	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO91	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO90	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO89	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO88	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.51 GPCLOCK Register (offset = BCh) [reset = 0h]

GPCLOCK is shown in [Figure 6-108](#) and described in [Table 6-115](#).

GPIO C Lock Configuration Register (GPIO64 to 95)

GPIO Configuration Lock for GPIO.

0: Bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx register which control the same pin can be changed

1: Locks changes to the bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx registers which control the same pin

Figure 6-108. GPCLOCK Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-115. GPCLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Configuration Lock bit for this pin
30	GPIO94	R/W	0h	Configuration Lock bit for this pin
29	GPIO93	R/W	0h	Configuration Lock bit for this pin
28	GPIO92	R/W	0h	Configuration Lock bit for this pin
27	GPIO91	R/W	0h	Configuration Lock bit for this pin
26	GPIO90	R/W	0h	Configuration Lock bit for this pin
25	GPIO89	R/W	0h	Configuration Lock bit for this pin
24	GPIO88	R/W	0h	Configuration Lock bit for this pin
23	GPIO87	R/W	0h	Configuration Lock bit for this pin
22	GPIO86	R/W	0h	Configuration Lock bit for this pin
21	GPIO85	R/W	0h	Configuration Lock bit for this pin
20	GPIO84	R/W	0h	Configuration Lock bit for this pin
19	GPIO83	R/W	0h	Configuration Lock bit for this pin
18	GPIO82	R/W	0h	Configuration Lock bit for this pin
17	GPIO81	R/W	0h	Configuration Lock bit for this pin
16	GPIO80	R/W	0h	Configuration Lock bit for this pin
15	GPIO79	R/W	0h	Configuration Lock bit for this pin
14	GPIO78	R/W	0h	Configuration Lock bit for this pin
13	GPIO77	R/W	0h	Configuration Lock bit for this pin
12	GPIO76	R/W	0h	Configuration Lock bit for this pin

Table 6-115. GPCLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO75	R/W	0h	Configuration Lock bit for this pin
10	GPIO74	R/W	0h	Configuration Lock bit for this pin
9	GPIO73	R/W	0h	Configuration Lock bit for this pin
8	GPIO72	R/W	0h	Configuration Lock bit for this pin
7	GPIO71	R/W	0h	Configuration Lock bit for this pin
6	GPIO70	R/W	0h	Configuration Lock bit for this pin
5	GPIO69	R/W	0h	Configuration Lock bit for this pin
4	GPIO68	R/W	0h	Configuration Lock bit for this pin
3	GPIO67	R/W	0h	Configuration Lock bit for this pin
2	GPIO66	R/W	0h	Configuration Lock bit for this pin
1	GPIO65	R/W	0h	Configuration Lock bit for this pin
0	GPIO64	R/W	0h	Configuration Lock bit for this pin

6.4.4.52 GPCCR Register (offset = BEh) [reset = 0h]

GPCCR is shown in [Figure 6-109](#) and described in [Table 6-116](#).

GPIO C Lock Commit Register (GPIO64 to 95)

GPIO Configuration Lock Commit for GPIO:

1: Locks changes to the bit in GPyLOCK register which controls the same pin

0: Bit in the GPyLOCK register which controls the same pin can be changed

Figure 6-109. GPCCR Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-116. GPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Configuration lock commit bit for this pin
30	GPIO94	R/W	0h	Configuration lock commit bit for this pin
29	GPIO93	R/W	0h	Configuration lock commit bit for this pin
28	GPIO92	R/W	0h	Configuration lock commit bit for this pin
27	GPIO91	R/W	0h	Configuration lock commit bit for this pin
26	GPIO90	R/W	0h	Configuration lock commit bit for this pin
25	GPIO89	R/W	0h	Configuration lock commit bit for this pin
24	GPIO88	R/W	0h	Configuration lock commit bit for this pin
23	GPIO87	R/W	0h	Configuration lock commit bit for this pin
22	GPIO86	R/W	0h	Configuration lock commit bit for this pin
21	GPIO85	R/W	0h	Configuration lock commit bit for this pin
20	GPIO84	R/W	0h	Configuration lock commit bit for this pin
19	GPIO83	R/W	0h	Configuration lock commit bit for this pin
18	GPIO82	R/W	0h	Configuration lock commit bit for this pin
17	GPIO81	R/W	0h	Configuration lock commit bit for this pin
16	GPIO80	R/W	0h	Configuration lock commit bit for this pin
15	GPIO79	R/W	0h	Configuration lock commit bit for this pin
14	GPIO78	R/W	0h	Configuration lock commit bit for this pin
13	GPIO77	R/W	0h	Configuration lock commit bit for this pin
12	GPIO76	R/W	0h	Configuration lock commit bit for this pin
11	GPIO75	R/W	0h	Configuration lock commit bit for this pin

Table 6-116. GPCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO74	R/W	0h	Configuration lock commit bit for this pin
9	GPIO73	R/W	0h	Configuration lock commit bit for this pin
8	GPIO72	R/W	0h	Configuration lock commit bit for this pin
7	GPIO71	R/W	0h	Configuration lock commit bit for this pin
6	GPIO70	R/W	0h	Configuration lock commit bit for this pin
5	GPIO69	R/W	0h	Configuration lock commit bit for this pin
4	GPIO68	R/W	0h	Configuration lock commit bit for this pin
3	GPIO67	R/W	0h	Configuration lock commit bit for this pin
2	GPIO66	R/W	0h	Configuration lock commit bit for this pin
1	GPIO65	R/W	0h	Configuration lock commit bit for this pin
0	GPIO64	R/W	0h	Configuration lock commit bit for this pin

6.4.4.53 GPDCTRL Register (offset = C0h) [reset = 0h]

GPDCTRL is shown in [Figure 6-110](#) and described in [Table 6-117](#).

GPIO D Qualification Sampling Period Control (GPIO96 to 127)

Figure 6-110. GPDCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUALPRD3								QUALPRD2								QUALPRD1				QUALPRD0											
R/W-0h								R/W-0h								R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-117. GPDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	QUALPRD3	R/W	0h	Qualification sampling period for GPIO120 to GPIO127: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
23-16	QUALPRD2	R/W	0h	Qualification sampling period for GPIO112 to GPIO119: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
15-8	QUALPRD1	R/W	0h	Qualification sampling period for GPIO104 to GPIO111: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
7-0	QUALPRD0	R/W	0h	Qualification sampling period for GPIO96 to GPIO103: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510

6.4.4.54 GPDQSEL1 Register (offset = C2h) [reset = 0h]

GPDQSEL1 is shown in [Figure 6-111](#) and described in [Table 6-118](#).

GPIO D Qualifier Select 1 Register (GPIO96 to 111)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-111. GPDQSEL1 Register

31	30	29	28	27	26	25	24
GPIO111		GPIO110		GPIO109		GPIO108	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO107		GPIO106		GPIO105		GPIO104	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO103		GPIO102		GPIO101		GPIO100	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO99		GPIO98		GPIO97		GPIO96	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-118. GPDQSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO111	R/W	0h	Input qualification type
29-28	GPIO110	R/W	0h	Input qualification type
27-26	GPIO109	R/W	0h	Input qualification type
25-24	GPIO108	R/W	0h	Input qualification type
23-22	GPIO107	R/W	0h	Input qualification type
21-20	GPIO106	R/W	0h	Input qualification type
19-18	GPIO105	R/W	0h	Input qualification type
17-16	GPIO104	R/W	0h	Input qualification type
15-14	GPIO103	R/W	0h	Input qualification type
13-12	GPIO102	R/W	0h	Input qualification type
11-10	GPIO101	R/W	0h	Input qualification type
9-8	GPIO100	R/W	0h	Input qualification type
7-6	GPIO99	R/W	0h	Input qualification type
5-4	GPIO98	R/W	0h	Input qualification type
3-2	GPIO97	R/W	0h	Input qualification type
1-0	GPIO96	R/W	0h	Input qualification type

6.4.4.55 GPDQSEL2 Register (offset = C4h) [reset = 0h]

GPDQSEL2 is shown in [Figure 6-112](#) and described in [Table 6-119](#).

GPIO D Qualifier Select 2 Register (GPIO112 to 127)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-112. GPDQSEL2 Register

31	30	29	28	27	26	25	24
GPIO127		GPIO126		GPIO125		GPIO124	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO123		GPIO122		GPIO121		GPIO120	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO119		GPIO118		GPIO117		GPIO116	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO115		GPIO114		GPIO113		GPIO112	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-119. GPDQSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO127	R/W	0h	Input qualification type
29-28	GPIO126	R/W	0h	Input qualification type
27-26	GPIO125	R/W	0h	Input qualification type
25-24	GPIO124	R/W	0h	Input qualification type
23-22	GPIO123	R/W	0h	Input qualification type
21-20	GPIO122	R/W	0h	Input qualification type
19-18	GPIO121	R/W	0h	Input qualification type
17-16	GPIO120	R/W	0h	Input qualification type
15-14	GPIO119	R/W	0h	Input qualification type
13-12	GPIO118	R/W	0h	Input qualification type
11-10	GPIO117	R/W	0h	Input qualification type
9-8	GPIO116	R/W	0h	Input qualification type
7-6	GPIO115	R/W	0h	Input qualification type
5-4	GPIO114	R/W	0h	Input qualification type
3-2	GPIO113	R/W	0h	Input qualification type
1-0	GPIO112	R/W	0h	Input qualification type

6.4.4.56 GPDMUX1 Register (offset = C6h) [reset = 0h]

GPDMUX1 is shown in [Figure 6-113](#) and described in [Table 6-120](#).

GPIO D Mux 1 Register (GPIO96 to 111)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-113. GPDMUX1 Register

31	30	29	28	27	26	25	24
GPIO111		GPIO110		GPIO109		GPIO108	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO107		GPIO106		GPIO105		GPIO104	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO103		GPIO102		GPIO101		GPIO100	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO99		GPIO98		GPIO97		GPIO96	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-120. GPDMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO111	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO110	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO109	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO108	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO107	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO106	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO105	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO104	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO103	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO102	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO101	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO100	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO99	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO98	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO97	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO96	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.57 GPDMUX2 Register (offset = C8h) [reset = 0h]

GPDMUX2 is shown in [Figure 6-114](#) and described in [Table 6-121](#).

GPIO D Mux 2 Register (GPIO112 to 127)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-114. GPDMUX2 Register

31	30	29	28	27	26	25	24
GPIO127		GPIO126		GPIO125		GPIO124	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO123		GPIO122		GPIO121		GPIO120	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO119		GPIO118		GPIO117		GPIO116	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO115		GPIO114		GPIO113		GPIO112	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-121. GPDMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO127	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO126	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO125	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO124	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO123	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO122	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO121	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO120	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO119	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO118	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO117	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO116	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO115	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO114	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO113	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO112	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.58 GPDDIR Register (offset = CAh) [reset = 0h]

GPDDIR is shown in [Figure 6-115](#) and described in [Table 6-122](#).

GPIO D Direction Register (GPIO96 to 127)

Controls direction of GPIO pins when the specified pin is configured in GPIO mode.

0: Configures pin as input.

1: Configures pin as output.

Reading the register returns the current value of the register setting.

Figure 6-115. GPDDIR Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-122. GPDDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Defines direction for this pin in GPIO mode
30	GPIO126	R/W	0h	Defines direction for this pin in GPIO mode
29	GPIO125	R/W	0h	Defines direction for this pin in GPIO mode
28	GPIO124	R/W	0h	Defines direction for this pin in GPIO mode
27	GPIO123	R/W	0h	Defines direction for this pin in GPIO mode
26	GPIO122	R/W	0h	Defines direction for this pin in GPIO mode
25	GPIO121	R/W	0h	Defines direction for this pin in GPIO mode
24	GPIO120	R/W	0h	Defines direction for this pin in GPIO mode
23	GPIO119	R/W	0h	Defines direction for this pin in GPIO mode
22	GPIO118	R/W	0h	Defines direction for this pin in GPIO mode
21	GPIO117	R/W	0h	Defines direction for this pin in GPIO mode
20	GPIO116	R/W	0h	Defines direction for this pin in GPIO mode
19	GPIO115	R/W	0h	Defines direction for this pin in GPIO mode
18	GPIO114	R/W	0h	Defines direction for this pin in GPIO mode
17	GPIO113	R/W	0h	Defines direction for this pin in GPIO mode
16	GPIO112	R/W	0h	Defines direction for this pin in GPIO mode
15	GPIO111	R/W	0h	Defines direction for this pin in GPIO mode
14	GPIO110	R/W	0h	Defines direction for this pin in GPIO mode
13	GPIO109	R/W	0h	Defines direction for this pin in GPIO mode
12	GPIO108	R/W	0h	Defines direction for this pin in GPIO mode

Table 6-122. GPDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO107	R/W	0h	Defines direction for this pin in GPIO mode
10	GPIO106	R/W	0h	Defines direction for this pin in GPIO mode
9	GPIO105	R/W	0h	Defines direction for this pin in GPIO mode
8	GPIO104	R/W	0h	Defines direction for this pin in GPIO mode
7	GPIO103	R/W	0h	Defines direction for this pin in GPIO mode
6	GPIO102	R/W	0h	Defines direction for this pin in GPIO mode
5	GPIO101	R/W	0h	Defines direction for this pin in GPIO mode
4	GPIO100	R/W	0h	Defines direction for this pin in GPIO mode
3	GPIO99	R/W	0h	Defines direction for this pin in GPIO mode
2	GPIO98	R/W	0h	Defines direction for this pin in GPIO mode
1	GPIO97	R/W	0h	Defines direction for this pin in GPIO mode
0	GPIO96	R/W	0h	Defines direction for this pin in GPIO mode

6.4.4.59 GPDPU Register (offset = CCh) [reset = FFFFFFFFh]

GPDPU is shown in [Figure 6-116](#) and described in [Table 6-123](#).

GPIO D Pull Up Disable Register (GPIO96 to 127)

Disables the Pull-Up on GPIO.

0: Enables the Pull-Up.

1: Disables the Pull-Up.

Reading the register returns the current value of the register setting.

Note:

[1] The Pull-Ups on the GPIO pins are disabled asynchronously when IORSn signal is low.

Figure 6-116. GPDPU Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-1h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-1h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-1h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-123. GPDPU Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	1h	Pull-Up Disable control for this pin
30	GPIO126	R/W	1h	Pull-Up Disable control for this pin
29	GPIO125	R/W	1h	Pull-Up Disable control for this pin
28	GPIO124	R/W	1h	Pull-Up Disable control for this pin
27	GPIO123	R/W	1h	Pull-Up Disable control for this pin
26	GPIO122	R/W	1h	Pull-Up Disable control for this pin
25	GPIO121	R/W	1h	Pull-Up Disable control for this pin
24	GPIO120	R/W	1h	Pull-Up Disable control for this pin
23	GPIO119	R/W	1h	Pull-Up Disable control for this pin
22	GPIO118	R/W	1h	Pull-Up Disable control for this pin
21	GPIO117	R/W	1h	Pull-Up Disable control for this pin
20	GPIO116	R/W	1h	Pull-Up Disable control for this pin
19	GPIO115	R/W	1h	Pull-Up Disable control for this pin
18	GPIO114	R/W	1h	Pull-Up Disable control for this pin
17	GPIO113	R/W	1h	Pull-Up Disable control for this pin
16	GPIO112	R/W	1h	Pull-Up Disable control for this pin
15	GPIO111	R/W	1h	Pull-Up Disable control for this pin
14	GPIO110	R/W	1h	Pull-Up Disable control for this pin
13	GPIO109	R/W	1h	Pull-Up Disable control for this pin

Table 6-123. GPDPUD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	GPIO108	R/W	1h	Pull-Up Disable control for this pin
11	GPIO107	R/W	1h	Pull-Up Disable control for this pin
10	GPIO106	R/W	1h	Pull-Up Disable control for this pin
9	GPIO105	R/W	1h	Pull-Up Disable control for this pin
8	GPIO104	R/W	1h	Pull-Up Disable control for this pin
7	GPIO103	R/W	1h	Pull-Up Disable control for this pin
6	GPIO102	R/W	1h	Pull-Up Disable control for this pin
5	GPIO101	R/W	1h	Pull-Up Disable control for this pin
4	GPIO100	R/W	1h	Pull-Up Disable control for this pin
3	GPIO99	R/W	1h	Pull-Up Disable control for this pin
2	GPIO98	R/W	1h	Pull-Up Disable control for this pin
1	GPIO97	R/W	1h	Pull-Up Disable control for this pin
0	GPIO96	R/W	1h	Pull-Up Disable control for this pin

6.4.4.60 GPDINV Register (offset = D0h) [reset = 0h]

GPDINV is shown in [Figure 6-117](#) and described in [Table 6-124](#).

GPIO D Input Polarity Invert Registers (GPIO96 to 127)

Selects between non-inverted and inverted GPIO input to the device.

0: selects non-inverted GPIO input

1: selects inverted GPIO input

Reading the register returns the current value of the register setting.

Figure 6-117. GPDINV Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-124. GPDINV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Input inversion control for this pin
30	GPIO126	R/W	0h	Input inversion control for this pin
29	GPIO125	R/W	0h	Input inversion control for this pin
28	GPIO124	R/W	0h	Input inversion control for this pin
27	GPIO123	R/W	0h	Input inversion control for this pin
26	GPIO122	R/W	0h	Input inversion control for this pin
25	GPIO121	R/W	0h	Input inversion control for this pin
24	GPIO120	R/W	0h	Input inversion control for this pin
23	GPIO119	R/W	0h	Input inversion control for this pin
22	GPIO118	R/W	0h	Input inversion control for this pin
21	GPIO117	R/W	0h	Input inversion control for this pin
20	GPIO116	R/W	0h	Input inversion control for this pin
19	GPIO115	R/W	0h	Input inversion control for this pin
18	GPIO114	R/W	0h	Input inversion control for this pin
17	GPIO113	R/W	0h	Input inversion control for this pin
16	GPIO112	R/W	0h	Input inversion control for this pin
15	GPIO111	R/W	0h	Input inversion control for this pin
14	GPIO110	R/W	0h	Input inversion control for this pin
13	GPIO109	R/W	0h	Input inversion control for this pin
12	GPIO108	R/W	0h	Input inversion control for this pin

Table 6-124. GPDINV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO107	R/W	0h	Input inversion control for this pin
10	GPIO106	R/W	0h	Input inversion control for this pin
9	GPIO105	R/W	0h	Input inversion control for this pin
8	GPIO104	R/W	0h	Input inversion control for this pin
7	GPIO103	R/W	0h	Input inversion control for this pin
6	GPIO102	R/W	0h	Input inversion control for this pin
5	GPIO101	R/W	0h	Input inversion control for this pin
4	GPIO100	R/W	0h	Input inversion control for this pin
3	GPIO99	R/W	0h	Input inversion control for this pin
2	GPIO98	R/W	0h	Input inversion control for this pin
1	GPIO97	R/W	0h	Input inversion control for this pin
0	GPIO96	R/W	0h	Input inversion control for this pin

6.4.4.61 GPDODR Register (offset = D2h) [reset = 0h]

GPDODR is shown in [Figure 6-118](#) and described in [Table 6-125](#).

GPIO D Open Drain Output Register (GPIO96 to GPIO127)

Selects between normal and open-drain output for the GPIO pin.

0: Normal Output

1: Open Drain Output

Reading the register returns the current value of the register setting.

Note:

[1] In the Open Drain output mode, if the buffer is configured for output mode, a 0 value to be driven out comes out on the on the PAD while a 1 value to be driven out tri-states the buffer.

Figure 6-118. GPDODR Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-125. GPDODR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Output Open-Drain control for this pin
30	GPIO126	R/W	0h	Output Open-Drain control for this pin
29	GPIO125	R/W	0h	Output Open-Drain control for this pin
28	GPIO124	R/W	0h	Output Open-Drain control for this pin
27	GPIO123	R/W	0h	Output Open-Drain control for this pin
26	GPIO122	R/W	0h	Output Open-Drain control for this pin
25	GPIO121	R/W	0h	Output Open-Drain control for this pin
24	GPIO120	R/W	0h	Output Open-Drain control for this pin
23	GPIO119	R/W	0h	Output Open-Drain control for this pin
22	GPIO118	R/W	0h	Output Open-Drain control for this pin
21	GPIO117	R/W	0h	Output Open-Drain control for this pin
20	GPIO116	R/W	0h	Output Open-Drain control for this pin
19	GPIO115	R/W	0h	Output Open-Drain control for this pin
18	GPIO114	R/W	0h	Output Open-Drain control for this pin
17	GPIO113	R/W	0h	Output Open-Drain control for this pin
16	GPIO112	R/W	0h	Output Open-Drain control for this pin
15	GPIO111	R/W	0h	Output Open-Drain control for this pin
14	GPIO110	R/W	0h	Output Open-Drain control for this pin

Table 6-125. GPDODR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO109	R/W	0h	Output Open-Drain control for this pin
12	GPIO108	R/W	0h	Output Open-Drain control for this pin
11	GPIO107	R/W	0h	Output Open-Drain control for this pin
10	GPIO106	R/W	0h	Output Open-Drain control for this pin
9	GPIO105	R/W	0h	Output Open-Drain control for this pin
8	GPIO104	R/W	0h	Output Open-Drain control for this pin
7	GPIO103	R/W	0h	Output Open-Drain control for this pin
6	GPIO102	R/W	0h	Output Open-Drain control for this pin
5	GPIO101	R/W	0h	Output Open-Drain control for this pin
4	GPIO100	R/W	0h	Output Open-Drain control for this pin
3	GPIO99	R/W	0h	Output Open-Drain control for this pin
2	GPIO98	R/W	0h	Output Open-Drain control for this pin
1	GPIO97	R/W	0h	Output Open-Drain control for this pin
0	GPIO96	R/W	0h	Output Open-Drain control for this pin

6.4.4.62 GPDGMUX1 Register (offset = E0h) [reset = 0h]

GPDGMUX1 is shown in [Figure 6-119](#) and described in [Table 6-126](#).

GPIO D Peripheral Group Mux (GPIO96 to 111)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-119. GPDGMUX1 Register

31	30	29	28	27	26	25	24
GPIO111		GPIO110		GPIO109		GPIO108	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO107		GPIO106		GPIO105		GPIO104	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO103		GPIO102		GPIO101		GPIO100	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO99		GPIO98		GPIO97		GPIO96	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-126. GPDGMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO111	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO110	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO109	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO108	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO107	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO106	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO105	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO104	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO103	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO102	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO101	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO100	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO99	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO98	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO97	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO96	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.63 GPDGMUX2 Register (offset = E2h) [reset = 0h]

GPDGMUX2 is shown in [Figure 6-120](#) and described in [Table 6-127](#).

GPIO D Peripheral Group Mux (GPIO112 to 127)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-120. GPDGMUX2 Register

31	30	29	28	27	26	25	24
GPIO127		GPIO126		GPIO125		GPIO124	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO123		GPIO122		GPIO121		GPIO120	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO119		GPIO118		GPIO117		GPIO116	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO115		GPIO114		GPIO113		GPIO112	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-127. GPDGMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO127	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO126	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO125	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO124	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO123	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO122	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO121	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO120	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO119	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO118	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO117	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO116	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO115	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO114	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO113	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO112	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.64 GPDCSEL1 Register (offset = E8h) [reset = 0h]

GPDCSEL1 is shown in [Figure 6-121](#) and described in [Table 6-128](#).

GPIO D Core Select Register (GPIO96 to 103)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-121. GPDCSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO103				GPIO102				GPIO101				GPIO100			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO99				GPIO98				GPIO97				GPIO96			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-128. GPDCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO103	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO102	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO101	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO100	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO99	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO98	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO97	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO96	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.65 GPDCSEL2 Register (offset = EAh) [reset = 0h]

GPDCSEL2 is shown in [Figure 6-122](#) and described in [Table 6-129](#).

GPIO D Core Select Register (GPIO104 to 111)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-122. GPDCSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO111				GPIO110				GPIO109				GPIO108			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO107				GPIO106				GPIO105				GPIO104			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-129. GPDCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO111	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO110	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO109	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO108	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO107	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO106	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO105	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO104	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.66 GPDCSEL3 Register (offset = ECh) [reset = 0h]

GPDCSEL3 is shown in [Figure 6-123](#) and described in [Table 6-130](#).

GPIO D Core Select Register (GPIO112 to 119)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-123. GPDCSEL3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO119				GPIO118				GPIO117				GPIO116			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO115				GPIO114				GPIO113				GPIO112			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-130. GPDCSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO119	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO118	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO117	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO116	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO115	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO114	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO113	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO112	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.67 GPDCSEL4 Register (offset = EEh) [reset = 0h]

GPDCSEL4 is shown in [Figure 6-124](#) and described in [Table 6-131](#).

GPIO D Core Select Register (GPIO120 to 127)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-124. GPDCSEL4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO127				GPIO126				GPIO125				GPIO124			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO123				GPIO122				GPIO121				GPIO120			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-131. GPDCSEL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO127	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO126	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO125	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO124	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO123	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO122	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO121	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO120	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.68 GPDLOCK Register (offset = FCh) [reset = 0h]

GPDLOCK is shown in [Figure 6-125](#) and described in [Table 6-132](#).

GPIO D Lock Configuration Register (GPIO96 to 127)

GPIO Configuration Lock for GPIO.

0: Bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx register which control the same pin can be changed

1: Locks changes to the bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx registers which control the same pin

Figure 6-125. GPDLOCK Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-132. GPDLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Configuration Lock bit for this pin
30	GPIO126	R/W	0h	Configuration Lock bit for this pin
29	GPIO125	R/W	0h	Configuration Lock bit for this pin
28	GPIO124	R/W	0h	Configuration Lock bit for this pin
27	GPIO123	R/W	0h	Configuration Lock bit for this pin
26	GPIO122	R/W	0h	Configuration Lock bit for this pin
25	GPIO121	R/W	0h	Configuration Lock bit for this pin
24	GPIO120	R/W	0h	Configuration Lock bit for this pin
23	GPIO119	R/W	0h	Configuration Lock bit for this pin
22	GPIO118	R/W	0h	Configuration Lock bit for this pin
21	GPIO117	R/W	0h	Configuration Lock bit for this pin
20	GPIO116	R/W	0h	Configuration Lock bit for this pin
19	GPIO115	R/W	0h	Configuration Lock bit for this pin
18	GPIO114	R/W	0h	Configuration Lock bit for this pin
17	GPIO113	R/W	0h	Configuration Lock bit for this pin
16	GPIO112	R/W	0h	Configuration Lock bit for this pin
15	GPIO111	R/W	0h	Configuration Lock bit for this pin
14	GPIO110	R/W	0h	Configuration Lock bit for this pin
13	GPIO109	R/W	0h	Configuration Lock bit for this pin
12	GPIO108	R/W	0h	Configuration Lock bit for this pin

Table 6-132. GPDLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO107	R/W	0h	Configuration Lock bit for this pin
10	GPIO106	R/W	0h	Configuration Lock bit for this pin
9	GPIO105	R/W	0h	Configuration Lock bit for this pin
8	GPIO104	R/W	0h	Configuration Lock bit for this pin
7	GPIO103	R/W	0h	Configuration Lock bit for this pin
6	GPIO102	R/W	0h	Configuration Lock bit for this pin
5	GPIO101	R/W	0h	Configuration Lock bit for this pin
4	GPIO100	R/W	0h	Configuration Lock bit for this pin
3	GPIO99	R/W	0h	Configuration Lock bit for this pin
2	GPIO98	R/W	0h	Configuration Lock bit for this pin
1	GPIO97	R/W	0h	Configuration Lock bit for this pin
0	GPIO96	R/W	0h	Configuration Lock bit for this pin

6.4.4.69 GPDCR Register (offset = FEh) [reset = 0h]

GPDCR is shown in [Figure 6-126](#) and described in [Table 6-133](#).

GPIO D Lock Commit Register (GPIO96 to 127)

GPIO Configuration Lock Commit for GPIO:

1: Locks changes to the bit in GPyLOCK register which controls the same pin

0: Bit in the GPyLOCK register which controls the same pin can be changed

Figure 6-126. GPDCR Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-133. GPDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Configuration lock commit bit for this pin
30	GPIO126	R/W	0h	Configuration lock commit bit for this pin
29	GPIO125	R/W	0h	Configuration lock commit bit for this pin
28	GPIO124	R/W	0h	Configuration lock commit bit for this pin
27	GPIO123	R/W	0h	Configuration lock commit bit for this pin
26	GPIO122	R/W	0h	Configuration lock commit bit for this pin
25	GPIO121	R/W	0h	Configuration lock commit bit for this pin
24	GPIO120	R/W	0h	Configuration lock commit bit for this pin
23	GPIO119	R/W	0h	Configuration lock commit bit for this pin
22	GPIO118	R/W	0h	Configuration lock commit bit for this pin
21	GPIO117	R/W	0h	Configuration lock commit bit for this pin
20	GPIO116	R/W	0h	Configuration lock commit bit for this pin
19	GPIO115	R/W	0h	Configuration lock commit bit for this pin
18	GPIO114	R/W	0h	Configuration lock commit bit for this pin
17	GPIO113	R/W	0h	Configuration lock commit bit for this pin
16	GPIO112	R/W	0h	Configuration lock commit bit for this pin
15	GPIO111	R/W	0h	Configuration lock commit bit for this pin
14	GPIO110	R/W	0h	Configuration lock commit bit for this pin
13	GPIO109	R/W	0h	Configuration lock commit bit for this pin
12	GPIO108	R/W	0h	Configuration lock commit bit for this pin
11	GPIO107	R/W	0h	Configuration lock commit bit for this pin

Table 6-133. GPDCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO106	R/W	0h	Configuration lock commit bit for this pin
9	GPIO105	R/W	0h	Configuration lock commit bit for this pin
8	GPIO104	R/W	0h	Configuration lock commit bit for this pin
7	GPIO103	R/W	0h	Configuration lock commit bit for this pin
6	GPIO102	R/W	0h	Configuration lock commit bit for this pin
5	GPIO101	R/W	0h	Configuration lock commit bit for this pin
4	GPIO100	R/W	0h	Configuration lock commit bit for this pin
3	GPIO99	R/W	0h	Configuration lock commit bit for this pin
2	GPIO98	R/W	0h	Configuration lock commit bit for this pin
1	GPIO97	R/W	0h	Configuration lock commit bit for this pin
0	GPIO96	R/W	0h	Configuration lock commit bit for this pin

6.4.4.70 GPECTRL Register (offset = 100h) [reset = 0h]

GPECTRL is shown in [Figure 6-127](#) and described in [Table 6-134](#).

GPIO E Qualification Sampling Period Control (GPIO128 to 159)

Figure 6-127. GPECTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUALPRD3								QUALPRD2								QUALPRD1				QUALPRD0											
R/W-0h								R/W-0h								R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-134. GPECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	QUALPRD3	R/W	0h	Qualification sampling period for GPIO152 to GPIO159: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
23-16	QUALPRD2	R/W	0h	Qualification sampling period for GPIO144 to GPIO151: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
15-8	QUALPRD1	R/W	0h	Qualification sampling period for GPIO136 to GPIO143: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
7-0	QUALPRD0	R/W	0h	Qualification sampling period for GPIO128 to GPIO135: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510

6.4.4.71 GPEQSEL1 Register (offset = 102h) [reset = 0h]

GPEQSEL1 is shown in [Figure 6-128](#) and described in [Table 6-135](#).

GPIO E Qualifier Select 1 Register (GPIO128 to 143)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-128. GPEQSEL1 Register

31	30	29	28	27	26	25	24
GPIO143		GPIO142		GPIO141		GPIO140	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO139		GPIO138		GPIO137		GPIO136	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO135		GPIO134		GPIO133		GPIO132	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO131		GPIO130		GPIO129		GPIO128	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-135. GPEQSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO143	R/W	0h	Input qualification type
29-28	GPIO142	R/W	0h	Input qualification type
27-26	GPIO141	R/W	0h	Input qualification type
25-24	GPIO140	R/W	0h	Input qualification type
23-22	GPIO139	R/W	0h	Input qualification type
21-20	GPIO138	R/W	0h	Input qualification type
19-18	GPIO137	R/W	0h	Input qualification type
17-16	GPIO136	R/W	0h	Input qualification type
15-14	GPIO135	R/W	0h	Input qualification type
13-12	GPIO134	R/W	0h	Input qualification type
11-10	GPIO133	R/W	0h	Input qualification type
9-8	GPIO132	R/W	0h	Input qualification type
7-6	GPIO131	R/W	0h	Input qualification type
5-4	GPIO130	R/W	0h	Input qualification type
3-2	GPIO129	R/W	0h	Input qualification type
1-0	GPIO128	R/W	0h	Input qualification type

6.4.4.72 GPEQSEL2 Register (offset = 104h) [reset = 0h]

GPEQSEL2 is shown in [Figure 6-129](#) and described in [Table 6-136](#).

GPIO E Qualifier Select 2 Register (GPIO144 to 159)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-129. GPEQSEL2 Register

31	30	29	28	27	26	25	24
GPIO159		GPIO158		GPIO157		GPIO156	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO155		GPIO154		GPIO153		GPIO152	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO151		GPIO150		GPIO149		GPIO148	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO147		GPIO146		GPIO145		GPIO144	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-136. GPEQSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO159	R/W	0h	Input qualification type
29-28	GPIO158	R/W	0h	Input qualification type
27-26	GPIO157	R/W	0h	Input qualification type
25-24	GPIO156	R/W	0h	Input qualification type
23-22	GPIO155	R/W	0h	Input qualification type
21-20	GPIO154	R/W	0h	Input qualification type
19-18	GPIO153	R/W	0h	Input qualification type
17-16	GPIO152	R/W	0h	Input qualification type
15-14	GPIO151	R/W	0h	Input qualification type
13-12	GPIO150	R/W	0h	Input qualification type
11-10	GPIO149	R/W	0h	Input qualification type
9-8	GPIO148	R/W	0h	Input qualification type
7-6	GPIO147	R/W	0h	Input qualification type
5-4	GPIO146	R/W	0h	Input qualification type
3-2	GPIO145	R/W	0h	Input qualification type
1-0	GPIO144	R/W	0h	Input qualification type

6.4.4.73 GPEMUX1 Register (offset = 106h) [reset = 0h]

GPEMUX1 is shown in [Figure 6-130](#) and described in [Table 6-137](#).

GPIO E Mux 1 Register (GPIO128 to 143)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-130. GPEMUX1 Register

31	30	29	28	27	26	25	24
GPIO143		GPIO142		GPIO141		GPIO140	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO139		GPIO138		GPIO137		GPIO136	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO135		GPIO134		GPIO133		GPIO132	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO131		GPIO130		GPIO129		GPIO128	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-137. GPEMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO143	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO142	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO141	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO140	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO139	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO138	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO137	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO136	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO135	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO134	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO133	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO132	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO131	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO130	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO129	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO128	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.74 GPEMUX2 Register (offset = 108h) [reset = 0h]

GPEMUX2 is shown in [Figure 6-131](#) and described in [Table 6-138](#).

GPIO E Mux 2 Register (GPIO144 to 159)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-131. GPEMUX2 Register

31	30	29	28	27	26	25	24
GPIO159		GPIO158		GPIO157		GPIO156	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO155		GPIO154		GPIO153		GPIO152	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO151		GPIO150		GPIO149		GPIO148	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO147		GPIO146		GPIO145		GPIO144	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-138. GPEMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO159	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO158	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO157	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO156	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO155	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO154	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO153	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO152	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO151	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO150	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO149	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO148	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO147	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO146	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO145	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO144	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.75 GPEDIR Register (offset = 10Ah) [reset = 0h]

GPEDIR is shown in [Figure 6-132](#) and described in [Table 6-139](#).

GPIO E Direction Register (GPIO128 to 159)

Controls direction of GPIO pins when the specified pin is configured in GPIO mode.

0: Configures pin as input.

1: Configures pin as output.

Reading the register returns the current value of the register setting.

Figure 6-132. GPEDIR Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-139. GPEDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Defines direction for this pin in GPIO mode
30	GPIO158	R/W	0h	Defines direction for this pin in GPIO mode
29	GPIO157	R/W	0h	Defines direction for this pin in GPIO mode
28	GPIO156	R/W	0h	Defines direction for this pin in GPIO mode
27	GPIO155	R/W	0h	Defines direction for this pin in GPIO mode
26	GPIO154	R/W	0h	Defines direction for this pin in GPIO mode
25	GPIO153	R/W	0h	Defines direction for this pin in GPIO mode
24	GPIO152	R/W	0h	Defines direction for this pin in GPIO mode
23	GPIO151	R/W	0h	Defines direction for this pin in GPIO mode
22	GPIO150	R/W	0h	Defines direction for this pin in GPIO mode
21	GPIO149	R/W	0h	Defines direction for this pin in GPIO mode
20	GPIO148	R/W	0h	Defines direction for this pin in GPIO mode
19	GPIO147	R/W	0h	Defines direction for this pin in GPIO mode
18	GPIO146	R/W	0h	Defines direction for this pin in GPIO mode
17	GPIO145	R/W	0h	Defines direction for this pin in GPIO mode
16	GPIO144	R/W	0h	Defines direction for this pin in GPIO mode
15	GPIO143	R/W	0h	Defines direction for this pin in GPIO mode
14	GPIO142	R/W	0h	Defines direction for this pin in GPIO mode
13	GPIO141	R/W	0h	Defines direction for this pin in GPIO mode
12	GPIO140	R/W	0h	Defines direction for this pin in GPIO mode

Table 6-139. GPEDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO139	R/W	0h	Defines direction for this pin in GPIO mode
10	GPIO138	R/W	0h	Defines direction for this pin in GPIO mode
9	GPIO137	R/W	0h	Defines direction for this pin in GPIO mode
8	GPIO136	R/W	0h	Defines direction for this pin in GPIO mode
7	GPIO135	R/W	0h	Defines direction for this pin in GPIO mode
6	GPIO134	R/W	0h	Defines direction for this pin in GPIO mode
5	GPIO133	R/W	0h	Defines direction for this pin in GPIO mode
4	GPIO132	R/W	0h	Defines direction for this pin in GPIO mode
3	GPIO131	R/W	0h	Defines direction for this pin in GPIO mode
2	GPIO130	R/W	0h	Defines direction for this pin in GPIO mode
1	GPIO129	R/W	0h	Defines direction for this pin in GPIO mode
0	GPIO128	R/W	0h	Defines direction for this pin in GPIO mode

6.4.4.76 GPEPUD Register (offset = 10Ch) [reset = FFFFFFFFh]

GPEPUD is shown in [Figure 6-133](#) and described in [Table 6-140](#).

GPIO E Pull Up Disable Register (GPIO128 to 159)

Disables the Pull-Up on GPIO.

0: Enables the Pull-Up.

1: Disables the Pull-Up.

Reading the register returns the current value of the register setting.

Note:

[1] The Pull-Ups on the GPIO pins are disabled asynchronously when IORSn signal is low.

Figure 6-133. GPEPUD Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-1h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-1h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-1h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-140. GPEPUD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	1h	Pull-Up Disable control for this pin
30	GPIO158	R/W	1h	Pull-Up Disable control for this pin
29	GPIO157	R/W	1h	Pull-Up Disable control for this pin
28	GPIO156	R/W	1h	Pull-Up Disable control for this pin
27	GPIO155	R/W	1h	Pull-Up Disable control for this pin
26	GPIO154	R/W	1h	Pull-Up Disable control for this pin
25	GPIO153	R/W	1h	Pull-Up Disable control for this pin
24	GPIO152	R/W	1h	Pull-Up Disable control for this pin
23	GPIO151	R/W	1h	Pull-Up Disable control for this pin
22	GPIO150	R/W	1h	Pull-Up Disable control for this pin
21	GPIO149	R/W	1h	Pull-Up Disable control for this pin
20	GPIO148	R/W	1h	Pull-Up Disable control for this pin
19	GPIO147	R/W	1h	Pull-Up Disable control for this pin
18	GPIO146	R/W	1h	Pull-Up Disable control for this pin
17	GPIO145	R/W	1h	Pull-Up Disable control for this pin
16	GPIO144	R/W	1h	Pull-Up Disable control for this pin
15	GPIO143	R/W	1h	Pull-Up Disable control for this pin
14	GPIO142	R/W	1h	Pull-Up Disable control for this pin
13	GPIO141	R/W	1h	Pull-Up Disable control for this pin

Table 6-140. GPEPUD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	GPIO140	R/W	1h	Pull-Up Disable control for this pin
11	GPIO139	R/W	1h	Pull-Up Disable control for this pin
10	GPIO138	R/W	1h	Pull-Up Disable control for this pin
9	GPIO137	R/W	1h	Pull-Up Disable control for this pin
8	GPIO136	R/W	1h	Pull-Up Disable control for this pin
7	GPIO135	R/W	1h	Pull-Up Disable control for this pin
6	GPIO134	R/W	1h	Pull-Up Disable control for this pin
5	GPIO133	R/W	1h	Pull-Up Disable control for this pin
4	GPIO132	R/W	1h	Pull-Up Disable control for this pin
3	GPIO131	R/W	1h	Pull-Up Disable control for this pin
2	GPIO130	R/W	1h	Pull-Up Disable control for this pin
1	GPIO129	R/W	1h	Pull-Up Disable control for this pin
0	GPIO128	R/W	1h	Pull-Up Disable control for this pin

6.4.4.77 GPEINV Register (offset = 110h) [reset = 0h]

GPEINV is shown in [Figure 6-134](#) and described in [Table 6-141](#).

GPIO E Input Polarity Invert Registers (GPIO128 to 159)

Selects between non-inverted and inverted GPIO input to the device.

0: selects non-inverted GPIO input

1: selects inverted GPIO input

Reading the register returns the current value of the register setting.

Figure 6-134. GPEINV Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-141. GPEINV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Input inversion control for this pin
30	GPIO158	R/W	0h	Input inversion control for this pin
29	GPIO157	R/W	0h	Input inversion control for this pin
28	GPIO156	R/W	0h	Input inversion control for this pin
27	GPIO155	R/W	0h	Input inversion control for this pin
26	GPIO154	R/W	0h	Input inversion control for this pin
25	GPIO153	R/W	0h	Input inversion control for this pin
24	GPIO152	R/W	0h	Input inversion control for this pin
23	GPIO151	R/W	0h	Input inversion control for this pin
22	GPIO150	R/W	0h	Input inversion control for this pin
21	GPIO149	R/W	0h	Input inversion control for this pin
20	GPIO148	R/W	0h	Input inversion control for this pin
19	GPIO147	R/W	0h	Input inversion control for this pin
18	GPIO146	R/W	0h	Input inversion control for this pin
17	GPIO145	R/W	0h	Input inversion control for this pin
16	GPIO144	R/W	0h	Input inversion control for this pin
15	GPIO143	R/W	0h	Input inversion control for this pin
14	GPIO142	R/W	0h	Input inversion control for this pin
13	GPIO141	R/W	0h	Input inversion control for this pin
12	GPIO140	R/W	0h	Input inversion control for this pin

Table 6-141. GPEINV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO139	R/W	0h	Input inversion control for this pin
10	GPIO138	R/W	0h	Input inversion control for this pin
9	GPIO137	R/W	0h	Input inversion control for this pin
8	GPIO136	R/W	0h	Input inversion control for this pin
7	GPIO135	R/W	0h	Input inversion control for this pin
6	GPIO134	R/W	0h	Input inversion control for this pin
5	GPIO133	R/W	0h	Input inversion control for this pin
4	GPIO132	R/W	0h	Input inversion control for this pin
3	GPIO131	R/W	0h	Input inversion control for this pin
2	GPIO130	R/W	0h	Input inversion control for this pin
1	GPIO129	R/W	0h	Input inversion control for this pin
0	GPIO128	R/W	0h	Input inversion control for this pin

6.4.4.78 GPEODR Register (offset = 112h) [reset = 0h]

GPEODR is shown in [Figure 6-135](#) and described in [Table 6-142](#).

GPIO E Open Drain Output Register (GPIO128 to GPIO159)

Selects between normal and open-drain output for the GPIO pin.

0: Normal Output

1: Open Drain Output

Reading the register returns the current value of the register setting.

Note:

[1] In the Open Drain output mode, if the buffer is configured for output mode, a 0 value to be driven out comes out on the on the PAD while a 1 value to be driven out tri-states the buffer.

Figure 6-135. GPEODR Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-142. GPEODR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Output Open-Drain control for this pin
30	GPIO158	R/W	0h	Output Open-Drain control for this pin
29	GPIO157	R/W	0h	Output Open-Drain control for this pin
28	GPIO156	R/W	0h	Output Open-Drain control for this pin
27	GPIO155	R/W	0h	Output Open-Drain control for this pin
26	GPIO154	R/W	0h	Output Open-Drain control for this pin
25	GPIO153	R/W	0h	Output Open-Drain control for this pin
24	GPIO152	R/W	0h	Output Open-Drain control for this pin
23	GPIO151	R/W	0h	Output Open-Drain control for this pin
22	GPIO150	R/W	0h	Output Open-Drain control for this pin
21	GPIO149	R/W	0h	Output Open-Drain control for this pin
20	GPIO148	R/W	0h	Output Open-Drain control for this pin
19	GPIO147	R/W	0h	Output Open-Drain control for this pin
18	GPIO146	R/W	0h	Output Open-Drain control for this pin
17	GPIO145	R/W	0h	Output Open-Drain control for this pin
16	GPIO144	R/W	0h	Output Open-Drain control for this pin
15	GPIO143	R/W	0h	Output Open-Drain control for this pin
14	GPIO142	R/W	0h	Output Open-Drain control for this pin

Table 6-142. GPEODR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO141	R/W	0h	Output Open-Drain control for this pin
12	GPIO140	R/W	0h	Output Open-Drain control for this pin
11	GPIO139	R/W	0h	Output Open-Drain control for this pin
10	GPIO138	R/W	0h	Output Open-Drain control for this pin
9	GPIO137	R/W	0h	Output Open-Drain control for this pin
8	GPIO136	R/W	0h	Output Open-Drain control for this pin
7	GPIO135	R/W	0h	Output Open-Drain control for this pin
6	GPIO134	R/W	0h	Output Open-Drain control for this pin
5	GPIO133	R/W	0h	Output Open-Drain control for this pin
4	GPIO132	R/W	0h	Output Open-Drain control for this pin
3	GPIO131	R/W	0h	Output Open-Drain control for this pin
2	GPIO130	R/W	0h	Output Open-Drain control for this pin
1	GPIO129	R/W	0h	Output Open-Drain control for this pin
0	GPIO128	R/W	0h	Output Open-Drain control for this pin

6.4.4.79 GPEGMUX1 Register (offset = 120h) [reset = 0h]

GPEGMUX1 is shown in [Figure 6-136](#) and described in [Table 6-143](#).

GPIO E Peripheral Group Mux (GPIO128 to 143)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-136. GPEGMUX1 Register

31	30	29	28	27	26	25	24
GPIO143		GPIO142		GPIO141		GPIO140	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO139		GPIO138		GPIO137		GPIO136	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO135		GPIO134		GPIO133		GPIO132	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO131		GPIO130		GPIO129		GPIO128	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-143. GPEGMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO143	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO142	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO141	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO140	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO139	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO138	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO137	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO136	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO135	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO134	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO133	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO132	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO131	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO130	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO129	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO128	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.80 GPEGMUX2 Register (offset = 122h) [reset = 0h]

GPEGMUX2 is shown in [Figure 6-137](#) and described in [Table 6-144](#).

GPIO E Peripheral Group Mux (GPIO144 to 159)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-137. GPEGMUX2 Register

31	30	29	28	27	26	25	24
GPIO159		GPIO158		GPIO157		GPIO156	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
GPIO155		GPIO154		GPIO153		GPIO152	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
GPIO151		GPIO150		GPIO149		GPIO148	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO147		GPIO146		GPIO145		GPIO144	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-144. GPEGMUX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	GPIO159	R/W	0h	Defines pin-muxing selection for GPIO
29-28	GPIO158	R/W	0h	Defines pin-muxing selection for GPIO
27-26	GPIO157	R/W	0h	Defines pin-muxing selection for GPIO
25-24	GPIO156	R/W	0h	Defines pin-muxing selection for GPIO
23-22	GPIO155	R/W	0h	Defines pin-muxing selection for GPIO
21-20	GPIO154	R/W	0h	Defines pin-muxing selection for GPIO
19-18	GPIO153	R/W	0h	Defines pin-muxing selection for GPIO
17-16	GPIO152	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO151	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO150	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO149	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO148	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO147	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO146	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO145	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO144	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.81 GPECSEL1 Register (offset = 128h) [reset = 0h]

GPECSEL1 is shown in [Figure 6-138](#) and described in [Table 6-145](#).

GPIO E Core Select Register (GPIO128 to 135)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-138. GPECSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO135				GPIO134				GPIO133				GPIO132			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO131				GPIO130				GPIO129				GPIO128			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-145. GPECSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO135	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO134	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO133	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO132	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO131	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO130	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO129	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO128	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.82 GPECSEL2 Register (offset = 12Ah) [reset = 0h]

GPECSEL2 is shown in [Figure 6-139](#) and described in [Table 6-146](#).

GPIO E Core Select Register (GPIO136 to 143)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-139. GPECSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO143				GPIO142				GPIO141				GPIO140			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO139				GPIO138				GPIO137				GPIO136			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-146. GPECSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO143	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO142	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO141	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO140	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO139	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO138	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO137	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO136	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.83 GPECSEL3 Register (offset = 12Ch) [reset = 0h]

GPECSEL3 is shown in [Figure 6-140](#) and described in [Table 6-147](#).

GPIO E Core Select Register (GPIO144 to 151)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-140. GPECSEL3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO151				GPIO150				GPIO149				GPIO148			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO147				GPIO146				GPIO145				GPIO144			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-147. GPECSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO151	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO150	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO149	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO148	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO147	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO146	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO145	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO144	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.84 GPECSEL4 Register (offset = 12Eh) [reset = 0h]

GPECSEL4 is shown in [Figure 6-141](#) and described in [Table 6-148](#).

GPIO E Core Select Register (GPIO152 to 159)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-141. GPECSEL4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO159				GPIO158				GPIO157				GPIO156			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO155				GPIO154				GPIO153				GPIO152			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-148. GPECSEL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO159	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO158	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO157	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO156	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO155	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO154	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO153	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO152	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.85 GPELOCK Register (offset = 13Ch) [reset = 0h]

GPELOCK is shown in [Figure 6-142](#) and described in [Table 6-149](#).

GPIO E Lock Configuration Register (GPIO128 to 159)

GPIO Configuration Lock for GPIO.

0: Bits in GPYMUX1, GPYMUX2, GPYDIR, GPYINV, GPYODR, GPYAMSEL, GPYGMUX1, GPYGMUX2 and GPYCSELx register which control the same pin can be changed

1: Locks changes to the bits in GPYMUX1, GPYMUX2, GPYDIR, GPYINV, GPYODR, GPYAMSEL, GPYGMUX1, GPYGMUX2 and GPYCSELx registers which control the same pin

Figure 6-142. GPELOCK Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-149. GPELOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Configuration Lock bit for this pin
30	GPIO158	R/W	0h	Configuration Lock bit for this pin
29	GPIO157	R/W	0h	Configuration Lock bit for this pin
28	GPIO156	R/W	0h	Configuration Lock bit for this pin
27	GPIO155	R/W	0h	Configuration Lock bit for this pin
26	GPIO154	R/W	0h	Configuration Lock bit for this pin
25	GPIO153	R/W	0h	Configuration Lock bit for this pin
24	GPIO152	R/W	0h	Configuration Lock bit for this pin
23	GPIO151	R/W	0h	Configuration Lock bit for this pin
22	GPIO150	R/W	0h	Configuration Lock bit for this pin
21	GPIO149	R/W	0h	Configuration Lock bit for this pin
20	GPIO148	R/W	0h	Configuration Lock bit for this pin
19	GPIO147	R/W	0h	Configuration Lock bit for this pin
18	GPIO146	R/W	0h	Configuration Lock bit for this pin
17	GPIO145	R/W	0h	Configuration Lock bit for this pin
16	GPIO144	R/W	0h	Configuration Lock bit for this pin
15	GPIO143	R/W	0h	Configuration Lock bit for this pin
14	GPIO142	R/W	0h	Configuration Lock bit for this pin
13	GPIO141	R/W	0h	Configuration Lock bit for this pin
12	GPIO140	R/W	0h	Configuration Lock bit for this pin

Table 6-149. GPELOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	GPIO139	R/W	0h	Configuration Lock bit for this pin
10	GPIO138	R/W	0h	Configuration Lock bit for this pin
9	GPIO137	R/W	0h	Configuration Lock bit for this pin
8	GPIO136	R/W	0h	Configuration Lock bit for this pin
7	GPIO135	R/W	0h	Configuration Lock bit for this pin
6	GPIO134	R/W	0h	Configuration Lock bit for this pin
5	GPIO133	R/W	0h	Configuration Lock bit for this pin
4	GPIO132	R/W	0h	Configuration Lock bit for this pin
3	GPIO131	R/W	0h	Configuration Lock bit for this pin
2	GPIO130	R/W	0h	Configuration Lock bit for this pin
1	GPIO129	R/W	0h	Configuration Lock bit for this pin
0	GPIO128	R/W	0h	Configuration Lock bit for this pin

6.4.4.86 GPECR Register (offset = 13Eh) [reset = 0h]

GPECR is shown in [Figure 6-143](#) and described in [Table 6-150](#).

GPIO E Lock Commit Register (GPIO128 to 159)

GPIO Configuration Lock Commit for GPIO:

1: Locks changes to the bit in GPyLOCK register which controls the same pin

0: Bit in the GPyLOCK register which controls the same pin can be changed

Figure 6-143. GPECR Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-150. GPECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Configuration lock commit bit for this pin
30	GPIO158	R/W	0h	Configuration lock commit bit for this pin
29	GPIO157	R/W	0h	Configuration lock commit bit for this pin
28	GPIO156	R/W	0h	Configuration lock commit bit for this pin
27	GPIO155	R/W	0h	Configuration lock commit bit for this pin
26	GPIO154	R/W	0h	Configuration lock commit bit for this pin
25	GPIO153	R/W	0h	Configuration lock commit bit for this pin
24	GPIO152	R/W	0h	Configuration lock commit bit for this pin
23	GPIO151	R/W	0h	Configuration lock commit bit for this pin
22	GPIO150	R/W	0h	Configuration lock commit bit for this pin
21	GPIO149	R/W	0h	Configuration lock commit bit for this pin
20	GPIO148	R/W	0h	Configuration lock commit bit for this pin
19	GPIO147	R/W	0h	Configuration lock commit bit for this pin
18	GPIO146	R/W	0h	Configuration lock commit bit for this pin
17	GPIO145	R/W	0h	Configuration lock commit bit for this pin
16	GPIO144	R/W	0h	Configuration lock commit bit for this pin
15	GPIO143	R/W	0h	Configuration lock commit bit for this pin
14	GPIO142	R/W	0h	Configuration lock commit bit for this pin
13	GPIO141	R/W	0h	Configuration lock commit bit for this pin
12	GPIO140	R/W	0h	Configuration lock commit bit for this pin
11	GPIO139	R/W	0h	Configuration lock commit bit for this pin

Table 6-150. GPECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO138	R/W	0h	Configuration lock commit bit for this pin
9	GPIO137	R/W	0h	Configuration lock commit bit for this pin
8	GPIO136	R/W	0h	Configuration lock commit bit for this pin
7	GPIO135	R/W	0h	Configuration lock commit bit for this pin
6	GPIO134	R/W	0h	Configuration lock commit bit for this pin
5	GPIO133	R/W	0h	Configuration lock commit bit for this pin
4	GPIO132	R/W	0h	Configuration lock commit bit for this pin
3	GPIO131	R/W	0h	Configuration lock commit bit for this pin
2	GPIO130	R/W	0h	Configuration lock commit bit for this pin
1	GPIO129	R/W	0h	Configuration lock commit bit for this pin
0	GPIO128	R/W	0h	Configuration lock commit bit for this pin

6.4.4.87 GPFCTRL Register (offset = 140h) [reset = 0h]

GPFCTRL is shown in [Figure 6-144](#) and described in [Table 6-151](#).

GPIO F Qualification Sampling Period Control (GPIO160 to 168)

Figure 6-144. GPFCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED								QUALPRD1				QUALPRD0											
R-0h								R-0h								R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-151. GPFCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	RESERVED	R	0h	Reserved
15-8	QUALPRD1	R/W	0h	Qualification sampling period for GPIO168: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510
7-0	QUALPRD0	R/W	0h	Qualification sampling period for GPIO160 to GPIO167: 0x00,QUALPRDx = PLLSYSCLK 0x01,QUALPRDx = PLLSYSCLK/2 0x02,QUALPRDx = PLLSYSCLK/4 0xFF,QUALPRDx = PLLSYSCLK/510

6.4.4.88 GPFQSEL1 Register (offset = 142h) [reset = 0h]

GPFQSEL1 is shown in [Figure 6-145](#) and described in [Table 6-152](#).

GPIO F Qualifier Select 1 Register (GPIO160 to 168)

Input qualification type:

0,0 Sync

0,1 Qualification (3 samples)

1,0 Qualification (6 samples)

1,1 Async (no Sync or Qualification)

Figure 6-145. GPFQSEL1 Register

31	30	29	28	27	26	25	24
RESERVED		RESERVED		RESERVED		RESERVED	
	R-0h		R-0h		R-0h		R-0h
23	22	21	20	19	18	17	16
RESERVED		RESERVED		RESERVED		GPIO168	
	R-0h		R-0h		R-0h		R/W-0h
15	14	13	12	11	10	9	8
GPIO167		GPIO166		GPIO165		GPIO164	
	R/W-0h		R/W-0h		R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
GPIO163		GPIO162		GPIO161		GPIO160	
	R/W-0h		R/W-0h		R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-152. GPFQSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	RESERVED	R	0h	Reserved
27-26	RESERVED	R	0h	Reserved
25-24	RESERVED	R	0h	Reserved
23-22	RESERVED	R	0h	Reserved
21-20	RESERVED	R	0h	Reserved
19-18	RESERVED	R	0h	Reserved
17-16	GPIO168	R/W	0h	Input qualification type
15-14	GPIO167	R/W	0h	Input qualification type
13-12	GPIO166	R/W	0h	Input qualification type
11-10	GPIO165	R/W	0h	Input qualification type
9-8	GPIO164	R/W	0h	Input qualification type
7-6	GPIO163	R/W	0h	Input qualification type
5-4	GPIO162	R/W	0h	Input qualification type
3-2	GPIO161	R/W	0h	Input qualification type
1-0	GPIO160	R/W	0h	Input qualification type

6.4.4.89 GPFMUX1 Register (offset = 146h) [reset = 0h]

GPFMUX1 is shown in [Figure 6-146](#) and described in [Table 6-153](#).

GPIO F Mux 1 Register (GPIO160 to 168)

Defines pin-muxing selection for GPIO.

Notes:

The respective GPyGMUXn.GPIOz must be configured prior to this register to avoid intermediate peripheral selects being mapped to the GPIO. Refer to GPIO chapter for more details.

Figure 6-146. GPFMUX1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPIO168	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h	
15	14	13	12	11	10	9	8
GPIO167		GPIO166		GPIO165		GPIO164	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO163		GPIO162		GPIO161		GPIO160	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-153. GPFMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	RESERVED	R	0h	Reserved
27-26	RESERVED	R	0h	Reserved
25-24	RESERVED	R	0h	Reserved
23-22	RESERVED	R	0h	Reserved
21-20	RESERVED	R	0h	Reserved
19-18	RESERVED	R	0h	Reserved
17-16	GPIO168	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO167	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO166	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO165	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO164	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO163	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO162	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO161	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO160	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.90 GPFDIR Register (offset = 14Ah) [reset = 0h]

GPFDIR is shown in [Figure 6-147](#) and described in [Table 6-154](#).

GPIO F Direction Register (GPIO160 to 168)

Controls direction of GPIO pins when the specified pin is configured in GPIO mode.

0: Configures pin as input.

1: Configures pin as output.

Reading the register returns the current value of the register setting.

Figure 6-147. GPFDIR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	GPIO168						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-154. GPFDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	0h	Defines direction for this pin in GPIO mode

Table 6-154. GPFDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	GPIO167	R/W	0h	Defines direction for this pin in GPIO mode
6	GPIO166	R/W	0h	Defines direction for this pin in GPIO mode
5	GPIO165	R/W	0h	Defines direction for this pin in GPIO mode
4	GPIO164	R/W	0h	Defines direction for this pin in GPIO mode
3	GPIO163	R/W	0h	Defines direction for this pin in GPIO mode
2	GPIO162	R/W	0h	Defines direction for this pin in GPIO mode
1	GPIO161	R/W	0h	Defines direction for this pin in GPIO mode
0	GPIO160	R/W	0h	Defines direction for this pin in GPIO mode

6.4.4.91 GPFPUD Register (offset = 14Ch) [reset = FFFFFFFFh]

GPFPUD is shown in [Figure 6-148](#) and described in [Table 6-155](#).

GPIO F Pull Up Disable Register (GPIO160 to 168)

Disables the Pull-Up on GPIO.

0: Enables the Pull-Up.

1: Disables the Pull-Up.

Reading the register returns the current value of the register setting.

Note:

[1] The Pull-Ups on the GPIO pins are disabled asynchronously when IORSn signal is low.

Figure 6-148. GPFPUD Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	GPIO168						
R-0h	R/W-1h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-155. GPFPUD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved

Table 6-155. GPFPUD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	1h	Pull-Up Disable control for this pin
7	GPIO167	R/W	1h	Pull-Up Disable control for this pin
6	GPIO166	R/W	1h	Pull-Up Disable control for this pin
5	GPIO165	R/W	1h	Pull-Up Disable control for this pin
4	GPIO164	R/W	1h	Pull-Up Disable control for this pin
3	GPIO163	R/W	1h	Pull-Up Disable control for this pin
2	GPIO162	R/W	1h	Pull-Up Disable control for this pin
1	GPIO161	R/W	1h	Pull-Up Disable control for this pin
0	GPIO160	R/W	1h	Pull-Up Disable control for this pin

6.4.4.92 GPFINV Register (offset = 150h) [reset = 0h]

GPFINV is shown in [Figure 6-149](#) and described in [Table 6-156](#).

GPIO F Input Polarity Invert Registers (GPIO160 to 168)

Selects between non-inverted and inverted GPIO input to the device.

0: selects non-inverted GPIO input

1: selects inverted GPIO input

Reading the register returns the current value of the register setting.

Figure 6-149. GPFINV Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	GPIO168						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-156. GPFINV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	0h	Input inversion control for this pin

Table 6-156. GPFINV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	GPIO167	R/W	0h	Input inversion control for this pin
6	GPIO166	R/W	0h	Input inversion control for this pin
5	GPIO165	R/W	0h	Input inversion control for this pin
4	GPIO164	R/W	0h	Input inversion control for this pin
3	GPIO163	R/W	0h	Input inversion control for this pin
2	GPIO162	R/W	0h	Input inversion control for this pin
1	GPIO161	R/W	0h	Input inversion control for this pin
0	GPIO160	R/W	0h	Input inversion control for this pin

6.4.4.93 GPFODR Register (offset = 152h) [reset = 0h]

GPFODR is shown in [Figure 6-150](#) and described in [Table 6-157](#).

GPIO F Open Drain Output Register (GPIO160 to GPIO168)

Selects between normal and open-drain output for the GPIO pin.

0: Normal Output

1: Open Drain Output

Reading the register returns the current value of the register setting.

Note:

[1] In the Open Drain output mode, if the buffer is configured for output mode, a 0 value to be driven out comes out on the on the PAD while a 1 value to be driven out tri-states the buffer.

Figure 6-150. GPFODR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	GPIO168						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-157. GPFODR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved

Table 6-157. GPFODR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	0h	Output Open-Drain control for this pin
7	GPIO167	R/W	0h	Output Open-Drain control for this pin
6	GPIO166	R/W	0h	Output Open-Drain control for this pin
5	GPIO165	R/W	0h	Output Open-Drain control for this pin
4	GPIO164	R/W	0h	Output Open-Drain control for this pin
3	GPIO163	R/W	0h	Output Open-Drain control for this pin
2	GPIO162	R/W	0h	Output Open-Drain control for this pin
1	GPIO161	R/W	0h	Output Open-Drain control for this pin
0	GPIO160	R/W	0h	Output Open-Drain control for this pin

6.4.4.94 GPFGMUX1 Register (offset = 160h) [reset = 0h]

GPFGMUX1 is shown in [Figure 6-151](#) and described in [Table 6-158](#).

GPIO F Peripheral Group Mux (GPIO160 to 168)

Defines pin-muxing selection for GPIO.

Notes:

[1]For complete pin-mux selection on GPIOx, GPAMUXy.GPIOx configuration is also required. Refer to GPIO specification for more details

Figure 6-151. GPFGMUX1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPIO168	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h	
15	14	13	12	11	10	9	8
GPIO167		GPIO166		GPIO165		GPIO164	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
GPIO163		GPIO162		GPIO161		GPIO160	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-158. GPFGMUX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	RESERVED	R	0h	Reserved
27-26	RESERVED	R	0h	Reserved
25-24	RESERVED	R	0h	Reserved
23-22	RESERVED	R	0h	Reserved
21-20	RESERVED	R	0h	Reserved
19-18	RESERVED	R	0h	Reserved
17-16	GPIO168	R/W	0h	Defines pin-muxing selection for GPIO
15-14	GPIO167	R/W	0h	Defines pin-muxing selection for GPIO
13-12	GPIO166	R/W	0h	Defines pin-muxing selection for GPIO
11-10	GPIO165	R/W	0h	Defines pin-muxing selection for GPIO
9-8	GPIO164	R/W	0h	Defines pin-muxing selection for GPIO
7-6	GPIO163	R/W	0h	Defines pin-muxing selection for GPIO
5-4	GPIO162	R/W	0h	Defines pin-muxing selection for GPIO
3-2	GPIO161	R/W	0h	Defines pin-muxing selection for GPIO
1-0	GPIO160	R/W	0h	Defines pin-muxing selection for GPIO

6.4.4.95 GPFCSEL1 Register (offset = 168h) [reset = 0h]

GPFCSEL1 is shown in [Figure 6-152](#) and described in [Table 6-159](#).

GPIO F Core Select Register (GPIO160 to 167)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-152. GPFCSEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIO167				GPIO166				GPIO165				GPIO164			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO163				GPIO162				GPIO161				GPIO160			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-159. GPFCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GPIO167	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
27-24	GPIO166	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
23-20	GPIO165	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
19-16	GPIO164	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
15-12	GPIO163	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
11-8	GPIO162	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
7-4	GPIO161	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin
3-0	GPIO160	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.96 GPFCSEL2 Register (offset = 16Ah) [reset = 0h]

GPFCSEL2 is shown in [Figure 6-153](#) and described in [Table 6-160](#).

GPIO F Core Select Register (GPIO168)

Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

xx00: CPU1 selected

xx01: CPU1.CLA1 selected

xx10: CPU2 selected

xx11: CPU2.CLA1 selected

Figure 6-153. GPFCSEL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h				R-0h				R-0h				R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				GPIO168			
R-0h				R-0h				R-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-160. GPFCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	RESERVED	R	0h	Reserved
23-20	RESERVED	R	0h	Reserved
19-16	RESERVED	R	0h	Reserved
15-12	RESERVED	R	0h	Reserved
11-8	RESERVED	R	0h	Reserved
7-4	RESERVED	R	0h	Reserved
3-0	GPIO168	R/W	0h	Selects which master's GPIODAT/SET/CLEAR/TOGGLE registers control this GPIO pin

6.4.4.97 GPFLOCK Register (offset = 17Ch) [reset = 0h]

GPFLOCK is shown in [Figure 6-154](#) and described in [Table 6-161](#).

GPIO F Lock Configuration Register (GPIO160 to 168)

GPIO Configuration Lock for GPIO.

0: Bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx register which control the same pin can be changed

1: Locks changes to the bits in GPyMUX1, GPyMUX2, GPyDIR, GPyINV, GPyODR, GPyAMSEL, GPyGMUX1, GPyGMUX2 and GPyCSELx registers which control the same pin

Figure 6-154. GPFLOCK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-161. GPFLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved

Table 6-161. GPFLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	GPIO168	R/W	0h	Configuration Lock bit for this pin
7	GPIO167	R/W	0h	Configuration Lock bit for this pin
6	GPIO166	R/W	0h	Configuration Lock bit for this pin
5	GPIO165	R/W	0h	Configuration Lock bit for this pin
4	GPIO164	R/W	0h	Configuration Lock bit for this pin
3	GPIO163	R/W	0h	Configuration Lock bit for this pin
2	GPIO162	R/W	0h	Configuration Lock bit for this pin
1	GPIO161	R/W	0h	Configuration Lock bit for this pin
0	GPIO160	R/W	0h	Configuration Lock bit for this pin

6.4.4.98 GPFCSR Register (offset = 17Eh) [reset = 0h]

GPFCSR is shown in [Figure 6-155](#) and described in [Table 6-162](#).

GPIO F Lock Commit Register (GPIO160 to 168)

GPIO Configuration Lock Commit for GPIO:

1: Locks changes to the bit in GPyLOCK register which controls the same pin

0: Bit in the GPyLOCK register which controls the same pin can be changed

Figure 6-155. GPFCSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	GPIO168						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-162. GPFCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	0h	Configuration lock commit bit for this pin
7	GPIO167	R/W	0h	Configuration lock commit bit for this pin

Table 6-162. GPFCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	GPIO166	R/W	0h	Configuration lock commit bit for this pin
5	GPIO165	R/W	0h	Configuration lock commit bit for this pin
4	GPIO164	R/W	0h	Configuration lock commit bit for this pin
3	GPIO163	R/W	0h	Configuration lock commit bit for this pin
2	GPIO162	R/W	0h	Configuration lock commit bit for this pin
1	GPIO161	R/W	0h	Configuration lock commit bit for this pin
0	GPIO160	R/W	0h	Configuration lock commit bit for this pin

6.4.5 GPIO_DATA_REGS Registers

Table 6-163 lists the memory-mapped registers for the GPIO_DATA_REGS. All register offset addresses not listed in Table 6-163 should be considered as reserved locations and the register contents should not be modified.

Table 6-163. GPIO_DATA_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	GPADAT	GPIO A Data Register (GPIO0 to 31)	Section 6.4.5.1	
2h	GPASET	GPIO A Data Set Register (GPIO0 to 31)	Section 6.4.5.2	
4h	GPACLEAR	GPIO A Data Clear Register (GPIO0 to 31)	Section 6.4.5.3	
6h	GPATOGGLE	GPIO A Data Toggle Register (GPIO0 to 31)	Section 6.4.5.4	
8h	GPBDAT	GPIO B Data Register (GPIO32 to 63)	Section 6.4.5.5	
Ah	GPBSET	GPIO B Data Set Register (GPIO32 to 63)	Section 6.4.5.6	
Ch	GPBCLEAR	GPIO B Data Clear Register (GPIO32 to 63)	Section 6.4.5.7	
Eh	GPBToggle	GPIO B Data Toggle Register (GPIO32 to 63)	Section 6.4.5.8	
10h	GPCDAT	GPIO C Data Register (GPIO64 to 95)	Section 6.4.5.9	
12h	GPCSET	GPIO C Data Set Register (GPIO64 to 95)	Section 6.4.5.10	
14h	GPCCLEAR	GPIO C Data Clear Register (GPIO64 to 95)	Section 6.4.5.11	
16h	GPCTOGGLE	GPIO C Data Toggle Register (GPIO64 to 95)	Section 6.4.5.12	
18h	GPDDAT	GPIO D Data Register (GPIO96 to 127)	Section 6.4.5.13	
1Ah	GPDSET	GPIO D Data Set Register (GPIO96 to 127)	Section 6.4.5.14	
1Ch	GPDCLEAR	GPIO D Data Clear Register (GPIO96 to 127)	Section 6.4.5.15	
1Eh	GPDToggle	GPIO D Data Toggle Register (GPIO96 to 127)	Section 6.4.5.16	
20h	GPEDAT	GPIO E Data Register (GPIO128 to 159)	Section 6.4.5.17	
22h	GPESET	GPIO E Data Set Register (GPIO128 to 159)	Section 6.4.5.18	
24h	GPECLEAR	GPIO E Data Clear Register (GPIO128 to 159)	Section 6.4.5.19	
26h	GPETOGGLE	GPIO E Data Toggle Register (GPIO128 to 159)	Section 6.4.5.20	
28h	GPFDAT	GPIO F Data Register (GPIO160 to 168)	Section 6.4.5.21	
2Ah	GPFSET	GPIO F Data Set Register (GPIO160 to 168)	Section 6.4.5.22	
2Ch	GPFCLEAR	GPIO F Data Clear Register (GPIO160 to 168)	Section 6.4.5.23	
2Eh	GPFTOGGLE	GPIO F Data Toggle Register (GPIO160 to 168)	Section 6.4.5.24	

6.4.5.1 GPADAT Register (offset = 0h) [reset = 0h]

GPADAT is shown in [Figure 6-156](#) and described in [Table 6-164](#).

GPIO A Data Register (GPIO0 to 31)

Reading this register indicates the current status of the GPIO pin, irrespective of which mode the pin is in. Writing to this register will set the GPIO pin high or low if the pin is enabled for GPIO output mode, otherwise the value written is latched but ignored. The state of the output register latch will remain in its current state until the next write operation. A system reset will clear all bits and latched values to zero.

DESIGNER NOTE:

[1] Reading the GPIODAT register should reflect the state of the PIN (after qualification), not the state of the output latch of the GPIODAT register.

Figure 6-156. GPADAT Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-164. GPADAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Data Register for this pin
30	GPIO30	R/W	0h	Data Register for this pin
29	GPIO29	R/W	0h	Data Register for this pin
28	GPIO28	R/W	0h	Data Register for this pin
27	GPIO27	R/W	0h	Data Register for this pin
26	GPIO26	R/W	0h	Data Register for this pin
25	GPIO25	R/W	0h	Data Register for this pin
24	GPIO24	R/W	0h	Data Register for this pin
23	GPIO23	R/W	0h	Data Register for this pin
22	GPIO22	R/W	0h	Data Register for this pin
21	GPIO21	R/W	0h	Data Register for this pin
20	GPIO20	R/W	0h	Data Register for this pin
19	GPIO19	R/W	0h	Data Register for this pin
18	GPIO18	R/W	0h	Data Register for this pin
17	GPIO17	R/W	0h	Data Register for this pin
16	GPIO16	R/W	0h	Data Register for this pin
15	GPIO15	R/W	0h	Data Register for this pin
14	GPIO14	R/W	0h	Data Register for this pin

Table 6-164. GPADAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO13	R/W	0h	Data Register for this pin
12	GPIO12	R/W	0h	Data Register for this pin
11	GPIO11	R/W	0h	Data Register for this pin
10	GPIO10	R/W	0h	Data Register for this pin
9	GPIO9	R/W	0h	Data Register for this pin
8	GPIO8	R/W	0h	Data Register for this pin
7	GPIO7	R/W	0h	Data Register for this pin
6	GPIO6	R/W	0h	Data Register for this pin
5	GPIO5	R/W	0h	Data Register for this pin
4	GPIO4	R/W	0h	Data Register for this pin
3	GPIO3	R/W	0h	Data Register for this pin
2	GPIO2	R/W	0h	Data Register for this pin
1	GPIO1	R/W	0h	Data Register for this pin
0	GPIO0	R/W	0h	Data Register for this pin

6.4.5.2 GPASET Register (offset = 2h) [reset = 0h]

GPASET is shown in [Figure 6-157](#) and described in [Table 6-165](#).

GPIO A Data Set Register (GPIO0 to 31)

Writing a 1 will force GPIO output data latch to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-157. GPASET Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-165. GPASET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Output Set bit for this pin
30	GPIO30	R/W	0h	Output Set bit for this pin
29	GPIO29	R/W	0h	Output Set bit for this pin
28	GPIO28	R/W	0h	Output Set bit for this pin
27	GPIO27	R/W	0h	Output Set bit for this pin
26	GPIO26	R/W	0h	Output Set bit for this pin
25	GPIO25	R/W	0h	Output Set bit for this pin
24	GPIO24	R/W	0h	Output Set bit for this pin
23	GPIO23	R/W	0h	Output Set bit for this pin
22	GPIO22	R/W	0h	Output Set bit for this pin
21	GPIO21	R/W	0h	Output Set bit for this pin
20	GPIO20	R/W	0h	Output Set bit for this pin
19	GPIO19	R/W	0h	Output Set bit for this pin
18	GPIO18	R/W	0h	Output Set bit for this pin
17	GPIO17	R/W	0h	Output Set bit for this pin
16	GPIO16	R/W	0h	Output Set bit for this pin
15	GPIO15	R/W	0h	Output Set bit for this pin
14	GPIO14	R/W	0h	Output Set bit for this pin
13	GPIO13	R/W	0h	Output Set bit for this pin
12	GPIO12	R/W	0h	Output Set bit for this pin
11	GPIO11	R/W	0h	Output Set bit for this pin

Table 6-165. GPASET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO10	R/W	0h	Output Set bit for this pin
9	GPIO9	R/W	0h	Output Set bit for this pin
8	GPIO8	R/W	0h	Output Set bit for this pin
7	GPIO7	R/W	0h	Output Set bit for this pin
6	GPIO6	R/W	0h	Output Set bit for this pin
5	GPIO5	R/W	0h	Output Set bit for this pin
4	GPIO4	R/W	0h	Output Set bit for this pin
3	GPIO3	R/W	0h	Output Set bit for this pin
2	GPIO2	R/W	0h	Output Set bit for this pin
1	GPIO1	R/W	0h	Output Set bit for this pin
0	GPIO0	R/W	0h	Output Set bit for this pin

6.4.5.3 GPACLEAR Register (offset = 4h) [reset = 0h]

GPACLEAR is shown in [Figure 6-158](#) and described in [Table 6-166](#).

GPIO A Data Clear Register (GPIO0 to 31)

Writing a 1 will force GPIO0 output data latch to 0.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-158. GPACLEAR Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-166. GPACLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Output Clear bit for this pin
30	GPIO30	R/W	0h	Output Clear bit for this pin
29	GPIO29	R/W	0h	Output Clear bit for this pin
28	GPIO28	R/W	0h	Output Clear bit for this pin
27	GPIO27	R/W	0h	Output Clear bit for this pin
26	GPIO26	R/W	0h	Output Clear bit for this pin
25	GPIO25	R/W	0h	Output Clear bit for this pin
24	GPIO24	R/W	0h	Output Clear bit for this pin
23	GPIO23	R/W	0h	Output Clear bit for this pin
22	GPIO22	R/W	0h	Output Clear bit for this pin
21	GPIO21	R/W	0h	Output Clear bit for this pin
20	GPIO20	R/W	0h	Output Clear bit for this pin
19	GPIO19	R/W	0h	Output Clear bit for this pin
18	GPIO18	R/W	0h	Output Clear bit for this pin
17	GPIO17	R/W	0h	Output Clear bit for this pin
16	GPIO16	R/W	0h	Output Clear bit for this pin
15	GPIO15	R/W	0h	Output Clear bit for this pin
14	GPIO14	R/W	0h	Output Clear bit for this pin
13	GPIO13	R/W	0h	Output Clear bit for this pin
12	GPIO12	R/W	0h	Output Clear bit for this pin
11	GPIO11	R/W	0h	Output Clear bit for this pin

Table 6-166. GPACLEAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO10	R/W	0h	Output Clear bit for this pin
9	GPIO9	R/W	0h	Output Clear bit for this pin
8	GPIO8	R/W	0h	Output Clear bit for this pin
7	GPIO7	R/W	0h	Output Clear bit for this pin
6	GPIO6	R/W	0h	Output Clear bit for this pin
5	GPIO5	R/W	0h	Output Clear bit for this pin
4	GPIO4	R/W	0h	Output Clear bit for this pin
3	GPIO3	R/W	0h	Output Clear bit for this pin
2	GPIO2	R/W	0h	Output Clear bit for this pin
1	GPIO1	R/W	0h	Output Clear bit for this pin
0	GPIO0	R/W	0h	Output Clear bit for this pin

6.4.5.4 GPATOGGLE Register (offset = 6h) [reset = 0h]

GPATOGGLE is shown in [Figure 6-159](#) and described in [Table 6-167](#).

GPIO A Data Toggle Register (GPIO0 to 31)

Writing a 1 will toggle GPIO0 output data latch 1 to 0 or 0 to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-159. GPATOGGLE Register

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
R/W-0h							
23	22	21	20	19	18	17	16
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
R/W-0h							
15	14	13	12	11	10	9	8
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
R/W-0h							
7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-167. GPATOGGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R/W	0h	Output Toggle Register GPIO pin
30	GPIO30	R/W	0h	Output Toggle Register GPIO pin
29	GPIO29	R/W	0h	Output Toggle Register GPIO pin
28	GPIO28	R/W	0h	Output Toggle Register GPIO pin
27	GPIO27	R/W	0h	Output Toggle Register GPIO pin
26	GPIO26	R/W	0h	Output Toggle Register GPIO pin
25	GPIO25	R/W	0h	Output Toggle Register GPIO pin
24	GPIO24	R/W	0h	Output Toggle Register GPIO pin
23	GPIO23	R/W	0h	Output Toggle Register GPIO pin
22	GPIO22	R/W	0h	Output Toggle Register GPIO pin
21	GPIO21	R/W	0h	Output Toggle Register GPIO pin
20	GPIO20	R/W	0h	Output Toggle Register GPIO pin
19	GPIO19	R/W	0h	Output Toggle Register GPIO pin
18	GPIO18	R/W	0h	Output Toggle Register GPIO pin
17	GPIO17	R/W	0h	Output Toggle Register GPIO pin
16	GPIO16	R/W	0h	Output Toggle Register GPIO pin
15	GPIO15	R/W	0h	Output Toggle Register GPIO pin
14	GPIO14	R/W	0h	Output Toggle Register GPIO pin
13	GPIO13	R/W	0h	Output Toggle Register GPIO pin
12	GPIO12	R/W	0h	Output Toggle Register GPIO pin
11	GPIO11	R/W	0h	Output Toggle Register GPIO pin

Table 6-167. GPATOGGLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO10	R/W	0h	Output Toggle Register GPIO pin
9	GPIO9	R/W	0h	Output Toggle Register GPIO pin
8	GPIO8	R/W	0h	Output Toggle Register GPIO pin
7	GPIO7	R/W	0h	Output Toggle Register GPIO pin
6	GPIO6	R/W	0h	Output Toggle Register GPIO pin
5	GPIO5	R/W	0h	Output Toggle Register GPIO pin
4	GPIO4	R/W	0h	Output Toggle Register GPIO pin
3	GPIO3	R/W	0h	Output Toggle Register GPIO pin
2	GPIO2	R/W	0h	Output Toggle Register GPIO pin
1	GPIO1	R/W	0h	Output Toggle Register GPIO pin
0	GPIO0	R/W	0h	Output Toggle Register GPIO pin

6.4.5.5 GPBDAT Register (offset = 8h) [reset = 0h]

GPBDAT is shown in [Figure 6-160](#) and described in [Table 6-168](#).

GPIO B Data Register (GPIO32 to 63)

Reading this register indicates the current status of the GPIO pin, irrespective of which mode the pin is in. Writing to this register will set the GPIO pin high or low if the pin is enabled for GPIO output mode, otherwise the value written is latched but ignored. The state of the output register latch will remain in its current state until the next write operation. A system reset will clear all bits and latched values to zero.

DESIGNER NOTE:

[1] Reading the GPIODAT register should reflect the state of the PIN (after qualification), not the state of the output latch of the GPIODAT register.

Figure 6-160. GPBDAT Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-168. GPBDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Data Register for this pin
30	GPIO62	R/W	0h	Data Register for this pin
29	GPIO61	R/W	0h	Data Register for this pin
28	GPIO60	R/W	0h	Data Register for this pin
27	GPIO59	R/W	0h	Data Register for this pin
26	GPIO58	R/W	0h	Data Register for this pin
25	GPIO57	R/W	0h	Data Register for this pin
24	GPIO56	R/W	0h	Data Register for this pin
23	GPIO55	R/W	0h	Data Register for this pin
22	GPIO54	R/W	0h	Data Register for this pin
21	GPIO53	R/W	0h	Data Register for this pin
20	GPIO52	R/W	0h	Data Register for this pin
19	GPIO51	R/W	0h	Data Register for this pin
18	GPIO50	R/W	0h	Data Register for this pin
17	GPIO49	R/W	0h	Data Register for this pin
16	GPIO48	R/W	0h	Data Register for this pin
15	GPIO47	R/W	0h	Data Register for this pin
14	GPIO46	R/W	0h	Data Register for this pin

Table 6-168. GPBDAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO45	R/W	0h	Data Register for this pin
12	GPIO44	R/W	0h	Data Register for this pin
11	GPIO43	R/W	0h	Data Register for this pin
10	GPIO42	R/W	0h	Data Register for this pin
9	GPIO41	R/W	0h	Data Register for this pin
8	GPIO40	R/W	0h	Data Register for this pin
7	GPIO39	R/W	0h	Data Register for this pin
6	GPIO38	R/W	0h	Data Register for this pin
5	GPIO37	R/W	0h	Data Register for this pin
4	GPIO36	R/W	0h	Data Register for this pin
3	GPIO35	R/W	0h	Data Register for this pin
2	GPIO34	R/W	0h	Data Register for this pin
1	GPIO33	R/W	0h	Data Register for this pin
0	GPIO32	R/W	0h	Data Register for this pin

6.4.5.6 GPBSET Register (offset = Ah) [reset = 0h]

GPBSET is shown in [Figure 6-161](#) and described in [Table 6-169](#).

GPIO B Data Set Register (GPIO32 to 63)

Writing a 1 will force GPIO output data latch to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-161. GPBSET Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-169. GPBSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Output Set bit for this pin
30	GPIO62	R/W	0h	Output Set bit for this pin
29	GPIO61	R/W	0h	Output Set bit for this pin
28	GPIO60	R/W	0h	Output Set bit for this pin
27	GPIO59	R/W	0h	Output Set bit for this pin
26	GPIO58	R/W	0h	Output Set bit for this pin
25	GPIO57	R/W	0h	Output Set bit for this pin
24	GPIO56	R/W	0h	Output Set bit for this pin
23	GPIO55	R/W	0h	Output Set bit for this pin
22	GPIO54	R/W	0h	Output Set bit for this pin
21	GPIO53	R/W	0h	Output Set bit for this pin
20	GPIO52	R/W	0h	Output Set bit for this pin
19	GPIO51	R/W	0h	Output Set bit for this pin
18	GPIO50	R/W	0h	Output Set bit for this pin
17	GPIO49	R/W	0h	Output Set bit for this pin
16	GPIO48	R/W	0h	Output Set bit for this pin
15	GPIO47	R/W	0h	Output Set bit for this pin
14	GPIO46	R/W	0h	Output Set bit for this pin
13	GPIO45	R/W	0h	Output Set bit for this pin
12	GPIO44	R/W	0h	Output Set bit for this pin
11	GPIO43	R/W	0h	Output Set bit for this pin

Table 6-169. GPBSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO42	R/W	0h	Output Set bit for this pin
9	GPIO41	R/W	0h	Output Set bit for this pin
8	GPIO40	R/W	0h	Output Set bit for this pin
7	GPIO39	R/W	0h	Output Set bit for this pin
6	GPIO38	R/W	0h	Output Set bit for this pin
5	GPIO37	R/W	0h	Output Set bit for this pin
4	GPIO36	R/W	0h	Output Set bit for this pin
3	GPIO35	R/W	0h	Output Set bit for this pin
2	GPIO34	R/W	0h	Output Set bit for this pin
1	GPIO33	R/W	0h	Output Set bit for this pin
0	GPIO32	R/W	0h	Output Set bit for this pin

6.4.5.7 GPBCLEAR Register (offset = Ch) [reset = 0h]

GPBCLEAR is shown in [Figure 6-162](#) and described in [Table 6-170](#).

GPIO B Data Clear Register (GPIO32 to 63)

Writing a 1 will force GPIO0 output data latch to 0.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-162. GPBCLEAR Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-170. GPBCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Output Clear bit for this pin
30	GPIO62	R/W	0h	Output Clear bit for this pin
29	GPIO61	R/W	0h	Output Clear bit for this pin
28	GPIO60	R/W	0h	Output Clear bit for this pin
27	GPIO59	R/W	0h	Output Clear bit for this pin
26	GPIO58	R/W	0h	Output Clear bit for this pin
25	GPIO57	R/W	0h	Output Clear bit for this pin
24	GPIO56	R/W	0h	Output Clear bit for this pin
23	GPIO55	R/W	0h	Output Clear bit for this pin
22	GPIO54	R/W	0h	Output Clear bit for this pin
21	GPIO53	R/W	0h	Output Clear bit for this pin
20	GPIO52	R/W	0h	Output Clear bit for this pin
19	GPIO51	R/W	0h	Output Clear bit for this pin
18	GPIO50	R/W	0h	Output Clear bit for this pin
17	GPIO49	R/W	0h	Output Clear bit for this pin
16	GPIO48	R/W	0h	Output Clear bit for this pin
15	GPIO47	R/W	0h	Output Clear bit for this pin
14	GPIO46	R/W	0h	Output Clear bit for this pin
13	GPIO45	R/W	0h	Output Clear bit for this pin
12	GPIO44	R/W	0h	Output Clear bit for this pin
11	GPIO43	R/W	0h	Output Clear bit for this pin

Table 6-170. GPBCLEAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO42	R/W	0h	Output Clear bit for this pin
9	GPIO41	R/W	0h	Output Clear bit for this pin
8	GPIO40	R/W	0h	Output Clear bit for this pin
7	GPIO39	R/W	0h	Output Clear bit for this pin
6	GPIO38	R/W	0h	Output Clear bit for this pin
5	GPIO37	R/W	0h	Output Clear bit for this pin
4	GPIO36	R/W	0h	Output Clear bit for this pin
3	GPIO35	R/W	0h	Output Clear bit for this pin
2	GPIO34	R/W	0h	Output Clear bit for this pin
1	GPIO33	R/W	0h	Output Clear bit for this pin
0	GPIO32	R/W	0h	Output Clear bit for this pin

6.4.5.8 GPBTOGGLE Register (offset = Eh) [reset = 0h]

GPBTOGGLE is shown in [Figure 6-163](#) and described in [Table 6-171](#).

GPIO B Data Toggle Register (GPIO32 to 63)

Writing a 1 will toggle GPIO0 output data latch 1 to 0 or 0 to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-163. GPBTOGGLE Register

31	30	29	28	27	26	25	24
GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56
R/W-0h							
23	22	21	20	19	18	17	16
GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
R/W-0h							
15	14	13	12	11	10	9	8
GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40
R/W-0h							
7	6	5	4	3	2	1	0
GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-171. GPBTOGGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO63	R/W	0h	Output Toggle Register GPIO pin
30	GPIO62	R/W	0h	Output Toggle Register GPIO pin
29	GPIO61	R/W	0h	Output Toggle Register GPIO pin
28	GPIO60	R/W	0h	Output Toggle Register GPIO pin
27	GPIO59	R/W	0h	Output Toggle Register GPIO pin
26	GPIO58	R/W	0h	Output Toggle Register GPIO pin
25	GPIO57	R/W	0h	Output Toggle Register GPIO pin
24	GPIO56	R/W	0h	Output Toggle Register GPIO pin
23	GPIO55	R/W	0h	Output Toggle Register GPIO pin
22	GPIO54	R/W	0h	Output Toggle Register GPIO pin
21	GPIO53	R/W	0h	Output Toggle Register GPIO pin
20	GPIO52	R/W	0h	Output Toggle Register GPIO pin
19	GPIO51	R/W	0h	Output Toggle Register GPIO pin
18	GPIO50	R/W	0h	Output Toggle Register GPIO pin
17	GPIO49	R/W	0h	Output Toggle Register GPIO pin
16	GPIO48	R/W	0h	Output Toggle Register GPIO pin
15	GPIO47	R/W	0h	Output Toggle Register GPIO pin
14	GPIO46	R/W	0h	Output Toggle Register GPIO pin
13	GPIO45	R/W	0h	Output Toggle Register GPIO pin
12	GPIO44	R/W	0h	Output Toggle Register GPIO pin
11	GPIO43	R/W	0h	Output Toggle Register GPIO pin

Table 6-171. GPBTOGGLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO42	R/W	0h	Output Toggle Register GPIO pin
9	GPIO41	R/W	0h	Output Toggle Register GPIO pin
8	GPIO40	R/W	0h	Output Toggle Register GPIO pin
7	GPIO39	R/W	0h	Output Toggle Register GPIO pin
6	GPIO38	R/W	0h	Output Toggle Register GPIO pin
5	GPIO37	R/W	0h	Output Toggle Register GPIO pin
4	GPIO36	R/W	0h	Output Toggle Register GPIO pin
3	GPIO35	R/W	0h	Output Toggle Register GPIO pin
2	GPIO34	R/W	0h	Output Toggle Register GPIO pin
1	GPIO33	R/W	0h	Output Toggle Register GPIO pin
0	GPIO32	R/W	0h	Output Toggle Register GPIO pin

6.4.5.9 GPCDAT Register (offset = 10h) [reset = 0h]

GPCDAT is shown in [Figure 6-164](#) and described in [Table 6-172](#).

GPIO C Data Register (GPIO64 to 95)

Reading this register indicates the current status of the GPIO pin, irrespective of which mode the pin is in. Writing to this register will set the GPIO pin high or low if the pin is enabled for GPIO output mode, otherwise the value written is latched but ignored. The state of the output register latch will remain in its current state until the next write operation. A system reset will clear all bits and latched values to zero.

DESIGNER NOTE:

[1] Reading the GPIODAT register should reflect the state of the PIN (after qualification), not the state of the output latch of the

Figure 6-164. GPCDAT Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-172. GPCDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Data Register for this pin
30	GPIO94	R/W	0h	Data Register for this pin
29	GPIO93	R/W	0h	Data Register for this pin
28	GPIO92	R/W	0h	Data Register for this pin
27	GPIO91	R/W	0h	Data Register for this pin
26	GPIO90	R/W	0h	Data Register for this pin
25	GPIO89	R/W	0h	Data Register for this pin
24	GPIO88	R/W	0h	Data Register for this pin
23	GPIO87	R/W	0h	Data Register for this pin
22	GPIO86	R/W	0h	Data Register for this pin
21	GPIO85	R/W	0h	Data Register for this pin
20	GPIO84	R/W	0h	Data Register for this pin
19	GPIO83	R/W	0h	Data Register for this pin
18	GPIO82	R/W	0h	Data Register for this pin
17	GPIO81	R/W	0h	Data Register for this pin
16	GPIO80	R/W	0h	Data Register for this pin
15	GPIO79	R/W	0h	Data Register for this pin
14	GPIO78	R/W	0h	Data Register for this pin

Table 6-172. GPCDAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO77	R/W	0h	Data Register for this pin
12	GPIO76	R/W	0h	Data Register for this pin
11	GPIO75	R/W	0h	Data Register for this pin
10	GPIO74	R/W	0h	Data Register for this pin
9	GPIO73	R/W	0h	Data Register for this pin
8	GPIO72	R/W	0h	Data Register for this pin
7	GPIO71	R/W	0h	Data Register for this pin
6	GPIO70	R/W	0h	Data Register for this pin
5	GPIO69	R/W	0h	Data Register for this pin
4	GPIO68	R/W	0h	Data Register for this pin
3	GPIO67	R/W	0h	Data Register for this pin
2	GPIO66	R/W	0h	Data Register for this pin
1	GPIO65	R/W	0h	Data Register for this pin
0	GPIO64	R/W	0h	Data Register for this pin

6.4.5.10 GPCSET Register (offset = 12h) [reset = 0h]

GPCSET is shown in [Figure 6-165](#) and described in [Table 6-173](#).

GPIO C Data Set Register (GPIO64 to 95)

Writing a 1 will force GPIO output data latch to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-165. GPCSET Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-173. GPCSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Output Set bit for this pin
30	GPIO94	R/W	0h	Output Set bit for this pin
29	GPIO93	R/W	0h	Output Set bit for this pin
28	GPIO92	R/W	0h	Output Set bit for this pin
27	GPIO91	R/W	0h	Output Set bit for this pin
26	GPIO90	R/W	0h	Output Set bit for this pin
25	GPIO89	R/W	0h	Output Set bit for this pin
24	GPIO88	R/W	0h	Output Set bit for this pin
23	GPIO87	R/W	0h	Output Set bit for this pin
22	GPIO86	R/W	0h	Output Set bit for this pin
21	GPIO85	R/W	0h	Output Set bit for this pin
20	GPIO84	R/W	0h	Output Set bit for this pin
19	GPIO83	R/W	0h	Output Set bit for this pin
18	GPIO82	R/W	0h	Output Set bit for this pin
17	GPIO81	R/W	0h	Output Set bit for this pin
16	GPIO80	R/W	0h	Output Set bit for this pin
15	GPIO79	R/W	0h	Output Set bit for this pin
14	GPIO78	R/W	0h	Output Set bit for this pin
13	GPIO77	R/W	0h	Output Set bit for this pin
12	GPIO76	R/W	0h	Output Set bit for this pin
11	GPIO75	R/W	0h	Output Set bit for this pin

Table 6-173. GPCSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO74	R/W	0h	Output Set bit for this pin
9	GPIO73	R/W	0h	Output Set bit for this pin
8	GPIO72	R/W	0h	Output Set bit for this pin
7	GPIO71	R/W	0h	Output Set bit for this pin
6	GPIO70	R/W	0h	Output Set bit for this pin
5	GPIO69	R/W	0h	Output Set bit for this pin
4	GPIO68	R/W	0h	Output Set bit for this pin
3	GPIO67	R/W	0h	Output Set bit for this pin
2	GPIO66	R/W	0h	Output Set bit for this pin
1	GPIO65	R/W	0h	Output Set bit for this pin
0	GPIO64	R/W	0h	Output Set bit for this pin

6.4.5.11 GPCCLEAR Register (offset = 14h) [reset = 0h]

GPCCLEAR is shown in [Figure 6-166](#) and described in [Table 6-174](#).

GPIO C Data Clear Register (GPIO64 to 95)

Writing a 1 will force GPIO0 output data latch to 0.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-166. GPCCLEAR Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-174. GPCCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Output Clear bit for this pin
30	GPIO94	R/W	0h	Output Clear bit for this pin
29	GPIO93	R/W	0h	Output Clear bit for this pin
28	GPIO92	R/W	0h	Output Clear bit for this pin
27	GPIO91	R/W	0h	Output Clear bit for this pin
26	GPIO90	R/W	0h	Output Clear bit for this pin
25	GPIO89	R/W	0h	Output Clear bit for this pin
24	GPIO88	R/W	0h	Output Clear bit for this pin
23	GPIO87	R/W	0h	Output Clear bit for this pin
22	GPIO86	R/W	0h	Output Clear bit for this pin
21	GPIO85	R/W	0h	Output Clear bit for this pin
20	GPIO84	R/W	0h	Output Clear bit for this pin
19	GPIO83	R/W	0h	Output Clear bit for this pin
18	GPIO82	R/W	0h	Output Clear bit for this pin
17	GPIO81	R/W	0h	Output Clear bit for this pin
16	GPIO80	R/W	0h	Output Clear bit for this pin
15	GPIO79	R/W	0h	Output Clear bit for this pin
14	GPIO78	R/W	0h	Output Clear bit for this pin
13	GPIO77	R/W	0h	Output Clear bit for this pin
12	GPIO76	R/W	0h	Output Clear bit for this pin
11	GPIO75	R/W	0h	Output Clear bit for this pin

Table 6-174. GPCCLEAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO74	R/W	0h	Output Clear bit for this pin
9	GPIO73	R/W	0h	Output Clear bit for this pin
8	GPIO72	R/W	0h	Output Clear bit for this pin
7	GPIO71	R/W	0h	Output Clear bit for this pin
6	GPIO70	R/W	0h	Output Clear bit for this pin
5	GPIO69	R/W	0h	Output Clear bit for this pin
4	GPIO68	R/W	0h	Output Clear bit for this pin
3	GPIO67	R/W	0h	Output Clear bit for this pin
2	GPIO66	R/W	0h	Output Clear bit for this pin
1	GPIO65	R/W	0h	Output Clear bit for this pin
0	GPIO64	R/W	0h	Output Clear bit for this pin

6.4.5.12 GPCTOGGLE Register (offset = 16h) [reset = 0h]

GPCTOGGLE is shown in [Figure 6-167](#) and described in [Table 6-175](#).

GPIO C Data Toggle Register (GPIO64 to 95)

Writing a 1 will toggle GPIO0 output data latch 1 to 0 or 0 to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-167. GPCTOGGLE Register

31	30	29	28	27	26	25	24
GPIO95	GPIO94	GPIO93	GPIO92	GPIO91	GPIO90	GPIO89	GPIO88
R/W-0h							
23	22	21	20	19	18	17	16
GPIO87	GPIO86	GPIO85	GPIO84	GPIO83	GPIO82	GPIO81	GPIO80
R/W-0h							
15	14	13	12	11	10	9	8
GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72
R/W-0h							
7	6	5	4	3	2	1	0
GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-175. GPCTOGGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO95	R/W	0h	Output Toggle Register GPIO pin
30	GPIO94	R/W	0h	Output Toggle Register GPIO pin
29	GPIO93	R/W	0h	Output Toggle Register GPIO pin
28	GPIO92	R/W	0h	Output Toggle Register GPIO pin
27	GPIO91	R/W	0h	Output Toggle Register GPIO pin
26	GPIO90	R/W	0h	Output Toggle Register GPIO pin
25	GPIO89	R/W	0h	Output Toggle Register GPIO pin
24	GPIO88	R/W	0h	Output Toggle Register GPIO pin
23	GPIO87	R/W	0h	Output Toggle Register GPIO pin
22	GPIO86	R/W	0h	Output Toggle Register GPIO pin
21	GPIO85	R/W	0h	Output Toggle Register GPIO pin
20	GPIO84	R/W	0h	Output Toggle Register GPIO pin
19	GPIO83	R/W	0h	Output Toggle Register GPIO pin
18	GPIO82	R/W	0h	Output Toggle Register GPIO pin
17	GPIO81	R/W	0h	Output Toggle Register GPIO pin
16	GPIO80	R/W	0h	Output Toggle Register GPIO pin
15	GPIO79	R/W	0h	Output Toggle Register GPIO pin
14	GPIO78	R/W	0h	Output Toggle Register GPIO pin
13	GPIO77	R/W	0h	Output Toggle Register GPIO pin
12	GPIO76	R/W	0h	Output Toggle Register GPIO pin
11	GPIO75	R/W	0h	Output Toggle Register GPIO pin

Table 6-175. GPCTOGGLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO74	R/W	0h	Output Toggle Register GPIO pin
9	GPIO73	R/W	0h	Output Toggle Register GPIO pin
8	GPIO72	R/W	0h	Output Toggle Register GPIO pin
7	GPIO71	R/W	0h	Output Toggle Register GPIO pin
6	GPIO70	R/W	0h	Output Toggle Register GPIO pin
5	GPIO69	R/W	0h	Output Toggle Register GPIO pin
4	GPIO68	R/W	0h	Output Toggle Register GPIO pin
3	GPIO67	R/W	0h	Output Toggle Register GPIO pin
2	GPIO66	R/W	0h	Output Toggle Register GPIO pin
1	GPIO65	R/W	0h	Output Toggle Register GPIO pin
0	GPIO64	R/W	0h	Output Toggle Register GPIO pin

6.4.5.13 GPDDAT Register (offset = 18h) [reset = 0h]

GPDDAT is shown in [Figure 6-168](#) and described in [Table 6-176](#).

GPIO D Data Register (GPIO96 to 127)

Reading this register indicates the current status of the GPIO pin, irrespective of which mode the pin is in. Writing to this register will set the GPIO pin high or low if the pin is enabled for GPIO output mode, otherwise the value written is latched but ignored. The state of the output register latch will remain in its current state until the next write operation. A system reset will clear all bits and latched values to zero.

DESIGNER NOTE:

[1] Reading the GPIODAT register should reflect the state of the PIN (after qualification), not the state of the output latch of the GPIODAT register.

Figure 6-168. GPDDAT Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-176. GPDDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Data Register for this pin
30	GPIO126	R/W	0h	Data Register for this pin
29	GPIO125	R/W	0h	Data Register for this pin
28	GPIO124	R/W	0h	Data Register for this pin
27	GPIO123	R/W	0h	Data Register for this pin
26	GPIO122	R/W	0h	Data Register for this pin
25	GPIO121	R/W	0h	Data Register for this pin
24	GPIO120	R/W	0h	Data Register for this pin
23	GPIO119	R/W	0h	Data Register for this pin
22	GPIO118	R/W	0h	Data Register for this pin
21	GPIO117	R/W	0h	Data Register for this pin
20	GPIO116	R/W	0h	Data Register for this pin
19	GPIO115	R/W	0h	Data Register for this pin
18	GPIO114	R/W	0h	Data Register for this pin
17	GPIO113	R/W	0h	Data Register for this pin
16	GPIO112	R/W	0h	Data Register for this pin
15	GPIO111	R/W	0h	Data Register for this pin
14	GPIO110	R/W	0h	Data Register for this pin

Table 6-176. GPDDAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO109	R/W	0h	Data Register for this pin
12	GPIO108	R/W	0h	Data Register for this pin
11	GPIO107	R/W	0h	Data Register for this pin
10	GPIO106	R/W	0h	Data Register for this pin
9	GPIO105	R/W	0h	Data Register for this pin
8	GPIO104	R/W	0h	Data Register for this pin
7	GPIO103	R/W	0h	Data Register for this pin
6	GPIO102	R/W	0h	Data Register for this pin
5	GPIO101	R/W	0h	Data Register for this pin
4	GPIO100	R/W	0h	Data Register for this pin
3	GPIO99	R/W	0h	Data Register for this pin
2	GPIO98	R/W	0h	Data Register for this pin
1	GPIO97	R/W	0h	Data Register for this pin
0	GPIO96	R/W	0h	Data Register for this pin

6.4.5.14 GPDSET Register (offset = 1Ah) [reset = 0h]

GPDSET is shown in [Figure 6-169](#) and described in [Table 6-177](#).

GPIO D Data Set Register (GPIO96 to 127)

Writing a 1 will force GPIO output data latch to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-169. GPDSET Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-177. GPDSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Output Set bit for this pin
30	GPIO126	R/W	0h	Output Set bit for this pin
29	GPIO125	R/W	0h	Output Set bit for this pin
28	GPIO124	R/W	0h	Output Set bit for this pin
27	GPIO123	R/W	0h	Output Set bit for this pin
26	GPIO122	R/W	0h	Output Set bit for this pin
25	GPIO121	R/W	0h	Output Set bit for this pin
24	GPIO120	R/W	0h	Output Set bit for this pin
23	GPIO119	R/W	0h	Output Set bit for this pin
22	GPIO118	R/W	0h	Output Set bit for this pin
21	GPIO117	R/W	0h	Output Set bit for this pin
20	GPIO116	R/W	0h	Output Set bit for this pin
19	GPIO115	R/W	0h	Output Set bit for this pin
18	GPIO114	R/W	0h	Output Set bit for this pin
17	GPIO113	R/W	0h	Output Set bit for this pin
16	GPIO112	R/W	0h	Output Set bit for this pin
15	GPIO111	R/W	0h	Output Set bit for this pin
14	GPIO110	R/W	0h	Output Set bit for this pin
13	GPIO109	R/W	0h	Output Set bit for this pin
12	GPIO108	R/W	0h	Output Set bit for this pin
11	GPIO107	R/W	0h	Output Set bit for this pin

Table 6-177. GPDSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO106	R/W	0h	Output Set bit for this pin
9	GPIO105	R/W	0h	Output Set bit for this pin
8	GPIO104	R/W	0h	Output Set bit for this pin
7	GPIO103	R/W	0h	Output Set bit for this pin
6	GPIO102	R/W	0h	Output Set bit for this pin
5	GPIO101	R/W	0h	Output Set bit for this pin
4	GPIO100	R/W	0h	Output Set bit for this pin
3	GPIO99	R/W	0h	Output Set bit for this pin
2	GPIO98	R/W	0h	Output Set bit for this pin
1	GPIO97	R/W	0h	Output Set bit for this pin
0	GPIO96	R/W	0h	Output Set bit for this pin

6.4.5.15 GPDCLEAR Register (offset = 1Ch) [reset = 0h]

GPDCLEAR is shown in [Figure 6-170](#) and described in [Table 6-178](#).

GPIO D Data Clear Register (GPIO96 to 127)

Writing a 1 will force GPIO0 output data latch to 0.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-170. GPDCLEAR Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-178. GPDCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Output Clear bit for this pin
30	GPIO126	R/W	0h	Output Clear bit for this pin
29	GPIO125	R/W	0h	Output Clear bit for this pin
28	GPIO124	R/W	0h	Output Clear bit for this pin
27	GPIO123	R/W	0h	Output Clear bit for this pin
26	GPIO122	R/W	0h	Output Clear bit for this pin
25	GPIO121	R/W	0h	Output Clear bit for this pin
24	GPIO120	R/W	0h	Output Clear bit for this pin
23	GPIO119	R/W	0h	Output Clear bit for this pin
22	GPIO118	R/W	0h	Output Clear bit for this pin
21	GPIO117	R/W	0h	Output Clear bit for this pin
20	GPIO116	R/W	0h	Output Clear bit for this pin
19	GPIO115	R/W	0h	Output Clear bit for this pin
18	GPIO114	R/W	0h	Output Clear bit for this pin
17	GPIO113	R/W	0h	Output Clear bit for this pin
16	GPIO112	R/W	0h	Output Clear bit for this pin
15	GPIO111	R/W	0h	Output Clear bit for this pin
14	GPIO110	R/W	0h	Output Clear bit for this pin
13	GPIO109	R/W	0h	Output Clear bit for this pin
12	GPIO108	R/W	0h	Output Clear bit for this pin
11	GPIO107	R/W	0h	Output Clear bit for this pin

Table 6-178. GPDCLEAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO106	R/W	0h	Output Clear bit for this pin
9	GPIO105	R/W	0h	Output Clear bit for this pin
8	GPIO104	R/W	0h	Output Clear bit for this pin
7	GPIO103	R/W	0h	Output Clear bit for this pin
6	GPIO102	R/W	0h	Output Clear bit for this pin
5	GPIO101	R/W	0h	Output Clear bit for this pin
4	GPIO100	R/W	0h	Output Clear bit for this pin
3	GPIO99	R/W	0h	Output Clear bit for this pin
2	GPIO98	R/W	0h	Output Clear bit for this pin
1	GPIO97	R/W	0h	Output Clear bit for this pin
0	GPIO96	R/W	0h	Output Clear bit for this pin

6.4.5.16 GPDTOGGLE Register (offset = 1Eh) [reset = 0h]

GPDTOGGLE is shown in [Figure 6-171](#) and described in [Table 6-179](#).

GPIO D Data Toggle Register (GPIO96 to 127)

Writing a 1 will toggle GPIO0 output data latch 1 to 0 or 0 to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-171. GPDTOGGLE Register

31	30	29	28	27	26	25	24
GPIO127	GPIO126	GPIO125	GPIO124	GPIO123	GPIO122	GPIO121	GPIO120
R/W-0h							
23	22	21	20	19	18	17	16
GPIO119	GPIO118	GPIO117	GPIO116	GPIO115	GPIO114	GPIO113	GPIO112
R/W-0h							
15	14	13	12	11	10	9	8
GPIO111	GPIO110	GPIO109	GPIO108	GPIO107	GPIO106	GPIO105	GPIO104
R/W-0h							
7	6	5	4	3	2	1	0
GPIO103	GPIO102	GPIO101	GPIO100	GPIO99	GPIO98	GPIO97	GPIO96
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-179. GPDTOGGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO127	R/W	0h	Output Toggle Register GPIO pin
30	GPIO126	R/W	0h	Output Toggle Register GPIO pin
29	GPIO125	R/W	0h	Output Toggle Register GPIO pin
28	GPIO124	R/W	0h	Output Toggle Register GPIO pin
27	GPIO123	R/W	0h	Output Toggle Register GPIO pin
26	GPIO122	R/W	0h	Output Toggle Register GPIO pin
25	GPIO121	R/W	0h	Output Toggle Register GPIO pin
24	GPIO120	R/W	0h	Output Toggle Register GPIO pin
23	GPIO119	R/W	0h	Output Toggle Register GPIO pin
22	GPIO118	R/W	0h	Output Toggle Register GPIO pin
21	GPIO117	R/W	0h	Output Toggle Register GPIO pin
20	GPIO116	R/W	0h	Output Toggle Register GPIO pin
19	GPIO115	R/W	0h	Output Toggle Register GPIO pin
18	GPIO114	R/W	0h	Output Toggle Register GPIO pin
17	GPIO113	R/W	0h	Output Toggle Register GPIO pin
16	GPIO112	R/W	0h	Output Toggle Register GPIO pin
15	GPIO111	R/W	0h	Output Toggle Register GPIO pin
14	GPIO110	R/W	0h	Output Toggle Register GPIO pin
13	GPIO109	R/W	0h	Output Toggle Register GPIO pin
12	GPIO108	R/W	0h	Output Toggle Register GPIO pin
11	GPIO107	R/W	0h	Output Toggle Register GPIO pin

Table 6-179. GPDToggle Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO106	R/W	0h	Output Toggle Register GPIO pin
9	GPIO105	R/W	0h	Output Toggle Register GPIO pin
8	GPIO104	R/W	0h	Output Toggle Register GPIO pin
7	GPIO103	R/W	0h	Output Toggle Register GPIO pin
6	GPIO102	R/W	0h	Output Toggle Register GPIO pin
5	GPIO101	R/W	0h	Output Toggle Register GPIO pin
4	GPIO100	R/W	0h	Output Toggle Register GPIO pin
3	GPIO99	R/W	0h	Output Toggle Register GPIO pin
2	GPIO98	R/W	0h	Output Toggle Register GPIO pin
1	GPIO97	R/W	0h	Output Toggle Register GPIO pin
0	GPIO96	R/W	0h	Output Toggle Register GPIO pin

6.4.5.17 GPEDAT Register (offset = 20h) [reset = 0h]

GPEDAT is shown in [Figure 6-172](#) and described in [Table 6-180](#).

GPIO E Data Register (GPIO128 to 159)

Reading this register indicates the current status of the GPIO pin, irrespective of which mode the pin is in. Writing to this register will set the GPIO pin high or low if the pin is enabled for GPIO output mode, otherwise the value written is latched but ignored. The state of the output register latch will remain in its current state until the next write operation. A system reset will clear all bits and latched values to zero.

DESIGNER NOTE:

[1] Reading the GPIODAT register should reflect the state of the PIN (after qualification), not the state of the output latch of the

Figure 6-172. GPEDAT Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-180. GPEDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Data Register for this pin
30	GPIO158	R/W	0h	Data Register for this pin
29	GPIO157	R/W	0h	Data Register for this pin
28	GPIO156	R/W	0h	Data Register for this pin
27	GPIO155	R/W	0h	Data Register for this pin
26	GPIO154	R/W	0h	Data Register for this pin
25	GPIO153	R/W	0h	Data Register for this pin
24	GPIO152	R/W	0h	Data Register for this pin
23	GPIO151	R/W	0h	Data Register for this pin
22	GPIO150	R/W	0h	Data Register for this pin
21	GPIO149	R/W	0h	Data Register for this pin
20	GPIO148	R/W	0h	Data Register for this pin
19	GPIO147	R/W	0h	Data Register for this pin
18	GPIO146	R/W	0h	Data Register for this pin
17	GPIO145	R/W	0h	Data Register for this pin
16	GPIO144	R/W	0h	Data Register for this pin
15	GPIO143	R/W	0h	Data Register for this pin
14	GPIO142	R/W	0h	Data Register for this pin

Table 6-180. GPEDAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GPIO141	R/W	0h	Data Register for this pin
12	GPIO140	R/W	0h	Data Register for this pin
11	GPIO139	R/W	0h	Data Register for this pin
10	GPIO138	R/W	0h	Data Register for this pin
9	GPIO137	R/W	0h	Data Register for this pin
8	GPIO136	R/W	0h	Data Register for this pin
7	GPIO135	R/W	0h	Data Register for this pin
6	GPIO134	R/W	0h	Data Register for this pin
5	GPIO133	R/W	0h	Data Register for this pin
4	GPIO132	R/W	0h	Data Register for this pin
3	GPIO131	R/W	0h	Data Register for this pin
2	GPIO130	R/W	0h	Data Register for this pin
1	GPIO129	R/W	0h	Data Register for this pin
0	GPIO128	R/W	0h	Data Register for this pin

6.4.5.18 GPESET Register (offset = 22h) [reset = 0h]

GPESET is shown in [Figure 6-173](#) and described in [Table 6-181](#).

GPIO E Data Set Register (GPIO128 to 159)

Writing a 1 will force GPIO output data latch to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-173. GPESET Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-181. GPESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Output Set bit for this pin
30	GPIO158	R/W	0h	Output Set bit for this pin
29	GPIO157	R/W	0h	Output Set bit for this pin
28	GPIO156	R/W	0h	Output Set bit for this pin
27	GPIO155	R/W	0h	Output Set bit for this pin
26	GPIO154	R/W	0h	Output Set bit for this pin
25	GPIO153	R/W	0h	Output Set bit for this pin
24	GPIO152	R/W	0h	Output Set bit for this pin
23	GPIO151	R/W	0h	Output Set bit for this pin
22	GPIO150	R/W	0h	Output Set bit for this pin
21	GPIO149	R/W	0h	Output Set bit for this pin
20	GPIO148	R/W	0h	Output Set bit for this pin
19	GPIO147	R/W	0h	Output Set bit for this pin
18	GPIO146	R/W	0h	Output Set bit for this pin
17	GPIO145	R/W	0h	Output Set bit for this pin
16	GPIO144	R/W	0h	Output Set bit for this pin
15	GPIO143	R/W	0h	Output Set bit for this pin
14	GPIO142	R/W	0h	Output Set bit for this pin
13	GPIO141	R/W	0h	Output Set bit for this pin
12	GPIO140	R/W	0h	Output Set bit for this pin
11	GPIO139	R/W	0h	Output Set bit for this pin

Table 6-181. GPESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO138	R/W	0h	Output Set bit for this pin
9	GPIO137	R/W	0h	Output Set bit for this pin
8	GPIO136	R/W	0h	Output Set bit for this pin
7	GPIO135	R/W	0h	Output Set bit for this pin
6	GPIO134	R/W	0h	Output Set bit for this pin
5	GPIO133	R/W	0h	Output Set bit for this pin
4	GPIO132	R/W	0h	Output Set bit for this pin
3	GPIO131	R/W	0h	Output Set bit for this pin
2	GPIO130	R/W	0h	Output Set bit for this pin
1	GPIO129	R/W	0h	Output Set bit for this pin
0	GPIO128	R/W	0h	Output Set bit for this pin

6.4.5.19 GPECLEAR Register (offset = 24h) [reset = 0h]

GPECLEAR is shown in [Figure 6-174](#) and described in [Table 6-182](#).

GPIO E Data Clear Register (GPIO128 to 159)

Writing a 1 will force GPIO0 output data latch to 0.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-174. GPECLEAR Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-182. GPECLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Output Clear bit for this pin
30	GPIO158	R/W	0h	Output Clear bit for this pin
29	GPIO157	R/W	0h	Output Clear bit for this pin
28	GPIO156	R/W	0h	Output Clear bit for this pin
27	GPIO155	R/W	0h	Output Clear bit for this pin
26	GPIO154	R/W	0h	Output Clear bit for this pin
25	GPIO153	R/W	0h	Output Clear bit for this pin
24	GPIO152	R/W	0h	Output Clear bit for this pin
23	GPIO151	R/W	0h	Output Clear bit for this pin
22	GPIO150	R/W	0h	Output Clear bit for this pin
21	GPIO149	R/W	0h	Output Clear bit for this pin
20	GPIO148	R/W	0h	Output Clear bit for this pin
19	GPIO147	R/W	0h	Output Clear bit for this pin
18	GPIO146	R/W	0h	Output Clear bit for this pin
17	GPIO145	R/W	0h	Output Clear bit for this pin
16	GPIO144	R/W	0h	Output Clear bit for this pin
15	GPIO143	R/W	0h	Output Clear bit for this pin
14	GPIO142	R/W	0h	Output Clear bit for this pin
13	GPIO141	R/W	0h	Output Clear bit for this pin
12	GPIO140	R/W	0h	Output Clear bit for this pin
11	GPIO139	R/W	0h	Output Clear bit for this pin

Table 6-182. GPECLEAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO138	R/W	0h	Output Clear bit for this pin
9	GPIO137	R/W	0h	Output Clear bit for this pin
8	GPIO136	R/W	0h	Output Clear bit for this pin
7	GPIO135	R/W	0h	Output Clear bit for this pin
6	GPIO134	R/W	0h	Output Clear bit for this pin
5	GPIO133	R/W	0h	Output Clear bit for this pin
4	GPIO132	R/W	0h	Output Clear bit for this pin
3	GPIO131	R/W	0h	Output Clear bit for this pin
2	GPIO130	R/W	0h	Output Clear bit for this pin
1	GPIO129	R/W	0h	Output Clear bit for this pin
0	GPIO128	R/W	0h	Output Clear bit for this pin

6.4.5.20 GPETOGGLE Register (offset = 26h) [reset = 0h]

GPETOGGLE is shown in [Figure 6-175](#) and described in [Table 6-183](#).

GPIO E Data Toggle Register (GPIO128 to 159)

Writing a 1 will toggle GPIO0 output data latch 1 to 0 or 0 to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-175. GPETOGGLE Register

31	30	29	28	27	26	25	24
GPIO159	GPIO158	GPIO157	GPIO156	GPIO155	GPIO154	GPIO153	GPIO152
R/W-0h							
23	22	21	20	19	18	17	16
GPIO151	GPIO150	GPIO149	GPIO148	GPIO147	GPIO146	GPIO145	GPIO144
R/W-0h							
15	14	13	12	11	10	9	8
GPIO143	GPIO142	GPIO141	GPIO140	GPIO139	GPIO138	GPIO137	GPIO136
R/W-0h							
7	6	5	4	3	2	1	0
GPIO135	GPIO134	GPIO133	GPIO132	GPIO131	GPIO130	GPIO129	GPIO128
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-183. GPETOGGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GPIO159	R/W	0h	Output Toggle Register GPIO pin
30	GPIO158	R/W	0h	Output Toggle Register GPIO pin
29	GPIO157	R/W	0h	Output Toggle Register GPIO pin
28	GPIO156	R/W	0h	Output Toggle Register GPIO pin
27	GPIO155	R/W	0h	Output Toggle Register GPIO pin
26	GPIO154	R/W	0h	Output Toggle Register GPIO pin
25	GPIO153	R/W	0h	Output Toggle Register GPIO pin
24	GPIO152	R/W	0h	Output Toggle Register GPIO pin
23	GPIO151	R/W	0h	Output Toggle Register GPIO pin
22	GPIO150	R/W	0h	Output Toggle Register GPIO pin
21	GPIO149	R/W	0h	Output Toggle Register GPIO pin
20	GPIO148	R/W	0h	Output Toggle Register GPIO pin
19	GPIO147	R/W	0h	Output Toggle Register GPIO pin
18	GPIO146	R/W	0h	Output Toggle Register GPIO pin
17	GPIO145	R/W	0h	Output Toggle Register GPIO pin
16	GPIO144	R/W	0h	Output Toggle Register GPIO pin
15	GPIO143	R/W	0h	Output Toggle Register GPIO pin
14	GPIO142	R/W	0h	Output Toggle Register GPIO pin
13	GPIO141	R/W	0h	Output Toggle Register GPIO pin
12	GPIO140	R/W	0h	Output Toggle Register GPIO pin
11	GPIO139	R/W	0h	Output Toggle Register GPIO pin

Table 6-183. GPETOGGLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GPIO138	R/W	0h	Output Toggle Register GPIO pin
9	GPIO137	R/W	0h	Output Toggle Register GPIO pin
8	GPIO136	R/W	0h	Output Toggle Register GPIO pin
7	GPIO135	R/W	0h	Output Toggle Register GPIO pin
6	GPIO134	R/W	0h	Output Toggle Register GPIO pin
5	GPIO133	R/W	0h	Output Toggle Register GPIO pin
4	GPIO132	R/W	0h	Output Toggle Register GPIO pin
3	GPIO131	R/W	0h	Output Toggle Register GPIO pin
2	GPIO130	R/W	0h	Output Toggle Register GPIO pin
1	GPIO129	R/W	0h	Output Toggle Register GPIO pin
0	GPIO128	R/W	0h	Output Toggle Register GPIO pin

6.4.5.21 GPFDAT Register (offset = 28h) [reset = 0h]

GPFDAT is shown in [Figure 6-176](#) and described in [Table 6-184](#).

GPIO F Data Register (GPIO160 to 168)

Reading this register indicates the current status of the GPIO pin, irrespective of which mode the pin is in. Writing to this register will set the GPIO pin high or low if the pin is enabled for GPIO output mode, otherwise the value written is latched but ignored. The state of the output register latch will remain in its current state until the next write operation. A system reset will clear all bits and latched values to zero.

DESIGNER NOTE:

[1] Reading the GPIODAT register should reflect the state of the PIN (after qualification), not the state of the output latch of the

Figure 6-176. GPFDAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	GPIO168						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-184. GPFDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved

Table 6-184. GPFDAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	0h	Data Register for this pin
7	GPIO167	R/W	0h	Data Register for this pin
6	GPIO166	R/W	0h	Data Register for this pin
5	GPIO165	R/W	0h	Data Register for this pin
4	GPIO164	R/W	0h	Data Register for this pin
3	GPIO163	R/W	0h	Data Register for this pin
2	GPIO162	R/W	0h	Data Register for this pin
1	GPIO161	R/W	0h	Data Register for this pin
0	GPIO160	R/W	0h	Data Register for this pin

6.4.5.22 GPFSET Register (offset = 2Ah) [reset = 0h]

GPFSET is shown in [Figure 6-177](#) and described in [Table 6-185](#).

GPIO F Data Set Register (GPIO160 to 168)

Writing a 1 will force GPIO output data latch to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-177. GPFSET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-185. GPFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	0h	Output Set bit for this pin
7	GPIO167	R/W	0h	Output Set bit for this pin

Table 6-185. GPFSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	GPIO166	R/W	0h	Output Set bit for this pin
5	GPIO165	R/W	0h	Output Set bit for this pin
4	GPIO164	R/W	0h	Output Set bit for this pin
3	GPIO163	R/W	0h	Output Set bit for this pin
2	GPIO162	R/W	0h	Output Set bit for this pin
1	GPIO161	R/W	0h	Output Set bit for this pin
0	GPIO160	R/W	0h	Output Set bit for this pin

6.4.5.23 GPFCLEAR Register (offset = 2Ch) [reset = 0h]

GPFCLEAR is shown in [Figure 6-178](#) and described in [Table 6-186](#).

GPIO F Data Clear Register (GPIO160 to 168)

Writing a 1 will force GPIO0 output data latch to 0.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-178. GPFCLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-186. GPFCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	0h	Output Clear bit for this pin
7	GPIO167	R/W	0h	Output Clear bit for this pin

Table 6-186. GPFCLEAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	GPIO166	R/W	0h	Output Clear bit for this pin
5	GPIO165	R/W	0h	Output Clear bit for this pin
4	GPIO164	R/W	0h	Output Clear bit for this pin
3	GPIO163	R/W	0h	Output Clear bit for this pin
2	GPIO162	R/W	0h	Output Clear bit for this pin
1	GPIO161	R/W	0h	Output Clear bit for this pin
0	GPIO160	R/W	0h	Output Clear bit for this pin

6.4.5.24 GPFTOGGLE Register (offset = 2Eh) [reset = 0h]

GPFTOGGLE is shown in [Figure 6-179](#) and described in [Table 6-187](#).

GPIO F Data Toggle Register (GPIO160 to 168)

Writing a 1 will toggle GPIO0 output data latch 1 to 0 or 0 to 1.

Writes of 0 are ignored.

Always reads back a 0.

Figure 6-179. GPFTOGGLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	GPIO168						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
GPIO167	GPIO166	GPIO165	GPIO164	GPIO163	GPIO162	GPIO161	GPIO160
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 6-187. GPFTOGGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	GPIO168	R/W	0h	Output Toggle Register GPIO pin
7	GPIO167	R/W	0h	Output Toggle Register GPIO pin

Table 6-187. GPFTOGGLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	GPIO166	R/W	0h	Output Toggle Register GPIO pin
5	GPIO165	R/W	0h	Output Toggle Register GPIO pin
4	GPIO164	R/W	0h	Output Toggle Register GPIO pin
3	GPIO163	R/W	0h	Output Toggle Register GPIO pin
2	GPIO162	R/W	0h	Output Toggle Register GPIO pin
1	GPIO161	R/W	0h	Output Toggle Register GPIO pin
0	GPIO160	R/W	0h	Output Toggle Register GPIO pin

Analog Subsystem

This analog subsystem module is described in this chapter.

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7.1 Analog Subsystem	1189
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7.1 Analog Subsystem

The analog modules on this device include the Analog-to-Digital Converter (ADC), Temperature Sensor, Buffered Digital-to-Analog Converter (DAC), and Comparator Subsystem (CMPSS).

7.1.1 Features

The analog subsystem has the following features:

- Flexible voltage references
 - VREFHIA to VREFHID externally supplied reference voltage pins
 - Selectable by ADCs and buffered DACs
 - VDAC externally supplied reference voltage pin
 - Selectable by buffered DACs and comparator subsystem DACs
- Flexible pin usage
 - Buffered DAC and comparator subsystem functions multiplexed with ADC inputs
 - Internal connection to VREFLO on all ADCs for offset self-calibration

7.1.2 Block Diagram

Figure 7-1 shows the connections between the different integrated analog modules and to the device pins.

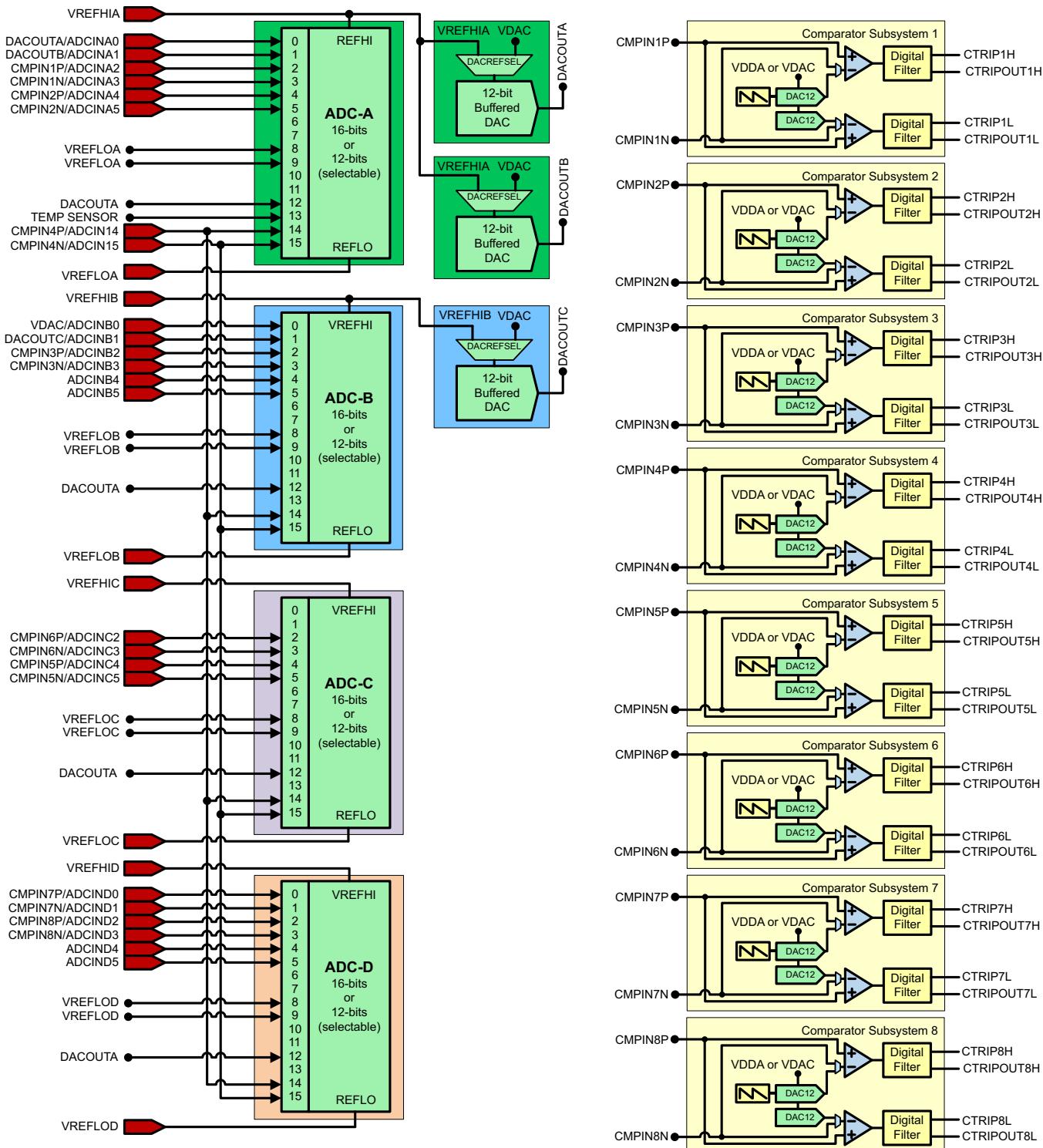
These pins fall into two categories: reference pins and analog module inputs/outputs. The reference pins, VREFHIA to VRFHID and VREFLOA to VREFLOD, can be used to externally supply the reference to the ADC. VREFHIA can also be used to supply the reference voltage to DAC A and DAC B and VREFHIB can be used to supply the reference to DAC C.

The analog module input/outputs are all ADC inputs by default. The pins which connect to CMPSS inputs can be used for the CMPSS without further action and without preventing use as an ADC input simultaneously. DAC outputs must be enabled; this will prevent the channel from simultaneously being used as an ADC input. Similarly, VDAC can be optionally used as a voltage reference for the DACs, but this will prevent the channel from simultaneously functioning as an ADC input.

The output of the temperature sensor can be enabled via the TSNCTL register and is available as an internal ADC input. The output of DACA as well as VREFLO can also be accessed via internal only ADC connections.

The block diagram for the analog subsystem is presented in [Figure 7-1](#).

Figure 7-1. Analog Subsystem Block Diagram

**NOTES:**

- Not all analog pins are available on all devices. Consult the datasheet for your specific device to determine which pins are available.
- Consult the datasheet for your device to determine the allowable voltage range for VREFHI and VREFLO if using external reference mode.

- An external capacitor is required on the VREFHI pins. Consult the datasheet for the specific value required.

7.1.3 Lock Registers

Setting the TSNSCTL bit in the LOCK register will disable any further changes in the TSNSCTL register.

7.2 Registers

7.2.1 Analog Subsystem Base Addresses

Table 7-1. Analog Subsystem Base Address Table

AnalogSubsysRegs ⁽¹⁾	ANALOG_SUBSYS_REGS	0x0005_D1A0	0x0005_D1FF
---------------------------------	--------------------	-------------	-------------

⁽¹⁾ Only available on CPU1.

7.2.2 ANALOG_SUBSYS_REGS Registers

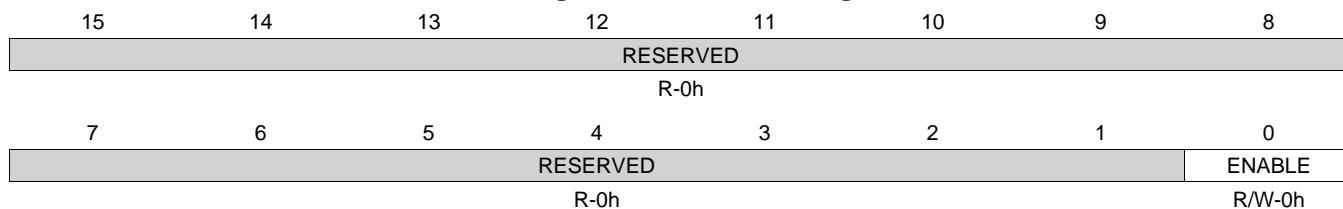
Table 7-2 lists the memory-mapped registers for the ANALOG_SUBSYS_REGS. All register offset addresses not listed in Table 7-2 should be considered as reserved locations and the register contents should not be modified.

Table 7-2. ANALOG_SUBSYS_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
26h	TSNSCTL	Temperature Sensor Control Register	Section 7.2.2.1	EALLOW
2Eh	LOCK	Lock Register	Section 7.2.2.2	EALLOW

7.2.2.1 TSNSCTL Register (offset = 26h) [reset = 0h]TSNSCTL is shown in [Figure 7-2](#) and described in [Table 7-3](#).

Temperature Sensor Control Register

Figure 7-2. TSNSCTL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 7-3. TSNSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	ENABLE	R/W	0h	Temperature Sensor Enable. This bit enables the temperature sensor output to the ADC. 0 Disabled 1 Enabled

7.2.2.2 LOCK Register (offset = 2Eh) [reset = 0h]

LOCK is shown in [Figure 7-3](#) and described in [Table 7-4](#).

Lock Register

Figure 7-3. LOCK Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	TSNSCTL	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R/WOnce-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 7-4. LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18-7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	TSNSCTL	R/WOnce	0h	Temperature Sensor Control Register Lock. Setting this bit will disable any future write to the respective register. This bit can only be cleared by a reset.
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

Analog-to-Digital Converter (ADC)

The analog-to-digital converter module described in this chapter is a Type 4 ADC. See the *TMS320C28xx, 28xxx DSP Peripheral Reference Guide* ([SPRU566](#)) for a list of all devices with modules of the same type, to determine the differences between the types, and for a list of device-specific differences within a type.

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8.1 Analog-to-Digital Converter (ADC)	1196
8.2 ADC Timings (TBD)	1215
8.3 Additional Information	1215
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8.1 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with selectable resolution of either 16 bits or 12 bits. This chapter refers to the analog circuits of the converter as the “core,” and includes the channel select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and includes logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

8.1.1 Features

Each ADC module consists of a single sample-and-hold (s/h) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC) based (see [SOC Principle of Operation](#)).

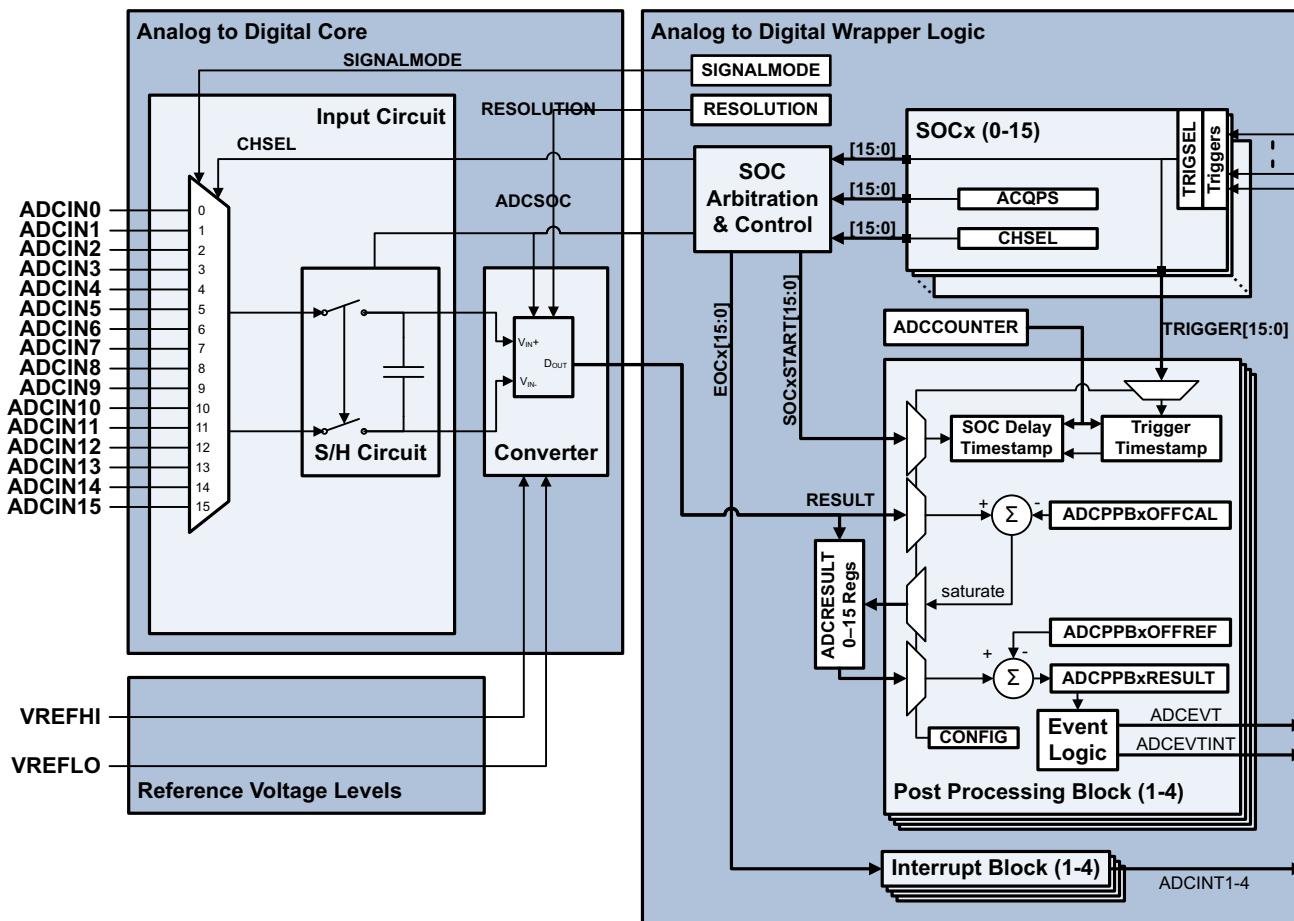
Each ADC has the following features:

- Selectable resolution of 16 bits or 12 bits
- Ratiometric external reference set by VREFHI\|VREFLO
- Differential signal conversions
- Single-ended signal conversions (12-bit mode only)
- Input multiplexer with up to 16 channels (single-ended) or 8 channels (differential)
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
 - S/W - software immediate start
 - All ePWMs - ADCSOC A,B,C, or D
 - GPIO XINT2
 - CPU Timers 0/1/2 (from each C28x core present)
 - ADCINT1/2
- Four flexible PIE interrupts
- Burst mode
- Four post-processing blocks, each with:
 - Saturating offset calibration
 - Error from setpoint calculation
 - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
 - Trigger-to-sample delay capture

NOTE: Not every channel may be pinned out from all ADCs. Check the datasheet for your device to determine which channels are available.

8.1.2 ADC Block Diagram

The block diagram for the ADC core and ADC wrapper are presented in [Figure 8-1](#).

Figure 8-1. ADC Module Block Diagram


8.1.3 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. [Table 8-1](#) summarizes the basic ADC options and their level of configurability. The subsequent sections discuss these configurations.

Table 8-1. ADC Options and Configuration Levels

Options	Configurability
Clock	Per module
Resolution (16-bits or 12-bits)	Per module
Signal mode (Differential or Single-Ended)	Per module
Trigger source	Per SOC
Converted channel	Per SOC
Acquisition window duration	Per SOC
EOC location	Per module
Burst Mode	Per module

8.1.3.1 Clock Configuration

The base ADC clock is provided directly by the system clock (SYSCLK). This clock is used to generate the ADC acquisition window. The register ADCCTL2 has a PRESCALE field which determines the ADCCLK. The ADCCLK is used to clock the converter.

NOTE: To determine an appropriate value for ADCCTL2.PRESCALE, consult the datasheet of your device to determine the maximum SYSCLK and ADCCLK frequency.

8.1.3.2 Resolution

The resolution of the ADC determines how finely the analog range is quantized into digital values. This ADC supports a configurable resolution of 16 bits or 12 bits. This can be configured by writing to the ADCCTL2.RESOLUTION register.

In 16-bit mode, the core requires 29 ADCLCK cycles to process a voltage into a conversion result, while in 12-bit mode, this process requires 10 ADCCLK cycles. The choice of resolution will also determine the necessary duration of the acquisition window, see [Choosing an Acquisition Window Duration](#).

8.1.3.3 Voltage Reference

Each ADC has a VREFHI input and a VREFLO input, which is used as a ratiometric reference.

See [Designing an External Reference Circuit](#) for information on how to supply the reference voltage.

NOTES:

- On devices with no external VREFLO signals, VREFLO has been internally connected to the device analog ground, VSSA.
- Consult the datasheet for your device to determine the allowable voltage range for VREFHI and VREFLO.
- The external reference mode requires an external capacitor on the VREFHI pin. Consult the device datasheet for the specific value required.

8.1.3.4 Signal Mode

The ADC supports two signal modes; single-ended and differential. In single-ended mode, the input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO (VSSA for internal reference mode). In differential signaling mode, the input voltage to the converter is sampled through a pair of input pins, of which one is the positive input (ADCINxP) and the other is the negative input (ADCINxN). The actual input voltage is the difference between the two ($\text{ADCINxP} - \text{ADCINxN}$).

NOTES:

- In 16-bit differential signaling mode, VREFLO must be connected to VSSA.
- In differential signal mode, the common mode voltage is
 $V_{CM} = (\text{ADCINxP} + \text{ADCINxN})/2$
 The datasheet for a particular device will place some requirements on how close this voltage needs to be to
 $(\text{VREFHI} + \text{VREFLO})/2$ (external reference mode)
- Differential signaling mode is advantageous because noise encountered on both inputs will be largely cancelled. The effect can be maximized by routing the positive and negative traces for the same differential input as close together as possible and keeping them symmetrical with respect to the signal reference.

8.1.3.5 Expected Conversion Results

Based on a given analog input voltage, the ideal expected digital conversion is given by the below tables. Fractional values are truncated.

Table 8-2. Analog-to-Digital Formulas

12-bit		
Single-Ended	ADCRESULTx = 0	when ADCINy ≤ VREFLO
	ADCRESULTx = 4096 $\left(\frac{\text{ADCINy} - \text{VREFLO}}{\text{VREFHI} - \text{VREFLO}} \right)$	when VREFLO < ADCINy < VREFHI
	ADCRESULTx = 4095	when ADCINy ≥ VREFHI
Differential	ADCRESULTx = 0	when ADCINyP - ADCINyN ≤ -RANGE ⁽¹⁾
	ADCRESULTx = 4096 $\left(\frac{\text{ADCINyP} - \text{ADCINyN} + \text{RANGE}}{2 \text{ RANGE}} \right)$	when -RANGE < ADCINyP - ADCINyN < RANGE ⁽¹⁾
	ADCRESULTx = 4095	when ADCINyP - ADCINyN ≥ RANGE ⁽¹⁾
16-bit		
Single-Ended Differential	Invalid Mode	Invalid Mode
	ADCRESULTx = 0	when -VREFHI < ADCINyP - ADCINyN < VREFHI
	ADCRESULTx = 65536 $\left(\frac{\text{ADCINyP} - \text{ADCINyN} + \text{VREFHI}}{2 \text{ VREFHI}} \right)$	
	ADCRESULTx = 65535	when ADCINyP - ADCINyN ≥ VREFHI

⁽¹⁾ RANGE = VREFHI - VREFLO

8.1.3.6 Interpreting Conversion Results

Based on a given ADC conversion result, the ideal corresponding analog input is given by the below tables. This corresponds to the center of the possible range of analog voltages that could have produced this conversion result.

Table 8-3. Digital-to-Analog Formulas, 12-Bit

12-bit		
Single-Ended	ADCINx ≤ VREFLO	when ADCRESULTy = 0
	$\text{ADCINx} = (\text{VREFHI} - \text{VREFLO}) \left(\frac{\text{ADCRESULTy}}{4096} \right) + \text{VREFLO}$	when $0 < \text{ADCRESULTy} < 4095$
	ADCINx ≥ VREFHI	when ADCRESULTy = 4095
Differential	$\text{ADCINxP} - \text{ADCINxN} \leq -\text{RANGE}$ ⁽¹⁾	when ADCRESULTy = 0
	$\text{ADCINxP} - \text{ADCINxN} = \text{RANGE}$ ⁽¹⁾ $\left(\frac{2 \text{ADCRESULTy}}{4096} - 1 \right)$	when $0 < \text{ADCRESULTy} < 4095$
	$\text{ADCINxP} - \text{ADCINxN} \geq \text{RANGE}$ ⁽¹⁾	when ADCRESULTy = 4095
16-bit		
Single-Ended	Invalid Mode	Invalid Mode
Differential	$\text{ADCINxP} - \text{ADCINxN} \leq -\text{VREFHI}$	when ADCRESULTy = 0
	$\text{ADCINxP} - \text{ADCINxN} = \text{VREFHI}$ $\left(\frac{2 \text{ADCRESULTy}}{65536} - 1 \right)$	when $0 < \text{ADCRESULTy} < 65535$
	$\text{ADCINxP} - \text{ADCINxN} \geq \text{VREFHI}$	when ADCRESULTy = 65535

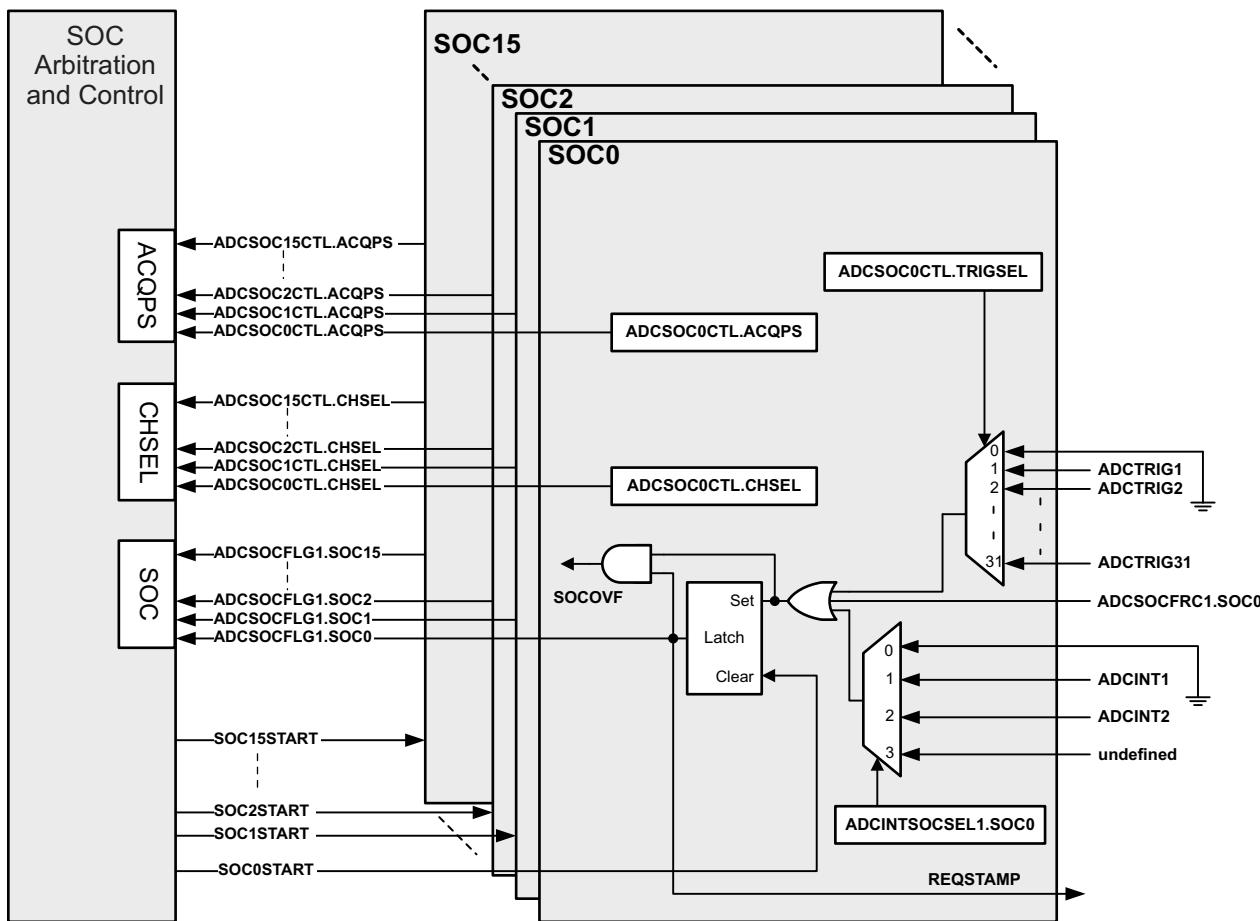
⁽¹⁾ RANGE = VREFHI - VREFLO

8.1.4 SOC Principle of Operation

The ADC triggering and conversion sequencing is accomplished through configurable start-of-conversions (SOCs). Each SOC is a configuration set defining the single conversion of a single channel. In that set there are three configurations: the trigger source that starts the conversion, the channel to convert, and the acquisition (sample) window duration. Upon receiving the trigger configured for a SOC, the wrapper will ensure that the specified channel is captured using the specified acquisition window duration.

Multiple SOCs can be configured for the same trigger, channel, and/or acquisition window as desired. Configuring multiple SOCs to use the same trigger will allow the trigger to generate a sequence of conversions. Configuring multiple SOCs to use the same trigger and channel will allow for oversampling.

Figure 8-2. SOC Block Diagram



8.1.4.1 SOC Configuration

Each SOC has its own configuration register, ADCSOCxCTL. Within this register, SOCx can be configured for trigger source, channel to convert, and acquisition (sample) window duration.

8.1.4.2 Trigger Operation

Each SOC can be configured to start on one of many input triggers. The primary trigger select for SOCx is in the ADCSOCxCTL.TRIGSEL register, which can select between:

- Disabled (software only)
 - CPU Timers 0/1/2 (from each C28x core present)
 - ADCEXTSOC (GPIO)
 - ePWM1 to ePWM12, ADCSOCA/C or ADCSOCB/D

In addition, each SOC can also be triggered when the ADCINT1 flag or ADCINT2 flag is set. This is achieved by configuring the ADCINTSOCSEL1 register (for SOC0 to SOC7) or the ADCINTSOCSEL2 register (for SOC8 to SOC15). This is useful for creating continuous conversions.

8.1.4.3 ADC Acquisition (Sample and Hold) Window

External signal sources vary in their ability to drive an analog signal quickly and effectively. In order to achieve rated resolution, the signal source needs to charge the sampling capacitor in the ADC core to within 0.5LSBs of the signal voltage. The acquisition window is the amount of time the sampling capacitor is allowed to charge and is configurable for SOCx by the ADCSOCxCTL.ACQPS register.

ACQPS is a 9-bit register that can be set to a value between 0 and 511, resulting in an acquisition window duration of:

$$\text{Acquisition window} = (\text{ACQPS} + 1) \cdot (\text{System Clock (SYSCLK) cycle time})$$

- The acquisition window duration is based off of the System Clock (SYSCLK), not the ADC clock (ADCCLK).
- The selected acquisition window duration must be at least as long as one ADCCLK cycle.
- The datasheet will specify a minimum acquisition window duration (in nanoseconds). The user is responsible for selecting an acquisition window duration that meets this requirement.

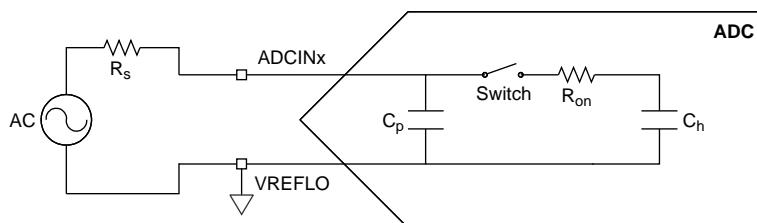
8.1.4.4 ADC Input Models

For single-ended operation, the ADC input characteristics are given by [Table 8-4](#) and [Figure 8-3](#).

Table 8-4. ADC Single-Ended Input

	Description	12-bit mode	16-bit mode
C _p	Parasitic input capacitance	3pF	N/A
R _{on}	Sampling switch resistance	1kΩ	N/A
C _h	Sampling capacitor	4.5pF	N/A
R _s	Nominal source impedance	50Ω	N/A

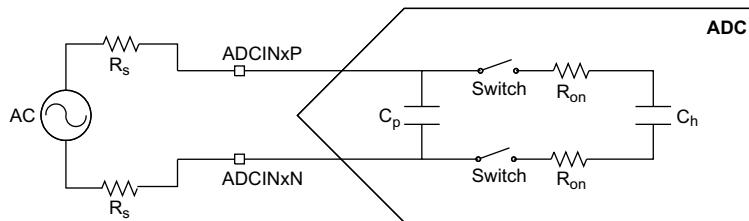
Figure 8-3. Single-Ended Input Diagram



For differential operation, the ADC input characteristics are given by [Table 8-5](#) and [Figure 8-4](#).

Table 8-5. ADC Differential Input

	Description	12-bit mode	16-bit mode
C _p	Parasitic input capacitance	1.5pF	1.5pF
R _{on}	Sampling switch resistance	1kΩ	1kΩ
C _h	Sampling capacitor	2.3pF	8.5pF
R _s	Nominal source impedance	50Ω	50Ω

Figure 8-4. Differential Input Diagram

These input models should be used along with actual signal source impedance to determine the acquisition window duration. See [Choosing an Acquisition Window Duration](#) for more information.

8.1.4.5 Channel Selection

Each SOC can be configured to convert any of the ADC channels. This behavior is selected for SOCx by the ADCSOCxCTL.CHSEL register. Depending on the signal mode, the selection is different. For single-ended signal mode, the value in CHSEL selects a single pin as the input. For differential signal mode, the value in CHSEL selects an even-odd pin pair to be the positive and negative inputs. This is summarized in [Table 8-6](#).

Table 8-6. Channel Selection of Input Pins

Input Mode	CHSEL	Input	
Single-Ended	0	ADCIN0	
	1	ADCIN1	
	2	ADCIN2	
	3	ADCIN3	
	4	ADCIN4	
	5	ADCIN5	
	6	ADCIN6	
	7	ADCIN7	
	8	ADCIN8	
	9	ADCIN9	
	10	ADCIN10	
	11	ADCIN11	
	12	ADCIN12	
	13	ADCIN13	
	14	ADCIN14	
	15	ADCIN15	
	CHSEL	Positive Input	Negative Input
Differential	0 and 8	ADCIN0	ADCIN1
	1 and 9	ADCIN2	ADCIN3
	2 and 10	ADCIN4	ADCIN5
	3 and 11	ADCIN6	ADCIN7
	4 and 12	ADCIN8	ADCIN9
	5 and 13	ADCIN10	ADCIN11
	6 and 14	ADCIN12	ADCIN13
	7 and 15	ADCIN14	ADCIN15

8.1.5 SOC Configuration Examples

The following sections provide some specific examples of how to configure the SOCs to produce some conversions.

8.1.5.1 Single Conversion from ePWM Trigger

To configure ADCA to perform a single conversion on channel ADCIN1 when the ePWM timer reaches its period match, a few things are necessary. First, ePWM3 must be configured to generate an SOCA, SOCB, SOCC, or SOCD signal (in this statement, SOC refers to a signal in the ePWM module). See the *Enhanced Pulse Width Modulator Module (ePWM)* chapter on how to do this. Assume that SOCB was chosen.

SOC5 is chosen arbitrarily. Any of the 16 SOCs could be used.

Assuming a 100ns sample window is desired with a SYSCLK frequency of 200MHz, then the acquisition window duration should be $100\text{ns}/5\text{ns} = 20$ SYSCLK cycles. The ACQPS field should therefore be set to $20 - 1 = 19$.

```
AdcaRegs.ADCSOC5CTL.bit.CHSEL = 1;           //SOC5 will convert ADCINA1
AdcaRegs.ADCSOC5CTL.bit.ACQPS = 19;          //SOC5 will use sample duration of 20 SYSCLK cycles
AdcaRegs.ADCSOC5CTL.bit.TRIGSEL = 10;         //SOC5 will begin conversion on ePWM3 SOCB/D
```

As configured, when ePWM3 matches its period and generates the SOCB signal, the ADC will begin sampling channel ADCINA1 (SOC5) immediately if the ADC is idle. If the ADC is busy, ADCINA1 will begin sampling when SOC5 gains priority (see [ADC Conversion Priority](#)). The ADC control logic will sample ADCINA1 with the specified acquisition window width of 100 ns. Immediately after the acquisition is complete, the ADC will begin converting the sampled voltage to a digital value. When the ADC conversion is complete, the results will be available in the ADCRESULT5 register (see [ADC Timings](#) for exact sample, conversion, and result latch timings).

8.1.5.2 Oversampled Conversion from ePWM Trigger

To configure the ADC to oversample ADCINA1 4 times, we use the same configurations as the previous example, but apply them to SOC5, SOC6, SOC7, and SOC8.

```
AdcaRegs.ADCSOC5CTL.bit.CHSEL = 1;           //SOC5 will convert ADCINA1
AdcaRegs.ADCSOC5CTL.bit.ACQPS = 19;          //SOC5 will use sample duration of 20 SYSCLK cycles
AdcaRegs.ADCSOC5CTL.bit.TRIGSEL = 10;         //SOC5 will begin conversion on ePWM3 SOCB/D
AdcaRegs.ADCSOC6CTL.bit.CHSEL = 1;           //SOC6 will convert ADCINA1
AdcaRegs.ADCSOC6CTL.bit.ACQPS = 19;          //SOC6 will use sample duration of 20 SYSCLK cycles
AdcaRegs.ADCSOC6CTL.bit.TRIGSEL = 10;         //SOC6 will begin conversion on ePWM3 SOCB/D
AdcaRegs.ADCSOC7CTL.bit.CHSEL = 1;           //SOC7 will convert ADCINA1
AdcaRegs.ADCSOC7CTL.bit.ACQPS = 19;          //SOC7 will use sample duration of 20 SYSCLK cycles
AdcaRegs.ADCSOC7CTL.bit.TRIGSEL = 10;         //SOC7 will begin conversion on ePWM3 SOCB/D
AdcaRegs.ADCSOC8CTL.bit.CHSEL = 1;           //SOC8 will convert ADCINA1
AdcaRegs.ADCSOC8CTL.bit.ACQPS = 19;          //SOC8 will use sample duration of 20 SYSCLK cycles
AdcaRegs.ADCSOC8CTL.bit.TRIGSEL = 10;         //SOC8 will begin conversion on ePWM3 SOCB/D
```

As configured, when ePWM3 matches its period and generates the SOCB signal, the ADC will begin sampling channel ADCINA1 (SOC5) immediately if the ADC is idle. If the ADC is busy, ADCINA1 will begin sampling when SOC5 gains priority (see [ADC Conversion Priority](#)). Once the conversion is complete for SOC5, SOC6 will begin converting ADCINA1 and the results for SOC5 will be placed in the ADCRESULT5 register. All 4 conversions will eventually be completed sequentially, with the results in ADCRESULT5, ADCRESULT6, ADCRESULT7, and ADCRESULT8 for SOC5, SOC6, SOC7, and SOC8, respectively.

NOTE: It is possible, but unlikely, that the ADC could begin converting SOC6, SOC7, or SOC8 before SOC5 depending on the position of the round-robin pointer when the ePWM trigger is received. See [ADC Conversion Priority](#) to understand how the next SOC to be converted is chosen.

8.1.5.3 Multiple Conversions from CPU Timer Trigger

This example will show how to sample multiple signals with different acquisition window requirements. CPU1 Timer 2 will be used to generate the trigger. To see how to configure the CPU timer, see the *System Control and Interrupts* chapter.

A good first step when designing a sampling scheme with many signals is to list out the signals and their required acquisition window. From this, calculate the necessary number of SYSCLK cycles for each signal, then the ACQPS register setting. This is shown in [Table 8-7](#), where a SYCLK of 200MHz is assumed (5ns cycle time).

Table 8-7. Example Requirements for Multiple Signal Sampling

Signal Name	Acquisition Window Requirement (ns)	Acquisition Window SYSCLK Cycles	ACQPS Register Value
Signal 1	>120 ns	120ns/5ns = 24	24 – 1 = 23
Signal 2	>444 ns	444ns/5ns = 89 (round up)	89 – 1 = 88
Signal 3	>110 ns	110ns/5ns = 22	22 – 1 = 21
Signal 4	>291 ns	291ns/5ns = 59 (round up)	59 – 1 = 58

Next decide which ADC pins to connect to each signal. This will be highly dependent on application board layout. Once the pins are selected, determining the value of CHSEL is straightforward (see [Table 8-8](#)).

Table 8-8. Example Connections for Multiple Signal Sampling

Signal Name	ADC PIN	CHSEL Register Value
Signal 1	ADCINA5	5
Signal 2	ADCINA0	0
Signal 3	ADCINA3	3
Signal 4	ADCINA2	2

With the information tabulated, it is easy to generate the SOC configurations:

```
AdcaRegs.ADCSOC0CTL.bit.CHSEL = 5;           //SOC0 will convert ADCINA5
AdcaRegs.ADCSOC0CTL.bit.ACQPS = 23;           //SOC0 will use sample duration of 24 SYSCLK cycles
AdcaRegs.ADCSOC0CTL.bit.TRIGSEL = 3;           //SOC0 will begin conversion on CPU1 Timer 2
AdcaRegs.ADCSOC1CTL.bit.CHSEL = 0;             //SOC1 will convert ADCINA0
AdcaRegs.ADCSOC1CTL.bit.ACQPS = 88;            //SOC1 will use sample duration of 89 SYSCLK cycles
AdcaRegs.ADCSOC1CTL.bit.TRIGSEL = 3;           //SOC1 will begin conversion on CPU1 Timer 2
AdcaRegs.ADCSOC2CTL.bit.CHSEL = 3;             //SOC2 will convert ADCINA3
AdcaRegs.ADCSOC2CTL.bit.ACQPS = 21;            //SOC2 will use sample duration of 22 SYSCLK cycles
AdcaRegs.ADCSOC2CTL.bit.TRIGSEL = 3;           //SOC2 will begin conversion on CPU1 Timer 2
AdcaRegs.ADCSOC3CTL.bit.CHSEL = 2;             //SOC3 will convert ADCINA2
AdcaRegs.ADCSOC3CTL.bit.ACQPS = 58;            //SOC3 will use sample duration of 59 SYSCLK cycles
AdcaRegs.ADCSOC3CTL.bit.TRIGSEL = 3;           //SOC3 will begin conversion on CPU1 Timer 2
```

As configured, when CPU1 Timer 2 generates an event, SOC0, SOC1, SOC2, and SOC3 will eventually be sampled and converted, in that order. The conversion results for ADCINA5 (Signal 1) will be in ADCRESULT0. Similarly, The results for ADCINA0 (Signal 2), ADCINA3 (Signal 3), and ADCINA2 (Signal 4) will be in ADCRESULT1, ADCRESULT2, and ADCRESULT3, respectively.

NOTE: It is possible, but unlikely, that the ADC could begin converting SOC1, SOC2, or SOC3 before SOC0 depending on the position of the round-robin pointer when the CPU Timer trigger is received. See [ADC Conversion Priority](#) to understand how the next SOC to be converted is chosen.

8.1.5.4 Software Triggering of SOCs

At any point, whether or not the SOCs have been configured to accept a specific trigger, a software trigger can set the SOCs to be converted. This is accomplished by writing bits in the ADCSOCFRC1 register.

Software triggering of the previous example without waiting for the CPU1 Timer 2 to generate the trigger could be accomplished by the statement:

```
AdcaRegs.ADCSOCFRC1.all = 0x000F;           //set SOC flags for SOC0 to SOC3
```

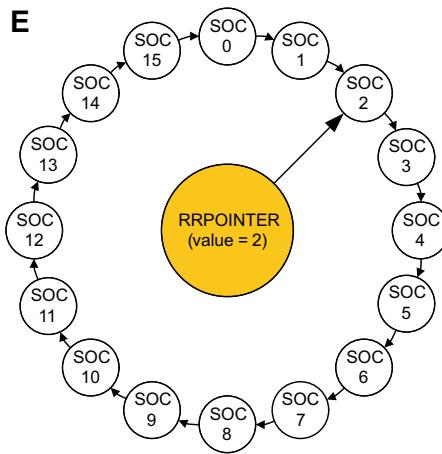
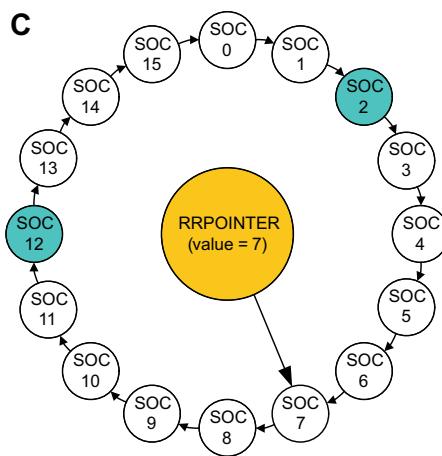
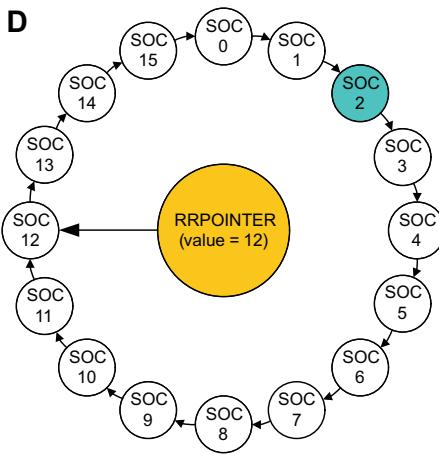
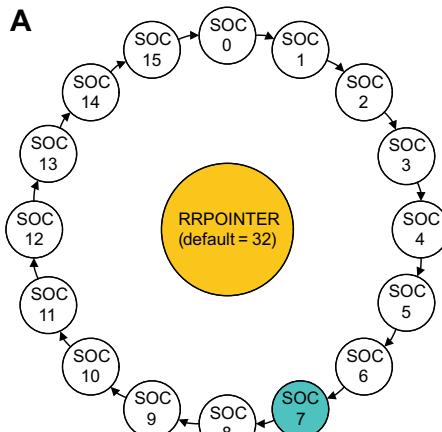
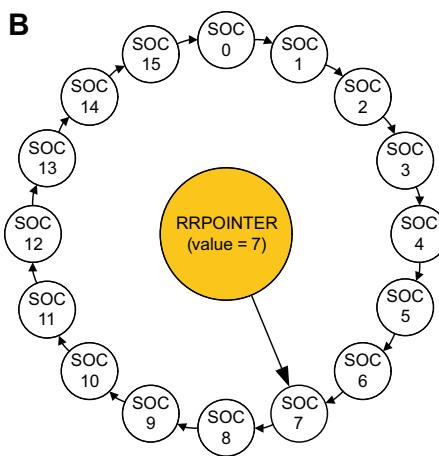
8.1.6 ADC Conversion Priority

When multiple SOC flags are set at the same time, one of two forms of priority determines the order in which they are converted. The default priority method is round robin. In this scheme, no SOC has an inherent higher priority than another. Priority depends on the round robin pointer (RRPOINTER). The RRPOINTER reflected in the ADCSOCPRIORTYCTL register points to the last SOC converted. The highest priority SOC is given to the next value greater than the RRPOINTER value, wrapping around back to SOC0 after SOC15. At reset the value is 32 since 0 indicates a conversion has already occurred. When RRPOINTER equals 32 the highest priority is given to SOC0. The RRPOINTER is reset by a device reset, when the ADCCTL1.RESET bit is set, or when the SOCPRICTL register is written.

An example of the round robin priority method is given in [Figure 8-5](#).

Figure 8-5. Round Robin Priority Example

- A** After reset, SOC0 is highest priority SOC ;
SOC7 receives trigger ;
SOC7 configured channel is converted immediately .
- B** RRPOINTER changes to point to SOC 7 ;
SOC8 is now highest priority SOC .
- C** SOC2 & SOC12 triggers rcvd . simultaneously ;
SOC12 is first on round robin wheel ;
SOC12 configured channel is converted while
SOC2 stays pending .
- D** RRPOINTER changes to point to SOC 12 ;
SOC2 configured channel is now converted .
- E** RRPOINTER changes to point to SOC 2 ;
SOC3 is now highest priority SOC .



The SOCPRIORITY field in the ADCSOCPRIORITYCTL register can be used to assign high priority from a single to all of the SOC's. When configured as high priority, an SOC will interrupt the round robin wheel after any current conversion completes and insert itself in as the next conversion. After its conversion completes, the round robin wheel will continue where it was interrupted. If two high priority SOC's are triggered at the same time, the SOC with the lower number will take precedence.

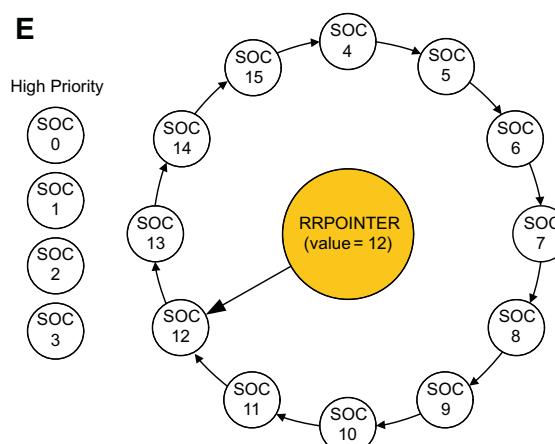
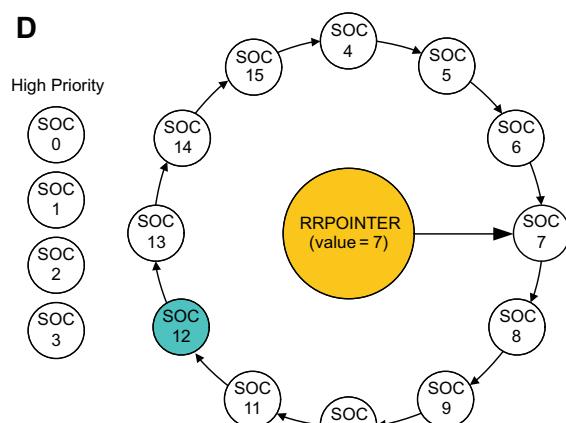
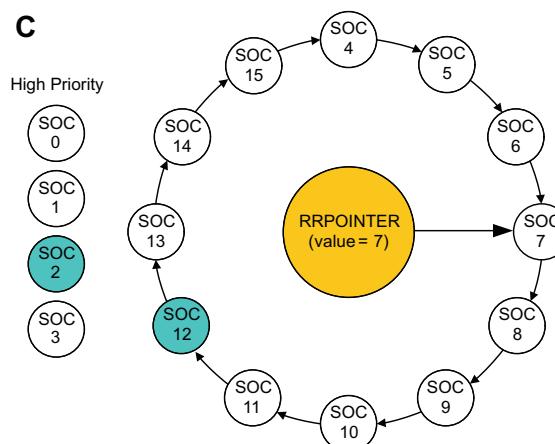
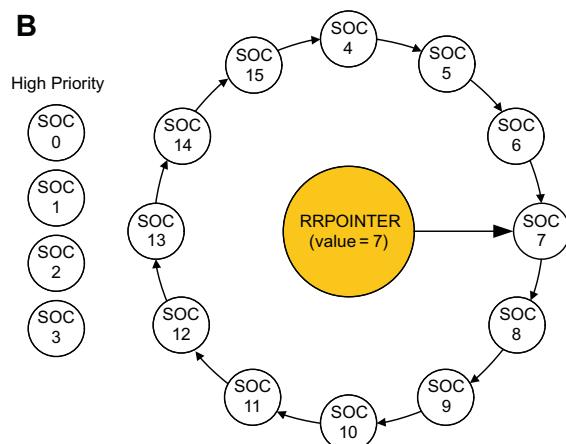
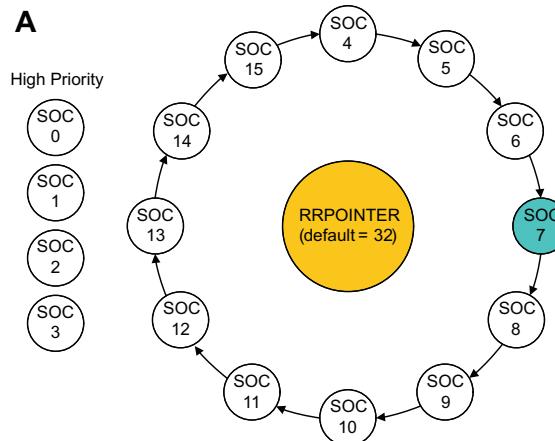
High priority mode is assigned first to SOC0, then in increasing numerical order. The value written in the SOCPRIORITY field defines the first SOC that is not high priority. In other words, if a value of 4 is written into SOCPRIORITY, then SOC0, SOC1, SOC2, and SOC3 are defined as high priority, with SOC0 the highest.

An example using high priority SOC's is given in [Figure 8-6](#).

Figure 8-6. High Priority Example

Example when SOCPRIORITY = 4

- A After reset, SOC4 is 1st on round robin wheel ;
SOC7 receives trigger;
SOC7 configured channel is converted immediately .
- B RRPOINTER changes to point to SOC 7;
SOC8 is now 1st on round robin wheel .
- C SOC2 & SOC12 triggers rcvd. simultaneously ;
SOC2 interrupts round robin wheel and SOC 2 configured channel is converted while SOC 12 stays pending .
- D RRPOINTER stays pointing to 7;
SOC12 configured channel is now converted .
- E RRPOINTER changes to point to SOC 12;
SOC13 is now 1st on round robin wheel .



8.1.7 Burst Mode

Burst mode allows a single trigger to walk through the round-robin SOCs one or more at a time. Setting the bit BURSTEN in the ADCBURSTCTL register configures the ADC wrapper for burst mode. This causes the TRIGSEL field to be ignored, but only for SOCs that are configured for round-robin operation (not high priority). Instead of the TRIGSEL field, all round-robin SOCs are triggered based on the BURSTTRIG field in the ADCBURSTCTL register. Upon reception of the burst trigger, the ADC wrapper will not set all round-robin SOCs to be converted, but only (ADCBURSTCTL.BURSTSIZEx1) SOCs. The first SOC to be set will be that with the highest priority based on the round-robin pointer, and subsequent SOCs will be set until BURSTSIZEx1 SOCs have been set.

NOTE: When configuring the ADC for burst mode, the user is responsible for ensuring that each burst of conversions is allowed to complete before the next burst trigger is received.

8.1.7.1 Burst Mode Example

Burst mode can be used to sample a different set of signals on every other trigger. In the following example, ADCIN7 and ADCIN5 are converted on the first trigger from CPU1 Timer 2 and every other trigger thereafter. ADCIN2 and ACIN3 are converted on the second trigger from CPU1 Timer 2 and every other trigger thereafter. All signals are converted with 20 SYSCLK cycle wide acquisition windows, but different durations could be configured for each SOC as desired.

```
AdcaRegs.BURSTCTL.BURSTEN = 1;           //Enable ADC burst mode
AdcaRegs.BURSTCTL.BURSTTRIG = 3;          //CPU1 Timer 2 will trigger burst of conversions
AdcaRegs.BURSTCTL.BURSTSIZEx1 = 1;         //conversion bursts are 1 + 1 = 2 conversions long

AdcaRegs.SOCPRICCTL.bit.SOCPPRIORITY = 12; //SOC0 to SOC11 are high priority

AdcaRegs.ADCSOC12CTL.bit.CHSEL = 7;        //SOC12 will convert ADCINA7
AdcaRegs.ADCSOC12CTL.bit.ACQPS = 19;       //SOC12 will use sample duration of 20 SYSCLK cycles
AdcaRegs.ADCSOC13CTL.bit.CHSEL = 5;        //SOC13 will convert ADCINA5
AdcaRegs.ADCSOC13CTL.bit.ACQPS = 19;       //SOC13 will use sample duration of 20 SYSCLK cycles
AdcaRegs.ADCSOC14CTL.bit.CHSEL = 2;         //SOC14 will convert ADCINA2
AdcaRegs.ADCSOC14CTL.bit.ACQPS = 19;       //SOC14 will use sample duration of 20 SYSCLK cycles
AdcaRegs.ADCSOC15CTL.bit.CHSEL = 3;         //SOC15 will convert ADCINA3
AdcaRegs.ADCSOC15CTL.bit.ACQPS = 19;       //SOC15 will use sample duration of 20 SYSCLK cycles
```

When the first CPU1 Timer 2 trigger is received, SOC12 and SOC13 will be converted immediately if the ADC is idle. If the ADC is busy, SOC12 and SOC13 will be converted once their SOCs gain priority. The results for SOC12 and SOC13 will be in ADCRESULT12 and ADCRESULT13, respectively. After SOC13 completes, the round robin pointer will give highest priority to SOC14. Because of this, when the next CPU1 Timer 2 trigger is received, SOC14 and SOC15 will be set as pending and eventually be converted. The results for SOC14 and SOC15 will be in ADCRESULT14 and ADCRESULT15, respectively. Subsequent triggers will continue to toggle between converting SOC12 and SOC13, and converting SOC14 and SOC15.

While the above example toggles between two sets of conversions, three or more different sets of conversions could be achieved using a similar approach.

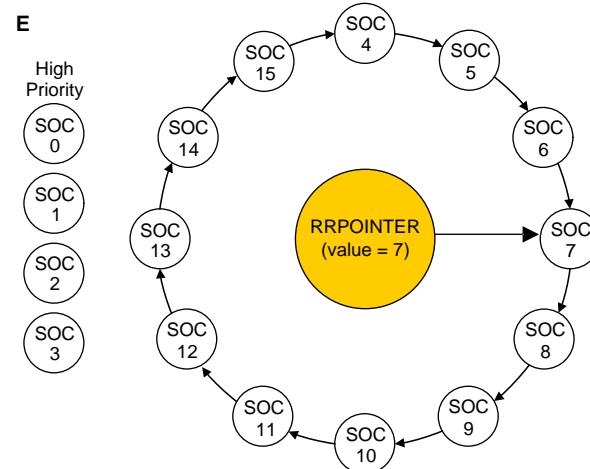
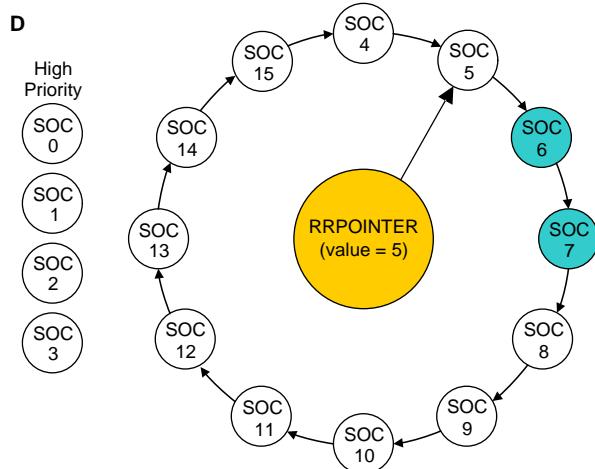
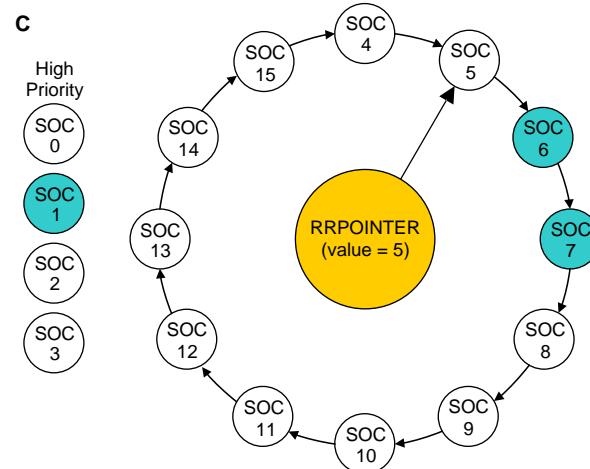
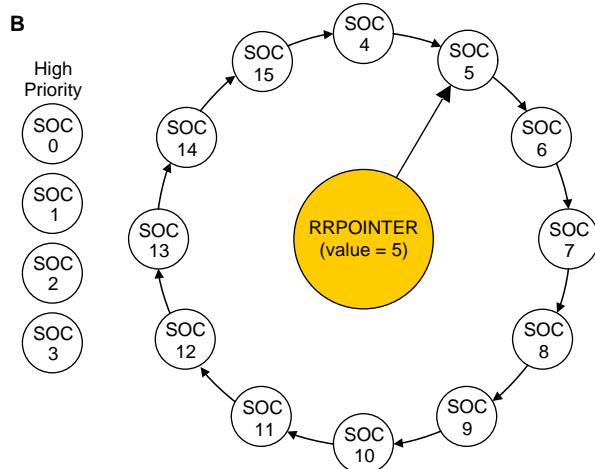
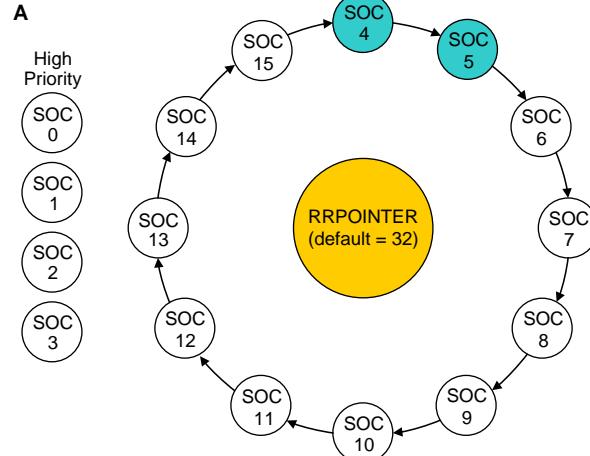
8.1.7.2 Burst Mode Priority Example

An example of priority resolution using burst mode and high-priority SOCs is presented in [Figure 8-7](#).

Figure 8-7. ADC Burst Priority

Example when SOC_PRIORITY = 4, BURSTEN = 1, and BURSTSIZE = 1

- A After reset, SOC4 is 1st on round robin wheel; BURSTTRIG trigger is received; SOC4 & SOC5 are set and configured channels converted immediately.
- B RRPOINTER changes to point to SOC5; SOC6 is now 1st on round robin wheel.
- C BURSTTRIG & SOC1 triggers rcvd. simultaneously; SOC1, SOC6, and SOC7 are set; SOC1 interrupts round robin wheel and SOC1 configured channel is converted while SOC6 and SOC7 stay pending.
- D RRPOINTER stays pointing to 5; SOC6/SOC7 configured channels are now converted.
- E RRPOINTER changes to point to SOC7; SOC8 is now 1st on round robin wheel, waiting for BURSTTRIG.



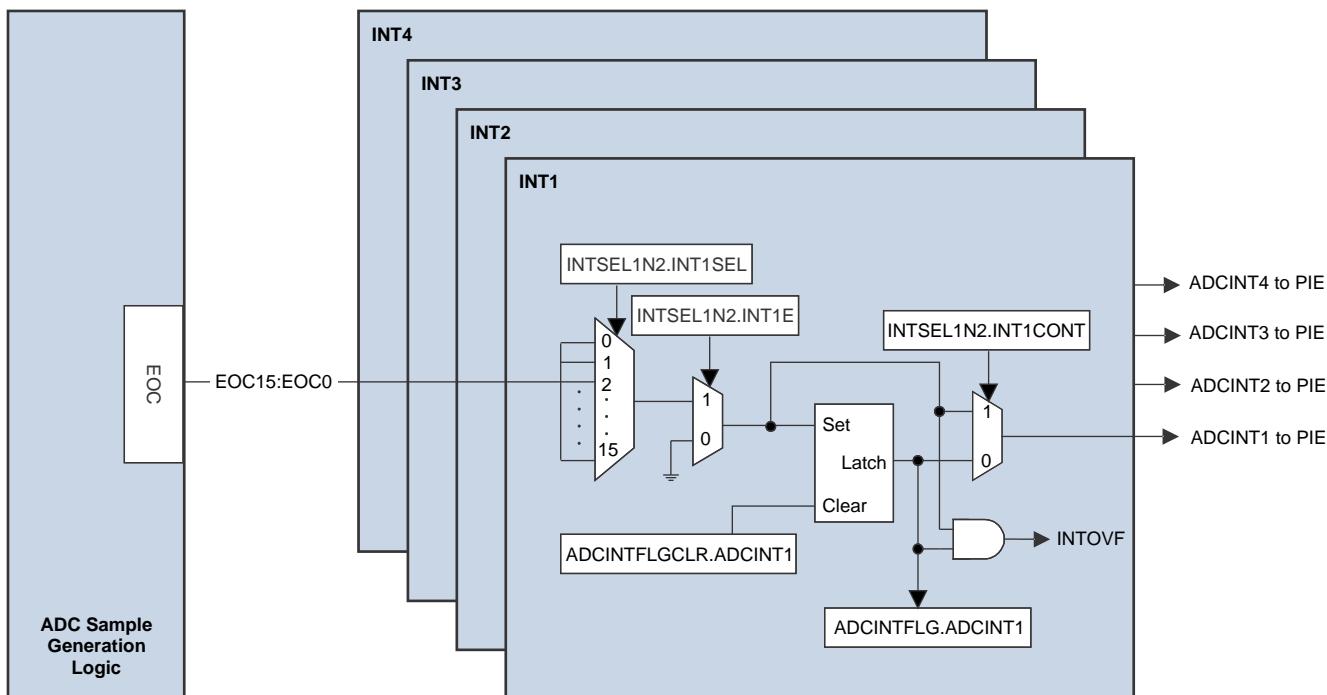
8.1.8 EOC and Interrupt Operation

Each SOC has a corresponding end-of-conversion (EOC) signal. This EOC signal can be used to trigger an ADC interrupt. The ADC can be configured to generate the EOC pulse at either the end of the acquisition window or at the end of the voltage conversion. This is configured using the bit INTPULSEPOS in the ADCCTL1 register. See [ADC Timings](#), for exact EOC pulse location.

Each ADC module has 4 configurable ADC interrupts. These interrupts can be triggered by any of the 16 EOC signals. The flag bit for each ADCINT can be read directly or the interrupt can be passed on to the PIE.

[Figure 8-8](#) shows a block diagram of the ADC interrupt structure.

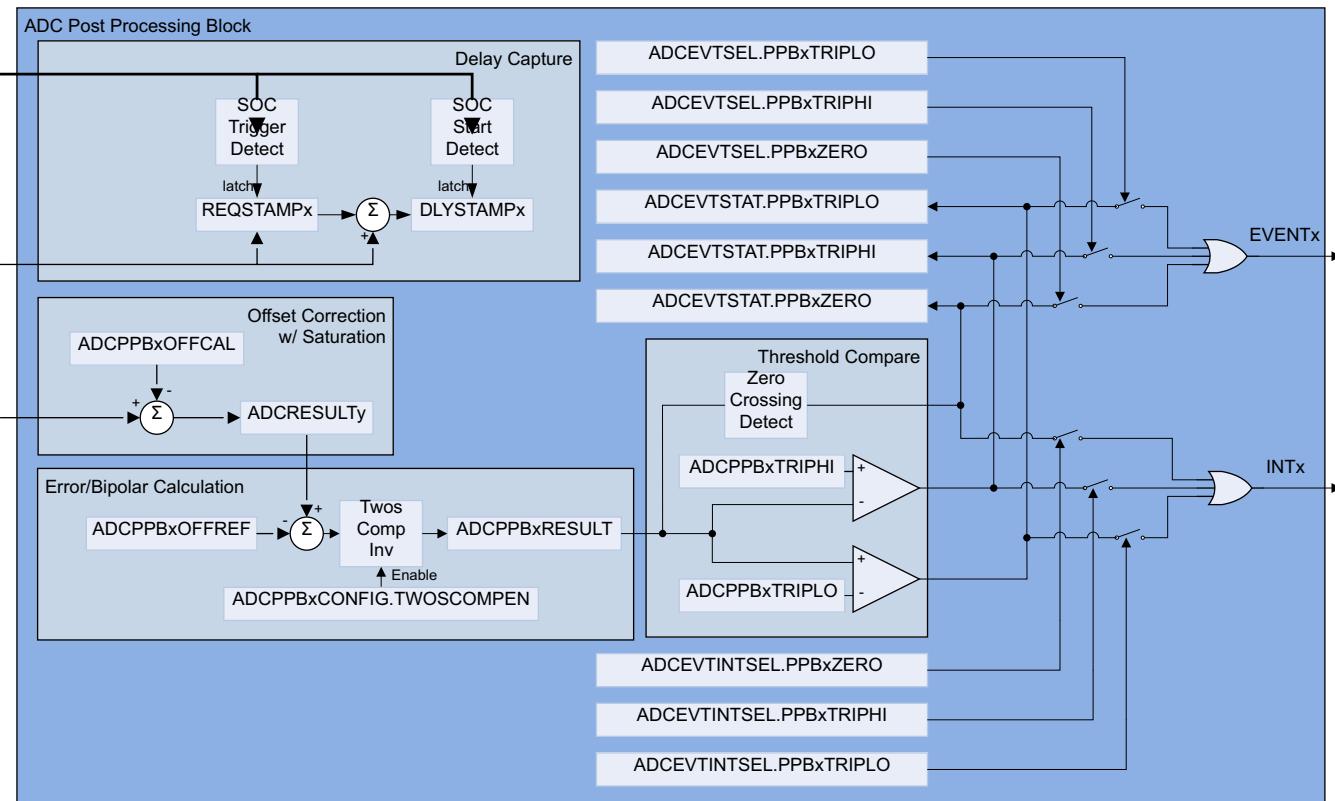
Figure 8-8. ADC EOC Interrupts



8.1.9 Post-Processing Blocks

Each ADC module contains four post-processing blocks (PPB). These blocks can be associated with any of the 16 RESULT registers using the ADCPPBxCONFIG.CONFIG bit field. Each PPB can simultaneously remove an offset associated with the ADCIN channel, subtract out a reference value, flag a zero-crossing point, and flag a high or low compare limit. Furthermore, the zero-crossing and compare flags can trip a PWM and/or generate an interrupt. A PPB is also capable of recording the delay between when the SOC associated with the PPB is triggered and when it actually begins to be sampled. [Figure 8-9](#) presents the structure of each PPB. Subsequent sections explain the use of each submodule.

Figure 8-9. ADC PPB Block



8.1.9.1 PPB Offset Correction

In many applications, external sensors and signal sources produce an offset. A global trimming of the ADC offset is not enough to compensate for these offsets, which vary from channel to channel. The post-processing block can remove these offsets with zero overhead, saving numerous cycles in tight control loops.

Offset correction is accomplished by first pointing the ADCPPBxCONFIG.CONFIG to the desired SOC, then writing an offset correction value to the ADCPPBxOFFCAL.OFFCAL register. The post-processing block will automatically add or subtract the value in the OFFCAL register from the raw conversion result and store it in the ADCRESULT register. This addition/subtraction will saturate at 0 on the low end and either 4095 or 65535 on the high end for 12-bit or 16-bit mode, respectively.

NOTES:

- Writing a 0 to the OFFCAL register effectively disables the offset correction feature, passing the raw result unchanged to the ADCRESULT register.
- It is possible to point multiple PPBs to the same SOC. In this case, the OFFCAL value that will actually be applied will be that of the PPB with the highest number.
- In particular, care needs to be taken when using the PPB on SOC0, as all the PPB point to this SOC by default. This may cause unintentional overwriting of offset correction of a lower numbered PPB by a higher numbered PPB.

8.1.9.2 PPB Error Calculation

In many applications, an error from a setpoint or expected value must be computed from the digital output of an ADC conversion. In other cases, a bipolar signal is necessary or convenient for control calculations. The PPB can perform these function automatically, reducing the sample to output latency and reducing software overhead.

Error calculation is accomplished by first pointing the ADCPPBxCONFIG.CONFIG to the desired SOC, then writing a value to the ADCPPBxOFFCAL.OFFREF register. The post-processing block will automatically subtract the value in the OFFREF register from the ADCRESULT value and store it in the ADCPPBxRESULT register. This subtraction will produce a sign-extended 32-bit result. It is also possible to selectively invert the calculated value before storing in the ADCPPBxRESULT register by setting the TWOSCOMPEN bit in the ADCPPBxCONFIG register.

NOTES:

- In 12-bit mode, do not write a value larger than 12 bits to the OFFREF register.
- Since the PPBxRESULT register is unique for each PPB, it is possible to point multiple PPBs to the same SOC and get different results for each PPB.
- Writing a 0 to the OFFREF register effectively disables the error calculation feature, passing the ADCRESULT value unchanged to the ADCPPBxRESULT register.

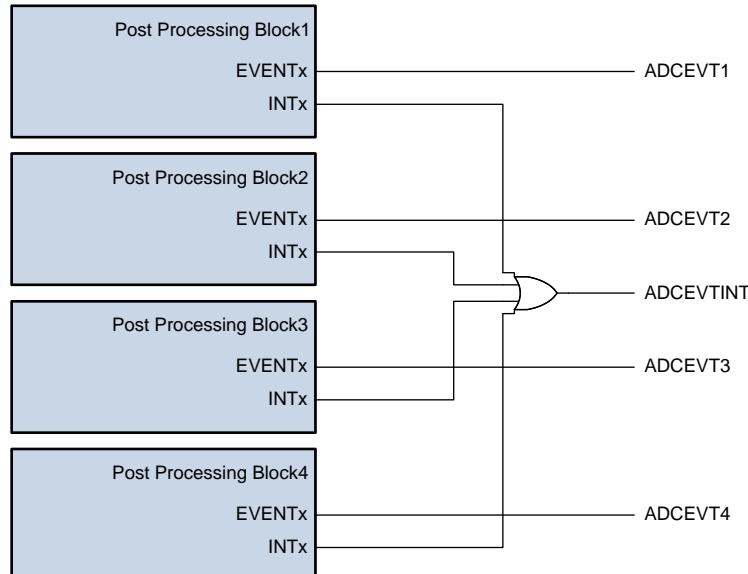
8.1.9.3 PPB Limit Detection and Zero-Crossing Detection

Many applications perform a limit check against the ADC conversion results. The PPB can automatically perform a check against a high and low limit or whenever ADCPPBxRESULT changes sign. Based on these comparisons, it can generate a trip to the PWM and/or an interrupt automatically, lowering the sample to ePWM latency and reducing software overhead. This functionality also enables safety conscious applications to trip the ePWM based on an out-of-range ADC conversion without any CPU intervention.

To enable this functionality, first point the ADCPPBxCONFIG.CONFIG to the desired SOC, then write a value to one or both of the registers ADCPPBxTRIPHI.LIMITHI and ADCPPBxTRIPLO.LIMITLO (zero-crossing detection does not require further configuration). Whenever these limits are exceeded, the PPBxTRIPHI bit or PPBxTRIPLO bit will be set in the ADCEVTSTAT register. Whenever the ADCPPBxRESULT changes sign, the PPBxZERO bit will be set in the ADCEVTSTAT register. The ADCEVTCLR register has corresponding bits to clear these event flags. The ADCEVTSEL register has corresponding bits which allow the events to propagate through to the PWM. The ADCINTSEL register has corresponding bits which allow the events to propagate through to the PIE.

One PIE interrupt is shared between all the PPBs for a given ADC module as shown in [Figure 8-10](#).

Figure 8-10. ADC PPB Interrupt Event

**NOTES:**

- Zero-crossing and limit compare reference the ADCPPBxRESULT register. This will include any correction applied by the OFFCAL and OFFREF registers. TRIPHI and TRIPLO do NOT perform a signed comparison. It is recommended to leave OFFREF as 0 when using limit compare functionality.

- If different actions need to be taken for different PPB events from the same ADC module, then the ADCEVTINT ISR will have to read the PPB event flags in the ADCEVTSTAT register to determine which event caused the interrupt.
- If different ePWM trips need to be generated separately for high compare, low compare, and/or zero-crossing, this can be achieved by pointing multiple PPBs to the same SOC.

8.1.9.4 PPB Sample Delay Capture

When multiple control loops are running asynchronously on the same ADC, there is a chance that an ADC request from two or more loops will collide, causing one of the samples to be delayed. This shows up as a measurement error in the system. By knowing when this delay occurs and the amount of delay that has occurred software can employ extrapolation techniques to reduce the error.

To this effect, each PPB has the field DLYSTAMP in the ADCPPBxSTAMP register. This field will contain the number of SYSCLK cycles between when the associate SOC was triggered and when it began converting.

This is achieved by having a global 12-bit free running counter based off of SYSCLK, which is in the field FREECOUNT in the ADCCOUNTER register. When the trigger for the associated SOC arrives, the value of this counter is loaded into the bit field ADCPPBxTRIPLO.REQSTAMP. When the actual sample window for that SOC begins, the value in REQSTAMP is subtracted from the current FREECOUNT value and stored in DLYSTAMP.

NOTE: If more than $212 = 4096$ SYSCLK cycles elapse between the SOC trigger and the actual start of the SOC acquisition, the FREECOUNT register may overflow more than once, leading to incorrect DLYSTAMP value. Be cautious when using very slow conversions to prevent this from happening.

NOTE: The sample delay capture will not function if the associated SOC is triggered via software. It will, however, correctly record the delay if the software triggering of a different SOC causes the SOC associated with the PPB to be delayed

8.1.10 Power Up Sequence

Upon device power-up or system level reset, the ADC will be powered down and disabled. When powering up the ADC, use the following sequence:

1. Set the bit to enable the desired ADC clock in the PCLKCR13 register.
2. Set the desired ADC clock divider in the PRESCALE field of ADCCTL2.
3. Power up the ADC by setting the ADCPWDNZ bit in ADCCTL1.
4. Allow at least 1ms delay before sampling.

If multiple ADCs are powered up simultaneously, steps 1 and step 3 can each be done for all ADCs in one write instruction. Also, only one delay is necessary as long as it occurs after all the ADCs have begun powering up.

8.1.11 ADC Calibration

During the fabrication and test process, Texas Instruments calibrates the ADC as the internal oscillators and the DACs. These trim settings are embedded into TI reserved OTP memory as part of a C-callable function named Device_cal(). This function copies the trim values stored in OTP memory to their respective trim registers. Until this occurs, the ADC (and other modules) will not be guaranteed to operate within datasheet specifications. Similarly, if trim values other than the factory settings are placed into the trim registers, the ADC (and other modules) will not be guaranteed to operate within datasheet specifications.

The boot ROM will call the Device_cal() function, so correct trim values should be populated without user intervention. However, if the trims are cleared due to a module reset or modified for some other reason, then the user can call the Device_cal() function (defined in the headerfiles) or can use a gel script function provided with the header files.

8.1.11.1 ADC Zero Offset Calibration

Zero offset error is defined as the resultant digital value that occurs when converting a voltage at VREFLO. This base error affects all conversions of the ADC and together with the full scale gain and linearity specifications, determine the DC accuracy of a converter. The zero offset error can be positive, meaning that a positive digital value is output when VREFLO is presented, or negative, meaning that a voltage higher than a one step above VREFLO still reads as a digital zero value. To correct this error, the two's complement of the error is written into the ADCOFFTRIM register. The value contained in this register will be applied before the results are available in the ADC result registers. This operation is fully contained within the ADC core, so the timing for the results will not be affected and the full dynamic range of the ADC will be maintained for any trim value. Calling the Device_cal() function writes the ADCOFFTRIM register with the factory calibrated offset error correction, but the user can modify the ADCOFFTRIM register to compensate for additional offset error induced by the application environment. This can be done without sacrificing an ADC channel by using an internal channel, connected to VREFLO.

Use the following procedure to re-calibrate the ADC offset:

1. **Set ADCOFFTRIM to 80 (50h).** This adds an artificial offset to account for negative offset that may reside in the ADC core.
2. **Perform multiple conversions on VREFLO and take an average to account for board noise..**
3. **Set ADCOFFTRIM to 80 (50h) minus the average obtained in step 3.** This removes the artificial offset from step 1 and creates a two's compliment of the offset error.

8.2 ADC Timings (TBD)

TBD

8.3 Additional Information

The following sections contain additional practical information.

8.3.1 Choosing an Acquisition Window Duration

For correct operation, the input signal to the ADC must be allowed adequate time to charge the sample and hold capacitor, Ch. Typically, the S+H duration is chosen such that the sampling capacitor will be charged to within $\frac{1}{2}$ LSB or $\frac{1}{4}$ LSB of the final value, depending on tolerable settling error. A rough approximation of the required sampling time can be determined using a first-order RC model with $R = R_s + R_{on}$ and $C = Ch$. The RC time constant is then $(R_s + R_{on}) \cdot (Ch)$. The required number of time constants is:

$$t = -\ln\left(\frac{\text{settling accuracy (LSBs)}}{2^N}\right)$$

For example, assuming desired accuracy is $\frac{1}{4}$ LSB, resolution is 12-bits, $R_s = 1k\Omega$, $R_{on} = 1k\Omega$, and $Ch = 4.5pF$.

$$t = -\ln\left(\frac{\text{settling accuracy (LSBs)}}{2^N}\right) T$$

$$t = -\ln\left(\frac{0.25}{2^{12}}\right) (2k\Omega \cdot 4.5 \text{ pf}) = 87 \text{ ns}$$

The sample and hold window duration for this ADC is

$$T_{S+H} = (ACQPS + 1) \frac{1}{SYSCLK}$$

If SYSCLK = 200MHz, then 1/SYSCLK = 5ns, and 1+ACQPS should therefore be chosen to be 18, giving ACQPS = 17.

While this gives a rough estimate of the required acquisition window, a better method would be to setup a circuit with the ADC input model, a model of the source impedance/capacitance, and any board parasitics in SPICE (or similar software) and simulate to verify that the sampling capacitor settles to the desired accuracy.

8.3.2 Achieving Simultaneous Sampling

While the Type 4 ADC does not have dual S+H circuits, it is easy to achieve simultaneous sampling. This is accomplished by setting the SOC triggers on two or more ADC modules to use the same trigger source. The example below demonstrates x4 simultaneous sampling based on an ePWM3 event. ADCINA3, ADCINB5, ADCINC5, and ADCIND2 are sampled. An acquisition window of 20 SYSCLK cycles is used, but different durations are possible. SOC0 is used for all ADCs, but a different SOC is possible, including different SOCs for each ADC.

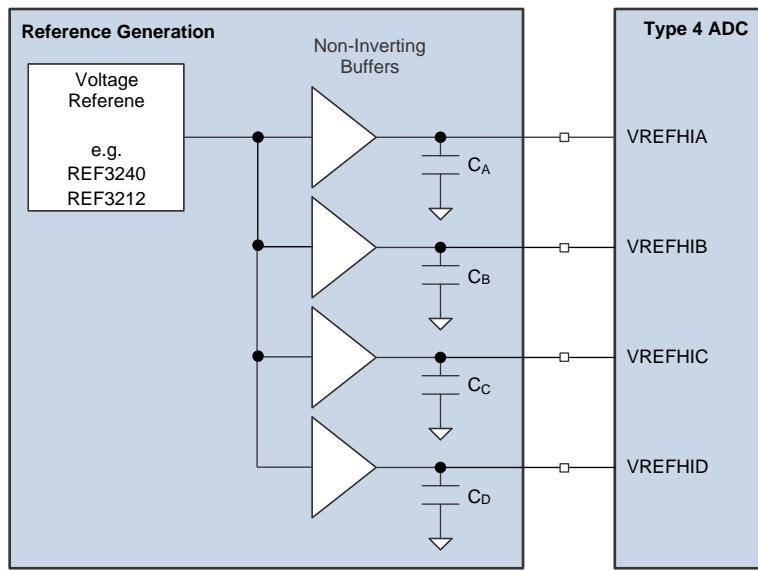
```

AdcaRegs.ADCSOC0CTL.bit.CHSEL = 3;           //SOC0 will convert ADCINA3
AdcaRegs.ADCSOC0CTL.bit.ACQPS = 19;          //SOC0 will convert with 20 SYSCLK cycle acquisition
                                              window
AdcaRegs.ADCSOC0CTL.bit.TRIGSEL = 10;         //SOC0 will begin conversion on ePWM3 SOCB/D
AdcbRegs.ADCSOC0CTL.bit.CHSEL = 5;           //SOC0 will convert ADCINB5
AdcbRegs.ADCSOC0CTL.bit.ACQPS = 19;          //SOC0 will convert with 20 SYSCLK cycle acquisition
                                              window
AdcbRegs.ADCSOC0CTL.bit.TRIGSEL = 10;         //SOC0 will begin conversion on ePWM3 SOCB/D
AdccRegs.ADCSOC0CTL.bit.CHSEL = 5;           //SOC0 will convert ADCINC5
AdccRegs.ADCSOC0CTL.bit.ACQPS = 19;          //SOC0 will convert with 20 SYSCLK cycle acquisition
                                              window
AdccRegs.ADCSOC0CTL.bit.TRIGSEL = 10;         //SOC0 will begin conversion on ePWM3 SOCB/D
AdcdRegs.ADCSOC0CTL.bit.CHSEL = 2;           //SOC0 will convert ADCIND2
AdcdRegs.ADCSOC0CTL.bit.ACQPS = 19;          //SOC0 will convert with 20 SYSCLK cycle acquisition
                                              window
AdcdRegs.ADCSOC0CTL.bit.TRIGSEL = 10;         //SOC0 will begin conversion on ePWM3 SOCB/D
\
```

When the ePWM3 trigger is received, all four ADCs will begin converting in parallel immediately. All results will be in the ADCRESULT0 register for each ADC. Note that this assumes that all ADCs are idle when the trigger is received. If one or more ADCs is busy, the samples will not happen at exactly the same time.

8.3.3 Designing an External Reference Circuit

One external reference circuit can be shared by one or more ADC module. This is desirable to keep ADC reference mismatch minimal, and to save on the number of components necessary in the system. A block diagram for a shared reference system is presented below in [Figure 8-11](#).

Figure 8-11. Shared Reference System

8.3.4 Internal Temperature Sensor

The internal temperature sensor measures the junction temperature of the device. The output of the sensor can be sampled with the ADC through an internal connection. This can be enabled on channel ADCIN13 on ADCA by setting the ENABLE bit in the TSNSCTL register. When sampling the temperature sensor, the external signal on the ADCINA13 pin has no effect on the conversion result.

NOTE: To sample the temperature sensor, the ADC must be in single-ended 12-bit mode.

8.4 Registers

8.4.1 ADC Base Addresses

Table 8-9. ADC Base Address Table

Device Registers	Register Name	Start Address	End Address
AdcaResultRegs	ADC_RESULT_REGS	0x0000_0B00	0x0000_0B1F
AdcbResultRegs	ADC_RESULT_REGS	0x0000_0B20	0x0000_0B3F
AdccResultRegs	ADC_RESULT_REGS	0x0000_0B40	0x0000_0B5F
AdcdResultRegs	ADC_RESULT_REGS	0x0000_0B60	0x0000_0B7F
AdcaRegs	ADC_REGS	0x0000_7400	0x0000_747F
AdcbRegs	ADC_REGS	0x0000_7480	0x0000_74FF
AdccRegs	ADC_REGS	0x0000_7500	0x0000_757F
AdcdRegs	ADC_REGS	0x0000_7580	0x0000_75FF

8.4.2 ADC_REGS Registers

Table 8-10 lists the memory-mapped registers for the ADC_REGS. All register offset addresses not listed in [Table 8-10](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-10. ADC_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	ADCCTL1	ADC Control 1 Register	Section 8.4.2.1	EALLOW
1h	ADCCTL2	ADC Control 2 Register	Section 8.4.2.2	EALLOW
2h	ADCBURSTCTL	ADC Burst Control Register	Section 8.4.2.3	EALLOW
3h	ADCINTFLG	ADC Interrupt Flag Register	Section 8.4.2.4	
4h	ADCINTFLGCLR	ADC Interrupt Flag Clear Register	Section 8.4.2.5	
5h	ADCINTOVF	ADC Interrupt Overflow Register	Section 8.4.2.6	
6h	ADCINTOVFCLR	ADC Interrupt Overflow Clear Register	Section 8.4.2.7	
7h	ADCINTSEL1N2	ADC Interrupt 1 and 2 Selection Register	Section 8.4.2.8	EALLOW
8h	ADCINTSEL3N4	ADC Interrupt 3 and 4 Selection Register	Section 8.4.2.9	EALLOW
9h	ADCSOCPRICL	ADC SOC Priority Control Register	Section 8.4.2.10	EALLOW
Ah	ADCINTSOCSEL1	ADC Interrupt SOC Selection 1 Register	Section 8.4.2.11	EALLOW
Bh	ADCINTSOCSEL2	ADC Interrupt SOC Selection 2 Register	Section 8.4.2.12	EALLOW
Ch	ADCSOCFLG1	ADC SOC Flag 1 Register	Section 8.4.2.13	
Dh	ADCSOCFRC1	ADC SOC Force 1 Register	Section 8.4.2.14	
Eh	ADCSOCOVF1	ADC SOC Overflow 1 Register	Section 8.4.2.15	
Fh	ADCSOCOVFCLR1	ADC SOC Overflow Clear 1 Register	Section 8.4.2.16	
10h	ADCSOC0CTL	ADC SOC0 Control Register	Section 8.4.2.17	EALLOW
12h	ADCSOC1CTL	ADC SOC1 Control Register	Section 8.4.2.18	EALLOW
14h	ADCSOC2CTL	ADC SOC2 Control Register	Section 8.4.2.19	EALLOW
16h	ADCSOC3CTL	ADC SOC3 Control Register	Section 8.4.2.20	EALLOW
18h	ADCSOC4CTL	ADC SOC4 Control Register	Section 8.4.2.21	EALLOW
1Ah	ADCSOC5CTL	ADC SOC5 Control Register	Section 8.4.2.22	EALLOW
1Ch	ADCSOC6CTL	ADC SOC6 Control Register	Section 8.4.2.23	EALLOW
1Eh	ADCSOC7CTL	ADC SOC7 Control Register	Section 8.4.2.24	EALLOW
20h	ADCSOC8CTL	ADC SOC8 Control Register	Section 8.4.2.25	EALLOW
22h	ADCSOC9CTL	ADC SOC9 Control Register	Section 8.4.2.26	EALLOW
24h	ADCSOC10CTL	ADC SOC10 Control Register	Section 8.4.2.27	EALLOW
26h	ADCSOC11CTL	ADC SOC11 Control Register	Section 8.4.2.28	EALLOW
28h	ADCSOC12CTL	ADC SOC12 Control Register	Section 8.4.2.29	EALLOW
2Ah	ADCSOC13CTL	ADC SOC13 Control Register	Section 8.4.2.30	EALLOW
2Ch	ADCSOC14CTL	ADC SOC14 Control Register	Section 8.4.2.31	EALLOW
2Eh	ADCSOC15CTL	ADC SOC15 Control Register	Section 8.4.2.32	EALLOW
30h	ADCEVTSTAT	ADC Event Status Register	Section 8.4.2.33	
32h	ADCEVTCLR	ADC Event Clear Register	Section 8.4.2.34	
34h	ADCEVTSEL	ADC Event Selection Register	Section 8.4.2.35	EALLOW
36h	ADCEVTINTSEL	ADC Event Interrupt Selection Register	Section 8.4.2.36	EALLOW
39h	ADCCOUNTER	ADC Counter Register	Section 8.4.2.37	
3Ah	ADCREV	ADC Revision Register	Section 8.4.2.38	
3Bh	ADCOFFTRIM	ADC Offset Trim Register	Section 8.4.2.39	EALLOW
40h	ADCPPB1CONFIG	ADC PPB1 Config Register	Section 8.4.2.40	EALLOW
41h	ADCPPB1STAMP	ADC PPB1 Sample Delay Time Stamp Register	Section 8.4.2.41	
42h	ADCPPB1OFFCAL	ADC PPB1 Offset Calibration Register	Section 8.4.2.42	EALLOW

Table 8-10. ADC_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
43h	ADCPPB1OFFREF	ADC PPB1 Offset Reference Register	Section 8.4.2.43	
44h	ADCPPB1TRIPHI	ADC PPB1 Trip High Register	Section 8.4.2.44	EALLOW
46h	ADCPPB1TRIPLO	ADC PPB1 Trip Low/Trigger Time Stamp Register	Section 8.4.2.45	EALLOW
48h	ADCPPB2CONFIG	ADC PPB2 Config Register	Section 8.4.2.46	EALLOW
49h	ADCPPB2STAMP	ADC PPB2 Sample Delay Time Stamp Register	Section 8.4.2.47	
4Ah	ADCPPB2OFFCAL	ADC PPB2 Offset Calibration Register	Section 8.4.2.48	EALLOW
4Bh	ADCPPB2OFFREF	ADC PPB2 Offset Reference Register	Section 8.4.2.49	
4Ch	ADCPPB2TRIPHI	ADC PPB2 Trip High Register	Section 8.4.2.50	EALLOW
4Eh	ADCPPB2TRIPLO	ADC PPB2 Trip Low/Trigger Time Stamp Register	Section 8.4.2.51	EALLOW
50h	ADCPPB3CONFIG	ADC PPB3 Config Register	Section 8.4.2.52	EALLOW
51h	ADCPPB3STAMP	ADC PPB3 Sample Delay Time Stamp Register	Section 8.4.2.53	
52h	ADCPPB3OFFCAL	ADC PPB3 Offset Calibration Register	Section 8.4.2.54	EALLOW
53h	ADCPPB3OFFREF	ADC PPB3 Offset Reference Register	Section 8.4.2.55	
54h	ADCPPB3TRIPHI	ADC PPB3 Trip High Register	Section 8.4.2.56	EALLOW
56h	ADCPPB3TRIPLO	ADC PPB3 Trip Low/Trigger Time Stamp Register	Section 8.4.2.57	EALLOW
58h	ADCPPB4CONFIG	ADC PPB4 Config Register	Section 8.4.2.58	EALLOW
59h	ADCPPB4STAMP	ADC PPB4 Sample Delay Time Stamp Register	Section 8.4.2.59	
5Ah	ADCPPB4OFFCAL	ADC PPB4 Offset Calibration Register	Section 8.4.2.60	EALLOW
5Bh	ADCPPB4OFFREF	ADC PPB4 Offset Reference Register	Section 8.4.2.61	
5Ch	ADCPPB4TRIPHI	ADC PPB4 Trip High Register	Section 8.4.2.62	EALLOW
5Eh	ADCPPB4TRIPLO	ADC PPB4 Trip Low/Trigger Time Stamp Register	Section 8.4.2.63	EALLOW
70h	ADCINLTRIM1	ADC Linearity Trim 1 Register	Section 8.4.2.64	EALLOW
72h	ADCINLTRIM2	ADC Linearity Trim 2 Register	Section 8.4.2.65	EALLOW
74h	ADCINLTRIM3	ADC Linearity Trim 3 Register	Section 8.4.2.66	EALLOW
76h	ADCINLTRIM4	ADC Linearity Trim 4 Register	Section 8.4.2.67	EALLOW
78h	ADCINLTRIM5	ADC Linearity Trim 5 Register	Section 8.4.2.68	EALLOW
7Ah	ADCINLTRIM6	ADC Linearity Trim 6 Register	Section 8.4.2.69	EALLOW

8.4.2.1 ADCCTL1 Register (offset = 0h) [reset = 0h]ADCCTL1 is shown in [Figure 8-12](#) and described in [Table 8-11](#).

ADC Control 1 Register

Figure 8-12. ADCCTL1 Register

15	14	13	12	11	10	9	8
RESERVED		ADCBSY	RESERVED	ADCBSYCHN			
R-0h		R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
ADCPWDNZ		RESERVED				INTPULSEPOS	RESERVED
R/W-0h		R-0h				R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-11. ADCCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	ADCBSY	R	0h	ADC Busy. Set when ADC SOC is generated, cleared by hardware four ADC clocks after negative edge of S/H pulse. 0 ADC is not busy 1 ADC is busy and cannot sample another channel
12	RESERVED	R	0h	Reserved
11-8	ADCBSYCHN	R	0h	ADC Busy Channel. Set when ADC SOC for current channel is generated. When ADCBSY=0: holds the value of the last converted channel When ADCBSY=1: reflects channel currently being processed 0h ADCIN0 is currently processing or was last channel converted 1h ADCIN1 is currently processing or was last channel converted 2h ADCIN2 is currently processing or was last channel converted 3h ADCIN3 is currently processing or was last channel converted 4h ADCIN4 is currently processing or was last channel converted 5h ADCIN5 is currently processing or was last channel converted 6h ADCIN6 is currently processing or was last channel converted 7h ADCIN7 is currently processing or was last channel converted 8h ADCIN8 is currently processing or was last channel converted 9h ADCIN9 is currently processing or was last channel converted Ah ADCIN10 is currently processing or was last channel converted Bh ADCIN11 is currently processing or was last channel converted
7	ADCPWDNZ	R/W	0h	ADC Power Down (active low). This bit controls the power up and power down of all the analog circuitry inside the analog core. 0 All analog circuitry inside the core is powered down 1 All analog circuitry inside the core is powered up
6-3	RESERVED	R	0h	Reserved
2	INTPULSEPOS	R/W	0h	ADC Interrupt Pulse Position. 0 Interrupt pulse generation occurs at the end of the acquisition window 1 Interrupt pulse generation occurs at the end of the conversion, 1 cycle prior to the ADC result latching into its result register
1-0	RESERVED	R	0h	Reserved

8.4.2.2 ADCCTL2 Register (offset = 1h) [reset = 0h]ADCCTL2 is shown in [Figure 8-13](#) and described in [Table 8-12](#).

ADC Control 2 Register

Figure 8-13. ADCCTL2 Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED			
R-0h				R-0h			
7	6	5	4	3	2	1	0
SIGNALMODE	RESOLUTION	RESERVED		PRESCALE			
R/W-0h	R/W-0h	R-0h		R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-12. ADCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	RESERVED	R	0h	Reserved
7	SIGNALMODE	R/W	0h	SOC Signaling Mode. Selects the input mode of the converter. 0 Single-ended 1 Differential
6	RESOLUTION	R/W	0h	SOC Conversion Resolution. Selects the resolution of the converter. 0 12-bit resolution 1 16-bit resolution
5-4	RESERVED	R	0h	Reserved
3-0	PRESCALE	R/W	0h	ADC Clock Prescaler. 0000 ADCCLK = Input Clock / 1.0 0001 Invalid 0010 ADCCLK = Input Clock / 2.0 0011 ADCCLK = Input Clock / 2.5 0100 ADCCLK = Input Clock / 3.0 0101 ADCCLK = Input Clock / 3.5 0110 ADCCLK = Input Clock / 4.0 0111 ADCCLK = Input Clock / 4.5 1000 ADCCLK = Input Clock / 5.0 1001 ADCCLK = Input Clock / 5.5 1010 ADCCLK = Input Clock / 6.0 1011 ADCCLK = Input Clock / 6.5 1100 ADCCLK = Input Clock / 7.0 1101 ADCCLK = Input Clock / 7.5 1110 ADCCLK = Input Clock / 8.0 1111 ADCCLK = Input Clock / 8.5

8.4.2.3 ADCBURSTCTL Register (offset = 2h) [reset = 0h]

ADCBURSTCTL is shown in Figure 8-14 and described in Table 8-13.

ADC Burst Control Register

Figure 8-14. ADCBURSTCTL Register

15	14	13	12	11	10	9	8
BURSTEN	RESERVED				BURSTSIZE		
R/W-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	BURSTTRIGSEL				R/W-0h		
	R-0h				R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-13. ADCBURSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BURSTEN	R/W	0h	SOC Burst Mode Enable. This bit enables the SOC Burst Mode of operation. 0 Burst mode is disabled. 1 Burst mode is enabled.
14-12	RESERVED	R	0h	Reserved
11-8	BURSTSIZE	R/W	0h	SOC Burst Size Select. This bit field determines how many SOCs are converted when a burst conversion sequence is started. The first SOC converted is defined by the round robin pointer, which is advanced as each SOC is converted. 0h 1 SOC converted 1h 2 SOCs converted 2h 3 SOCs converted 3h 4 SOCs converted 4h 5 SOCs converted 5h 6 SOCs converted 6h 7 SOCs converted 7h 8 SOCs converted 8h 9 SOCs converted 9h 10 SOCs converted Ah 11 SOCs converted Bh 12 SOCs converted Ch 13 SOCs converted Dh 14 SOCs converted Eh 15 SOCs converted Fh 16 SOCs converted
7-6	RESERVED	R	0h	Reserved

Table 8-13. ADCBURSTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	BURSTTRIGSEL	R/W	0h	SOC Burst Trigger Source Select. Configures which trigger will start a burst conversion sequence. 00h BURSTTRIG0 - Software only 01h BURSTTRIG1 - CPU1 Timer 0, TINT0n 02h BURSTTRIG2 - CPU1 Timer 1, TINT1n 03h BURSTTRIG3 - CPU1 Timer 2, TINT2n 04h BURSTTRIG4 - GPIO, ADCEXTSOC 05h BURSTTRIG5 - ePWM1, ADCSOCA/C 06h BURSTTRIG6 - ePWM1, ADCSOCB/D 07h BURSTTRIG7 - ePWM2, ADCSOCA/C 08h BURSTTRIG8 - ePWM2, ADCSOCB/D 09h BURSTTRIG9 - ePWM3, ADCSOCA/C 0Ah BURSTTRIG10 - ePWM3, ADCSOCB/D 0Bh BURSTTRIG11 - ePWM4, ADCSOCA/C 0Ch BURSTTRIG12 - ePWM4, ADCSOCB/D 0Dh BURSTTRIG13 - ePWM5, ADCSOCA/C 0Eh BURSTTRIG14 - ePWM5, ADCSOCB/D 0Fh BURSTTRIG15 - ePWM6, ADCSOCA/C 10h BURSTTRIG16 - ePWM6, ADCSOCB/D 11h BURSTTRIG17 - ePWM7, ADCSOCA/C 12h BURSTTRIG18 - ePWM7, ADCSOCB/D 13h BURSTTRIG19 - ePWM8, ADCSOCA/C 14h BURSTTRIG20 - ePWM8, ADCSOCB/D 15h BURSTTRIG21 - ePWM9, ADCSOCA/C 16h BURSTTRIG22 - ePWM9, ADCSOCB/D 17h BURSTTRIG23 - ePWM10, ADCSOCA/C 18h BURSTTRIG24 - ePWM10, ADCSOCB/D 19h BURSTTRIG25 - ePWM11, ADCSOCA/C 1Ah BURSTTRIG26 - ePWM11, ADCSOCB/D 1Bh BURSTTRIG27 - ePWM12, ADCSOCA/C 1Ch BURSTTRIG28 - ePWM12, ADCSOCB/D 1Dh BURSTTRIG29 - CPU2 Timer 0, TINT0n 1Eh BURSTTRIG30 - CPU2 Timer 1, TINT1n 1Fh BURSTTRIG31 - CPU2 Timer 2, TINT2n

8.4.2.4 ADCINTFLG Register (offset = 3h) [reset = 0h]ADCINTFLG is shown in [Figure 8-15](#) and described in [Table 8-14](#).

ADC Interrupt Flag Register

Figure 8-15. ADCINTFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-14. ADCINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	ADCINT4	R	0h	ADC Interrupt 4 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continuous mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
2	ADCINT3	R	0h	ADC Interrupt 3 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continuous mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
1	ADCINT2	R	0h	ADC Interrupt 2 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continuous mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

Table 8-14. ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	R	0h	ADC Interrupt 1 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continuous mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

8.4.2.5 ADCINTFLGCLR Register (offset = 4h) [reset = 0h]

ADCINTFLGCLR is shown in [Figure 8-16](#) and described in [Table 8-15](#).

ADC Interrupt Flag Clear Register

Figure 8-16. ADCINTFLGCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R-0h				R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-15. ADCINTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	ADCINT4	R=0/W=1	0h	<p>ADC Interrupt 4 Flag Clear. Reads return 0.</p> <p>0 No action</p> <p>1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority but the overflow bit will not be affected (retains current state)</p> <p>Boundary condition: If hardware is trying to set the bit flag while software tries to clear the bit in the same cycle, the following will take place:</p> <ol style="list-style-type: none"> 1. SW has priority and will clear the flag 2. HW set will be discarded no signal will propagate to the PIE from the latch 3. Overflow flag/condition will be generated
2	ADCINT3	R=0/W=1	0h	<p>ADC Interrupt 3 Flag Clear. Reads return 0.</p> <p>0 No action</p> <p>1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority but the overflow bit will not be affected (retains current state)</p> <p>Boundary condition: If hardware is trying to set the bit flag while software tries to clear the bit in the same cycle, the following will take place:</p> <ol style="list-style-type: none"> 1. SW has priority and will clear the flag 2. HW set will be discarded no signal will propagate to the PIE from the latch 3. Overflow flag/condition will be generated
1	ADCINT2	R=0/W=1	0h	<p>ADC Interrupt 2 Flag Clear. Reads return 0.</p> <p>0 No action</p> <p>1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority but the overflow bit will not be affected (retains current state)</p> <p>Boundary condition: If hardware is trying to set the bit flag while software tries to clear the bit in the same cycle, the following will take place:</p> <ol style="list-style-type: none"> 1. SW has priority and will clear the flag 2. HW set will be discarded no signal will propagate to the PIE from the latch 3. Overflow flag/condition will be generated

Table 8-15. ADCINTFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	R=0/W=1	0h	<p>ADC Interrupt 1 Flag Clear. Reads return 0.</p> <p>0 No action</p> <p>1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority but the overflow bit will not be affected (retains current state)</p> <p>Boundary condition: If hardware is trying to set the bit flag while software tries to clear the bit in the same cycle, the following will take place:</p> <ol style="list-style-type: none"> 1. SW has priority and will clear the flag 2. HW set will be discarded no signal will propagate to the PIE from the latch 3. Overflow flag/condition will be generated

8.4.2.6 ADCINTOVF Register (offset = 5h) [reset = 0h]ADCINTOVF is shown in [Figure 8-17](#) and described in [Table 8-16](#).

ADC Interrupt Overflow Register

Figure 8-17. ADCINTOVF Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R-0h				R-0h	R-0h	R-0h	R-0h

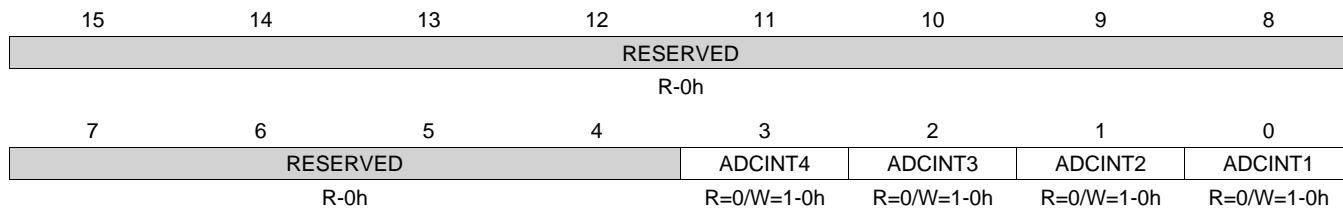
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-16. ADCINTOVF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	ADCINT4	R	0h	<p>ADC Interrupt 4 Overflow Flags</p> <p>Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs.</p> <p>0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected.</p> <p>The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.</p>
2	ADCINT3	R	0h	<p>ADC Interrupt 3 Overflow Flags</p> <p>Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs.</p> <p>0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected.</p> <p>The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.</p>
1	ADCINT2	R	0h	<p>ADC Interrupt 2 Overflow Flags</p> <p>Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs.</p> <p>0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected.</p> <p>The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.</p>
0	ADCINT1	R	0h	<p>ADC Interrupt 1 Overflow Flags</p> <p>Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs.</p> <p>0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected.</p> <p>The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.</p>

8.4.2.7 ADCINTOVFCLR Register (offset = 6h) [reset = 0h]ADCINTOVFCLR is shown in [Figure 8-18](#) and described in [Table 8-17](#).

ADC Interrupt Overflow Clear Register

Figure 8-18. ADCINTOVFCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-17. ADCINTOVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	ADCINT4	R=0/W=1	0h	ADC Interrupt 4 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
2	ADCINT3	R=0/W=1	0h	ADC Interrupt 3 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
1	ADCINT2	R=0/W=1	0h	ADC Interrupt 2 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
0	ADCINT1	R=0/W=1	0h	ADC Interrupt 1 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.

8.4.2.8 ADCINTSEL1N2 Register (offset = 7h) [reset = 0h]

ADCINTSEL1N2 is shown in [Figure 8-19](#) and described in [Table 8-18](#).

ADC Interrupt 1 and 2 Selection Register

Figure 8-19. ADCINTSEL1N2 Register

15	14	13	12	11	10	9	8			
RESERVED	INT2CONT	INT2E	RESERVED	INT2SEL						
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h						
7	6	5	4	3	2	1	0			
RESERVED	INT1CONT	INT1E	RESERVED	INT1SEL						
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-18. ADCINTSEL1N2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	INT2CONT	R/W	0h	ADCINT2 Continuous Mode Enable 0 No further ADCINT2 pulses are generated until ADCINT2 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT2E	R/W	0h	ADCINT2 Interrupt Enable 0 ADCINT2 is disabled 1 ADCINT2 is enabled
12	RESERVED	R	0h	Reserved
11-8	INT2SEL	R/W	0h	ADCINT2 EOC Source Select 0h EOC0 is trigger for ADCINT2 1h EOC1 is trigger for ADCINT2 2h EOC2 is trigger for ADCINT2 3h EOC3 is trigger for ADCINT2 4h EOC4 is trigger for ADCINT2 5h EOC5 is trigger for ADCINT2 6h EOC6 is trigger for ADCINT2 7h EOC7 is trigger for ADCINT2 8h EOC8 is trigger for ADCINT2 9h EOC9 is trigger for ADCINT2 Ah EOC10 is trigger for ADCINT2 Bh EOC11 is trigger for ADCINT2 Ch EOC12 is trigger for ADCINT2 Dh EOC13 is trigger for ADCINT2 Eh EOC14 is trigger for ADCINT2 Fh EOC15 is trigger for ADCINT2
7	RESERVED	R	0h	Reserved
6	INT1CONT	R/W	0h	ADCINT1 Continuous Mode Enable 0 No further ADCINT1 pulses are generated until ADCINT1 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.

Table 8-18. ADCINTSEL1N2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT1E	R/W	0h	ADCINT1 Interrupt Enable 0 ADCINT1 is disabled 1 ADCINT1 is enabled
4	RESERVED	R	0h	Reserved
3-0	INT1SEL	R/W	0h	ADCINT1 EOC Source Select 0h EOC0 is trigger for ADCINT1 1h EOC1 is trigger for ADCINT1 2h EOC2 is trigger for ADCINT1 3h EOC3 is trigger for ADCINT1 4h EOC4 is trigger for ADCINT1 5h EOC5 is trigger for ADCINT1 6h EOC6 is trigger for ADCINT1 7h EOC7 is trigger for ADCINT1 8h EOC8 is trigger for ADCINT1 9h EOC9 is trigger for ADCINT1 Ah EOC10 is trigger for ADCINT1 Bh EOC11 is trigger for ADCINT1 Ch EOC12 is trigger for ADCINT1 Dh EOC13 is trigger for ADCINT1 Eh EOC14 is trigger for ADCINT1 Fh EOC15 is trigger for ADCINT1

8.4.2.9 ADCINTSEL3N4 Register (offset = 8h) [reset = 0h]

ADCINTSEL3N4 is shown in Figure 8-20 and described in Table 8-19.

ADC Interrupt 3 and 4 Selection Register

Figure 8-20. ADCINTSEL3N4 Register

15	14	13	12	11	10	9	8			
RESERVED	INT4CONT	INT4E	RESERVED	INT4SEL						
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h						
7	6	5	4	3	2	1	0			
RESERVED	INT3CONT	INT3E	RESERVED	INT3SEL						
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-19. ADCINTSEL3N4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	INT4CONT	R/W	0h	ADCINT4 Continuous Mode Enable 0 No further ADCINT4 pulses are generated until ADCINT4 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT4E	R/W	0h	ADCINT4 Interrupt Enable 0 ADCINT4 is disabled 1 ADCINT4 is enabled
12	RESERVED	R	0h	Reserved
11-8	INT4SEL	R/W	0h	ADCINT4 EOC Source Select 0h EOC0 is trigger for ADCINT4 1h EOC1 is trigger for ADCINT4 2h EOC2 is trigger for ADCINT4 3h EOC3 is trigger for ADCINT4 4h EOC4 is trigger for ADCINT4 5h EOC5 is trigger for ADCINT4 6h EOC6 is trigger for ADCINT4 7h EOC7 is trigger for ADCINT4 8h EOC8 is trigger for ADCINT4 9h EOC9 is trigger for ADCINT4 Ah EOC10 is trigger for ADCINT4 Bh EOC11 is trigger for ADCINT4 Ch EOC12 is trigger for ADCINT4 Dh EOC13 is trigger for ADCINT4 Eh EOC14 is trigger for ADCINT4 Fh EOC15 is trigger for ADCINT4
7	RESERVED	R	0h	Reserved
6	INT3CONT	R/W	0h	ADCINT3 Continuous Mode Enable 0 No further ADCINT3 pulses are generated until ADCINT3 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.

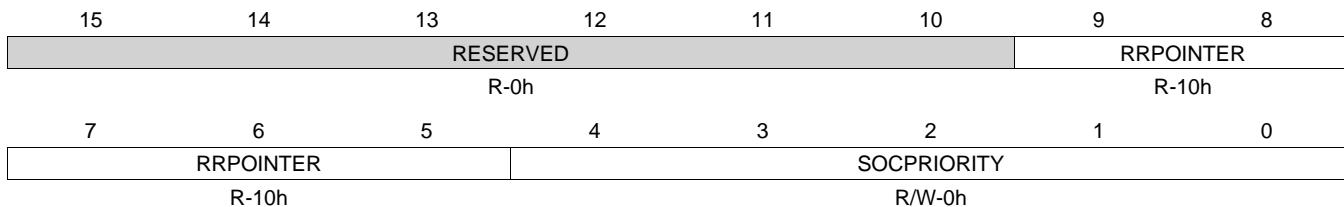
Table 8-19. ADCINTSEL3N4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT3E	R/W	0h	ADCINT3 Interrupt Enable 0 ADCINT3 is disabled 1 ADCINT3 is enabled
4	RESERVED	R	0h	Reserved
3-0	INT3SEL	R/W	0h	ADCINT3 EOC Source Select 0h EOC0 is trigger for ADCINT3 1h EOC1 is trigger for ADCINT3 2h EOC2 is trigger for ADCINT3 3h EOC3 is trigger for ADCINT3 4h EOC4 is trigger for ADCINT3 5h EOC5 is trigger for ADCINT3 6h EOC6 is trigger for ADCINT3 7h EOC7 is trigger for ADCINT3 8h EOC8 is trigger for ADCINT3 9h EOC9 is trigger for ADCINT3 Ah EOC10 is trigger for ADCINT3 Bh EOC11 is trigger for ADCINT3 Ch EOC12 is trigger for ADCINT3 Dh EOC13 is trigger for ADCINT3 Eh EOC14 is trigger for ADCINT3 Fh EOC15 is trigger for ADCINT3

8.4.2.10 ADCSOCPRICL Register (offset = 9h) [reset = 200h]

ADCSOCPRICL is shown in [Figure 8-21](#) and described in [Table 8-20](#).

ADC SOC Priority Control Register

Figure 8-21. ADCSOCPRICL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-20. ADCSOCPRICL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved

Table 8-20. ADCSOCPRICL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-5	RRPOINTER	R	10h	<p>Round Robin Pointer. Holds the value of the last converted round robin SOCx to be used by the round robin scheme to determine order of conversions.</p> <p>00h SOC0 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>01h SOC1 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>02h SOC2 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>03h SOC3 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>04h SOC4 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>05h SOC5 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>06h SOC6 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>07h SOC7 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>08h SOC8 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>09h SOC9 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>0Ah SOC10 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>0Bh SOC11 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>0Ch SOC12 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>0Dh SOC13 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>0Eh SOC14 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>0Fh SOC15 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>10h Reset value to indicate no SOC has been converted. SOC0 is highest round robin priority. Set to this value when the device is reset, when the ADCCTL1.RESET bit is set, or when the SOCPRICL register is written. In the latter case, if a conversion is currently in progress, it will complete and then the new priority will take effect.</p> <p>Others Invalid value.</p>

Table 8-20. ADCSOCPRICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	SOC_PRIORITY	R/W	0h	<p>SOC Priority</p> <p>Determines the cutoff point for priority mode and round robin arbitration for SOCx</p> <p>00h SOC priority is handled in round robin mode for all channels.</p> <p>01h SOC0 is high priority, rest of channels are in round robin mode.</p> <p>02h SOC0-SOC1 are high priority, SOC2-SOC15 are in round robin mode.</p> <p>03h SOC0-SOC2 are high priority, SOC3-SOC15 are in round robin mode.</p> <p>04h SOC0-SOC3 are high priority, SOC4-SOC15 are in round robin mode.</p> <p>05h SOC0-SOC4 are high priority, SOC5-SOC15 are in round robin mode.</p> <p>06h SOC0-SOC5 are high priority, SOC6-SOC15 are in round robin mode.</p> <p>07h SOC0-SOC6 are high priority, SOC7-SOC15 are in round robin mode.</p> <p>08h SOC0-SOC7 are high priority, SOC8-SOC15 are in round robin mode.</p> <p>09h SOC0-SOC8 are high priority, SOC9-SOC15 are in round robin mode.</p> <p>0Ah SOC0-SOC9 are high priority, SOC10-SOC15 are in round robin mode.</p> <p>0Bh SOC0-SOC10 are high priority, SOC11-SOC15 are in round robin mode.</p> <p>0Ch SOC0-SOC11 are high priority, SOC12-SOC15 are in round robin mode.</p> <p>0Dh SOC0-SOC12 are high priority, SOC13-SOC15 are in round robin mode.</p> <p>0Eh SOC0-SOC13 are high priority, SOC14-SOC15 are in round robin mode.</p> <p>0Fh SOC0-SOC14 are high priority, SOC15 is in round robin mode.</p> <p>10h All SOCs are in high priority mode, arbitrated by SOC number.</p> <p>Others Invalid selection.</p>

8.4.2.11 ADCINTSOCSEL1 Register (offset = Ah) [reset = 0h]ADCINTSOCSEL1 is shown in [Figure 8-22](#) and described in [Table 8-21](#).

ADC Interrupt SOC Selection 1 Register

Figure 8-22. ADCINTSOCSEL1 Register

15	14	13	12	11	10	9	8
SOC7		SOC6		SOC5		SOC4	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
SOC3		SOC2		SOC1		SOC0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-21. ADCINTSOCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SOC7	R/W	0h	SOC7 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC7. This field is OR'ed with the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC7. TRIGSEL field determines SOC7 trigger. 01 ADCINT1 will trigger SOC7. TRIGSEL field is ignored. 10 ADCINT2 will trigger SOC7. TRIGSEL field is ignored. 11 Invalid selection.
13-12	SOC6	R/W	0h	SOC6 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC6. This field is OR'ed with the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC6. TRIGSEL field determines SOC6 trigger. 01 ADCINT1 will trigger SOC6. TRIGSEL field is ignored. 10 ADCINT2 will trigger SOC6. TRIGSEL field is ignored. 11 Invalid selection.
11-10	SOC5	R/W	0h	SOC5 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC5. This field is OR'ed with the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC5. TRIGSEL field determines SOC5 trigger. 01 ADCINT1 will trigger SOC5. TRIGSEL field is ignored. 10 ADCINT2 will trigger SOC5. TRIGSEL field is ignored. 11 Invalid selection.
9-8	SOC4	R/W	0h	SOC4 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC4. This field is OR'ed with the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC4. TRIGSEL field determines SOC4 trigger. 01 ADCINT1 will trigger SOC4. TRIGSEL field is ignored. 10 ADCINT2 will trigger SOC4. TRIGSEL field is ignored. 11 Invalid selection.

Table 8-21. ADCINTSOCSEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	SOC3	R/W	0h	<p>SOC3 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC3. This field is OR'ed with the TRIGSEL field in the ADCSOCxCTL register.</p> <p>00 No ADCINT will trigger SOC3. TRIGSEL field determines SOC3 trigger.</p> <p>01 ADCINT1 will trigger SOC3. TRIGSEL field is ignored.</p> <p>10 ADCINT2 will trigger SOC3. TRIGSEL field is ignored.</p> <p>11 Invalid selection.</p>
5-4	SOC2	R/W	0h	<p>SOC2 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC2. This field is OR'ed with the TRIGSEL field in the ADCSOCxCTL register.</p> <p>00 No ADCINT will trigger SOC2. TRIGSEL field determines SOC2 trigger.</p> <p>01 ADCINT1 will trigger SOC2. TRIGSEL field is ignored.</p> <p>10 ADCINT2 will trigger SOC2. TRIGSEL field is ignored.</p> <p>11 Invalid selection.</p>
3-2	SOC1	R/W	0h	<p>SOC1 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC1. This field is OR'ed with the TRIGSEL field in the ADCSOCxCTL register.</p> <p>00 No ADCINT will trigger SOC1. TRIGSEL field determines SOC1 trigger.</p> <p>01 ADCINT1 will trigger SOC1. TRIGSEL field is ignored.</p> <p>10 ADCINT2 will trigger SOC1. TRIGSEL field is ignored.</p> <p>11 Invalid selection.</p>
1-0	SOC0	R/W	0h	<p>SOC0 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC0. This field is OR'ed with the TRIGSEL field in the ADCSOCxCTL register.</p> <p>00 No ADCINT will trigger SOC0. TRIGSEL field determines SOC0 trigger.</p> <p>01 ADCINT1 will trigger SOC0. TRIGSEL field is ignored.</p> <p>10 ADCINT2 will trigger SOC0. TRIGSEL field is ignored.</p> <p>11 Invalid selection.</p>

8.4.2.12 ADCINTSOCSEL2 Register (offset = Bh) [reset = 0h]ADCINTSOCSEL2 is shown in [Figure 8-23](#) and described in [Table 8-22](#).

ADC Interrupt SOC Selection 2 Register

Figure 8-23. ADCINTSOCSEL2 Register

15	14	13	12	11	10	9	8
SOC15		SOC14		SOC13		SOC12	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
SOC11		SOC10		SOC9		SOC8	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-22. ADCINTSOCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SOC15	R/W	0h	SOC15 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC15. This field overrides the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC15. TRIGSEL field determines SOC15 trigger. 01 ADCINT1 will trigger SOC15. TRIGSEL field is ignored. 10 ADCINT2 will trigger SOC15. TRIGSEL field is ignored. 11 Invalid selection.
13-12	SOC14	R/W	0h	SOC14 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC14. This field overrides the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC14. TRIGSEL field determines SOC14 trigger. 01 ADCINT1 will trigger SOC14. TRIGSEL field is ignored. 10 ADCINT2 will trigger SOC14. TRIGSEL field is ignored. 11 Invalid selection.
11-10	SOC13	R/W	0h	SOC13 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC13. This field overrides the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC13. TRIGSEL field determines SOC13 trigger. 01 ADCINT1 will trigger SOC13. TRIGSEL field is ignored. 10 ADCINT2 will trigger SOC13. TRIGSEL field is ignored. 11 Invalid selection.
9-8	SOC12	R/W	0h	SOC12 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC12. This field overrides the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC12. TRIGSEL field determines SOC12 trigger. 01 ADCINT1 will trigger SOC12. TRIGSEL field is ignored. 10 ADCINT2 will trigger SOC12. TRIGSEL field is ignored. 11 Invalid selection.

Table 8-22. ADCINTSOCSEL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	SOC11	R/W	0h	<p>SOC11 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC11. This field overrides the TRIGSEL field in the ADCSOCxCTL register.</p> <p>00 No ADCINT will trigger SOC11. TRIGSEL field determines SOC11 trigger.</p> <p>01 ADCINT1 will trigger SOC11. TRIGSEL field is ignored.</p> <p>10 ADCINT2 will trigger SOC11. TRIGSEL field is ignored.</p> <p>11 Invalid selection.</p>
5-4	SOC10	R/W	0h	<p>SOC10 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC10. This field overrides the TRIGSEL field in the ADCSOCxCTL register.</p> <p>00 No ADCINT will trigger SOC10. TRIGSEL field determines SOC10 trigger.</p> <p>01 ADCINT1 will trigger SOC10. TRIGSEL field is ignored.</p> <p>10 ADCINT2 will trigger SOC10. TRIGSEL field is ignored.</p> <p>11 Invalid selection.</p>
3-2	SOC9	R/W	0h	<p>SOC9 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC9. This field overrides the TRIGSEL field in the ADCSOCxCTL register.</p> <p>00 No ADCINT will trigger SOC9. TRIGSEL field determines SOC9 trigger.</p> <p>01 ADCINT1 will trigger SOC9. TRIGSEL field is ignored.</p> <p>10 ADCINT2 will trigger SOC9. TRIGSEL field is ignored.</p> <p>11 Invalid selection.</p>
1-0	SOC8	R/W	0h	<p>SOC8 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC8. This field overrides the TRIGSEL field in the ADCSOCxCTL register.</p> <p>00 No ADCINT will trigger SOC8. TRIGSEL field determines SOC8 trigger.</p> <p>01 ADCINT1 will trigger SOC8. TRIGSEL field is ignored.</p> <p>10 ADCINT2 will trigger SOC8. TRIGSEL field is ignored.</p> <p>11 Invalid selection.</p>

8.4.2.13 ADCSOCFLG1 Register (offset = Ch) [reset = 0h]

ADCSOCFLG1 is shown in [Figure 8-24](#) and described in [Table 8-23](#).

ADC SOC Flag 1 Register

Figure 8-24. ADCSOCFLG1 Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-23. ADCSOCFLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Flag. Indicates the state of SOC15 conversions. 0 No sample pending for SOC15. 1 Trigger has been received and sample is pending for SOC15. This bit will be automatically cleared when the SOC15 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
14	SOC14	R	0h	SOC14 Start of Conversion Flag. Indicates the state of SOC14 conversions. 0 No sample pending for SOC14. 1 Trigger has been received and sample is pending for SOC14. This bit will be automatically cleared when the SOC14 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
13	SOC13	R	0h	SOC13 Start of Conversion Flag. Indicates the state of SOC13 conversions. 0 No sample pending for SOC13. 1 Trigger has been received and sample is pending for SOC13. This bit will be automatically cleared when the SOC13 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
12	SOC12	R	0h	SOC12 Start of Conversion Flag. Indicates the state of SOC12 conversions. 0 No sample pending for SOC12. 1 Trigger has been received and sample is pending for SOC12. This bit will be automatically cleared when the SOC12 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

Table 8-23. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R	0h	SOC11 Start of Conversion Flag. Indicates the state of SOC11 conversions. 0 No sample pending for SOC11. 1 Trigger has been received and sample is pending for SOC11. This bit will be automatically cleared when the SOC11 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
10	SOC10	R	0h	SOC10 Start of Conversion Flag. Indicates the state of SOC10 conversions. 0 No sample pending for SOC10. 1 Trigger has been received and sample is pending for SOC10. This bit will be automatically cleared when the SOC10 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
9	SOC9	R	0h	SOC9 Start of Conversion Flag. Indicates the state of SOC9 conversions. 0 No sample pending for SOC9. 1 Trigger has been received and sample is pending for SOC9. This bit will be automatically cleared when the SOC9 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
8	SOC8	R	0h	SOC8 Start of Conversion Flag. Indicates the state of SOC8 conversions. 0 No sample pending for SOC8. 1 Trigger has been received and sample is pending for SOC8. This bit will be automatically cleared when the SOC8 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
7	SOC7	R	0h	SOC7 Start of Conversion Flag. Indicates the state of SOC7 conversions. 0 No sample pending for SOC7. 1 Trigger has been received and sample is pending for SOC7. This bit will be automatically cleared when the SOC7 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

Table 8-23. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SOC6	R	0h	SOC6 Start of Conversion Flag. Indicates the state of SOC6 conversions. 0 No sample pending for SOC6. 1 Trigger has been received and sample is pending for SOC6. This bit will be automatically cleared when the SOC6 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
5	SOC5	R	0h	SOC5 Start of Conversion Flag. Indicates the state of SOC5 conversions. 0 No sample pending for SOC5. 1 Trigger has been received and sample is pending for SOC5. This bit will be automatically cleared when the SOC5 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
4	SOC4	R	0h	SOC4 Start of Conversion Flag. Indicates the state of SOC4 conversions. 0 No sample pending for SOC4. 1 Trigger has been received and sample is pending for SOC4. This bit will be automatically cleared when the SOC4 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
3	SOC3	R	0h	SOC3 Start of Conversion Flag. Indicates the state of SOC3 conversions. 0 No sample pending for SOC3. 1 Trigger has been received and sample is pending for SOC3. This bit will be automatically cleared when the SOC3 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
2	SOC2	R	0h	SOC2 Start of Conversion Flag. Indicates the state of SOC2 conversions. 0 No sample pending for SOC2. 1 Trigger has been received and sample is pending for SOC2. This bit will be automatically cleared when the SOC2 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

Table 8-23. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SOC1	R	0h	SOC1 Start of Conversion Flag. Indicates the state of SOC1 conversions. 0 No sample pending for SOC1. 1 Trigger has been received and sample is pending for SOC1. This bit will be automatically cleared when the SOC1 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
0	SOC0	R	0h	SOC0 Start of Conversion Flag. Indicates the state of SOC0 conversions. 0 No sample pending for SOC0. 1 Trigger has been received and sample is pending for SOC0. This bit will be automatically cleared when the SOC0 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

8.4.2.14 ADCSOCFRC1 Register (offset = Dh) [reset = 0h]

ADCSOCFRC1 is shown in [Figure 8-25](#) and described in [Table 8-24](#).

ADC SOC Force 1 Register

Figure 8-25. ADCSOCFRC1 Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R=0/W=1-0h							
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-24. ADCSOCFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R=0/W=1	0h	<p>SOC15 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC15 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC15 flag bit to 1. This will cause a conversion to start once priority is given to SOC15.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC15 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
14	SOC14	R=0/W=1	0h	<p>SOC14 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC14 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC14 flag bit to 1. This will cause a conversion to start once priority is given to SOC14.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC14 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
13	SOC13	R=0/W=1	0h	<p>SOC13 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC13 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC13 flag bit to 1. This will cause a conversion to start once priority is given to SOC13.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC13 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>

Table 8-24. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SOC12	R=0/W=1	0h	<p>SOC12 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC12 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC12 flag bit to 1. This will cause a conversion to start once priority is given to SOC12.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC12 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
11	SOC11	R=0/W=1	0h	<p>SOC11 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC11 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC11 flag bit to 1. This will cause a conversion to start once priority is given to SOC11.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC11 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
10	SOC10	R=0/W=1	0h	<p>SOC10 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC10 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC10 flag bit to 1. This will cause a conversion to start once priority is given to SOC10.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC10 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
9	SOC9	R=0/W=1	0h	<p>SOC9 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC9 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC9 flag bit to 1. This will cause a conversion to start once priority is given to SOC9.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC9 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>

Table 8-24. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SOC8	R=0/W=1	0h	<p>SOC8 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC8 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC8 flag bit to 1. This will cause a conversion to start once priority is given to SOC8.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC8 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
7	SOC7	R=0/W=1	0h	<p>SOC7 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC7 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC7 flag bit to 1. This will cause a conversion to start once priority is given to SOC7.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC7 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
6	SOC6	R=0/W=1	0h	<p>SOC6 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC6 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC6 flag bit to 1. This will cause a conversion to start once priority is given to SOC6.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC6 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
5	SOC5	R=0/W=1	0h	<p>SOC5 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC5 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC5 flag bit to 1. This will cause a conversion to start once priority is given to SOC5.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC5 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>

Table 8-24. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SOC4	R=0/W=1	0h	<p>SOC4 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC4 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC4 flag bit to 1. This will cause a conversion to start once priority is given to SOC4.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC4 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
3	SOC3	R=0/W=1	0h	<p>SOC3 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC3 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC3 flag bit to 1. This will cause a conversion to start once priority is given to SOC3.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC3 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
2	SOC2	R=0/W=1	0h	<p>SOC2 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC2 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC2 flag bit to 1. This will cause a conversion to start once priority is given to SOC2.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC2 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>
1	SOC1	R=0/W=1	0h	<p>SOC1 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC1 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC1 flag bit to 1. This will cause a conversion to start once priority is given to SOC1.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC1 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>

Table 8-24. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SOC0	R=0/W=1	0h	<p>SOC0 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC0 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC0 flag bit to 1. This will cause a conversion to start once priority is given to SOC0.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC0 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p>

8.4.2.15 ADCSOCOVF1 Register (offset = Eh) [reset = 0h]ADCSOCOVF1 is shown in [Figure 8-26](#) and described in [Table 8-25](#).

ADC SOC Overflow 1 Register

Figure 8-26. ADCSOCOVF1 Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-25. ADCSOCOVF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Overflow Flag. Indicates an SOC15 event was generated in hardware while an existing SOC15 event was already pending. 0 No SOC15 event overflow. 1 SOC15 event overflow. An overflow condition does not stop SOC15 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
14	SOC14	R	0h	SOC14 Start of Conversion Overflow Flag. Indicates an SOC14 event was generated in hardware while an existing SOC14 event was already pending. 0 No SOC14 event overflow. 1 SOC14 event overflow. An overflow condition does not stop SOC14 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
13	SOC13	R	0h	SOC13 Start of Conversion Overflow Flag. Indicates an SOC13 event was generated in hardware while an existing SOC13 event was already pending. 0 No SOC13 event overflow. 1 SOC13 event overflow. An overflow condition does not stop SOC13 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
12	SOC12	R	0h	SOC12 Start of Conversion Overflow Flag. Indicates an SOC12 event was generated in hardware while an existing SOC12 event was already pending. 0 No SOC12 event overflow. 1 SOC12 event overflow. An overflow condition does not stop SOC12 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

Table 8-25. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R	0h	SOC11 Start of Conversion Overflow Flag. Indicates an SOC11 event was generated in hardware while an existing SOC11 event was already pending. 0 No SOC11 event overflow. 1 SOC11 event overflow. An overflow condition does not stop SOC11 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
10	SOC10	R	0h	SOC10 Start of Conversion Overflow Flag. Indicates an SOC10 event was generated in hardware while an existing SOC10 event was already pending. 0 No SOC10 event overflow. 1 SOC10 event overflow. An overflow condition does not stop SOC10 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
9	SOC9	R	0h	SOC9 Start of Conversion Overflow Flag. Indicates an SOC9 event was generated in hardware while an existing SOC9 event was already pending. 0 No SOC9 event overflow. 1 SOC9 event overflow. An overflow condition does not stop SOC9 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
8	SOC8	R	0h	SOC8 Start of Conversion Overflow Flag. Indicates an SOC8 event was generated in hardware while an existing SOC8 event was already pending. 0 No SOC8 event overflow. 1 SOC8 event overflow. An overflow condition does not stop SOC8 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
7	SOC7	R	0h	SOC7 Start of Conversion Overflow Flag. Indicates an SOC7 event was generated in hardware while an existing SOC7 event was already pending. 0 No SOC7 event overflow. 1 SOC7 event overflow. An overflow condition does not stop SOC7 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
6	SOC6	R	0h	SOC6 Start of Conversion Overflow Flag. Indicates an SOC6 event was generated in hardware while an existing SOC6 event was already pending. 0 No SOC6 event overflow. 1 SOC6 event overflow. An overflow condition does not stop SOC6 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

Table 8-25. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SOC5	R	0h	SOC5 Start of Conversion Overflow Flag. Indicates an SOC5 event was generated in hardware while an existing SOC5 event was already pending. 0 No SOC5 event overflow. 1 SOC5 event overflow. An overflow condition does not stop SOC5 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
4	SOC4	R	0h	SOC4 Start of Conversion Overflow Flag. Indicates an SOC4 event was generated in hardware while an existing SOC4 event was already pending. 0 No SOC4 event overflow. 1 SOC4 event overflow. An overflow condition does not stop SOC4 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
3	SOC3	R	0h	SOC3 Start of Conversion Overflow Flag. Indicates an SOC3 event was generated in hardware while an existing SOC3 event was already pending. 0 No SOC3 event overflow. 1 SOC3 event overflow. An overflow condition does not stop SOC3 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
2	SOC2	R	0h	SOC2 Start of Conversion Overflow Flag. Indicates an SOC2 event was generated in hardware while an existing SOC2 event was already pending. 0 No SOC2 event overflow. 1 SOC2 event overflow. An overflow condition does not stop SOC2 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
1	SOC1	R	0h	SOC1 Start of Conversion Overflow Flag. Indicates an SOC1 event was generated in hardware while an existing SOC1 event was already pending. 0 No SOC1 event overflow. 1 SOC1 event overflow. An overflow condition does not stop SOC1 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
0	SOC0	R	0h	SOC0 Start of Conversion Overflow Flag. Indicates an SOC0 event was generated in hardware while an existing SOC0 event was already pending. 0 No SOC0 event overflow. 1 SOC0 event overflow. An overflow condition does not stop SOC0 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

8.4.2.16 ADCSOCOVFCLR1 Register (offset = Fh) [reset = 0h]

ADCSOCOVFCLR1 is shown in [Figure 8-27](#) and described in [Table 8-26](#).

ADC SOC Overflow Clear 1 Register

Figure 8-27. ADCSOCOVFCLR1 Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R=0/W=1-0h							
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-26. ADCSOCOVFCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R=0/W=1	0h	SOC15 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC15 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC15 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
14	SOC14	R=0/W=1	0h	SOC14 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC14 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC14 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
13	SOC13	R=0/W=1	0h	SOC13 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC13 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC13 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
12	SOC12	R=0/W=1	0h	SOC12 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC12 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC12 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
11	SOC11	R=0/W=1	0h	SOC11 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC11 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC11 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

Table 8-26. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SOC10	R=0/W=1	0h	<p>SOC10 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC10 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC10 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
9	SOC9	R=0/W=1	0h	<p>SOC9 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC9 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC9 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
8	SOC8	R=0/W=1	0h	<p>SOC8 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC8 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC8 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
7	SOC7	R=0/W=1	0h	<p>SOC7 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC7 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC7 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
6	SOC6	R=0/W=1	0h	<p>SOC6 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC6 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC6 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
5	SOC5	R=0/W=1	0h	<p>SOC5 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC5 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC5 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
4	SOC4	R=0/W=1	0h	<p>SOC4 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC4 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC4 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>

Table 8-26. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R=0/W=1	0h	<p>SOC3 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC3 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC3 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
2	SOC2	R=0/W=1	0h	<p>SOC2 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC2 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC2 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
1	SOC1	R=0/W=1	0h	<p>SOC1 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC1 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC1 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>
0	SOC0	R=0/W=1	0h	<p>SOC0 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC0 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.</p> <p>0 No action.</p> <p>1 Clear SOC0 overflow flag.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..</p>

8.4.2.17 ADCSOC0CTL Register (offset = 10h) [reset = 0h]

ADCSOC0CTL is shown in [Figure 8-28](#) and described in [Table 8-27](#).

ADC SOC0 Control Register

Figure 8-28. ADCSOC0CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED		CHSEL	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL		RESERVED					ACQPS
R/W-0h		R-0h					R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-27. ADCSOC0CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-27. ADCSOC0CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-27. ADCSOC0CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.18 ADCSOC1CTL Register (offset = 12h) [reset = 0h]ADCSOC1CTL is shown in [Figure 8-29](#) and described in [Table 8-28](#).

ADC SOC1 Control Register

Figure 8-29. ADCSOC1CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	CHSEL		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-28. ADCSOC1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-28. ADCSOC1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-28. ADCSOC1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.19 ADCSOC2CTL Register (offset = 14h) [reset = 0h]

ADCSOC2CTL is shown in [Figure 8-30](#) and described in [Table 8-29](#).

ADC SOC2 Control Register

Figure 8-30. ADCSOC2CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED		CHSEL	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL		RESERVED					ACQPS
R/W-0h		R-0h					R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-29. ADCSOC2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-29. ADCSOC2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-29. ADCSOC2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.20 ADCSOC3CTL Register (offset = 16h) [reset = 0h]ADCSOC3CTL is shown in [Figure 8-31](#) and described in [Table 8-30](#).

ADC SOC3 Control Register

Figure 8-31. ADCSOC3CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	CHSEL		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-30. ADCSOC3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-30. ADCSOC3CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-30. ADCSOC3CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.21 ADCSOC4CTL Register (offset = 18h) [reset = 0h]

ADCSOC4CTL is shown in [Figure 8-32](#) and described in [Table 8-31](#).

ADC SOC4 Control Register

Figure 8-32. ADCSOC4CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED		CHSEL	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-31. ADCSOC4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-31. ADCSOC4CTL Register Field Descriptions (continued)

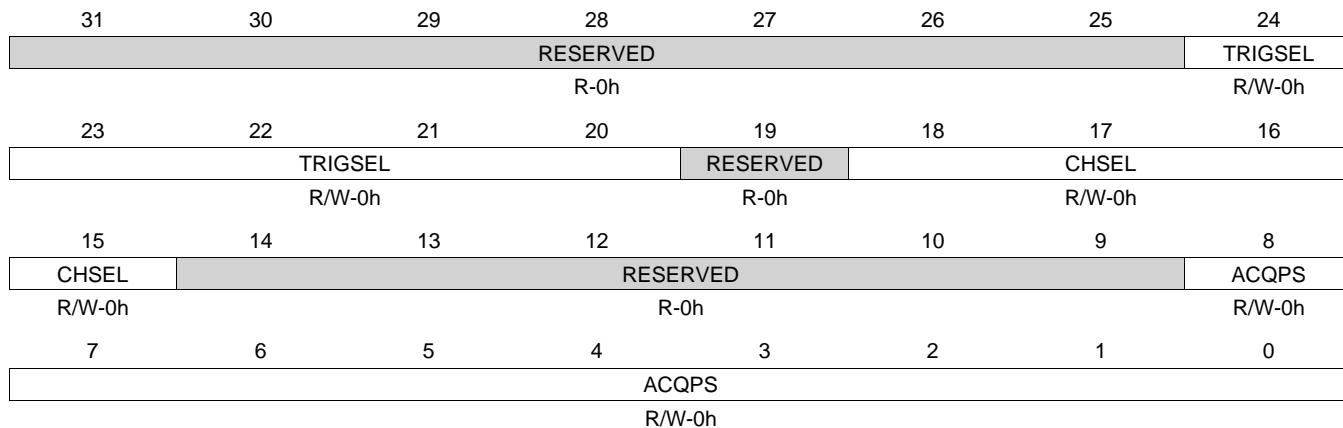
Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-31. ADCSOC4CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.22 ADCSOC5CTL Register (offset = 1Ah) [reset = 0h]ADCSOC5CTL is shown in [Figure 8-33](#) and described in [Table 8-32](#).

ADC SOC5 Control Register

Figure 8-33. ADCSOC5CTL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-32. ADCSOC5CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-32. ADCSOC5CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-32. ADCSOC5CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.23 ADCSOC6CTL Register (offset = 1Ch) [reset = 0h]

ADCSOC6CTL is shown in [Figure 8-34](#) and described in [Table 8-33](#).

ADC SOC6 Control Register

Figure 8-34. ADCSOC6CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED		CHSEL	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL		RESERVED					ACQPS
R/W-0h		R-0h					R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-33. ADCSOC6CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-33. ADCSOC6CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-33. ADCSOC6CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.24 ADCSOC7CTL Register (offset = 1Eh) [reset = 0h]ADCSOC7CTL is shown in [Figure 8-35](#) and described in [Table 8-34](#).

ADC SOC7 Control Register

Figure 8-35. ADCSOC7CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	CHSEL		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-34. ADCSOC7CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-34. ADCSOC7CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-34. ADCSOC7CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC. Single-ended Signaling Mode (SIGNALMODE = 0): 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 Differential Signaling Mode (SIGNALMODE = 1): 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

8.4.2.25 ADCSOC8CTL Register (offset = 20h) [reset = 0h]

ADCSOC8CTL is shown in [Figure 8-36](#) and described in [Table 8-35](#).

ADC SOC8 Control Register

Figure 8-36. ADCSOC8CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED		CHSEL	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-35. ADCSOC8CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-35. ADCSOC8CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-35. ADCSOC8CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.26 ADCSOC9CTL Register (offset = 22h) [reset = 0h]ADCSOC9CTL is shown in [Figure 8-37](#) and described in [Table 8-36](#).

ADC SOC9 Control Register

Figure 8-37. ADCSOC9CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	CHSEL		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-36. ADCSOC9CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-36. ADCSOC9CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-36. ADCSOC9CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.27 ADCSOC10CTL Register (offset = 24h) [reset = 0h]

ADCSOC10CTL is shown in [Figure 8-38](#) and described in [Table 8-37](#).

ADC SOC10 Control Register

Figure 8-38. ADCSOC10CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED		CHSEL	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL		RESERVED					ACQPS
R/W-0h		R-0h					R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-37. ADCSOC10CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-37. ADCSOC10CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-37. ADCSOC10CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.28 ADCSOC11CTL Register (offset = 26h) [reset = 0h]ADCSOC11CTL is shown in [Figure 8-39](#) and described in [Table 8-38](#).

ADC SOC11 Control Register

Figure 8-39. ADCSOC11CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	CHSEL		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-38. ADCSOC11CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-38. ADCSOC11CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-38. ADCSOC11CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.29 ADCSOC12CTL Register (offset = 28h) [reset = 0h]

ADCSOC12CTL is shown in [Figure 8-40](#) and described in [Table 8-39](#).

ADC SOC12 Control Register

Figure 8-40. ADCSOC12CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED		CHSEL	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL		RESERVED					ACQPS
R/W-0h		R-0h					R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-39. ADCSOC12CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-39. ADCSOC12CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-39. ADCSOC12CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.30 ADCSOC13CTL Register (offset = 2Ah) [reset = 0h]ADCSOC13CTL is shown in [Figure 8-41](#) and described in [Table 8-40](#).

ADC SOC13 Control Register

Figure 8-41. ADCSOC13CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	CHSEL		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-40. ADCSOC13CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-40. ADCSOC13CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-40. ADCSOC13CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.31 ADCSOC14CTL Register (offset = 2Ch) [reset = 0h]

ADCSOC14CTL is shown in [Figure 8-42](#) and described in [Table 8-41](#).

ADC SOC14 Control Register

Figure 8-42. ADCSOC14CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED		CHSEL	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL		RESERVED					ACQPS
R/W-0h		R-0h					R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-41. ADCSOC14CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-41. ADCSOC14CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-41. ADCSOC14CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.32 ADCSOC15CTL Register (offset = 2Eh) [reset = 0h]

ADCSOC15CTL is shown in [Figure 8-43](#) and described in [Table 8-42](#).

ADC SOC15 Control Register

Figure 8-43. ADCSOC15CTL Register

31	30	29	28	27	26	25	24
RESERVED							TRIGSEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	CHSEL		
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CHSEL	RESERVED						ACQPS
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-42. ADCSOC15CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved

Table 8-42. ADCSOC15CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-20	TRIGSEL	R/W	0h	SOC Trigger Source Select. Along with the corresponding SOC field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the corresponding SOC flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - CPU1 Timer 0, TINT0n 02h ADCTRIG2 - CPU1 Timer 1, TINT1n 03h ADCTRIG3 - CPU1 Timer 2, TINT2n 04h ADCTRIG4 - GPIO, ADCEXTSOC 05h ADCTRIG5 - ePWM1, ADCSOCA/C 06h ADCTRIG6 - ePWM1, ADCSOCB/D 07h ADCTRIG7 - ePWM2, ADCSOCA/C 08h ADCTRIG8 - ePWM2, ADCSOCB/D 09h ADCTRIG9 - ePWM3, ADCSOCA/C 0Ah ADCTRIG10 - ePWM3, ADCSOCB/D 0Bh ADCTRIG11 - ePWM4, ADCSOCA/C 0Ch ADCTRIG12 - ePWM4, ADCSOCB/D 0Dh ADCTRIG13 - ePWM5, ADCSOCA/C 0Eh ADCTRIG14 - ePWM5, ADCSOCB/D 0Fh ADCTRIG15 - ePWM6, ADCSOCA/C 10h ADCTRIG16 - ePWM6, ADCSOCB/D 11h ADCTRIG17 - ePWM7, ADCSOCA/C 12h ADCTRIG18 - ePWM7, ADCSOCB/D 13h ADCTRIG19 - ePWM8, ADCSOCA/C 14h ADCTRIG20 - ePWM8, ADCSOCB/D 15h ADCTRIG21 - ePWM9, ADCSOCA/C 16h ADCTRIG22 - ePWM9, ADCSOCB/D 17h ADCTRIG23 - ePWM10, ADCSOCA/C 18h ADCTRIG24 - ePWM10, ADCSOCB/D 19h ADCTRIG25 - ePWM11, ADCSOCA/C 1Ah ADCTRIG26 - ePWM11, ADCSOCB/D 1Bh ADCTRIG27 - ePWM12, ADCSOCA/C 1Ch ADCTRIG28 - ePWM12, ADCSOCB/D 1Dh ADCTRIG29 - CPU2 Timer 0, TINT0n 1Eh ADCTRIG30 - CPU2 Timer 1, TINT1n 1Fh ADCTRIG31 - CPU2 Timer 2, TINT2n
19	RESERVED	R	0h	Reserved

Table 8-42. ADCSOC15CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	CHSEL	R/W	0h	<p>SOC Channel Select. Selects the channel to be converted when this SOC is received by the ADC.</p> <p>Single-ended Signaling Mode (SIGNALMODE = 0):</p> <ul style="list-style-type: none"> 0h ADCIN0 1h ADCIN1 2h ADCIN2 3h ADCIN3 4h ADCIN4 5h ADCIN5 6h ADCIN6 7h ADCIN7 8h ADCIN8 9h ADCIN9 Ah ADCIN10 Bh ADCIN11 Ch ADCIN12 Dh ADCIN13 Eh ADCIN14 Fh ADCIN15 <p>Differential Signaling Mode (SIGNALMODE = 1):</p> <ul style="list-style-type: none"> 0h ADCIN0 (non-inverting) and ADCIN1 (inverting) 1h ADCIN0 (non-inverting) and ADCIN1 (inverting) 2h ADCIN2 (non-inverting) and ADCIN3 (inverting) 3h ADCIN2 (non-inverting) and ADCIN3 (inverting) 4h ADCIN4 (non-inverting) and ADCIN5 (inverting) 5h ADCIN4 (non-inverting) and ADCIN5 (inverting) 6h ADCIN6 (non-inverting) and ADCIN7 (inverting) 7h ADCIN6 (non-inverting) and ADCIN7 (inverting) 8h ADCIN8 (non-inverting) and ADCIN9 (inverting) 9h ADCIN8 (non-inverting) and ADCIN9 (inverting) Ah ADCIN10 (non-inverting) and ADCIN11 (inverting) Bh ADCIN10 (non-inverting) and ADCIN11 (inverting) Ch ADCIN12 (non-inverting) and ADCIN13 (inverting) Dh ADCIN12 (non-inverting) and ADCIN13 (inverting) Eh ADCIN14 (non-inverting) and ADCIN15 (inverting) Fh ADCIN14 (non-inverting) and ADCIN15 (inverting)
14-9	RESERVED	R	0h	Reserved
8-0	ACQPS	R/W	0h	<p>SOC Acquisition Prescale. Controls the sample and hold window for this SOC. The minimum acquisition time is one ADCCLK cycle.</p> <p>000h Sample window is 1 system clock cycle wide</p> <p>001h Sample window is 2 system clock cycles wide</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p>

8.4.2.33 ADCEVTSTAT Register (offset = 30h) [reset = 0h]

ADCEVTSTAT is shown in [Figure 8-44](#) and described in [Table 8-43](#).

ADC Event Status Register

Figure 8-44. ADCEVTSTAT Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-43. ADCEVTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	PPB4ZERO	R	0h	Post Processing Block 4 Zero Crossing Flag. When set indicates the ADCPPB4RESULT register has changed sign.
13	PPB4TRIPLO	R	0h	Post Processing Block 4 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
12	PPB4TRIPHI	R	0h	Post Processing Block 4 Trip High Flag. When set indicates a digital compare trip high event has occurred.
11	RESERVED	R	0h	Reserved
10	PPB3ZERO	R	0h	Post Processing Block 3 Zero Crossing Flag. When set indicates the ADCPPB3RESULT register has changed sign.
9	PPB3TRIPLO	R	0h	Post Processing Block 3 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
8	PPB3TRIPHI	R	0h	Post Processing Block 3 Trip High Flag. When set indicates a digital compare trip high event has occurred.
7	RESERVED	R	0h	Reserved
6	PPB2ZERO	R	0h	Post Processing Block 2 Zero Crossing Flag. When set indicates the ADCPPB2RESULT register has changed sign.
5	PPB2TRIPLO	R	0h	Post Processing Block 2 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
4	PPB2TRIPHI	R	0h	Post Processing Block 2 Trip High Flag. When set indicates a digital compare trip high event has occurred.
3	RESERVED	R	0h	Reserved
2	PPB1ZERO	R	0h	Post Processing Block 1 Zero Crossing Flag. When set indicates the ADCPPB1RESULT register has changed sign.
1	PPB1TRIPLO	R	0h	Post Processing Block 1 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
0	PPB1TRIPHI	R	0h	Post Processing Block 1 Trip High Flag. When set indicates a digital compare trip high event has occurred.

8.4.2.34 ADCEVTCLR Register (offset = 32h) [reset = 0h]

ADCEVTCLR is shown in [Figure 8-45](#) and described in [Table 8-44](#).

ADC Event Clear Register

Figure 8-45. ADCEVTCLR Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-44. ADCEVTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
11	RESERVED	R	0h	Reserved
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
7	RESERVED	R	0h	Reserved
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
3	RESERVED	R	0h	Reserved
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.

8.4.2.35 ADCEVTSEL Register (offset = 34h) [reset = 0h]

ADCEVTSEL is shown in [Figure 8-46](#) and described in [Table 8-45](#).

ADC Event Selection Register

Figure 8-46. ADCEVTSEL Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-45. ADCEVTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
11	RESERVED	R	0h	Reserved
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
7	RESERVED	R	0h	Reserved
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
3	RESERVED	R	0h	Reserved

Table 8-45. ADCEVTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

8.4.2.36 ADCEVTINTSEL Register (offset = 36h) [reset = 0h]

ADCEVTINTSEL is shown in [Figure 8-47](#) and described in [Table 8-46](#).

ADC Event Interrupt Selection Register

Figure 8-47. ADCEVTINTSEL Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-46. ADCEVTINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
11	RESERVED	R	0h	Reserved
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
7	RESERVED	R	0h	Reserved
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
3	RESERVED	R	0h	Reserved

Table 8-46. ADCEVTINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

8.4.2.37 ADCCOUNTER Register (offset = 39h) [reset = 0h]

ADCCOUNTER is shown in Figure 8-48 and described in Table 8-47.

ADC Counter Register

Figure 8-48. ADCCOUNTER Register

15	14	13	12	11	10	9	8
RESERVED				FREECOUNT			
R-0h				R-0h			
7	6	5	4	3	2	1	0
FREECOUNT				R-0h			

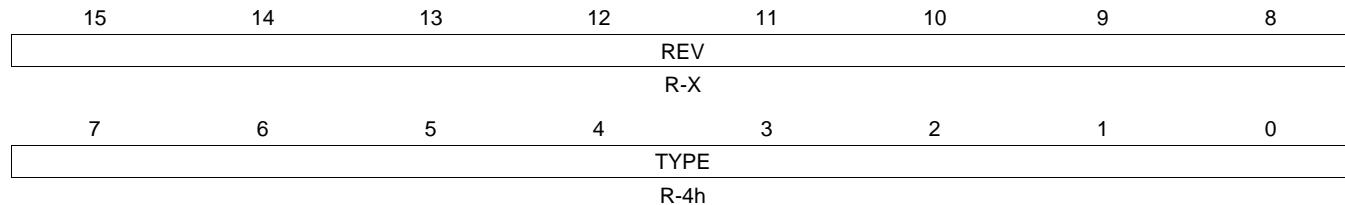
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-47. ADCCOUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	FREECOUNT	R	0h	ADC Free Running Counter Value. This bit field reflects the status of the free running ADC counter.

8.4.2.38 ADCREV Register (offset = 3Ah) [reset = 4h]ADCREV is shown in [Figure 8-49](#) and described in [Table 8-48](#).

ADC Revision Register

Figure 8-49. ADCREV Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

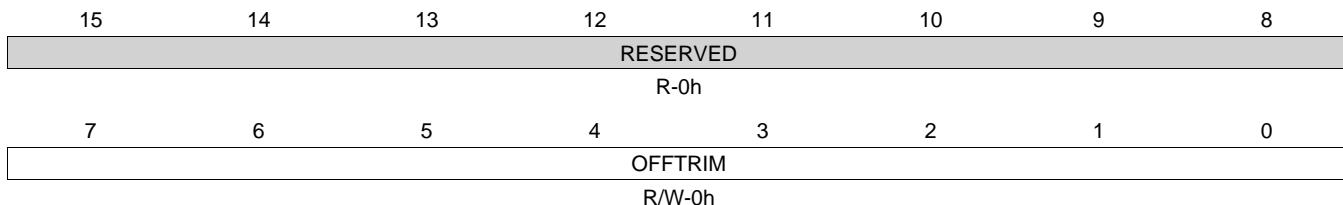
Table 8-48. ADCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	REV	R	X	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h.
7-0	TYPE	R	4h	ADC Type. Always set to 4 for this ADC.

8.4.2.39 ADCOFFTRIM Register (offset = 3Bh) [reset = 0h]

ADCOFFTRIM is shown in [Figure 8-50](#) and described in [Table 8-49](#).

ADC Offset Trim Register

Figure 8-50. ADCOFFTRIM Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-49. ADCOFFTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	OFFTRIM	R/W	0h	ADC Offset Trim. This value equates to a 16-bit mode trim. When the ADC is operating in 12-bit mode the value of this bus must be shifted right by 4 to determine the number of LSBs the offset is adjusted. A value of 0 defines a trim midpoint (0 is equivalent to 0x3F). A value of 1 defines the minimum offset. A value of 0x7F defines the maximum trim. These bits are loaded by device boot code with a factory trim setting.

8.4.2.40 ADCPPB1CONFIG Register (offset = 40h) [reset = 0h]ADCPPB1CONFIG is shown in [Figure 8-51](#) and described in [Table 8-50](#).

ADC PPB1 Config Register

Figure 8-51. ADCPPB1CONFIG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		TWOSCOMPE N			CONFIG		
R-0h		R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 8-50. ADCPPB1CONFIG Register Field Descriptions

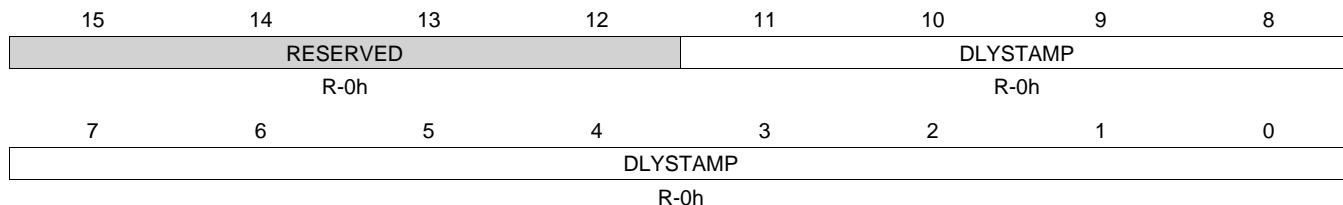
Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the appropriate ADCPPBxRESULT register. 0 ADCPPBxRESULT = ADCRESULTx - ADCSOCxOFFREF 1 ADCPPBxRESULT = ADCSOCxOFFREF - ADCRESULTx

Table 8-50. ADCPPB1CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CONFIG	R/W	0h	ADC Post Processing Block Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with this post processing block 0001 SOC1/EOC1/RESULT1 is associated with this post processing block 0010 SOC2/EOC2/RESULT2 is associated with this post processing block 0011 SOC3/EOC3/RESULT3 is associated with this post processing block 0100 SOC4/EOC4/RESULT4 is associated with this post processing block 0101 SOC5/EOC5/RESULT5 is associated with this post processing block 0110 SOC6/EOC6/RESULT6 is associated with this post processing block 0111 SOC7/EOC7/RESULT7 is associated with this post processing block 1000 SOC8/EOC8/RESULT8 is associated with this post processing block 1001 SOC9/EOC9/RESULT9 is associated with this post processing block 1010 SOC10/EOC10/RESULT10 is associated with this post processing block 1011 SOC11/EOC11/RESULT11 is associated with this post processing block 1100 SOC12/EOC12/RESULT12 is associated with this post processing block 1101 SOC13/EOC13/RESULT13 is associated with this post processing block 1110 SOC14/EOC14/RESULT14 is associated with this post processing block 1111 SOC15/EOC15/RESULT15 is associated with this post processing block

8.4.2.41 ADCPPB1STAMP Register (offset = 41h) [reset = 0h]ADCPPB1STAMP is shown in [Figure 8-52](#) and described in [Table 8-51](#).

ADC PPB1 Sample Delay Time Stamp Register

Figure 8-52. ADCPPB1STAMP Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

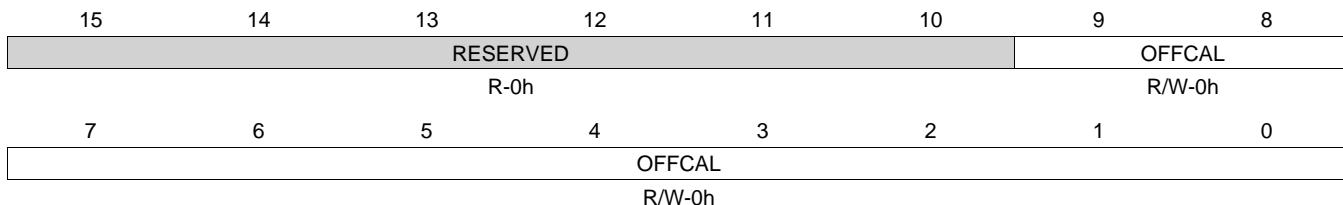
Table 8-51. ADCPPB1STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DLYSTAMP	R	0h	ADC Post Processing Block Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

8.4.2.42 ADCPPB1OFFCAL Register (offset = 42h) [reset = 0h]

ADCPPB1OFFCAL is shown in [Figure 8-53](#) and described in [Table 8-52](#).

ADC PPB1 Offset Calibration Register

Figure 8-53. ADCPPB1OFFCAL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-52. ADCPPB1OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	OFFCAL	R/W	0h	<p>ADC Post Processing Block Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register.</p> <p>000h No change. The ADC output is stored directly into ADCRESULT.</p> <p>001h ADC output - 1 is stored into ADCRESULT.</p> <p>002h ADC output - 2 is stored into ADCRESULT.</p> <p>...</p> <p>200h ADC output + 512 is stored into ADCRESULT.</p> <p>...</p> <p>3FFh ADC output + 1 is stored into ADCRESULT.</p> <p>NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 03FFh before being stored into the ADCRESULT register.</p>

8.4.2.43 ADCPPB1OFFREF Register (offset = 43h) [reset = 0h]ADCPPB1OFFREF is shown in [Figure 8-54](#) and described in [Table 8-53](#).

ADC PPB1 Offset Reference Register

Figure 8-54. ADCPPB1OFFREF Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFREF															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

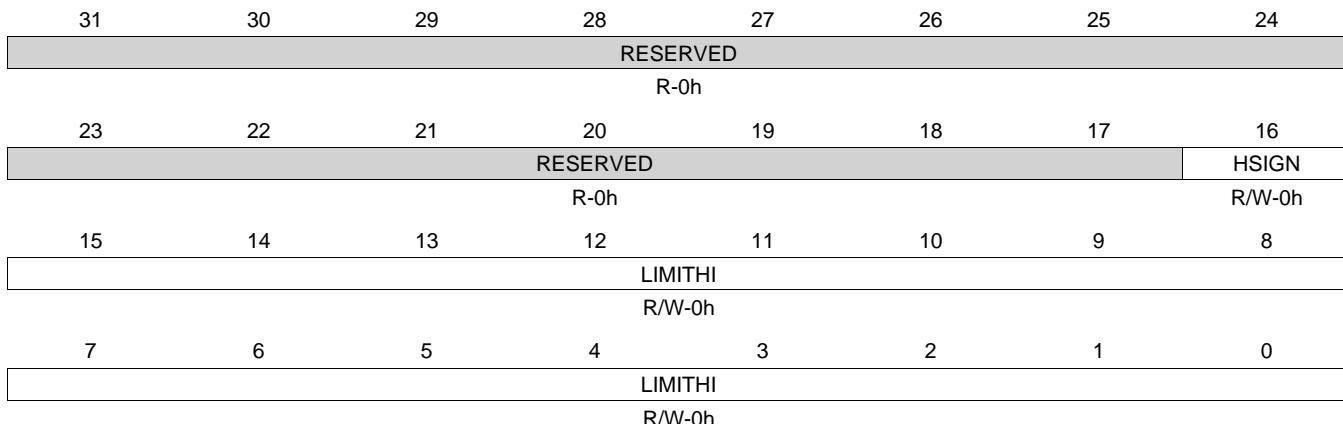
Table 8-53. ADCPPB1OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	OFFREF	R/W	0h	<p>ADC Post Processing Block Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB1RESULT register. This subtraction is not saturated.</p> <p>0000h No change. The ADCRESULT value is passed on.</p> <p>0001h ADCRESULT - 1 is passed on.</p> <p>0002h ADCRESULT - 2 is passed on.</p> <p>...</p> <p>8000h ADCRESULT - 32,768 is passed on.</p> <p>...</p> <p>FFFFh ADCRESULT - 65,535 is passed on.</p> <p>NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.</p>

8.4.2.44 ADCPPB1TRIPHI Register (offset = 44h) [reset = 0h]

ADCPPB1TRIPHI is shown in [Figure 8-55](#) and described in [Table 8-54](#).

ADC PPB1 Trip High Register

Figure 8-55. ADCPPB1TRIPHI Register

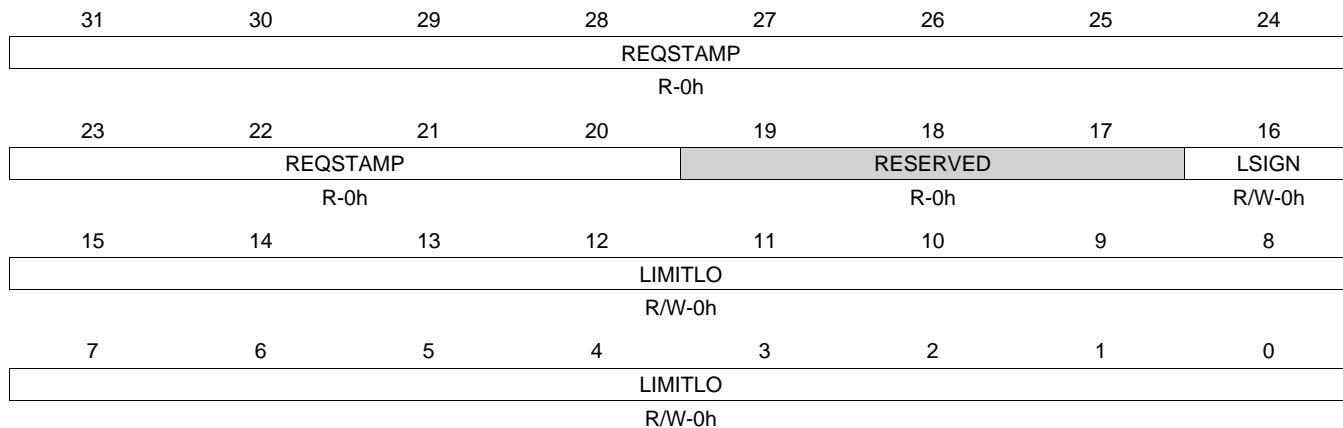
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-54. ADCPPB1TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15-0	LIMITHI	R/W	0h	ADC Post Processing Block Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the associated ADCPPBxRESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRRESULT bit field of the associated ADCPPBxRESULT register.

8.4.2.45 ADCPPB1TRIPLO Register (offset = 46h) [reset = 0h]ADCPPB1TRIPLO is shown in [Figure 8-56](#) and described in [Table 8-55](#).

ADC PPB1 Trip Low/Trigger Time Stamp Register

Figure 8-56. ADCPPB1TRIPLO Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

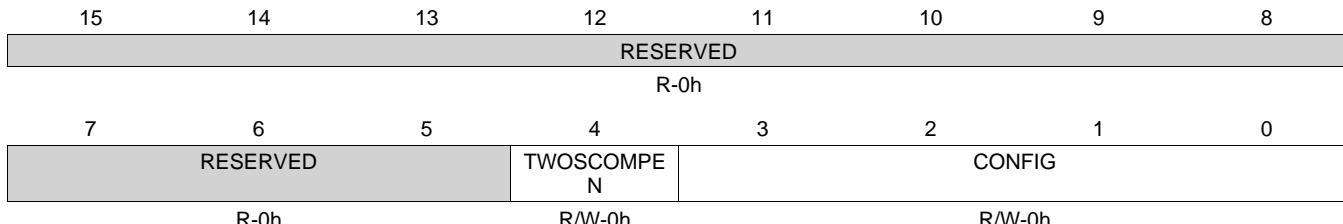
Table 8-55. ADCPPB1TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	REQSTAMP	R	0h	ADC Post Processing Block Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19-17	RESERVED	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15-0	LIMITLO	R/W	0h	ADC Post Processing Block Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the associated ADCPPBxRESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRRESULT bit field of the associated ADCPPBxRESULT register.

8.4.2.46 ADCPPB2CONFIG Register (offset = 48h) [reset = 0h]

ADCPPB2CONFIG is shown in [Figure 8-57](#) and described in [Table 8-56](#).

ADC PPB2 Config Register

Figure 8-57. ADCPPB2CONFIG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 8-56. ADCPPB2CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the appropriate ADCPPBxRESULT register. 0 ADCPPBxRESULT = ADCRESULTx - ADCSOCxOFFREF 1 ADCPPBxRESULT = ADCSOCxOFFREF - ADCRESULTx

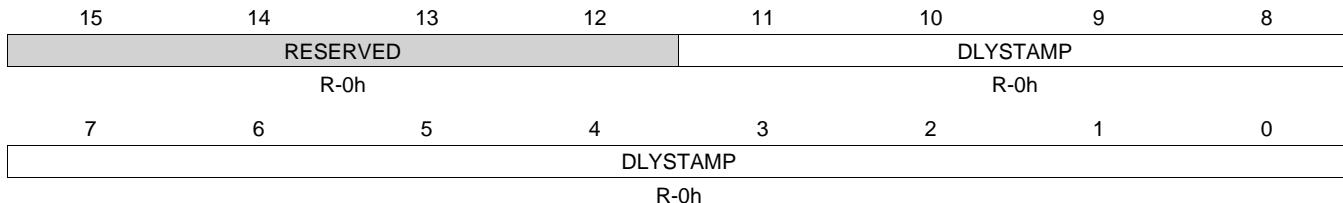
Table 8-56. ADCPPB2CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CONFIG	R/W	0h	ADC Post Processing Block Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with this post processing block 0001 SOC1/EOC1/RESULT1 is associated with this post processing block 0010 SOC2/EOC2/RESULT2 is associated with this post processing block 0011 SOC3/EOC3/RESULT3 is associated with this post processing block 0100 SOC4/EOC4/RESULT4 is associated with this post processing block 0101 SOC5/EOC5/RESULT5 is associated with this post processing block 0110 SOC6/EOC6/RESULT6 is associated with this post processing block 0111 SOC7/EOC7/RESULT7 is associated with this post processing block 1000 SOC8/EOC8/RESULT8 is associated with this post processing block 1001 SOC9/EOC9/RESULT9 is associated with this post processing block 1010 SOC10/EOC10/RESULT10 is associated with this post processing block 1011 SOC11/EOC11/RESULT11 is associated with this post processing block 1100 SOC12/EOC12/RESULT12 is associated with this post processing block 1101 SOC13/EOC13/RESULT13 is associated with this post processing block 1110 SOC14/EOC14/RESULT14 is associated with this post processing block 1111 SOC15/EOC15/RESULT15 is associated with this post processing block

8.4.2.47 ADCPPB2STAMP Register (offset = 49h) [reset = 0h]

ADCPPB2STAMP is shown in [Figure 8-58](#) and described in [Table 8-57](#).

ADC PPB2 Sample Delay Time Stamp Register

Figure 8-58. ADCPPB2STAMP Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-57. ADCPPB2STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DLYSTAMP	R	0h	ADC Post Processing Block Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

8.4.2.48 ADCPPB2OFFCAL Register (offset = 4Ah) [reset = 0h]ADCPPB2OFFCAL is shown in [Figure 8-59](#) and described in [Table 8-58](#).

ADC PPB2 Offset Calibration Register

Figure 8-59. ADCPPB2OFFCAL Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
OFFCAL						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-58. ADCPPB2OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	OFFCAL	R/W	0h	ADC Post Processing Block Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 03FFh before being stored into the ADCRESULT register.

8.4.2.49 ADCPPB2OFFREF Register (offset = 4Bh) [reset = 0h]

ADCPPB2OFFREF is shown in [Figure 8-60](#) and described in [Table 8-59](#).

ADC PPB2 Offset Reference Register

Figure 8-60. ADCPPB2OFFREF Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFREF															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

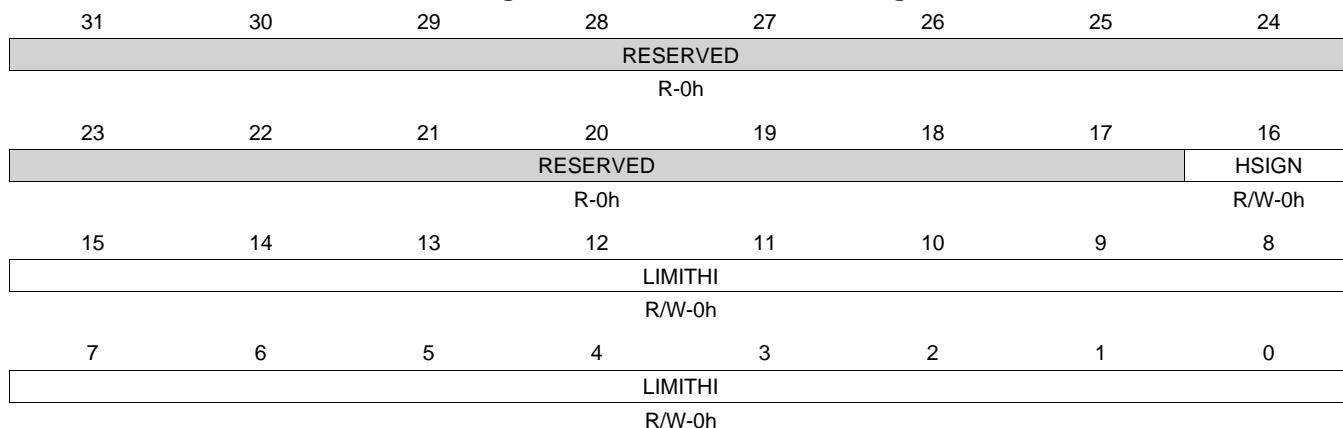
Table 8-59. ADCPPB2OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	OFFREF	R/W	0h	<p>ADC Post Processing Block Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB2RESULT register. This subtraction is not saturated.</p> <p>0000h No change. The ADCRESULT value is passed on.</p> <p>0001h ADCRESULT - 1 is passed on.</p> <p>0002h ADCRESULT - 2 is passed on.</p> <p>...</p> <p>8000h ADCRESULT - 32,768 is passed on.</p> <p>...</p> <p>FFFFh ADCRESULT - 65,535 is passed on.</p> <p>NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.</p>

8.4.2.50 ADCPPB2TRIPHI Register (offset = 4Ch) [reset = 0h]

ADCPPB2TRIPHI is shown in [Figure 8-61](#) and described in [Table 8-60](#).

ADC PPB2 Trip High Register

Figure 8-61. ADCPPB2TRIPHI Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

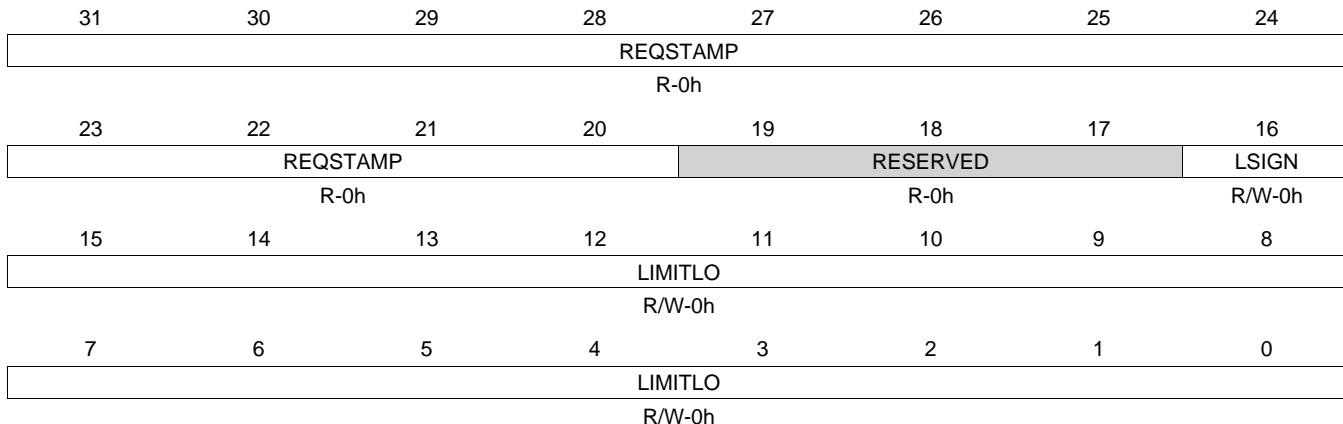
Table 8-60. ADCPPB2TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15-0	LIMITHI	R/W	0h	ADC Post Processing Block Trip High Limit. This value sets the digital comparator trip high limit.

8.4.2.51 ADCPPB2TRIPLO Register (offset = 4Eh) [reset = 0h]

ADCPPB2TRIPLO is shown in [Figure 8-62](#) and described in [Table 8-61](#).

ADC PPB2 Trip Low/Trigger Time Stamp Register

Figure 8-62. ADCPPB2TRIPLO Register

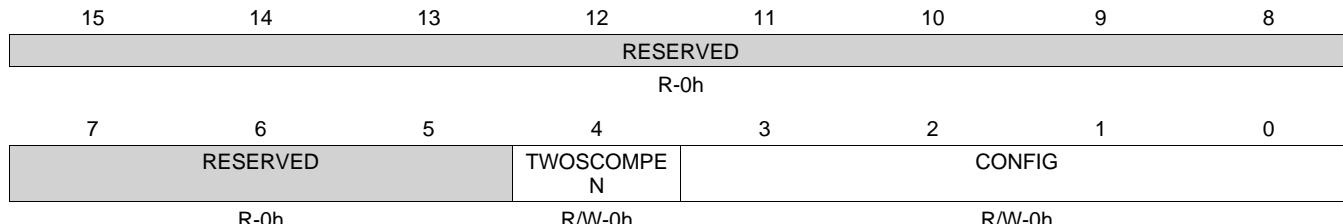
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-61. ADCPPB2TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	REQSTAMP	R	0h	ADC Post Processing Block Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19-17	RESERVED	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15-0	LIMITLO	R/W	0h	ADC Post Processing Block Trip Low Limit. This value sets the digital comparator trip low limit.

8.4.2.52 ADCPPB3CONFIG Register (offset = 50h) [reset = 0h]ADCPPB3CONFIG is shown in [Figure 8-63](#) and described in [Table 8-62](#).

ADC PPB3 Config Register

Figure 8-63. ADCPPB3CONFIG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-62. ADCPPB3CONFIG Register Field Descriptions

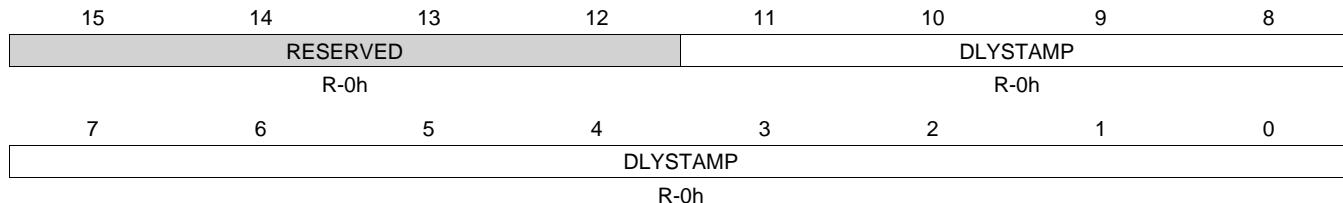
Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the appropriate ADCPPBxRESULT register. 0 ADCPPBxRESULT = ADCRESULTx - ADCSOCxOFFREF 1 ADCPPBxRESULT = ADCSOCxOFFREF - ADCRESULTx

Table 8-62. ADCPPB3CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CONFIG	R/W	0h	<p>ADC Post Processing Block Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block.</p> <p>0000 SOC0/EOC0/RESULT0 is associated with this post processing block</p> <p>0001 SOC1/EOC1/RESULT1 is associated with this post processing block</p> <p>0010 SOC2/EOC2/RESULT2 is associated with this post processing block</p> <p>0011 SOC3/EOC3/RESULT3 is associated with this post processing block</p> <p>0100 SOC4/EOC4/RESULT4 is associated with this post processing block</p> <p>0101 SOC5/EOC5/RESULT5 is associated with this post processing block</p> <p>0110 SOC6/EOC6/RESULT6 is associated with this post processing block</p> <p>0111 SOC7/EOC7/RESULT7 is associated with this post processing block</p> <p>1000 SOC8/EOC8/RESULT8 is associated with this post processing block</p> <p>1001 SOC9/EOC9/RESULT9 is associated with this post processing block</p> <p>1010 SOC10/EOC10/RESULT10 is associated with this post processing block</p> <p>1011 SOC11/EOC11/RESULT11 is associated with this post processing block</p> <p>1100 SOC12/EOC12/RESULT12 is associated with this post processing block</p> <p>1101 SOC13/EOC13/RESULT13 is associated with this post processing block</p> <p>1110 SOC14/EOC14/RESULT14 is associated with this post processing block</p> <p>1111 SOC15/EOC15/RESULT15 is associated with this post processing block</p>

8.4.2.53 ADCPPB3STAMP Register (offset = 51h) [reset = 0h]ADCPPB3STAMP is shown in [Figure 8-64](#) and described in [Table 8-63](#).

ADC PPB3 Sample Delay Time Stamp Register

Figure 8-64. ADCPPB3STAMP Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-63. ADCPPB3STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DLYSTAMP	R	0h	ADC Post Processing Block Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

8.4.2.54 ADCPPB3OFFCAL Register (offset = 52h) [reset = 0h]

ADCPPB3OFFCAL is shown in [Figure 8-65](#) and described in [Table 8-64](#).

ADC PPB3 Offset Calibration Register

Figure 8-65. ADCPPB3OFFCAL Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
OFFCAL						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-64. ADCPPB3OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	OFFCAL	R/W	0h	<p>ADC Post Processing Block Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register.</p> <p>000h No change. The ADC output is stored directly into ADCRESULT.</p> <p>001h ADC output - 1 is stored into ADCRESULT.</p> <p>002h ADC output - 2 is stored into ADCRESULT.</p> <p>...</p> <p>200h ADC output + 512 is stored into ADCRESULT.</p> <p>...</p> <p>3FFh ADC output + 1 is stored into ADCRESULT.</p> <p>NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 03FFh before being stored into the ADCRESULT register.</p>

8.4.2.55 ADCPPB3OFFREF Register (offset = 53h) [reset = 0h]ADCPPB3OFFREF is shown in [Figure 8-66](#) and described in [Table 8-65](#).

ADC PPB3 Offset Reference Register

Figure 8-66. ADCPPB3OFFREF Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFREF															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

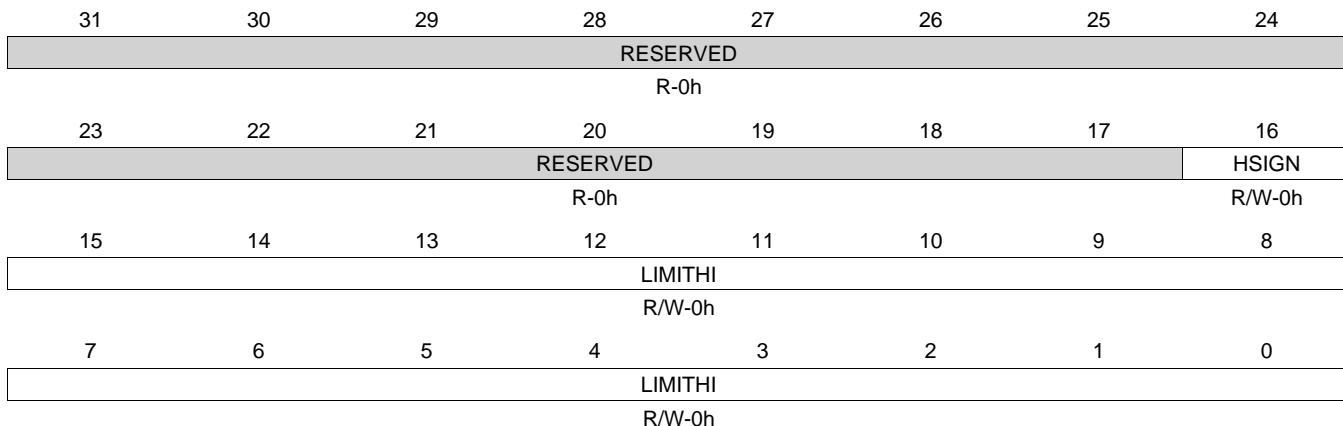
Table 8-65. ADCPPB3OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	OFFREF	R/W	0h	<p>ADC Post Processing Block Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB3RESULT register. This subtraction is not saturated.</p> <p>0000h No change. The ADCRESULT value is passed on.</p> <p>0001h ADCRESULT - 1 is passed on.</p> <p>0002h ADCRESULT - 2 is passed on.</p> <p>...</p> <p>8000h ADCRESULT - 32,768 is passed on.</p> <p>...</p> <p>FFFFh ADCRESULT - 65,535 is passed on.</p> <p>NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.</p>

8.4.2.56 ADCPPB3TRIPHI Register (offset = 54h) [reset = 0h]

ADCPPB3TRIPHI is shown in [Figure 8-67](#) and described in [Table 8-66](#).

ADC PPB3 Trip High Register

Figure 8-67. ADCPPB3TRIPHI Register

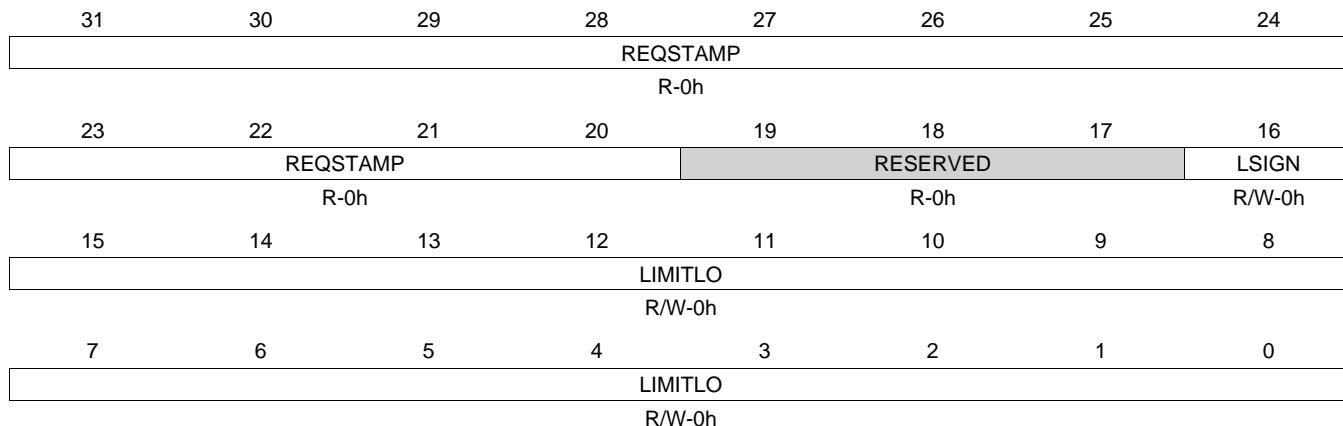
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-66. ADCPPB3TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15-0	LIMITHI	R/W	0h	ADC Post Processing Block Trip High Limit. This value sets the digital comparator trip high limit.

8.4.2.57 ADCPPB3TRIPLO Register (offset = 56h) [reset = 0h]ADCPPB3TRIPLO is shown in [Figure 8-68](#) and described in [Table 8-67](#).

ADC PPB3 Trip Low/Trigger Time Stamp Register

Figure 8-68. ADCPPB3TRIPLO Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

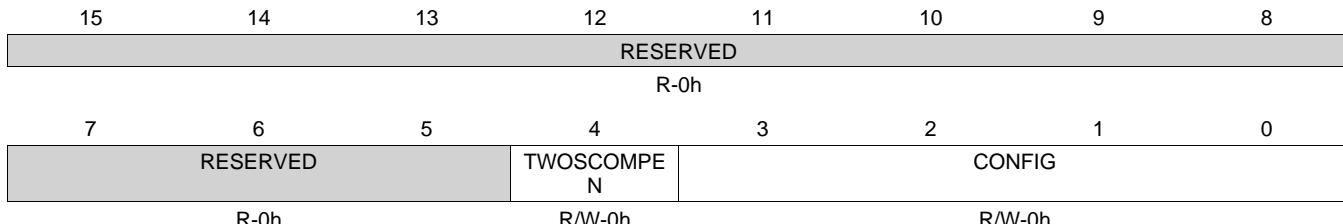
Table 8-67. ADCPPB3TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	REQSTAMP	R	0h	ADC Post Processing Block Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19-17	RESERVED	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15-0	LIMITLO	R/W	0h	ADC Post Processing Block Trip Low Limit. This value sets the digital comparator trip low limit.

8.4.2.58 ADCPPB4CONFIG Register (offset = 58h) [reset = 0h]

ADCPPB4CONFIG is shown in [Figure 8-69](#) and described in [Table 8-68](#).

ADC PPB4 Config Register

Figure 8-69. ADCPPB4CONFIG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-68. ADCPPB4CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the appropriate ADCPPBxRESULT register. 0 ADCPPBxRESULT = ADCRESULTx - ADCSOCxOFFREF 1 ADCPPBxRESULT = ADCSOCxOFFREF - ADCRESULTx

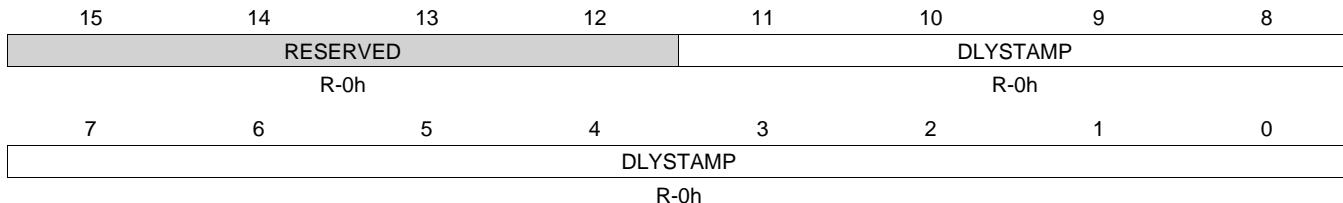
Table 8-68. ADCPPB4CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CONFIG	R/W	0h	ADC Post Processing Block Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with this post processing block 0001 SOC1/EOC1/RESULT1 is associated with this post processing block 0010 SOC2/EOC2/RESULT2 is associated with this post processing block 0011 SOC3/EOC3/RESULT3 is associated with this post processing block 0100 SOC4/EOC4/RESULT4 is associated with this post processing block 0101 SOC5/EOC5/RESULT5 is associated with this post processing block 0110 SOC6/EOC6/RESULT6 is associated with this post processing block 0111 SOC7/EOC7/RESULT7 is associated with this post processing block 1000 SOC8/EOC8/RESULT8 is associated with this post processing block 1001 SOC9/EOC9/RESULT9 is associated with this post processing block 1010 SOC10/EOC10/RESULT10 is associated with this post processing block 1011 SOC11/EOC11/RESULT11 is associated with this post processing block 1100 SOC12/EOC12/RESULT12 is associated with this post processing block 1101 SOC13/EOC13/RESULT13 is associated with this post processing block 1110 SOC14/EOC14/RESULT14 is associated with this post processing block 1111 SOC15/EOC15/RESULT15 is associated with this post processing block

8.4.2.59 ADCPPB4STAMP Register (offset = 59h) [reset = 0h]

ADCPPB4STAMP is shown in [Figure 8-70](#) and described in [Table 8-69](#).

ADC PPB4 Sample Delay Time Stamp Register

Figure 8-70. ADCPPB4STAMP Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-69. ADCPPB4STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DLYSTAMP	R	0h	ADC Post Processing Block Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

8.4.2.60 ADCPPB4OFFCAL Register (offset = 5Ah) [reset = 0h]ADCPPB4OFFCAL is shown in [Figure 8-71](#) and described in [Table 8-70](#).

ADC PPB4 Offset Calibration Register

Figure 8-71. ADCPPB4OFFCAL Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
OFFCAL						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-70. ADCPPB4OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	OFFCAL	R/W	0h	<p>ADC Post Processing Block Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register.</p> <p>000h No change. The ADC output is stored directly into ADCRESULT.</p> <p>001h ADC output - 1 is stored into ADCRESULT.</p> <p>002h ADC output - 2 is stored into ADCRESULT.</p> <p>...</p> <p>200h ADC output + 512 is stored into ADCRESULT.</p> <p>...</p> <p>3FFh ADC output + 1 is stored into ADCRESULT.</p> <p>NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 03FFh before being stored into the ADCRESULT register.</p>

8.4.2.61 ADCPPB4OFFREF Register (offset = 5Bh) [reset = 0h]

ADCPPB4OFFREF is shown in [Figure 8-72](#) and described in [Table 8-71](#).

ADC PPB4 Offset Reference Register

Figure 8-72. ADCPPB4OFFREF Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFREF															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

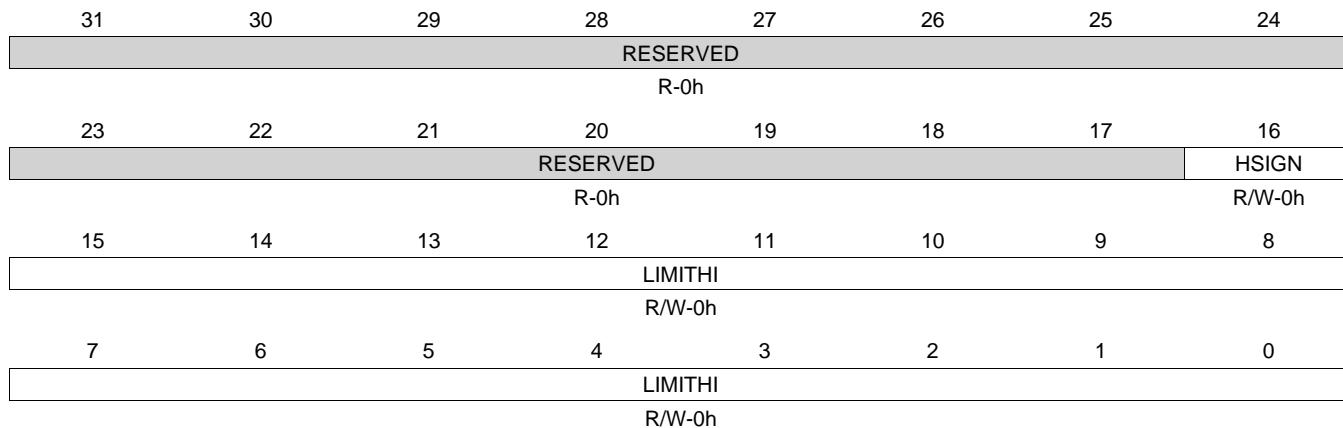
Table 8-71. ADCPPB4OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	OFFREF	R/W	0h	<p>ADC Post Processing Block Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB4RESULT register. This subtraction is not saturated.</p> <p>0000h No change. The ADCRESULT value is passed on.</p> <p>0001h ADCRESULT - 1 is passed on.</p> <p>0002h ADCRESULT - 2 is passed on.</p> <p>...</p> <p>8000h ADCRESULT - 32,768 is passed on.</p> <p>...</p> <p>FFFFh ADCRESULT - 65,535 is passed on.</p> <p>NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.</p>

8.4.2.62 ADCPPB4TRIPHI Register (offset = 5Ch) [reset = 0h]

ADCPPB4TRIPHI is shown in [Figure 8-73](#) and described in [Table 8-72](#).

ADC PPB4 Trip High Register

Figure 8-73. ADCPPB4TRIPHI Register

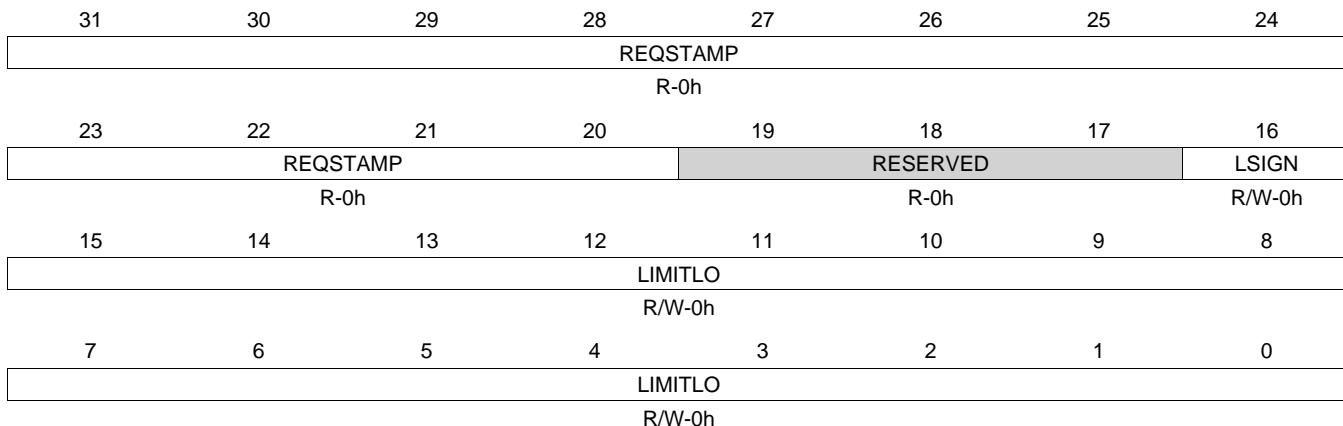
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-72. ADCPPB4TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15-0	LIMITHI	R/W	0h	ADC Post Processing Block Trip High Limit. This value sets the digital comparator trip high limit.

8.4.2.63 ADCPPB4TRIPLO Register (offset = 5Eh) [reset = 0h]ADCPPB4TRIPLO is shown in [Figure 8-74](#) and described in [Table 8-73](#).

ADC PPB4 Trip Low/Trigger Time Stamp Register

Figure 8-74. ADCPPB4TRIPLO Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-73. ADCPPB4TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	REQSTAMP	R	0h	ADC Post Processing Block Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19-17	RESERVED	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15-0	LIMITLO	R/W	0h	ADC Post Processing Block Trip Low Limit. This value sets the digital comparator trip low limit.

8.4.2.64 ADCINLTRIM1 Register (offset = 70h) [reset = 0h]ADCINLTRIM1 is shown in [Figure 8-75](#) and described in [Table 8-74](#).

ADC Linearity Trim 1 Register

Figure 8-75. ADCINLTRIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM31TO0																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-74. ADCINLTRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INLTRIM31TO0	R/W	0h	ADC Linearity Trim Bits 31-0.

8.4.2.65 ADCINLTRIM2 Register (offset = 72h) [reset = 0h]

ADCINLTRIM2 is shown in [Figure 8-76](#) and described in [Table 8-75](#).

ADC Linearity Trim 2 Register

Figure 8-76. ADCINLTRIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM63TO32																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-75. ADCINLTRIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INLTRIM63TO32	R/W	0h	ADC Linearity Trim Bits 63-32.

8.4.2.66 ADCINLTRIM3 Register (offset = 74h) [reset = 0h]ADCINLTRIM3 is shown in [Figure 8-77](#) and described in [Table 8-76](#).

ADC Linearity Trim 3 Register

Figure 8-77. ADCINLTRIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM95TO64																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-76. ADCINLTRIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INLTRIM95TO64	R/W	0h	ADC Linearity Trim Bits 95-64.

8.4.2.67 ADCINLTRIM4 Register (offset = 76h) [reset = 0h]

ADCINLTRIM4 is shown in [Figure 8-78](#) and described in [Table 8-77](#).

ADC Linearity Trim 4 Register

Figure 8-78. ADCINLTRIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM127TO96																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-77. ADCINLTRIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INLTRIM127TO96	R/W	0h	ADC Linearity Trim Bits 127-96.

8.4.2.68 ADCINLTRIM5 Register (offset = 78h) [reset = 0h]ADCINLTRIM5 is shown in [Figure 8-79](#) and described in [Table 8-78](#).

ADC Linearity Trim 5 Register

Figure 8-79. ADCINLTRIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM159TO128																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-78. ADCINLTRIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INLTRIM159TO128	R/W	0h	ADC Linearity Trim Bits 159-128.

8.4.2.69 ADCINLTRIM6 Register (offset = 7Ah) [reset = 0h]

ADCINLTRIM6 is shown in [Figure 8-80](#) and described in [Table 8-79](#).

ADC Linearity Trim 6 Register

Figure 8-80. ADCINLTRIM6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM191TO160																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-79. ADCINLTRIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INLTRIM191TO160	R/W	0h	ADC Linearity Trim Bits 191-160.

8.4.3 ADC_RESULT_REGS Registers

Table 8-80 lists the memory-mapped registers for the ADC_RESULT_REGS. All register offset addresses not listed in Table 8-80 should be considered as reserved locations and the register contents should not be modified.

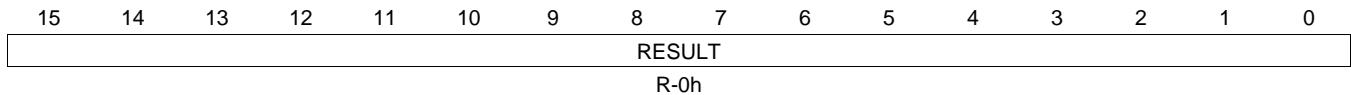
Table 8-80. ADC_RESULT_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	ADCRESULT0	ADC Result 0 Register	Section 8.4.3.1	
1h	ADCRESULT1	ADC Result 1 Register	Section 8.4.3.2	
2h	ADCRESULT2	ADC Result 2 Register	Section 8.4.3.3	
3h	ADCRESULT3	ADC Result 3 Register	Section 8.4.3.4	
4h	ADCRESULT4	ADC Result 4 Register	Section 8.4.3.5	
5h	ADCRESULT5	ADC Result 5 Register	Section 8.4.3.6	
6h	ADCRESULT6	ADC Result 6 Register	Section 8.4.3.7	
7h	ADCRESULT7	ADC Result 7 Register	Section 8.4.3.8	
8h	ADCRESULT8	ADC Result 8 Register	Section 8.4.3.9	
9h	ADCRESULT9	ADC Result 9 Register	Section 8.4.3.10	
Ah	ADCRESULT10	ADC Result 10 Register	Section 8.4.3.11	
Bh	ADCRESULT11	ADC Result 11 Register	Section 8.4.3.12	
Ch	ADCRESULT12	ADC Result 12 Register	Section 8.4.3.13	
Dh	ADCRESULT13	ADC Result 13 Register	Section 8.4.3.14	
Eh	ADCRESULT14	ADC Result 14 Register	Section 8.4.3.15	
Fh	ADCRESULT15	ADC Result 15 Register	Section 8.4.3.16	
10h	ADCPPB1RESULT	ADC Post Processing Block 1 Result Register	Section 8.4.3.17	
12h	ADCPPB2RESULT	ADC Post Processing Block 2 Result Register	Section 8.4.3.18	
14h	ADCPPB3RESULT	ADC Post Processing Block 3 Result Register	Section 8.4.3.19	
16h	ADCPPB4RESULT	ADC Post Processing Block 4 Result Register	Section 8.4.3.20	

8.4.3.1 ADCRESULT0 Register (offset = 0h) [reset = 0h]

ADCRESULT0 is shown in [Figure 8-81](#) and described in [Table 8-81](#).

ADC Result 0 Register

Figure 8-81. ADCRESULT0 Register

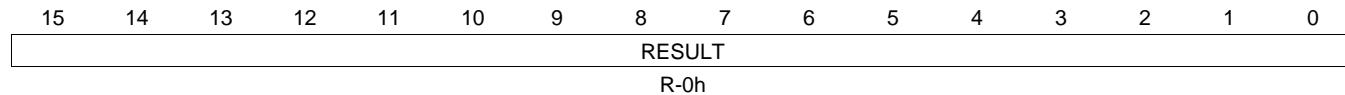
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-81. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

8.4.3.2 ADCRESULT1 Register (offset = 1h) [reset = 0h]ADCRESULT1 is shown in [Figure 8-82](#) and described in [Table 8-82](#).

ADC Result 1 Register

Figure 8-82. ADCRESULT1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-82. ADCRESULT1 Register Field Descriptions

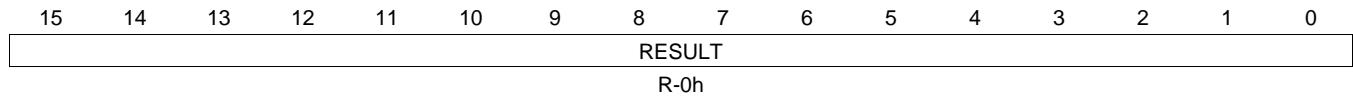
Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

8.4.3.3 ADCRESULT2 Register (offset = 2h) [reset = 0h]

ADCRESULT2 is shown in [Figure 8-83](#) and described in [Table 8-83](#).

ADC Result 2 Register

Figure 8-83. ADCRESULT2 Register



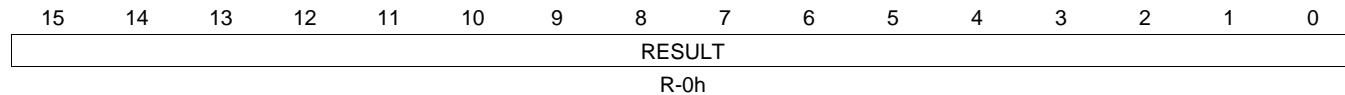
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-83. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

8.4.3.4 ADCRESULT3 Register (offset = 3h) [reset = 0h]ADCRESULT3 is shown in [Figure 8-84](#) and described in [Table 8-84](#).

ADC Result 3 Register

Figure 8-84. ADCRESULT3 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

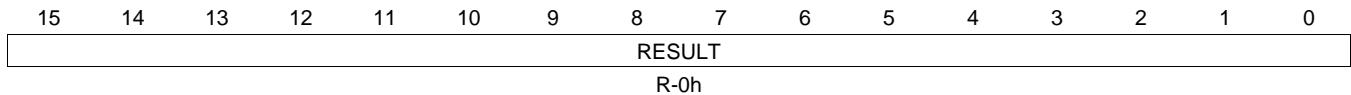
Table 8-84. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

8.4.3.5 ADCRESULT4 Register (offset = 4h) [reset = 0h]

ADCRESULT4 is shown in [Figure 8-85](#) and described in [Table 8-85](#).

ADC Result 4 Register

Figure 8-85. ADCRESULT4 Register

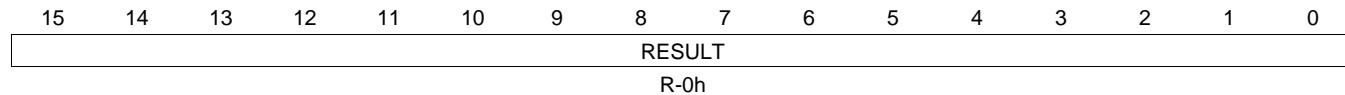
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-85. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

8.4.3.6 ADCRESULT5 Register (offset = 5h) [reset = 0h]ADCRESULT5 is shown in [Figure 8-86](#) and described in [Table 8-86](#).

ADC Result 5 Register

Figure 8-86. ADCRESULT5 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

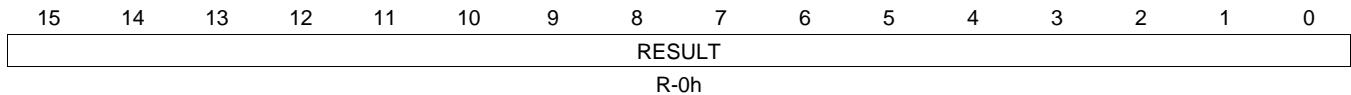
Table 8-86. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

8.4.3.7 ADCRESULT6 Register (offset = 6h) [reset = 0h]

ADCRESULT6 is shown in [Figure 8-87](#) and described in [Table 8-87](#).

ADC Result 6 Register

Figure 8-87. ADCRESULT6 Register

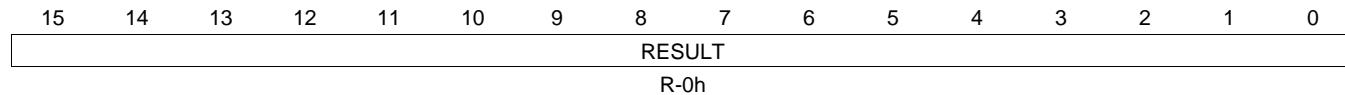
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-87. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

8.4.3.8 ADCRESULT7 Register (offset = 7h) [reset = 0h]ADCRESULT7 is shown in [Figure 8-88](#) and described in [Table 8-88](#).

ADC Result 7 Register

Figure 8-88. ADCRESULT7 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

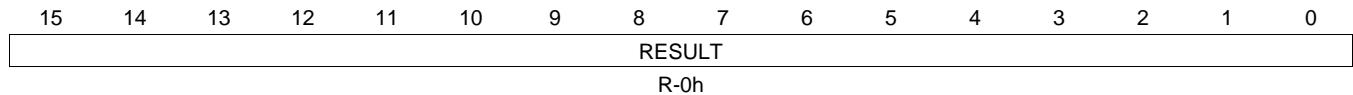
Table 8-88. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

8.4.3.9 ADCRESULT8 Register (offset = 8h) [reset = 0h]

ADCRESULT8 is shown in [Figure 8-89](#) and described in [Table 8-89](#).

ADC Result 8 Register

Figure 8-89. ADCRESULT8 Register

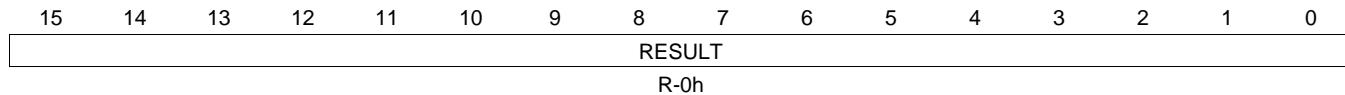
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-89. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

8.4.3.10 ADCRESULT9 Register (offset = 9h) [reset = 0h]ADCRESULT9 is shown in [Figure 8-90](#) and described in [Table 8-90](#).

ADC Result 9 Register

Figure 8-90. ADCRESULT9 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

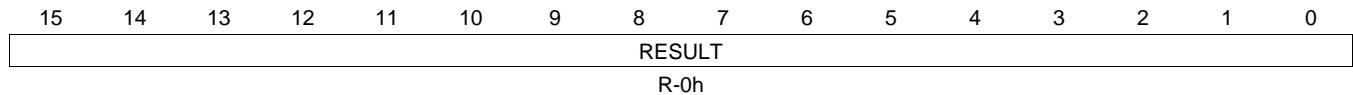
Table 8-90. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

8.4.3.11 ADCRESULT10 Register (offset = Ah) [reset = 0h]

ADCRESULT10 is shown in [Figure 8-91](#) and described in [Table 8-91](#).

ADC Result 10 Register

Figure 8-91. ADCRESULT10 Register

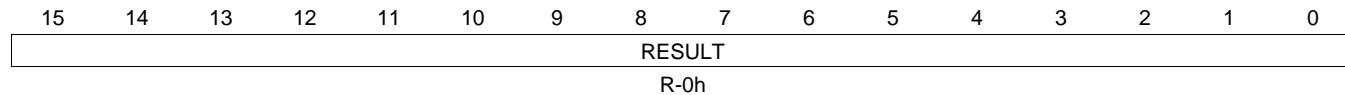
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-91. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

8.4.3.12 ADCRESULT11 Register (offset = B_h) [reset = 0h]ADCRESULT11 is shown in [Figure 8-92](#) and described in [Table 8-92](#).

ADC Result 11 Register

Figure 8-92. ADCRESULT11 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

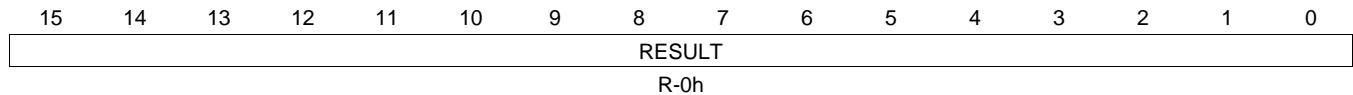
Table 8-92. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

8.4.3.13 ADCRESULT12 Register (offset = Ch) [reset = 0h]

ADCRESULT12 is shown in [Figure 8-93](#) and described in [Table 8-93](#).

ADC Result 12 Register

Figure 8-93. ADCRESULT12 Register

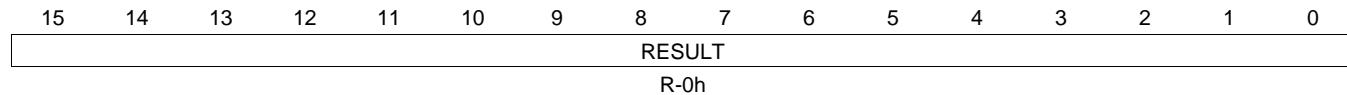
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-93. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

8.4.3.14 ADCRESULT13 Register (offset = Dh) [reset = 0h]ADCRESULT13 is shown in [Figure 8-94](#) and described in [Table 8-94](#).

ADC Result 13 Register

Figure 8-94. ADCRESULT13 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

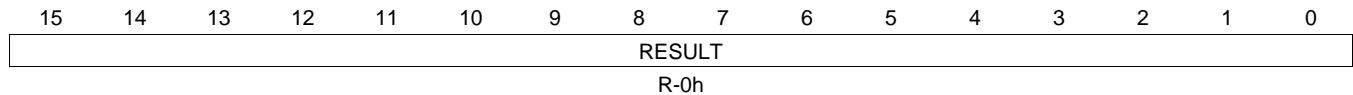
Table 8-94. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

8.4.3.15 ADCRESULT14 Register (offset = Eh) [reset = 0h]

ADCRESULT14 is shown in [Figure 8-95](#) and described in [Table 8-95](#).

ADC Result 14 Register

Figure 8-95. ADCRESULT14 Register

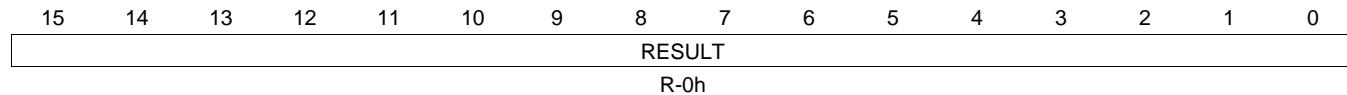
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-95. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

8.4.3.16 ADCRESULT15 Register (offset = Fh) [reset = 0h]ADCRESULT15 is shown in [Figure 8-96](#) and described in [Table 8-96](#).

ADC Result 15 Register

Figure 8-96. ADCRESULT15 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-96. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result. 16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

8.4.3.17 ADCPPB1RESULT Register (offset = 10h) [reset = 0h]

ADCPPB1RESULT is shown in [Figure 8-97](#) and described in [Table 8-97](#).

ADC Post Processing Block 1 Result Register

Figure 8-97. ADCPPB1RESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																PPBRESULT															

R-0h

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-97. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 13, and reflect the same value as bit 12.
15-0	PPBRESULT	R	0h	ADC Post Processing Block Result. The result of the offset/reference subtraction post conversion processing is stored in this register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

8.4.3.18 ADCPPB2RESULT Register (offset = 12h) [reset = 0h]

ADCPPB2RESULT is shown in [Figure 8-98](#) and described in [Table 8-98](#).

ADC Post Processing Block 2 Result Register

Figure 8-98. ADCPPB2RESULT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-98. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 13, and reflect the same value as bit 12.
15-0	PPBRESULT	R	0h	ADC Post Processing Block Result. The result of the offset/reference subtraction post conversion processing is stored in this register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

8.4.3.19 ADCPPB3RESULT Register (offset = 14h) [reset = 0h]

ADCPPB3RESULT is shown in [Figure 8-99](#) and described in [Table 8-99](#).

ADC Post Processing Block 3 Result Register

Figure 8-99. ADCPPB3RESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																PPBRESULT															

R-0h

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-99. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 13, and reflect the same value as bit 12.
15-0	PPBRESULT	R	0h	ADC Post Processing Block Result. The result of the offset/reference subtraction post conversion processing is stored in this register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

8.4.3.20 ADCPPB4RESULT Register (offset = 16h) [reset = 0h]

ADCPPB4RESULT is shown in [Figure 8-100](#) and described in [Table 8-100](#).

ADC Post Processing Block 4 Result Register

Figure 8-100. ADCPPB4RESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																PPBRESULT															

R-0h

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 8-100. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 13, and reflect the same value as bit 12.
15-0	PPBRESULT	R	0h	ADC Post Processing Block Result. The result of the offset/reference subtraction post conversion processing is stored in this register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

Buffered Digital to Analog Converter (DAC)

The buffered digital to analog converter (DAC) is an analog module that can output a programmable, arbitrary reference voltage.

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9.1 Buffered Digital to Analog Converter (DAC) Overview	1369
9.2 Using the DAC	1369
9.3 Lock Registers	1370
9.4 Registers	1370

9.1 Buffered Digital to Analog Converter (DAC) Overview

The buffered DAC module consists of an internal reference DAC and an analog output buffer that is capable of driving an external load. An integrated pull-down resistor on the DAC output helps to provide a known pin voltage when the output buffer is disabled. This pull-down resistor cannot be disabled and remains as a passive component on the pin, even for other shared pinmux functions. Software writes to the DAC value register can take effect immediately or can be synchronized with PWMSYNC events.

9.1.1 Features

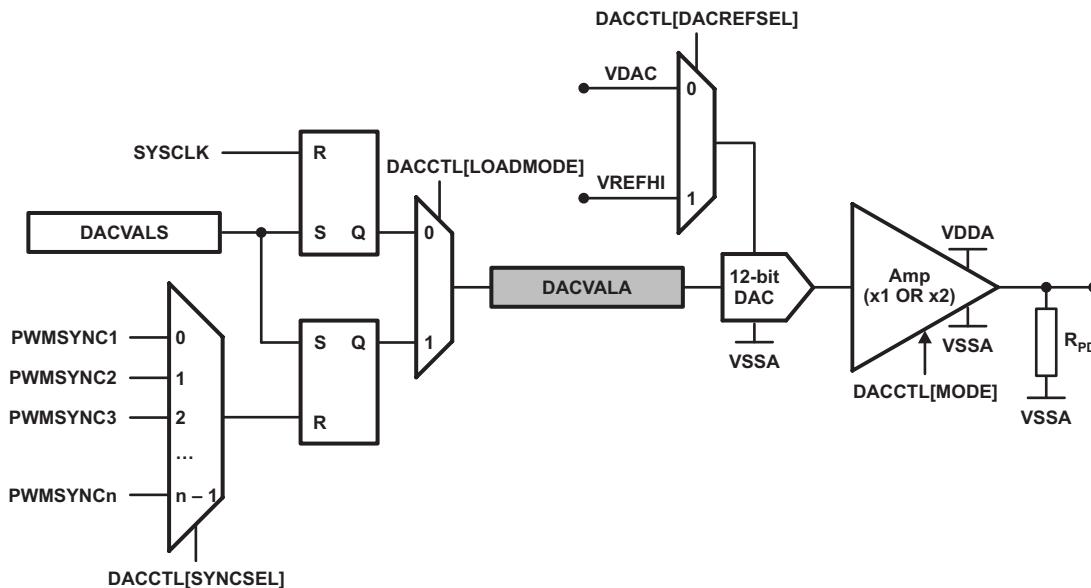
Each buffered DAC has the following features:

- 12-bit programmable internal DAC
- Selectable reference voltage
- Analog output buffer with programmable gain setting (Gain=1 or Gain=2)
- Pull-down resistor on output
- Ability to synchronize with PWMSYNC

9.1.2 Block Diagram

The block diagram for the buffered DAC is shown in [Figure 9-1](#).

Figure 9-1. DAC Module Block Diagram



9.2 Using the DAC

The reference voltages for the internal DAC are selectable between the two voltage pairs:

- VDAC and VSSA
- VREFHI and VSSA

Two sets of DACVAL registers are present in the buffered DAC module: DACVALA and DACVALS. DACVALA is a read-only register that actively controls the DAC value. DACVALS is a writable shadow register that loads into DACVALA either immediately or synchronized with the next PWMSYNC event.

The ideal output of the internal DAC can be calculated as follows:

$$V_{DAC} = \frac{DACVALA * DACREF}{4096}$$

The Buffered DAC output buffer may exhibit non-linear behavior near the supply rails (VDDA/VSSA). See the device datasheet to determine the valid operating range of the Buffered DAC.

9.3 Lock Registers

A DACLOCK register is provided to prevent spurious writes from modifying the DACCTL, DACVALS, and DACOUTEN registers. Once a register is protected through DACLOCK, write access will be locked out until the device is reset.

9.4 Registers

9.4.1 DAC Base Addresses

Table 9-1. DAC Base Address Table

Device Registers	Register Name	Start Address	End Address
DacaRegs	DAC_REGS	0x0000_5C00	0x0000_5C0F
DacbRegs	DAC_REGS	0x0000_5C10	0x0000_5C1F
DaccRegs	DAC_REGS	0x0000_5C20	0x0000_5C2F

9.4.2 DAC_REGS Registers

Table 9-2 lists the memory-mapped registers for the DAC_REGS. All register offset addresses not listed in Table 9-2 should be considered as reserved locations and the register contents should not be modified.

Table 9-2. DAC_REGS REGISTERS

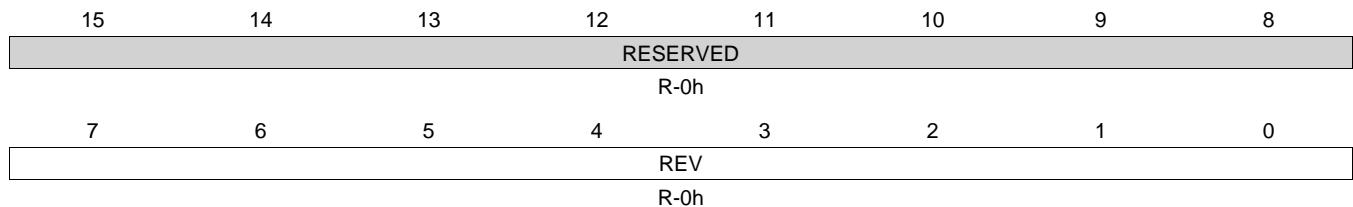
Offset	Acronym	Register Name	Section	Write Protection
0h	DACREV	DAC Revision Register	Section 9.4.2.1	
1h	DACCTL	DAC Control Register	Section 9.4.2.2	EALLOW
2h	DACVALA	DAC Value Register - Active	Section 9.4.2.3	
3h	DACVALS	DAC Value Register - Shadow	Section 9.4.2.4	
4h	DACOUTEN	DAC Output Enable Register	Section 9.4.2.5	EALLOW
5h	DACLOCK	DAC Lock Register	Section 9.4.2.6	EALLOW

9.4.2.1 DACREV Register (offset = 0h) [reset = 0h]

DACREV is shown in [Figure 9-2](#) and described in [Table 9-3](#).

DAC Revision Register

Figure 9-2. DACREV Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

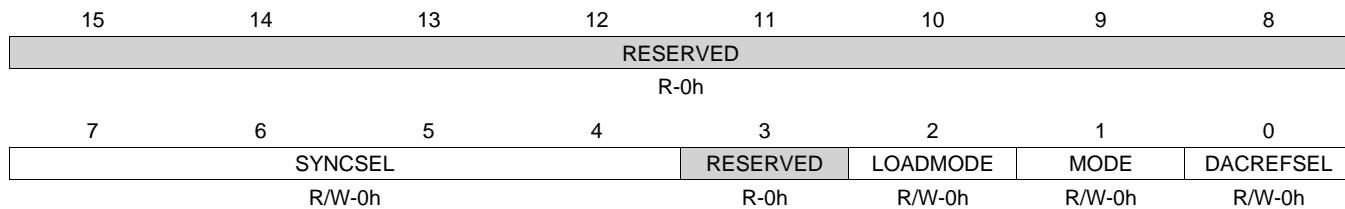
Table 9-3. DACREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	REV	R	0h	DAC Revision

9.4.2.2 DACCTL Register (offset = 1h) [reset = 0h]

DACCTL is shown in [Figure 9-3](#) and described in [Table 9-4](#).

DAC Control Register

Figure 9-3. DACCTL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 9-4. DACCTL Register Field Descriptions

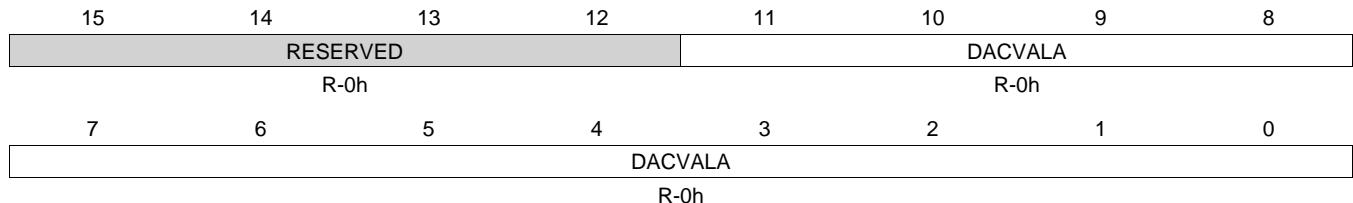
Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-4	SYNCSEL	R/W	0h	DAC PWMSYNC select. Determines which PWMSYNC signal will update the DACVALA register. 0 PWMSYNC1 1 PWMSYNC2 2 PWMSYNC3 ... n-1 PWMSYNCn
3	RESERVED	R	0h	Reserved
2	LOADMODE	R/W	0h	DACVALA load mode. Determines when the DACVALA register is updated with the value from DACVALS. 0 Load on next SYSCLK 1 Load on next PWMSYNC specified by SYNCSEL
1	MODE	R/W	0h	DAC gain mode select. Selects the gain mode for the buffered output. The MODE value is only used when DACREFSEL=1 and internal ADC reference mode is selected. 0 Gain is 1 1 Gain is 2
0	DACREFSEL	R/W	0h	DAC reference select. Selects which voltage references are used by the DAC. 0 VDAC/VSSA are the reference voltages 1 ADC VREFHI/VSSA are the reference voltages

9.4.2.3 DACVALA Register (offset = 2h) [reset = 0h]

DACVALA is shown in [Figure 9-4](#) and described in [Table 9-5](#).

DAC Value Register - Active

Figure 9-4. DACVALA Register



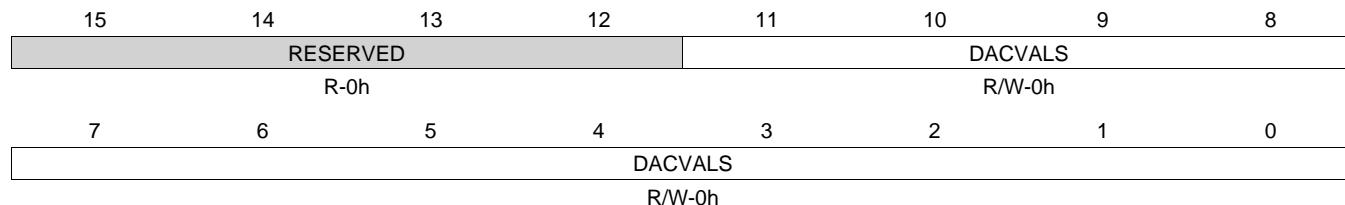
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 9-5. DACVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVALA	R	0h	Active output code currently driven by the DAC

9.4.2.4 DACVALS Register (offset = 3h) [reset = 0h]DACVALS is shown in [Figure 9-5](#) and described in [Table 9-6](#).

DAC Value Register - Shadow

Figure 9-5. DACVALS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

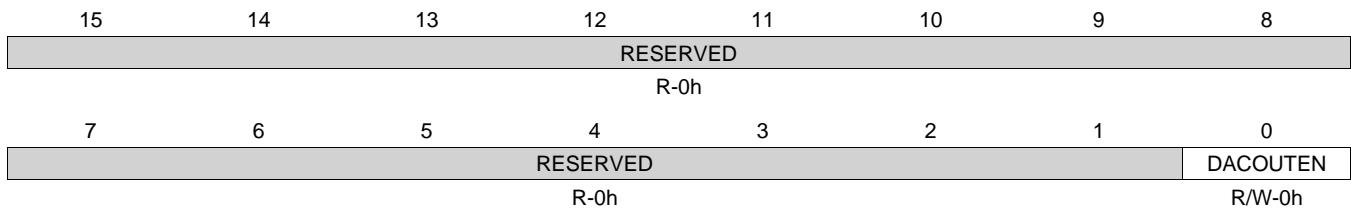
Table 9-6. DACVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVALS	R/W	0h	Shadow output code to be loaded into DACVALA

9.4.2.5 DACOUTEN Register (offset = 4h) [reset = 0h]

DACOUTEN is shown in [Figure 9-6](#) and described in [Table 9-7](#).

DAC Output Enable Register

Figure 9-6. DACOUTEN Register

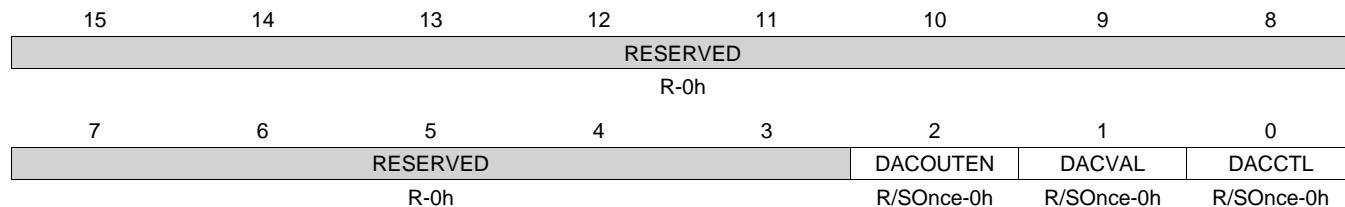
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 9-7. DACOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	DACOUTEN	R/W	0h	DAC output enable 0 DAC output is disabled 1 DAC output is enabled

9.4.2.6 DACLOCK Register (offset = 5h) [reset = 0h]DACLOCK is shown in [Figure 9-7](#) and described in [Table 9-8](#).

DAC Lock Register

Figure 9-7. DACLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 9-8. DACLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2	DACOUTEN	R/SOnce	0h	Lock write-access to the DACOUTEN register. 0 DACOUTEN register is not locked. Write 0 to this bit has no effect. 1 DACOUTEN register is locked. Only a system reset can clear this bit.
1	DACVAL	R/SOnce	0h	Lock write-access to the DACVALS register. 0 DACVALS register is not locked. Write 0 to this bit has no effect. 1 DACVALS register is locked. Only a system reset can clear this bit.
0	DACCTL	R/SOnce	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.

Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting components that are combined into a topology that is useful for power applications such as peak current mode control, switched-mode power, power factor correction, and voltage trip monitoring.

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10.1 CMPSS Overview	1379
10.2 Comparator	1380
10.3 Internal DAC	1380
10.4 Ramp Generator	1380
10.5 Digital Filter	1381
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10.1 CMPSS Overview

The Comparator Subsystem is built around a pair of analog comparators. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is always driven from an external pin, but the negative input can be driven by either an external pin or by an internal programmable 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. A ramp generator circuit is optionally available to control the internal DAC value for one comparator in the subsystem.

10.1.1 Features

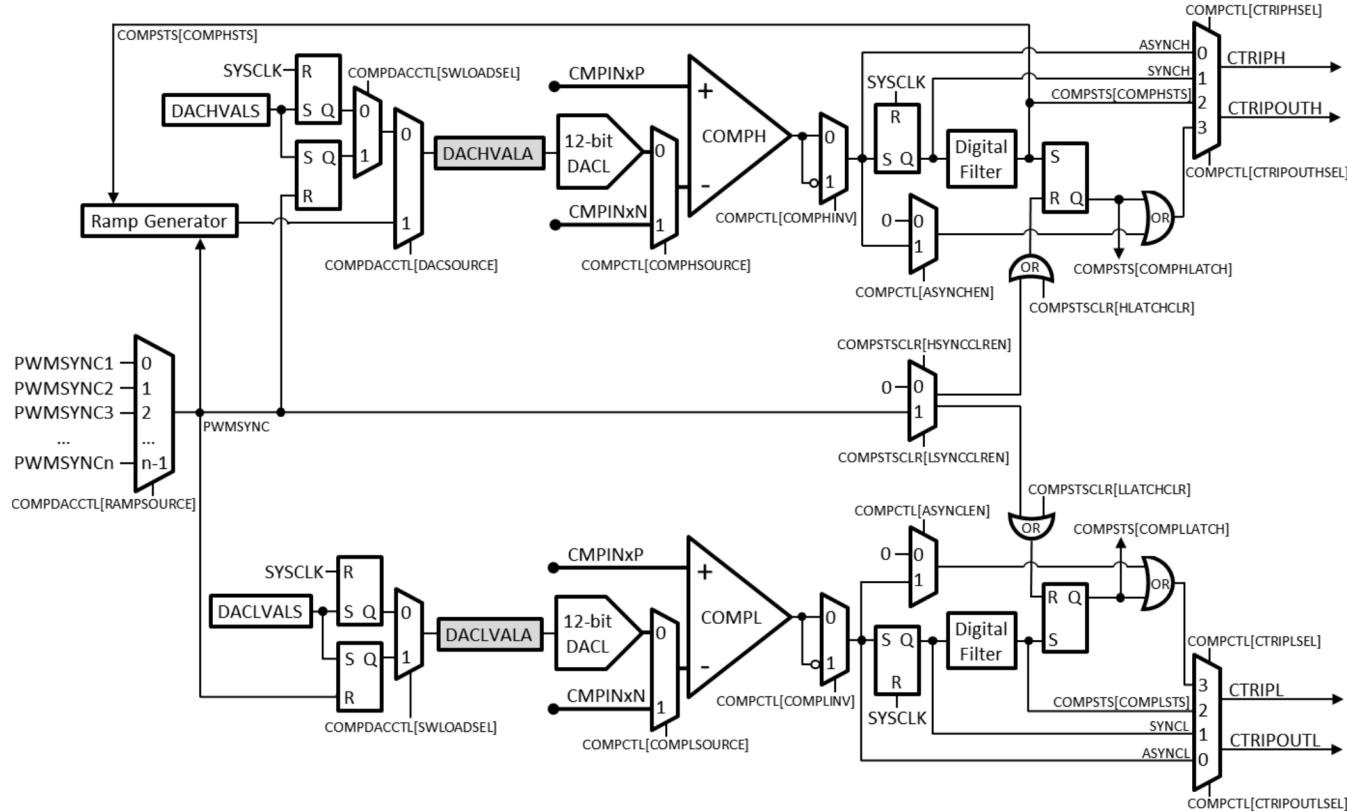
CMPSS Features

- Each CMPSS module includes:
 - Two analog comparators
 - Two programmable 12-bit DACs
 - One ramp generator
 - Two digital filters
- Ability to synchronize with PWMSYNC
- Negative input of comparator can be driven by an external signal or by an internal DAC
- Option to choose between VDDA or VDAC to be the DAC reference voltage

10.1.2 Block Diagram

The block diagram for the CMPSS is shown in [Figure 10-1](#).

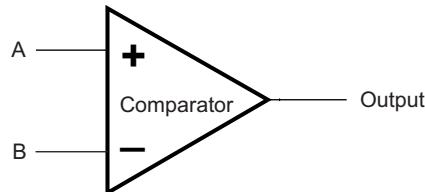
Figure 10-1. CMPSS Module Block Diagram



10.2 Comparator

The comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input.

Figure 10-2. Comparator Digital Output



Voltages	Output
Voltage A > Voltage B	1
Voltage B < Voltage A	0

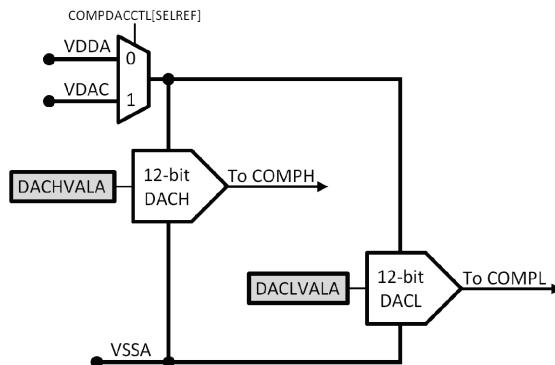
10.3 Internal DAC

Each 12-bit internal DAC can be configured to drive the reference voltage into the negative input of its respective comparator. The DAC output is internal only and cannot be observed externally.

Two sets of DACxVAL registers are present for each DAC: DACxVALA and DACxVALS. DACxVALA is a read-only register that actively controls the DAC value. DACxVALS is a writable shadow register that loads into DACxVALA either immediately or synchronized with the next PWMSYNC event. The high DAC can optionally source its DACHVALA value from the Ramp Generator instead of DACVALS.

The operating range of the DACs is bound by its high and low reference voltages. The high voltage reference is VDDA by default, but it can be configured to be VDAC instead.

Figure 10-3. DAC Reference Select



The ideal output voltage of the DACs can be calculated as follows:

Figure 10-4. Output Voltage Calculation

$$V_{DACx} = \frac{DACxVALA * DACREF}{4096}$$

10.4 Ramp Generator

When selected, the ramp generator produces a falling-ramp DAC reference output signal. In this mode, the DAC uses the most significant 12 bits of the RAMPSTS countdown register as its input.

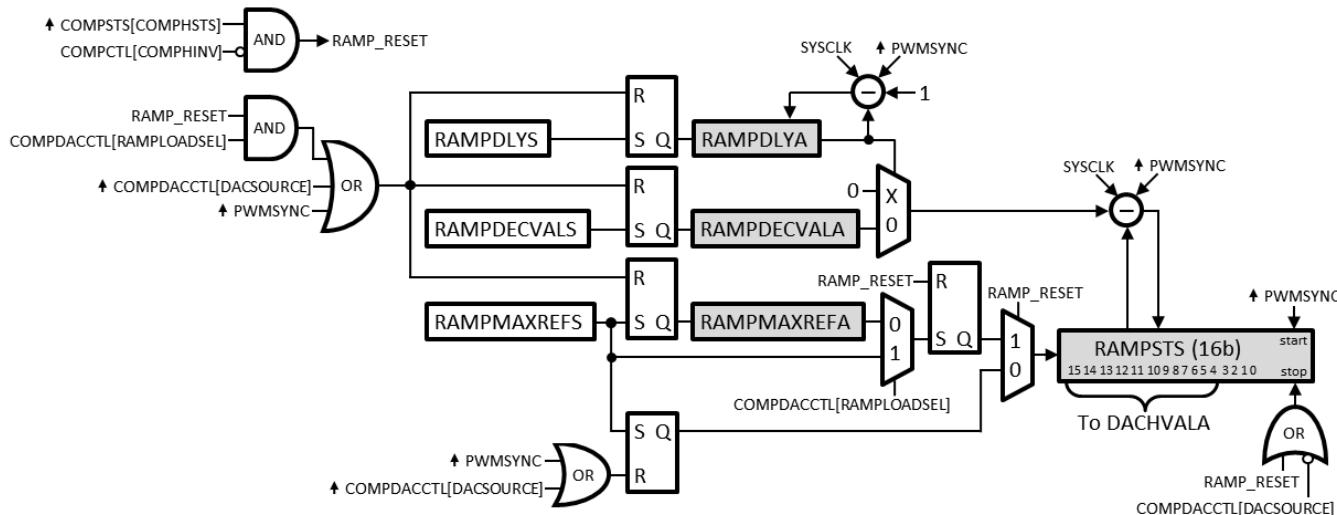
The RAMPSTS register is loaded from RAMPMAXREFS when the selected PWMSYNC signal is received. After the PWMSYNC event, the value of RAMPDECVLA is subtracted from RAMPSTS on every SYSCLK cycle thereafter.

The RAMPDLYA register serves as a delay counter to hold off the RAMPSTS subtraction. When a PWMSYNC signal is received, the value of RAMPDLYA is decremented by one for every SYSCLK cycle until the register reaches zero. RAMPSTS subtraction will only begin when RAMPDLYA is zero.

When the ramp generator is first enabled by setting DACSOURCE = 1, the value of RAMPSTS is loaded from RAMPMAXREFS, and the register remains static until the first PWMSYNC signal is received.

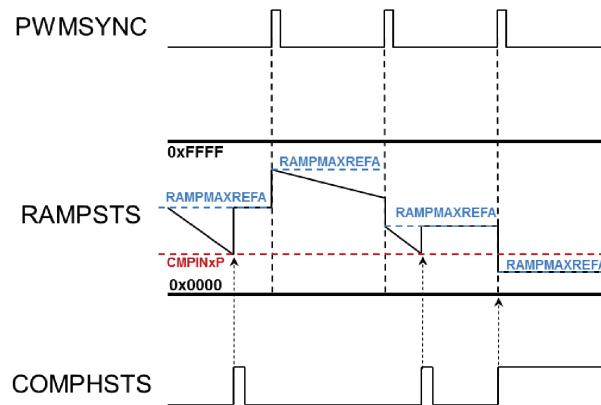
If the COMPHSTS bit is set by the comparator while the ramp generator is active, the RAMPSTS register will reset to the value of RAMPMAXREFS and remain static until the next PWMSYNC signal is received. If the value of RAMPSTS reaches zero, the RAMPSTS register will remain static at zero until the next PWMSYNC is received. The ramp generator is illustrated in [Figure 10-5](#).

Figure 10-5. Ramp Generator



The ramp generator behavior is further illustrated in [Figure 10-6](#).

Figure 10-6. Ramp Generator Behavior



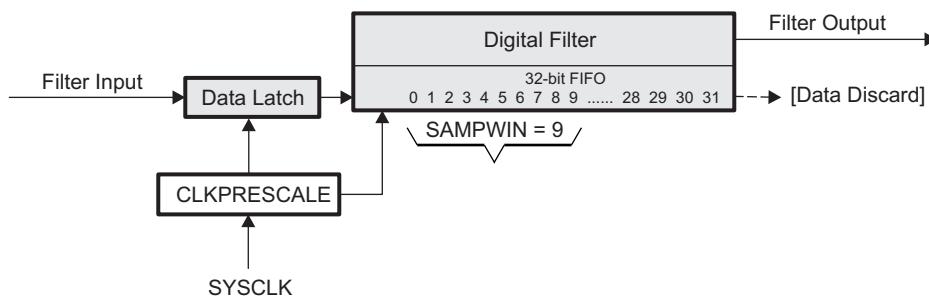
10.5 Digital Filter

The digital filter works on a window of FIFO samples (SAMPWIN + 1) taken from the input. The filter output resolves to the majority value of the sample window, where majority is defined by the threshold (THRESH) value. If the majority threshold is not satisfied, the filter output remains unchanged.

For proper operation, the value of THRESH must be greater than SAMPWIN / 2.

A prescale function (CLKPRESSCALE) determines the filter sampling rate, where the filter FIFO captures one sample every CLKPRESSCALE system clocks. Old data from the FIFO is discarded.

A conceptual model of the digital filter is shown in [Figure 10-7](#).

Figure 10-7. Digital Filter Behavior

```

if (FILTER_OUTPUT == 0) {
    if (Num_1s_in_SAMPWIN >= THRESH) {
        FILTER_OUTPUT = 1;
    }
}
else {
    if (Num_0s_in_SAMPWIN >= THRESH) {
        FILTER_OUTPUT = 0;
    }
}

```

To ensure proper operation of the digital filter, the following initialization sequence is recommended:

1. Configure and enable the comparator for operation
2. Configure the digital filter parameters for operation
 - Set SAMPWIN for the number of samples to monitor in FIFO window
 - Set THRESH for the threshold required for majority qualification
 - Set CLKPRESCALE for the digital filter clock prescale value
3. Initialize the sample values in the digital FIFO window by setting FILINIT
4. Configure the CTRIP and CTRIPOUT signal paths
5. If desired, configure the EPWM and GPIO modules to accept the filtered signals

10.6 Registers

10.6.1 CMPSS Base Addresses

Table 10-1. CMPSS Base Address Table

Device Registers	Register Name	Start Address	End Address
Cmpss1Regs	CMPSS_REGS	0x0000_5C80	0x0000_5C9F
Cmpss2Regs	CMPSS_REGS	0x0000_5CA0	0x0000_5CBF
Cmpss3Regs	CMPSS_REGS	0x0000_5CC0	0x0000_5CDF
Cmpss4Regs	CMPSS_REGS	0x0000_5CE0	0x0000_5CF
Cmpss5Regs	CMPSS_REGS	0x0000_5D00	0x0000_5D1F
Cmpss6Regs	CMPSS_REGS	0x0000_5D20	0x0000_5D3F
Cmpss7Regs	CMPSS_REGS	0x0000_5D40	0x0000_5D5F
Cmpss8Regs	CMPSS_REGS	0x0000_5D60	0x0000_5D7F

10.6.2 CMPSS_REGS Registers

Table 10-2 lists the memory-mapped registers for the CMPSS_REGS. All register offset addresses not listed in **Table 10-2** should be considered as reserved locations and the register contents should not be modified.

Table 10-2. CMPSS_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	COMPCTL	CMPSS Comparator Control Register	Section 10.6.2.1	EALLOW
1h	COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	Section 10.6.2.2	EALLOW
2h	COMPSTS	CMPSS Comparator Status Register	Section 10.6.2.3	
3h	COMPSTSCLR	CMPSS Comparator Status Clear Register	Section 10.6.2.4	EALLOW
4h	COMPDACCTL	CMPSS DAC Control Register	Section 10.6.2.5	EALLOW
6h	DACHVALS	CMPSS High DAC Value Shadow Register	Section 10.6.2.6	
7h	DACHVALA	CMPSS High DAC Value Active Register	Section 10.6.2.7	
8h	RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	Section 10.6.2.8	
Ah	RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	Section 10.6.2.9	
Ch	RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	Section 10.6.2.10	
Eh	RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	Section 10.6.2.11	
10h	RAMPSTS	CMPSS Ramp Status Register	Section 10.6.2.12	
12h	DACLVALS	CMPSS Low DAC Value Shadow Register	Section 10.6.2.13	
13h	DACLVALA	CMPSS Low DAC Value Active Register	Section 10.6.2.14	
14h	RAMPDLYA	CMPSS Ramp Delay Active Register	Section 10.6.2.15	
15h	RAMPDLYS	CMPSS Ramp Delay Shadow Register	Section 10.6.2.16	
16h	CTRIPLFILCTL	CTRIPL Filter Control Register	Section 10.6.2.17	EALLOW
17h	CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	Section 10.6.2.18	EALLOW
18h	CTRIPHFILCTL	CTRIPH Filter Control Register	Section 10.6.2.19	EALLOW
19h	CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	Section 10.6.2.20	EALLOW
1Ah	COMPLOCK	CMPSS Lock Register	Section 10.6.2.21	EALLOW

10.6.2.1 COMPCTL Register (offset = 0h) [reset = 0h]

COMPCTL is shown in [Figure 10-8](#) and described in [Table 10-3](#).

CMPSS Comparator Control Register

Figure 10-8. COMPCTL Register

15	14	13	12	11	10	9	8
COMPDACE	ASYNCLEN	CTRIPOUTLSEL		CTRIPSEL		COMPLINV	COMPLSOURCE
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	ASYNCLEN	CTRIPOUTHSEL		CTRIPHSEL		COMPHINV	COMPHSOURCE
R-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-3. COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	R/W	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled
14	ASYNCLEN	R/W	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
13-12	CTRIPOUTLSEL	R/W	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL
11-10	CTRIPSEL	R/W	0h	Low comparator CTRIPSEL source select. 0 Asynchronous comparator output drives CTRIPSEL 1 Synchronous comparator output drives CTRIPSEL 2 Output of digital filter drives CTRIPSEL 3 Latched output of digital filter drives CTRIPSEL
9	COMPLINV	R/W	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
8	COMPLSOURCE	R/W	0h	Low comparator input source. 0 Inverting input of comparator driven by internal DAC 1 Inverting input of comparator driven through external pin
7	RESERVED	R	0h	Reserved
6	ASYNCLEN	R/W	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output

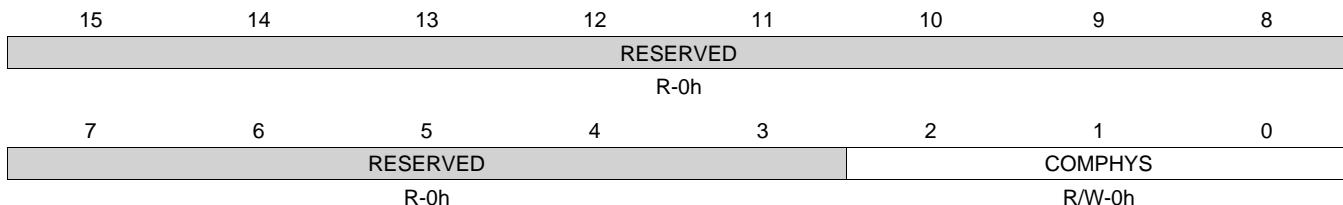
Table 10-3. COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	CTRIPOUTHSEL	R/W	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH
3-2	CTRIPHSEL	R/W	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH
1	COMPHINV	R/W	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
0	COMPHSOURCE	R/W	0h	High comparator input source. 0 Inverting input of comparator driven by internal DAC 1 Inverting input of comparator driven through external pin

10.6.2.2 COMPHYSCTL Register (offset = 1h) [reset = 0h]

COMPHYSCTL is shown in [Figure 10-9](#) and described in [Table 10-4](#).

CMPSS Comparator Hysteresis Control Register

Figure 10-9. COMPHYSCTL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-4. COMPHYSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2-0	COMPHYS	R/W	0h	Comparator hysteresis. Sets the amount of hysteresis on the comparator inputs. 0 None 1 Set to typical hysteresis 2 Set to 2x of typical hysteresis 3 Set to 3x of typical hysteresis 4 Set to 4x of typical hysteresis

10.6.2.3 COMPSTS Register (offset = 2h) [reset = 0h]

COMPSTS is shown in [Figure 10-10](#) and described in [Table 10-5](#).

CMPSS Comparator Status Register

Figure 10-10. COMPSTS Register

15	14	13	12	11	10	9	8
RESERVED						COMPLATCH	COMPLSTS
R-0h						R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED						COMPHLATCH	COMPHSTS
R-0h						R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-5. COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	COMPLATCH	R	0h	Latched value of low comparator digital filter output
8	COMPLSTS	R	0h	Low comparator digital filter output
7-2	RESERVED	R	0h	Reserved
1	COMPHLATCH	R	0h	Latched value of high comparator digital filter output
0	COMPHSTS	R	0h	High comparator digital filter output

10.6.2.4 COMPSTSCLR Register (offset = 3h) [reset = 0h]

COMPSTSCLR is shown in [Figure 10-11](#) and described in [Table 10-6](#).

CMPSS Comparator Status Clear Register

Figure 10-11. COMPSTSCLR Register

15	14	13	12	11	10	9	8
RESERVED			LSYNCCLREN			LLATCHCLR	RESERVED
R-0h			R/W-0h			R=0/W=1-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED			HSYNCCLREN			HLATCHCLR	RESERVED
R-0h			R/W-0h			R=0/W=1-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-6. COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	LSYNCCLREN	R/W	0h	Low comparator latch PWMSYNC clear. Enable PWMSYNC reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 PWMSYNC will not reset latch 1 PWMSYNC will reset latch
9	LLATCHCLR	R=0/W=1	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH]
8-3	RESERVED	R	0h	Reserved
2	HSYNCCLREN	R/W	0h	High comparator latch PWMSYNC clear. Enable PWMSYNC reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 PWMSYNC will not reset latch 1 PWMSYNC will reset latch
1	HLATCHCLR	R=0/W=1	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH]
0	RESERVED	R	0h	Reserved

10.6.2.5 COMPDACCTL Register (offset = 4h) [reset = 0h]

COMPDACCTL is shown in [Figure 10-12](#) and described in [Table 10-7](#).

CMPSS DAC Control Register

Figure 10-12. COMPDACCTL Register

15	14	13	12	11	10	9	8
FREESOFT	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
SWLOADSEL	RAMPLOADSEL	SELREF		RAMPSOURCE		DACSOURCE	
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

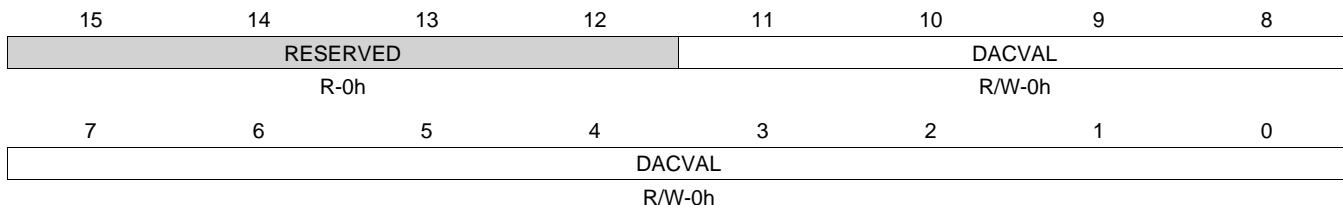
Table 10-7. COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREESOFT	R/W	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next PWMSYNC during emulation suspend 1Xb Ramp generator runs freely
13-8	RESERVED	R	0h	Reserved
7	SWLOADSEL	R/W	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or PWMSYNC. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on PWMSYNC
6	RAMPLOADSEL	R/W	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS
5	SELREF	R/W	0h	DAC reference select. Determines which voltage supply is used as the reference for the internal comparator DACs. 0 VDDA is the voltage reference for the DAC 1 VDAC is the voltage reference for the DAC
4-1	RAMPSOURCE	R/W	0h	Ramp generator source select. Determines which PWMSYNCx signal is used within the CMPSS module. 0 PWMSYNC1 1 PWMSYNC2 2 PWMSYNC3 ... n-1 PWMSYNCn
0	DACSOURCE	R/W	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator

10.6.2.6 DACHVALS Register (offset = 6h) [reset = 0h]

DACHVALS is shown in [Figure 10-13](#) and described in [Table 10-8](#).

CMPSS High DAC Value Shadow Register

Figure 10-13. DACHVALS Register

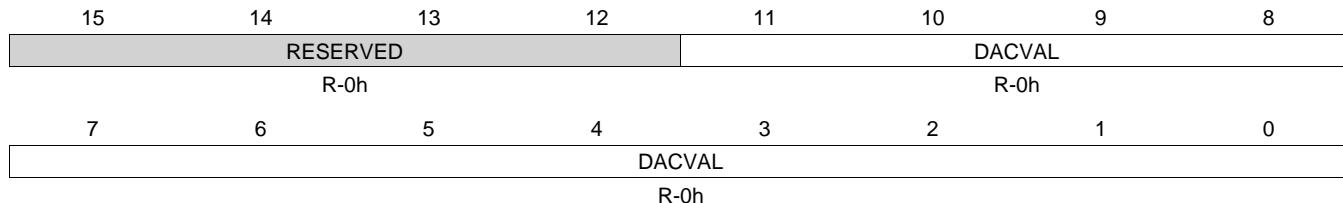
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-8. DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVAL	R/W	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

10.6.2.7 DACHVALA Register (offset = 7h) [reset = 0h]DACHVALA is shown in [Figure 10-14](#) and described in [Table 10-9](#).

CMPSS High DAC Value Active Register

Figure 10-14. DACHVALA Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

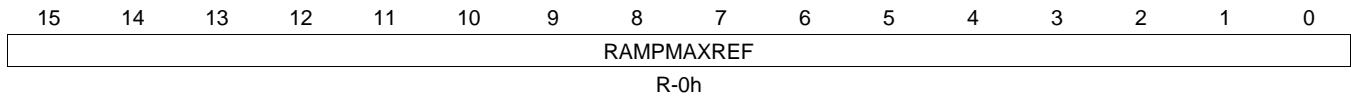
Table 10-9. DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVAL	R	0h	High DAC active value. Value that is actively driven by the high DAC.

10.6.2.8 RAMPMAXREFA Register (offset = 8h) [reset = 0h]

RAMPMAXREFA is shown in [Figure 10-15](#) and described in [Table 10-10](#).

CMPSS Ramp Max Reference Active Register

Figure 10-15. RAMPMAXREFA Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-10. RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RAMPMAXREF	R	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS.

10.6.2.9 RAMPMAXREFS Register (offset = Ah) [reset = 0h]RAMPMAXREFS is shown in [Figure 10-16](#) and described in [Table 10-11](#).

CMPSS Ramp Max Reference Shadow Register

Figure 10-16. RAMPMAXREFS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMPMAXREF															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

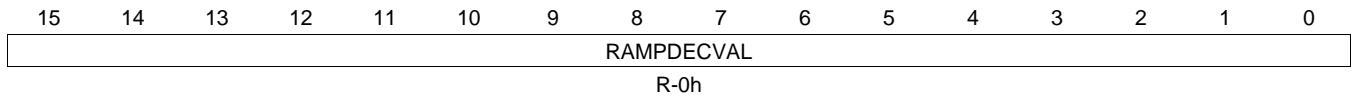
Table 10-11. RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RAMPMAXREF	R/W	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS.

10.6.2.10 RAMPDECVALA Register (offset = Ch) [reset = 0h]

RAMPDECVALA is shown in [Figure 10-17](#) and described in [Table 10-12](#).

CMPSS Ramp Decrement Value Active Register

Figure 10-17. RAMPDECVALA Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-12. RAMPDECVALA Register Field Descriptions

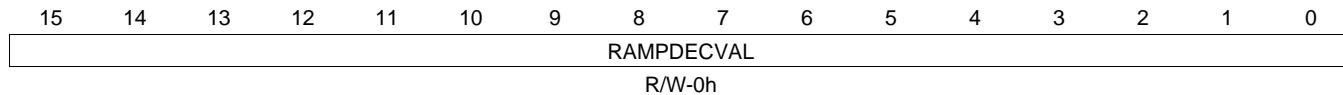
Bit	Field	Type	Reset	Description
15-0	RAMPDECVAL	R	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS.

10.6.2.11 RAMPDECVALS Register (offset = Eh) [reset = 0h]

RAMPDECVALS is shown in [Figure 10-18](#) and described in [Table 10-13](#).

CMPSS Ramp Decrement Value Shadow Register

Figure 10-18. RAMPDECVALS Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

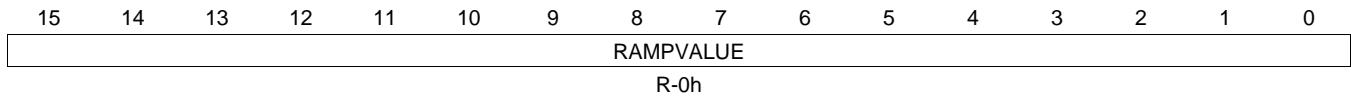
Table 10-13. RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RAMPDECVAL	R/W	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA.

10.6.2.12 RAMPSTS Register (offset = 10h) [reset = 0h]

RAMPSTS is shown in [Figure 10-19](#) and described in [Table 10-14](#).

CMPSS Ramp Status Register

Figure 10-19. RAMPSTS Register

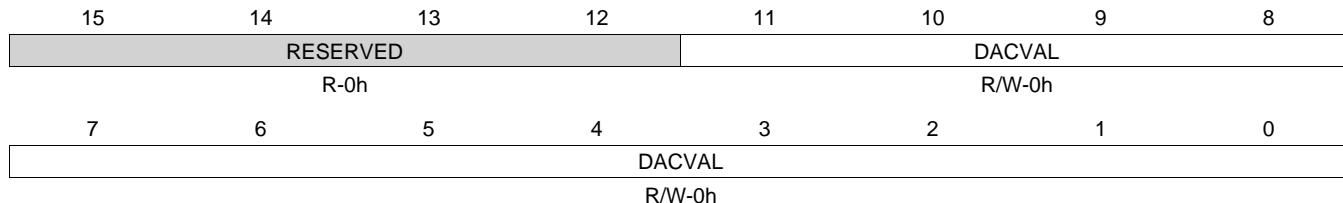
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-14. RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RAMPVALUE	R	0h	Ramp value. Present value of ramp generator.

10.6.2.13 DACLVALS Register (offset = 12h) [reset = 0h]DACLVALS is shown in [Figure 10-20](#) and described in [Table 10-15](#).

CMPSS Low DAC Value Shadow Register

Figure 10-20. DACLVALS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

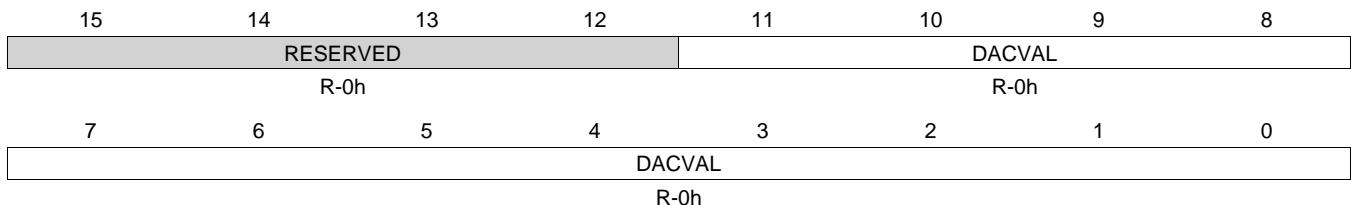
Table 10-15. DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVAL	R/W	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

10.6.2.14 DACLVALA Register (offset = 13h) [reset = 0h]

DACLVALA is shown in [Figure 10-21](#) and described in [Table 10-16](#).

CMPSS Low DAC Value Active Register

Figure 10-21. DACLVALA Register

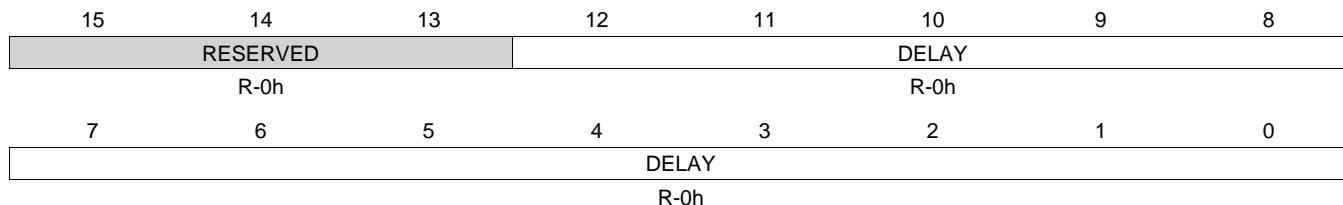
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-16. DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVAL	R	0h	Low DAC active value. Value that is actively driven by the low DAC.

10.6.2.15 RAMPDLYA Register (offset = 14h) [reset = 0h]RAMPDLYA is shown in [Figure 10-22](#) and described in [Table 10-17](#).

CMPSS Ramp Delay Active Register

Figure 10-22. RAMPDLYA Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-17. RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-0	DELAY	R	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a PWMSYNC is received.

10.6.2.16 RAMPDLYS Register (offset = 15h) [reset = 0h]

RAMPDLYS is shown in [Figure 10-23](#) and described in [Table 10-18](#).

CMPSS Ramp Delay Shadow Register

Figure 10-23. RAMPDLYS Register

15	14	13	12	11	10	9	8
RESERVED		DELAY					
R-0h							R/W-0h
7	6	5	4	3	2	1	0
DELAY							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-18. RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-0	DELAY	R/W	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA.

10.6.2.17 CTRIPLFILCTL Register (offset = 16h) [reset = 0h]

CTRIPLFILCTL is shown in [Figure 10-24](#) and described in [Table 10-19](#).

CTRIPL Filter Control Register

Figure 10-24. CTRIPLFILCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED			THRESH			SAMPWIN
R=0/W=1-0h	R-0h			R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
	SAMPWIN				RESERVED		R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-19. CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R=0/W=1	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8-4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3-0	RESERVED	R	0h	Reserved

10.6.2.18 CTRIPLFILCLKCTL Register (offset = 17h) [reset = 0h]

CTRIPLFILCLKCTL is shown in [Figure 10-25](#) and described in [Table 10-20](#).

CTRIPL Filter Clock Control Register

Figure 10-25. CTRIPLFILCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-20. CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples.

10.6.2.19 CTRIPHFILCTL Register (offset = 18h) [reset = 0h]

CTRIPHFILCTL is shown in [Figure 10-26](#) and described in [Table 10-21](#).

CTRIPH Filter Control Register

Figure 10-26. CTRIPHFILCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED			THRESH			SAMPWIN
R=0/W=1-0h	R-0h			R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
	SAMPWIN				RESERVED		R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-21. CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R=0/W=1	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8-4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3-0	RESERVED	R	0h	Reserved

10.6.2.20 CTRIPHFICLKCTL Register (offset = 19h) [reset = 0h]

CTRIPHFICLKCTL is shown in [Figure 10-27](#) and described in [Table 10-22](#).

CTRIPH Filter Clock Control Register

Figure 10-27. CTRIPHFICLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

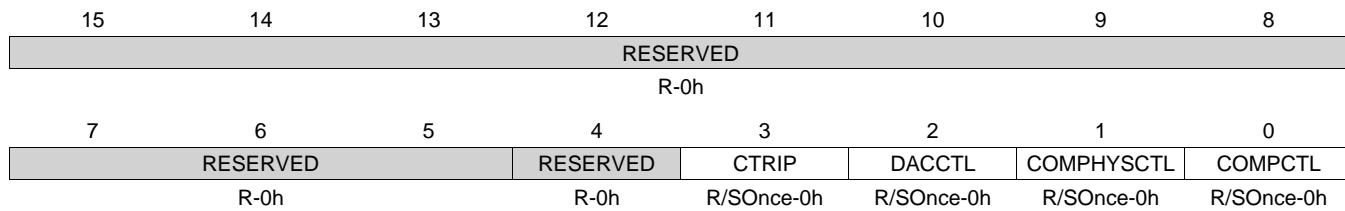
Table 10-22. CTRIPHFICLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples.

10.6.2.21 COMPLOCK Register (offset = 1Ah) [reset = 0h]

COMPLOCK is shown in [Figure 10-28](#) and described in [Table 10-23](#).

CMPSS Lock Register

Figure 10-28. COMPLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 10-23. COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	CTRIP	R/SOnce	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit.
2	DACCTL	R/SOnce	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.
1	COMPHYSCTL	R/SOnce	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit.
0	COMPCTL	R/SOnce	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit.

Sigma Delta Filter Module (SDFM)

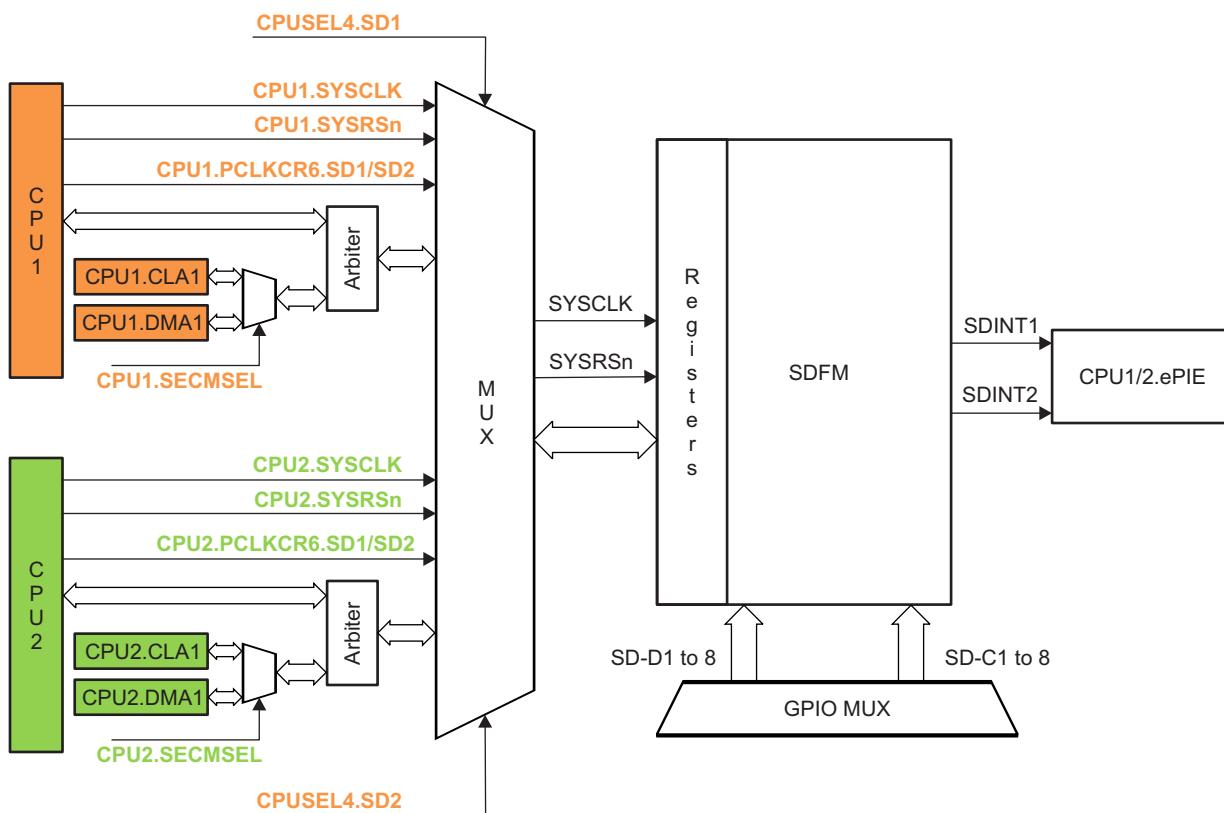
This chapter describes the sigma delta filter module (SDFM). SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent delta-sigma ($\Delta\Sigma$) modulator bit stream. The bit streams are processed by four individually-programmable digital decimation filters. The filter set includes a fast comparator for immediate digital threshold comparisons for over-current and under-current monitoring. The flexible SDFM also offers a filter-bypass mode to enable data logging, analysis, and customized filtering.

Topic	Page
11.1 SDFM Module Overview	1407
11.2 Input Control Unit	1409
11.3 Comparator Unit	1411
11.4 Data Filter Unit	1412
11.5 Interrupt Unit	1415
11.6 Register Descriptions	1417
11.7 Registers	1418

11.1 SDFM Module Overview

Figure 11-1 shows the SDFM CPU interfaces:

Figure 11-1. Sigma Delta Filter Module (SDFM) CPU Interface



11.1.1 SDFM Features

The SDFM features include:

- 8 external pins per SDFM module
 - 4 sigma delta data input pins per SDFM module (SD-Dx, where x = 1 to 4)
 - 4 sigma delta clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- 4 different configurable modulator clock modes:
 - Modulator clock rate equals modulator data rate
 - Modulator clock rate running at half the modulator data rate
 - Modulator data is Manchester encoded. Modulator clock not required.
 - Modulator clock rate is double that of modulator data rate
- 4 independent configurable comparator units:
 - 4 different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
 - Ability to detect over and under value conditions
 - OSR value for comparator programmable from 1 to 32
- 4 independent configurable sinc filter units:
 - 4 different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
 - Ability to bypass filter module
 - OSR value for filter unit programmable from 1 to 256
 - Ability to enable / disable individual filter module
 - Ability to synchronize all the 4 independent filters of a SDFM module using Master Filter Enable

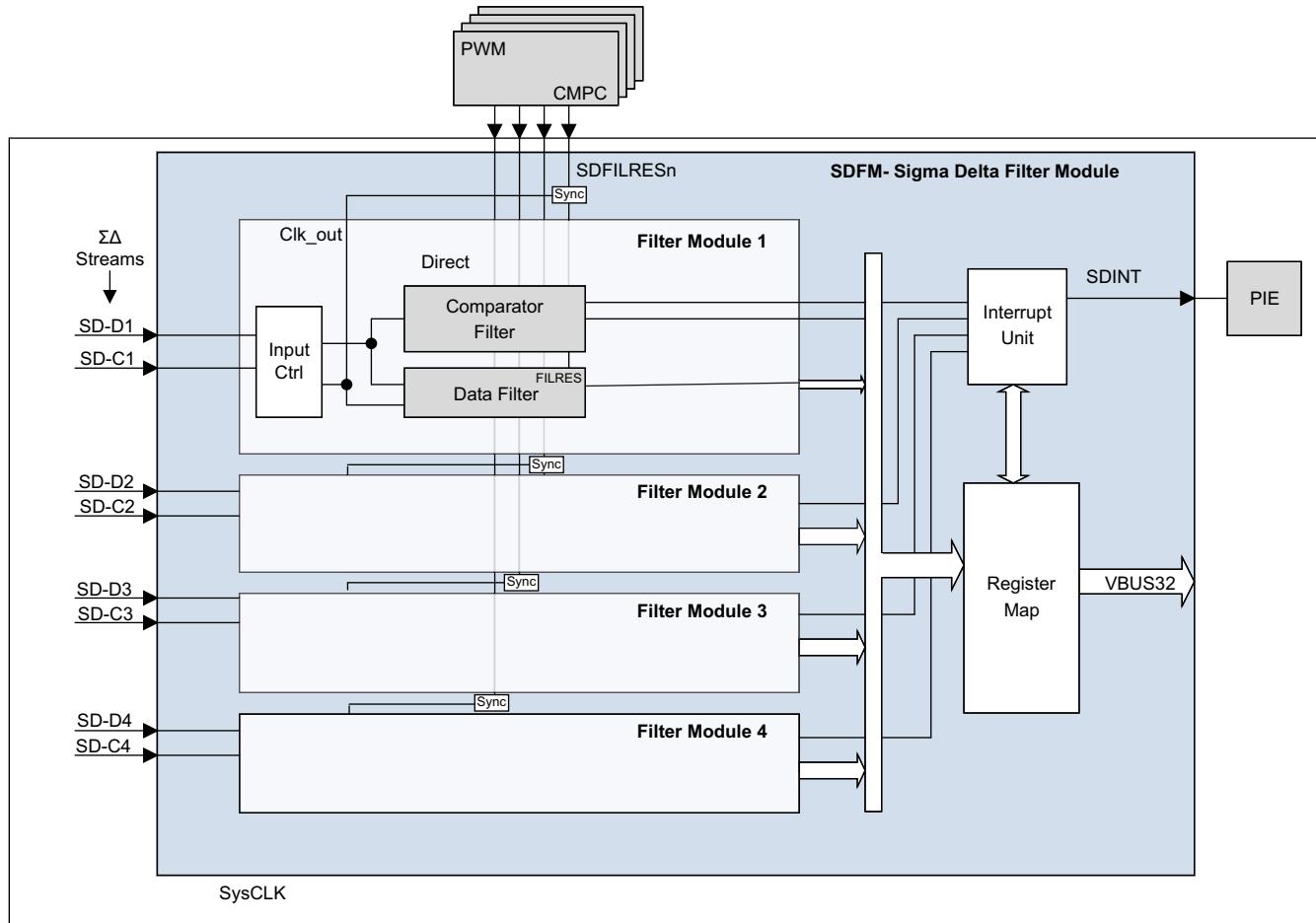
(MFE) bit (or) using PWM signals.

- Data filter output can be represented in either 16 bits (or) 32 bits
- PWMS can be used to generate a modulator clock for sigma delta modulators

11.1.2 Block Diagram

Figure 11-2 shows the SDFM module block diagram. The SDFM port operation is configured and controlled by the registers listed in Table 11-1.

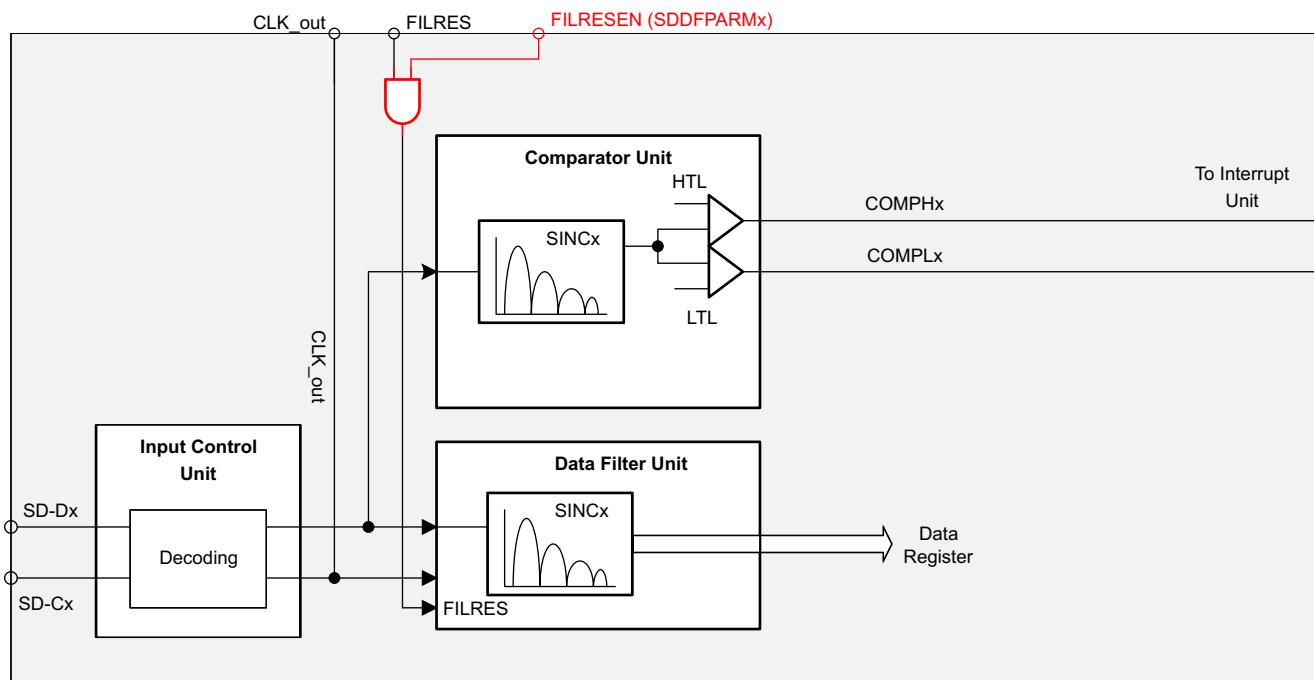
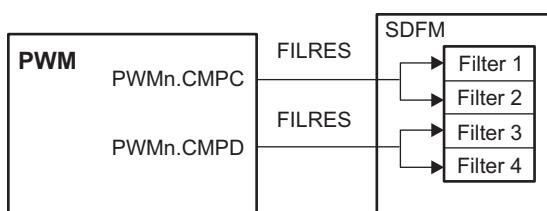
Figure 11-2. Sigma Delta Filter Module (SDFM) Block Diagram



Each SDFM module has four independent filter modules. These filter modules are identical and can be configured independently. Each individual filter module has the following units:

- Input Control unit
- Data filter unit
- Comparator unit

Figure 11-3 shows the block diagram of one filter module. When the SDDFPARMx.FILRESEN bit is set, the filter reset signal (FILRES) from the PWM module can be used to synchronize filters. It should be noted that the FILRES input is ONLY connected to the main Data Filter Unit and NOT the comparator, and that the reset function is limited to resetting the OSR counter. The FILRES input does not reset the data registers in the Filter Unit. Figure 11-4 shows how the PWM signals are connected to sigma delta module. In this device, PWM11 can be used to reset SDFM1 module and PWM12 can be used to reset SDFM2 module.

Figure 11-3. Block Diagram of One Filter Module**Figure 11-4. Typical PWM Interface to Sigma Delta Filter Module**

Note: When using PWM11 (or) PWM12 for SDFM filter synchronization, users MUST configure PWMs in up-count (or) down-count mode to ensure that only one CMPC (or) CMPD event will be generated per PWM timer period. Configuring PWM11 or 12 in up-down count mode when using CMPC or CMPD as a filter synchronizer will corrupt SDFM timing by providing two pulses per PWM timer period.

11.2 Input Control Unit

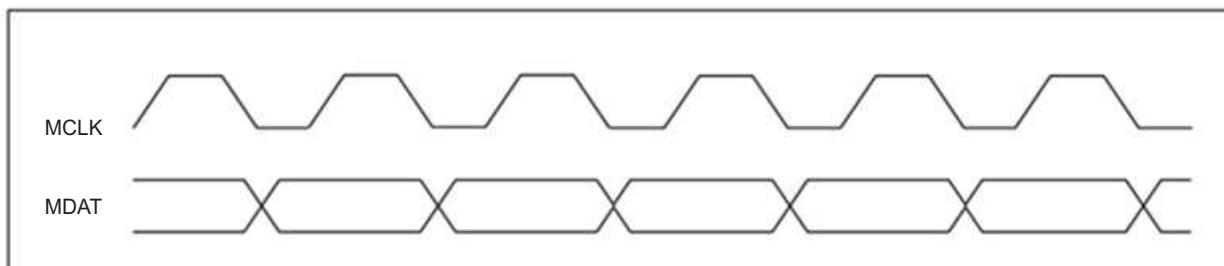
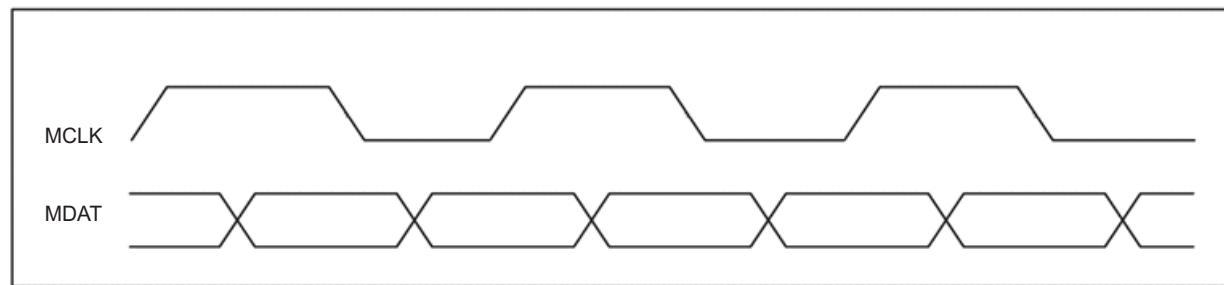
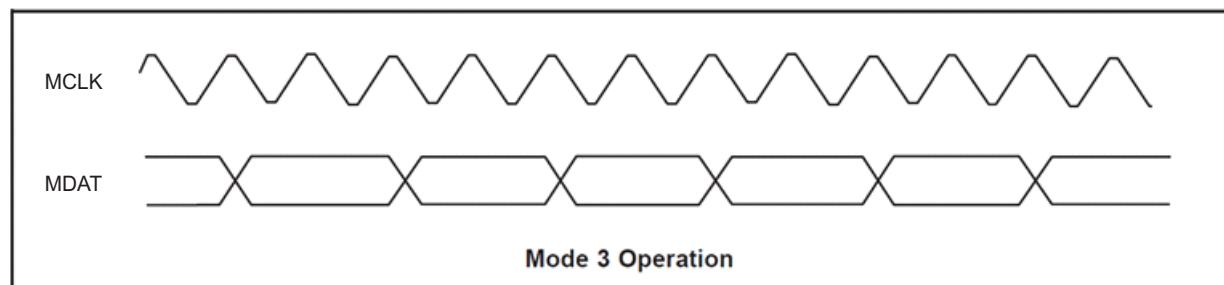
The input control unit receives sigma delta modulated data and sigma delta modulated clock. The modulated data received is captured and passed onto the data filter unit and comparator unit. This unit can be configured to receive the modulated data in four different modes. [Table 11-1](#) shows how SDCTLPARMx.MOD bits can be configured in these four different modes.

Table 11-1. Modulator Clock Modes

MODULATOR MODE [MOD]	DESCRIPTION
0	The modulator clock is running with the modulator data rate. The modulator data is strobed at every rising edge of the modulator clock.
1	The modulator clock is running with half of the modulator data rate. The modulator data is strobed at every edge of the modulator clock.
2	The modulator clock is off and the modulator data is Manchester-encoded.

Table 11-1. Modulator Clock Modes (continued)

MODULATOR MODE [MOD]	DESCRIPTION
3	The modulator clock is running with double of the modulator data rate. The modulator data is strobed at every other positive modulator clock edge.

**Mode 0 Operation****Mode 1 Operation****Mode 3 Operation**

When MOD=2, data and modulated clock signal are encoded into modulated data as shown in [Figure 11-5](#). In this mode, clock input SDCLKx.pin should be left floating. Input control unit performs continuous automatic calibration to achieve optimum decoding performance. The status of this calibration can be checked in the SDCTLPARMn Register bits MS[10:0] and in the SDSTATUS Register bits Manchester Locked (MALn) and Manchester Fail (MAFn).

11.2.1 Manchester Decoding

Manchester signaling is a method of encoding a data signal in such a way that it can be retrieved without the need of a separate clock line. When configured in Mode 2, the SDFM can translate a Manchester-encoded signal on SD-Dx into a clock signal and a data signal. An automatic calibration is continuously performed to optimize the decoding of the data.

The calibration mechanism follows this sequence:

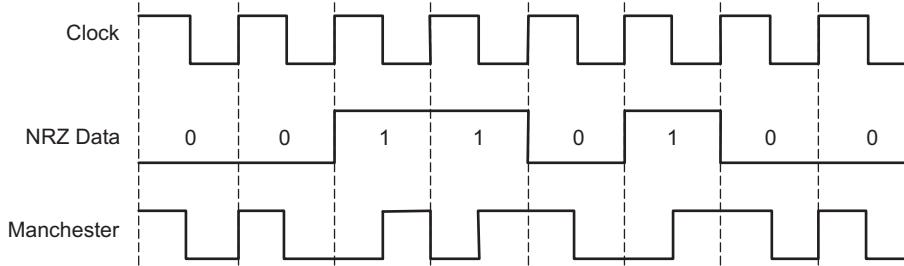
1. The modulator data is sampled at the frequency of the system clock (SYSCLK). The number of CLK cycles between transitions is counted and recorded for 1024 consecutive transitions.
2. The resulting array will have a '1' in the bit location that corresponds to the number of SYSCLK cycles counted between transitions. For example, the sequence shown in [Table 11-2](#) means that there was at least one instance where three and four, as well as seven and eight, CLK cycles occurred between two transitions. This array is stored in the bits MS10–MS0 in the SDCTLPARMn Control Parameter register.
3. An algorithm looks for a group of zeros that has ones before and after it. If this pattern is not found, the bits MALx and MAFx in the SDSTATUS Register are set high.
4. If the algorithm is successful, it will use the location of the first '0' as the number of SYSCLK cycles needed to determine the frequency and which transitions are valid in the Manchester code.
5. The algorithm starts over from Step 2 automatically.

Table 11-2. Example Control Parameter Register

Value	0	0	0	1	1	0	0	1	1	0	0
Bit	MS10	MS9	MS8	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0
CLK Cycles	11	10	9	8	7	6	5	4	3	2	1

Note: Bit refers to MS[] bits, not absolute SDCTLPARMn[] bit locations.

Figure 11-5. Manchester Coding Scheme



The MALx bit shows the status of the previous Manchester decoder calibration cycle. If it is high, the decoder calibration has failed on the previous calibration cycle. The MAFx bit shows if any failures have occurred since the last read of the SDSTATUS Register. Any MALx failure will cause MAFx to go high. MAFx is reset to low when the SDStatus Register is read.

The decoding procedure is performed continuously when the SDFM is configured for Modulator Mode 2 (Manchester encoded data). Note that the SYSCLK frequency must be at least six times the Manchester data rate for the decoder to perform properly.

11.3 Comparator Unit

An independent comparator unit allows the user to monitor input conditions with a fast settling time without sacrificing input measurement resolution. The comparator filter is a configurable sinc filter which supports the following filter types:- Sinc1, Sinc2, Sinc3 and Sincfast filter. Comparator filter OSR (COSR) value can be configured from 1 to 32. With Sinc3 as filter type and OSR = 32, a maximum 15-bit output width of 32,768 can be achieved. The output of the filter is compared with two programmed threshold levels to

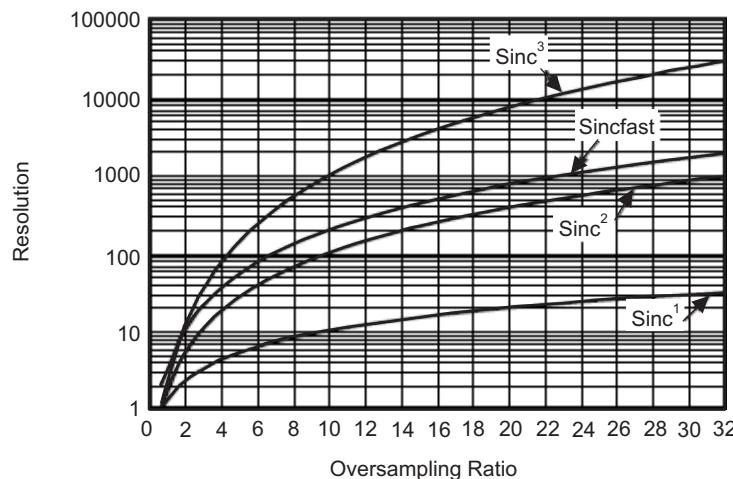
detect over- and under-value conditions. But output of the comparator filter cannot be read out of the filter. The comparator unit can be configured by high- and low-level Threshold registers (SDCMPHx and SDCMPLx) for each individual filter module. When an over- or under-value condition occurs, appropriate bits in SDIFLG (Interrupt Flag) register are set and then this register can be polled to see which condition caused interrupt signal.

The comparator filter unit and the data filter unit differ in the way they handle input data. The comparator filter unit translates a low input signal to a '0' and a high input signal to a '1', whereas the data filter unit uses '-1' and '1'. The resulting calculations give only positive values for the output of the comparator filter. The data representation is straight binary. [Table 11-3](#) and [Figure 11-6](#) show the different full-scale values that the comparator filter can store using different oversampling ratios.

Table 11-3. Peak Data Values for Different OSR/Filter Combinations

OSR	Sinc1	Sinc2	Sinc3	Sincfast
x	0 to x	0 to x2	0 to x3	0 to 2x2
4	0 to 4	0 to 16	0 to 64	0 to 32
8	0 to 8	0 to 64	0 to 512	0 to 128
16	0 to 16	0 to 256	0 to 4096	0 to 512
32	0 to 32	0 to 1024	0 to 32,768	0 to 2048

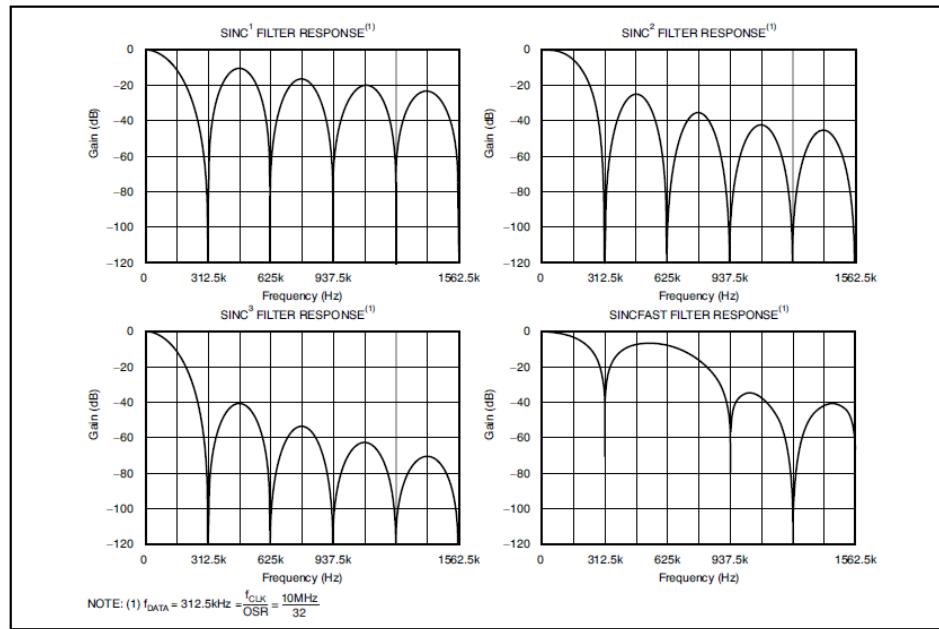
Figure 11-6. Comparator Filter Resolution



In order to achieve the maximum value, the delta-sigma modulator is operated at absolute maximum positive or negative full-scale, which is outside of the recommended full-scale range of 80% of most delta-sigma modulators.

11.4 Data Filter Unit

The data filter is a configurable sinc filter which supports the following filter types:- Sinc1, Sinc2, Sinc3 and Sincfast filter. Data filter OSR (DOSR) value can be configured from 1 to 256. [Figure 11-7](#) illustrates the frequency response of each type of filter when DOSR = 32 and modulator rate = 10 Mhz.

Figure 11-7. Frequency Response of Various Sinc Filters


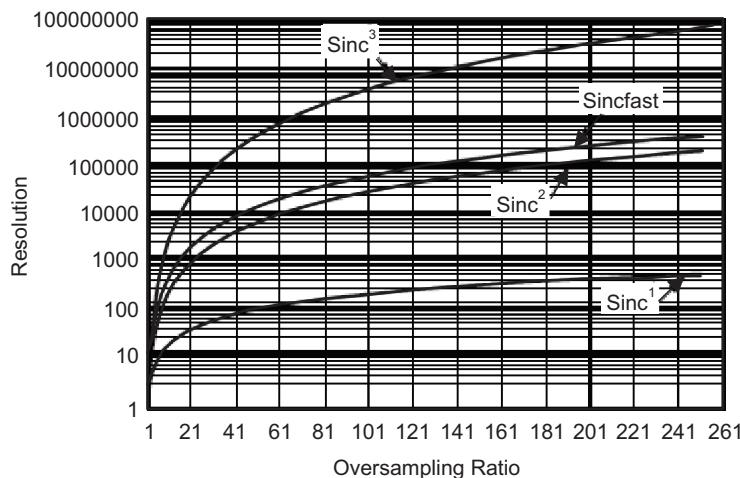
The data filter's data rate is controlled by modulator data rate and DOSR which can be configured in the Data Filter Parameter Register, SDDFPARMx.DOSR. The data filter data rate can be calculated by the formulae shown in [Equation 1](#).

$$\text{Data (filter unit data rate)} = \frac{\text{Modulator data rate}}{\text{DOSR}} \quad (1)$$

The user can achieve higher resolution by increasing the Data Filter Over Sampling Ratio (DOSR) but this would reduce the data rate of the data filter. [Table 11-4](#) shows the peak data for different filter type / DOSR combinations and [Figure 11-8](#) shows the relationship between DOSR and filter resolution. The highest resolution for any given DOSR can be achieved by using Sinc3 filter and the highest possible resolution can be achieved with DOSR = 256 and Sinc3 filter.

Table 11-4. Peak Data Values for Different DOSR/Filter Combinations

DOSR	Sinc1	Sinc2	Sinc3	Sincfast
x	x	x^2	x^3	$2x^2$
4	-4 to 4	-16 to 16	-64 to 64	-32 to 32
8	-8 to 8	-64 to 64	-512 to 512	-128 to 128
16	-16 to 16	-256 to 256	-4096 to 4096	-512 to 512
32	-32 to 32	-1024 to 1024	-32,768 to 32,768	-2048 to 2048
64	-64 to 64	-4096 to 4096	-262,144 to 262,144	-8192 to 8192
128	-128 to 128	-16,384 to 16,384	-2,097,152 to 2,097,152	-32,768 to 32,768
256	-256 to 256	-65,536 to 65,536	-16,777,216 to 16,777,215	-131,072 to 131,072

Figure 11-8. Data Filter Resolution

The data filter uses 25 bits to represent signed integer in two's complement format. The maximum possible resolution gives a 25-bit word (-16,777,216 to +16,777,215). Note that this value is only reached if the delta-sigma modulator is operated at absolute maximum positive or negative full-scale, which is beyond the recommended full-scale range of 80% of most delta-sigma modulators. This value also does not represent the resolution of the signal. The signal resolution is determined by the modulator, and increasing the filter bit width will not offer any improved noise performance beyond the modulator capabilities.

11.5 Interrupt Unit

Figure 11-9 shows the structure of the interrupt unit. Each SDFM module can generate a CPU interrupt. A SDFM interrupt can be triggered by any of these 16 interrupts sources:

- Four comparator low (IELx)

This interrupt source can be enabled when master interrupt (SDCTL.MIE = 1) and the appropriate individual filter interrupt are enabled (SDCPARMx.IEL = 1). When the input data stream is equal to (or) goes below lower threshold appropriate IFLx flag bit is set in Interrupt Flag Register (SDIFLG). Low-level Threshold Register (SDCMPLx.LLT) can be used to set appropriate lower threshold value. This flag will be reset if the Interrupt Register cleared (by setting the corresponding bit in the SDIFLGCLR register) and the interrupt source is no longer active.

- Four comparator high (IEHx)

This interrupt source can be enabled when master interrupt (SDCTL.MIE = 1) and the appropriate individual filter interrupt are enabled (SDCPARMx.IEH = 1). When the input data stream is equal to (or) goes above higher threshold appropriate IFHx flag bit is set in Interrupt Flag Register (SDIFLG). High-level Threshold Register (SDCMPHx.HLT) can be used to set appropriate higher threshold value. This flag will be reset if the Interrupt Register cleared (by setting the corresponding bit in the SDIFLGCLR register) and the interrupt source is no longer active.

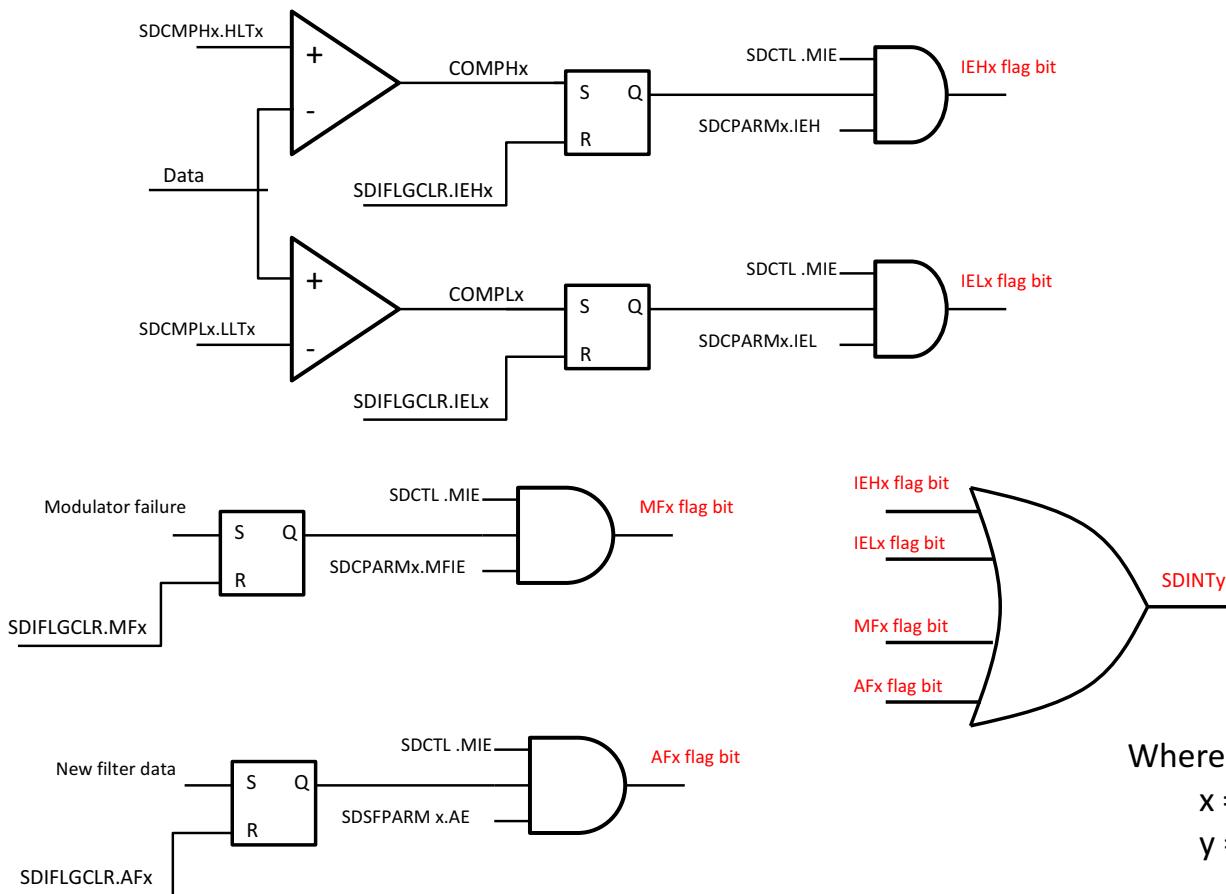
- Four modulator failure (MFx)

This interrupt source can be enabled when master interrupt (SDCTL.MIE = 1) and the appropriate individual filter interrupt are enabled (SDCPARMx.MFIE = 1). When modulator clock (SD-Cx) fails (or) goes missing appropriate MFx flag bit is set in Interrupt Flag Register (SDIFLG). This flag will be reset if the Interrupt Register cleared (by setting the corresponding bit in the SDIFLGCLR register) and the interrupt source is no longer active. If the modulator clock is failing (when the modulator clock is slower than 1/64th of the system clock SYSCLK), appropriate MFx flag bit is set, if the appropriate modulator flag interrupt enable bit (MFIEx) and the master interrupt enable (MIE) is set.

- Four filter data acknowledge (AFx)

This interrupt source can be enabled when master interrupt (SDCTL.MIE = 1) and the appropriate individual filter interrupts are enabled (SDDFPARMx.AE = 1). When the data filter generates a new data appropriate AFx flag bit is set in Interrupt Flag Register (SDIFLG). This flag will be reset if the Interrupt Register cleared (by setting the corresponding bit in the SDIFLGCLR register) and the interrupt source is no longer active. The acknowledge flags cannot be set if the data filter is disabled. Each acknowledge flag can be disabled if the Acknowledge Enable control bit (AE) in the appropriate Data Filter Parameter Register SDDFPARMx is set to low.

Figure 11-9. SDFM Interrupt Unit



Where,

 $x = 1 \text{ to } 4$ $y = 1 \text{ (or) } 2$

11.6 Register Descriptions

The register descriptions are shown in the following table and subsections.

Table 11-5. General Registers

Name	SDFM1 address	SDFM2 address	Size (x16)	Description	EALLOW?
SDIFLG	0x5E00	0x5E80	2	Interrupt Flag Register	
SDIFLGCCLR	0x5E02	0x5E82	2	Interrupt Flag Clear Register	
SDCTL	0x5E04	0x5E84	1	SD Control Register	YES
SDMFILEN	0x5E06	0x5E86	1	SD Master Filter Enable	YES
SDSTATUS	0x5E07	0x5E87	1	SD Status Register	YES

Table 11-6. Filter 1 Registers

Name	SDFM1 address	SDFM2 address	Size (x16)	Description	EALLOW?
SDCTLPARM1	0x5E10	0x5E90	1	Control Parameter Register for Ch1	YES
SDDFPARM1	0x5E11	0x5E91	1	Data Filter Parameter Register for Ch1	YES
SDIPARM1	0x5E12	0x5E92	1	Integer Parameter Register for Ch1	YES
SDCMPPH1	0x5E13	0x5E93	1	High-level Threshold Register for Ch1	YES
SDCMPL1	0x5E14	0x5E94	1	Low-level Threshold Register for Ch1	YES
SDCPARM1	0x5E15	0x5E95	1	Comparator Parameter Register for Ch1	YES
SDDATA1	0x5E16	0x5E96	2	Filter Data Register (16- or 32-bit) for Ch1	

Table 11-7. Filter 2 Registers

Name	SDFM1 address	SDFM2 address	Size (x16)	Description	EALLOW?
SDCTLPARM2	0x5E20	0x5EA0	1	Control Parameter Register for Ch2	YES
SDDFPARM2	0x5E21	0x5EA1	1	Data Filter Parameter Register for Ch2	YES
SDIPARM2	0x5E22	0x5EA2	1	Integer Parameter Register for Ch2	YES
SDCMPPH2	0x5E23	0x5EA3	1	High-level Threshold Register for Ch2	YES
SDCMPL2	0x5E24	0x5EA4	1	Low-level Threshold Register for Ch2	YES
SDCPARM2	0x5E25	0x5EA5	1	Comparator Parameter Register for Ch2	YES
SDDATA2	0x5E26	0x5EA6	2	Filter Data Register (16- or 32-bit) for Ch2	

Table 11-8. Filter 3 Registers

Name	SDFM1 address	SDFM2 address	Size (x16)	Description	EALLOW?
SDCTLPARM3	0x5E30	0x5EB0	1	Control Parameter Register for Ch3	YES
SDDFPARM3	0x5E31	0x5EB1	1	Data Filter Parameter Register for Ch3	YES
SDIPARM3	0x5E32	0x5EB2	1	Integer Parameter Register for Ch3	YES
SDCMPH3	0x5E33	0x5EB3	1	High-level Threshold Register for Ch3	YES
SDCMPL3	0x5E34	0x5EB4	1	Low-level Threshold Register for Ch3	YES
SDCPARM3	0x5E35	0x5EB5	1	Comparator Parameter Register for Ch3	YES
SDDATA3	0x5E36	0x5EB6	2	Filter Data Register (16- or 32-bit) for Ch3	

Table 11-9. Filter 4 Registers

Name	SDFM1 address	SDFM2 address	Size (x16)	Description	EALLOW?
SDCTLPARM4	0x5E40	0x5EC0	1	Control Parameter Register for Ch4	YES
SDDFPARM4	0x5E41	0x5EC1	1	Data Filter Parameter Register for Ch4	YES
SDIPARM4	0x5E42	0x5EC2	1	Integer Parameter Register for Ch4	YES
SDCMPH4	0x5E43	0x5EC3	1	High-level Threshold Register for Ch4	YES
SDCMPL4	0x5E44	0x5EC4	1	Low-level Threshold Register for Ch4	YES
SDCPARM4	0x5E45	0x5EC5	1	Comparator Parameter Register for Ch4	YES
SDDATA4	0x5E46	0x5EC6	2	Filter Data Register (16- or 32-bit) for Ch4	

11.7 Registers

11.7.1 SDFM Base Addresses

Table 11-10. SDFM Base Address Table

Device Registers	Register Name	Start Address	End Address
Sdfm1Regs	SDFM_REGS	0x0000_5E00	0x0000_5E7F
Sdfm2Regs	SDFM_REGS	0x0000_5E80	0x0000_5EFF

11.7.2 SDFM_REGS Registers

Table 11-11 lists the memory-mapped registers for the SDFM_REGS. All register offset addresses not listed in **Table 11-11** should be considered as reserved locations and the register contents should not be modified.

Table 11-11. SDFM_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	SDIFLG	Interrupt Flag Register	Section 11.7.2.1	
2h	SDIFLGCLR	Interrupt Flag Clear Register	Section 11.7.2.2	
4h	SDCTL	SD Control Register	Section 11.7.2.3	EALLOW
6h	SDMFILEN	SD Master Filter Enable	Section 11.7.2.4	EALLOW
7h	SDSTATUS	SD Status Register	Section 11.7.2.5	EALLOW
10h	SDCTLPARM1	Control Parameter Register for Ch1	Section 11.7.2.6	EALLOW
11h	SDDFPARM1	Data Filter Parameter Register for Ch1	Section 11.7.2.7	EALLOW
12h	SDIPARM1	Integer Parameter Register for Ch1	Section 11.7.2.8	EALLOW
13h	SDCMPH1	High-level Threshold Register for Ch1	Section 11.7.2.9	EALLOW
14h	SDCMPL1	Low-level Threshold Register for Ch1	Section 11.7.2.10	EALLOW
15h	SDCPARM1	Comparator Parameter Register for Ch1	Section 11.7.2.11	EALLOW
16h	SDDATA1	Filter Data Register (16 or 32bit) for Ch1	Section 11.7.2.12	
20h	SDCTLPARM2	Control Parameter Register for Ch2	Section 11.7.2.13	EALLOW
21h	SDDFPARM2	Data Filter Parameter Register for Ch2	Section 11.7.2.14	EALLOW
22h	SDIPARM2	Integer Parameter Register for Ch2	Section 11.7.2.15	EALLOW
23h	SDCMPH2	High-level Threshold Register for Ch2	Section 11.7.2.16	EALLOW
24h	SDCMPL2	Low-level Threshold Register for Ch2	Section 11.7.2.17	EALLOW
25h	SDCPARM2	Comparator Parameter Register for Ch2	Section 11.7.2.18	EALLOW
26h	SDDATA2	Filter Data Register (16 or 32bit) for Ch2	Section 11.7.2.19	
30h	SDCTLPARM3	Control Parameter Register for Ch3	Section 11.7.2.20	EALLOW
31h	SDDFPARM3	Data Filter Parameter Register for Ch3	Section 11.7.2.21	EALLOW
32h	SDIPARM3	Integer Parameter Register for Ch3	Section 11.7.2.22	EALLOW
33h	SDCMPH3	High-level Threshold Register for Ch3	Section 11.7.2.23	EALLOW
34h	SDCMPL3	Low-level Threshold Register for Ch3	Section 11.7.2.24	EALLOW
35h	SDCPARM3	Comparator Parameter Register for Ch3	Section 11.7.2.25	EALLOW
36h	SDDATA3	Filter Data Register (16 or 32bit) for Ch3	Section 11.7.2.26	
40h	SDCTLPARM4	Control Parameter Register for Ch4	Section 11.7.2.27	EALLOW
41h	SDDFPARM4	Data Filter Parameter Register for Ch4	Section 11.7.2.28	EALLOW
42h	SDIPARM4	Integer Parameter Register for Ch4	Section 11.7.2.29	EALLOW

Table 11-11. SDFM_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
43h	SDCMPH4	High-level Threshold Register for Ch4	Section 11.7.2.30	EALLOW
44h	SDCMPL4	Low-level Threshold Register for Ch4	Section 11.7.2.31	EALLOW
45h	SDCPARM4	Comparator Parameter Register for Ch4	Section 11.7.2.32	EALLOW
46h	SDDATA4	Filter Data Register (16 or 32bit) for Ch4	Section 11.7.2.33	

11.7.2.1 SDIFLG Register (offset = 0h) [reset = 0h]

SDIFLG is shown in [Figure 11-10](#) and described in [Table 11-12](#).

Interrupt Flag Register

Figure 11-10. SDIFLG Register

31	30	29	28	27	26	25	24
MIF	RESERVED						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							R-0h
15	14	13	12	11	10	9	8
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
IFL4	IFH4	IFL3	IFH3	IFL2	IFH2	IFL1	IFH1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-12. SDIFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	R	0h	Set whenever any interrupt (ACK1-4, MF1-4, IFL1-4, IFH1-4) is active
30-16	RESERVED	R	0h	Reserved
15	AF4	R	0h	0: No new data available from Filter 4 1: New data available from Filter 4
14	AF3	R	0h	0: No new data available from Filter 3 1: New data available from Filter 3
13	AF2	R	0h	0: No new data available from Filter 2 1: New data available from Filter 2
12	AF1	R	0h	0: No new data available from Filter 1 1: New data available from Filter 1
11	MF4	R	0h	0: Modulator is operating normally for Filter 4 1: Modulator failure for Filter 4
10	MF3	R	0h	0: Modulator is operating normally for Filter 3 1: Modulator failure for Filter 3
9	MF2	R	0h	0: Modulator is operating normally for Filter 2 1: Modulator failure for Filter 2
8	MF1	R	0h	0: Modulator is operating normally for Filter 1 1: Modulator failure for Filter 1
7	IFL4	R	0h	0: Comparator Filter 4 output is above the low limit threshold 1: Comparator Filter 4 output is equal to or below the low level threshold, if enabled
6	IFH4	R	0h	0: Comparator Filter 4 output is below the high limit threshold 1: Comparator Filter 4 output is equal to or above the high level threshold, if enabled
5	IFL3	R	0h	0: Comparator Filter 3 output is above the low limit threshold 1: Comparator Filter 3 output is equal to or below the low level threshold, if enabled

Table 11-12. SDIFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IFH3	R	0h	0: Comparator Filter 3 output is below the high limit threshold 1: Comparator Filter 3 output is equal to or above the high level threshold, if enabled
3	IFL2	R	0h	0: Comparator Filter 2 output is above the low limit threshold 1: Comparator Filter 2 output is equal to or below the low level threshold, if enabled
2	IFH2	R	0h	0: Comparator Filter 2 output is below the high limit threshold 1: Comparator Filter 2 output is equal to or above the high level threshold, if enabled
1	IFL1	R	0h	0: Comparator Filter 1 output is above the low limit threshold 1: Comparator Filter 1 output is equal to or below the low level threshold, if enabled
0	IFH1	R	0h	0: Comparator Filter 1 output is below the high limit threshold 1: Comparator Filter 1 output is equal to or above the high level threshold, if enabled

11.7.2.2 SDIFLGCLR Register (offset = 2h) [reset = 0h]

SDIFLGCLR is shown in [Figure 11-11](#) and described in [Table 11-13](#).

Interrupt Flag Clear Register

Figure 11-11. SDIFLGCLR Register

31	30	29	28	27	26	25	24
MIF	RESERVED						
R=0/W=1-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							R-0h
15	14	13	12	11	10	9	8
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1
R=0/W=1-0h							
7	6	5	4	3	2	1	0
IFL4	IFH4	IFL3	IFH3	IFL2	IFH2	IFL1	IFH1
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-13. SDIFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	R=0/W=1	0h	Flag-clear bit for SDFM Master Interrupt flag. Write 1 to clear MIF. Writes of "0" are ignored. Note: If the MIF flag is cleared and other Interrupts are still pending, MIF will again be set to 1 on the following SysClk cycle, and the INT output will be reasserted (pulsed low)
30-16	RESERVED	R	0h	Reserved
15	AF4	R=0/W=1	0h	SD Module Interrupt Flag Clear Bits: Writing a "1" will clear the respective flag bit in the SDINTFLG register. Writes of "0" are ignored. Note: If user writes a "1" to clear a bit on the same cycle that the hardware is trying to set the bit to "1", then hardware has priority and the bit will not be cleared. Flag-clear bit for Acknowledge flag for Filter 4
14	AF3	R=0/W=1	0h	Flag-clear bit for Acknowledge flag for Filter 3
13	AF2	R=0/W=1	0h	Flag-clear bit for Acknowledge flag for Filter 2
12	AF1	R=0/W=1	0h	Flag-clear bit for Acknowledge flag for Filter 1
11	MF4	R=0/W=1	0h	Flag-clear bit for Modulator Failure for Filter 4
10	MF3	R=0/W=1	0h	Flag-clear bit for Modulator Failure for Filter 3
9	MF2	R=0/W=1	0h	Flag-clear bit for Modulator Failure for Filter 2
8	MF1	R=0/W=1	0h	Flag-clear bit for Modulator Failure for Filter 1
7	IFL4	R=0/W=1	0h	Flag-clear bit for Low-Level Interrupt flag Filter 4
6	IFH4	R=0/W=1	0h	Flag-clear bit for High-level Interrupt flag Filter 4
5	IFL3	R=0/W=1	0h	Flag-clear bit for Low-Level Interrupt flag Filter 3
4	IFH3	R=0/W=1	0h	Flag-clear bit for High-level Interrupt flag Filter 3
3	IFL2	R=0/W=1	0h	Flag-clear bit for Low-Level Interrupt flag Filter 2
2	IFH2	R=0/W=1	0h	Flag-clear bit for High-level Interrupt flag Filter 2
1	IFL1	R=0/W=1	0h	Flag-clear bit for Low-Level Interrupt flag Filter 1

Table 11-13. SDIFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IFH1	R=0/W=1	0h	Flag-clear bit for High-level Interrupt flag Filter 1

11.7.2.3 SDCTL Register (offset = 4h) [reset = 0h]

SDCTL is shown in [Figure 11-12](#) and described in [Table 11-14](#).

SD Control Register

Figure 11-12. SDCTL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	MIE			RESERVED		
R-0h	R-0h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-14. SDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	MIE	R/W	0h	Master interrupt enable. 0: Interrupt pin and interrupt flags are blocked (interrupt pin INT always inactive). 1: Interrupt pin and interrupt flags are not blocked and can be set and reset (if individually enabled).
12-0	RESERVED	R	0h	Reserved

11.7.2.4 SDMFILEN Register (offset = 6h) [reset = 0h]

SDMFILEN is shown in [Figure 11-13](#) and described in [Table 11-15](#).

SD Master Filter Enable

Figure 11-13. SDMFILEN Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED		MFE	RESERVED	RESERVED	RESERVED
R-0h		R-0h		R/W-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED		RESERVED			RESERVED		
R-0h		R-0h			R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-15. SDMFILEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	MFE	R/W	0h	Master Filter Enable. Functionally AND'ed with bit FEN in the Data Filter Parameter Register 0: Data filter units of all filter modules are disabled. 1: Data filter units can be enabled if bit FEN is '1'.
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8-7	RESERVED	R	0h	Reserved
6-4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

11.7.2.5 SDSTATUS Register (offset = 7h) [reset = 0h]

SDSTATUS is shown in [Figure 11-14](#) and described in [Table 11-16](#).

SD Status Register

Figure 11-14. SDSTATUS Register

15	14	13	12	11	10	9	8
MAL4	MAL3	MAL2	MAL1	MAF4	MAF3	MAF2	MAF1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

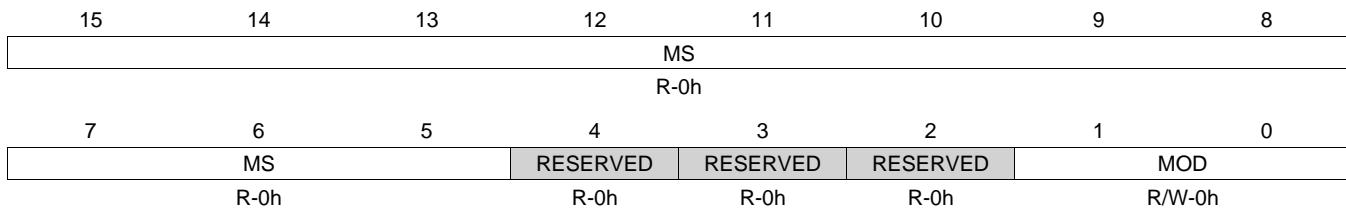
Table 11-16. SDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MAL4	R	0h	Manchester locked status for filter module 4. 0: The automatic Manchester decoder calibration is working properly 1: The automatic Manchester decoder calibration has not been able to perform a successful calibration
14	MAL3	R	0h	Manchester locked status for filter module 3. 0: The automatic Manchester decoder calibration is working properly 1: The automatic Manchester decoder calibration has not been able to perform a successful calibration
13	MAL2	R	0h	Manchester locked status for filter module 2. 0: The automatic Manchester decoder calibration is working properly 1: The automatic Manchester decoder calibration has not been able to perform a successful calibration
12	MAL1	R	0h	Manchester locked status for filter module 1. 0: The automatic Manchester decoder calibration is working properly 1: The automatic Manchester decoder calibration has not been able to perform a successful calibration
11	MAF4	R	0h	Manchester failure status for filter module 4. 0: The automatic Manchester decoder calibration has worked properly since last read access 1: The automatic Manchester decoder has detected problems since last read access
10	MAF3	R	0h	Manchester failure status for filter module 3. 0: The automatic Manchester decoder calibration has worked properly since last read access 1: The automatic Manchester decoder has detected problems since last read access
9	MAF2	R	0h	Manchester failure status for filter module 2. 0: The automatic Manchester decoder calibration has worked properly since last read access 1: The automatic Manchester decoder has detected problems since last read access
8	MAF1	R	0h	Manchester failure status for filter module 1. 0: The automatic Manchester decoder calibration has worked properly since last read access 1: The automatic Manchester decoder has detected problems since last read access
7-0	RESERVED	R	0h	Reserved

11.7.2.6 SDCTLPARM1 Register (offset = 10h) [reset = 0h]

SDCTLPARM1 is shown in [Figure 11-15](#) and described in [Table 11-17](#).

Control Parameter Register for Ch1

Figure 11-15. SDCTLPARM1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-17. SDCTLPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	MS	R	0h	Manchester Status MS10:MS0
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1-0	MOD	R/W	0h	Delta-Sigma Modulator mode 00: The clock speed is equal to the data rate from the modulator 01: The clock rate is half of the data rate from the modulator 10: The data from the modulator is Manchester decoded 11: The clock rate is twice the data rate of the modulator

11.7.2.7 SDDFPARM1 Register (offset = 11h) [reset = 0h]

SDDFPARM1 is shown in [Figure 11-16](#) and described in [Table 11-18](#).

Data Filter Parameter Register for Ch1

Figure 11-16. SDDFPARM1 Register

15	14	13	12	11	10	9	8
RESERVED		FILRESEN		SST		AE	FEN
R-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DOSR							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-18. SDDFPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	FILRESEN	R/W	0h	Data Filter Reset enable for External Reset typ from PWM Compare output. 0: Data filter cannot be reset by external PWM compare output 1: Data filter can be reset by external PWM compare output
11-10	SST	R/W	0h	Data filter structure. 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	R/W	0h	Acknowledge enable. 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	R/W	0h	Filter enable. 0: The filter is disabled and no data is produced 1: The filter is enabled and data are produced in the Data filter
7-0	DOSR	R/W	0h	Oversampling ratio. The actual rate is DOSR + 1. These bits set the oversampling ratio of the filter. 0x0FF represents an oversampling ratio of 256.

11.7.2.8 SDIPARM1 Register (offset = 12h) [reset = 0h]

SDIPARM1 is shown in [Figure 11-17](#) and described in [Table 11-19](#).

Integer Parameter Register for Ch1

Figure 11-17. SDIPARM1 Register

15	14	13	12	11	10	9	8
		SH		DR	RESERVED	RESERVED	
		R/W-0h		R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-19. SDIPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	R/W	0h	Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R	0h	Reserved
6-0	RESERVED	R/W	0h	Reserved

11.7.2.9 SDCMPH1 Register (offset = 13h) [reset = 0h]

SDCMPH1 is shown in [Figure 11-18](#) and described in [Table 11-20](#).

High-level Threshold Register for Ch1

Figure 11-18. SDCMPH1 Register

15	14	13	12	11	10	9	8
RESERVED				HLT			
				R-0h		R/W-0h	
7	6	5	4	3	2	1	0
				HLT		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-20. SDCMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	HLT	R/W	0h	Unsigned high-level threshold for the comparator filter output.

11.7.2.10 SDCMPL1 Register (offset = 14h) [reset = 0h]

SDCMPL1 is shown in [Figure 11-19](#) and described in [Table 11-21](#).

Low-level Threshold Register for Ch1

Figure 11-19. SDCMPL1 Register

15	14	13	12	11	10	9	8
RESERVED				LLT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
			LLT				R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-21. SDCMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output.

11.7.2.11 SDCPARM1 Register (offset = 15h) [reset = 0h]

SDCPARM1 is shown in [Figure 11-20](#) and described in [Table 11-22](#).

Comparator Parameter Register for Ch1

Figure 11-20. SDCPARM1 Register

15	14	13	12	11	10	9	8
RESERVED						MFIE	CS1_CS0
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CS1_CS0	IEL	IEH		COSR			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

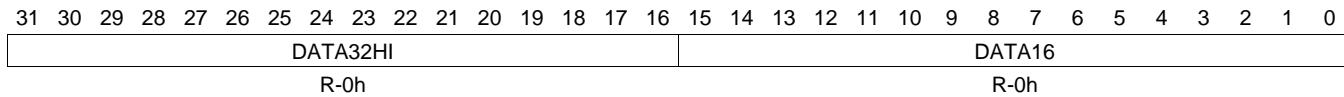
Table 11-22. SDCPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	MFIE	R/W	0h	0: The modulator failure flag as well as the output INT is disabled for this particular flag 1: The modulator failure flag is enabled
8-7	CS1_CS0	R/W	0h	Comparator filter structure. 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	IEL	R/W	0h	Low-level interrupt enable. 0: The low-level interrupt flag as well as the output INT is disabled for this particular flag 1: The low-level interrupt flag is enabled
5	IEH	R/W	0h	High-level interrupt enable. 0: The high-level interrupt flag as well as the output INT is disabled for this particular flag 1: The high-level interrupt flag is enabled
4-0	COSR	R/W	0h	Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 31.

11.7.2.12 SDDATA1 Register (offset = 16h) [reset = 0h]

SDDATA1 is shown in [Figure 11-21](#) and described in [Table 11-23](#).

Filter Data Register (16 or 32bit) for Ch1

Figure 11-21. SDDATA1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

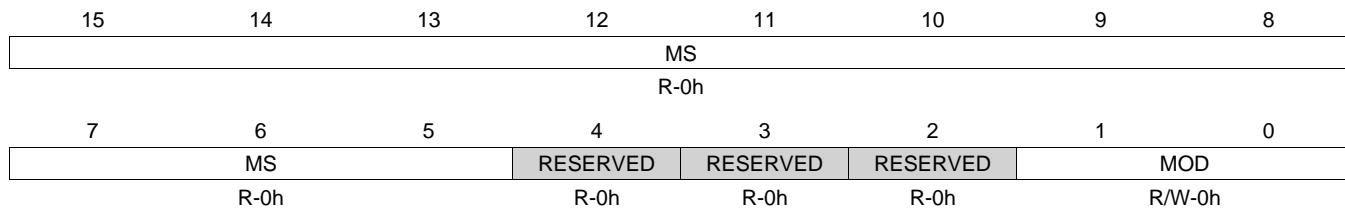
Table 11-23. SDDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode
15-0	DATA16	R	0h	16-bit Data in 16b mode, Lo-order 16b in 32b mode

11.7.2.13 SDCTLPARM2 Register (offset = 20h) [reset = 0h]

SDCTLPARM2 is shown in [Figure 11-22](#) and described in [Table 11-24](#).

Control Parameter Register for Ch2

Figure 11-22. SDCTLPARM2 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-24. SDCTLPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	MS	R	0h	Manchester Status MS10:MS0
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1-0	MOD	R/W	0h	Delta-Sigma Modulator mode 00: The clock speed is equal to the data rate from the modulator 01: The clock rate is half of the data rate from the modulator 10: The data from the modulator is Manchester decoded 11: The clock rate is twice the data rate of the modulator

11.7.2.14 SDDFPARM2 Register (offset = 21h) [reset = 0h]

SDDFPARM2 is shown in [Figure 11-23](#) and described in [Table 11-25](#).

Data Filter Parameter Register for Ch2

Figure 11-23. SDDFPARM2 Register

15	14	13	12	11	10	9	8
RESERVED		FILRESEN		SST		AE	FEN
R-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
			DOSR				
			R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-25. SDDFPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	FILRESEN	R/W	0h	Data Filter Reset enable for External Reset typ from PWM Compare output. 0: Data filter cannot be reset by external PWM compare output 1: Data filter can be reset by external PWM compare output
11-10	SST	R/W	0h	Data filter structure. 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	R/W	0h	Acknowledge enable. 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	R/W	0h	Filter enable. 0: The filter is disabled and no data is produced 1: The filter is enabled and data are produced in the Data filter
7-0	DOSR	R/W	0h	Oversampling ratio. The actual rate is DOSR + 1. These bits set the oversampling ratio of the filter. 0x0FF represents an oversampling ratio of 256.

11.7.2.15 SDIPARM2 Register (offset = 22h) [reset = 0h]SDIPARM2 is shown in [Figure 11-24](#) and described in [Table 11-26](#).

Integer Parameter Register for Ch2

Figure 11-24. SDIPARM2 Register

15	14	13	12	11	10	9	8
		SH		DR	RESERVED	RESERVED	
		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-26. SDIPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	R/W	0h	Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R	0h	Reserved
6-0	RESERVED	R/W	0h	Reserved

11.7.2.16 SDCMPH2 Register (offset = 23h) [reset = 0h]

SDCMPH2 is shown in [Figure 11-25](#) and described in [Table 11-27](#).

High-level Threshold Register for Ch2

Figure 11-25. SDCMPH2 Register

15	14	13	12	11	10	9	8
RESERVED				HLT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
				HLT			
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-27. SDCMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	HLT	R/W	0h	Unsigned high-level threshold for the comparator filter output.

11.7.2.17 SDCMPL2 Register (offset = 24h) [reset = 0h]SDCMPL2 is shown in [Figure 11-26](#) and described in [Table 11-28](#).

Low-level Threshold Register for Ch2

Figure 11-26. SDCMPL2 Register

15	14	13	12	11	10	9	8
RESERVED				LLT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
			LLT				R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-28. SDCMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output.

11.7.2.18 SDCPARM2 Register (offset = 25h) [reset = 0h]

SDCPARM2 is shown in [Figure 11-27](#) and described in [Table 11-29](#).

Comparator Parameter Register for Ch2

Figure 11-27. SDCPARM2 Register

15	14	13	12	11	10	9	8
RESERVED							MFIE
R-0h							R/W-0h
7	6	5	4	3	2	1	0
CS1_CS0	IEL	IEH			COSR		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

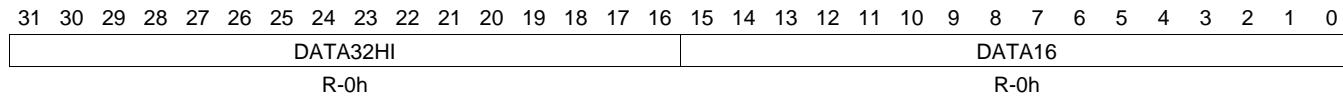
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-29. SDCPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	MFIE	R/W	0h	0: The modulator failure flag as well as the output INT is disabled for this particular flag 1: The modulator failure flag is enabled
8-7	CS1_CS0	R/W	0h	Comparator filter structure. 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	IEL	R/W	0h	Low-level interrupt enable. 0: The low-level interrupt flag as well as the output INT is disabled for this particular flag 1: The low-level interrupt flag is enabled
5	IEH	R/W	0h	High-level interrupt enable. 0: The high-level interrupt flag as well as the output INT is disabled for this particular flag 1: The high-level interrupt flag is enabled
4-0	COSR	R/W	0h	Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 31.

11.7.2.19 SDDATA2 Register (offset = 26h) [reset = 0h]SDDATA2 is shown in [Figure 11-28](#) and described in [Table 11-30](#).

Filter Data Register (16 or 32bit) for Ch2

Figure 11-28. SDDATA2 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

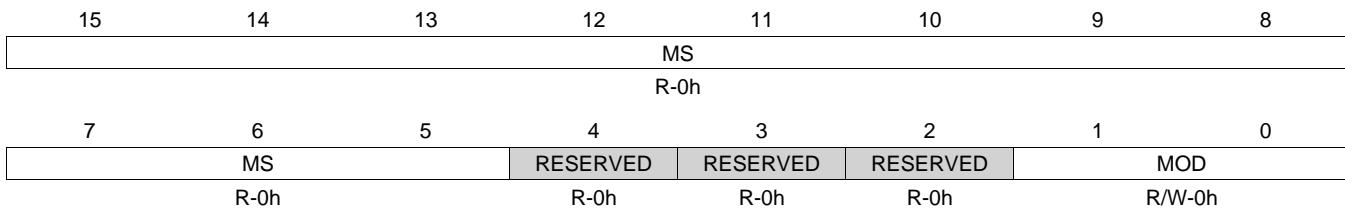
Table 11-30. SDDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode
15-0	DATA16	R	0h	16-bit Data in 16b mode, Lo-order 16b in 32b mode

11.7.2.20 SDCTLPARM3 Register (offset = 30h) [reset = 0h]

SDCTLPARM3 is shown in [Figure 11-29](#) and described in [Table 11-31](#).

Control Parameter Register for Ch3

Figure 11-29. SDCTLPARM3 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-31. SDCTLPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	MS	R	0h	Manchester Status MS10:MS0
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1-0	MOD	R/W	0h	Delta-Sigma Modulator mode 00: The clock speed is equal to the data rate from the modulator 01: The clock rate is half of the data rate from the modulator 10: The data from the modulator is Manchester decoded 11: The clock rate is twice the data rate of the modulator

11.7.2.21 SDDFPARM3 Register (offset = 31h) [reset = 0h]

SDDFPARM3 is shown in [Figure 11-30](#) and described in [Table 11-32](#).

Data Filter Parameter Register for Ch3

Figure 11-30. SDDFPARM3 Register

15	14	13	12	11	10	9	8
RESERVED		FILRESEN		SST		AE	FEN
R-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DOSR							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-32. SDDFPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	FILRESEN	R/W	0h	Data Filter Reset enable for External Reset typ from PWM Compare output. 0: Data filter cannot be reset by external PWM compare output 1: Data filter can be reset by external PWM compare output
11-10	SST	R/W	0h	Data filter structure. 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	R/W	0h	Acknowledge enable. 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	R/W	0h	Filter enable. 0: The filter is disabled and no data is produced 1: The filter is enabled and data are produced in the data filter
7-0	DOSR	R/W	0h	Oversampling ratio. The actual rate is DOSR + 1. These bits set the oversampling ratio of the filter. 0x0FF represents an oversampling ratio of 256.

11.7.2.22 SDIPARM3 Register (offset = 32h) [reset = 0h]

SDIPARM3 is shown in [Figure 11-31](#) and described in [Table 11-33](#).

Integer Parameter Register for Ch3

Figure 11-31. SDIPARM3 Register

15	14	13	12	11	10	9	8
		SH		DR	RESERVED	RESERVED	
		R/W-0h		R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-33. SDIPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	R/W	0h	Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R	0h	Reserved
6-0	RESERVED	R/W	0h	Reserved

11.7.2.23 SDCMPH3 Register (offset = 33h) [reset = 0h]SDCMPH3 is shown in [Figure 11-32](#) and described in [Table 11-34](#).

High-level Threshold Register for Ch3

Figure 11-32. SDCMPH3 Register

15	14	13	12	11	10	9	8
RESERVED				HLT			
	R-0h			R/W-0h			
7	6	5	4	3	2	1	0
		HLT		R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-34. SDCMPH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	HLT	R/W	0h	Unsigned high-level threshold for the comparator filter output.

11.7.2.24 SDCMPL3 Register (offset = 34h) [reset = 0h]

SDCMPL3 is shown in [Figure 11-33](#) and described in [Table 11-35](#).

Low-level Threshold Register for Ch3

Figure 11-33. SDCMPL3 Register

15	14	13	12	11	10	9	8
RESERVED				LLT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
			LLT				R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-35. SDCMPL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output.

11.7.2.25 SDCPARM3 Register (offset = 35h) [reset = 0h]

SDCPARM3 is shown in [Figure 11-34](#) and described in [Table 11-36](#).

Comparator Parameter Register for Ch3

Figure 11-34. SDCPARM3 Register

15	14	13	12	11	10	9	8
RESERVED						MFIE	CS1_CS0
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CS1_CS0	IEL	IEH			COSR		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

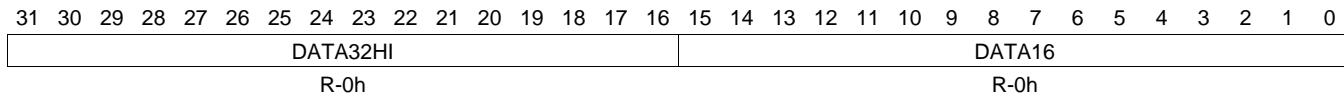
Table 11-36. SDCPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	MFIE	R/W	0h	0: The modulator failure flag as well as the output INT is disabled for this particular flag 1: The modulator failure flag is enabled
8-7	CS1_CS0	R/W	0h	Comparator filter structure. 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	IEL	R/W	0h	Low-level interrupt enable. 0: The low-level interrupt flag as well as the output INT is disabled for this particular flag 1: The low-level interrupt flag is enabled
5	IEH	R/W	0h	High-level interrupt enable. 0: The high-level interrupt flag as well as the output INT is disabled for this particular flag 1: The high-level interrupt flag is enabled
4-0	COSR	R/W	0h	Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 31.

11.7.2.26 SDDATA3 Register (offset = 36h) [reset = 0h]

SDDATA3 is shown in [Figure 11-35](#) and described in [Table 11-37](#).

Filter Data Register (16 or 32bit) for Ch3

Figure 11-35. SDDATA3 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

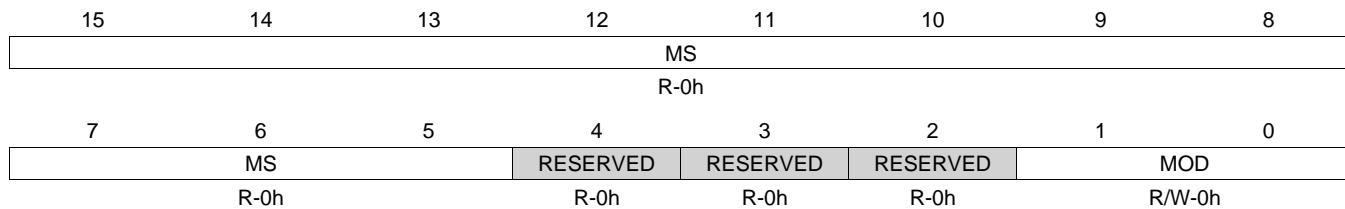
Table 11-37. SDDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode
15-0	DATA16	R	0h	16-bit Data in 16b mode, Lo-order 16b in 32b mode

11.7.2.27 SDCTLPARM4 Register (offset = 40h) [reset = 0h]

SDCTLPARM4 is shown in [Figure 11-36](#) and described in [Table 11-38](#).

Control Parameter Register for Ch4

Figure 11-36. SDCTLPARM4 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-38. SDCTLPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	MS	R	0h	Manchester Status MS10:MS0
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1-0	MOD	R/W	0h	Delta-Sigma Modulator mode 00: The clock speed is equal to the data rate from the modulator 01: The clock rate is half of the data rate from the modulator 10: The data from the modulator is Manchester decoded 11: The clock rate is twice the data rate of the modulator

11.7.2.28 SDDFPARM4 Register (offset = 41h) [reset = 0h]

SDDFPARM4 is shown in [Figure 11-37](#) and described in [Table 11-39](#).

Data Filter Parameter Register for Ch4

Figure 11-37. SDDFPARM4 Register

15	14	13	12	11	10	9	8
RESERVED		FILRESEN		SST		AE	FEN
R-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
			DOSR				
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-39. SDDFPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	FILRESEN	R/W	0h	Data Filter Reset enable for External Reset typ from PWM Compare output. 0: Data filter cannot be reset by external PWM compare output 1: Data filter can be reset by external PWM compare output
11-10	SST	R/W	0h	Data filter structure. 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	R/W	0h	Acknowledge enable. 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	R/W	0h	Filter enable. 0: The filter is disabled and no data is produced 1: The filter is enabled and data are produced in the sinc filter
7-0	DOSR	R/W	0h	Oversampling ratio. The actual rate is DOSR + 1. These bits set the oversampling ratio of the filter. 0x0FF represents an oversampling ratio of 256.

11.7.2.29 SDIPARM4 Register (offset = 42h) [reset = 0h]SDIPARM4 is shown in [Figure 11-38](#) and described in [Table 11-40](#).

Integer Parameter Register for Ch4

Figure 11-38. SDIPARM4 Register

15	14	13	12	11	10	9	8
		SH		DR	RESERVED	RESERVED	
		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			RESERVED				
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-40. SDIPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	R/W	0h	Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R	0h	Reserved
6-0	RESERVED	R/W	0h	Reserved

11.7.2.30 SDCMPH4 Register (offset = 43h) [reset = 0h]

SDCMPH4 is shown in [Figure 11-39](#) and described in [Table 11-41](#).

High-level Threshold Register for Ch4

Figure 11-39. SDCMPH4 Register

15	14	13	12	11	10	9	8
RESERVED				HLT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
				HLT			
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-41. SDCMPH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	HLT	R/W	0h	Unsigned high-level threshold for the comparator filter output.

11.7.2.31 SDCMPL4 Register (offset = 44h) [reset = 0h]SDCMPL4 is shown in [Figure 11-40](#) and described in [Table 11-42](#).

Low-level Threshold Register for Ch4

Figure 11-40. SDCMPL4 Register

15	14	13	12	11	10	9	8
RESERVED				LLT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
			LLT				R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-42. SDCMPL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output.

11.7.2.32 SDCPARM4 Register (offset = 45h) [reset = 0h]

SDCPARM4 is shown in [Figure 11-41](#) and described in [Table 11-43](#).

Comparator Parameter Register for Ch4

Figure 11-41. SDCPARM4 Register

15	14	13	12	11	10	9	8
RESERVED						MFIE	CS1_CS0
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CS1_CS0	IEL	IEH			COSR		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

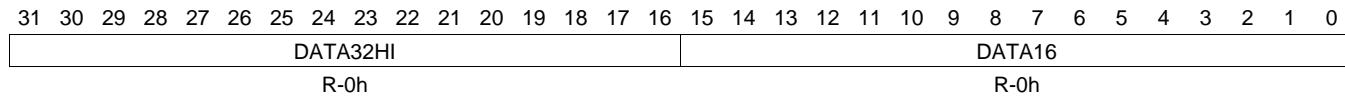
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-43. SDCPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	MFIE	R/W	0h	0: The modulator failure flag as well as the output INT is disabled for this particular flag 1: The modulator failure flag is enabled
8-7	CS1_CS0	R/W	0h	Comparator filter structure. 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	IEL	R/W	0h	Low-level interrupt enable. 0: The low-level interrupt flag as well as the output INT is disabled for this particular flag 1: The low-level interrupt flag is enabled
5	IEH	R/W	0h	High-level interrupt enable. 0: The high-level interrupt flag as well as the output INT is disabled for this particular flag 1: The high-level interrupt flag is enabled
4-0	COSR	R/W	0h	Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 31.

11.7.2.33 SDDATA4 Register (offset = 46h) [reset = 0h]SDDATA4 is shown in [Figure 11-42](#) and described in [Table 11-44](#).

Filter Data Register (16 or 32bit) for Ch4

Figure 11-42. SDDATA4 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 11-44. SDDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode
15-0	DATA16	R	0h	16-bit Data in 16b mode, Lo-order 16b in 32b mode

Enhanced Pulse Width Modulator (ePWM)

The enhanced pulse width modulator (ePWM) peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipments. These systems include digital motor control, switch mode power supply control, uninterruptible power supplies (UPS), and other forms of power conversion. The ePWM peripheral performs a digital to analog (DAC) function, where the duty cycle is equivalent to a DAC analog value; it is sometimes referred to as a Power DAC.

This chapter guide is applicable for ePWM type 4. See the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* ([SPRU566](#)) for a list of all devices with an ePWM module of the same type, to determine the differences between the types, and for a list of device-specific differences within a type.

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12.3 Applications to Power Topologies	1530
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12.1 Introduction

This chapter includes an overview of the module and information about each of its submodules:

- Time-Base Module
- Counter Compare Module
- Action Qualifier Module
- Dead-Band Generator Module
- PWM Chopper (PC) Module
- Trip Zone Module
- Event Trigger Module
- Digital Compare Module

ePWM Type 4 is fully compatible to the Type 2 module (a Type 3 does not exist). Type 4 has the following enhancements in addition to the Type 2 features:

- **Register Address Map**

Additional registers are required for new features on ePWM Type 4. ePWM register address space has been remapped for better alignment and easy usage.

- **Delayed Trip Functionality**

Changes have been added to achieve deadband insertion capabilities to support, for example, delayed trip functionality needed for peak current mode control type application scenarios.

- **Dead-Band Generator Module Enhancements**

Shadowing of DBCTL register to allow dynamic configuration changes

- **One Shot and Global Reload of Registers**

ePWM Type 4 allows one shot and global reload capability from shadow to active registers to avoid partial reloads in, for example, multi-phase applications. It also allows programmable pre-scale of shadow to active reload events.

- **Trip Zone Module Enhancements**

Independent flags have been added to reflect the trip status for each of the TZ sources. Changes have been made to the trip zone module to support certain power converter switching techniques like valley switching.

- **Digital Compare Module Enhancements**

Blanking window filter register width has been increased from 8 to 16 bits. DCCAP functionality has been enhanced to provide more programmability.

- **PWM SYNC Related Enhancements**

ePWM Type 4 allows PWM SYNCOUT generation based on CMPC and CMPD events. These events can also be used for PWMSYNC pulse selection.

ePWM Type 2 is fully compatible to the Type 1 module. Type 2 has the following enhancements in addition to the Type 1 features:

- **High Resolution Dead-Band Capability**

High-Resolution capability is added to Dead-band RED and FED in half-cycle clocking mode.

- **Dead-Band Generator Module Enhancements**

ePWM Type 2 has features to enable both RED and FED on either PWM outputs. Provides increased deadband with 14-bit counters and Dead-band / Dead-band high-resolution registers are shadowed

- **High Resolution Extension available on ePWMxB outputs**

Provides the ability to enable high-resolution period and duty cycle control on ePWMxB outputs. This is discussed in more detail in the HRPWM chapter in this manual.

- **Counter Compare Module Enhancements**

ePWM Type 2 allows Interrupts and SOC events to be generated by additional counter compares CMPC and CMPD.

- **Event Trigger Module Enhancements**

Prescaling logic to issue interrupt requests and ADC start of conversion expanded upto every 15 events. Allows Software initialization of event counters on SYNC event.

- **Digital Compare Module Enhancements**

Digital Compare Trip Select logic [DCTRIPSEL] has up to 12 external trip sources selected by the Input X-BAR logic in addition to an ability to OR all of them (up to 14 [external and internal sources]) to create the respective DCxEVts.

- **Simultaneous Writes to TBPRD and CMPx Registers**

This feature allows writes to TBPRD, CMPA:CMPAHR, CMPB:CMPBHR, CMPC and CMPD of any ePWM module to be tied to any other ePWM module, and also allows all ePWM modules to be tied to a particular ePWM module if desired.

- **Shadow to Active Load on SYNC of TBPRD and CMP Registers**

This feature supports simultaneous writes of TBPRD and CMPA/B/C/D registers.

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The ePWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the ePWM is built up from smaller single channel modules with separate resources that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In this document the letter x within a signal or module name is used to indicate a generic ePWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the ePWMx instance. Thus, EPWM1A and EPWM1B belong to ePWM1 and likewise EPWM4A and EPWM4B belong to ePWM4.

12.1.1 Submodule Overview

The ePWM module represents one complete PWM channel composed of two PWM outputs: EPWMxA and EPWMxB. Multiple ePWM modules are instanced within a device as shown in [Figure 12-1](#). Each ePWM instance is identical with one exception. Some instances include a hardware extension that allows more precise control of the PWM outputs. This extension is the high-resolution pulse width modulator (HRPWM) and is described in the device-specific *High-Resolution Pulse Width Modulator (HRPWM) Reference Guide*. See the device-specific data manual to determine which ePWM instances include this feature. Each ePWM module is indicated by a numerical value starting with 1. For example ePWM1 is the first instance and ePWM3 is the 3rd instance in the system and ePWMx indicates any instance.

The ePWM modules are chained together via a clock synchronization scheme that allows them to operate as a single system when required. Additionally, this synchronization scheme can be extended to the capture peripheral modules (eCAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

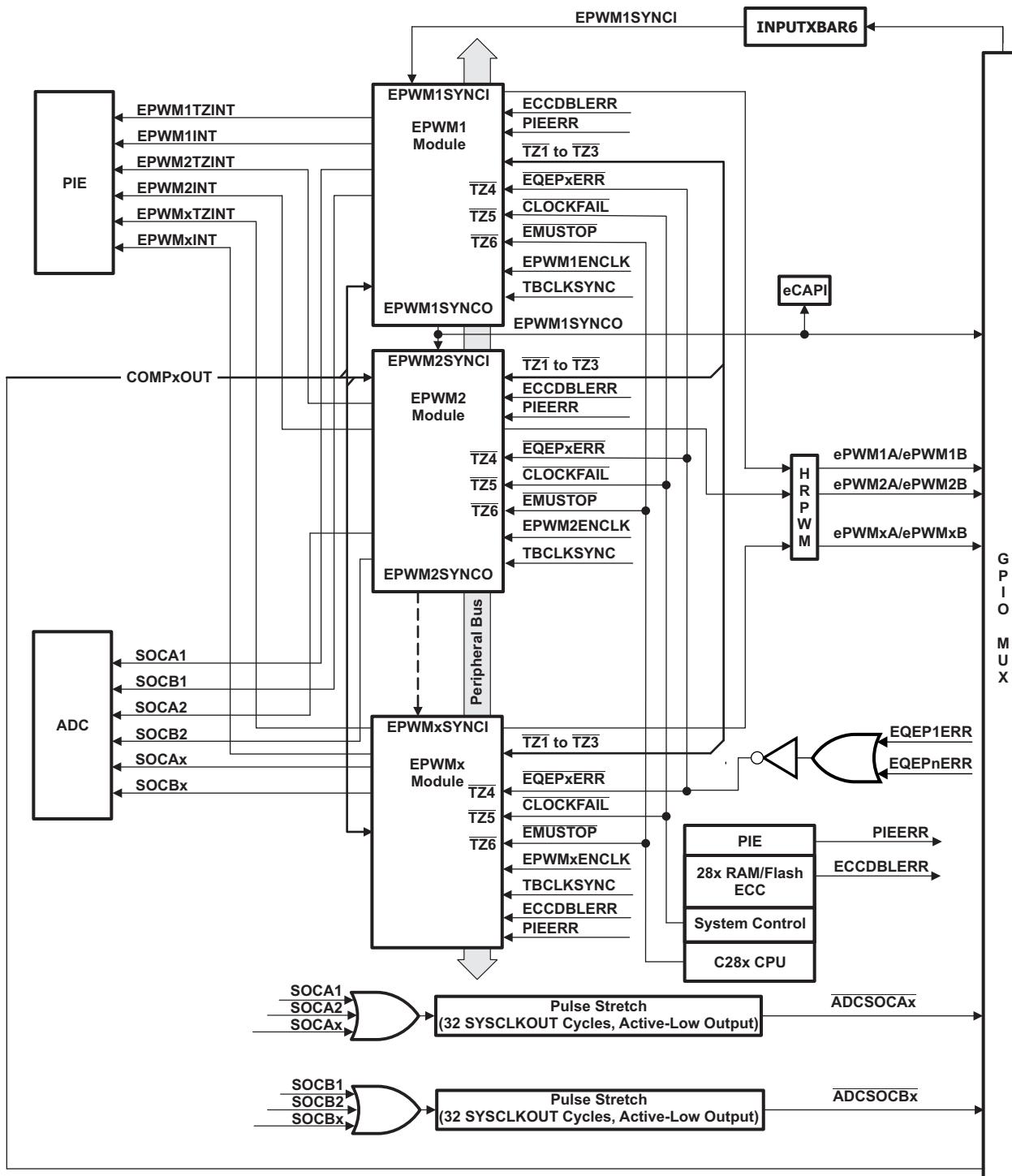
Each ePWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
 - Two independent PWM outputs with single-edge operation
 - Two independent PWM outputs with dual-edge symmetric operation
 - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software.
- Programmable phase-control support for lag or lead operation relative to other ePWM modules.
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis.
- Dead-band generation with independent rising and falling edge delay control.
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions.
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs.
- All events can trigger both CPU interrupts and ADC start of conversion (SOC)

- Programmable event prescaling minimizes CPU overhead on interrupts.
- PWM chopping by high-frequency carrier signal, useful for pulse transformer gate drives.

Each ePWM module is connected to the input/output signals shown in [Figure 12-1](#). The signals are described in detail in subsequent sections.

Figure 12-1. Multiple ePWM Modules



A This signal exists only on devices with an eQEP module.

The order in which the ePWM modules are connected may differ from what is shown in Figure 12-1. See Section 12.2.2.3.3 for the synchronization scheme for a particular device. Each ePWM module consists of eight submodules and is connected within a system via the signals shown in Figure 12-2.

Figure 12-2. Submodules and Signal Connections for an ePWM Module

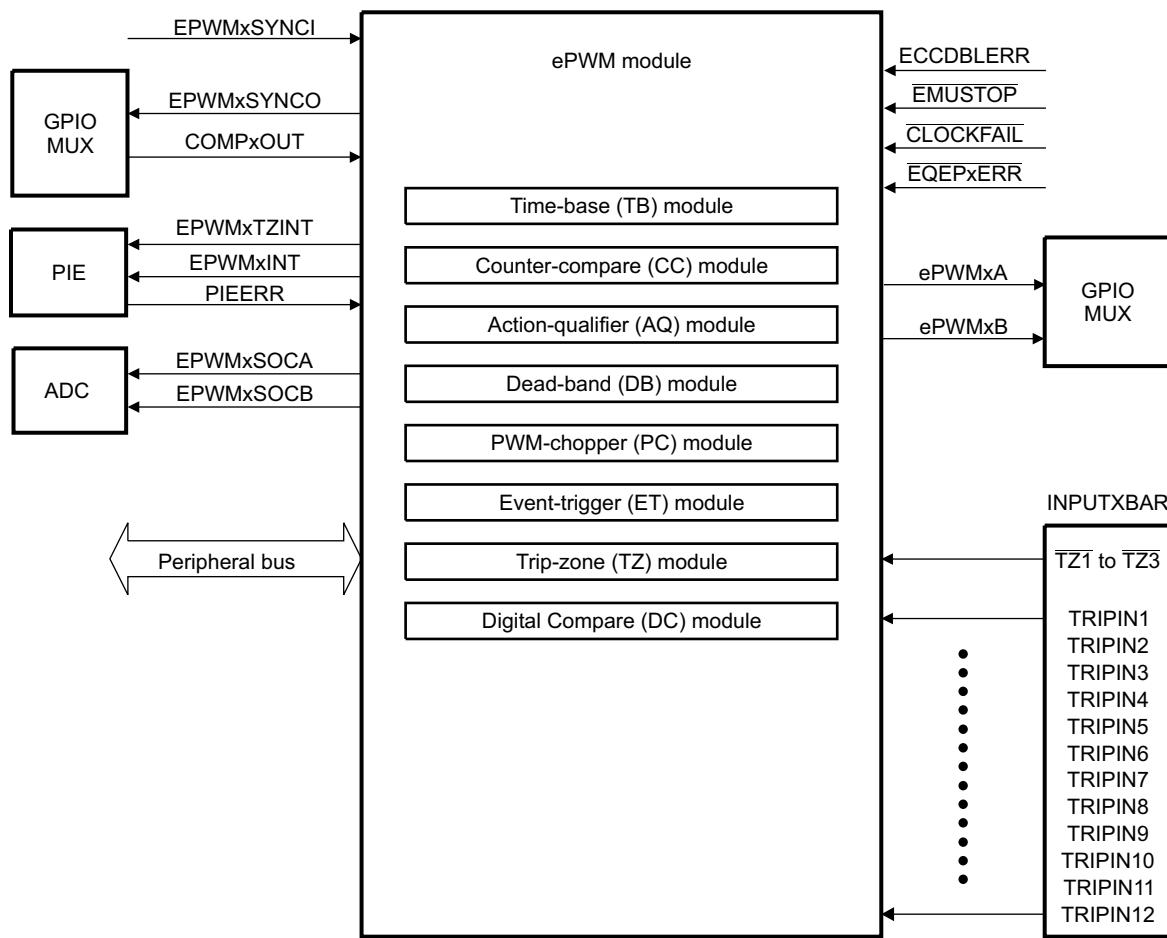


Figure 12-3 shows more internal details of a single ePWM module. The main signals used by the ePWM module are:

- **PWM output signals (EPWMxA and EPWMxB).**

The PWM output signals are made available external to the device through the GPIO peripheral described in the system control and interrupts guide for your device.

- **Trip-zone signals (TZ1 to TZ6).**

These input signals alert the ePWM module of fault conditions external to the ePWM module. Each module on a device can be configured to either use or ignore any of the trip-zone signals. The TZ1 to TZ3 trip-zone signals can be configured as asynchronous inputs through the GPIO peripheral using the Input X-BAR logic, refer to Figure 12-50. TZ4 is connected to an inverted EQEPx error signal (EQEPxERR), which can be generated from any one of the EQEP module (for those devices with an EQEP module). TZ5 is connected to the system clock fail logic, and TZ6 is connected to the EMUSTOP output from the CPU. This allows you to configure a trip action when the clock fails or the CPU halts.

- **Time-base synchronization input (EPWMxSYNCI) and output (EPWMxSYNCO) signals.**

The synchronization signals daisy chain the ePWM modules together. Each module can be configured via INPUTXBAR6 to either use or ignore its synchronization input. The clock synchronization input and output signal are brought out to pins only for ePWM1 (ePWM module #1). The ePWM modules are separate into groups of three for syncing purposes. An external sync signal (EXTSYNCIN1 or EXTSYNCIN2) may be used to issue a sync signal to the first ePWM module in each chain. These

same modules can also send their EPWMSYNCO signal to a GPIO. For more information, see the Time-Base Counter Synchronization Scheme in this chapter.

- **ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB).**

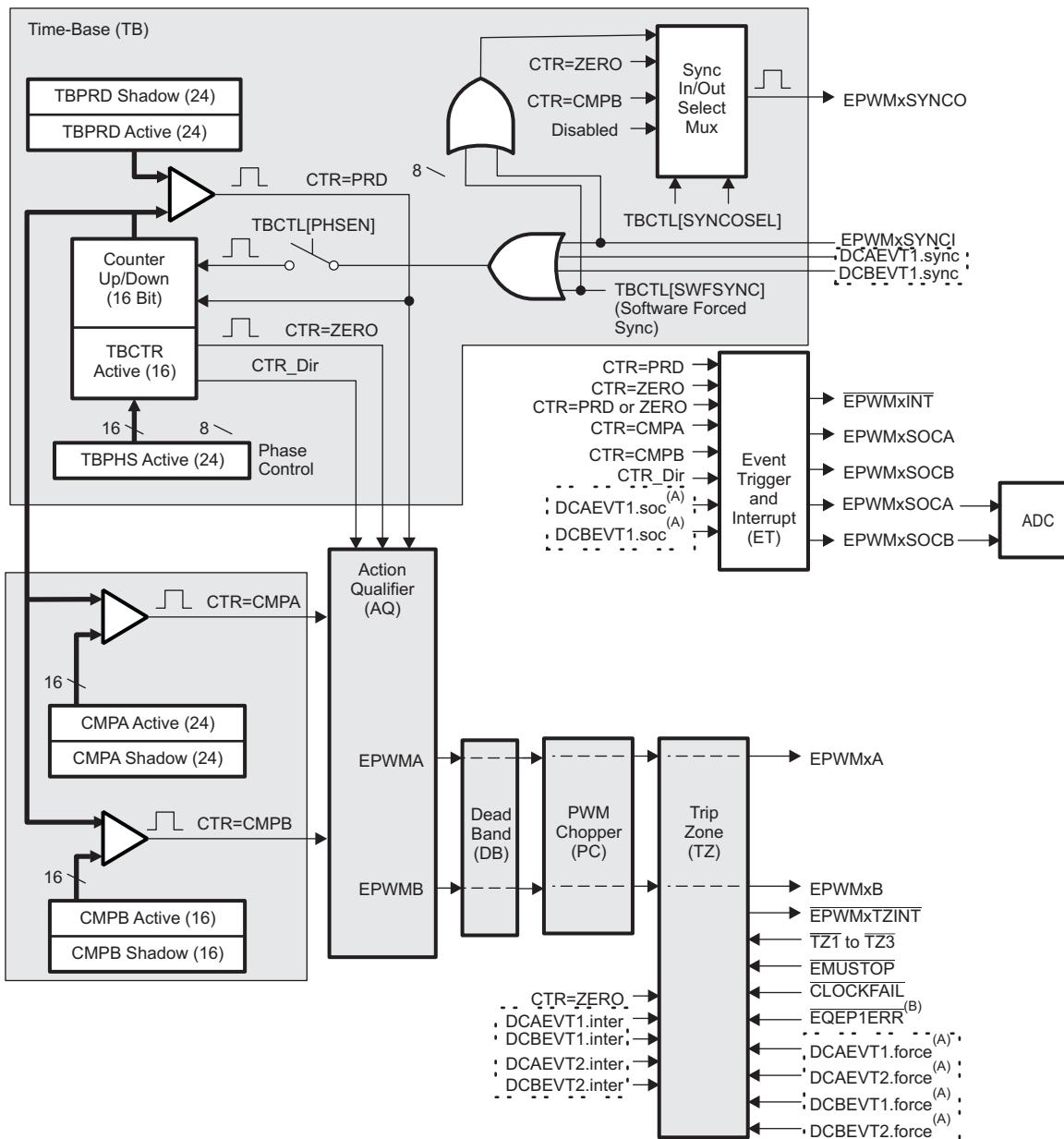
Each ePWM module has two ADC start of conversion signals. Any ePWM module can trigger a start of conversion. Whichever event triggers the start of conversion is configured in the Event-Trigger submodule of the ePWM.

- **Comparator output signals (COMPxOUT).**

Output signals from the comparator module can be fed through the Input X-BAR to one or all of the 12 trip inputs [TRIPIN1 - TRIPIN12] and in conjunction with the trip zone signals can generate digital compare events.

- **Peripheral Bus**

The peripheral bus is 32-bits wide and allows both 16-bit and 32-bit writes to the ePWM register file.

Figure 12-3. ePWM Submodules and Critical Internal Signal Interconnects

- A These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs [for example, COMPXOUT and TZ signals].
- B This signal exists only on devices with eQEP module

12.2 ePWM Submodules

Eight submodules are included in every ePWM peripheral. Each of these submodules performs specific tasks that can be configured by software.

12.2.1 Overview

[Table 12-1](#) lists the eight key submodules together with a list of their main configuration parameters. For example, if you need to adjust or control the duty cycle of a PWM waveform, then you should see the counter-compare submodule in [Section 12.2.3](#) for relevant details.

Table 12-1. Submodule Configuration Parameters

Submodule	Configuration Parameter or Option
Time-base (TB)	<ul style="list-style-type: none"> • Scale the time-base clock (TBCLK) relative to the system clock (SYSCLKOUT). • Configure the PWM time-base counter (TBCTR) frequency or period. • Set the mode for the time-base counter: <ul style="list-style-type: none"> – count-up mode: used for asymmetric PWM – count-down mode: used for asymmetric PWM – count-up-and-down mode: used for symmetric PWM • Configure the time-base phase relative to another ePWM module. • Synchronize the time-base counter between modules through hardware or software. • Configure the direction (up or down) of the time-base counter after a synchronization event. • Simultaneous writes to the TBPRD registers on all PWM's corresponding to the configuration on EPWMXLINK. • Configure how the time-base counter will behave when the device is halted by an emulator. • Specify the source for the synchronization output of the ePWM module: <ul style="list-style-type: none"> – Synchronization input signal – Time-base counter equal to zero – Time-base counter equal to counter-compare B (CMPB) – No output synchronization signal generated. • Configure one shot and global reload of registers in this module.
Counter-compare (CC)	<ul style="list-style-type: none"> • Specify the PWM duty cycle for output EPWMxA and/or output EPWMxB • Specify the time at which switching events occur on the EPWMxA or EPWMxB output • Specify the programmable delay for interrupt and SOC generation with additional comparators • Simultaneous writes to the CMPA, CMPB, CMPC, CMPD registers on all PWM's corresponding to the configuration on EPWMXLINK. • Configure one shot and global reload of registers in this module.
Action-qualifier (AQ)	<ul style="list-style-type: none"> • Specify the type of action taken when a time-base counter-compare, trip-zone submodule or comparator event occurs: <ul style="list-style-type: none"> – No action taken – Output EPWMxA and/or EPWMxB switched high – Output EPWMxA and/or EPWMxB switched low – Output EPWMxA and/or EPWMxB toggled • Force the PWM output state through software control • Configure and control the PWM dead-band through software • Configure one shot and global reload of registers in this module.
Dead-band (DB)	<ul style="list-style-type: none"> • Control of traditional complementary dead-band relationship between upper and lower switches • Specify the output rising-edge-delay value • Specify the output falling-edge delay value • Bypass the dead-band module entirely. In this case the PWM waveform is passed through without modification. • Option to enable half-cycle clocking for double resolution. • Allow ePWMxB phase shifting with respect to the ePWMxA output. • Configure one shot and global reload of registers in this module.

Table 12-1. Submodule Configuration Parameters (continued)

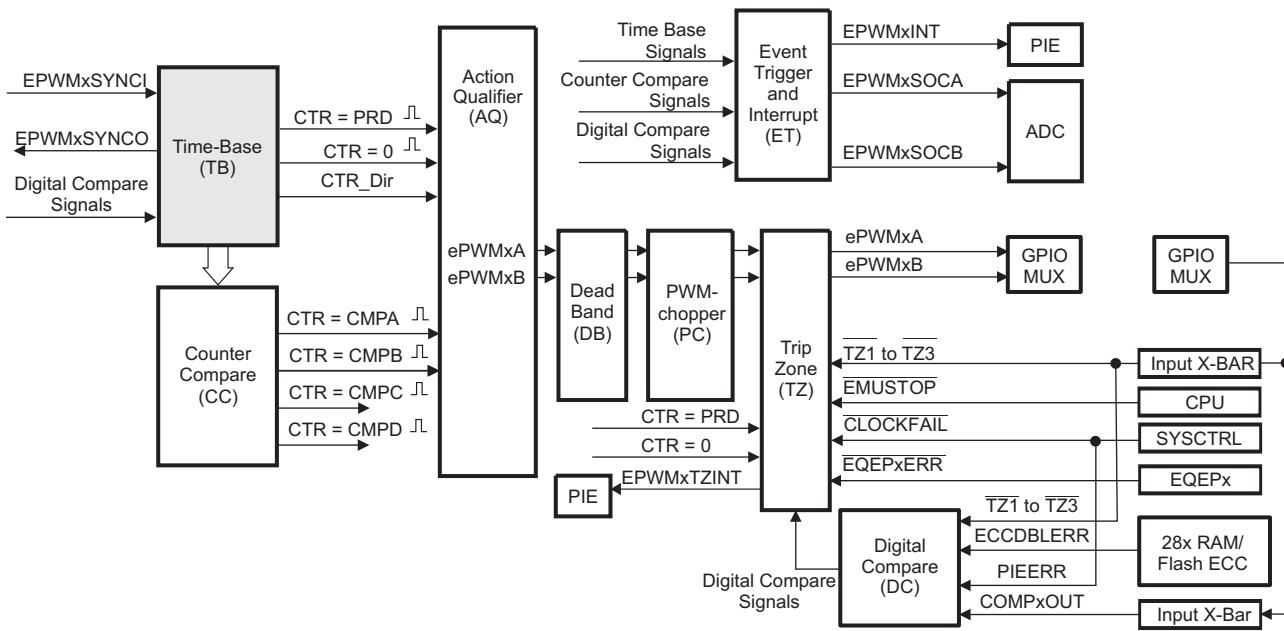
Submodule	Configuration Parameter or Option
PWM-chopper (PC)	<ul style="list-style-type: none"> Create a chopping (carrier) frequency. Pulse width of the first pulse in the chopped pulse train. Duty cycle of the second and subsequent pulses. Bypass the PWM-chopper module entirely. In this case the PWM waveform is passed through without modification.
Trip-zone (TZ)	<ul style="list-style-type: none"> Configure the ePWM module to react to one, all, or none of the trip-zone signals or digital compare events. Specify the trip action taken when a fault occurs: <ul style="list-style-type: none"> Force EPWMxA and/or EPWMxB high Force EPWMxA and/or EPWMxB low Force EPWMxA and/or EPWMxB to a high-impedance state Configure EPWMxA and/or EPWMxB to ignore any trip condition. Configure how often the ePWM will react to each trip-zone signal: <ul style="list-style-type: none"> One-shot Cycle-by-cycle Enable the trip-zone to initiate an interrupt. Bypass the trip-zone module entirely. Programmable option for Cycle-by-cycle trip clear If desired, independently configure trip actions taken when time-base counter is counting down.
Event-trigger (ET)	<ul style="list-style-type: none"> Enable the ePWM events that will trigger an interrupt. Enable ePWM events that will trigger an ADC start-of-conversion event. Specify the rate at which events cause triggers (every occurrence or every 2nd or up to 15th occurrence) Poll, set, or clear event flags
Digital-compare (DC)	<ul style="list-style-type: none"> Enables comparator (COMP) module outputs and trip zone signals which are configured using the Input X-BAR to create events and filtered events Specify event-filtering options to capture TBCTR counter, generate blanking window, or insert delay in PWM output or time-base counter based on captured value.

Code examples are provided in the remainder of this document that show how to implement various ePWM module configurations. These examples use the constant definitions in the device *EPwm_defines.h* file in the device-specific header file and peripheral examples software package.

12.2.2 Time-Base (TB) Submodule

Each ePWM module has its own time-base submodule that determines all of the event timing for the ePWM module. Built-in synchronization logic allows the time-base of multiple ePWM modules to work together as a single system. Figure 12-4 illustrates the time-base module's place within the ePWM.

Figure 12-4. Time-Base Submodule



12.2.2.1 Purpose of the Time-Base Submodule

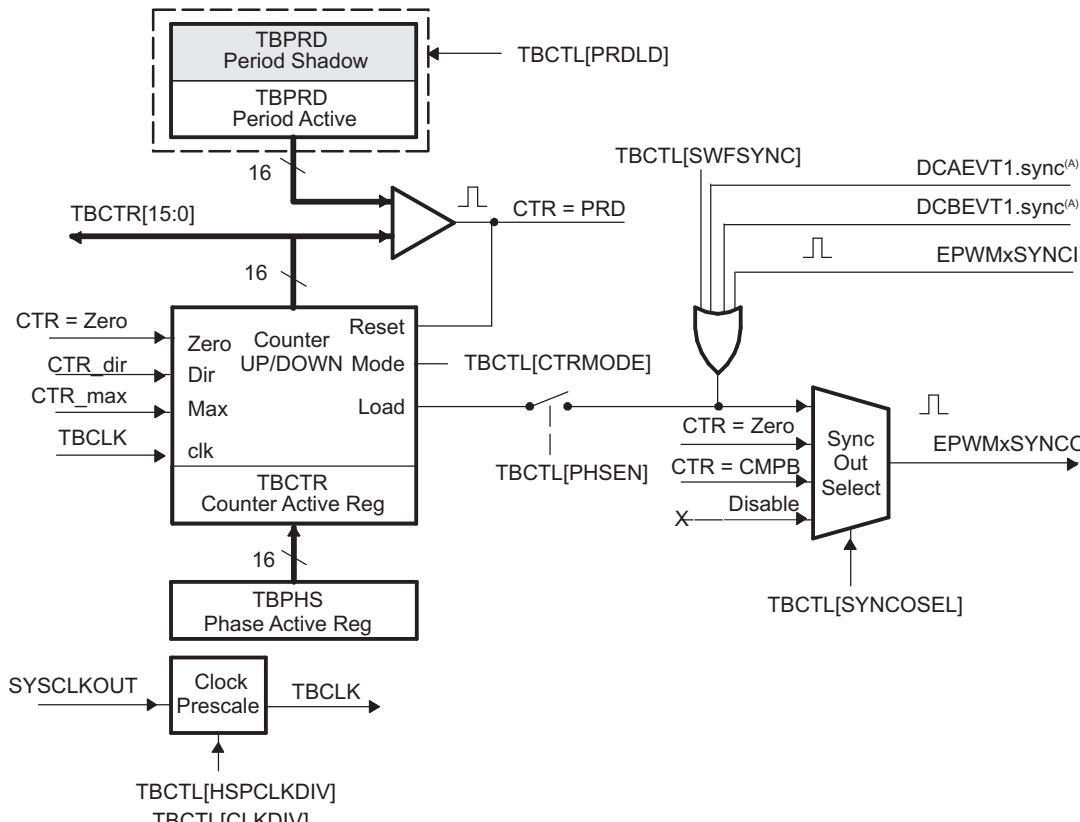
You can configure the time-base submodule for the following:

- Specify the ePWM time-base counter (TBCTR) frequency or period to control how often events occur.
- Manage time-base synchronization with other ePWM modules.
- Maintain a phase relationship with other ePWM modules.
- Set the time-base counter to count-up, count-down, or count-up-and-down mode.
- Generate the following events:
 - CTR = PRD: Time-base counter equal to the specified period (TBCTR = TBPRD) .
 - CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00).
- Configure the rate of the time-base clock; a prescaled version of the CPU system clock (SYSCLKOUT). This allows the time-base counter to increment/decrement at a slower rate.

12.2.2.2 Controlling and Monitoring the Time-Base Submodule

The block diagram in [Figure 12-5](#) shows the critical signals and registers of the time-base submodule. [Table 12-2](#) provides descriptions of the key signals associated with the time-base submodule.

Figure 12-5. Time-Base Submodule Signals and Registers



A. These signals are generated by the digital compare (DC) submodule.

Table 12-2. Key Time-Base Signals

Signal	Description
EPWMxSYNCI	Time-base synchronization input. Input pulse used to synchronize the time-base counter with the counter of ePWM module earlier in the synchronization chain. An ePWM peripheral can be configured to use or ignore this signal. For the first ePWM module in each synchronization chain, this signal may come from a device pin via INPUT5 or INPUT6 of the Input X-BAR or from a previous ePWM module. For subsequent ePWM modules in each chain, this signal is passed from another ePWM peripheral. For example, EPWM2SYNCI is generated by the ePWM1 peripheral, EPWM3SYNCI is generated by ePWM2 and so forth. For information on the synchronization order of a particular device, see Section 12.2.2.3.3 .
EPWMxSYNCO	Time-base synchronization output. This output pulse is used to synchronize the counter of an ePWM module later in the synchronization chain. The ePWM module generates this signal from one of three event sources: <ol style="list-style-type: none"> 1. EPWMxSYNCI (Synchronization input pulse) 2. CTR = Zero: The time-base counter equal to zero (TBCTR = 0x00). 3. CTR = CMPB: The time-base counter equal to the counter-compare B (TBCTR = CMPB) register.
CTR = PRD	Time-base counter equal to the specified period. This signal is generated whenever the counter value is equal to the active period register value. That is when TBCTR = TBPRD.
CTR = Zero	Time-base counter equal to zero This signal is generated whenever the counter value is zero. That is when TBCTR equals 0x00.

Table 12-2. Key Time-Base Signals (continued)

Signal	Description
CTR = CMPB	Time-base counter equal to active counter-compare B register (TBCTR = CMPB). This event is generated by the counter-compare submodule and used by the synchronization out logic
CTR_dir	Time-base counter direction. Indicates the current direction of the ePWM's time-base counter. This signal is high when the counter is increasing and low when it is decreasing.
CTR_max	Time-base counter equal max value. (TBCTR = 0xFFFF) Generated event when the TBCTR value reaches its maximum value. This signal is only used only as a status bit
TBCLK	Time-base clock. This is a prescaled version of the system clock (SYSCLKOUT) and is used by all submodules within the ePWM. This clock determines the rate at which time-base counter increments or decrements.

12.2.2.3 Calculating PWM Period and Frequency

The frequency of PWM events is controlled by the time-base period (TBPRD) register and the mode of the time-base counter. [Figure 12-6](#) shows the period (T_{pwm}) and frequency (F_{pwm}) relationships for the up-count, down-count, and up-down-count time-base counter modes when the period is set to 4 (TBPRD = 4). The time increment for each step is defined by the time-base clock (TBCLK) which is a prescaled version of the system clock (SYSCLKOUT).

The time-base counter has three modes of operation selected by the time-base control register (TBCTL):

- **Up-Down-Count Mode:**

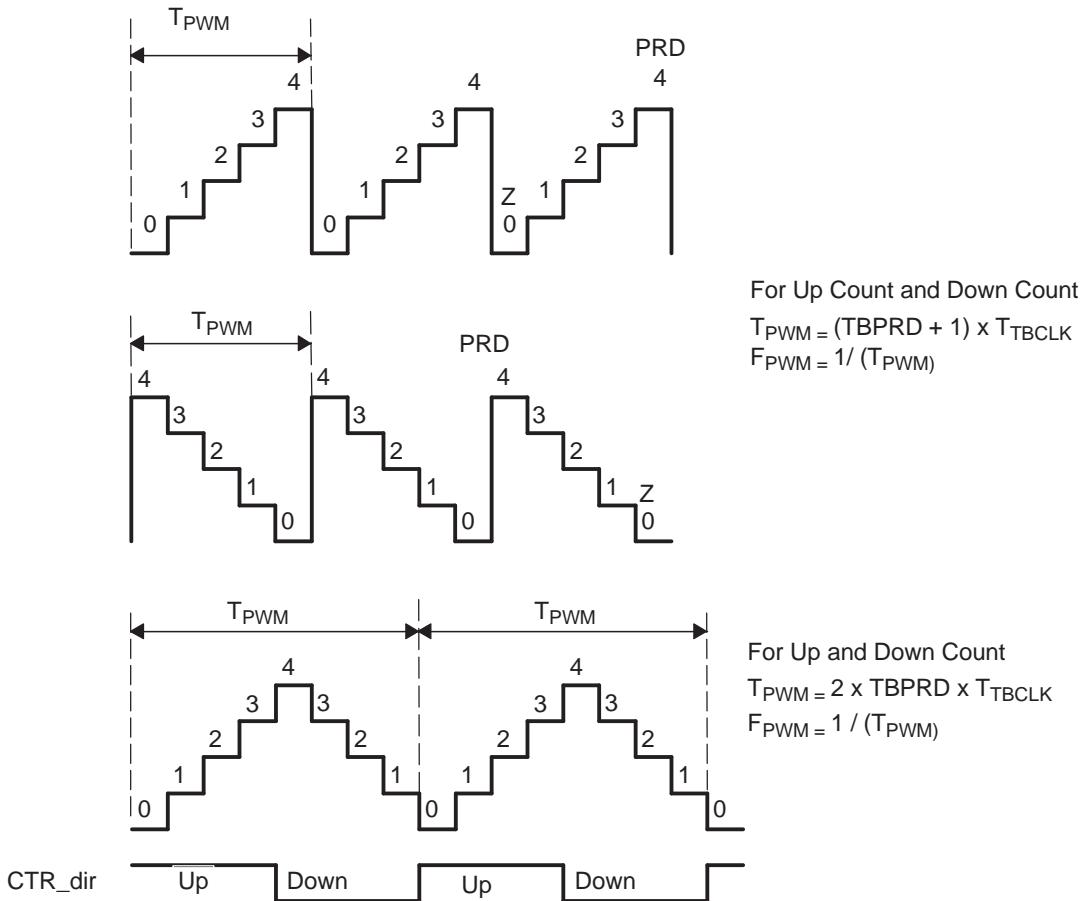
In up-down-count mode, the time-base counter starts from zero and increments until the period (TBPRD) value is reached. When the period value is reached, the time-base counter then decrements until it reaches zero. At this point the counter repeats the pattern and begins to increment.

- **Up-Count Mode:**

In this mode, the time-base counter starts from zero and increments until it reaches the value in the period register (TBPRD). When the period value is reached, the time-base counter resets to zero and begins to increment once again.

- **Down-Count Mode:**

In down-count mode, the time-base counter starts from the period (TBPRD) value and decrements until it reaches zero. When it reaches zero, the time-base counter is reset to the period value and it begins to decrement once again.

Figure 12-6. Time-Base Frequency and Period

12.2.2.3.1 Time-Base Period Shadow Register

The time-base period register (TBPRD) has a shadow register. Shadowing allows the register update to be synchronized with the hardware. The following definitions are used to describe all shadow registers in the ePWM module:

- **Active Register**

The active register controls the hardware and is responsible for actions that the hardware causes or invokes.

- **Shadow Register**

The shadow register buffers or provides a temporary holding location for the active register. It has no direct effect on any control hardware. At a strategic point in time the shadow register's content is transferred to the active register. This prevents corruption or spurious operation due to the register being asynchronously modified by software.

The memory address of the shadow period register is the same as the active register. Which register is written to or read from is determined by the TBCTL[PRLDLD] bit. This bit enables and disables the TBPRD shadow register as follows:

- **Time-Base Period Shadow Mode:**

The TBPRD shadow register is enabled when TBCTL[PRLDLD] = 0. Reads from and writes to the TBPRD memory address go to the shadow register. The shadow register contents are transferred to the active register (TBPRD (Active) \leftarrow TBPRD (shadow)) when the time-base counter equals zero (TBCTR = 0x00) and/or a sync event as determined by the TBCTL2[PRLDLDSYNC] bit. The PRDLDSYNC bit is valid only if TBCTL[PRLDLD] = 0. By default the TBPRD shadow register is enabled. The sources for the SYNC input is explained in Time-Base Counter Synchronization section of this chapter.

The global reload control mechanism can also be used with the time-base period register by configuring the appropriate bits in the global load configuration register (GLDCFG). When global reload mode is selected the transfer of contents from shadow register to active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL). Global reload control mechanism is explained in [Section 12.2.2.7](#).

- **Time-Base Period Immediate Load Mode:**

If immediate load mode is selected (TBCTL[PRDLD] = 1), then a read from or a write to the TBPRD memory address goes directly to the active register.

12.2.2.3.2 Time-Base Clock Synchronization

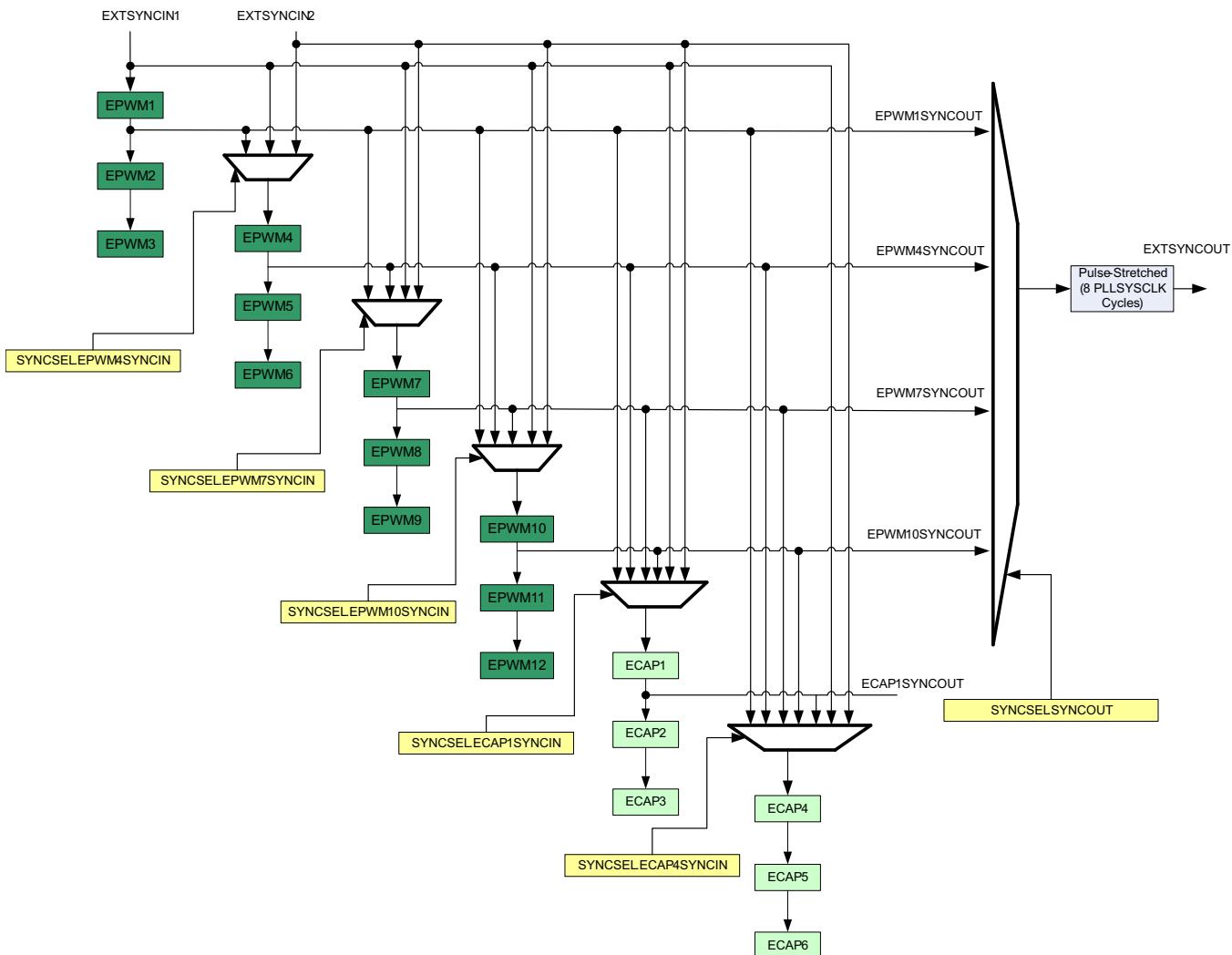
The TBCLKSYNC bit in the peripheral clock enable registers allows all users to globally synchronize all enabled ePWM modules to the time-base clock (TBCLK). When set, all enabled ePWM module clocks are started with the first rising edge of TBCLK aligned. For perfectly synchronized TBCLKs, the prescalers for each ePWM module must be set identically.

The proper procedure for enabling ePWM clocks is as follows:

1. Enable ePWM module clocks in the PCLKCRx register
2. Set TBCLKSYNC= 0
3. Configure ePWM modules
4. Set TBCLKSYNC=1

12.2.2.3.3 Time-Base Counter Synchronization

The ePWM type 4 introduces a new synchronization scheme that allows for increased flexibility of synchronization of the ePWM modules. Each ePWM module has a synchronization input (SYNCI) and a synchronization output (SYNCO). In [Figure 12-7](#), EXTSYNC1 is sourced from INPUTXBAR5 and EXTSYNC2 is sourced from INPUTXBAR6, which can be configured to select any GPIO as the synchronization input. When configuring the sync chain propagation path using the SYNCSEL registers, make sure that the longest path does not exceed four EPWM/ECAP modules.

Figure 12-7. Time-Base Counter Synchronization Scheme 4

NOTE: See the data manual for the number of ePWM and eCAP modules available on your specific device.

Each ePWM module can be configured to use or ignore the synchronization input. If the TBCTL[PHSEN] bit is set, then the time-base counter (TBCTR) of the ePWM module will be automatically loaded with the phase register (TBPHS) contents when one of the following conditions occur:

- **EPWM_xSYNCl: Synchronization Input Pulse:**

The value of the phase register is loaded into the counter register when an input synchronization pulse is detected (TBPHS → TBCTR). This operation occurs on the next valid time-base clock (TBCLK) edge.

The delay from internal master module to slave modules is given by:

- if (TBCLK = SYSCLKOUT): $2 \times \text{SYSCLKOUT}$
- if (TBCLK != SYSCLKOUT): 1 TBCLK

- **Software Forced Synchronization Pulse:**

Writing a 1 to the TBCTL[SWFSYNC] control bit invokes a software forced synchronization. This pulse is ORed with the synchronization input signal, and therefore has the same effect as a pulse on EPWM_xSYNCl.

- **Digital Compare Event Synchronization Pulse:**

DCAEVT1 and DCBEVT1 digital compare events can be configured to generate synchronization

pulses which have the same affect as EPWMxSYNCI.

This feature enables the ePWM module to be automatically synchronized to the time base of another ePWM module. Lead or lag phase control can be added to the waveforms generated by different ePWM modules to synchronize them. In up-down-count mode, the TBCTL[PSHDIR] bit configures the direction of the time-base counter immediately after a synchronization event. The new direction is independent of the direction prior to the synchronization event. The PHSDIR bit is ignored in count-up or count-down modes. See [Figure 12-8](#) through [Figure 12-11](#) for examples.

Clearing the TBCTL[PHSEN] bit configures the ePWM to ignore the synchronization input pulse. The synchronization pulse can still be allowed to flow-through to the EPWMxSYNCO and be used to synchronize other ePWM modules. In this way, you can set up a master time-base (for example, ePWM1) and downstream modules (ePWM2 - ePWMx) may elect to run in synchronization with the master. See the Application to Power Topologies [Section 12.3](#) for more details on synchronization strategies.

12.2.2.4 Phase Locking the Time-Base Clocks of Multiple ePWM Modules

The TBCLKSYNC bit can be used to globally synchronize the time-base clocks of all enabled ePWM modules on a device. This bit is part of the device's clock enable registers and is described in the *System Control and Interrupts* section of this manual. When TBCLKSYNC = 0, the time-base clock of all ePWM modules is stopped (default). When TBCLKSYNC = 1, all ePWM time-base clocks are started with the rising edge of TBCLK aligned. For perfectly synchronized TBCLKs, the prescaler bits in the TBCTL register of each ePWM module must be set identically. The proper procedure for enabling the ePWM clocks is as follows:

1. Enable the individual ePWM module clocks. This is described in the device-specific version of the *System Control and Interrupts Reference Guide*.
2. Set TBCLKSYNC = 0. This will stop the time-base clock within any enabled ePWM module.
3. Configure the prescaler values and desired ePWM modes.
4. Set TBCLKSYNC = 1.

12.2.2.5 Simultaneous Writes to TBPRD and CMPx Registers Between ePWM Modules

For variable frequency applications, there is a need for simultaneous writes of TBPRD and CMPx registers between ePWM modules. This prevents situations where a CTR = 0 or CTR = PRD pulse forces a shadow to active load of these registers before all registers are updated between ePWM modules (resulting in some registers being loaded from new shadow values while others are loaded from old shadow values). To support this, an ePWM register linking scheme for TBPRD:TBPRDH, CMPA:CMPAHR, CMPB:CMPBHR, CMPC, and CMPD registers between PWM modules has been added.

For a particular ePWM module # A , user code writes “B+1”, to the linked register bit-field in EPWMXLINK. “B” is the ePWM module # being linked to (i.e. Writes to the ePWM module “B” TBPRD:TBPRDH, CMPA:CMPAHR, CMPB:CMPBHR, or CMPC will simultaneously be written to corresponding register in ePWM module “A”) For instance if ePWM3 EPWMXLINK register is configured so that CMPA:CMPAHR are linked to ePWM1, then a write to CMPA:CMPAHR in ePWM 1 will simultaneously write the same value to CMPA:CMPAHR in ePWM3. If ePWM4 also has its CMPA:CMPAHR registers linked to ePWM1, then a write to ePWM 1 will write the same value to the CMPA:CMPAHR registers in both ePWM3 and ePWM4.

The register description for EPWMXLINK clearly explains the linked register bit-field values for corresponding ePWM.

NOTE: ePWM register linking scheme works with the TBPRD:TBPRDH [Mirrored instance], CMPA:CMPAHR [Mirrored instance], CMPB:CMPBHR [Mirrored instance], CMPC, and CMPD registers present in the upper page offset. Only the instance of these registers in offsets 0x62-0x6B are linked between ePWM modules

A typical example snippet will use the following registers linked between modules

EPwmRegs.TBPRDHMR2 , EPwmRegs.CMPAM2 , EPwmRegs.CMPBM ,
EPwmRegs.CMPC , EPwmRegs.CMPD

12.2.2.6 Time-base Counter Modes and Timing Waveforms

The time-base counter operates in one of four modes:

- Up-count mode which is asymmetrical.
- Down-count mode which is asymmetrical.
- Up-down-count which is symmetrical
- Frozen where the time-base counter is held constant at the current value

To illustrate the operation of the first three modes, the following timing diagrams show when events are generated and how the time-base responds to an EPWMxSYNCl signal.

Figure 12-8. Time-Base Up-Count Mode Waveforms

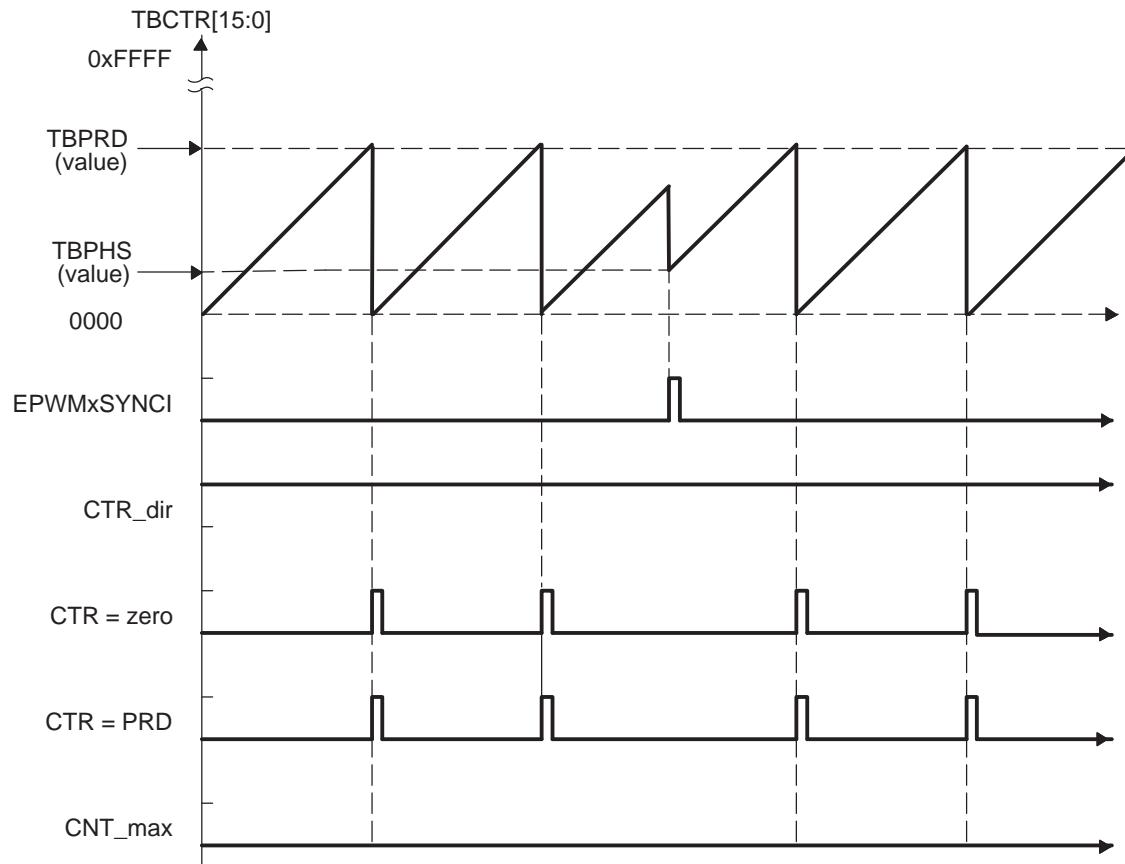


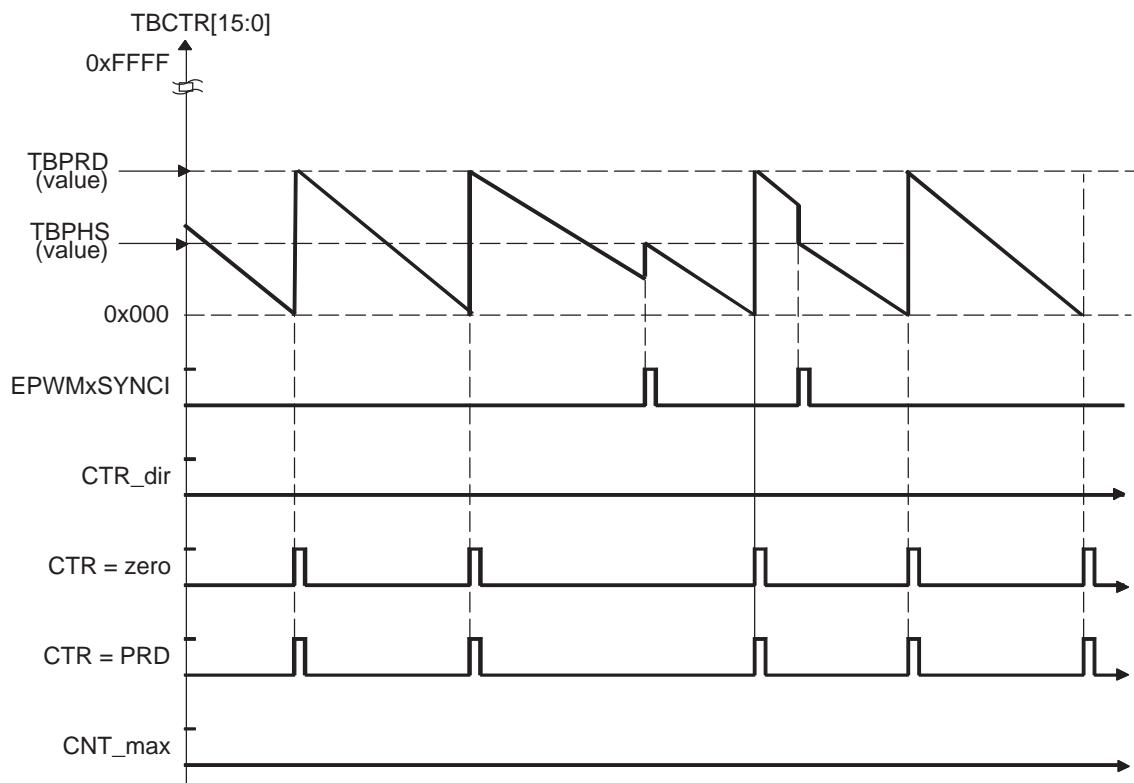
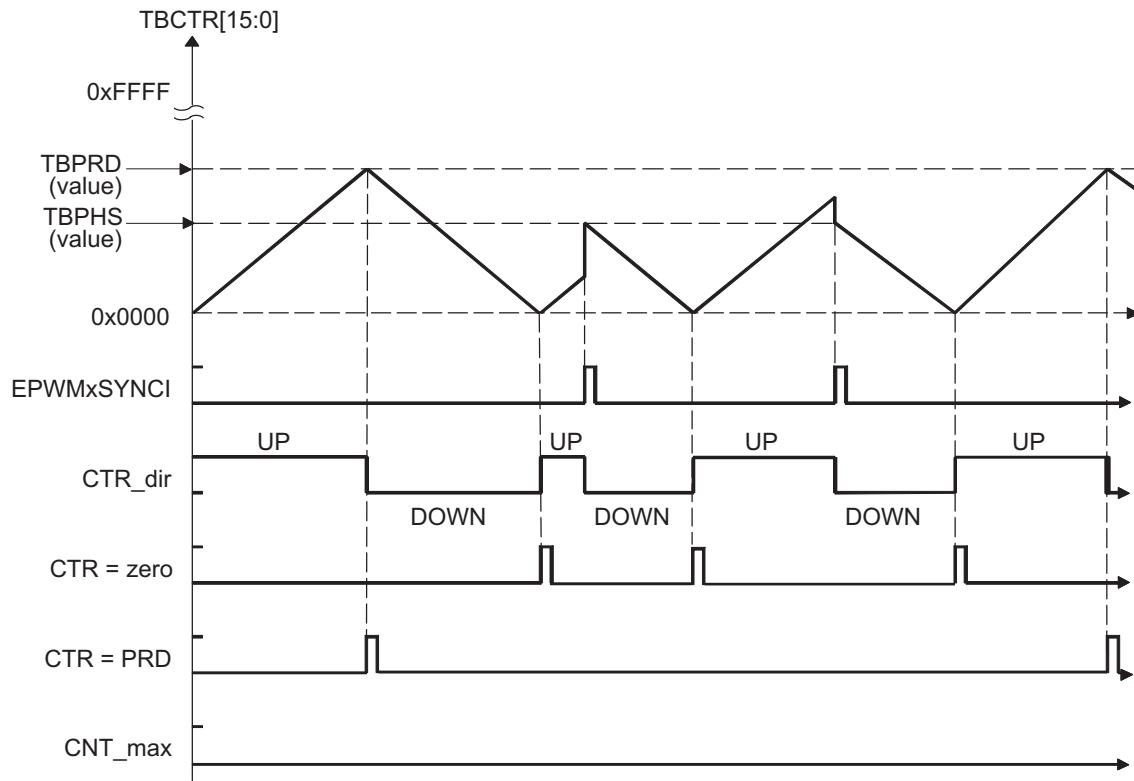
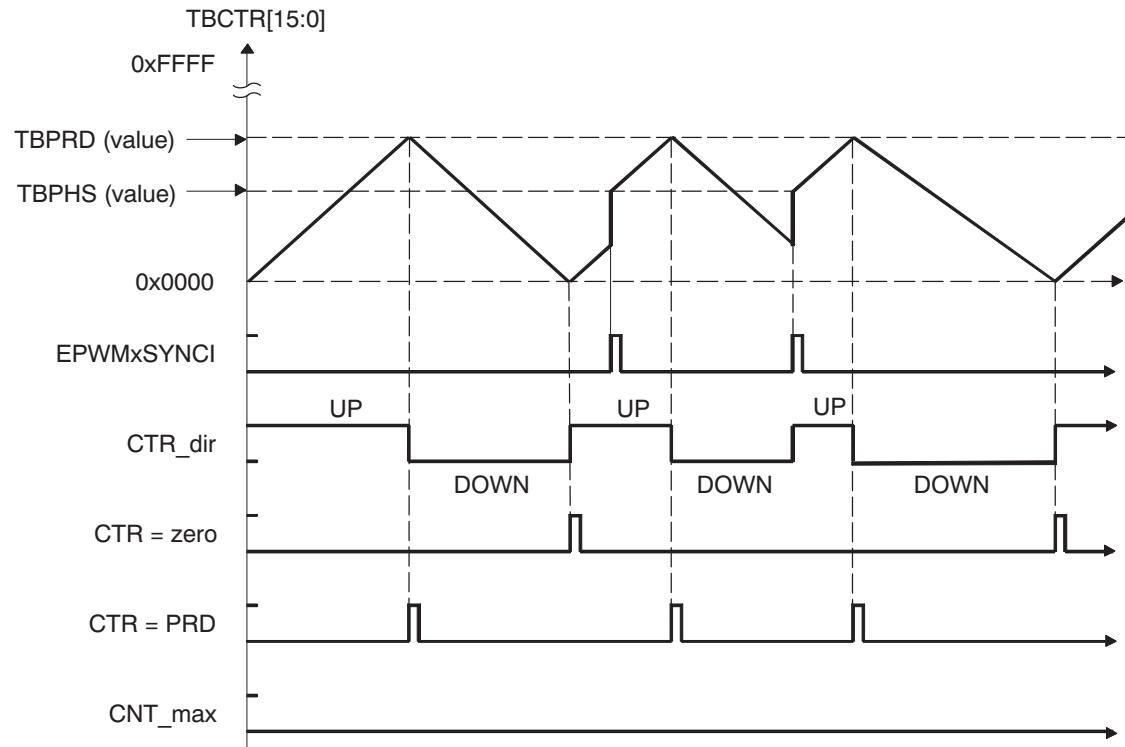
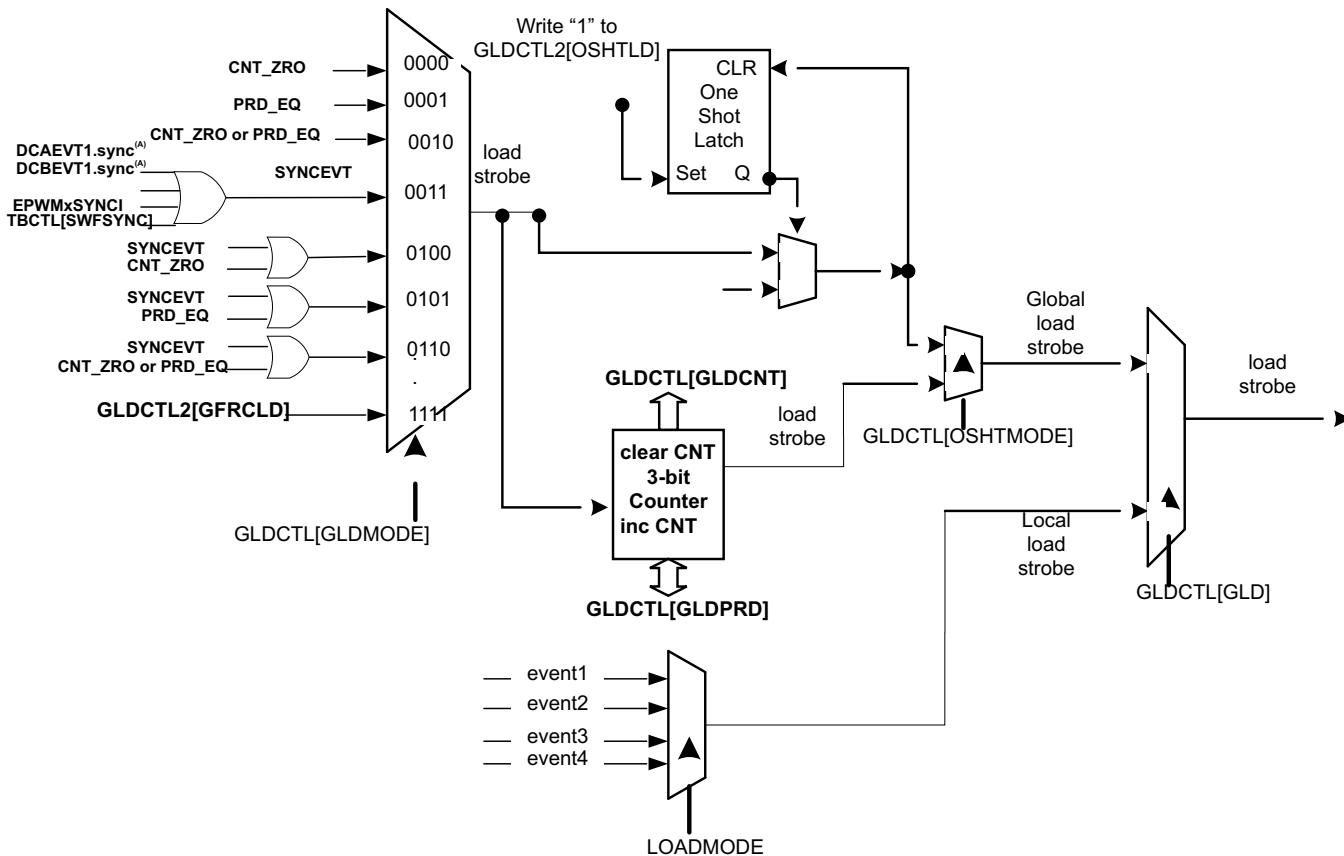
Figure 12-9. Time-Base Down-Count Mode Waveforms

Figure 12-10. Time-Base Up-Down-Count Waveforms, TBCTL[PHSDIR = 0] Count Down On Synchronization Event


Figure 12-11. Time-Base Up-Down Count Waveforms, TBCTL[PHSDIR = 1] Count Up On Synchronization Event



12.2.2.7 Global Reload

Figure 12-12 illustrates the signals and registers associated with the Global Reload feature.

Figure 12-12. Global Reload: Signals and Registers


When this feature is enabled, the transfer of contents from shadow register to active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL[GLDMODE]). When GLDCTL[GLD] = '1', shadow to active load event selection bits for individual shadowed registers are ignored and global load mode takes effect for the corresponding registers enabled by GLDCFG[REGx].

When GLDCTL[GLD] = '1' and GLDCFG[REGx] = '0' global load mode does not affect the corresponding register (REGx). Shadow to active load event selection bits for individual shadowed registers decide how the transfer of contents from shadow register to active register takes place.

12.2.2.7.1 Global Reload Pulse Pre-Scalar

This feature provides the capability to choose shadow to active transfers to happen once in 'N' occurrences of selected global reload pulse (GLDCTL[GLDMODE]). This pre-scale functionality is not available for registers that cannot or are not configured to use the global load mechanism (that is, GLDCTL[GLD] = '0' or GLDCFG[REGx] = '0').

12.2.2.7.2 One-Shot Reload Mode

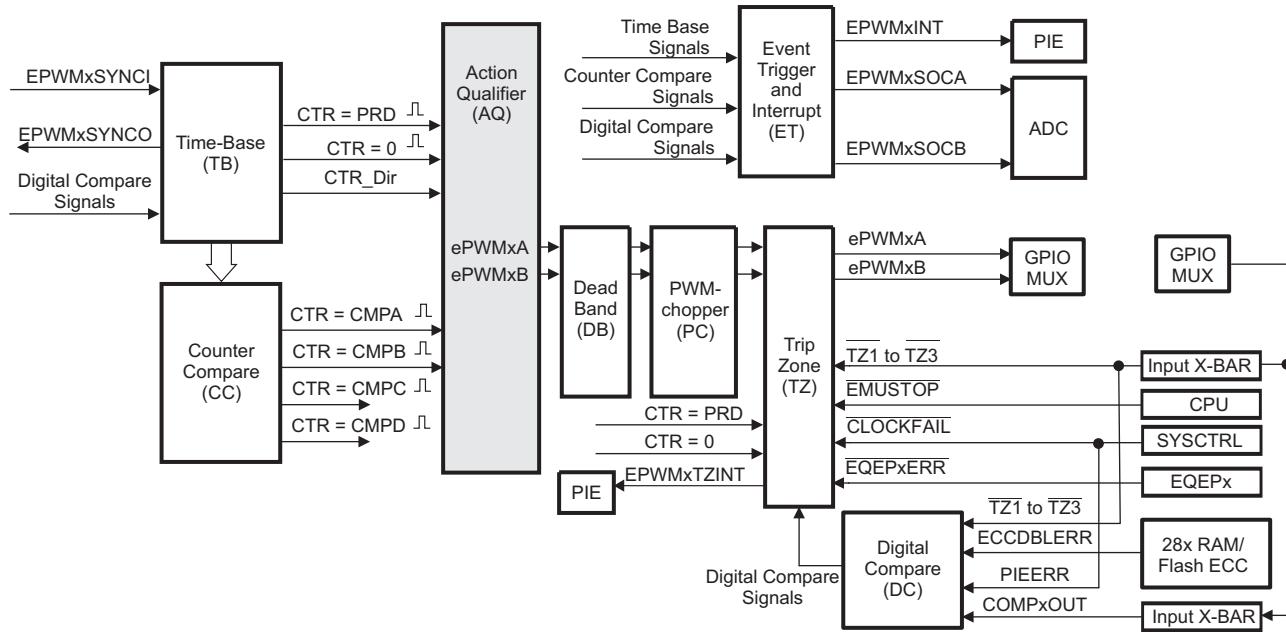
This feature allows users to cause shadow register to active register transfers to occur once. When GLDCTL2[OSHTLD] = '1' the shadow to active register transfer, for registers that are configured to use the global load mechanism, takes place on the event selected by GLDCTL[GLDMODE].

Software force loading of contents from shadow register to active register is possible by using GLDCTL2[GFRCLD]. The GLDCTL2 register can also be linked across multiple PWM modules by using EPWMXLINK[GLDCTL2LINK]. This, along with the one-shot reload mode feature discussed above, provides a method to correctly update multiple PWM registers in one or more PWM modules at certain PWM events or, if desired, in the same clock cycle. This is very useful in variable frequency applications and/or multi-phase interleaved applications.

12.2.3 Counter-Compare (CC) Submodule

Figure 12-13 illustrates the counter-compare submodule within the ePWM.

Figure 12-13. Counter-Compare Submodule



12.2.3.1 Purpose of the Counter-Compare Submodule

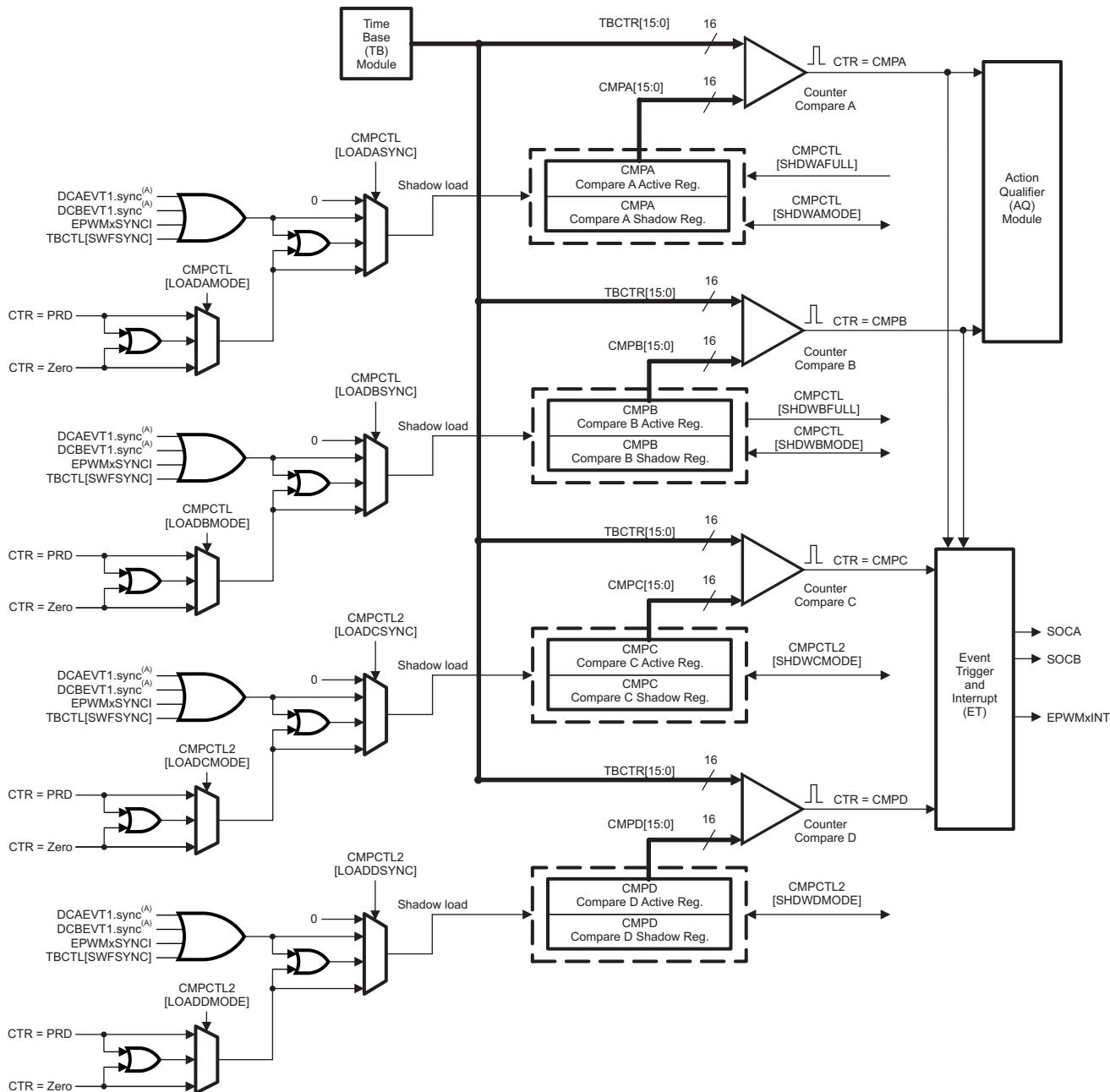
The counter-compare submodule takes as input the time-base counter value. This value is continuously compared to the counter-compare A (CMPA), counter-compare B (CMPB), counter-compare C (CMPC) and counter-compare D (CMPD) registers. When the time-base counter is equal to one of the compare registers, the counter-compare unit generates an appropriate event.

The counter-compare:

- Generates events based on programmable time stamps using the CMPA, CMPB, CMPC and CMPD registers
 - CTR = CMPA: Time-base counter equals counter-compare A register (TBCTR = CMPA).
 - CTR = CMPB: Time-base counter equals counter-compare B register (TBCTR = CMPB)
 - CTR = CMPC: Time-base counter equals counter-compare C register (TBCTR = CMPC).
 - CTR = CMPD: Time-base counter equals counter-compare D register (TBCTR = CMPD)
- Controls the PWM duty cycle if the action-qualifier submodule is configured appropriately using counter-compare A (CMPA) & counter-compare B (CMPB)
- Shadows new compare values to prevent corruption or glitches during the active PWM cycle

12.2.3.2 Controlling and Monitoring the Counter-Compare Submodule

The counter-compare submodule operation is shown in Figure 12-14.

Figure 12-14. Detailed View of the Counter-Compare Submodule


A These events are generated by the type 4 ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs [For Example: COMPxOUT and TZ signals].

12.2.3.3 Operational Highlights for the Counter-Compare Submodule

The counter-compare submodule is responsible for generating two independent compare events based on two compare registers, which is fed to action-qualifier submodule and Event Trigger submodule :

1. CTR = CMPA: Time-base counter equal to counter-compare A register (TBCTR = CMPA).
2. CTR = CMPB: Time-base counter equal to counter-compare B register (TBCTR = CMPB).

For up-count or down-count mode, each event occurs only once per cycle. For up-down-count mode each event occurs twice per cycle if the compare value is between 0x00-TBPRD and once per cycle if the compare value is equal to 0x00 or equal to TBPRD. These events are fed into the action-qualifier submodule where they are qualified by the counter direction and converted into actions if enabled. Refer to [Section 12.2.4.1](#) for more details.

The counter-compare registers CMPA and CMPB each have an associated shadow register. Shadowing provides a way to keep updates to the registers synchronized with the hardware. When shadowing is used, updates to the active registers only occur at strategic points. This prevents corruption or spurious operation due to the register being asynchronously modified by software. The memory address of the active register and the shadow register is identical. Which register is written to or read from is determined by the CMPCTL[SHDWAMODE] and CMPCTL[SHDWBMODE] bits. These bits enable and disable the CMPA shadow register and CMPB shadow register respectively. The behavior of the two load modes is described below:

Shadow Mode:

The shadow mode for the CMPA is enabled by clearing the CMPCTL[SHDWAMODE] bit and the shadow register for CMPB is enabled by clearing the CMPCTL[SHDWBMODE] bit. Shadow mode is enabled by default for both CMPA and CMPB.

If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events as specified by the CMPCTL[LOADAMODE] CMPCTL[LOADBMODE] CMPCTL[LOADASYNC] & CMPCTL[LOADBSYNC] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero
- SYNC event caused by DCAEVT1 or DCBEVT1 or EPWMxSYNC1 or TBCTL[SWFSYNC]
- Both SYNC event or a selection made by LOADAMODE/LOADBMODE

Only the active register contents are used by the counter-compare submodule to generate events to be sent to the action-qualifier.

Immediate Mode:

If immediate load mode is selected (that is, CMPCTL[SHDWAMODE] = 1 or CMPCTL[SHDWBMODE] = 1), then a read from or a write to the register will go directly to the active register.

Addtional Comparators

The counter-compare submodule on ePWMs type 2 and later are responsible for generating two additional independent compare events based on two compare registers, which is fed to Event Trigger submodule :

1. CTR = CMPC: Time-base counter equal to counter-compare C register (TBCTR = CMPC).
2. CTR = CMPD: Time-base counter equal to counter-compare D register (TBCTR = CMPD).

The counter-compare registers CMPC and CMPD each have an associated shadow register. By default this register is shadowed. The memory address of the active register and the shadow register is identical. The value in the active CMPC & CMPD register is compared to the time-base counter (TBCTR). When the values are equal, the counter compare module generates a “time-base counter equal to counter compare C or counter compare D” event respectively. Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWCMODE] and CMPCTL2[SHDWDMODE] bit. These bits enable and disable the CMPC shadow register and CMPD shadow register respectively. The behavior of the two load modes is described below:

Shadow Mode:

The shadow mode for the CMPC is enabled by clearing the CMPCTL2[SHDWCMODE] bit and the shadow register for CMPD is enabled by clearing the CMPCTL2[SHDWDMODE] bit. Shadow mode is enabled by default for both CMPC and CMPD.

If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events as specified by the CMPCTL2[LOADCMODE] CMPCTL2[LOADDMODE] CMPCTL2[LOADCSYNC] & CMPCTL2[LOADDSYNC] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero
- SYNC event caused by DCAEVT1 or DCBEVT1 or EPWMxSYNCI or TBCTL[SWFSYNC]
- Both SYNC event or a selection made by LOADCMODE/LOADDMODE

Only the active register contents are used by the counter-compare submodule to generate events to be sent to the action-qualifier.

Immediate Load Mode:

If immediate load mode is selected (i.e., CMPCTL2[SHDWCMODE] = 1 or CMPCTL2[SHDWDMODE] = 1), then a read from or a write to the register will go directly to the active register.

Global Reload Support

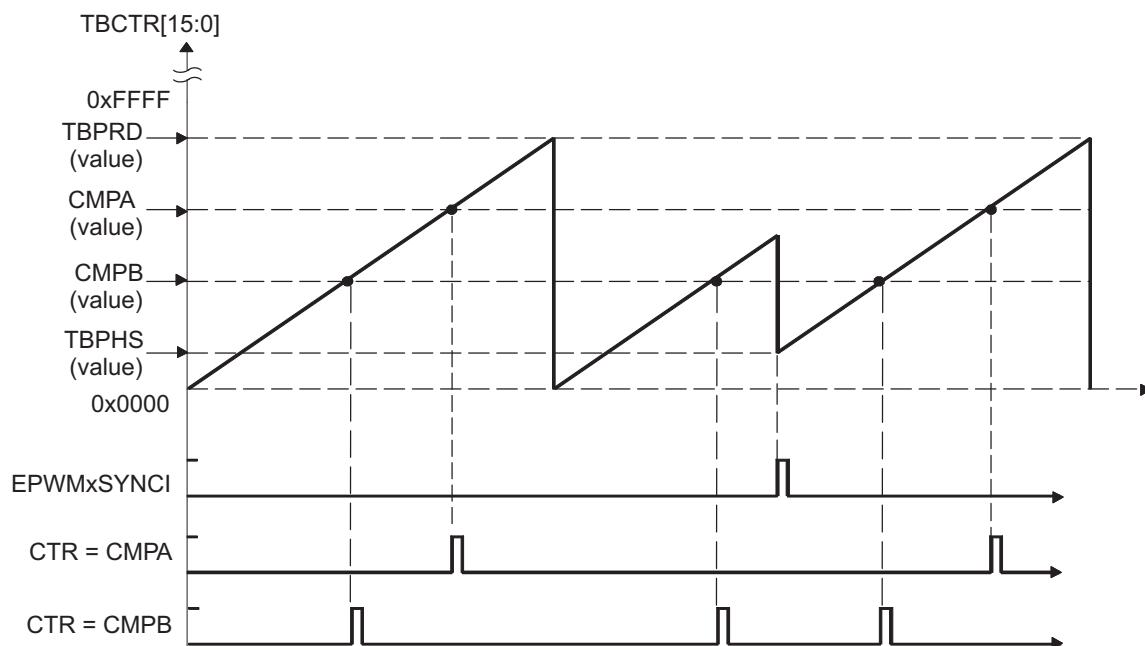
Global reload control mechanism can also be used for all counter-compare registers by configuring the appropriate bits in the global load configuration register (GLDCFG). When global reload mode is selected the transfer of contents from shadow register to active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL). Global reload control mechanism is explained in [Section 12.2.2.7](#).

12.2.3.4 Count Mode Timing Waveforms

The counter-compare module can generate compare events in all three count modes:

- Up-count mode: used to generate an asymmetrical PWM waveform.
- Down-count mode: used to generate an asymmetrical PWM waveform.
- Up-down-count mode: used to generate a symmetrical PWM waveform.

To best illustrate the operation of the first three modes, the timing diagrams in [Figure 12-15](#) through [Figure 12-18](#) show when events are generated and how the EPWMxSYNCI signal interacts.

Figure 12-15. Counter-Compare Event Waveforms in Up-Count Mode

NOTE: An EPWMxSYNCI external synchronization event can cause a discontinuity in the TBCTR count sequence. This can lead to a compare event being skipped. This skipping is considered normal operation and must be taken into account.

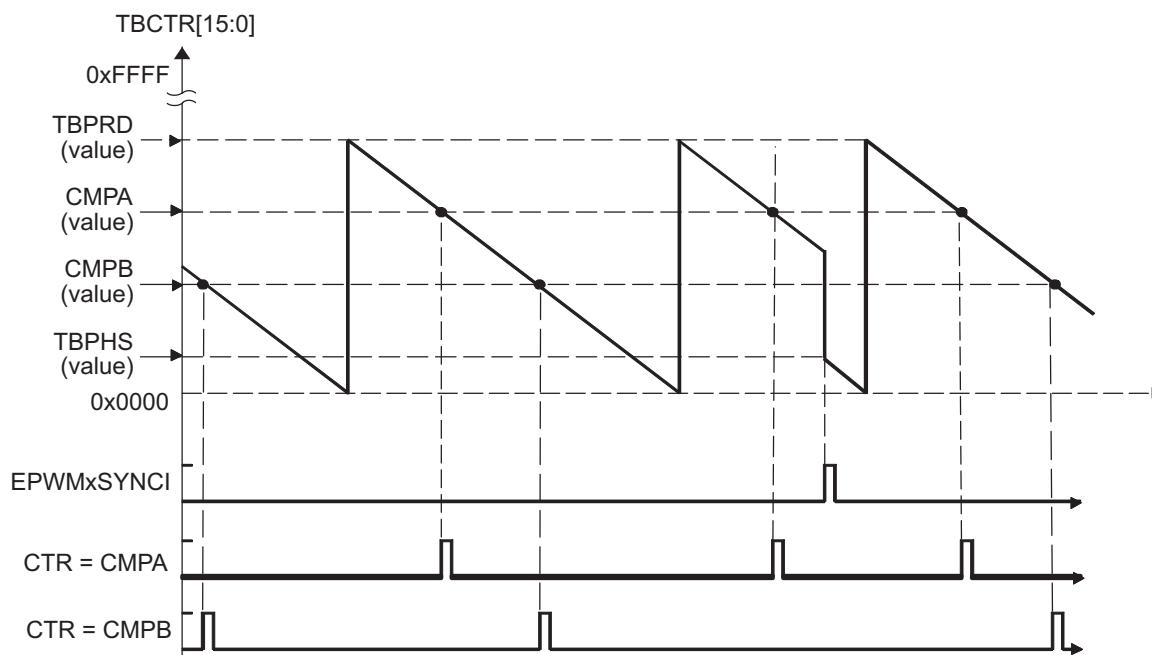
Figure 12-16. Counter-Compare Events in Down-Count Mode


Figure 12-17. Counter-Compare Events In Up-Down-Count Mode, TBCTL[PHSDIR = 0] Count Down On Synchronization Event

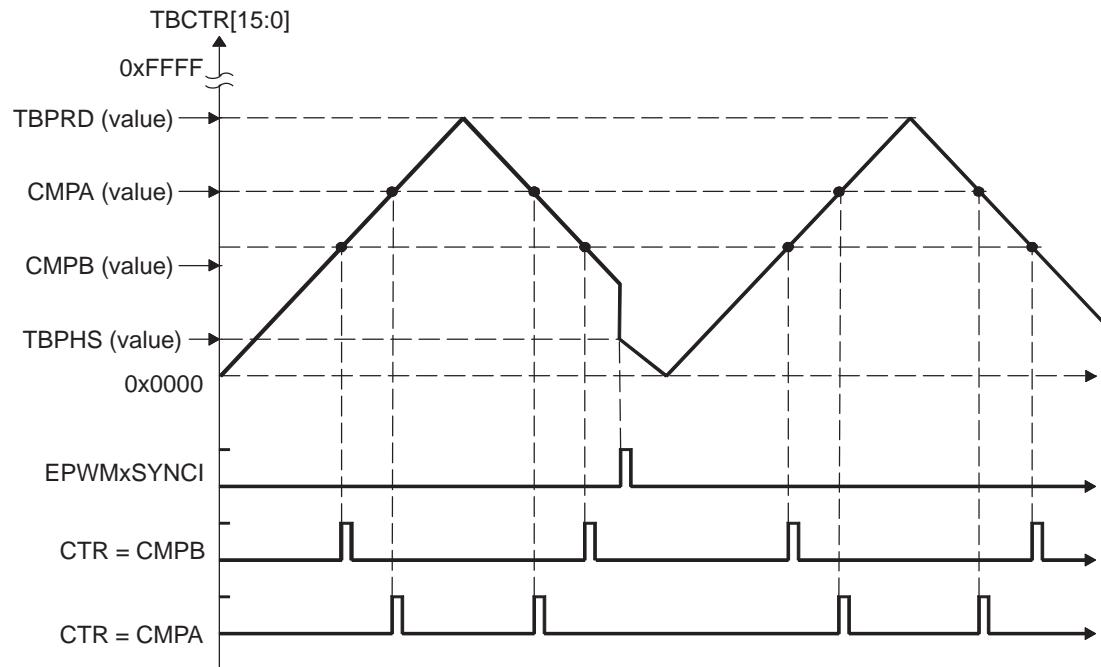
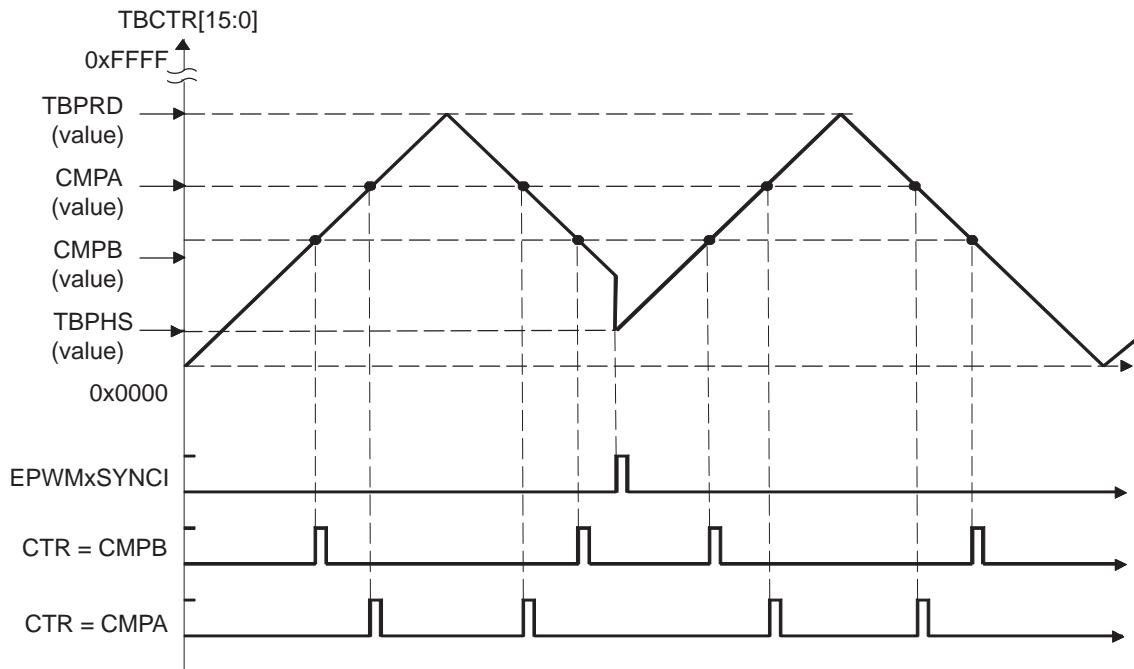
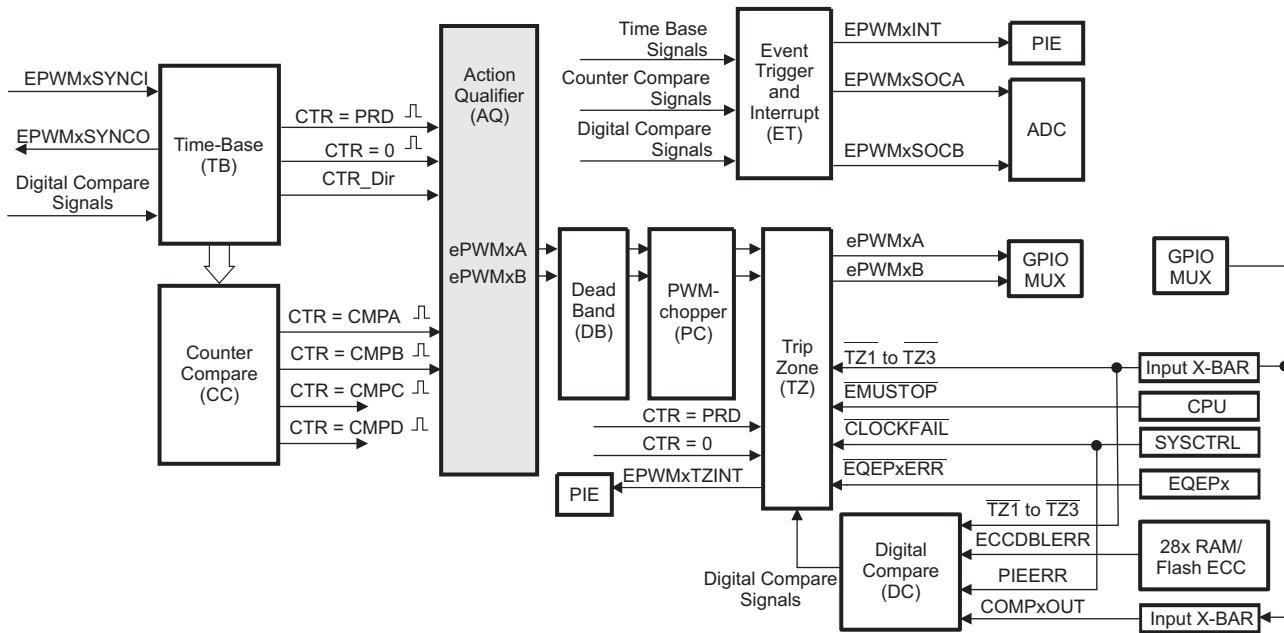


Figure 12-18. Counter-Compare Events In Up-Down-Count Mode, TBCTL[PHSDIR = 1] Count Up On Synchronization Event



12.2.4 Action-Qualifier (AQ) Submodule

Figure 12-19 shows the action-qualifier (AQ) submodule (see shaded block) in the ePWM system.

Figure 12-19. Action-Qualifier Submodule


The action-qualifier submodule has the most important role in waveform construction and PWM generation. It decides which events are converted into various action types, thereby producing the required switched waveforms at the EPWMxA and EPWMxB outputs.

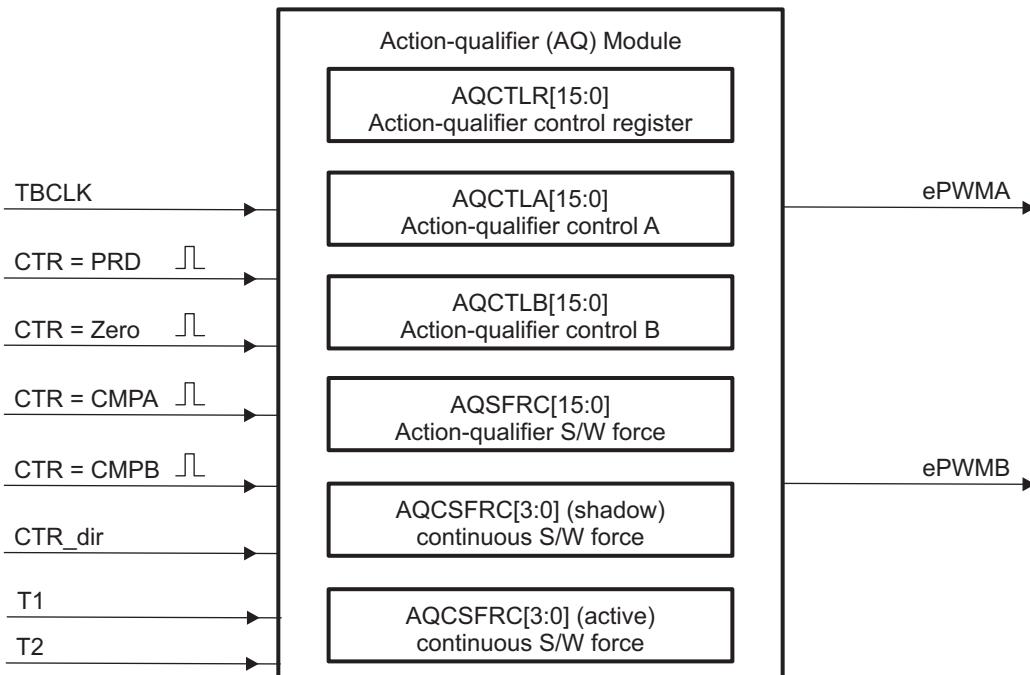
12.2.4.1 Purpose of the Action-Qualifier Submodule

The action-qualifier submodule is responsible for the following:

- Qualifying and generating actions (set, clear, toggle) based on the following events:
 - CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
 - CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
 - CTR = CMPA: Time-base counter equal to the counter-compare A register (TBCTR = CMPA)
 - CTR = CMPB: Time-base counter equal to the counter-compare B register (TBCTR = CMPB)
- T1, T2 events: Trigger events based on comparator, trip or syncin events
- Managing priority when these events occur concurrently
- Providing independent control of events when the time-base counter is increasing and when it is decreasing

12.2.4.2 Action-Qualifier Submodule Control and Status Register Definitions

The action-qualifier submodule operation is shown in [Figure 12-20](#) and monitored via the registers in .

Figure 12-20. Action-Qualifier Submodule Inputs and Outputs

For convenience, the possible input events are summarized again in [Table 12-3](#).

Table 12-3. Action-Qualifier Submodule Possible Input Events

Signal	Description	Registers Compared
CTR = PRD	Time-base counter equal to the period value	TBCTR = TBPRD
CTR = Zero	Time-base counter equal to zero	TBCTR = 0x00
CTR = CMPA	Time-base counter equal to the counter-compare A	TBCTR = CMPA
CTR = CMPB	Time-base counter equal to the counter-compare B	TBCTR = CMPB
T1 event	Based on comparator, trip or syncin events	None
T2 event	Based on comparator, trip or syncin events	None
Software forced event	Asynchronous event initiated by software	

The software forced action is a useful asynchronous event. This control is handled by registers AQSFRC and AQCSFRC.

The action-qualifier submodule controls how the two outputs EPWMxA and EPWMxB behave when a particular event occurs. The event inputs to the action-qualifier submodule are further qualified by the counter direction (up or down). This allows for independent action on outputs on both the count-up and count-down phases.

The possible actions imposed on outputs EPWMxA and EPWMxB are:

- **Set High:**
Set output EPWMxA or EPWMxB to a high level.
- **Clear Low:**
Set output EPWMxA or EPWMxB to a low level.
- **Toggle:**
If EPWMxA or EPWMxB is currently pulled high, then pull the output low. If EPWMxA or EPWMxB is currently pulled low, then pull the output high.
- **Do Nothing:**
Keep outputs EPWMxA and EPWMxB at same level as currently set. Although the "Do Nothing" option

prevents an event from causing an action on the EPWMxA and EPWMxB outputs, this event can still trigger interrupts and ADC start of conversion. See the Event-trigger Submodule description in [Section 12.2.8](#) for details.

Actions are specified independently for either output (EPWMxA or EPWMxB). Any or all events can be configured to generate actions on a given output. For example, both CTR = CMPA and CTR = CMPB can operate on output EPWMxA. All qualifier actions are configured via the control registers found at the end of this section.

For clarity, the drawings in this document use a set of symbolic actions. These symbols are summarized in [Figure 12-21](#). Each symbol represents an action as a marker in time. Some actions are fixed in time (zero and period) while the CMPA and CMPB actions are moveable and their time positions are programmed via the counter-compare A and B registers, respectively. To turn off or disable an action, use the "Do Nothing option"; it is the default at reset.

Figure 12-21. Possible Action-Qualifier Actions for EPWMxA and EPWMxB Outputs

S/W force	TB Counter equals							Actions
	Zero	Comp A	Comp B	Period	T1	T2		
								Do Nothing
								Clear Lo
								Set Hi
								Toggle

The Action Qualifier trigger event source selection register (AQTSRCSEL) is used to select the source for T1 and T2 events. T1/T2 selection and configuration of a trip/digital-compare event in Action Qualifier submodule is independent of the configuration of that event in Trip-Zone submodule. A particular trip event may or may not be configured to cause trip action in Trip Zone submodule, but the same event can be used by the Action Qualifier to generate T1/T2 for controlling PWM generation.

12.2.4.3 Action-Qualifier Event Priority

It is possible for the ePWM action qualifier to receive more than one event at the same time. In this case events are assigned a priority by the hardware. The general rule is events occurring later in time have a higher priority and software forced events always have the highest priority. The event priority levels for up-down-count mode are shown in [Table 12-4](#). A priority level of 1 is the highest priority and level 10 is the lowest. The priority changes slightly depending on the direction of TBCTR.

Table 12-4. Action-Qualifier Event Priority for Up-Down-Count Mode

Priority Level	Event If TBCTR is Incrementing TBCTR = Zero up to TBCTR = TBPRD	Event If TBCTR is Decrementing TBCTR = TBPRD down to TBCTR = 1
1 (Highest)	Software forced event	Software forced event
2	T1 on up-count (T1U)	T1 on down-count (T1D)
3	T2 on up-count (T2U)	T2 on down-count (T2D)
4	Counter equals CMPB on up-count (CBU)	Counter equals CMPB on down-count (CBD)
5	Counter equals CMPA on up-count (CAU)	Counter equals CMPA on down-count (CAD)
6	Counter equals zero	Counter equals period (TBPRD)
7	T1 on down-count (T1D)	T1 on up-count (T1U)
8	T2 on down-count (T2D)	T2 on up-count (T2U)
9	Counter equals CMPB on down-count (CBD)	Counter equals CMPB on up-count (CBU)
10 (Lowest)	Counter equals CMPA on down-count (CAD)	Counter equals CMPA on up-count (CBU)

[Table 12-5](#) shows the action-qualifier priority for up-count mode. In this case, the counter direction is always defined as up and thus down-count events will never be taken.

Table 12-5. Action-Qualifier Event Priority for Up-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to period (TBPRD)
3	T1 on up-count (T1U)
4	T2 on up-count (T2U)
5	Counter equal to CMPB on up-count (CBU)
6	Counter equal to CMPA on up-count (CAU)
7 (Lowest)	Counter equal to Zero

[Table 12-6](#) shows the action-qualifier priority for down-count mode. In this case, the counter direction is always defined as down and thus up-count events will never be taken.

Table 12-6. Action-Qualifier Event Priority for Down-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to Zero
3	T1 on down-count (T1D)
4	T2 on down-count (T2D)
3	Counter equal to CMPB on down-count (CBD)
4	Counter equal to CMPA on down-count (CAD)
5 (Lowest)	Counter equal to period (TBPRD)

It is possible to set the compare value greater than the period. In this case the action will take place as shown in [Table 12-7](#).

Table 12-7. Behavior if CMPA/CMPB is Greater than the Period

Counter Mode	Compare on Up-Count Event CAD/CBD	Compare on Down-Count Event CAD/CBD
Up-Count Mode	If $CMPA/CMPB \leq TBPRD$ period, then the event occurs on a compare match ($TBCTR=CMPA$ or $CMPB$). If $CMPA/CMPB > TBPRD$, then the event will not occur.	Never occurs.
	Down-Count Mode	Never occurs. If $CMPA/CMPB < TBPRD$, the event will occur on a compare match ($TBCTR=CMPA$ or $CMPB$). If $CMPA/CMPB \geq TBPRD$, the event will occur on a period match ($TBCTR=TBPRD$). If $CMPA/CMPB < TBPRD$ and the counter is incrementing, the event occurs on a compare match ($TBCTR=CMPA$ or $CMPB$). If $CMPA/CMPB \geq TBPRD$, the event will occur on a period match ($TBCTR = TBPRD$).
Up-Down-Count Mode	If $CMPA/CMPB < TBPRD$ and the counter is incrementing, the event occurs on a compare match ($TBCTR=CMPA$ or $CMPB$). If $CMPA/CMPB \geq TBPRD$, the event will occur on a period match ($TBCTR = TBPRD$).	If $CMPA/CMPB < TBPRD$ and the counter is decrementing, the event occurs on a compare match ($TBCTR=CMPA$ or $CMPB$). If $CMPA/CMPB \geq TBPRD$, the event occurs on a period match ($TBCTR=TBPRD$).

12.2.4.4 AQCTLA and AQCTLB Shadow Mode Operations

To enable Action Qualifier mode changes which must occur at the end of a period even when the phase changes, shadowing of the AQCTLA and AQCTLB registers has been added on ePWMS type 2 and later. Additionally, shadow to active load on SYNC of these registers is supported as well. Shadowing of this register is enabled and disabled by the AQCTLR[SHDWAQAMODE] and AQCTLR[SHDWAQBMODE] bits. These bits enable and disable the AQCTLA shadow register and AQCTLB shadow register, respectively. The behavior of the two load modes is described below:

Shadow Mode:

The shadow mode for the AQCTLA is enabled by setting the AQCTLR[SHDWAQAMODE] bit, and the shadow register for AQCTLB is enabled by setting the AQCTLR[SHDWAQBMODE] bit. Shadow mode is disabled by default for both AQCTLA and AQCTLB

If the shadow register is enabled, then the content of the shadow register is transferred to the active register on one of the following events as specified by the AQCTLR[LDAQAMODE] AQCTLR[LDAQBMODE] AQCTLR[LDAQASYNC] & AQCTLR[LDAQBSYNC] register bits:

- CTR = PRD: Time-base counter equal to the period ($TBCTR = TBPRD$).
- CTR = Zero: Time-base counter equal to zero ($TBCTR = 0x00$)
- Both CTR = PRD and CTR = Zero
- SYNC event caused by DCAEVT1 or DCBEVT1 or EPWMxSYNC1 or TBCTL[SWFSYNC]
- Both SYNC event or a selection made by LDAQAMODE/LDAQBMODE

Global Reload Support

Global reload control mechanism can also be used for AQCTLA:AQCTLA2, AQCTLB:AQCTLB2 and AQCSFRC registers by configuring the appropriate bits in the global load configuration register (GLDCFG). When global reload mode is selected the transfer of contents from shadow register to active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL). Global reload control mechanism is explained in [Section 12.2.2.7](#).

Immediate Load Mode:

If immediate load mode is selected (i.e., AQCTLR[SHDWAQAMODE] = 0 or AQCTLR[SHDWAQBMODE] = 0), then a read from or a write to the register will go directly to the active register. See [Figure 12-22](#) and [Figure 12-23](#).

NOTE: Shadow to Active Load of Action Qualifier Output A/B Control Register [AQCTLA & AQCTLB] on CMPA = 0 or CMPB = 0 boundary

If the Counter-Compare A Register (CMPA) or Counter-Compare B Register (CMPB) is set to a value of 0 and the action qualifier action on AQCTLA and AQCTLB is configured to occur in the same instant as a shadow to active load (i.e., CMPA=0 and AQCTLA shadow to active load on TBCTR=0 using AQCTLR register LDAQAMODE and LDAQAMODE bits), then both events enter contention and it is recommended to use a Non-Zero Counter-Compare when using Shadow to Active Load of Action Qualifier Output A/B Control Register on TBCTR = 0 boundary.

Figure 12-22. AQCTLR[SHDWAQAMODE]

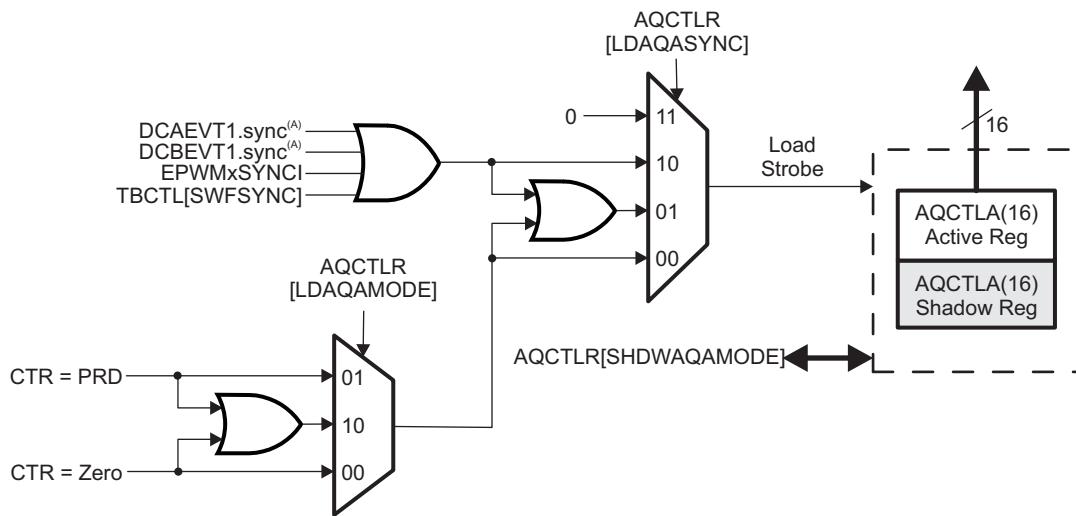
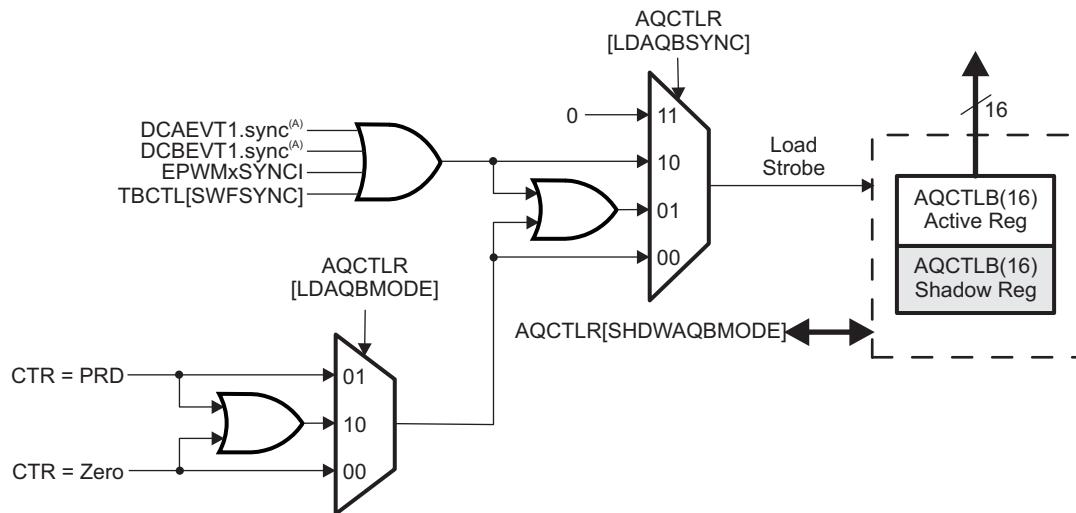


Figure 12-23. AQCTLR[SHDWAQBMODE]



12.2.4.5 Waveforms for Common Configurations

NOTE: The waveforms in this document show the ePWMS behavior for a static compare register value. In a running system, the active compare registers (CMPA and CMPB) are typically updated from their respective shadow registers once every period. The user specifies when the update will take place; either when the time-base counter reaches zero or when the time-base counter reaches period. There are some cases when the action based on the new value can be delayed by one period or the action based on the old value can take effect for an extra period. Some PWM configurations avoid this situation. These include, but are not limited to, the following:

Use up-down-count mode to generate a symmetric PWM:

- If you load CMPA/CMPB on zero, then use CMPA/CMPB values greater than or equal to 1.
- If you load CMPA/CMPB on period, then use CMPA/CMPB values less than or equal to TBPRD-1.

This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

Use up-down-count mode to generate an asymmetric PWM:

- To achieve 50%-0% asymmetric PWM use the following configuration: Load CMPA/CMPB on period and use the period action to clear the PWM and a compare-up action to set the PWM. Modulate the compare value from 0 to TBPRD to achieve 50%-0% PWM duty.

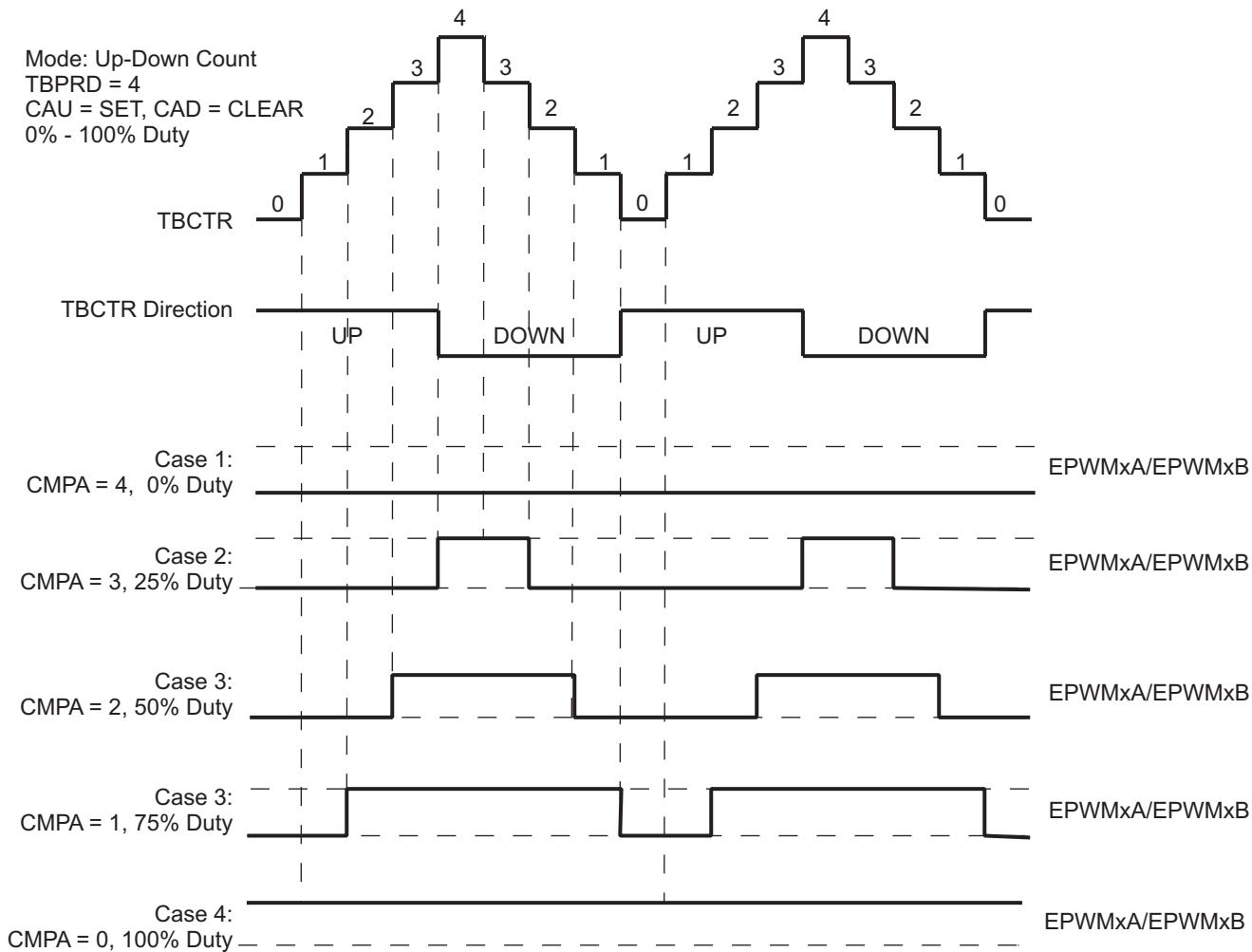
When using up-count mode to generate an asymmetric PWM:

- To achieve 0-100% asymmetric PWM use the following configuration: Load CMPA/CMPB on TBPRD. Use the Zero action to set the PWM and a compare-up action to clear the PWM. Modulate the compare value from 0 to TBPRD+1 to achieve 0-100% PWM duty.

See the *Using Enhanced Pulse Width Modulator (ePWM) Module for 0-100% Duty Cycle Control Application Report* (literature number [SPRAA11](#))

[Figure 12-24](#) shows how a symmetric PWM waveform can be generated using the up-down-count mode of the TBCTR. In this mode 0%-100% DC modulation is achieved by using equal compare matches on the up count and down count portions of the waveform. In the example shown, CMPA is used to make the comparison. When the counter is incrementing the CMPA match will pull the PWM output high. Likewise, when the counter is decrementing the compare match will pull the PWM signal low. When CMPA = 0, the PWM signal is low for the entire period giving the 0% duty waveform. When CMPA = TBPRD, the PWM signal is high achieving 100% duty.

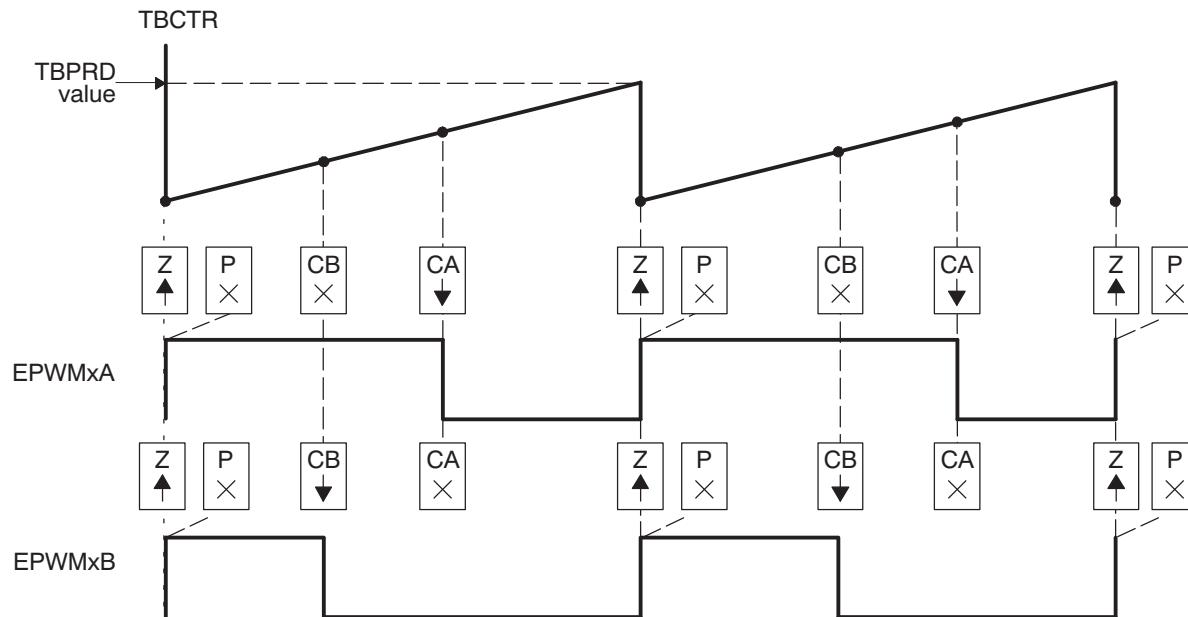
When using this configuration in practice, if you load CMPA/CMPB on zero, then use CMPA/CMPB values greater than or equal to 1. If you load CMPA/CMPB on period, then use CMPA/CMPB values less than or equal to TBPRD-1. This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

Figure 12-24. Up-Down-Count Mode Symmetrical Waveform

The PWM waveforms in [Figure 12-25](#) through [Figure 12-30](#) show some common action-qualifier configurations. Some conventions used in the figures and examples are as follows:

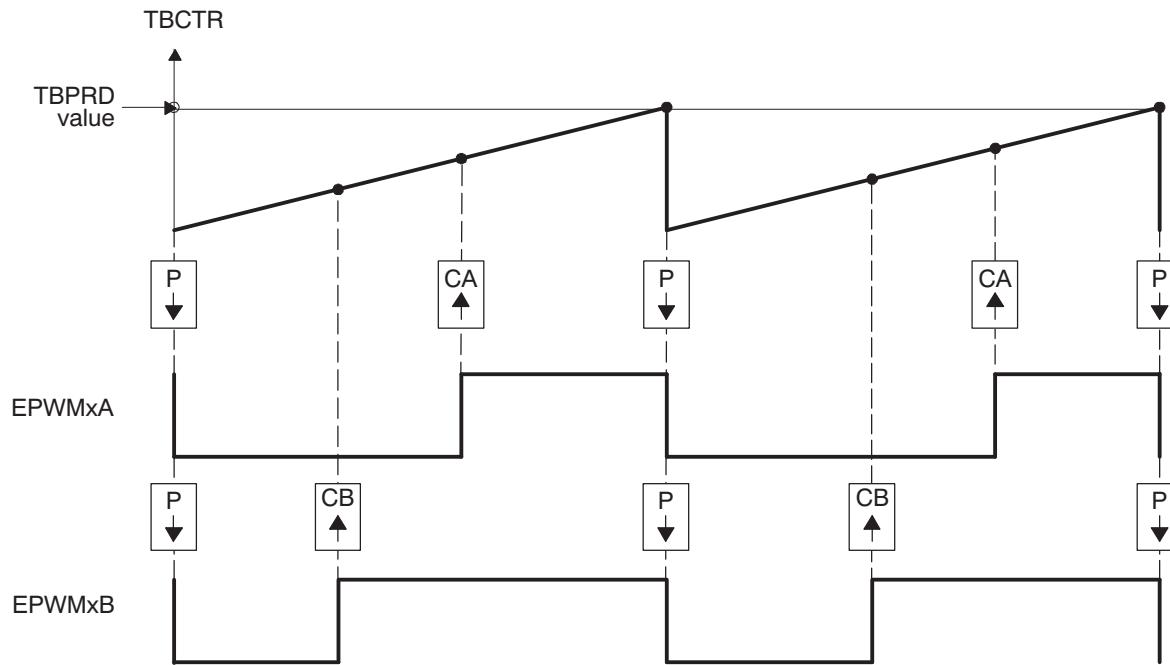
- TBPRD, CMPA, and CMPB refer to the value written in their respective registers. The active register, not the shadow register, is used by the hardware.
- CMPx, refers to either CMPA or CMPB.
- EPWMxA and EPWMxB refer to the output signals from ePWMx
- Up-Down means Count-up-and-down mode, Up means up-count mode and Dwn means down-count mode
- Sym = Symmetric, Asym = Asymmetric

Figure 12-25. Up, Single Edge Asymmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB—Active High



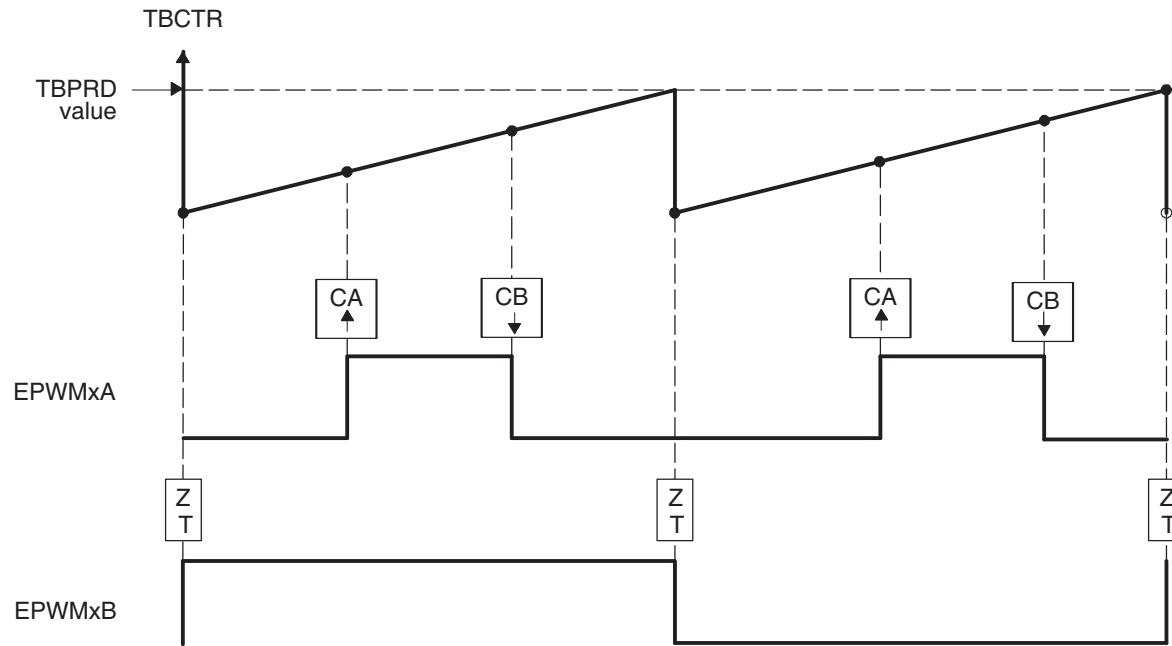
- A PWM period = $(TBPRD + 1) \times T_{TBCLK}$
- B Duty modulation for EPWMxA is set by CMPA, and is active high (that is, high time duty proportional to CMPA).
- C Duty modulation for EPWMxB is set by CMPB and is active high (that is, high time duty proportional to CMPB).
- D The "Do Nothing" actions (X) are shown for completeness, but will not be shown on subsequent diagrams.
- E Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCTR wraps from period to 0000.

Figure 12-26. Up, Single Edge Asymmetric Waveform With Independent Modulation on EPWMxA and EPWMxB—Active Low



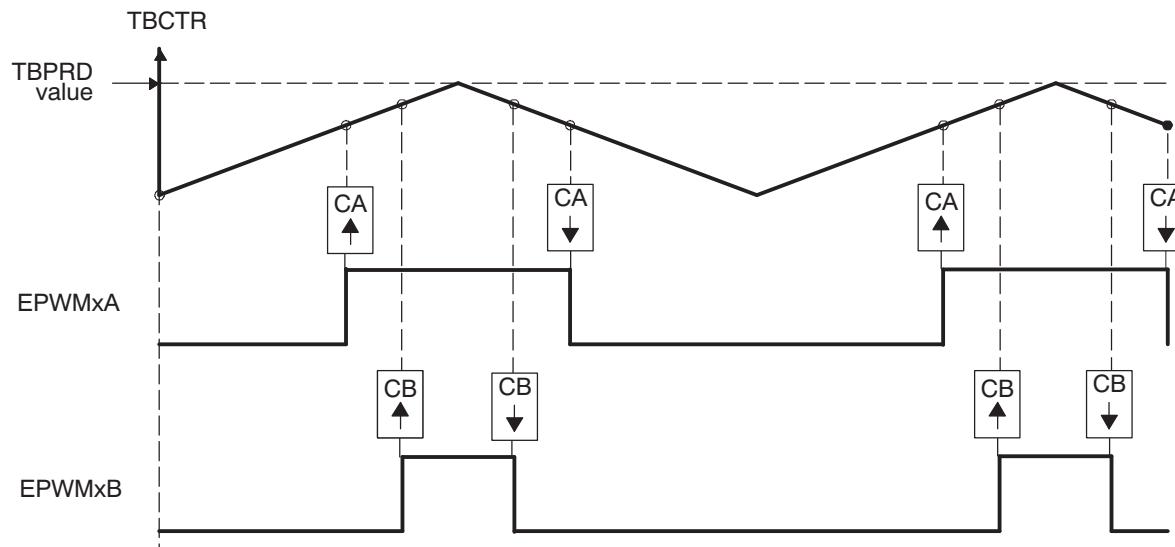
- A PWM period = $(TBPRD + 1) \times T_{TBCLK}$
- B Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).
- C Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).
- D Actions at zero and period, although appearing to occur concurrently, are actually separated by one T_{TBCLK} period. TBCTR wraps from period to 0000.

Figure 12-27. Up-Count, Pulse Placement Asymmetric Waveform With Independent Modulation on EPWMxA



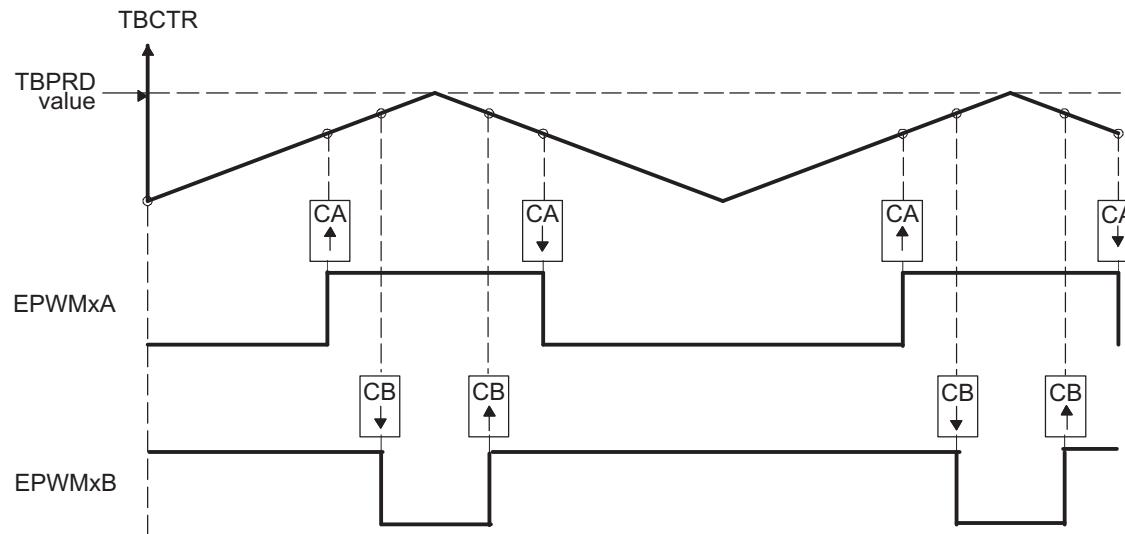
- A PWM frequency = $1 / ((TBPRD + 1) \times T_{TBCLK})$
- B Pulse can be placed anywhere within the PWM cycle (0000 - TBPRD)
- C High time duty proportional to (CMPB - CMPA)

Figure 12-28. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Active Low



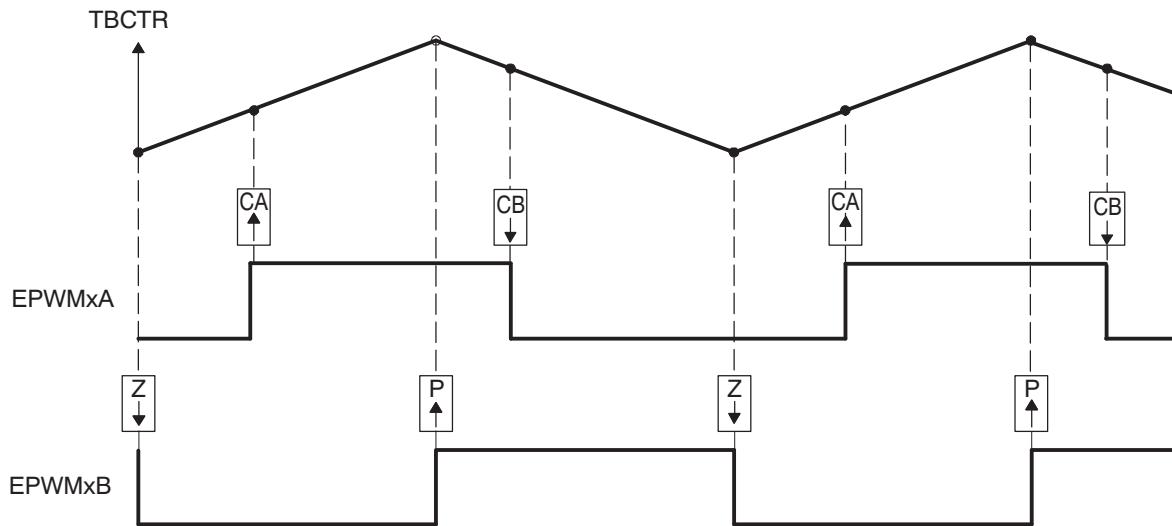
- A PWM period = $2 \times \text{TBPRD} \times T_{\text{TBCLK}}$
- B Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).
- C Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).
- D Outputs EPWMxA and EPWMxB can drive independent power switches

Figure 12-29. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Complementary



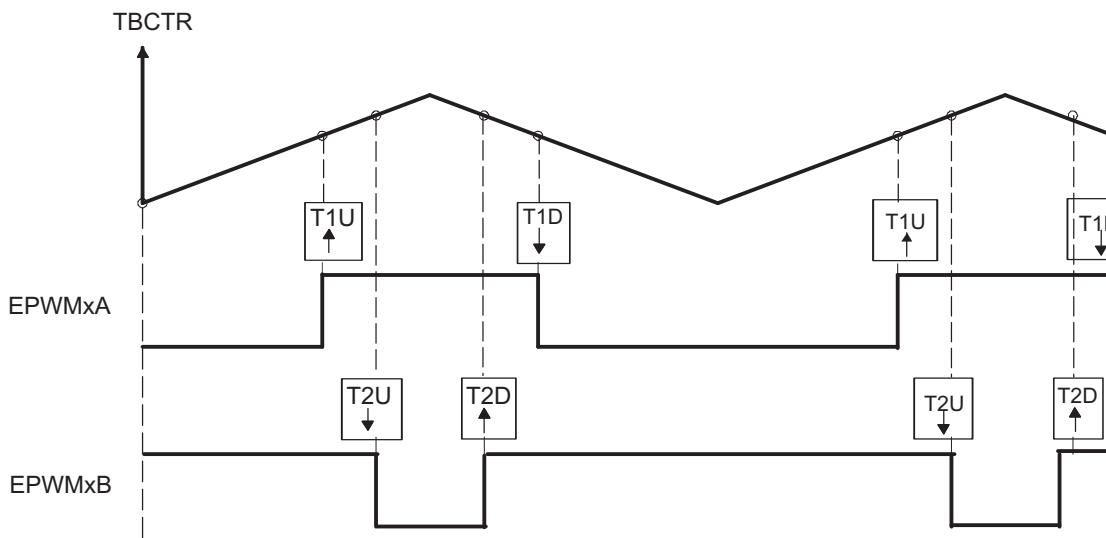
- A PWM period = $2 \times \text{TBPRD} \times T_{\text{TBCLK}}$
- B Duty modulation for EPWMxA is set by CMPA, and is active low, i.e., low time duty proportional to CMPA
- C Duty modulation for EPWMxB is set by CMPB and is active high, i.e., high time duty proportional to CMPB
- D Outputs EPWMx can drive upper/lower (complementary) power switches
- E Dead-band = CMPB - CMPA (fully programmable edge placement by software). Note the dead-band module is also available if the more classical edge delay method is required.

Figure 12-30. Up-Down-Count, Dual Edge Asymmetric Waveform, With Independent Modulation on EPWMxA—Active Low



- A PWM period = $2 \times \text{TBPRD} \times \text{TBCLK}$
- B Rising edge and falling edge can be asymmetrically positioned within a PWM cycle. This allows for pulse placement techniques.
- C Duty modulation for EPWMxA is set by CMPA and CMPB.
- D Low time duty for EPWMxA is proportional to $(\text{CMPA} + \text{CMPB})$.
- E To change this example to active high, CMPA and CMPB actions need to be inverted (that is, Clear on CMPA, Set on CMPB).
- F Duty modulation for EPWMxB is fixed at 50% (utilizes spare action resources for EPWMxB)

Figure 12-31. Up-Down-Count, PWM Waveform Generation Utilizing T1 and T2 Events

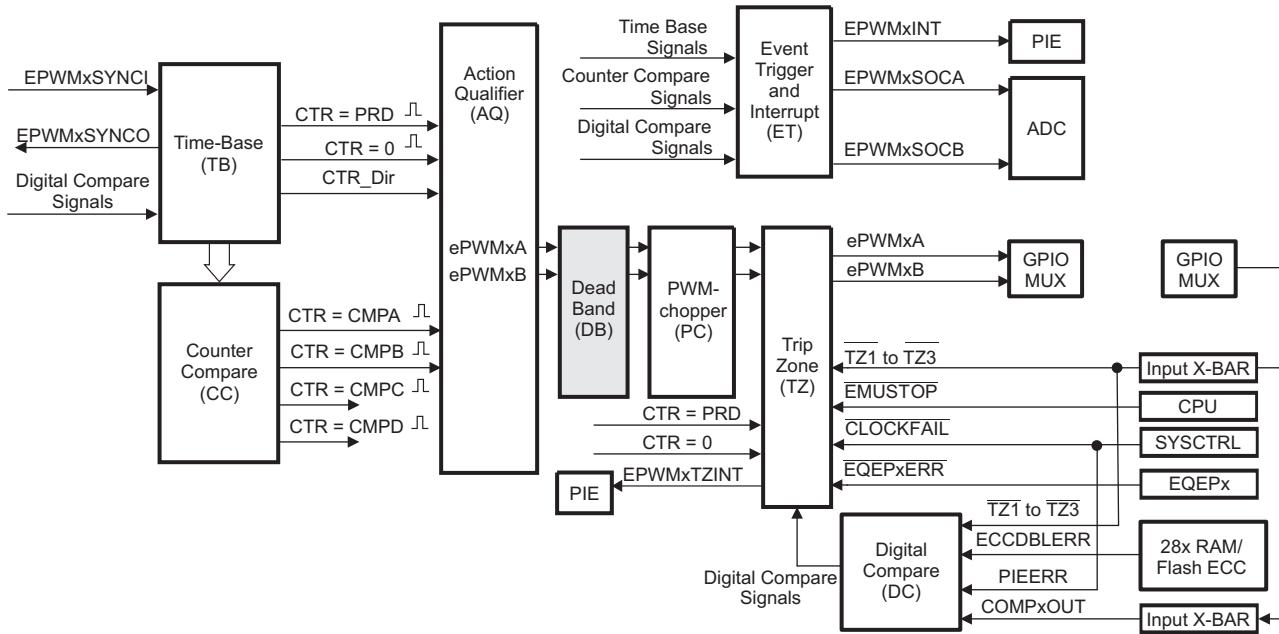


- A PWM period = $2 \times \text{TBPRD} \times \text{TTBCLK}$
- B Independent T1 event actions when counter is counting up and when it is counting down are used to generate EPWMxA output
- C Independent T2 event actions when counter is counting up and when it is counting down are used to generate EPWMxB output
- D TZ1 is selected as the source for T1
- E TZ2 is selected as the source for T2

12.2.5 Dead-Band Generator (DB) Submodule

Figure 12-32 illustrates the dead-band submodule within the ePWM module.

Figure 12-32. Dead_Band Submodule



12.2.5.1 Purpose of the Dead-Band Submodule

The Action-qualifier (AQ) Module section discussed how it is possible to generate the required dead-band by having full control over edge placement using both the CMPA and CMPB resources of the ePWM module. However, if the more classical edge delay-based dead-band with polarity control is required, then the dead-band submodule described here should be used.

The key functions of the dead-band module are:

- Generating appropriate signal pairs (EPWMxA and EPWMxB) with dead-band relationship from a single EPWMxA input
- Programming signal pairs for:
 - Active high (AH)
 - Active low (AL)
 - Active high complementary (AHC)
 - Active low complementary (ALC)
- Adding programmable delay to rising edges (RED)
- Adding programmable delay to falling edges (FED)
- Can be totally bypassed from the signal path (note dotted lines in diagram)

12.2.5.2 Dead band Submodule Additional Operating Modes

On type 1 ePWM RED could appear on one channel output and FED could appear on the other channel output.

The following list shows the distinct difference between type 1 and type 4 modules with respect to Dead Band operating modes

1. By adding S6, S7, and S8 in Figure 12-33, RED and FED can appear on both the A-channel and B-channel outputs. Additionally, both RED and FED together can be applied to either the A-channel or B-channel outputs to allow B-channel phase shifting with respect to the A-channel. Note: Phase shifting B-channel with respect to the A-channel using the dead-band submodule additional operating modes

- has limitations with respect to the choice of RED and FED delay with respect to the operating duty cycle of the ePWMxA and ePWMxB outputs.
2. The dead-band counters have also been increased to 14-bits
 3. Dead-band and dead-band High-resolution registers are now shadowed.
 4. High-resolution dead-band RED and FED have been enabled using the DBREDHR and DBFEDHR registers

NOTE: The PWM-Chopper will not be enabled when high-resolution dead-band is enabled

NOTE: High-resolution deadband RED and FED requires Half-Cycle clocking mode (DBCTL[HALFCYCLE] = 1).

Cannot have both RED and FED together applied to both ePWMxA and ePWMxB. RED and FED together can be applied only to either OutA OR OutB.

NOTE: Phase shifting B-channel with respect to the A-channel: When PWMxB is derived from PWMxA using the DEDB_MODE bit and by delaying rising edge and falling edge by the phase shift amount. When the duty cycle value on PWMxA is less than this phase shift amount, PWMxA's falling edge has precedence over the delayed rising edge for PWMxB. It is recommended to make sure the duty cycle value of the current waveform fed to the Dead band module is greater than the required phase shift amount.

Shadow Mode:

The shadow mode for the DBRED is enabled by setting the DBCTL[SHDWDBREDMODE] bit and the shadow register for DBFED is enabled by setting the DBCTL [SHDWDBFEDMODE] bit. Shadow mode is disabled by default for both DBRED and DBFED

If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events as specified by the DBCTL [LOADREDMODE] & DBCTL [LOADFEDMODE] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero

The DBCTL register can be shadowed. The shadow mode for DBCTL is enabled by setting the DBCTL2[SHDWDBCTLMODE] bit. If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events as specified by the DBCTL2[LOADDBCTLMODE] register bit:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero

Global Reload Support

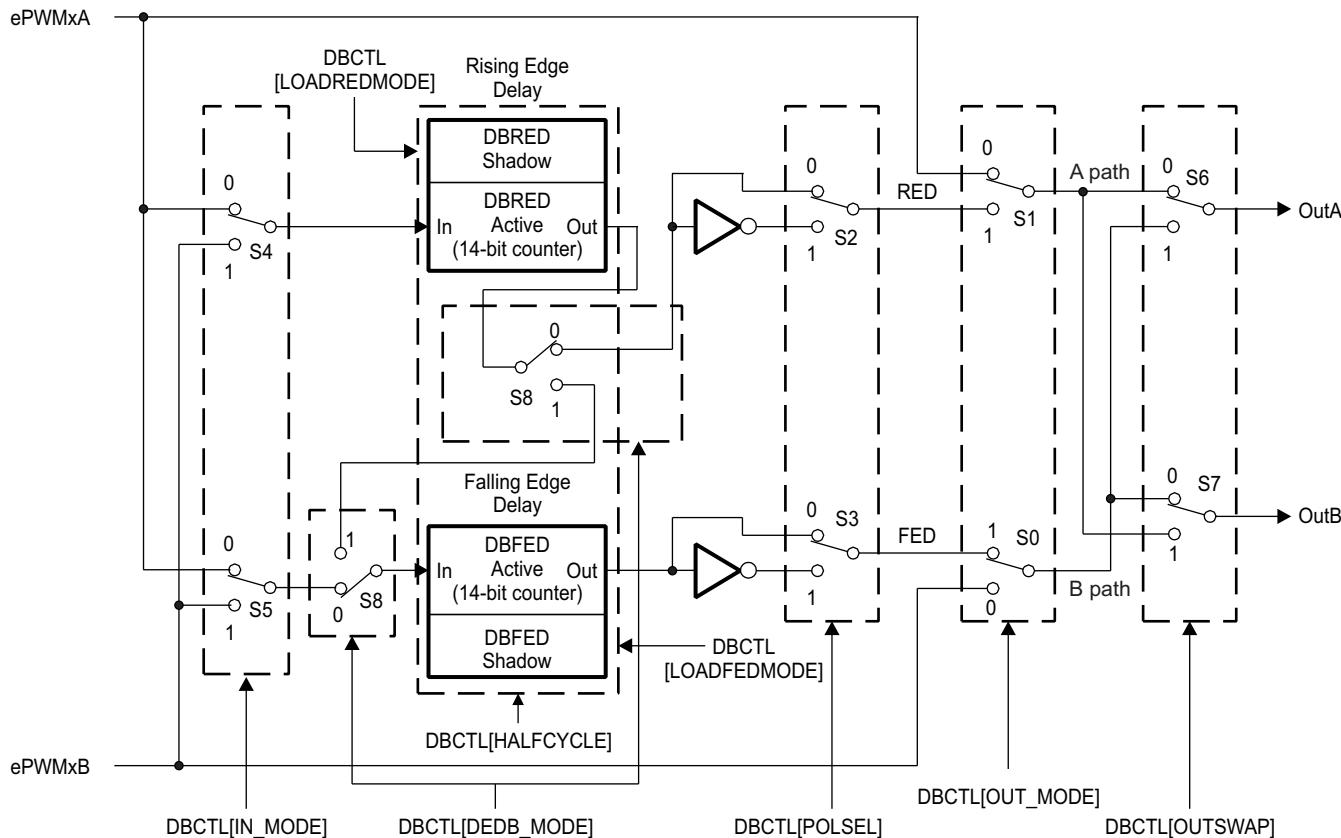
Global reload control mechanism can also be used for DBRED:DBREDHR, DBFED:DBFEDHR and DBCTL registers by configuring the appropriate bits in the global load configuration register (GLDCFG). When global reload mode is selected the transfer of contents from shadow register to active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL). The Global reload control mechanism is explained in [Section 12.2.2.7](#).

NOTE: When DBRED/DBFED active is loaded with a new shadow value while DB counters are counting, the new DBRED / DBFED value only affects the NEXT PWMx edge and not the current edge.

12.2.5.3 Operational Highlights for the Dead-Band Submodule

The configuration options for the dead-band submodule are shown in [Figure 12-33](#).

Figure 12-33. Configuration Options for the Dead-Band Submodule



Although all combinations are supported, not all are typical usage modes. [Table 12-8](#) documents some classical dead-band configurations. These modes assume that the DBCTL[IN_MODE] is configured such that EPWMxA In is the source for both falling-edge and rising-edge delay. Enhanced, or non-traditional modes can be achieved by changing the input signal source. The modes shown in [Table 12-8](#) fall into the following categories:

- Mode 1: Bypass both falling-edge delay (FED) and rising-edge delay (RED)**
Allows you to fully disable the dead-band submodule from the PWM signal path.
- Mode 2-5: Classical Dead-Band Polarity Settings:**

These represent typical polarity configurations that should address all the active high/low modes required by available industry power switch gate drivers. The waveforms for these typical cases are shown in [Figure 12-34](#). Note that to generate equivalent waveforms to [Figure 12-34](#), configure the action-qualifier submodule to generate the signal as shown for EPWMxA.

- Mode 6: Bypass rising-edge-delay and Mode 7: Bypass falling-edge-delay**

Finally the last two entries in [Table 12-8](#) show combinations where either the falling-edge-delay (FED) or rising-edge-delay (RED) blocks are bypassed.

Table 12-8. Classical Dead-Band Operating Modes

Mode	Mode Description	DBCTL[POLSEL]		DBCTL[OUT_MODE]	
		S3	S2	S1	S0
1	EPWMxA and EPWMxB Passed Through (No Delay)	X	X	0	0
2	Active High Complementary (AHC)	1	0	1	1
3	Active Low Complementary (ALC)	0	1	1	1

Table 12-8. Classical Dead-Band Operating Modes (continued)

Mode	Mode Description	DBCTL[POLSEL]		DBCTL[OUT_MODE]	
		S3	S2	S1	S0
4	Active High (AH)	0	0	1	1
5	Active Low (AL)	1	1	1	1
6	EPWMxA Out = EPWMxA In (No Delay) EPWMxB Out = EPWMxA In with Falling Edge Delay	0 or 1	0 or 1	0	1
7	EPWMxA Out = EPWMxA In with Rising Edge Delay EPWMxB Out = EPWMxB In with No Delay	0 or 1	0 or 1	1	0

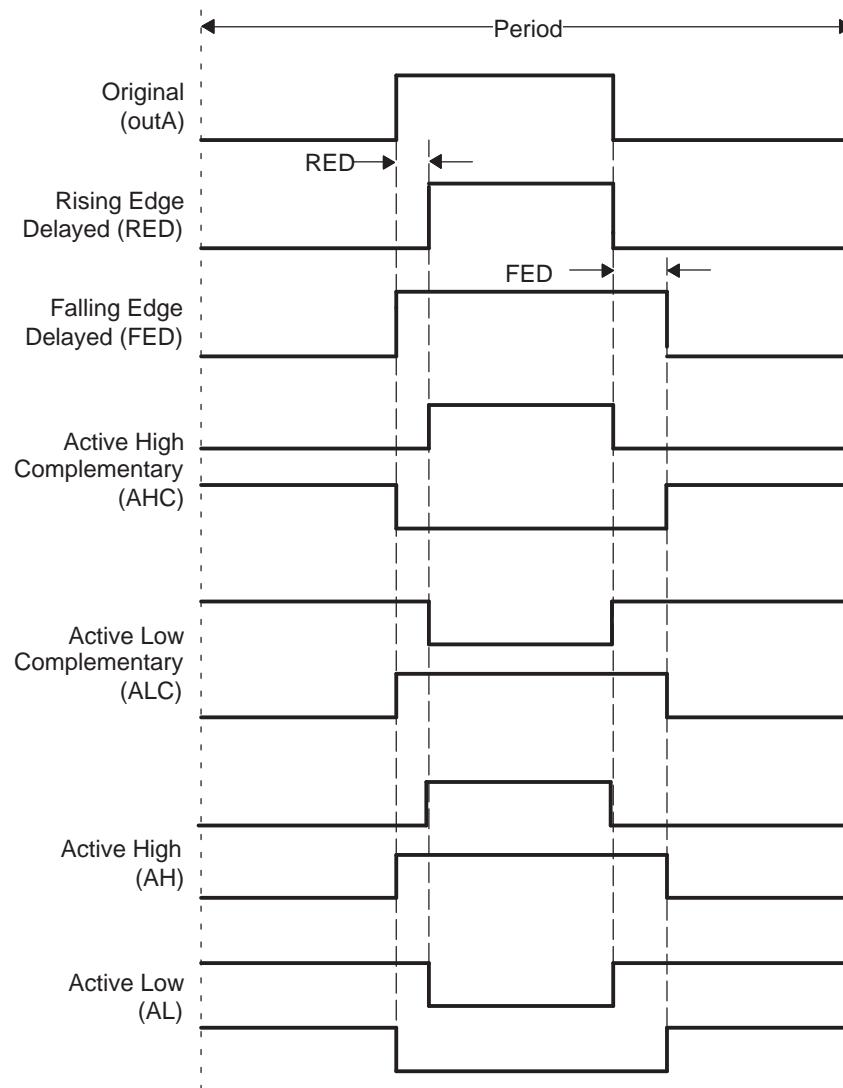
Table 12-9. Additional Dead-Band Operating Modes

Mode Description	DBCTL[DEDB-MODE]		DBCTL[OUTSWAP]	
	S8	S6	S6	S7
EPWMxA and EPWMxB signals are as defined by OUT-MODE bits.	0	0	0	0
EPWMxA = A-path as defined by OUT-MODE bits.	0	0	0	1
EPWMxB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A-signal path)				
EPWMxA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B-signal path)	0	1	0	
EPWMxB = B-path as defined by OUT-MODE bits				
EPWMxA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B-signal path)	0	1	1	
EPWMxB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A-signal path)				
Rising edge delay applied to EPWMxA / EPWMxB as selected by S4 switch (IN-MODE bits) on A signal path only.	0	X	X	
Falling edge delay applied to EPWMxA / EPWMxB as selected by S5 switch (IN-MODE bits) on B signal path only.				
Rising edge delay and falling edge delay applied to source selected by S4 switch (IN-MODE bits) and output to B signal path only. ⁽¹⁾	1	X	X	

⁽¹⁾ When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA **or** OUTSWAP bits such that EPWMxA=Bpath. Otherwise, EPWMxA will be invalid.

Figure 12-34 shows waveforms for typical cases where $0\% < \text{duty} < 100\%$.

Figure 12-34. Dead-Band Waveforms for Typical Cases ($0\% < \text{Duty} < 100\%$)



The dead-band submodule supports independent values for rising-edge (RED) and falling-edge (FED) delays. The amount of delay is programmed using the DBRED and DBFED registers. These are 10-bit registers and their value represents the number of time-base clock, TBCLK, periods by which a signal edge is delayed. For example, the formula to calculate falling-edge-delay and rising-edge-delay are:

$$FED = DBFED \times T_{TBCLK}$$

$$RED = DBRED \times T_{TBCLK}$$

Where T_{TBCLK} is the period of TBCLK, the prescaled version of SYSCLKOUT.

For convenience, delay values for various TBCLK options are shown in [Table 12-10](#). The ePWM input clock frequency that these delay values been computed by is 100 MHz.

Table 12-10. Dead-Band Delay Values in μ S as a Function of DBFED and DBRED

Dead-Band Value DBFED, DBRED	Dead-Band Delay in μ S		
	TBCLK = SYSCLKOUT/1	TBCLK = SYSCLKOUT /2	TBCLK = SYSCLKOUT/4
1	0.01 μ S	0.03 μ S	0.05 μ S
5	0.06 μ S	0.13 μ S	0.25 μ S
10	0.13 μ S	0.25 μ S	0.50 μ S
100	1.25 μ S	2.50 μ S	5.00 μ S
200	2.50 μ S	5.00 μ S	10.00 μ S
400	5.00 μ S	10.00 μ S	20.00 μ S
500	6.25 μ S	12.50 μ S	25.00 μ S
600	7.50 μ S	15.00 μ S	30.00 μ S
700	8.75 μ S	17.50 μ S	35.00 μ S
800	10.00 μ S	20.00 μ S	40.00 μ S
900	11.25 μ S	22.50 μ S	45.00 μ S
1000	12.50 μ S	25.00 μ S	50.00 μ S

When half-cycle clocking is enabled, the formula to calculate the falling-edge-delay and rising-edge-delay becomes:

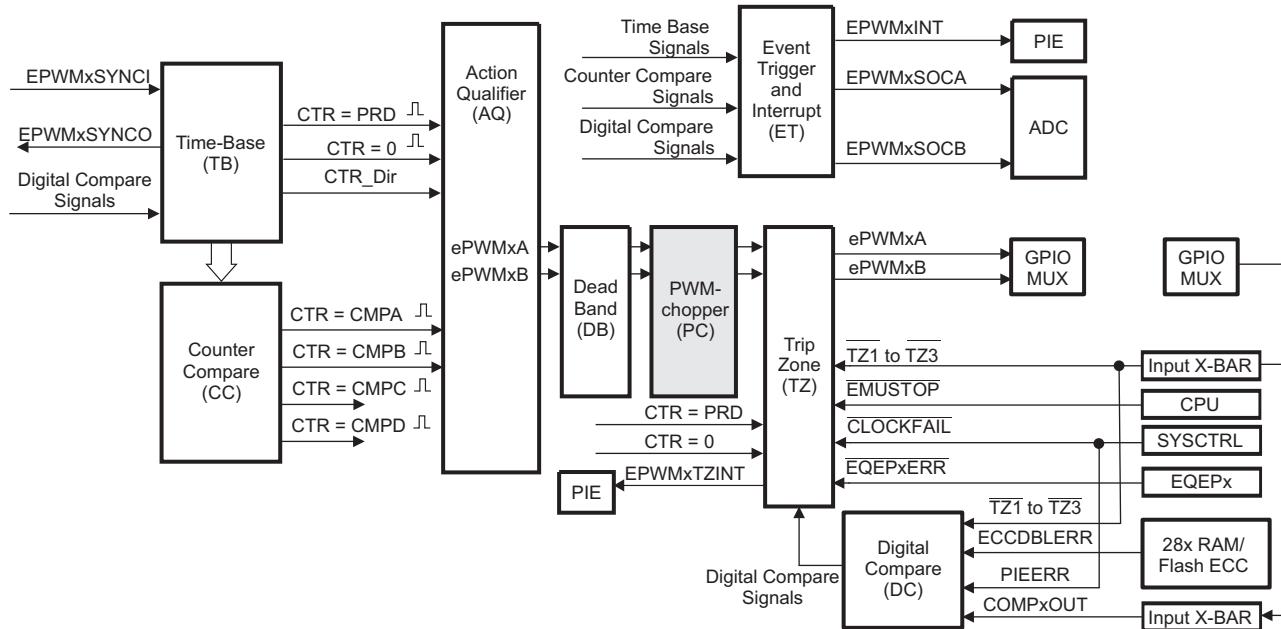
$$FED = DBFED \times T_{TBCLK}/2$$

$$RED = DBRED \times T_{TBCLK}/2$$

12.2.6 PWM-Chopper (PC) Submodule

Figure 12-35 illustrates the PWM-chopper (PC) submodule within the ePWM module.

Figure 12-35. PWM-Chopper Submodule



The PWM-chopper submodule allows a high-frequency carrier signal to modulate the PWM waveform generated by the action-qualifier and dead-band submodules. This capability is important if you need pulse transformer-based gate drivers to control the power switching elements.

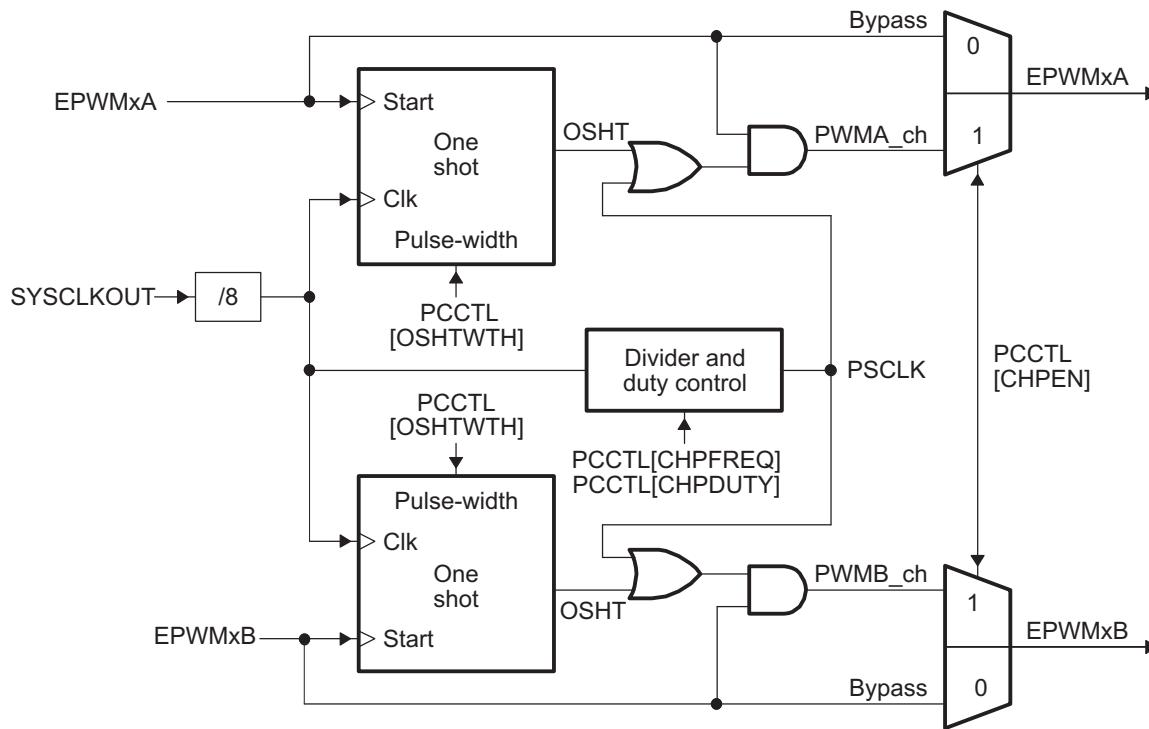
12.2.6.1 Purpose of the PWM-Chopper Submodule

The key functions of the PWM-chopper submodule are:

- Programmable chopping (carrier) frequency
- Programmable pulse width of first pulse
- Programmable duty cycle of second and subsequent pulses
- Can be fully bypassed if not required

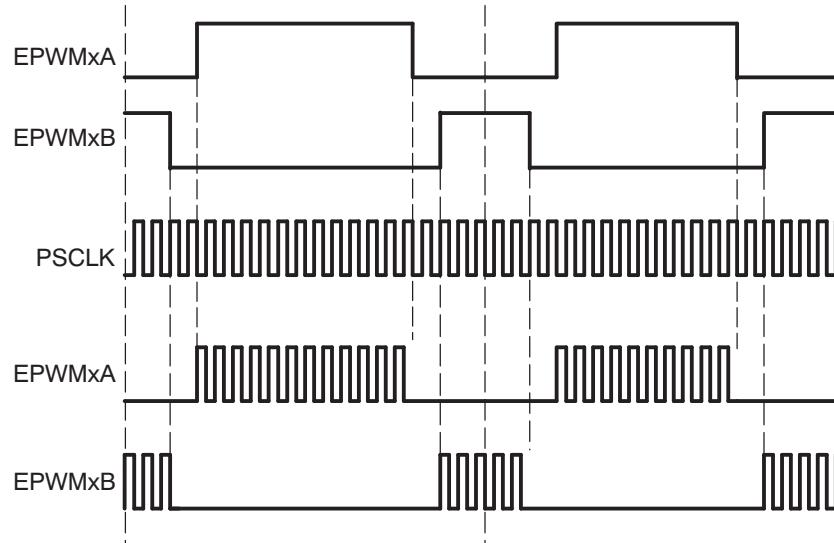
12.2.6.2 Operational Highlights for the PWM-Chopper Submodule

Figure 12-36 shows the operational details of the PWM-chopper submodule. The carrier clock is derived from SYSLKOUT. Its frequency and duty cycle are controlled via the CHPFREQ and CHPDUTY bits in the PCCTL register. The one-shot block is a feature that provides a high energy first pulse to ensure hard and fast power switch turn on, while the subsequent pulses sustain pulses, ensuring the power switch remains on. The one-shot width is programmed via the OSHTWTH bits. The PWM-chopper submodule can be fully disabled (bypassed) via the CHPEN bit.

Figure 12-36. PWM-Chopper Submodule Operational Details

12.2.6.3 Waveforms

Figure 12-37 shows simplified waveforms of the chopping action only; one-shot and duty-cycle control are not shown. Details of the one-shot and duty-cycle control are discussed in the following sections.

Figure 12-37. Simple PWM-Chopper Submodule Waveforms Showing Chopping Action Only

12.2.6.3.1 One-Shot Pulse

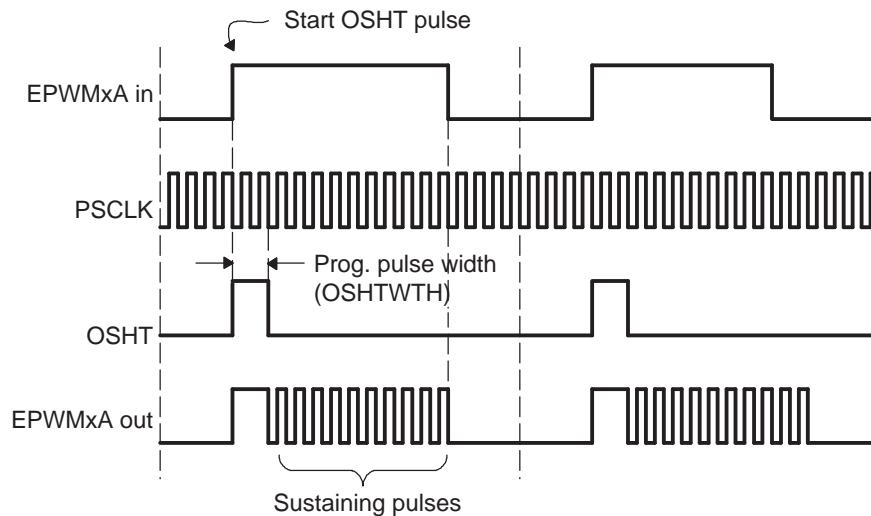
The width of the first pulse can be programmed to any of 16 possible pulse width values. The width or period of the first pulse is given by:

$$T_{1stpulse} = T_{SYSCLKOUT} \times 8 \times OSHTWTH$$

Where $T_{SYSCLKOUT}$ is the period of the system clock (SYSCLKOUT) and OSHTWTH is the four control bits (value from 1 to 16)

Figure 12-38 shows the first and subsequent sustaining pulses and Table 7.3 gives the possible pulse width values for a SYSCLKOUT = 80 MHz.

Figure 12-38. PWM-Chopper Submodule Waveforms Showing the First Pulse and Subsequent Sustaining Pulses



**Table 12-11. Possible Pulse Width Values for
SYSCLKOUT = 80 MHz**

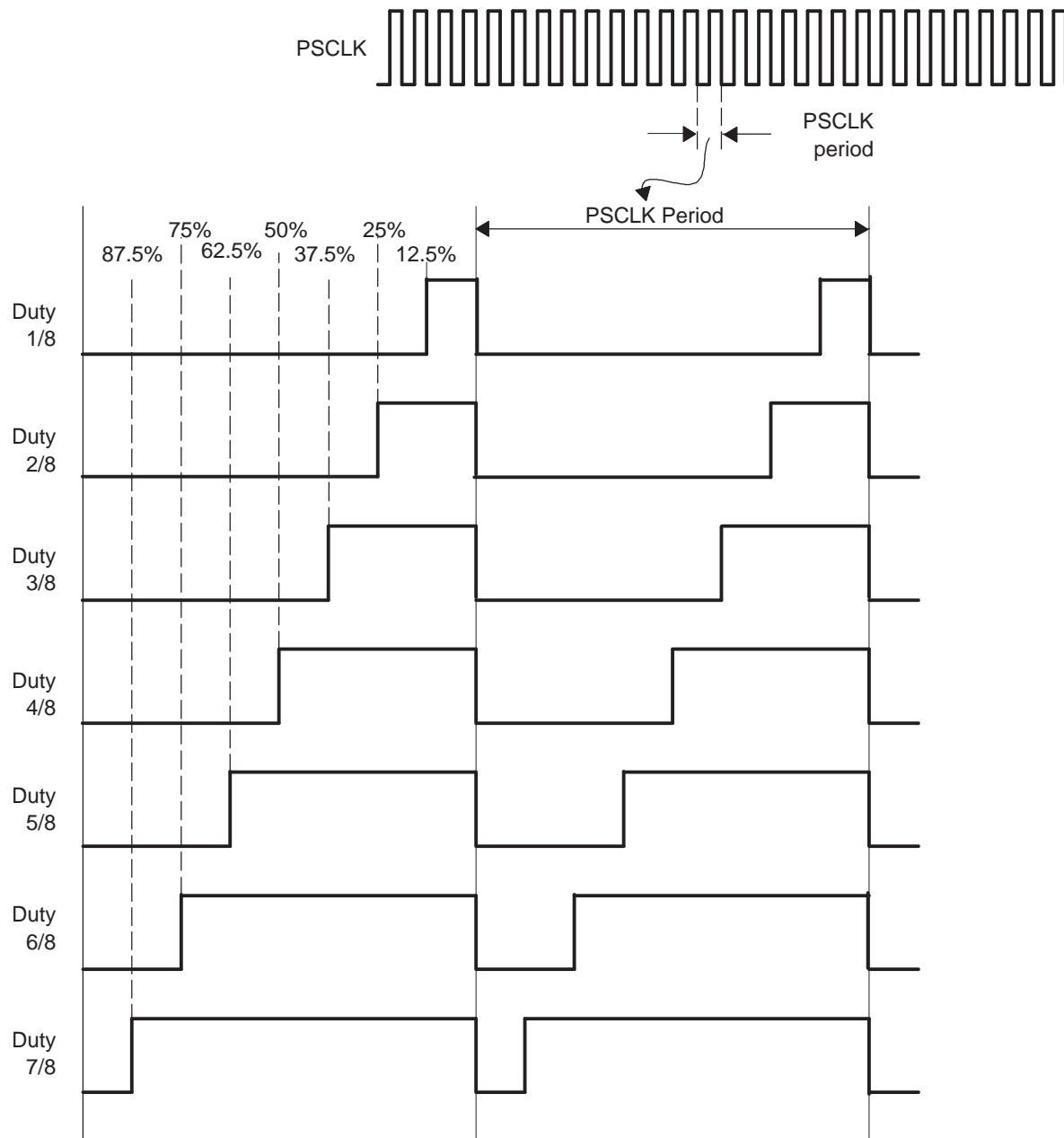
OSHTWTHz (hex)	Pulse Width (nS)
0	100
1	200
2	300
3	400
4	500
5	600
6	700
7	800
8	900
9	1000
A	1100
B	1200
C	1300
D	1400
E	1500
F	1600

12.2.6.3.2 Duty Cycle Control

Pulse transformer-based gate drive designs need to comprehend the magnetic properties or characteristics of the transformer and associated circuitry. Saturation is one such consideration. To assist the gate drive designer, the duty cycles of the second and subsequent pulses have been made programmable. These sustaining pulses ensure the correct drive strength and polarity is maintained on the power switch gate during the on period, and hence a programmable duty cycle allows a design to be tuned or optimized via software control.

[Figure 12-39](#) shows the duty cycle control that is possible by programming the CHPDUTY bits. One of seven possible duty ratios can be selected ranging from 12.5% to 87.5%.

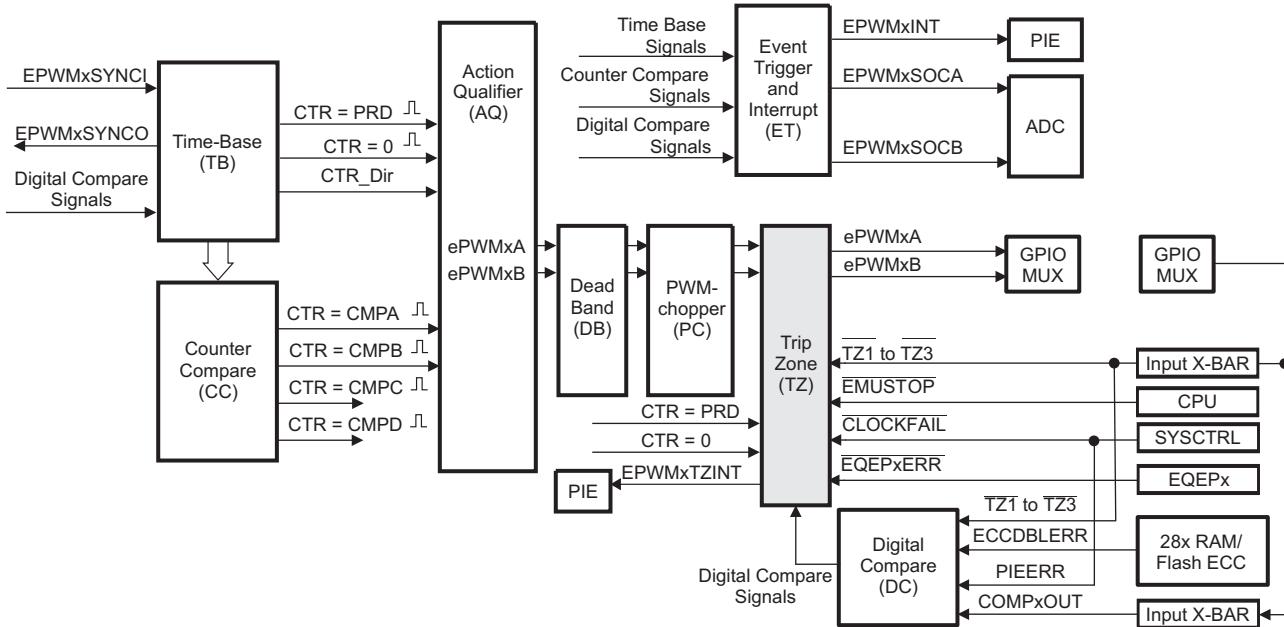
Figure 12-39. PWM-Chopper Submodule Waveforms Showing the Pulse Width (Duty Cycle) Control of Sustaining Pulses



12.2.7 Trip-Zone (TZ) Submodule

Figure 12-40 shows how the trip-zone (TZ) submodule fits within the ePWM module.

Figure 12-40. Trip-Zone Submodule



Each ePWM module is connected to six $\overline{TZ_n}$ signals ($\overline{TZ1}$ to $\overline{TZ6}$). $\overline{TZ1}$ to $\overline{TZ3}$ are sourced from the GPIO mux. $\overline{TZ4}$ is sourced from an inverted EQEPxERR signal on those devices with an EQEP module. $\overline{TZ5}$ is connected to the system clock fail logic, and $\overline{TZ6}$ is sourced from the EMUSTOP output from the CPU. These signals indicate external fault or trip conditions, and the ePWM outputs can be programmed to respond accordingly when faults occur.

12.2.7.1 Purpose of the Trip-Zone Submodule

The key functions of the Trip-Zone submodule are:

- Trip inputs $\overline{TZ1}$ to $\overline{TZ6}$ can be flexibly mapped to any ePWM module.
- Upon a fault condition, outputs EPWMxA and EPWMxB can be forced to one of the following:
 - High
 - Low
 - High-impedance
 - No action taken
- Support for one-shot trip (OSHT) for major short circuits or over-current conditions.
- Support for cycle-by-cycle tripping (CBC) for current limiting operation.
- Support for digital compare tripping (DC) based on state of on-chip analog comparator module outputs and/or $\overline{TZ1}$ to $\overline{TZ3}$ signals.
- Each trip-zone input and digital compare (DC) submodule DCAEVT1/2 or DCBEVT1/2 force event can be allocated to either one-shot or cycle-by-cycle operation.
- Interrupt generation is possible on any trip-zone input.
- Software-forced tripping is also supported.
- The trip-zone submodule can be fully bypassed if it is not required.

12.2.7.2 Operational Highlights for the Trip-Zone Submodule

The following sections describe the operational highlights and configuration options for the trip-zone submodule.

The trip-zone signals $\overline{TZ1}$ to $\overline{TZ6}$ (also collectively referred to as \overline{TZn}) are active low input signals. When one of these signals goes low, or when a DCAEVT1/2 or DCBEVT1/2 force happens based on the TZDCSEL register event selection, it indicates that a trip event has occurred. Each ePWM module can be individually configured to ignore or use each of the trip-zone signals or DC events. Which trip-zone signals or DC events are used by a particular ePWM module is determined by the TZSEL register for that specific ePWM module. The trip-zone signals may or may not be synchronized to the system clock (SYSCLKOUT) and digitally filtered within the GPIO MUX block. A minimum of $3 \times TBCLK$ low pulse width on \overline{TZn} inputs is sufficient to trigger a fault condition on the ePWM module. If the pulse width is less than this, the trip condition may not be latched by CBC or OST latches. The asynchronous trip makes sure that if clocks are missing for any reason, the outputs can still be tripped by a valid event present on \overline{TZn} inputs. The GPIOs or peripherals must be appropriately configured. For more information, see the device-specific version of the *System Control and Interrupts Reference Guide*.

Each \overline{TZn} input can be individually configured to provide either a cycle-by-cycle or one-shot trip event for an ePWM module. DCAEVT1 and DCBEVT1 events can be configured to directly trip an ePWM module or provide a one-shot trip event to the module. Likewise, DCAEVT2 and DCBEVT2 events can also be configured to directly trip an ePWM module or provide a cycle-by-cycle trip event to the module. This configuration is determined by the TZSEL[DCAEVT1/2], TZSEL[DCBEVT1/2], TZSEL[CBCn], and TZSEL[OSHTn] control bits (where n corresponds to the trip input) respectively.

- **Cycle-by-Cycle (CBC):**

When a cycle-by-cycle trip event occurs, the action specified in the TZCTL[TZA] and TZCTL[TZB] bits is carried out immediately on the EPWMxA and/or EPWMxB outputs. [Table 12-12](#) lists some of the possible actions. Independent actions can be specified based on the occurrence of the event while the counter is counting up and/or while it is counting down by appropriately configuring bits in the TZCTL2 register. Actions specified in the TZCTL2 register take effect only when the ETZE bit in TZCTL2 is set.

Additionally, when a cycle-by-cycle trip event occurs, the cycle-by-cycle trip event flag (TZFLG[CBC]) is set and a EPWMx_TZINT interrupt is generated if it is enabled in the TZEINT register and PIE peripheral. A corresponding flag for the event that caused the CBC event is also set in register TZCBCFLG.

If the CBC interrupt is enabled via the TZEINT register, and DCAEVT2 or DCBEVT2 are selected as CBC trip sources via the TZSEL register, it is not necessary to also enable the DCAEVT2 or DCBEVT2 interrupts in the TZEINT register, as the DC events trigger interrupts through the CBC mechanism.

The specified condition on the inputs is automatically cleared based on the selection made with TZCLR[CBCPULSE] if the trip event is no longer present. Therefore, in this mode, the trip event is cleared or reset every PWM cycle. The TZFLG[CBC] and TZCBCFLG flag bits will remain set until they are manually cleared by writing to the TZCLR[CBC] and TZCBCCLR flag bits. If the cycle-by-cycle trip event is still present when the TZFLG[CBC] and/or TZCBCFLG register bits are cleared, then these bits will again be immediately set..

- **One-Shot (OSHT):**

When a one-shot trip event occurs, the action specified in the TZCTL[TZA] and TZCTL[TZB] bits is carried out immediately on the EPWMxA and/or EPWMxB output. [Table 12-12](#) lists some of the possible actions. Independent actions can be specified based on the occurrence of the event while the counter is counting up and/or while it is counting down by appropriately configuring bits in TZCTL2 register. Actions specified in TZCTL2 register take effect only when ETZE bit in TZCTL2 is set.

Additionally, when a one-shot trip event occurs, the one-shot trip event flag (TZFLG[OST]) is set and a EPWMx_TZINT interrupt is generated if it is enabled in the TZEINT register and PIE peripheral. A corresponding flag for the event that caused the OST event is also set in register TZOSTFLG. The one-shot trip condition must be cleared manually by writing to the TZCLR[OST] bit. If desired, TZOSTFLG register bit should be cleared by manually writing to the corresponding bit in the TZOSTCLR register.

If the one-shot interrupt is enabled via the TZEINT register, and DCAEVT1 or DCBEVT1 are selected as OSHT trip sources via the TZSEL register, it is not necessary to also enable the DCAEVT1 or DCBEVT1 interrupts in the TZEINT register, as the DC events trigger interrupts through the OSHT mechanism.

- **Digital Compare Events (DCAEVT1/2 and DCBEVT1/2):**

A digital compare DCAEVT1/2 or DCBEVT1/2 event is generated based on a combination of the DCAH/DCAL and DCBH/DCBL signals as selected by the TZDCSEL register. The signals which

source the DCAH/DCAL and DCBH/DCBL signals are selected via the DCTRIPSEL register and can be either trip zone input pins or analog comparator COMPxOUT signals. For more information on the digital compare submodule signals, see [Section 12.2.9](#).

When a digital compare event occurs, the action specified in the TZCTL[DCAEVT1/2] and TZCTL[DCBEVT1/2] bits is carried out immediately on the EPWMxA and/or EPWMxB output.

[Table 12-12](#) lists the possible actions. Independent actions can be specified based on the occurrence of the event while the counter is counting up and/or while it is counting down by appropriately configuring bits in TZCTLDCA and TZCTLDCB register. Actions specified in TZCTLDCA and TZCTLDCB registers take effect only when ETZE bit in TZCTL2 is set.

In addition, the relevant DC trip event flag (TZFLG[DCAEVT1/2] / TZFLG[DCBEVT1/2]) is set and a EPWMx_TZINT interrupt is generated if it is enabled in the TZEINT register and PIE peripheral.

The specified condition on the pins is automatically cleared when the DC trip event is no longer present. The TZFLG[DCAEVT1/2] or TZFLG[DCBEVT1/2] flag bit will remain set until it is manually cleared by writing to the TZCLR[DCAEVT1/2] or TZCLR[DCBEVT1/2] bit. If the DC trip event is still present when the TZFLG[DCAEVT1/2] or TZFLG[DCBEVT1/2] flag is cleared, then it will again be immediately set.

The action taken when a trip event occurs can be configured individually for each of the ePWM output pins by way of the TZCTL, TZCTL2, TZCTLDCA,, and TZCTLDCB register bit fields. Some of the possible actions, shown in [Table 12-12](#), can be taken on a trip event.

Table 12-12. Possible Actions On a Trip Event

TZCTL Register bit-field Settings	EPWMxA and/or EPWMxB	Comment
0,0	High-Impedance	Tripped
0,1	Force to High State	Tripped
1,0	Force to Low State	Tripped
1,1	No Change	Do Nothing. No change is made to the output.

Example 12-1. Trip-Zone Configurations**Scenario A:**

A one-shot trip event on $\overline{TZ1}$ pulls both EPWM1A, EPWM1B low and also forces EPWM2A and EPWM2B high.

- Configure the ePWM1 registers as follows:
 - TZSEL[OSHT1] = 1: enables $\overline{TZ1}$ as a one-shot event source for ePWM1
 - TZCTL[TZA] = 2: EPWM1A will be forced low on a trip event.
 - TZCTL[TZB] = 2: EPWM1B will be forced low on a trip event.
- Configure the ePWM2 registers as follows:
 - TZSEL[OSHT1] = 1: enables $\overline{TZ1}$ as a one-shot event source for ePWM2
 - TZCTL[TZA] = 1: EPWM2A will be forced high on a trip event.
 - TZCTL[TZB] = 1: EPWM2B will be forced high on a trip event.

Scenario B:

A cycle-by-cycle event on $\overline{TZ5}$ pulls both EPWM1A, EPWM1B low.

A one-shot event on $\overline{TZ1}$ or $\overline{TZ6}$ puts EPWM2A into a high impedance state.

- Configure the ePWM1 registers as follows:
 - TZSEL[CBC5] = 1: enables $\overline{TZ5}$ as a one-shot event source for ePWM1
 - TZCTL[TZA] = 2: EPWM1A will be forced low on a trip event.
 - TZCTL[TZB] = 2: EPWM1B will be forced low on a trip event.
- Configure the ePWM2 registers as follows:
 - TZSEL[OSHT1] = 1: enables $\overline{TZ1}$ as a one-shot event source for ePWM2
 - TZSEL[OSHT6] = 1: enables $\overline{TZ6}$ as a one-shot event source for ePWM2
 - TZCTL[TZA] = 0: EPWM2A will be put into a high-impedance state on a trip event.
 - TZCTL[TZB] = 3: EPWM2B will ignore the trip event.

12.2.7.3 Generating Trip Event Interrupts

Figure 12-41 and Figure 12-42 illustrate the trip-zone submodule control and interrupt logic, respectively. DCAEVT1/2 and DCBEVT1/2 signals are described in further detail in [Section 12.2.9](#).

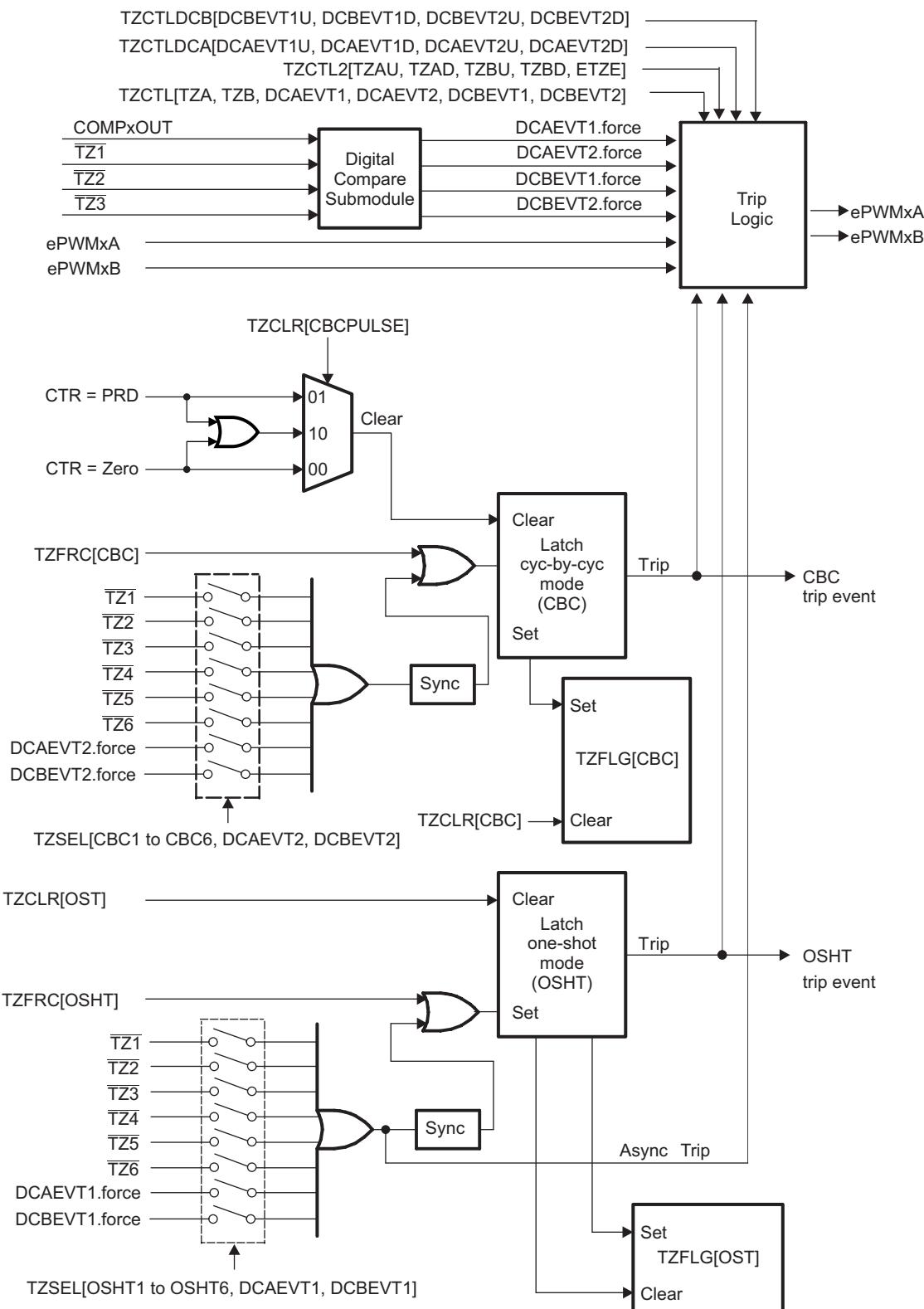
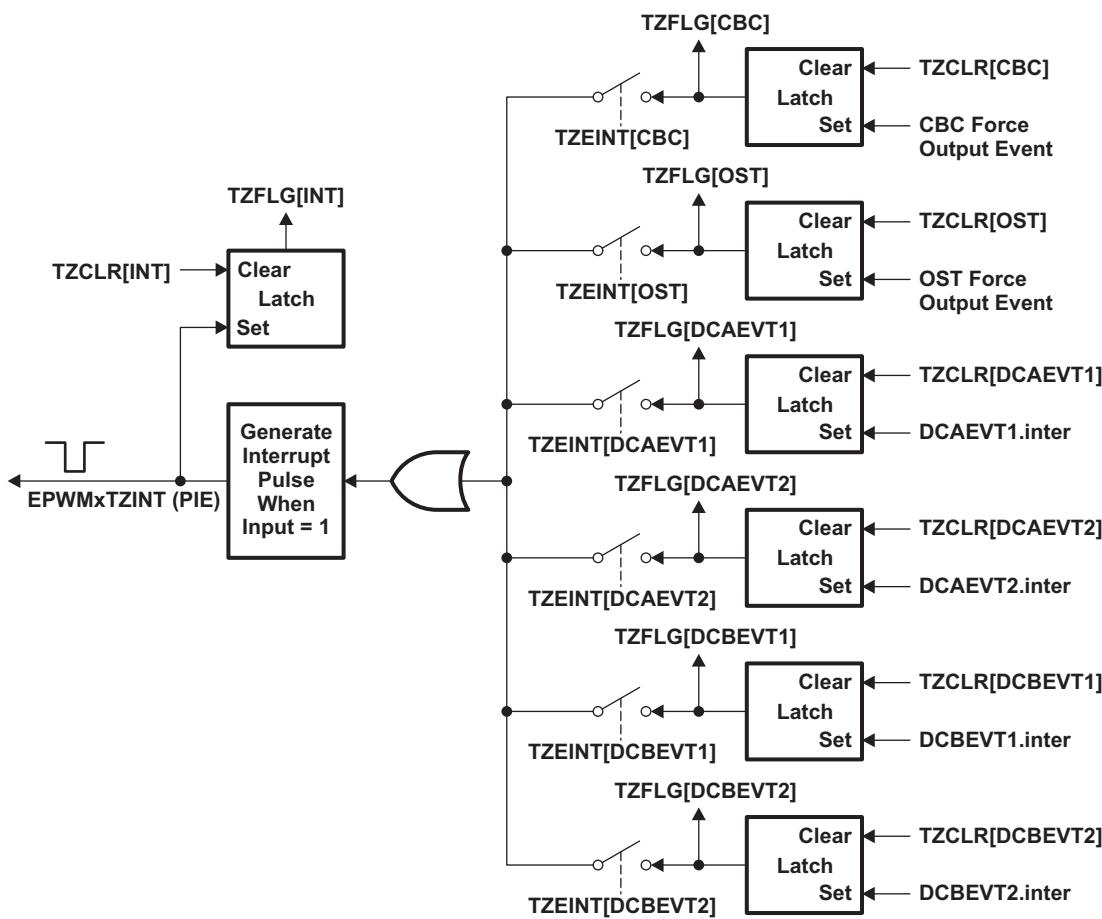
Figure 12-41. Trip-Zone Submodule Mode Control Logic


Figure 12-42. Trip-Zone Submodule Interrupt Logic

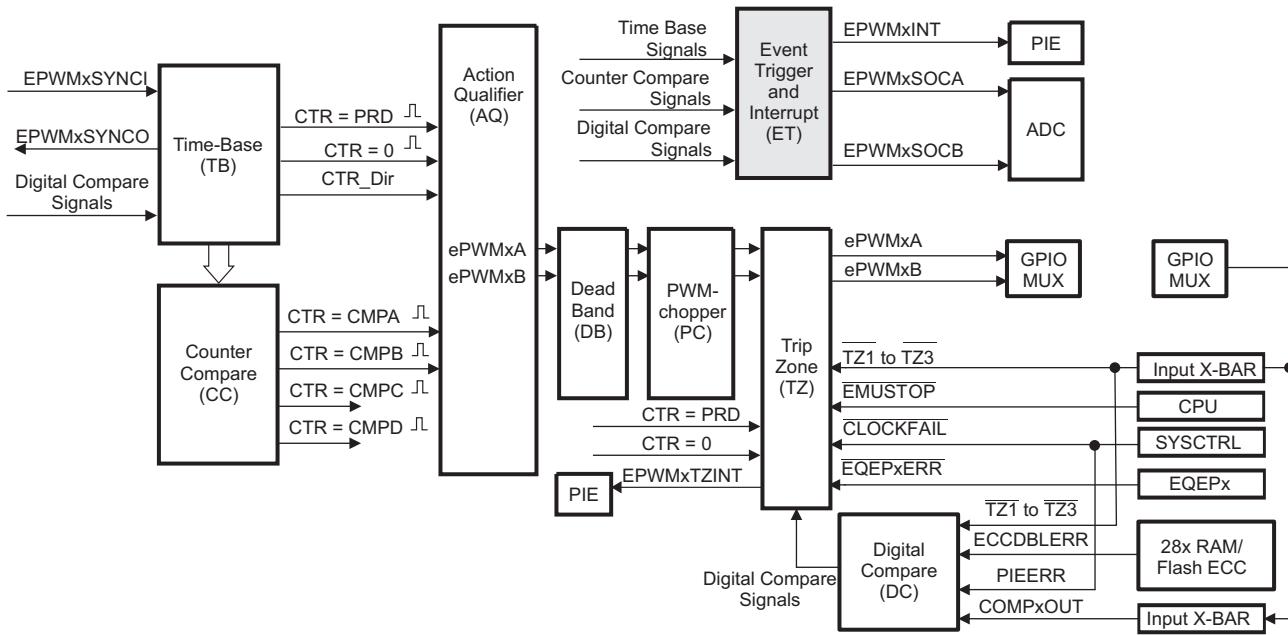


12.2.8 Event-Trigger (ET) Submodule

The key functions of the event-trigger submodule are:

- Receives event inputs generated by the time-base, counter-compare, and digital-compare submodules
- Uses the time-base direction information for up/down event qualification
- Uses prescaling logic to issue interrupt requests and ADC start of conversion at:
 - Every event
 - Every second event
 - Up to every fifteenth event
- Provides full visibility of event generation via event counters and flags
- Allows software forcing of Interrupts and ADC start of conversion

The event-trigger submodule manages the events generated by the time-base submodule, the counter-compare submodule, and the digital-compare submodule to generate an interrupt to the CPU and/or a start of conversion pulse to the ADC when a selected event occurs. Figure 12-43 illustrates where the event-trigger submodule fits within the ePWM system.

Figure 12-43. Event-Trigger Submodule


12.2.8.1 Operational Overview of the ePWM Type 4 Event-Trigger Submodule

The following sections describe the event-trigger submodule's operational highlights.

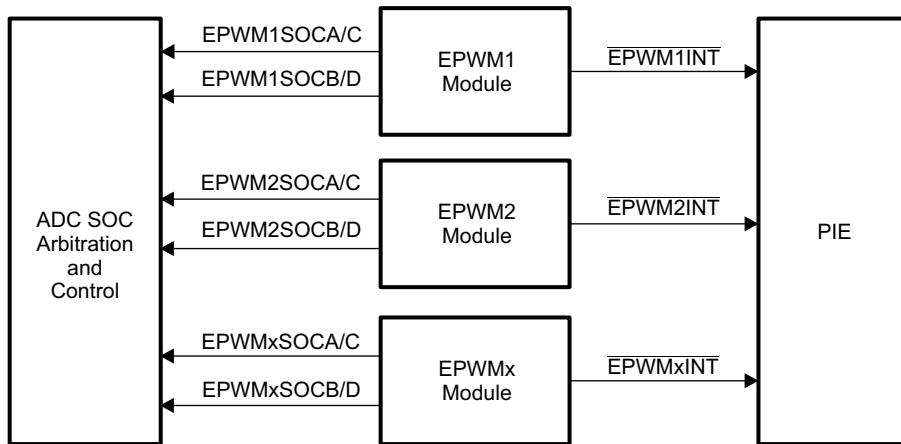
Each ePWM module has one interrupt request line connected to the PIE and two start of conversion signals connected to the ADC module. As shown in Figure 12-44, ADC start of conversion for all ePWM modules are connected to individual ADC trigger inputs to the ADC via the Analog Common Interface Bus (ACIB) and hence multiple modules can initiate an ADC start of conversion via the ADC trigger inputs. The configuration options for the TRIGxSEL register is shown in the below table. The trigger source for an ADC start of conversion is configured by a combination of the TRIGSEL field in the ADCSOCxCTL register, the appropriate bits in the ADCINTSOCSEL1 or ADCINTSOCSEL2 register, and setting the correct bits in the TRIGxSEL registers.

Table 12-13. TRIGxSEL Trigger Options

TRIGxSEL Bits	Trigger Source	Peripheral
00000	No Trigger Enabled (Default)	
00001	TINT0	CPU Timer 0
00010	TINT1	CPU Timer 1
00011	TINT2	CPU Timer 2
00100	XINT2	C28 GPIO MUX
00101	EPWM1SOCA	EPWM1
00110	EPWM1SOCB	
00111	EPWM1SYNC	
01000	EPWM2SOCA	EPWM2
01001	EPWM2SOCB	
01010	EPWM2SYNC	
01011	EPWM3SOCA	EPWM3
01100	EPWM3SOCB	
01101	EPWM3SYNC	

Table 12-13. TRIGxSEL Trigger Options (continued)

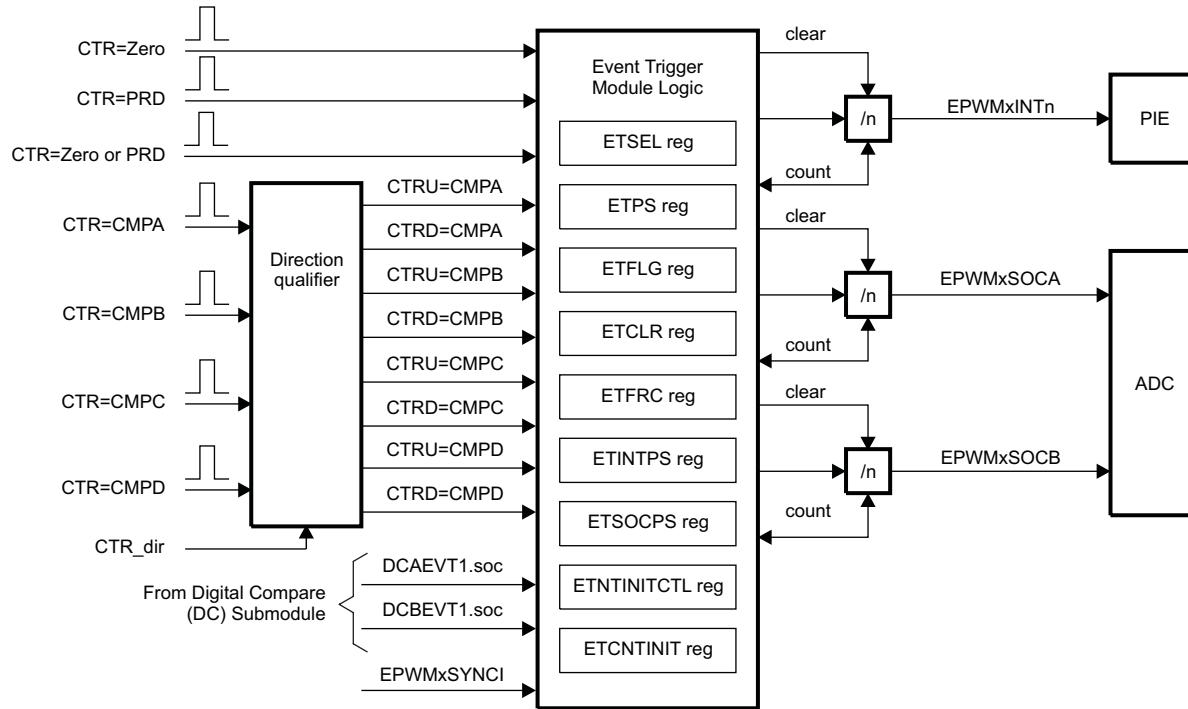
TRIGxSEL Bits	Trigger Source	Peripheral
01110	EPWM4SOCA	EPWM4
01111	EPWM4SOCB	
10000	EPWM4SYNC	
10001	EPWM5SOCA	EPWM5
10010	EPWM5SOCB	
10011	EPWM5SYNC	
10100	EPWM6SOCA	EPWM6
10101	EPWM6SOCB	
10110	EPWM6SYNC	
10111	EPWM7SOCA	EPWM7
11000	EPWM7SOCB	
11001	EPWM7SYNC	
11010	EPWM8SOCA	EPWM8
11011	EPWM8SOCB	
11100	EPWM8SYNC	
11101	EPWM9SOCA	EPWM9
11110	EPWM9SOCB	
11111	EPWM9SYNC	

Figure 12-44. Event-Trigger Submodule Inter-Connectivity of ADC Start of Conversion

The event-trigger submodule monitors various event conditions (shown as inputs on the left side of [Figure 12-45](#)) and can be configured to prescale these events before issuing an interrupt request or an ADC start of conversion. The event-trigger prescaling logic can issue interrupt requests and ADC start of conversion at:

- Every event
- Every second event
- Up to Every fifteenth event

Figure 12-45. Event-Trigger Submodule Showing Event Inputs and Prescaled Outputs



- ETSEL - This selects which of the possible events will trigger an interrupt or start an ADC conversion.
- ETPS - This programs the event prescaling options mentioned above.
- ETFLG - These are flag bits indicating status of the selected and prescaled events.
- ETCLR - These bits allow you to clear the flag bits in the ETFLG register via software.
- ETFRC - These bits allow software forcing of an event. Useful for debugging or software intervention.
- ETINTPS - This programs the interrupt event prescaling options, supporting count and period up to 15 events.
- ETSOCP - This programs the SOC event prescaling options, supporting count and period up to 15 events.
- ETCNTINITCTL - These bits enable ETCNTINIT initialization via SYNC event OR via software force.
- ETCNTINIT - These bits allow you to initialize INT/SOCA/SOCB counters on SYNC events (or software force) with user programmed value.

A more detailed look at how the various register bits interact with the Interrupt and ADC start of conversion logic are shown in [Figure 12-46](#), [Figure 12-47](#), and [Figure 12-48](#).

[Figure 12-46](#) shows the event-trigger's interrupt generation logic. The interrupt-period (ETPS[INTPRD]) bits specify the number of events required to cause an interrupt pulse to be generated. The choices available are:

- Do not generate an interrupt.
- Generate an interrupt on every event
- Generate an interrupt on every second event
- Generate an interrupt on every third event

On ePWM type 4, in order to enable event generation capability up to 15 events the following changes have been made. The selection made on ETPS[INTPSSEL] bit determines whether ETINTPS register, INTCNT2 and INTPRD2 bit fields determine frequency of events (interrupt once every 0-15 events).

Which event can cause an interrupt is configured by the interrupt selection (ETSEL[INTSEL]) and (ETSEL[INTSELCMP]) bits. The event can be one of the following:

- Time-base counter equal to zero (TBCTR = 0x00).
- Time-base counter equal to period (TBCTR = TBPRD).
- Time-base counter equal to zero or period (TBCTR = 0x00 || TBCTR = TBPRD).
- Time-base counter equal to the compare A register (CMPA) when the timer is incrementing.
- Time-base counter equal to the compare A register (CMPA) when the timer is decrementing.
- Time-base counter equal to the compare B register (CMPB) when the timer is incrementing.
- Time-base counter equal to the compare B register (CMPB) when the timer is decrementing.
- Time-base counter equal to the compare C register (CMPC) when the timer is incrementing.
- Time-base counter equal to the compare C register (CMPC) when the timer is decrementing.
- Time-base counter equal to the compare D register (CMPD) when the timer is incrementing.
- Time-base counter equal to the compare D register (CMPD) when the timer is decrementing.

The number of events that have occurred can be read from the interrupt event counter ETPS[INTCNT] or ETINTPS[INTCNT2] register bits based off of the selection made using ETPS[INTPSSEL]. That is, when the specified event occurs the ETPS[INTCNT] or ETINTPS[INTCNT2] bits are incremented until they reach the value specified by ETPS[INTPRD] or ETINTPS[INTPRD2] determined again by the selection made in ETPS[INTPSSEL]. When ETPS[INTCNT] = ETPS[INTPRD] the counter stops counting and its output is set. The counter is only cleared when an interrupt is sent to the PIE.

When ETPS[INTCNT] reaches ETPS[INTPRD] the following behavior will occur [The below behavior is also applicable to ETINTPS[INTCNT2] & ETINTPS[INTPRD2] :

- If interrupts are enabled, ETSEL[INTEN] = 1 and the interrupt flag is clear, ETFLG[INT] = 0, then an interrupt pulse is generated and the interrupt flag is set, ETFLG[INT] = 1, and the event counter is cleared ETPS[INTCNT] = 0. The counter will begin counting events again.
- If interrupts are disabled, ETSEL[INTEN] = 0, or the interrupt flag is set, ETFLG[INT] = 1, the counter stops counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD].
- If interrupts are enabled, but the interrupt flag is already set, then the counter will hold its output high until the ENTFLG[INT] flag is cleared. This allows for one interrupt to be pending while one is serviced.

Writing to the INTPRD bits will automatically clear the counter INTCTN = 0 and the counter output will be reset (so no interrupts are generated). Writing a 1 to the ETFRC[INT] bit will increment the event counter INTCTN. The counter will behave as described above when INTCTN = INTPRD. When INTPRD = 0, the counter is disabled and hence no events will be detected and the ETFRC[INT] bit is also ignored. The same applies to ETINTPS[INTCNT2] & ETINTPS[INTPRD2]

The above definition means that you can generate an interrupt on every event, on every second event, or on every third event if using the INTCTN and INTPRD. You can generate an interrupt on every event up to 15 events if using the INTCTN2 and INTPRD2.

The INTCTN2 value can be initialized with the value from ETCNTINIT[INTINIT] based on the selection made in ETCNTINITCTL[INTINITEN]. When ETCNTINITCTL[INTINITEN] is set, then it enables initialization of INTCTN2 counter with contents of ETCNTINIT[INTINIT] on a SYNC event or software force determined by ETCNTINITCTL[INTINITFRC] .

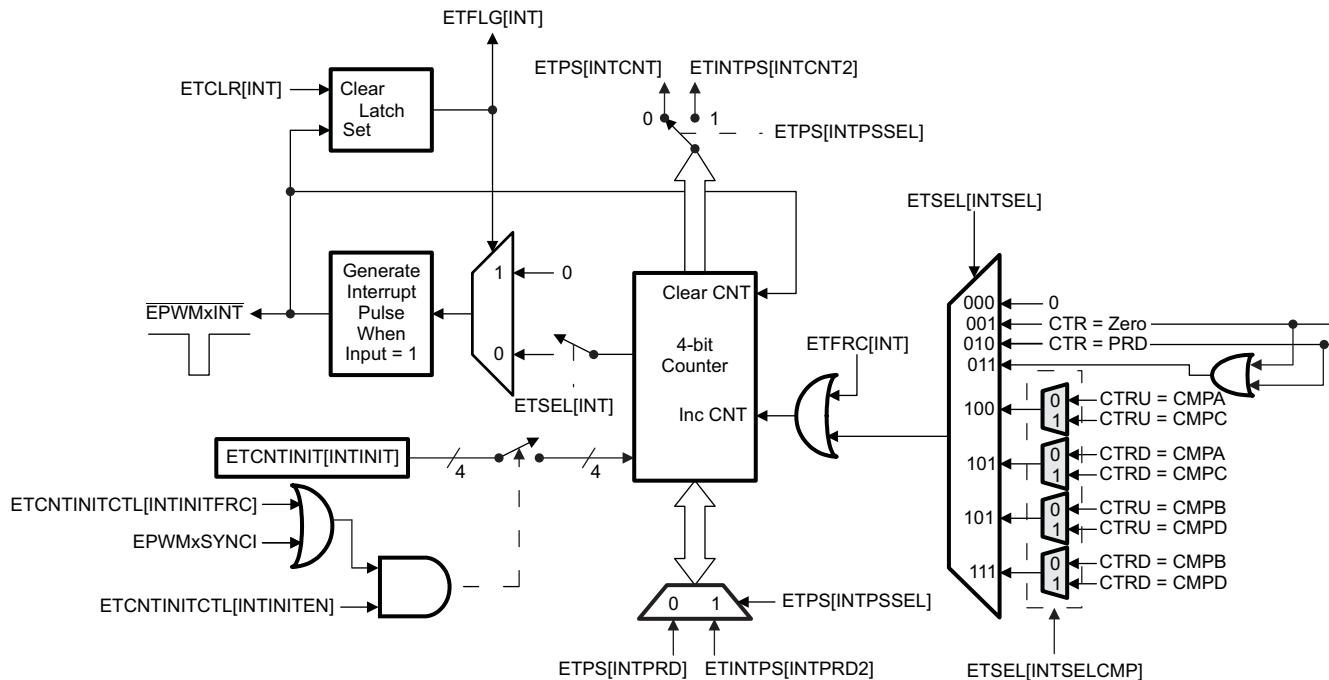
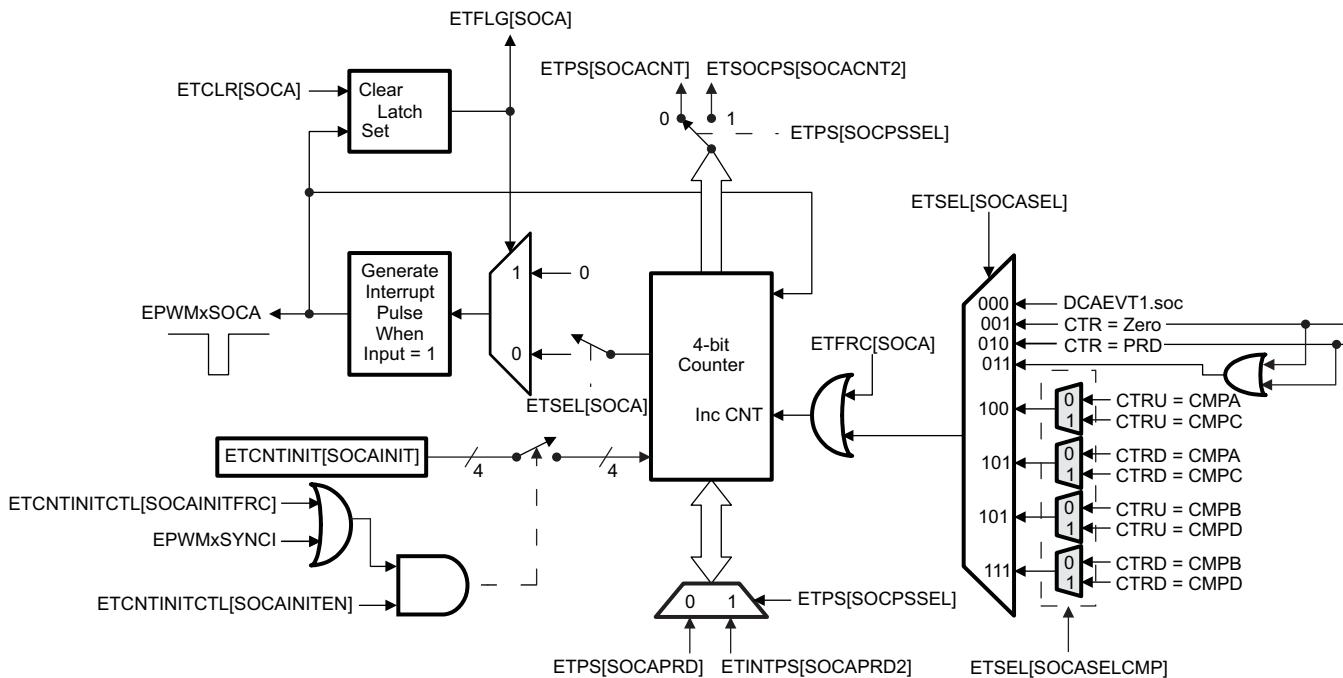
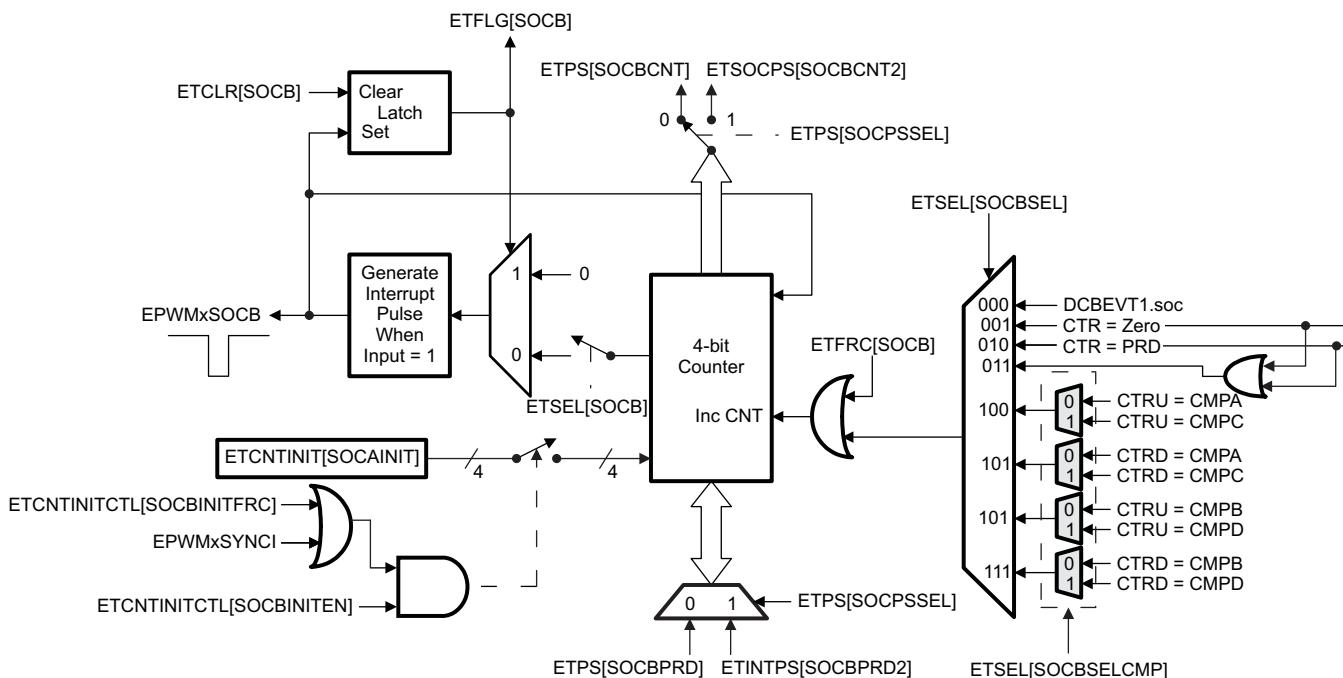
Figure 12-46. Event-Trigger Interrupt Generator


Figure 12-47 shows the operation of the event-trigger's start-of-conversion-A (SOCA) pulse generator. The enhancements include SOCASELCMP and SOCBSELCMP bit fields defined in the ETSEL register enable CMPC and CMPD events respectively to cause a start of conversion. The ETPS[SOCAPSSEL] bit field determines whether SOCACNT2 and SOCAPRD2 take control or not. The ETPS[SOCACNT] counter and ETPS[SOCAPRD] period values behave similarly to the interrupt generator except that the pulses are continuously generated. That is, the pulse flag ETFLG[SOCA] is latched when a pulse is generated, but it does not stop further pulse generation. The enable/disable bit ETSEL[SOCAEN] stops pulse generation, but input events can still be counted until the period value is reached as with the interrupt generation logic. The event that will trigger an SOCA and SOCB pulse can be configured separately in the ETSEL[SOCASEL] and ETSEL[SOCBSEL] bits. The possible events are the same events that can be specified for the interrupt generation logic with the addition of the DCAEVT1.soc and DCBEVT1.soc event signals from the digital compare (DC) submodule. The SOCACNT2 initialization scheme is very similar to the interrupt generator with respective enable, value initialize and SYNC or software force options.

Figure 12-47. Event-Trigger SOCA Pulse Generator

A The DCAEVT1.soc signals are signals generated by the Digital compare (DC) submodule in [Section 12.2.9](#).

[Figure 12-48](#) shows the operation of the event-trigger's start-of-conversion-B (SOCB) pulse generator. The event-trigger's SOCB pulse generator operates the same way as the SOCA.

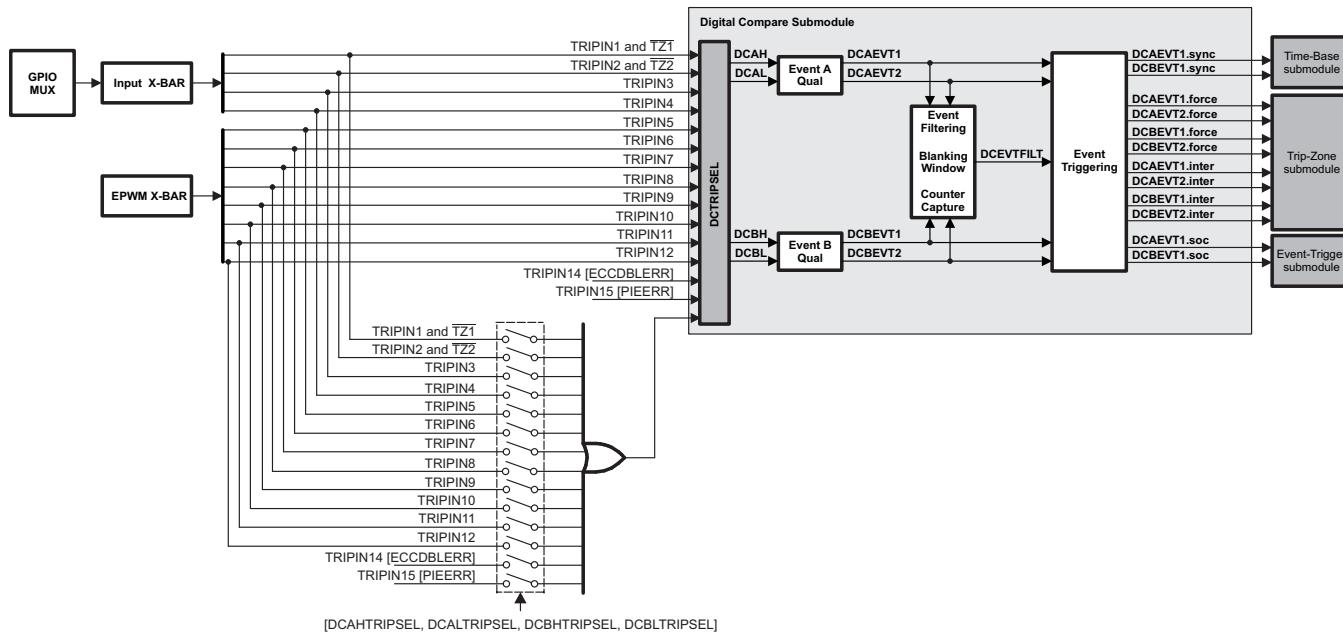
Figure 12-48. Event-Trigger SOCB Pulse Generator

A The DCBEVT1.soc signals are signals generated by the Digital compare (DC) submodule in [Section 12.2.9](#).

12.2.9 Digital Compare (DC) Submodule

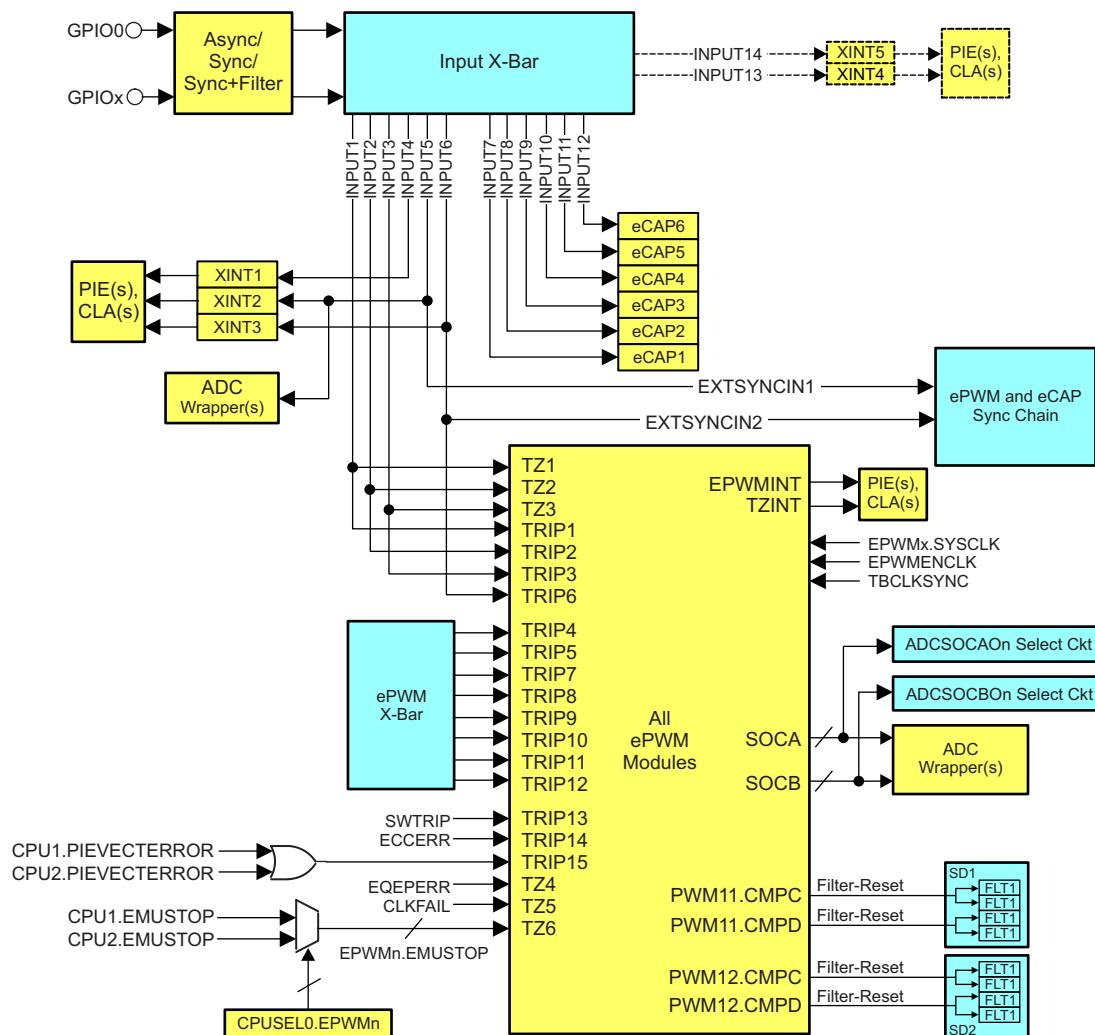
Figure 12-49 illustrates where the digital compare (DC) submodule signals interface to other submodules in the ePWM system.

Figure 12-49. Digital-Compare Submodule High-Level Block Diagram



The ECAP input signals are sourced from the Input X-BAR signals as shown in Figure 12-50.

Figure 12-50. GPIO MUX-to-Trip Input Connectivity



On this device, any of the GPIO pins can be flexibly mapped to be the trip-zone input and/or trip inputs to the trip-zone submodule and digital compare submodule. The Input X-BAR Input Select (INPUTxSELECT) register defines which GPIO pins gets assigned to be the trip-zone inputs / trip inputs.

The digital compare (DC) submodule compares signals external to the ePWM module (for instance, COMPxOUT signals from the analog comparators) to directly generate PWM events/actions which then feed to the event-trigger, trip-zone, and time-base submodules. Additionally, blanking window functionality is supported to filter noise or unwanted pulses from the DC event signals.

NOTE: The user is responsible for driving correct state on the selected pin before enabling clock and configuring the trip input for the respective ePWM peripheral to avoid spurious latch of TRIP signal

12.2.9.1 Purpose of the Digital Compare Submodule

The key functions of the digital compare submodule are:

- Analog Comparator (COMP) module outputs fed though the Input X-BAR logic externally using the GPIO peripheral, internal PIE, ECC error signals , TZ1, TZ2, and TZ3 inputs generate Digital Compare A High/Low (DCAH, DCAL) and Digital Compare B High/Low (DCBH, DCBL) signals.
- DCAH/L and DCBH/L signals trigger events which can then either be filtered or fed directly to the trip-zone, event-trigger, and time-base submodules to:

- generate a trip zone interrupt
- generate an ADC start of conversion
- force an event
- generate a synchronization event for synchronizing the ePWM module TBCTR.
- Event filtering (blanking window logic) can optionally blank the input signal to remove noise.

12.2.9.2 Enhanced Trip Action

In order to allow multiple comparators at a time to affect DCA/BEVTx events and trip actions, there is a OR logic to bring together ALL trip inputs (up to 15) from sources external to the ePWM module and feed into DCAH, DCAL, DCBH, and DCBL as “combinational input” using the DCTRIPSEL register. This is configured by writing appropriate value [Trip Combination input] to the DCAHCOMPSEL,DCALCOMPSEL, DCBHCOMPSEL, DCBLCOMPSEL bit fields in the DCTRIPSEL register.

The user has an discrete choice for which trip input to put through the combinational logic for Digital Compare A High/Low (DCAH, DCAL) and Digital Compare B High/Low (DCBH, DCBL) signals generation. This is achieved using the selection from DCAHTRIPSEL, DCALTRIPSEL, DCBHTRIPSEL and DCBLCOMPSEL register. The appropriate bit when set indicates that Trip input is chosen for “combinational input” by the DCTRIPSEL register.

Apart from these options user can also make the external trip inputs which feed into the OR gate individually selectable and not go through the “combinational input” by using the DCTRIPSEL register.

12.2.9.3 Operation Highlights of the Digital Compare Submodule

The following sections describe the operational highlights and configuration options for the digital compare submodule.

12.2.9.3.1 Digital Compare Events

As illustrated in [Section 12.2.9.3.2](#) earlier in this section, trip zone inputs ($\overline{TZ1}$, $\overline{TZ2}$, and $\overline{TZ3}$) and COMPxOUT signals from the analog comparator (COMP) module can be selected via the DCTRIPSEL bits to generate the Digital Compare A High and Low (DCAH/L) and Digital Compare B High and Low (DCBH/L) signals. Then, the configuration of the TZDCSEL register qualifies the actions on the selected DCAH/L and DCBH/L signals, which generate the DCAEVT1/2 and DCBEVT1/2 events (Event Qualification A and B).

NOTE: The \overline{TZn} signals, when used as a DCEVT tripping functions, are treated as a normal input signal and can be defined to be active high or active low inputs. EPWM outputs are asynchronously tripped when either the \overline{TZn} , DCAEVTx.force, or DCBEVTx.force signals are active. For the condition to remain latched, a minimum of $3 \times T_{BCLK}$ sync pulse width is required. If pulse width is $< 3 \times T_{BCLK}$ sync pulse width, the trip condition may or may not get latched by CBC or OST latches.

The DCAEVT1/2 and DCBEVT1/2 events can then be filtered to provide a filtered version of the event signals (DCEVTFILT) or the filtering can be bypassed. Filtering is discussed further in [Section 12.2.9.3.2](#). Either the DCAEVT1/2 and DCBEVT1/2 event signals or the filtered DCEVTFILT event signals can generate a force to the trip zone module, a TZ interrupt, an ADC SOC, or a PWM sync signal.

- **force signal:**

DCAEVT1/2.force signals force trip zone conditions which either directly influence the output on the EPWMxA pin (via TZCTL, TZCTLDC, TZCTLDCB register configurations) or, if the DCAEVT1/2 signals are selected as one-shot or cycle-by-cycle trip sources (via the TZSEL register), the DCAEVT1/2.force signals can effect the trip action via the TZCTL or TZCTL2 register configurations. The DCBEVT1/2.force signals behaves similarly, but affect the EPWMxB output pin instead of the EPWMxA output pin.

The priority of conflicting actions on the TZCTL, TZCTL2, TZCTLDC, and TZCTLDCB registers is as follows (highest priority overrides lower priority):

Output EPWMxA:

- TZA (highest) -> DCAEVT1 -> DCAEVT2 (lowest)
- TZAU (highest) -> DCAEVT1U -> DCAEVT2U (lowest)
- TZAD (highest) -> DCAEVT1D -> DCAEVT2D (lowest)

Output EPWMxB:

- TZB (highest) -> DCBEVT1 -> DCBEVT2 (lowest)
- TZBU (highest) -> DCBEVT1U -> DCBEVT2U (lowest)
- TZBD (highest) -> DCBEVT1D -> DCBEVT2D (lowest)

• **interrupt signal:**

DCAEVT1/2.interrupt signals generate trip zone interrupts to the PIE. To enable the interrupt, the user must set the DCAEVT1, DCAEVT2, DCBEVT1, or DCBEVT2 bits in the TZEINT register. Once one of these events occurs, an EPWMxTZINT interrupt is triggered, and the corresponding bit in the TZCLR register must be set in order to clear the interrupt.

• **soc signal:**

The DCAEVT1.soc signal interfaces with the event-trigger submodule and can be selected as an event which generates an ADC start-of-conversion-A (SOCA) pulse via the ETSEL[SOCASEL] bit. Likewise, the DCBEVT1.soc signal can be selected as an event which generates an ADC start-of-conversion-B (SOCB) pulse via the ETSEL[SOCBSEL] bit.

• **sync signal:**

The DCAEVT1.sync and DCBEVT1.sync events are ORed with the EPWMxSYNC1 input signal and the TBCTL[SWFSYNC] signal to generate a synchronization pulse to the time-base counter.

The diagrams below show how the DCAEVT1, DCAEVT2 or DCBEVTFLT signals are processed to generate the digital compare A event force, interrupt, soc and sync signals.

Figure 12-51. DCAEVT1 Event Triggering

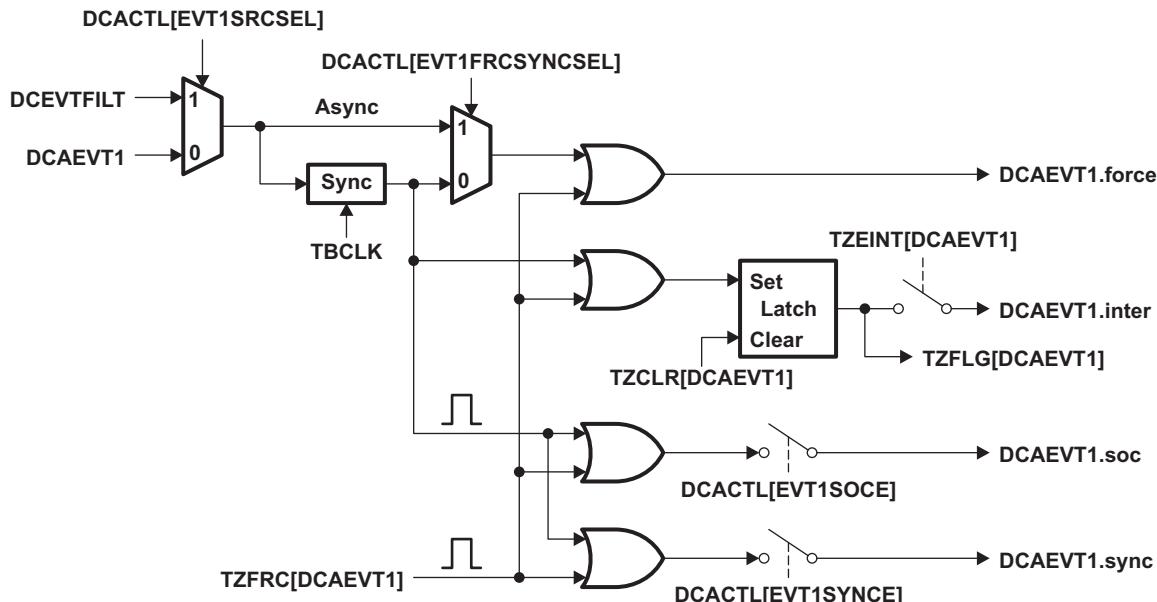
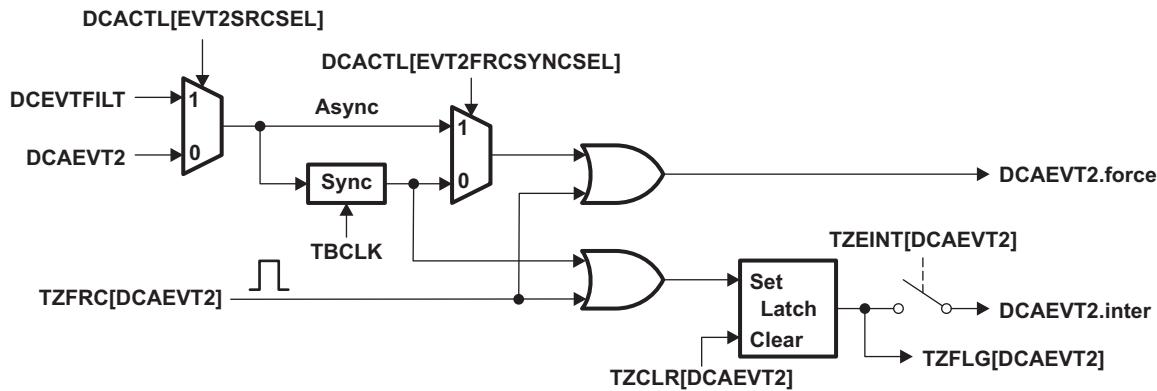


Figure 12-52. DCAEVT2 Event Triggering


The diagrams below show how the DCBEVT1, DCBEVT2 or DCEVTFLT signals are processed to generate the digital compare B event force, interrupt, soc and sync signals.

Figure 12-53. DCBEVT1 Event Triggering

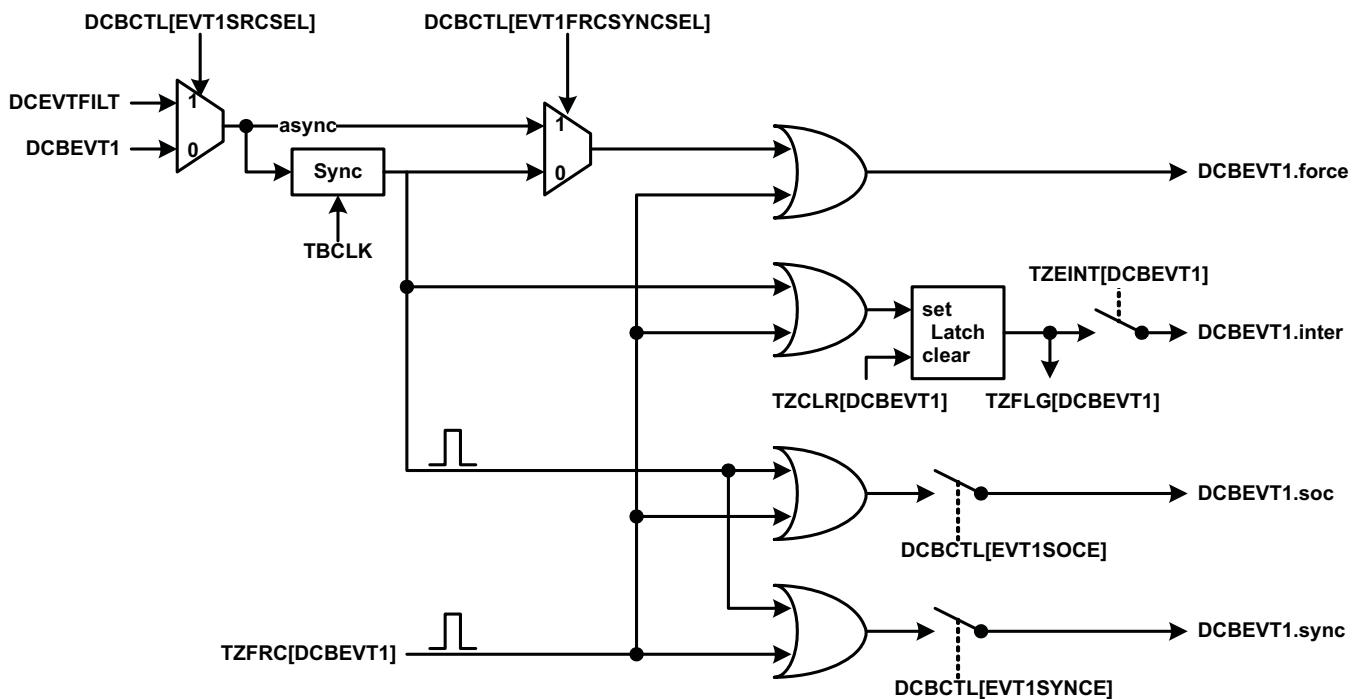
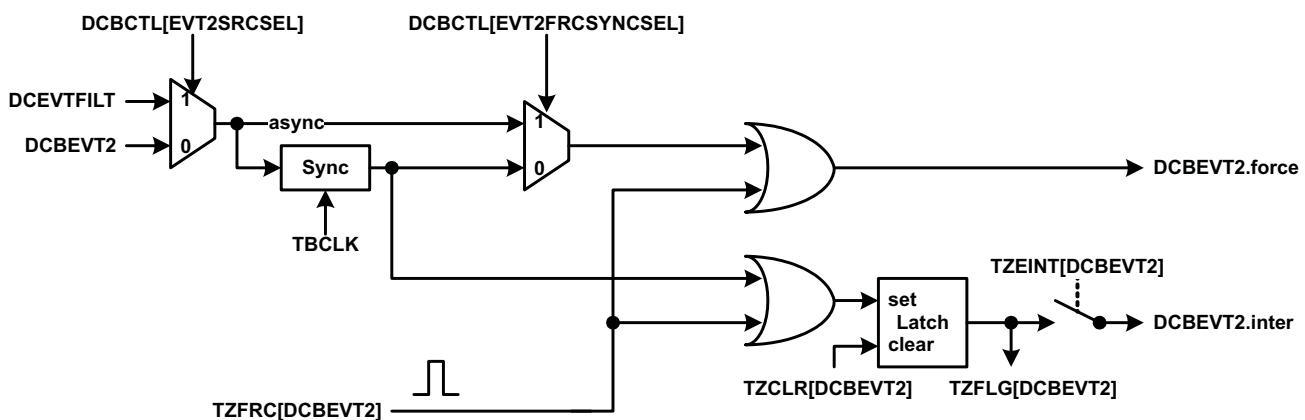
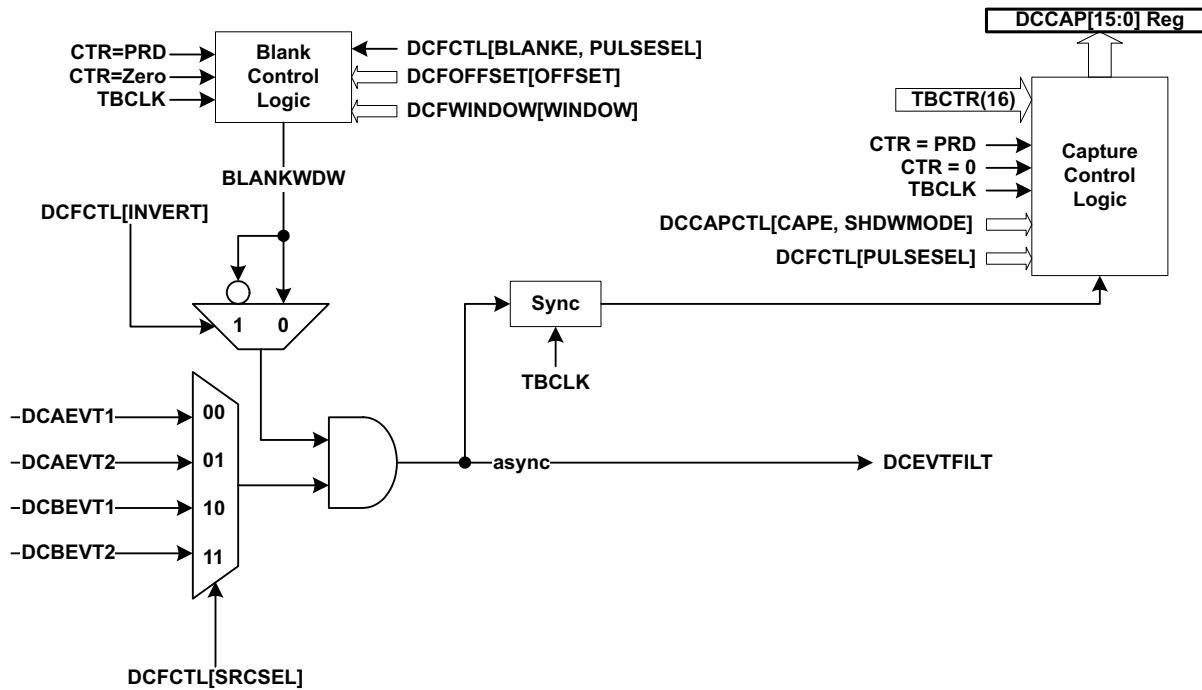


Figure 12-54. DCBEVT2 Event Triggering



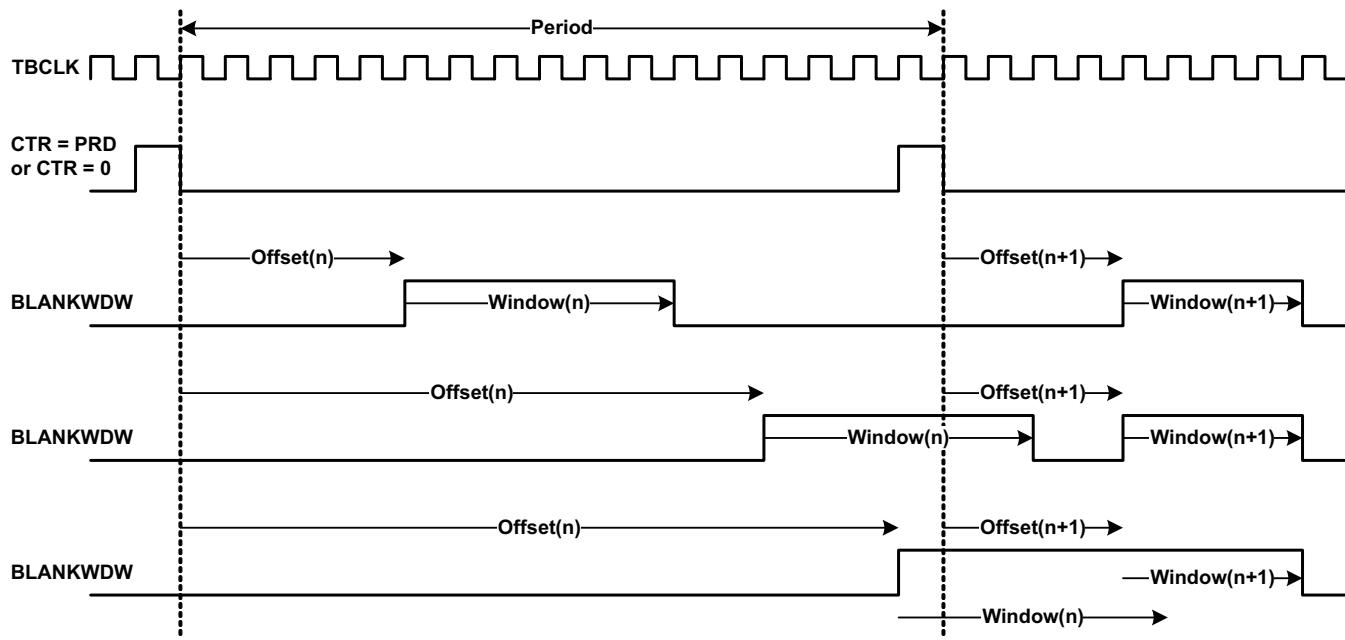
12.2.9.3.2 Event Filtering

The DCAEVT1/2 and DCBEVT1/2 events can be filtered via event filtering logic to remove noise by optionally blanking events for a certain period of time. This is useful for cases where the analog comparator outputs may be selected to trigger DCAEVT1/2 and DCBEVT1/2 events, and the blanking logic is used to filter out potential noise on the signal prior to tripping the PWM outputs or generating an interrupt or ADC start-of-conversion. The event filtering can also capture the TBCTR value of the trip event. The diagram below shows the details of the event filtering logic.

Figure 12-55. Event Filtering


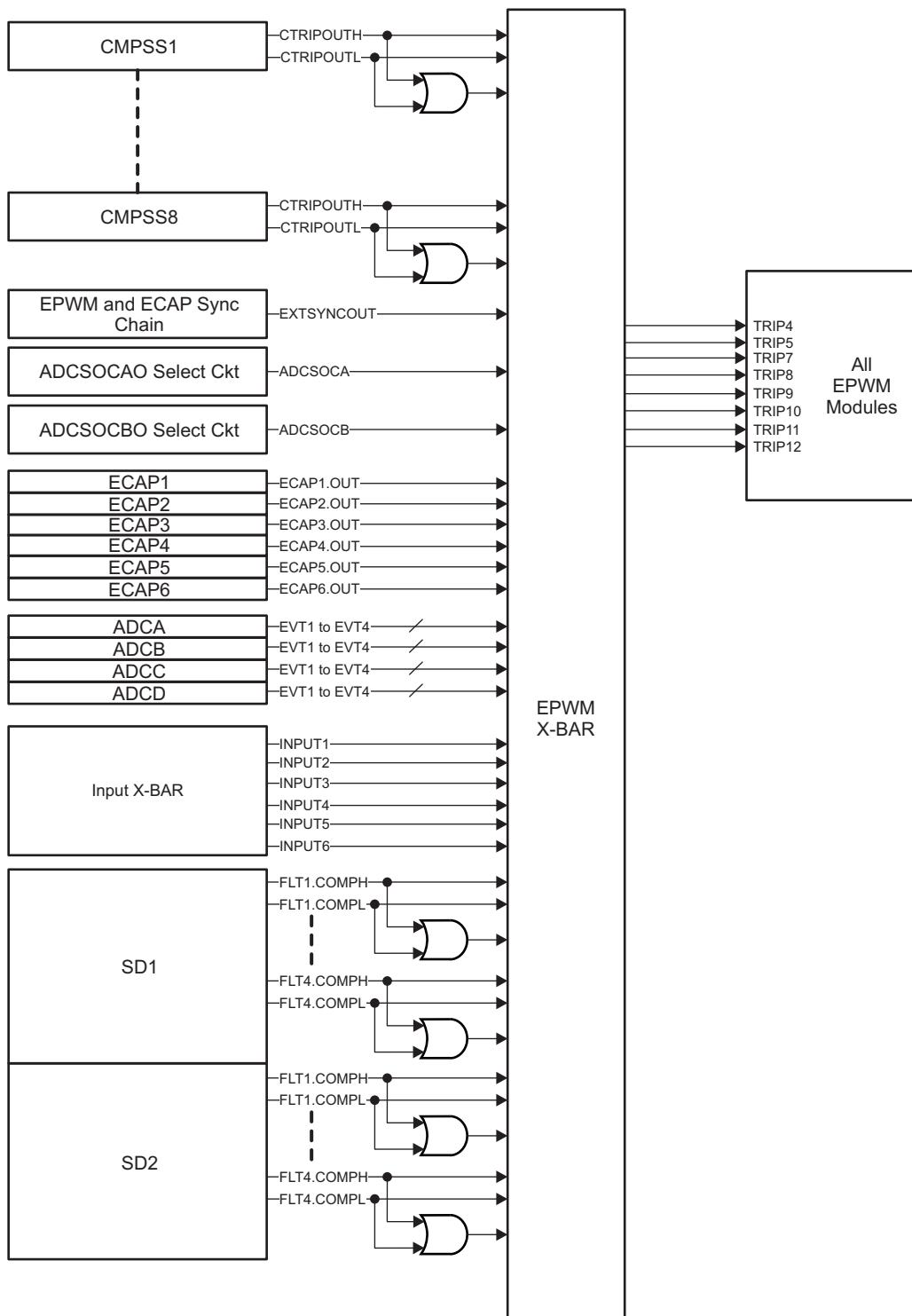
If the blanking logic is enabled, one of the digital compare events – DCAEVT1, DCAEVT2, DCBEVT1, DCBEVT2 – is selected for filtering. The blanking window, which filters out all event occurrences on the signal while it is active, will be aligned to either a CTR = PRD pulse or a CTR = 0 pulse or both CTR = PRD and CTR = 0 (configured by the DCFCTL[PULSESEL] bits). An offset value in TBCLK counts is programmed into the DCFOFFSET register, which determines at what point after the CTR = PRD or CTR = 0 pulse the blanking window starts. The duration of the blanking window, in number of TBCLK counts after the offset counter expires, is written to the DCFWINDOW register by the application. During the blanking window, all events are ignored. Before and after the blanking window ends, events can generate soc, sync, interrupt, and force signals as before.

The diagram below illustrates several timing conditions for the offset and blanking window within an ePWM period. Notice that if the blanking window crosses the CTR = 0 or CTR = PRD boundary, the next window still starts at the same offset value after the CTR = 0 or CTR = PRD pulse.

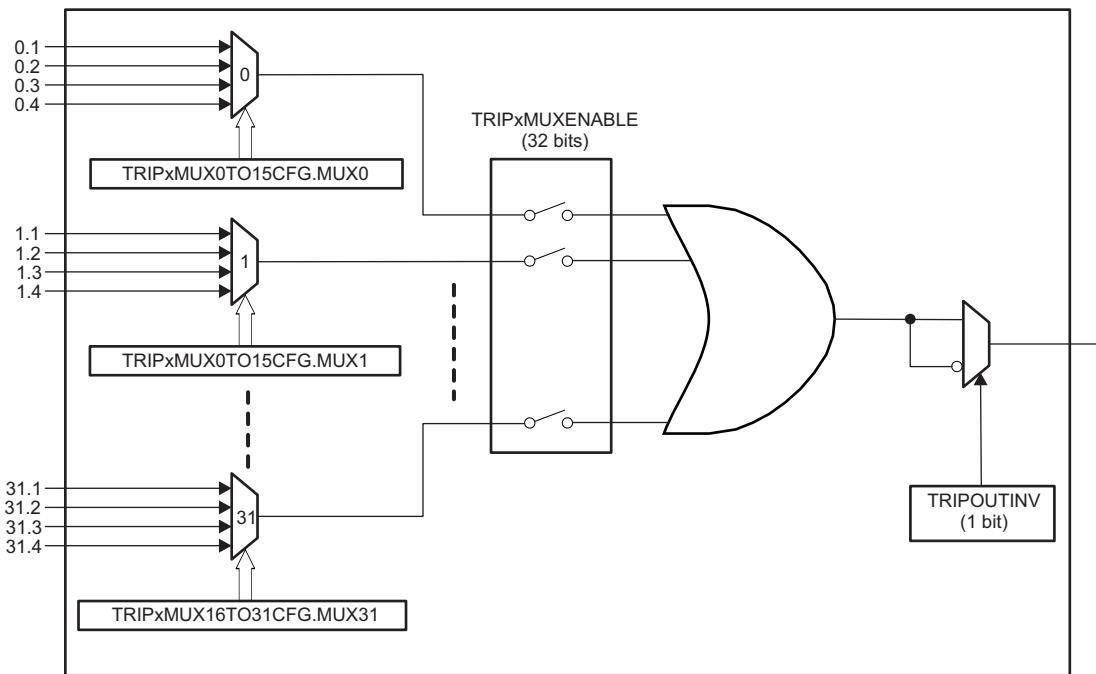
Figure 12-56. Blanking Window Timing Diagram

12.2.10 EPWM X-BAR

Figure 12-57 shows the architecture of the EPwm X-Bar. This module enables selection of various trigger sources into any of the eight dedicated ETWPM trips inputs, namely the TRIP4, TRIP5, TRIP7, TRIP8, TRIP9, TRIP10, TRIP11 and TRIP12.

Figure 12-57. EPWM X-BAR


The EPWM X-BAR has eight outputs which are routed to each EPWM module. [Figure 12-58](#) represents the architecture of a single output but it is identical to the architecture of all of the other outputs:

Figure 12-58. EPWM Architecture - Single Output

First, determine the signal(s) which should be passed to the EPWM by referencing the EPWM X-Bar Input Table. You may select up to one signal per mux (31 total muxes) for each TRIPx output. Select the inputs to each mux via the TRIPxMUX0TO15CFG and TRIPxMUX16TO31CFG registers. In order to pass any signal through to the EPWM, you must also enable the mux in the TRIPxMUXENABLE register. All muxes which are enabled will be logically OR'd before being passed on to the respective TRIPx signal on the EPWM. You may also optionally invert the signal via the TRIPOUTINV register.

Table 12-14. ePWM X-BAR Mux Configuration Table

Mux	1	2	3	4
0	CMPSS1.CTRIPH	CMPSS0.CTRIPH_OR_CTRIPL	ADCAEVT1	ECAP1.OUT
1	CMPSS1.CTRIPL	INPUTXBAR1		ADCCEVT1
2	CMPSS2.CTRIPH	CMPSS1.CTRIPH_OR_CTRIPL	ADCAEVT2	ECAP2.OUT
3	CMPSS2.CTRIPL	INPUTXBAR2		ADCCEVT2
4	CMPSS3.CTRIPH	CMPSS2.CTRIPH_OR_CTRIPL	ADCAEVT3	ECAP3.OUT
5	CMPSS3.CTRIPL	INPUTXBAR3		ADCCEVT3
6	CMPSS4.CTRIPH	CMPSS3.CTRIPH_OR_CTRIPL	ADCAEVT4	ECAP4.OUT
7	CMPSS4.CTRIPL	INPUTXBAR4		ADCCEVT4
8	CMPSS5.CTRIPH	CMPSS4.CTRIPH_OR_CTRIPL	ADCBEVT1	ECAP5.OUT
9	CMPSS5.CTRIPL	INPUTXBAR5		ADCDEVT1
10	CMPSS6.CTRIPH	CMPSS5.CTRIPH_OR_CTRIPL	ADCBEVT2	ECAP6.OUT
11	CMPSS6.CTRIPL	INPUTXBAR6		ADCDEVT2
12	CMPSS7.CTRIPH	CMPSS6.CTRIPH_OR_CTRIPL	ADCBEVT3	
13	CMPSS7.CTRIPL	ADCSOCA		ADCDEVT3
14	CMPSS8.CTRIPH	CMPSS7.CTRIPH_OR_CTRIPL	ADCBEVT4	EXTSYNCOUT
15	CMPSS8.CTRIPL	ADCSOCB		ADCDEVT4
16	SD1FLT1.COMPH	SD1FLT1.COMPH_OR_COMPL		
17	SD1FLT1.COMPL			
18	SD1FLT2.COMPH	SD1FLT2.COMPH_OR_COMPL		
19	SD1FLT2.COMPL			
20	SD1FLT3.COMPH	SD1FLT3.COMPH_OR_COMPL		
21	SD1FLT3.COMPL			
22	SD1FLT4.COMPH	SD1FLT4.COMPH_OR_COMPL		
23	SD1FLT4.COMPL			
24	SD2FLT1.COMPH	SD2FLT1.COMPH_OR_COMPL		
25	SD2FLT1.COMPL			
26	SD2FLT2.COMPH	SD2FLT2.COMPH_OR_COMPL		
27	SD2FLT2.COMPL			
28	SD2FLT3.COMPH	SD2FLT3.COMPH_OR_COMPL		
29	SD2FLT3.COMPL			
30	SD2FLT4.COMPH	SD2FLT4.COMPH_OR_COMPL		
31	SD2FLT4.COMPL			

Note: All unused and reserved positions are tied to '0'.

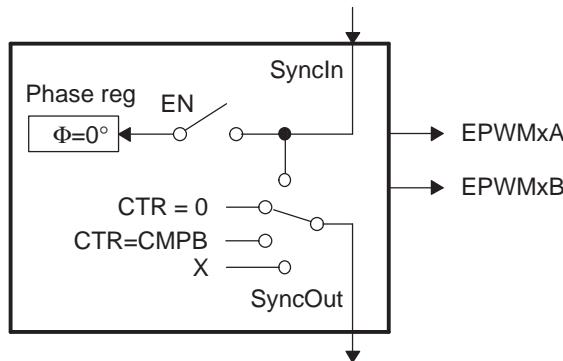
12.3 Applications to Power Topologies

An ePWM module has all the local resources necessary to operate completely as a standalone module or to operate in synchronization with other identical ePWM modules.

12.3.1 Overview of Multiple Modules

Previously in this user's guide, all discussions have described the operation of a single module. To facilitate the understanding of multiple modules working together in a system, the ePWM module described in reference is represented by the more simplified block diagram shown in [Figure 12-59](#). This simplified ePWM block shows only the key resources needed to explain how a multiswitch power topology is controlled with multiple ePWM modules working together.

Figure 12-59. Simplified ePWM Module

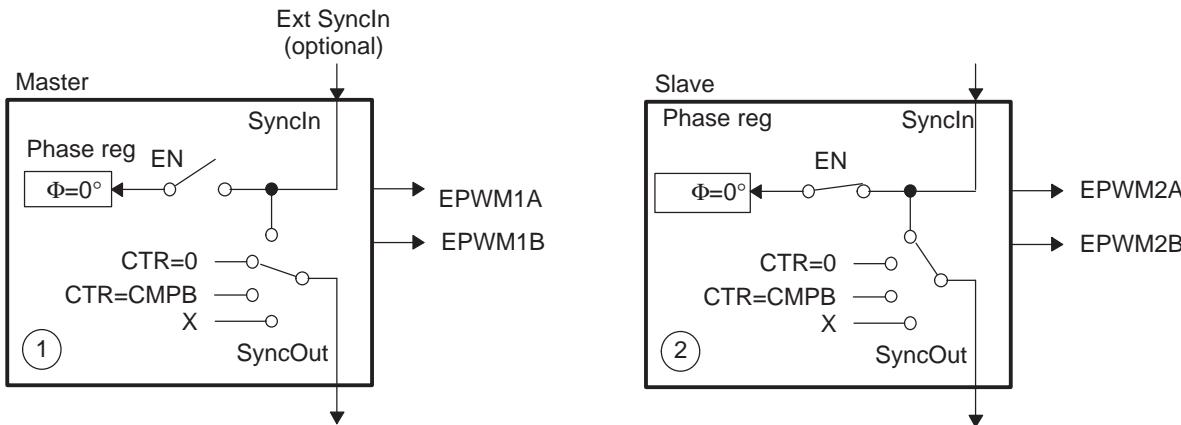


12.3.2 Key Configuration Capabilities

The key configuration choices available to each module are as follows:

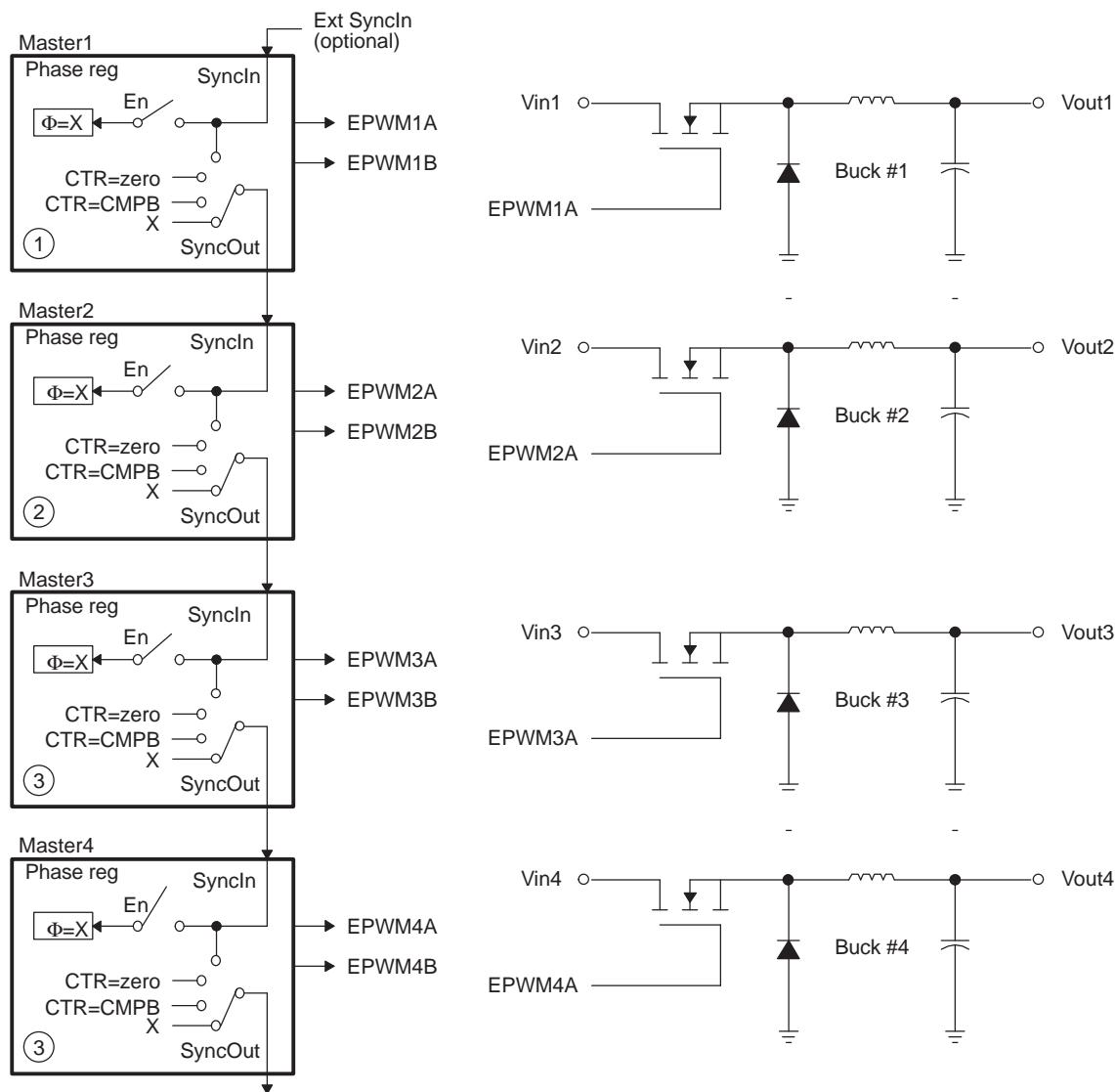
- Options for SyncIn
 - Load own counter with phase register on an incoming sync strobe—enable (EN) switch closed
 - Do nothing or ignore incoming sync strobe—enable switch open
 - Sync flow-through - SyncOut connected to SyncIn
 - Master mode, provides a sync at PWM boundaries—SyncOut connected to CTR = PRD
 - Master mode, provides a sync at any programmable point in time—SyncOut connected to CTR = CMPB
 - Module is in standalone mode and provides No sync to other modules—SyncOut connected to X (disabled)
- Options for SyncOut
 - Sync flow-through - SyncOut connected to SyncIn
 - Master mode, provides a sync at PWM boundaries—SyncOut connected to CTR = PRD
 - Master mode, provides a sync at any programmable point in time—SyncOut connected to CTR = CMPB
 - Module is in standalone mode and provides No sync to other modules—SyncOut connected to X (disabled)

For each choice of SyncOut, a module may also choose to load its own counter with a new phase value on a SyncIn strobe input or choose to ignore it, i.e., via the enable switch. Although various combinations are possible, the two most common—master module and slave module modes—are shown in [Figure 12-60](#).

Figure 12-60. EPWM1 Configured as a Typical Master, EPWM2 Configured as a Slave

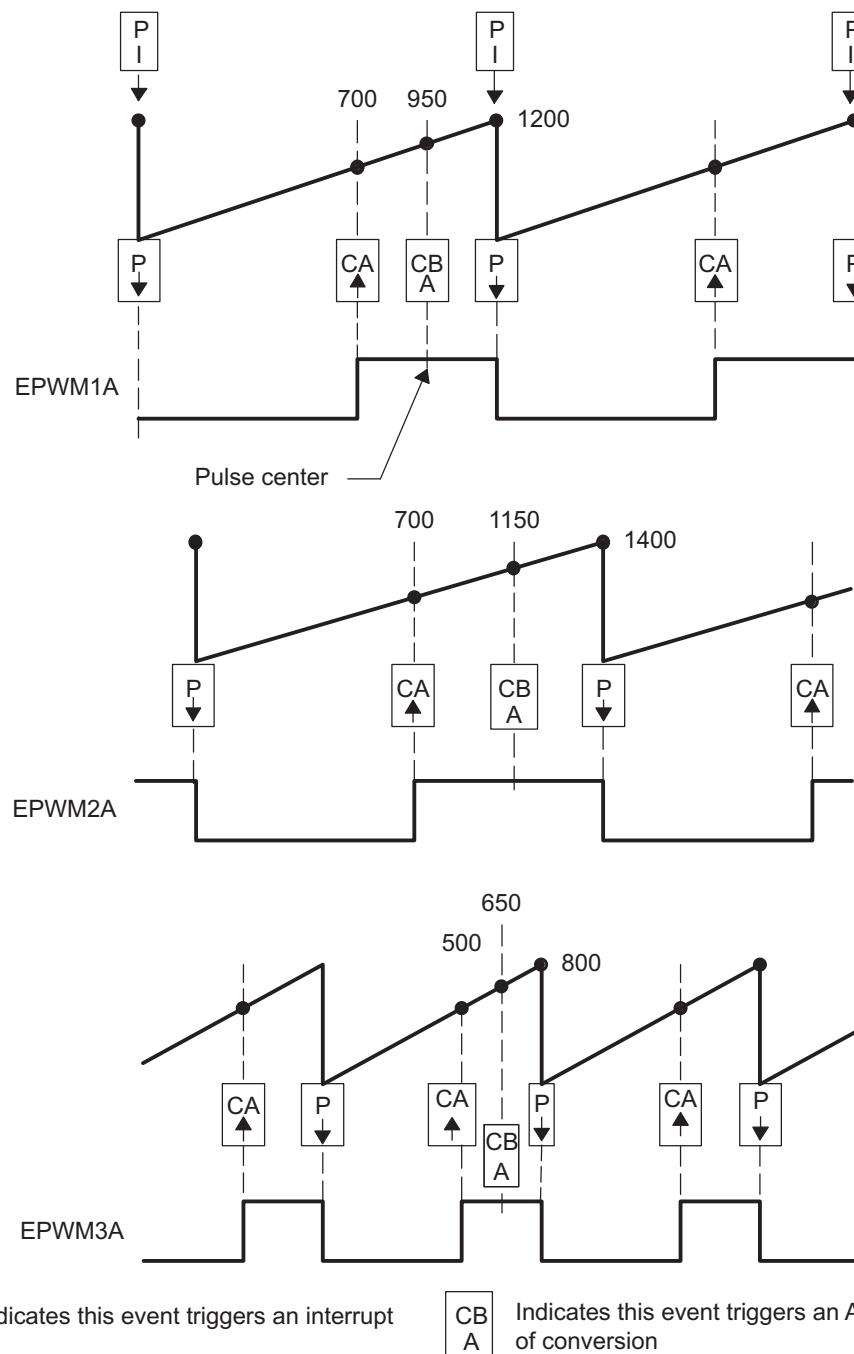
12.3.3 Controlling Multiple Buck Converters With Independent Frequencies

One of the simplest power converter topologies is the buck. A single ePWM module configured as a master can control two buck stages with the same PWM frequency. If independent frequency control is required for each buck converter, then one ePWM module must be allocated for each converter stage. Figure 12-61 shows four buck stages, each running at independent frequencies. In this case, all four ePWM modules are configured as Masters and no synchronization is used. Figure 12-62 shows the waveforms generated by the setup shown in Figure 12-61; note that only three waveforms are shown, although there are four stages.

Figure 12-61. Control of Four Buck Stages. Here $F_{PWM1} \neq F_{PWM2} \neq F_{PWM3} \neq F_{PWM4}$ 

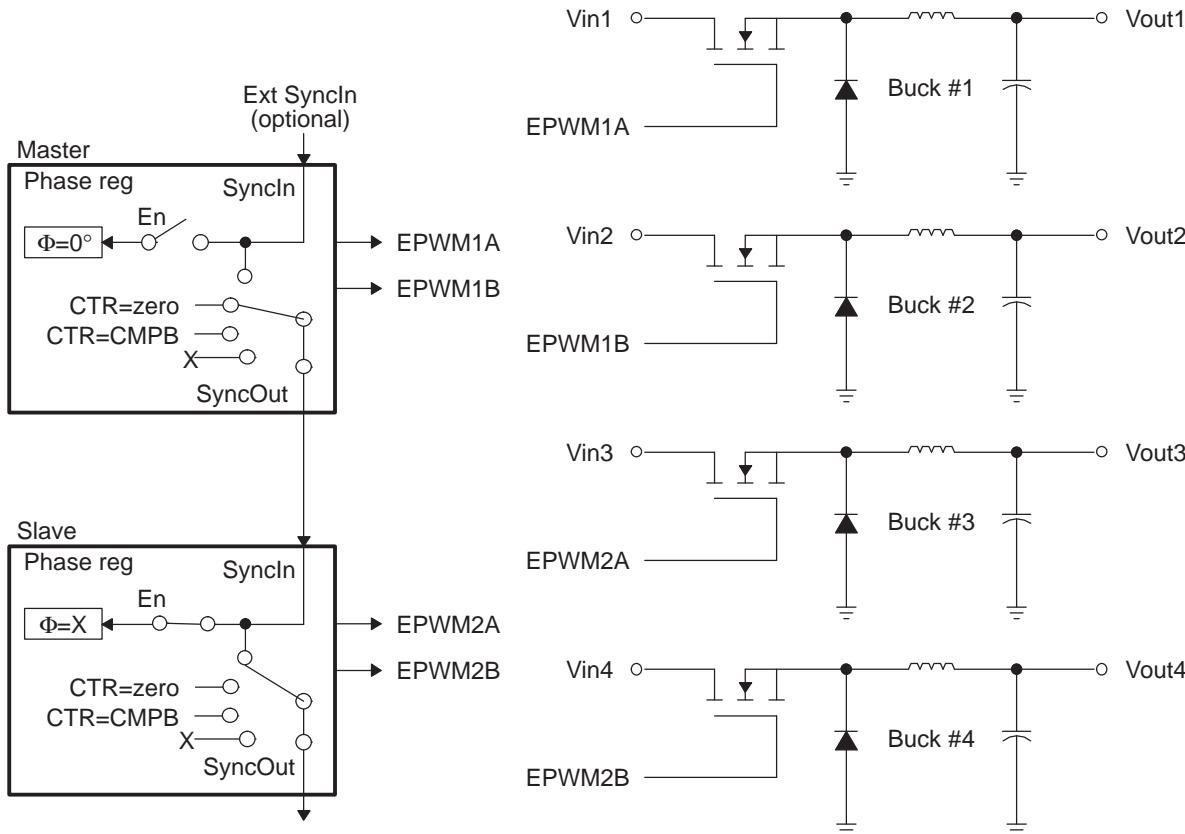
NOTE: $\varphi = X$ indicates value in phase register is a "don't care"

Figure 12-62. Buck Waveforms for Figure 12-61 (Note: Only three bucks shown here)

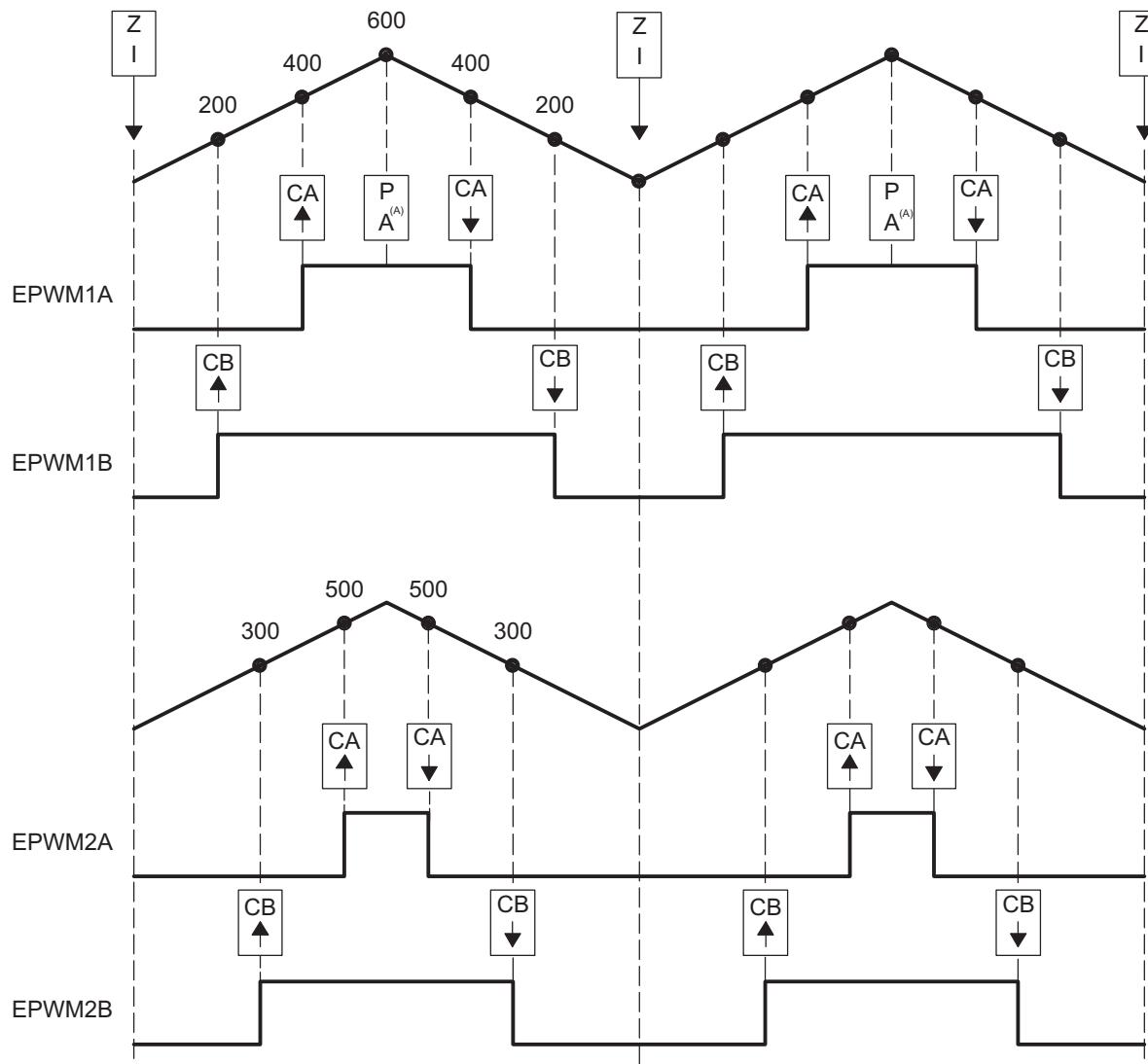


12.3.4 Controlling Multiple Buck Converters With Same Frequencies

If synchronization is a requirement, ePWM module 2 can be configured as a slave and can operate at integer multiple (N) frequencies of module 1. The sync signal from master to slave ensures these modules remain locked. [Figure 12-63](#) shows such a configuration; [Figure 12-64](#) shows the waveforms generated by the configuration.

Figure 12-63. Control of Four Buck Stages. (Note: $F_{PWM2} = N \times F_{PWM1}$)

NOTE: $\Phi = X$ indicates value in phase register is a "don't care"

Figure 12-64. Buck Waveforms for Figure 12-63 (Note: $F_{PWM2} = F_{PWM1}$)


A Starts ADC conversion.

12.3.5 Controlling Multiple Half H-Bridge (HHB) Converters

Topologies that require control of multiple switching elements can also be addressed with these same ePWM modules. It is possible to control a Half-H bridge stage with a single ePWM module. This control can be extended to multiple stages. [Figure 12-65](#) shows control of two synchronized Half-H bridge stages where stage 2 can operate at integer multiple (N) frequencies of stage 1. [Figure 12-66](#) shows the waveforms generated by the configuration shown in [Figure 12-65](#).

Module 2 (slave) is configured for Sync flow-through; if required, this configuration allows for a third Half-H bridge to be controlled by PWM module 3 and also, most importantly, to remain in synchronization with master module 1.

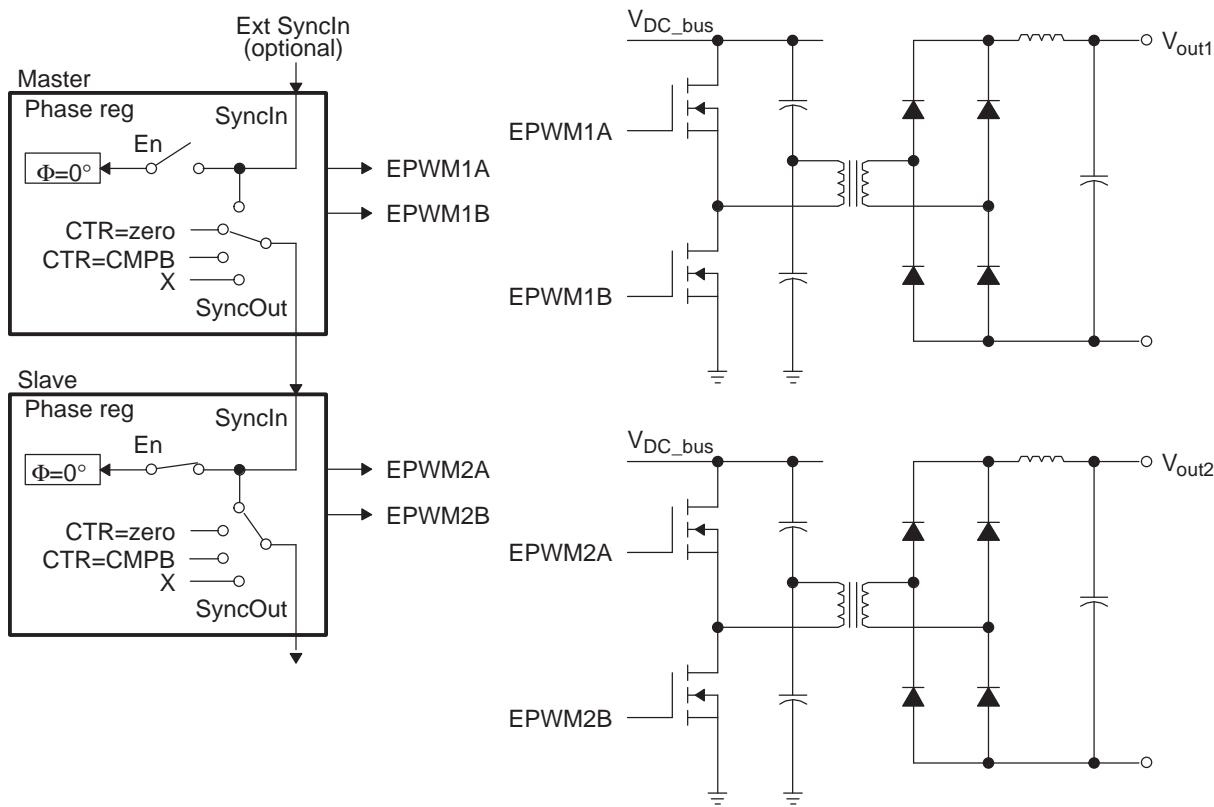
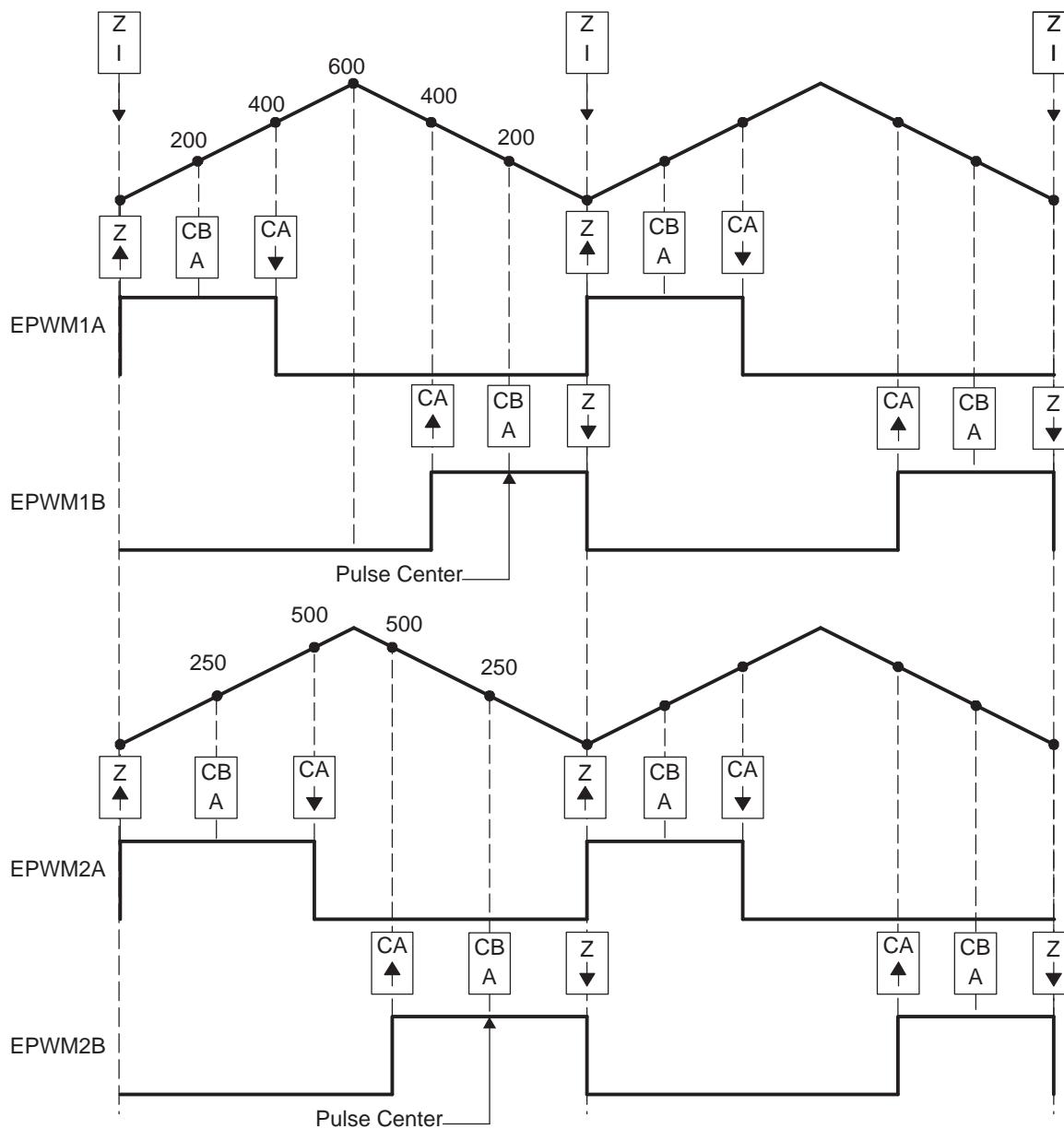
Figure 12-65. Control of Two Half-H Bridge Stages ($F_{\text{PWM}2} = N \times F_{\text{PWM}1}$)

Figure 12-66. Half-H Bridge Waveforms for Figure 12-65 (Note: Here $F_{PWM2} = F_{PWM1}$)


12.3.6 Controlling Dual 3-Phase Inverters for Motors (ACI and PMSM)

The idea of multiple modules controlling a single power stage can be extended to the 3-phase Inverter case. In such a case, six switching elements can be controlled using three PWM modules, one for each leg of the inverter. Each leg must switch at the same frequency and all legs must be synchronized. A master + two slaves configuration can easily address this requirement. [Figure 12-67](#) shows how six PWM modules can control two independent 3-phase Inverters; each running a motor.

As in the cases shown in the previous sections, we have a choice of running each inverter at a different frequency (module 1 and module 4 are masters as in [Figure 12-67](#)), or both inverters can be synchronized by using one master (module 1) and five slaves. In this case, the frequency of modules 4, 5, and 6 (all equal) can be integer multiples of the frequency for modules 1, 2, 3 (also all equal).

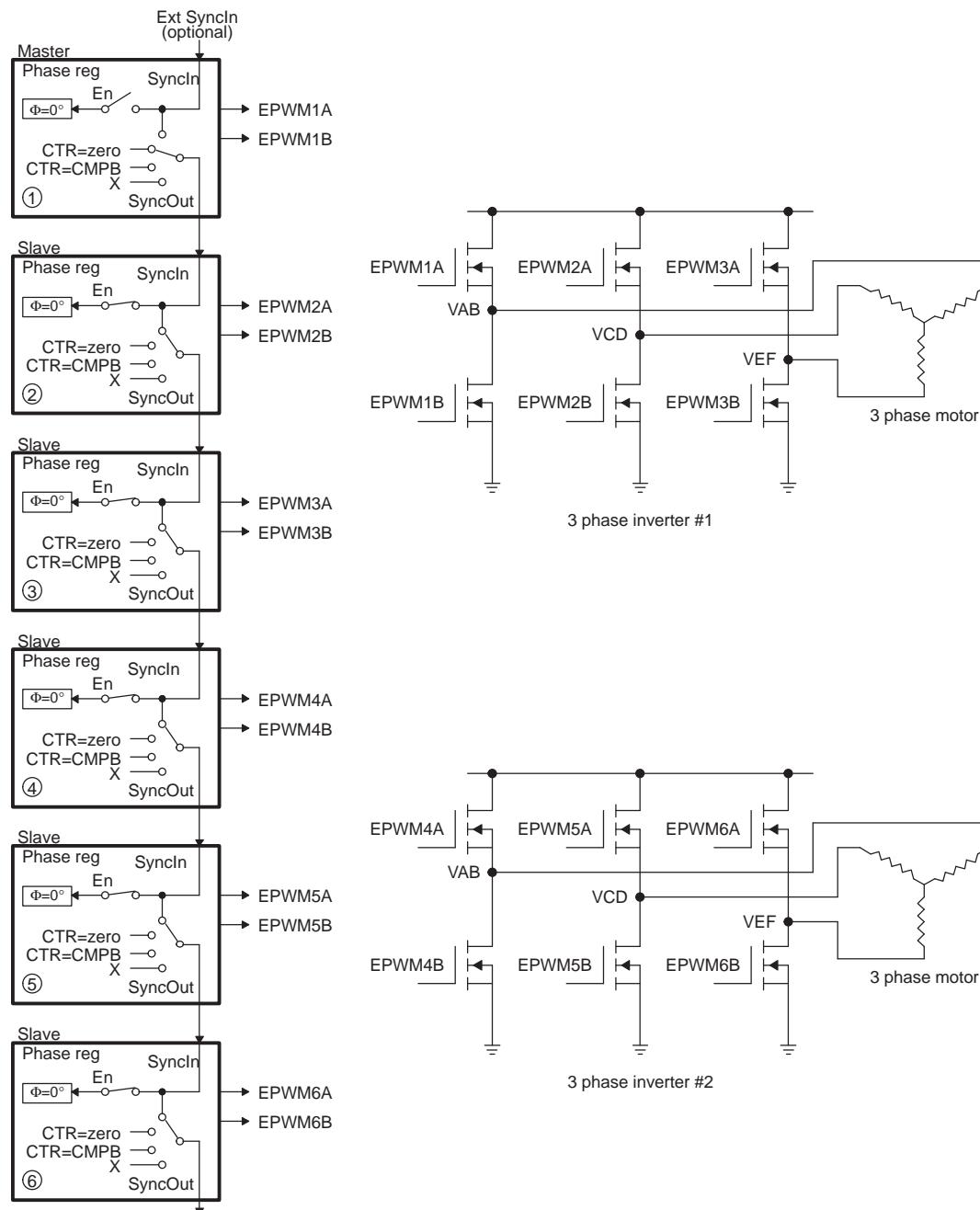
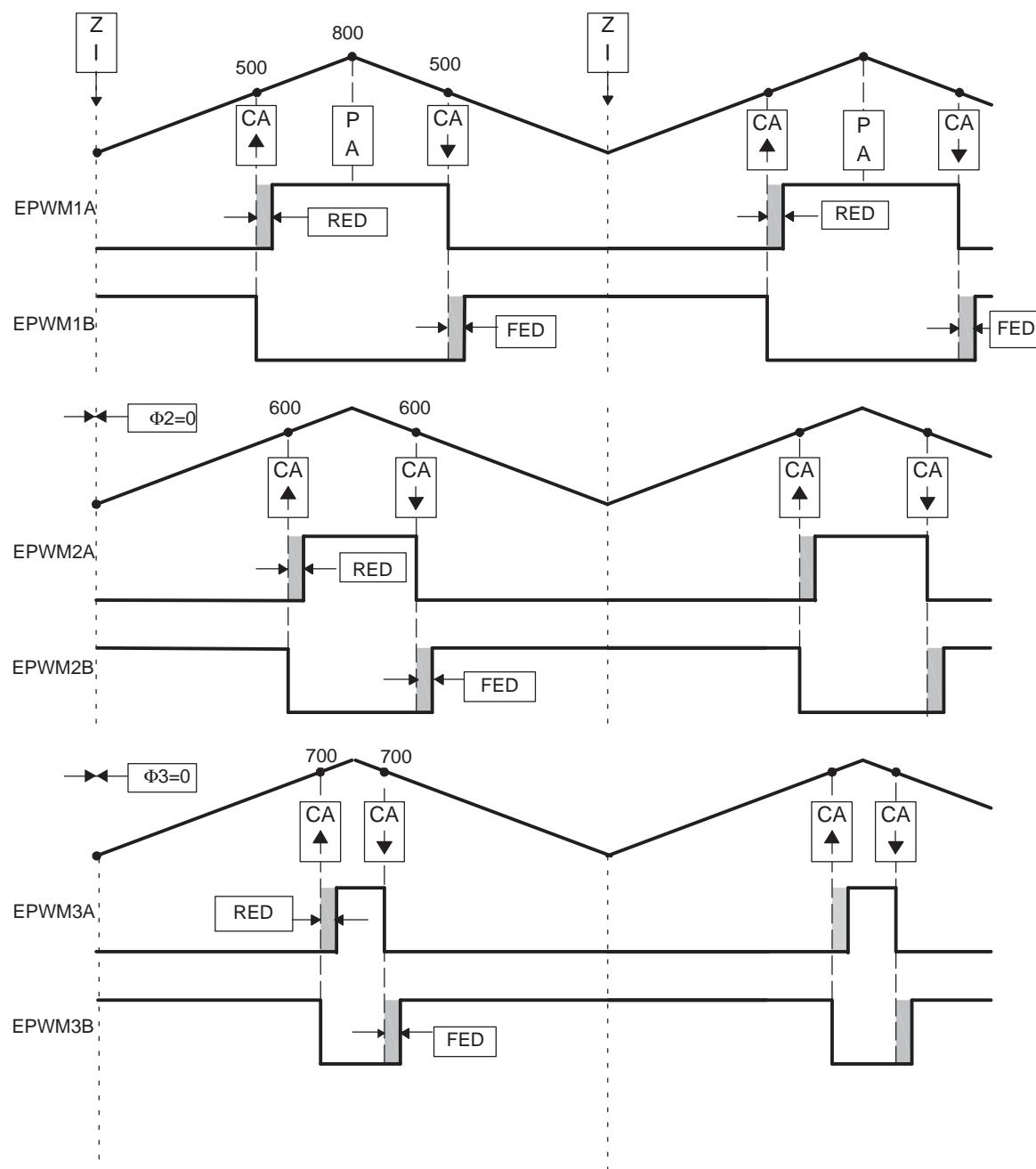
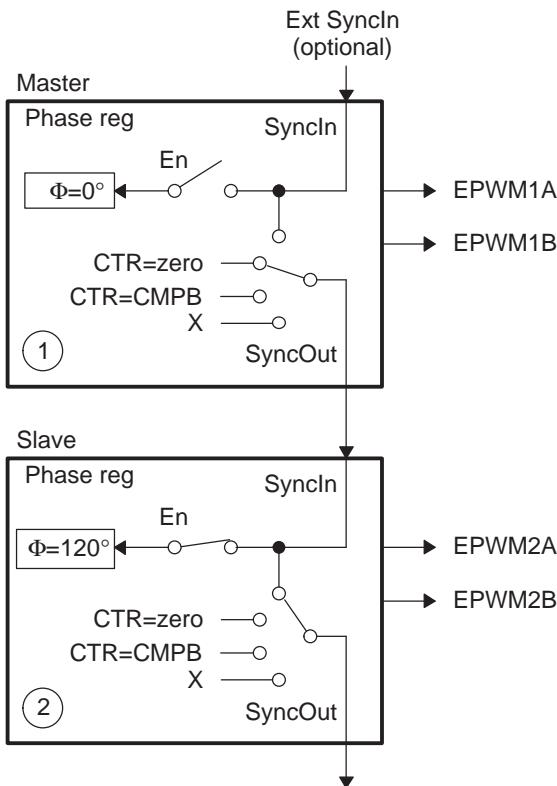
Figure 12-67. Control of Dual 3-Phase Inverter Stages as Is Commonly Used in Motor Control

Figure 12-68. 3-Phase Inverter Waveforms for Figure 12-67 (Only One Inverter Shown)


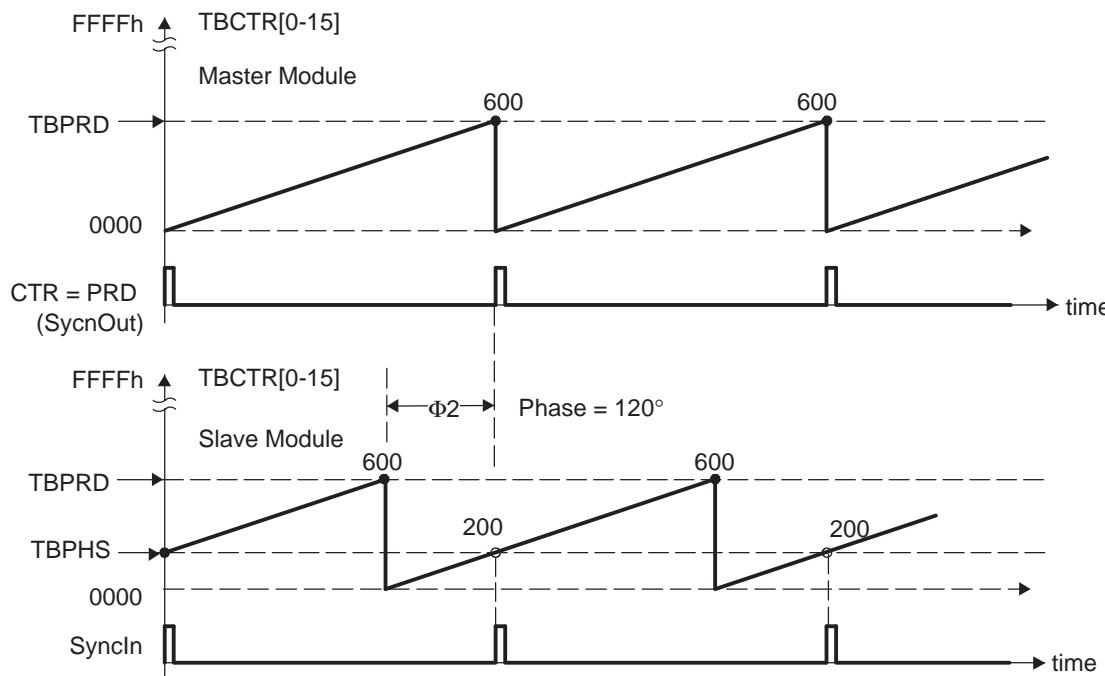
12.3.7 Practical Applications Using Phase Control Between PWM Modules

So far, none of the examples have made use of the phase register (TBPHS). It has either been set to zero or its value has been a don't care. However, by programming appropriate values into TBPHS, multiple PWM modules can address another class of power topologies that rely on phase relationship between legs (or stages) for correct operation. As described in the TB module section, a PWM module can be configured to allow a SyncIn pulse to cause the TBPHS register to be loaded into the TBCTR register. To illustrate this concept, [Figure 12-69](#) shows a master and slave module with a phase relationship of 120°, i.e., the slave leads the master.

Figure 12-69. Configuring Two PWM Modules for Phase Control



[Figure 12-70](#) shows the associated timing waveforms for this configuration. Here, TBPRD = 600 for both master and slave. For the slave, TBPHS = 200 (i.e., $200/600 \times 360^\circ = 120^\circ$). Whenever the master generates a SyncIn pulse (CTR = PRD), the value of TBPHS = 200 is loaded into the slave TBCTR register so the slave time-base is always leading the master's time-base by 120°.

Figure 12-70. Timing Waveforms Associated With Phase Control Between 2 Modules

12.3.8 Controlling a 3-Phase Interleaved DC/DC Converter

A popular power topology that makes use of phase-offset between modules is shown in [Figure 12-71](#). This system uses three PWM modules, with module 1 configured as the master. To work, the phase relationship between adjacent modules must be $F = 120^\circ$. This is achieved by setting the slave TBPHS registers 2 and 3 with values of $1/3$ and $2/3$ of the period value, respectively. For example, if the period register is loaded with a value of 600 counts, then $TBPHS$ (slave 2) = 200 and $TBPHS$ (slave 3) = 400. Both slave modules are synchronized to the master 1 module.

This concept can be extended to four or more phases, by setting the TBPHS values appropriately. The following formula gives the TBPHS values for N phases:

$$TBPHS(N,M) = (TBPRD/N) \times (-1)$$

Where:

N = number of phases

M = PWM module number

For example, for the 3-phase case (N=3), $TBPRD = 600$,

$$TBPHS(3,2) = (600/3) \times (2-1) = 200 \text{ (i.e., Phase value for Slave module 2)}$$

$$TBPHS(3,3) = 400 \text{ (i.e., Phase value for Slave module 3)}$$

[Figure 12-72](#) shows the waveforms for the configuration in [Figure 12-71](#).

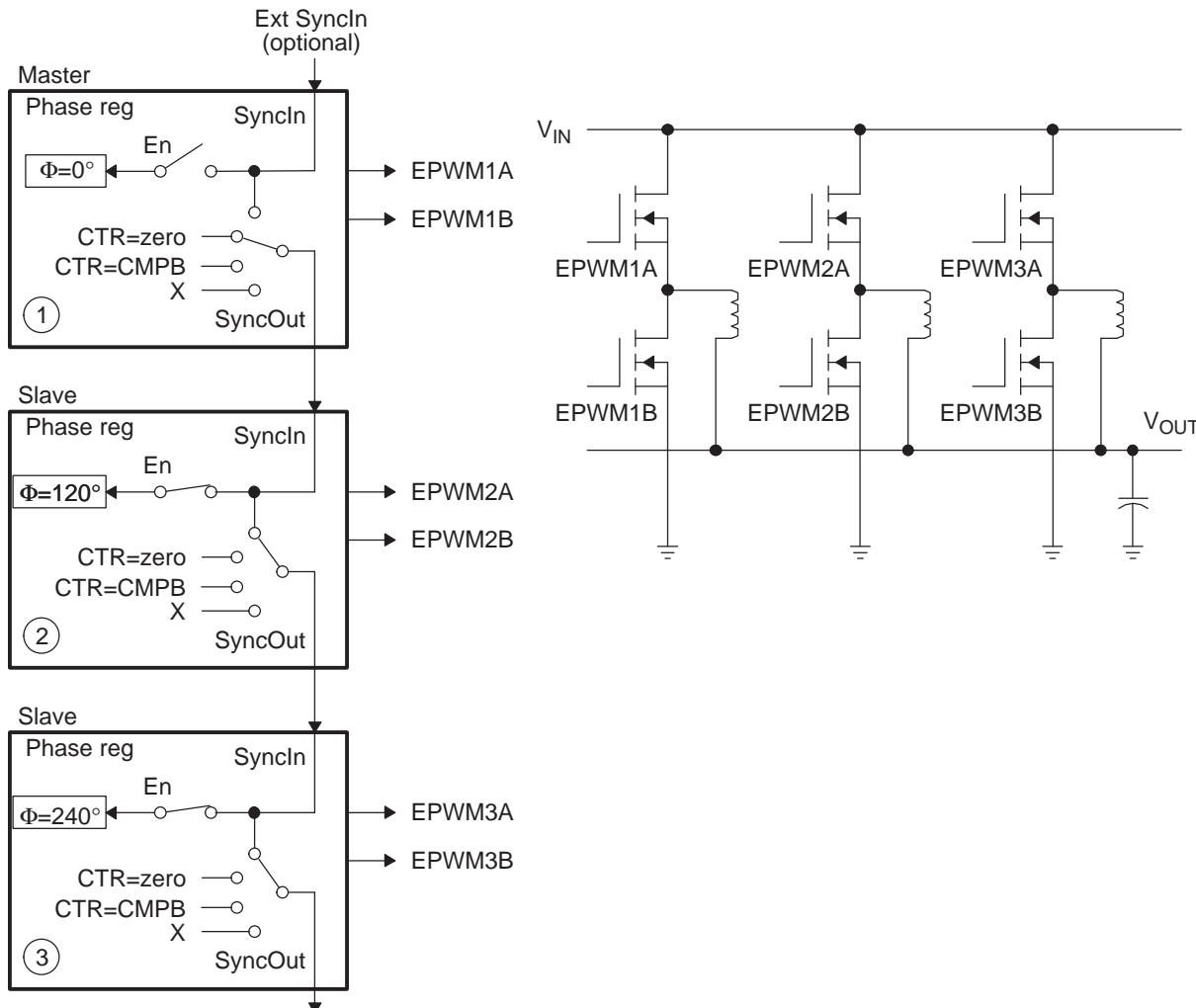
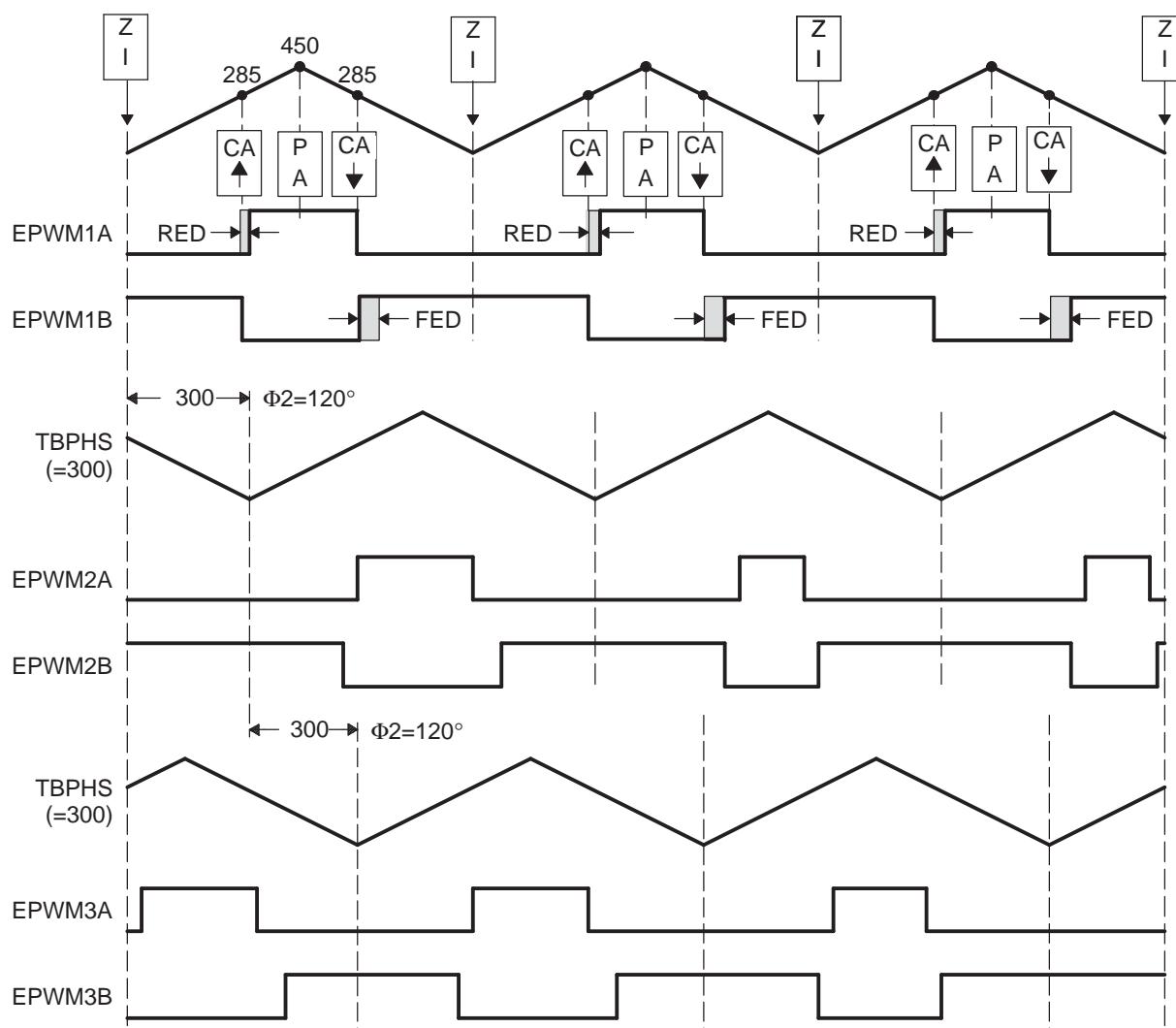
Figure 12-71. Control of a 3-Phase Interleaved DC/DC Converter

Figure 12-72. 3-Phase Interleaved DC/DC Converter Waveforms for Figure 12-71


12.3.9 Controlling Zero Voltage Switched Full Bridge (ZVSFB) Converter

The example given in [Figure 12-73](#) assumes a static or constant phase relationship between legs (modules). In such a case, control is achieved by modulating the duty cycle. It is also possible to dynamically change the phase value on a cycle-by-cycle basis. This feature lends itself to controlling a class of power topologies known as *phase-shifted full bridge*, or *zero voltage switched full bridge*. Here the controlled parameter is not duty cycle (this is kept constant at approximately 50 percent); instead it is the phase relationship between legs. Such a system can be implemented by allocating the resources of two PWM modules to control a single power stage, which in turn requires control of four switching elements. [Figure 12-74](#) shows a master/slave module combination synchronized together to control a full H-bridge. In this case, both master and slave modules are required to switch at the same PWM frequency. The phase is controlled by using the slave's phase register (TBPMS). The master's phase register is not used and therefore can be initialized to zero.

Figure 12-73. Controlling a Full-H Bridge Stage ($F_{\text{PWM}2} = F_{\text{PWM}1}$)

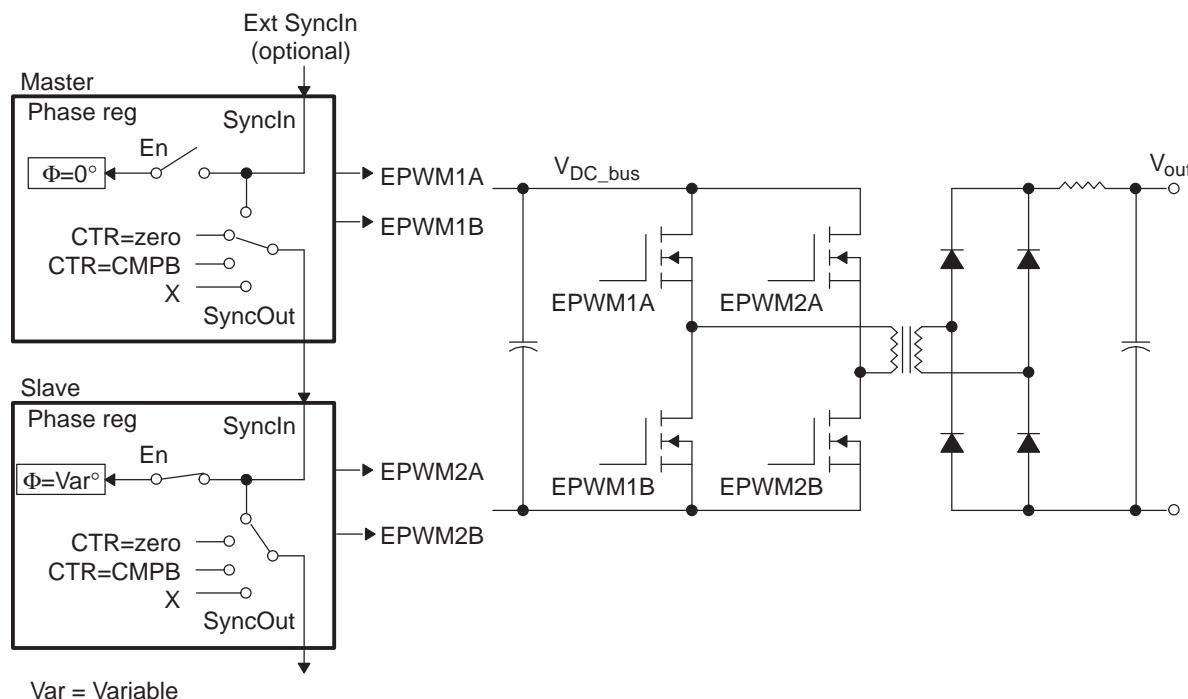
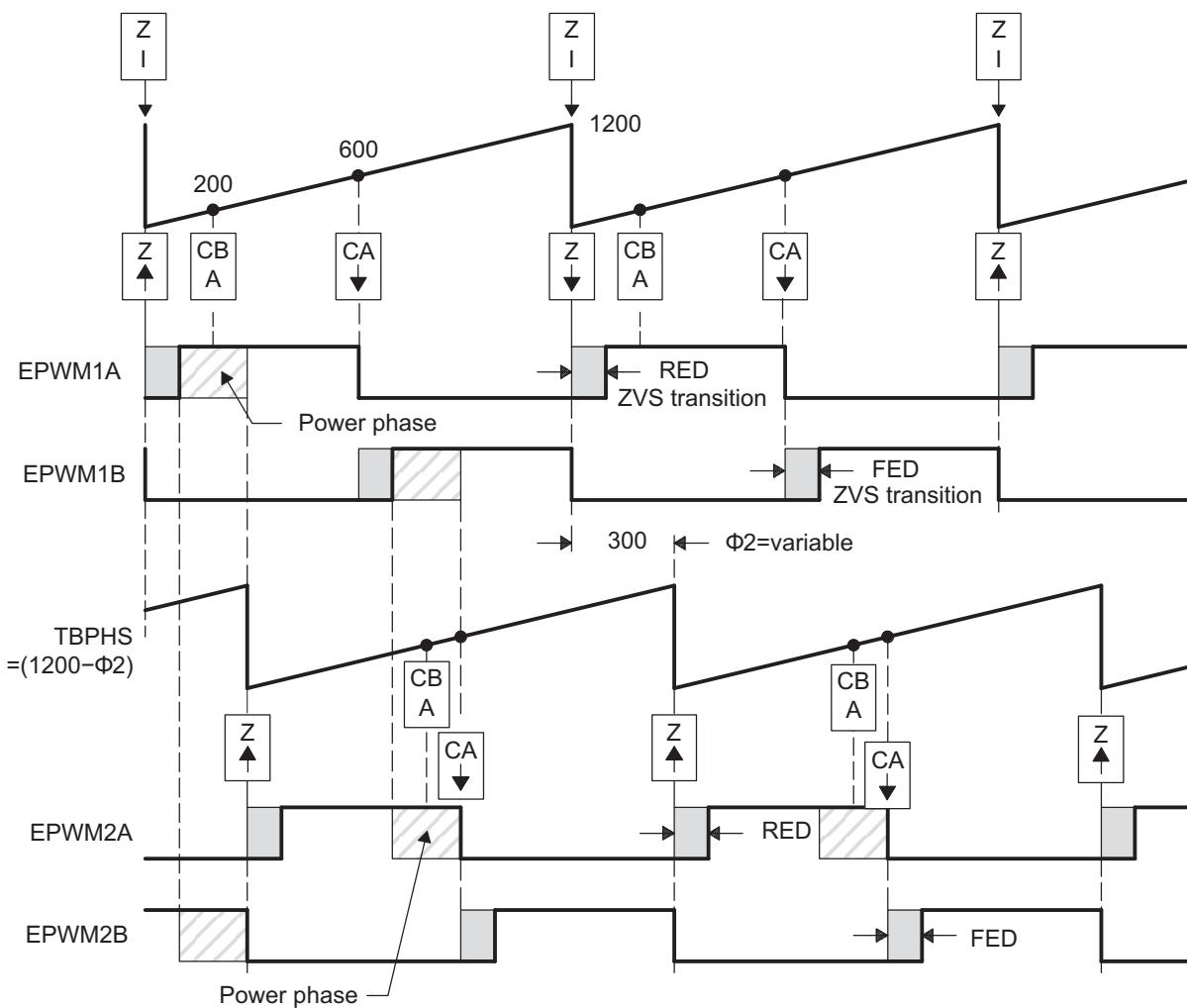
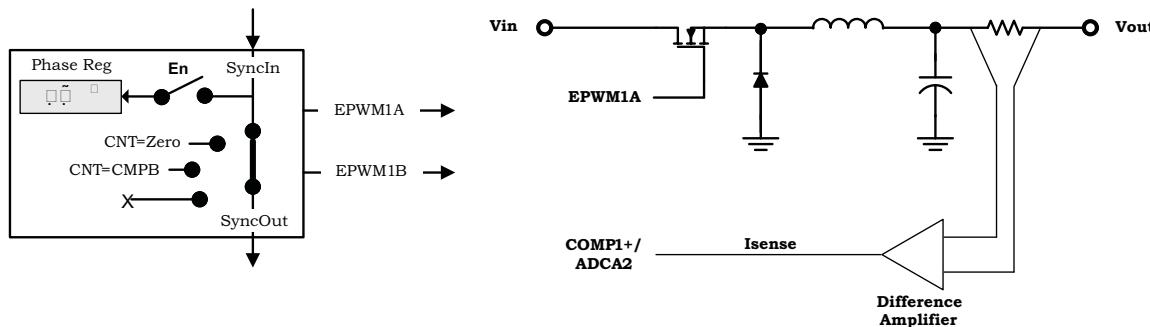
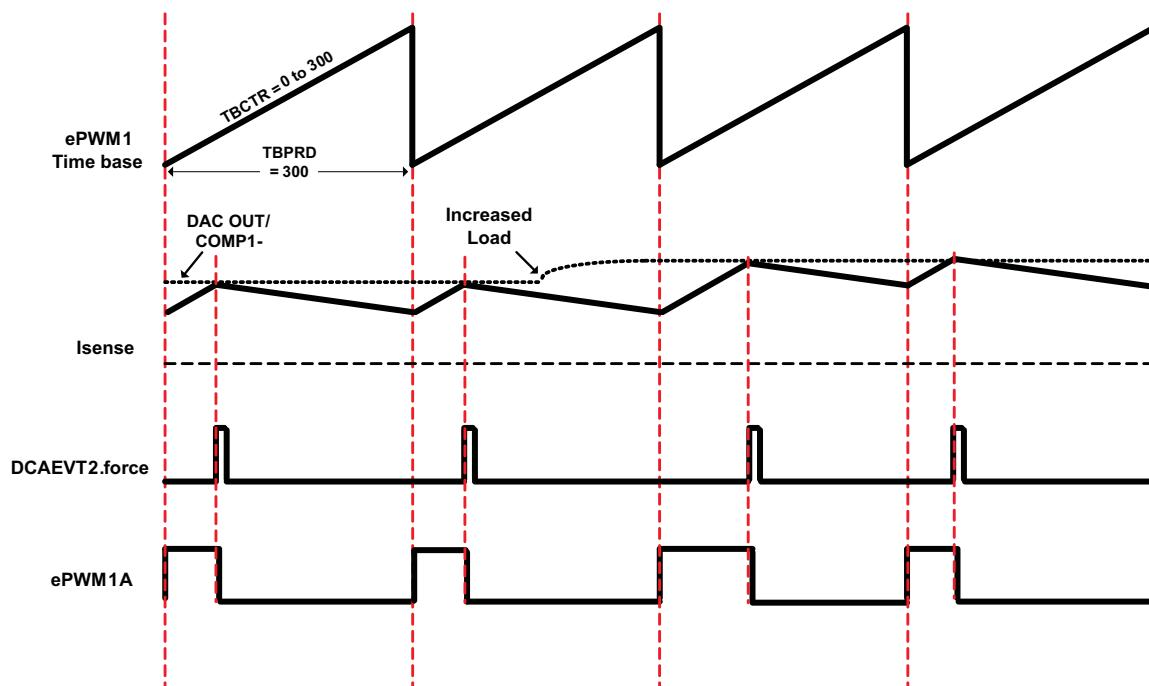


Figure 12-74. ZVS Full-H Bridge Waveforms


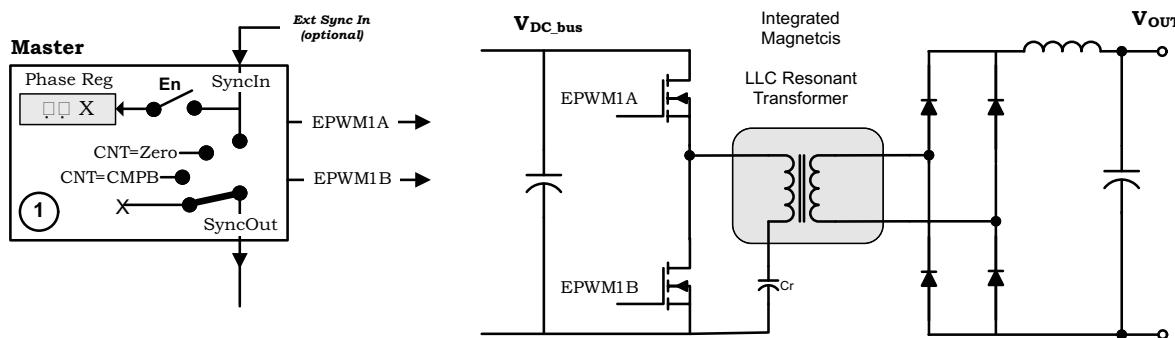
12.3.10 Controlling a Peak Current Mode Controlled Buck Module

Peak current control techniques offer a number of benefits like automatic over current limiting, fast correction for input voltage variations and reducing magnetic saturation. [Figure 12-75](#) shows the use of ePWM1A along with the on-chip analog comparator for buck converter topology. The output current is sensed through a current sense resistor and fed to the positive terminal of the on-chip comparator. The internal programmable 10-bit DAC can be used to provide a reference peak current at the negative terminal of the comparator. Alternatively, an external reference could be connected at this input. The comparator output is an input to the Digital compare sub-module. The ePWM module is configured in such a way so as to trip the ePWM1A output as soon as the sensed current reaches the peak reference value. A cycle-by-cycle trip mechanism is used. [Figure 12-76](#) shows the waveforms generated by the configuration.

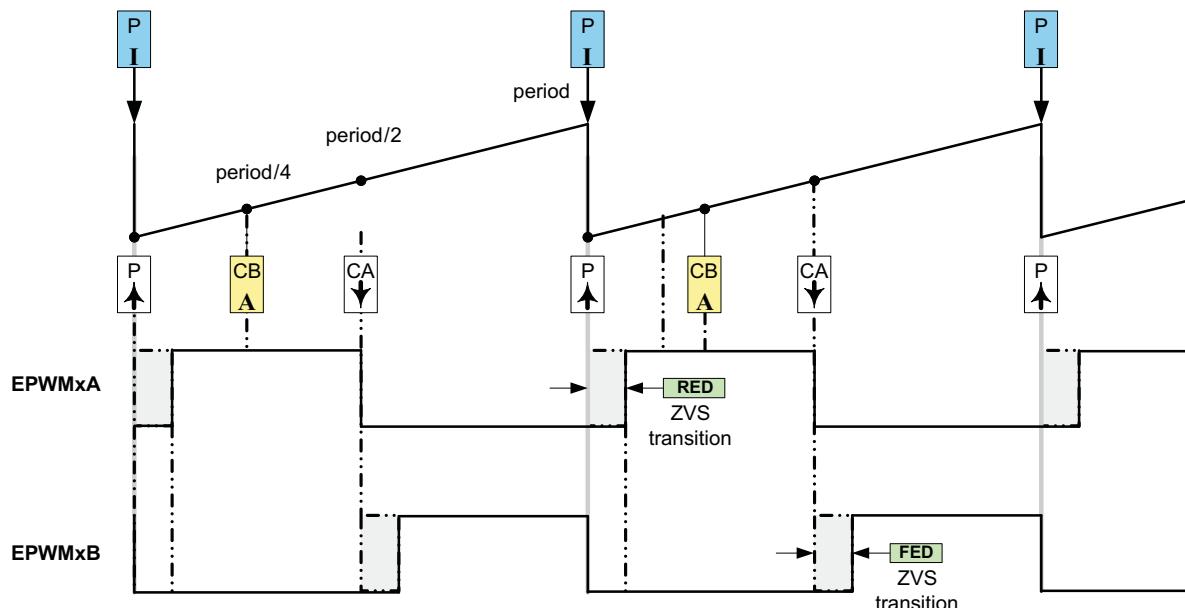
Figure 12-75. Peak Current Mode Control of a Buck Converter**Figure 12-76. Peak Current Mode Control Waveforms for Figure 12-75**

12.3.11 Controlling H-Bridge LLC Resonant Converter

Various topologies of resonant converters are well-known in the field of power electronics for many years. In addition to these, H-bridge LLC resonant converter topology has recently gained popularity in many consumer electronics applications where high efficiency and power density are required. In this example single channel configuration of ePWM1 is detailed, yet the configuration can easily be extended to multi channel. Here the controlled parameter is not duty cycle (this is kept constant at approximately 50 percent); instead it is frequency. Although the deadband is not controlled and kept constant as 300ns (i.e 30 @100MHz TBCLK), it is up to user to update it in real time to enhance the efficiency by adjusting enough time delay for soft switching.

Figure 12-77. Control of Two Resonant Converter Stages


NOTE: $\Theta = X$ indicates value in phase register is "don't care"

Figure 12-78. H-Bridge LLC Resonant Converter PWM Waveforms


Indicates this event triggers an interrupt



Indicates this event triggers an ADC start of conversion

12.4 Registers

12.4.1 EPWM Base Addresses

Table 12-15. EPWM Base Address Table

Device Register	Register Name	Start Address	End Address
EPwm1Regs	EPWM_REGS	0x0000_4000	0x0000_40FF
EPwm2Regs	EPWM_REGS	0x0000_4100	0x0000_41FF
EPwm3Regs	EPWM_REGS	0x0000_4200	0x0000_42FF
EPwm4Regs	EPWM_REGS	0x0000_4300	0x0000_43FF
EPwm5Regs	EPWM_REGS	0x0000_4400	0x0000_44FF
EPwm6Regs	EPWM_REGS	0x0000_4500	0x0000_45FF
EPwm7Regs	EPWM_REGS	0x0000_4600	0x0000_46FF
EPwm8Regs	EPWM_REGS	0x0000_4700	0x0000_47FF
EPwm9Regs	EPWM_REGS	0x0000_4800	0x0000_48FF
EPwm10Regs	EPWM_REGS	0x0000_4900	0x0000_49FF
EPwm11Regs	EPWM_REGS	0x0000_4A00	0x0000_4AFF
EPwm12Regs	EPWM_REGS	0x0000_4B00	0x0000_4BFF
EPwmXbarRegs ⁽¹⁾	EPWM_XBAR_REGS	0x0000_7A00	0x0000_7A3F
TrigRegs ⁽¹⁾	TRIG_REGS	0x0000_7940	0x0000_794F

⁽¹⁾ Only available on CPU1.

12.4.2 EPWM_REGS Registers

Table 12-16 lists the memory-mapped registers for the EPWM_REGS. All register offset addresses not listed in **Table 12-16** should be considered as reserved locations and the register contents should not be modified.

Table 12-16. EPWM_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	TBCTL	Time Base Control Register	Section 12.4.2.1	
1h	TBCTL2	Time Base Control Register 2	Section 12.4.2.2	
4h	TBCTR	Time Base Counter Register	Section 12.4.2.3	
5h	TBSTS	Time Base Status Register	Section 12.4.2.4	
8h	CMPCTL	Counter Compare Control Register	Section 12.4.2.5	
9h	CMPCTL2	Counter Compare Control Register 2	Section 12.4.2.6	
Ch	DBCTL	Dead-Band Generator Control Register	Section 12.4.2.7	
Dh	DBCTL2	Dead-Band Generator Control Register 2	Section 12.4.2.8	
10h	AQCTL	Action Qualifier Control Register	Section 12.4.2.9	
11h	AQTSRCSEL	Action Qualifier Trigger Event Source Select Register	Section 12.4.2.10	
14h	PCCTL	PWM Chopper Control Register	Section 12.4.2.11	
20h	HRCNFG	HRPWM Configuration Register	Section 12.4.2.12	EALLOW
21h	HRPWR	HRPWM Power Register	Section 12.4.2.13	EALLOW
26h	HRMSTEP	HRPWM MEP Step Register	Section 12.4.2.14	EALLOW
2Dh	HRPCTL	High Resolution Period Control Register	Section 12.4.2.15	EALLOW
34h	GLDCTL	Global PWM Load Control Register	Section 12.4.2.16	EALLOW
35h	GLDCFG	Global PWM Load Config Register	Section 12.4.2.17	EALLOW
38h	EPWMXLINK	EPWMx Link Register	Section 12.4.2.18	
40h	AQCTLA	Action Qualifier Control Register For Output A	Section 12.4.2.19	
41h	AQCTLA2	Additional Action Qualifier Control Register For Output A	Section 12.4.2.20	
42h	AQCTLB	Action Qualifier Control Register For Output B	Section 12.4.2.21	
43h	AQCTLB2	Additional Action Qualifier Control Register For Output B	Section 12.4.2.22	
47h	AQSFR	Action Qualifier Software Force Register	Section 12.4.2.23	
49h	AQCSFR	Action Qualifier Continuous S/W Force Register	Section 12.4.2.24	
50h	DBREDHR	Dead-Band Generator Rising Edge Delay High Resolution Mirror Register	Section 12.4.2.25	
51h	DBRED	Dead-Band Generator Rising Edge Delay High Resolution Mirror Register	Section 12.4.2.26	
52h	DBFEDHR	Dead-Band Generator Falling Edge Delay High Resolution Register	Section 12.4.2.27	
53h	DBFED	Dead-Band Generator Falling Edge Delay Count Register	Section 12.4.2.28	
60h	TBPHS	Time Base Phase High	Section 12.4.2.29	

Table 12-16. EPWM_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
62h	TBPRDHR	Time Base Period High Resolution Register	Section 12.4.2.30	
63h	TBPRD	Time Base Period Register	Section 12.4.2.31	
6Ah	CMPA	Counter Compare A Register	Section 12.4.2.32	
6Ch	CMPB	Compare B Register	Section 12.4.2.33	
6Fh	CMPC	Counter Compare C Register	Section 12.4.2.34	
71h	CMPD	Counter Compare D Register	Section 12.4.2.35	
74h	GLDCTL2	Global PWM Load Control Register 2	Section 12.4.2.36	
80h	TZSEL	Trip Zone Select Register	Section 12.4.2.37	EALLOW
82h	TZDCSEL	Trip Zone Digital Comparator Select Register	Section 12.4.2.38	EALLOW
84h	TZCTL	Trip Zone Control Register	Section 12.4.2.39	EALLOW
85h	TZCTL2	Additional Trip Zone Control Register	Section 12.4.2.40	EALLOW
86h	TZCTLDA	Trip Zone Control Register Digital Compare A	Section 12.4.2.41	EALLOW
87h	TZCTLDCA	Trip Zone Control Register Digital Compare B	Section 12.4.2.42	EALLOW
8Dh	TZEINT	Trip Zone Enable Interrupt Register	Section 12.4.2.43	EALLOW
93h	TZFLG	Trip Zone Flag Register	Section 12.4.2.44	
94h	TZCBCFLG	Trip Zone CBC Flag Register	Section 12.4.2.45	
95h	TZOSTFLG	Trip Zone OST Flag Register	Section 12.4.2.46	
97h	TZCLR	Trip Zone Clear Register	Section 12.4.2.47	EALLOW
98h	TZCBCCLR	Trip Zone CBC Clear Register	Section 12.4.2.48	EALLOW
99h	TZOSTCLR	Trip Zone OST Clear Register	Section 12.4.2.49	EALLOW
9Bh	TZFRC	Trip Zone Force Register	Section 12.4.2.50	EALLOW
A4h	ETSEL	Event Trigger Selection Register	Section 12.4.2.51	
A6h	ETPS	Event Trigger Pre-Scale Register	Section 12.4.2.52	
A8h	ETFLG	Event Trigger Flag Register	Section 12.4.2.53	
AAh	ETCLR	Event Trigger Clear Register	Section 12.4.2.54	
ACh	ETFRC	Event Trigger Force Register	Section 12.4.2.55	
AEh	ETINTPS	Event-Trigger Interrupt Pre-Scale Register	Section 12.4.2.56	

Table 12-16. EPWM_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
B0h	ETSOCPS	Event-Trigger SOC Pre-Scale Register	Section 12.4.2.57	
B2h	ETCNTINITCTL	Event-Trigger Counter Initialization Control Register	Section 12.4.2.58	
B4h	ETCNTINIT	Event-Trigger Counter Initialization Register	Section 12.4.2.59	
C0h	DCTRIPSEL	Digital Compare Trip Select Register	Section 12.4.2.60	EALLOW
C3h	DCACTL	Digital Compare A Control Register	Section 12.4.2.61	EALLOW
C4h	DCBCTL	Digital Compare B Control Register	Section 12.4.2.62	EALLOW
C7h	DCFCTL	Digital Compare Filter Control Register	Section 12.4.2.63	EALLOW
C8h	DCCAPCTL	Digital Compare Capture Control Register	Section 12.4.2.64	EALLOW
C9h	DCFOFFSET	Digital Compare Filter Offset Register	Section 12.4.2.65	
CAh	DCFOFFSETCNT	Digital Compare Filter Offset Counter Register	Section 12.4.2.66	
CBh	DCFWINDOW	Digital Compare Filter Window Register	Section 12.4.2.67	
CCh	DCFWINDOWCNT	Digital Compare Filter Window Counter Register	Section 12.4.2.68	
CFh	DCCAP	Digital Compare Counter Capture Register	Section 12.4.2.69	
D2h	DCAHTRIPSEL	Digital Compare AH Trip Select	Section 12.4.2.70	EALLOW
D3h	DCALTRIPSEL	Digital Compare AL Trip Select	Section 12.4.2.71	EALLOW
D4h	DCBHTRIPSEL	Digital Compare BH Trip Select	Section 12.4.2.72	EALLOW
D5h	DCBLTRIPSEL	Digital Compare BL Trip Select	Section 12.4.2.73	EALLOW

12.4.2.1 TBCTL Register (offset = 0h) [reset = 83h]

TBCTL is shown in [Figure 12-79](#) and described in [Table 12-17](#).

Time Base Control Register

Figure 12-79. TBCTL Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR		CLKDIV		HSPCLKDIV	
R/W-0h		R/W-0h		R/W-0h		R/W-1h	
7	6	5	4	3	2	1	0
HSPCLKDIV	SWFSYNC		SYNCOSEL	PRDLD	PHSEN		CTRMODE
R/W-1h	R=0/W=1-0h		R/W-0h	R/W-0h	R/W-0h		R/W-3h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-17. TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREE_SOFT	R/W	0h	Emulation Mode Bits. These bits select the behavior of the ePWM time-base counter during emulation events 00: Stop after the next time-base counter increment or decrement 01: Stop when counter completes a whole cycle: - Up-count mode: stop when the time-base counter = period (TBCTR = TBPRD) - Down-count mode: stop when the time-base counter = 0x00 (TBCTR = 0x00) - Up-down-count mode: stop when the time-base counter = 0x00 (TBCTR = 0x00) 1x: Free run
13	PHSDIR	R/W	0h	Phase Direction Bit This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter (TBCTR) will count after a synchronization event occurs and a new phase value is loaded from the phase (TBPHS) register. This is irrespective of the direction of the counter before the synchronization event.. In the up-count and down-count modes this bit is ignored. 0: Count down after the synchronization event. 1: Count up after the synchronization event.
12-10	CLKDIV	R/W	0h	Time Base Clock Pre-Scale Bits These bits select the time base clock pre-scale value (TBCLK = SYSCLKOUT/(HSPCLKDIV * CLKDIV): 000: /1 (default on reset) 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128

Table 12-17. TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-7	HSPCLKDIV	R/W	1h	<p>High Speed Time Base Clock Pre-Scale Bits These bits determine part of the time-base clock prescale value. $TBCLK = SYSCLKOUT / (HSPCLKDIV \times CLKDIV)$. This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager (EV) peripheral.</p> <p>000: /1 001: /2 (default on reset) 010: /4 011: /6 100: /8 101: /10 110: /12 111: /14</p>
6	SWFSYNC	R=0/W=1	0h	<p>Software Forced Sync Pulse 0: Writing a 0 has no effect and reads always return a 0. 1: Writing a 1 forces a one-time synchronization pulse to be generated. This event is ORed with the EPWMxSYNCI input of the ePWM module. SWFSYNC is valid (operates) only when EPWMxSYNCI is selected by SYNCSEL = 00.</p>
5-4	SYNCSEL	R/W	0h	<p>Sync Output Select 00: EPWMxSYNC 01: CTR = zero: Time-base counter equal to zero (TBCTR = 0x00) 10: CTR = CMPB : Time-base counter equal to counter-compare B (TBCTR = CMPB) 11: Disable EPWMxSYNCO signal</p>
3	PRDLD	R/W	0h	<p>Active Period Reg Load from Shadow Select 0: The period register (TBPRD) is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero. A write or read to the TBPRD register accesses the shadow register. 1: The period register (TBPRD) is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero and/or a sync event as determined by the TBCTL2[PRDLDSYNC] bit. A write/read to the TBPRD register accesses the shadow register.</p>
2	PHSEN	R/W	0h	<p>Counter Reg Load from Phase Reg Enable (CNTLDE) 0: Do not load the time-base counter (TBCTR) from the time-base phase register (TBPHS). 1: Allow Counter to be loaded from the Phase register (TBPHS) and shadow to active load events when an EPWMxSYNCI input signal occurs or a software-forced sync signal, see bit 6.</p>
1-0	CTRMODE	R/W	3h	<p>Counter Mode The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows: 00: Up-count mode 01: Down-count mode 10: Up-down count mode 11: Freeze counter operation (default on reset)</p>

12.4.2.2 TBCTL2 Register (offset = 1h) [reset = 0h]

TBCTL2 is shown in [Figure 12-80](#) and described in [Table 12-18](#).

Time Base Control Register 2

Figure 12-80. TBCTL2 Register

15	14	13	12	11	10	9	8
PRDLDSYNC		SYNCOSELX		RESERVED			
R/W-0h		R/W-0h			R=0-0h		
7	6	5	4	3	2	1	0
OSHTSYNC	OSHTSYNCMODE	SELFCLRTRREM		RESERVED			
R/W-0h	R/W-0h	R/W-0h			R=0-0h		

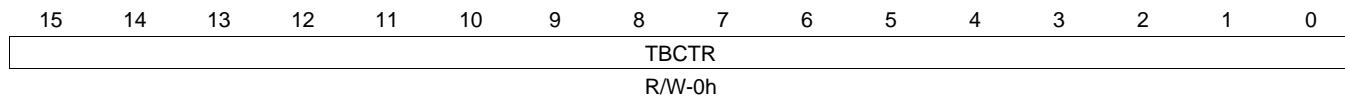
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-18. TBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	PRDLDSYNC	R/W	0h	Shadow to Active Period Register Load on SYNC event 00: Shadow to Active Load of TBRD occurs only when TBCTR = 0 (same as legacy). 01: Shadow to Active Load of TBRD occurs both when TBCTR = 0 and when SYNC occurs. 10: Shadow to Active Load of TBPRD occurs only when a SYNC is received. 11: Reserved Note: This bit selection is valid only if TBCTL[PRDLD]=0.
13-12	SYNCOSELX	R/W	0h	Extended selection bits for SYNCOUT 00: Disabled EPWMxSYNCO sync signal 01: EPWMxSYNCO = CMPC 10: EPWMxSYNCO = CMPD 11: Reserved
11-8	RESERVED	R=0	0h	Reserved
7	OSHTSYNC	R/W	0h	Oneshot sync bit 0: Writing a '0' has no effect. 1: Allow one sync pulse to propagate.
6	OSHTSYNCMODE	R/W	0h	Oneshot sync enable bit 0: Oneshot sync mode disabled 1: Oneshot sync mode enabled
5	SELFCLRTRREM	R/W	0h	Loop back sync pulse to enable self sync operation 0: Self clear function of TRREM disabled. 1: Self clear function of TRREM enabled
4-0	RESERVED	R=0	0h	Reserved

12.4.2.3 TBCTR Register (offset = 4h) [reset = 0h]TBCTR is shown in [Figure 12-81](#) and described in [Table 12-19](#).

Time Base Counter Register

Figure 12-81. TBCTR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

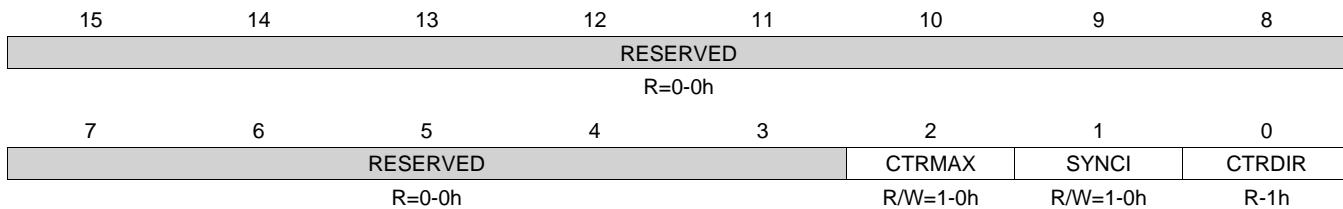
Table 12-19. TBCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TBCTR	R/W	0h	Time Base Counter Register

12.4.2.4 TBSTS Register (offset = 5h) [reset = 1h]

TBSTS is shown in [Figure 12-82](#) and described in [Table 12-20](#).

Time Base Status Register

Figure 12-82. TBSTS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-20. TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R=0	0h	Reserved
2	CTRMAX	R/W=1	0h	<p>Time-Base Counter Max Latched Status Bit 0: Reading a 0 indicates the time-base counter never reached its maximum value. Writing a 0 will have no effect. 1: Reading a 1 on this bit indicates that the time-base counter reached the max value 0xFFFF. Writing a 1 to this bit will clear the latched event.</p>
1	SYNCI	R/W=1	0h	<p>Input Synchronization Latched Status Bit 0: Writing a 0 will have no effect. Reading a 0 indicates no external synchronization event has occurred. 1: Reading a 1 on this bit indicates that an external synchronization event has occurred (EPWMxSYNCI). Writing a 1 to this bit will clear the latched event.</p>
0	CTRDIR	R	1h	<p>Time Base Counter Direction Status Bit At reset, the counter is frozen therefore, this bit has no meaning. To make this bit meaningful, you must first set the appropriate mode via TBCTL[CTRMODE]. 0: Time-Base Counter is currently counting down. 1: Time-Base Counter is currently counting up.</p>

12.4.2.5 CMPCTL Register (offset = 8h) [reset = 0h]

CMPCTL is shown in [Figure 12-83](#) and described in [Table 12-21](#).

Counter Compare Control Register

Figure 12-83. CMPCTL Register

15	14	13	12	11	10	9	8
RESERVED		LOADBSYNC		LOADASYNC		SHDWBFULL	SHDWAFULL
R=0-0h		R/W-0h		R/W-0h		R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	SHDWBMODE	RESERVED	SHDWAMODE	LOADBMODE		LOADAMODE	
R=0-0h	R/W-0h	R=0-0h	R/W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-21. CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R=0	0h	Reserved
13-12	LOADBSYNC	R/W	0h	Shadow to Active CMPB Register Load on SYNC event 00: Shadow to Active Load of CMPB:CMPBHR occurs according to LOADBMODE (bits 1,0) (same as legacy) 01: Shadow to Active Load of CMPB:CMPBHR occurs both according to LOADBMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPB:CMPBHR occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL[SHDWBMODE] = 0.
11-10	LOADASYNC	R/W	0h	Shadow to Active CMPA Register Load on SYNC event 00: Shadow to Active Load of CMPA:CMPAHR occurs according to LOADAMODE (bits 1,0) (same as legacy) 01: Shadow to Active Load of CMPA:CMPAHR occurs both according to LOADAMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPA:CMPAHR occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL[SHDWAMODE] = 0.
9	SHDWBFULL	R	0h	Counter-compare B (CMPB) Shadow Register Full Status Flag This bit self clears once a loadstrobe occurs. 0: CMPB shadow FIFO not full yet 1: Indicates the CMPB shadow FIFO is full a CPU write will overwrite current shadow value
8	SHDWAFULL	R	0h	Counter-compare A (CMPA) Shadow Register Full Status Flag The flag bit is set when a 32-bit write to CMPA:CMPAHR register or a 16-bit write to CMPA register is made. A 16-bit write to CMPAHR register will not affect the flag. This bit self clears once a load-strobe occurs. 0: CMPA shadow FIFO not full yet 1: Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value
7	RESERVED	R=0	0h	Reserved
6	SHDWBMODE	R/W	0h	Counter-compare B (CMPB) Register Operating Mode 0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1: Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action

Table 12-21. CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RESERVED	R=0	0h	Reserved
4	SHDWAMODE	R/W	0h	Counter-compare A (CMPA) Register Operating Mode 0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1: Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action
3-2	LOADBMODE	R/W	0h	Active Counter-Compare B (CMPB) Load From Shadow Select Mode This bit has no effect in immediate mode (CMPCTL[SHDWBMODE] = 1). 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible)
1-0	LOADAMODE	R/W	0h	Active Counter-Compare A (CMPA) Load From Shadow Select Mode This bit has no effect in immediate mode (CMPCTL[SHDWAMODE] = 1). 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible)

12.4.2.6 CMPCTL2 Register (offset = 9h) [reset = 0h]

CMPCTL2 is shown in [Figure 12-84](#) and described in [Table 12-22](#).

Counter Compare Control Register 2

Figure 12-84. CMPCTL2 Register

15	14	13	12	11	10	9	8
RESERVED		LOADDSYNC		LOADCSYNC		RESERVED	
R=0-0h		R/W-0h		R/W-0h		R=0-0h	
7	6	5	4	3	2	1	0
RESERVED	SHDWD MODE	RESERVED	SHDWCMODE	LOADDMODE		LOADCMODE	
R=0-0h	R/W-0h	R=0-0h	R/W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-22. CMPCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R=0	0h	Reserved
13-12	LOADDSYNC	R/W	0h	<p>Shadow to Active CMPD Register Load on SYNC event 00: Shadow to Active Load of CMPD occurs according to LOADCMODE 01: Shadow to Active Load of CMPD occurs both according to LOADCMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPD occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL2[SHDWD MODE] = 0.</p>
11-10	LOADCSYNC	R/W	0h	<p>Shadow to Active CMPC Register Load on SYNC event 00: Shadow to Active Load of CMPC occurs according to LOADCMODE 01: Shadow to Active Load of CMPC occurs both according to LOADCMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPC occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL2[SHDWCMODE] = 0.</p>
9-7	RESERVED	R=0	0h	Reserved
6	SHDWD MODE	R/W	0h	<p>Counter-Compare D Register Operating Mode 0: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1: Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action.</p>
5	RESERVED	R=0	0h	Reserved
4	SHDWCMODE	R/W	0h	<p>Counter-Compare C Register Operating Mode 0: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1: Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action.</p>

Table 12-22. CMPCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	LOADMODE	R/W	0h	<p>Active Counter-Compare D (CMFD) Load from Shadow Select Mode</p> <p>00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000)</p> <p>01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD)</p> <p>10: Load on either CTR = Zero or CTR = PRD</p> <p>11: Freeze (no loads possible)</p> <p>Note: Has no effect in Immediate mode.</p>
1-0	LOADCMODE	R/W	0h	<p>Active Counter-Compare C (CMPC) Load from Shadow Select Mode</p> <p>00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000)</p> <p>01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD)</p> <p>10: Load on either CTR = Zero or CTR = PRD</p> <p>11: Freeze (no loads possible)</p> <p>Note: Has no effect in Immediate mode.</p>

12.4.2.7 DBCTL Register (offset = Ch) [reset = 0h]

DBCTL is shown in [Figure 12-85](#) and described in [Table 12-23](#).

Dead-Band Generator Control Register

Figure 12-85. DBCTL Register

15	14	13	12	11	10	9	8
HALFCYCLE	DEDB_MODE	OUTSWAP		SHDWDBFED MODE	SHDWDBRED MODE	LOADFEDMODE	
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
LOADREDMODE		IN_MODE		POLSEL		OUT_MODE	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-23. DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HALFCYCLE	R/W	0h	Half Cycle Clocking Enable Bit 0: Full cycle clocking enabled. The dead-band counters are clocked at the TBCLK rate. 1: Half cycle clocking enabled. The dead-band counters are clocked at TBCLK*2.
14	DEDB_MODE	R/W	0h	Dead Band Dual-Edge B Mode Control (S8 switch) 0: Rising edge delay applied to InA/InB as selected by S4 switch (IN-MODE bits) on A signal path only. Falling edge delay applied to InA/InB as selected by S5 switch (INMODE bits) on B signal path only. 1: Rising edge delay and falling edge delay applied to source selected by S4 switch (INMODE bits) and output to B signal path only. Note: When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA OR OUTSWAP bits such that OutA=Bpath otherwise, OutA will be invalid.
13-12	OUTSWAP	R/W	0h	Dead Band Output Swap Control Bit 13 controls the S7 switch and bit 12 controls the S6 switch. 00: OutA and OutB signals are as defined by OUT-MODE bits. 01: OutA = A-path as defined by OUT-MODE bits. OutB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A signal path). 10: OutA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B signal path). OutB = B-path as defined by OUT-MODE bits. 11: OutA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B signal path). OutB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A signal path).
11	SHDWDBFEDMODE	R/W	0h	FED Dead-Band Load Mode 0: Immediate mode. Only the active DBFED register is used. All writes/reads via the CPU directly access the active register for immediate "FED dead-band action." 1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode (for compatibility with legacy).

Table 12-23. DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SHDWDBREDMODE	R/W	0h	<p>RED Dead-Band Load Mode</p> <p>0: Immediate mode. Only the active DBRED register is used. All writes/reads via the CPU directly access the active register for immediate "RED dead-band action."</p> <p>1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode (for compatibility with legacy).</p>
9-8	LOADFEDMODE	R/W	0h	<p>Active DBFED Load from Shadow Select Mode</p> <p>00: Load on Counter = 0 (CNT_eq)</p> <p>01: Load on Counter = Period (PRD_eq)</p> <p>10: Load on either Counter = 0, or Counter = Period</p> <p>11: Freeze (no loads possible)</p> <p>Note: has no effect in Immediate mode.</p>
7-6	LOADREDMODE	R/W	0h	<p>Active DBRED Load from Shadow Select Mode</p> <p>00: Load on Counter = 0 (CNT_eq)</p> <p>01: Load on Counter = Period (PRD_eq)</p> <p>10: Load on either Counter = 0, or Counter = Period</p> <p>11: Freeze (no loads possible)</p> <p>Note: has no effect in Immediate mode.</p>
5-4	IN_MODE	R/W	0h	<p>Dead-Band Input Mode Control</p> <p>Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is EPWMxA In is the source for both falling and rising-edge delays.</p> <p>00: EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay.</p> <p>01: EPWMxB In (from the action-qualifier) is the source for rising-edge delayed signal.</p> <p>EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal.</p> <p>10: EPWMxA In (from the action-qualifier) is the source for rising-edge delayed signal.</p> <p>EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal.</p> <p>11: EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.</p>
3-2	POLSEL	R/W	0h	<p>Polarity Select Control</p> <p>Bit 3 controls the S3 switch and bit 2 controls the S2 switch. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0x0. Other enhanced modes are also possible, but not regarded as typical usage modes.</p> <p>00: Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default).</p> <p>01: Active low complementary (ALC) mode. EPWMxA is inverted.</p> <p>10: Active high complementary (AHC). EPWMxB is inverted.</p> <p>11: Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.</p>

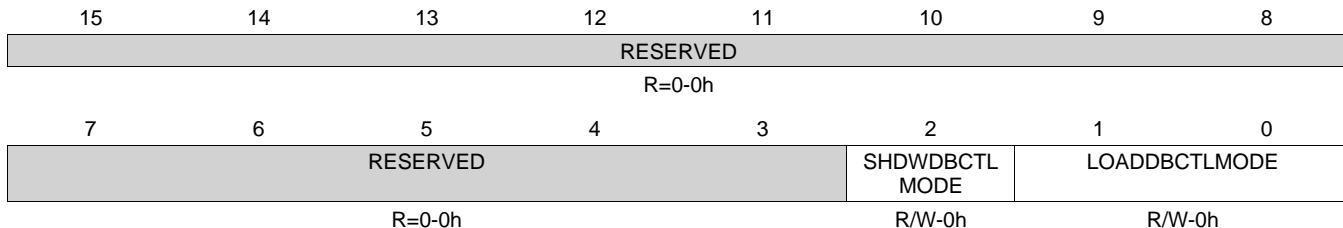
Table 12-23. DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	OUT_MODE	R/W	0h	<p>Dead-Band Output Mode Control</p> <p>Bit 1 controls the S1 switch and bit 0 controls the S0 switch.</p> <p>00: DBM is fully disabled or by-passed. In this mode the POLSEL and IN-MODE bits have no effect.</p> <p>01: Apath = InA (delay is by-passed for A signal path) Bpath = FED (Falling Edge Delay in B signal path)</p> <p>10: Apath = RED (Rising Edge Delay in A signal path) Bpath = InB (delay is by-passed for B signal path)</p> <p>11: DBM is fully enabled (i.e. both RED and FED active)</p>

12.4.2.8 DBCTL2 Register (offset = Dh) [reset = 0h]

DBCTL2 is shown in [Figure 12-86](#) and described in [Table 12-24](#).

Dead-Band Generator Control Register 2

Figure 12-86. DBCTL2 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-24. DBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R=0	0h	Reserved
2	SHDWDBCTL MODE	R/W	0h	<p>DBCTL Load Mode</p> <p>0: Immediate mode - only the Active DBCTL register is used. All writes/reads via the CPU directly access the Active register.</p> <p>1: Shadow mode - All writes and reads via the CPU access the Shadow register.</p>
1-0	LOADDBCTL MODE	R/W	0h	<p>Active DBCTL Load from Shadow Select Mode</p> <p>00: Load on Counter = 0 (CNT_eq)</p> <p>01: Load on Counter = Period (PRD_eq)</p> <p>10: Load on either Counter = 0, or Counter = Period</p> <p>11: Freeze (no loads possible)</p> <p>Note: has no effect in Immediate mode</p>

12.4.2.9 AQCTL Register (offset = 10h) [reset = 0h]

AQCTL is shown in [Figure 12-87](#) and described in [Table 12-25](#).

Action Qualifier Control Register

Figure 12-87. AQCTL Register

15	14	13	12	11	10	9	8
RESERVED				LDAQBSYNC	LDAQASYNC		
R=0-0h				R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	SHDWAQBMODE DE	RESERVED	SHDWAQAMODE DE	LDAQBMODE	LDAQAMODE		
R=0-0h	R/W-0h	R=0-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-25. AQCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11-10	LDAQBSYNC	R/W	0h	<p>Shadow to Active AQCTLB Register Load on SYNC event 00: Shadow to Active Load of AQCTLB occurs according to LDAQBMODE 01: Shadow to Active Load of AQCTLB occurs both according to LDAQBMODE bits and when SYNC occurs. 10: Shadow to Active Load of AQCTLB occurs only when a SYNC is received. 11: Reserved Note: This bit is valid only if AQCTLR[SHDWAQBMODE] = 1.</p>
9-8	LDAQASYNC	R/W	0h	<p>Shadow to Active AQCTLA Register Load on SYNC event 00: Shadow to Active Load of AQCTLA occurs according to LDAQAMODE 01: Shadow to Active Load of AQCTLA occurs both according to LDAQAMODE bits and when SYNC occurs. 10: Shadow to Active Load of AQCTLA occurs only when a SYNC is received. 11: Reserved Note: This bit is valid only if AQCTLR[SHDWAQAMODE] = 1.</p>
7	RESERVED	R=0	0h	Reserved
6	SHDWAQBMODE	R/W	0h	<p>Action Qualifier B Register operating mode 1: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0: Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register.</p>
5	RESERVED	R=0	0h	Reserved
4	SHDWAQAMODE	R/W	0h	<p>Action Qualifier A Register operating mode 1: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0: Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register.</p>

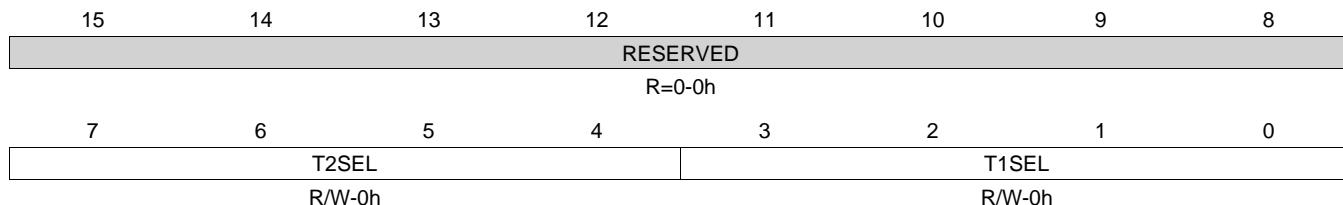
Table 12-25. AQCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	LDAQBMODE	R/W	0h	<p>Active Action Qualifier B Load from Shadow Select Mode</p> <p>00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000)</p> <p>01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD)</p> <p>10: Load on either CTR = Zero or CTR = PRD</p> <p>11: Freeze (no loads possible)</p> <p>Note: has no effect in Immediate mode.</p>
1-0	LDAQAMODE	R/W	0h	<p>Active Action Qualifier A Load from Shadow Select Mode</p> <p>00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000)</p> <p>01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD)</p> <p>10: Load on either CTR = Zero or CTR = PRD</p> <p>11: Freeze (no loads possible)</p> <p>Note: has no effect in Immediate mode.</p>

12.4.2.10 AQTSRCSEL Register (offset = 11h) [reset = 0h]

AQTSRCSEL is shown in [Figure 12-88](#) and described in [Table 12-26](#).

Action Qualifier Trigger Event Source Select Register

Figure 12-88. AQTSRCSEL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-26. AQTSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7-4	T2SEL	R/W	0h	T2 Event Source Select Bits 0000: DCAEVT1 0001: DCAEVT2 0010: DCBEVT1 0011: DCBEVT2 0100: TZ1 0101: TZ2 0110: TZ3 0111: EPWMxSYNCIN 1xxx: Reserved
3-0	T1SEL	R/W	0h	T1 Event Source Select Bits 0000: DCAEVT1 0001: DCAEVT2 0010: DCBEVT1 0011: DCBEVT2 0100: TZ1 0101: TZ2 0110: TZ3 0111: EPWMxSYNCIN 1xxx: Reserved

12.4.2.11 PCCTL Register (offset = 14h) [reset = 0h]

PCCTL is shown in [Figure 12-89](#) and described in [Table 12-27](#).

PWM Chopper Control Register

Figure 12-89. PCCTL Register

15	14	13	12	11	10	9	8
RESERVED						CHPDUTY	
R=0-0h						R/W-0h	
7	6	5	4	3	2	1	0
CHPFREQ			OSHTWTH			CHPEN	
R/W-0h			R/W-0h			R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-27. PCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R=0	0h	Reserved
10-8	CHPDUTY	R/W	0h	Chopping Clock Duty Cycle 000: Duty = 1/8 (12.5%) 001: Duty = 2/8 (25.0%) 010: Duty = 3/8 (37.5%) 011: Duty = 4/8 (50.0%) 100: Duty = 5/8 (62.5%) 101: Duty = 6/8 (75.0%) 110: Duty = 7/8 (87.5%) 111: Reserved
7-5	CHPFREQ	R/W	0h	Chopping Clock Frequency 000: Divide by 1 (no prescale, = 12.5 MHz at 100 MHz TBCLK) 001: Divide by 2 (6.25 MHz at 100 MHz TBCLK) 010: Divide by 3 (4.16 MHz at 100 MHz TBCLK) 011: Divide by 4 (3.12 MHz at 100 MHz TBCLK) 100: Divide by 5 (2.50 MHz at 100 MHz TBCLK) 101: Divide by 6 (2.08 MHz at 100 MHz TBCLK) 110: Divide by 7 (1.78 MHz at 100 MHz TBCLK) 111: Divide by 8 (1.56 MHz at 100 MHz TBCLK)

Table 12-27. PCCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-1	OSHTWTH	R/W	0h	One-Shot Pulse Width 0000: 1 x SYSCLKOUT / 8 wide (= 80 nS at 100 MHz SYSCLKOUT) 0001: 2 x SYSCLKOUT / 8 wide (= 160 nS at 100 MHz SYSCLKOUT) 0010: 3 x SYSCLKOUT / 8 wide (= 240 nS at 100 MHz SYSCLKOUT) 0011: 4 x SYSCLKOUT / 8 wide (= 320 nS at 100 MHz SYSCLKOUT) 0100: 5 x SYSCLKOUT / 8 wide (= 400 nS at 100 MHz SYSCLKOUT) 0101: 6 x SYSCLKOUT / 8 wide (= 480 nS at 100 MHz SYSCLKOUT) 0110: 7 x SYSCLKOUT / 8 wide (= 560 nS at 100 MHz SYSCLKOUT) 0111: 8 x SYSCLKOUT / 8 wide (= 640 nS at 100 MHz SYSCLKOUT) 1000: 9 x SYSCLKOUT / 8 wide (= 720 nS at 100 MHz SYSCLKOUT) 1001: 10 x SYSCLKOUT / 8 wide (= 800 nS at 100 MHz SYSCLKOUT) 1010: 11 x SYSCLKOUT / 8 wide (= 880 nS at 100 MHz SYSCLKOUT) 1011: 12 x SYSCLKOUT / 8 wide (= 960 nS at 100 MHz SYSCLKOUT) 1100: 13 x SYSCLKOUT / 8 wide (= 1040 nS at 100 MHz SYSCLKOUT) 1101: 14 x SYSCLKOUT / 8 wide (= 1120 nS at 100 MHz SYSCLKOUT) 1110: 15 x SYSCLKOUT / 8 wide (= 1200 nS at 100 MHz SYSCLKOUT) 1111: 16 x SYSCLKOUT / 8 wide (= 1280 nS at 100 MHz SYSCLKOUT)
0	CHPEN	R/W	0h	PWM-Chopping Enable 0: Disable (bypass) PWM chopping function 1: Enable chopping function

12.4.2.12 HRCNFG Register (offset = 20h) [reset = 0h]

HRCNFG is shown in [Figure 12-90](#) and described in [Table 12-28](#).

HRPWM Configuration Register

Figure 12-90. HRCNFG Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED		HRLOADB		CTLMODEB		EDGMODEB
R-0h	R=0-0h		R/W-0h		R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
SWAPAB	AUTOCONV	SELOUTB		HRLOAD	CTLMODE		EDGMODE
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-28. HRCNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R=0	0h	Reserved
12-11	HRLOADB	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPBHR shadow value into the active register. 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Reserved
10	CTLMODEB	R/W	0h	Control Mode Bits Selects the register (CMP/TBPRD or TBPHS) that controls the MEP: 0: CMPBHR(8) or TBPRDHR(8) Register controls the edge position (i.e., this is duty or period control mode). (Default on Reset) 1: TBPHSHR(8) Register controls the edge position (i.e., this is phase control mode).
9-8	EDGMODEB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic: 00: HRPWM capability is disabled (default on reset) 01: MEP control of rising edge (CMPBHR) 10: MEP control of falling edge (CMPBHR) 11: MEP control of both edges (TBPHSHR or TBPRDHR)
7	SWAPAB	R/W	0h	Swap ePWM A & B Output Signals This bit enables the swapping of the A & B signal outputs. The selection is as follows: 0: ePWMxA and ePWMxB outputs are unchanged. 1: ePWMxA signal appears on ePWMxB output and ePWMxB signal appears on ePWMxA output.

Table 12-28. HRCNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AUTOCONV	R/W	0h	<p>Auto Convert Delay Line Value</p> <p>Selects whether the fractional duty cycle/period/phase in the CMPAHR/TBPRDHR/TBPHSHR register is automatically scaled by the MEP scale factor in the HRMSTEP register or manually scaled by calculations in application software. The SFO library function automatically updates the HRMSTEP register with the appropriate MEP scale factor.</p> <p>0: Automatic HRMSTEP scaling is disabled. 1: Automatic HRMSTEP scaling is enabled.</p> <p>If application software is manually scaling the fractional duty cycle, or phase (i.e. software sets CMPAHR = (fraction(PWMduty * PWMperiod) * MEP Scale Factor)<<8 + 0x080 for duty cycle), then this mode must be disabled.</p>
5	SELOUTB	R/W	0h	<p>EPWMxB Output Select Bit</p> <p>This bit selects which signal is output on the ePWMxB channel output.</p> <p>0: ePWMxB output is normal. 1: ePWMxB output is inverted version of ePWMxA signal.</p>
4-3	HRLOAD	R/W	0h	<p>Shadow Mode Bit</p> <p>Selects the time event that loads the CMPAHR shadow value into the active register.</p> <p>00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Reserved</p>
2	CTLMODE	R/W	0h	<p>Control Mode Bits</p> <p>Selects the register (CMP/TBPRD or TBPHS) that controls the MEP:</p> <p>0: CMPAHR(8) or TBPRDHR(8) Register controls the edge position (i.e., this is duty or period control mode). (Default on Reset) 1: TBPHSHR(8) Register controls the edge position (i.e., this is phase control mode).</p>
1-0	EDGMODE	R/W	0h	<p>Edge Mode Bits</p> <p>Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic:</p> <p>00: HRPWM capability is disabled (default on reset) 01: MEP control of rising edge (CMPAHR) 10: MEP control of falling edge (CMPAHR) 11: MEP control of both edges (TBPHSHR or TBPRDHR)</p>

12.4.2.13 HRPWR Register (offset = 21h) [reset = 0h]

HRPWR is shown in [Figure 12-91](#) and described in [Table 12-29](#).

HRPWM Power Register

Figure 12-91. HRPWR Register

15	14	13	12	11	10	9	8
CALPWRON	RESERVED				RESERVED		
R/W-0h	R=0-0h				R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

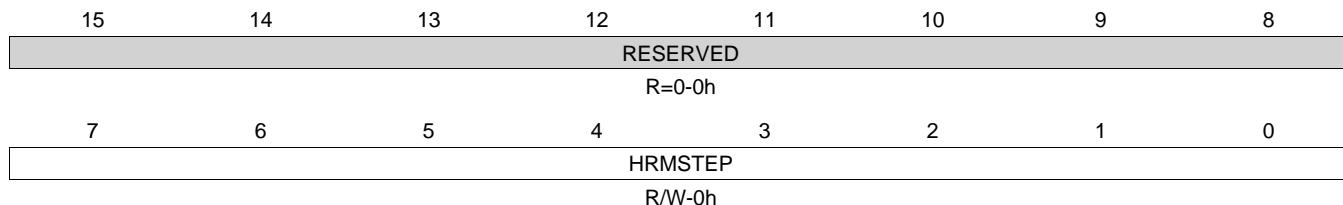
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-29. HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	R/W	0h	MEP Calibration Power Bits 0: Disables MEP calibration logic in the HRPWM and reduces power consumption. 1: Enables MEP calibration logic
14-10	RESERVED	R=0	0h	Reserved
9-6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1-0	RESERVED	R	0h	Reserved

12.4.2.14 HRMSTEP Register (offset = 26h) [reset = 0h]HRMSTEP is shown in [Figure 12-92](#) and described in [Table 12-30](#).

HRPWM MEP Step Register

Figure 12-92. HRMSTEP Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-30. HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7-0	HRMSTEP	R/W	0h	High Resolution MEP Step When auto-conversion is enabled (HRCNFG[AUTOCONV] = 1), This 8-bit field contains the MEP_ScaleFactor (number of MEP steps per coarse steps) used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run.

12.4.2.15 HRPCTL Register (offset = 2Dh) [reset = 0h]

HRPCTL is shown in [Figure 12-93](#) and described in [Table 12-31](#).

High Resolution Period Control Register

Figure 12-93. HRPCTL Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED		PWMSYNCSELX		RESERVED	TBPHSHRLOAD	RESERVED	HRPE
R=0-0h		R/W-0h		R-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-31. HRPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R=0	0h	Reserved
6-4	PWMSYNCSELX	R/W	0h	<p>PWMSYNCX Source Select Bit</p> <p>000: PWMSYNC is defined by TRCTL[PWMSYNCSEL] -> default condition (compatible with previous EPWM versions)</p> <p>001: Reserved</p> <p>010: Reserved</p> <p>011: Reserved</p> <p>100: PWMSYNC = CMPC_eq, Count direction Up</p> <p>101: PWMSYNC = CMPC_eq, Count direction Down</p> <p>110: PWMSYNC = CMPD_eq, Count direction Up</p> <p>111: PWMSYNC = CMPD_eq, Count direction Down</p>
3	RESERVED	R	0h	Reserved
2	TBPHSHRLOAD	R/W	0h	<p>TBPHSHR Load Enable</p> <p>This bit allows you to synchronize ePWM modules with a high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event. This allows for multiple ePWM modules operating at the same frequency to be phase aligned with high-resolution.</p> <p>0: Disables synchronization of high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event:</p> <p>1: Synchronize the high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital comparator synchronization event. The phase is synchronized using the contents of the high-resolution phase TBPHSHR register. The TBCTL[PHSEN] bit which enables the loading of the TBCTR register with TBPHS register value on a SYNCIN or TBCTL[SWFSYNC] event works independently. However, users need to enable this bit also if they want to control phase in conjunction with the high-resolution period feature.</p> <p>This bit and the TBCTL[PHSEN] bit must be set to 1 when high-resolution period is enabled for up-down count mode even if TBPHSHR = 0x0000. This bit does not need to be set when only high-resolution duty is enabled.</p>
1	RESERVED	R	0h	Reserved
0	HRPE	R/W	0h	<p>High Resolution Period Enable Bit</p> <p>0: High resolution period feature disabled. In this mode the ePWM behaves as a Type 0 ePWM.</p> <p>1: High resolution period enabled. In this mode the HRPWM module can control high-resolution of both the duty and frequency. When high-resolution period is enabled, TBCTL[CTRMODE] = 0,1 (down-count mode) is not supported.</p>

12.4.2.16 GLDCTL Register (offset = 34h) [reset = 0h]

GLDCTL is shown in [Figure 12-94](#) and described in [Table 12-32](#).

Global PWM Load Control Register

Figure 12-94. GLDCTL Register

15	14	13	12	11	10	9	8
RESERVED			GLDCNT			GLDPRD	
R=0-0h			R-0h			R/W-0h	
7	6	5	4	3	2	1	0
GLDPRD	RESERVED	OSHTMODE	GLDMODE			GLD	
R/W-0h	R=0-0h	R/W-0h	R/W-0h			R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-32. GLDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R=0	0h	Reserved
12-10	GLDCNT	R	0h	Global Reload Strobe Counter Register These bits indicate how many selected events have occurred: 000: No events 001: 1 event 010: 2 events 011: 3 events 100: 4 events 101: 5 events 110: 6 events 111: 7 events
9-7	GLDPRD	R/W	0h	Global Reload Strobe Period Select Register These bits select how many selected events need to occur before a load strobe is generated 000: Disable counter 001: Generate strobe on GLDCNT = 001 (1st event) 010: Generate strobe on GLDCNT = 010 (2nd event) 011: Generate strobe on GLDCNT = 011 (3rd event) 100: Generate strobe on GLDCNT = 011 (4th event) 101: Generate strobe on GLDCNT = 001 (5th event) 110: Generate strobe on GLDCNT = 010 (6th event) 111: Generate strobe on GLDCNT = 011 (7th event)
6	RESERVED	R=0	0h	Reserved
5	OSHTMODE	R/W	0h	One Shot Load Mode Control Bit 0: One shot load mode is disabled and shadow to active loading happens continuously on all the chosen load strobes. 1: One shot mode is active. All load strobes are blocked until GLDCTL2[OSHTLD] is written with 1. Note: One Shot mode can only be used with global shadow to active load mode enabled (GLDCTL[GLD]=1)

Table 12-32. GLDCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-1	GLDMODE	R/W	0h	<p>Global Load Pulse selection for Shadow to Active Mode Reloads</p> <p>0000: Load on Counter = 0 (CNT_ZRO)</p> <p>0001: Load on Counter = Period (PRD_EQ)</p> <p>0010: Load on either Counter = 0, or Counter = Period</p> <p>0011: Load on SYNCCEVT - this is logical OR of DCAEV1.sync, DCBEVT1.sync, EPWMxSYNC1 and TBCTL[SWFSYNC]</p> <p>0100: Load on SYNCCEVT or CNT_ZRO</p> <p>0101: Load on SYNCCEVT or PRD_EQ</p> <p>0110: Load on SYNCCEVT or CNT_ZRO or PRD_EQ</p> <p>1000: Reserved</p> <p>...</p> <p>1110: Reserved</p> <p>1111: Load on GLDCTL[GLDFRCLD] write</p>
0	GLD	R/W	0h	<p>Global Shadow to Active Load Event Control</p> <p>0: Shadow to active reload for all shadowed registers happens as per the individual reload control bits specified (Compatible with previous EPWM versions).</p> <p>1: When set, all the shadow to active reload events are defined by GLDMODE bits in GLDCTL register. All the shadow registers use same reload pulse from shadow to active reloading. Individual LOADMODE bits are ignored.</p>

12.4.2.17 GLDCFG Register (offset = 35h) [reset = 0h]

GLDCFG is shown in [Figure 12-95](#) and described in [Table 12-33](#).

Global PWM Load Config Register

Figure 12-95. GLDCFG Register

15	14	13	12	11	10	9	8
RESERVED				AQCSFRC	AQCTLB_AQC TLB2	AQCTLA_AQC TLA2	
				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DBCTL	DBFED_DBFE DHR	DBRED_DBRE DHR	CMPD	CMPC	CMPB_CMPBH R	CMPA_CMPAH R	TBPRD_TBPR DHR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-33. GLDCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R=0	0h	Reserved
10	AQCSFRC	R/W	0h	Global load event configuration for AQCSFRC 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
9	AQCTLB_AQCTLB2	R/W	0h	Global load event configuration for AQCTLB_AQCTLB2 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
8	AQCTLA_AQCTLA2	R/W	0h	Global load event configuration for AQCTLA_AQCTLA2 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
7	DBCTL	R/W	0h	Global load event configuration for DBCTL 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
6	DBFED_DBFEDHR	R/W	0h	Global load event configuration for DBFED_DBFEDHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
5	DBRED_DBREDHR	R/W	0h	Global load event configuration for DBRED_DBREDHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
4	CMPD	R/W	0h	Global load event configuration for CMPD 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1

Table 12-33. GLDCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMPC	R/W	0h	Global load event configuration for CMPC 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
2	CMPB_CMPBHR	R/W	0h	Global load event configuration for CMPB_CMPBHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
1	CMPA_CMPAHR	R/W	0h	Global load event configuration for CMPA_CMPAHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1
0	TBPRD_TBPRDHHR	R/W	0h	Global load event configuration for TBPRD_TBPRDHHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global reload configuration if this bit is set and GLDCTL(GLD)=1

12.4.2.18 EPWMXLINK Register (offset = 38h) [reset = 0h]

EPWMXLINK is shown in [Figure 12-96](#) and described in [Table 12-34](#).

EPWMx Link Register

Figure 12-96. EPWMXLINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
					RESERVED										CMPDLINK
					R=0-0h										R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					CMPCLINK			CMPBLINK			CMPALINK			TBPRDLINK	
					R/W-0h			R/W-0h			R/W-0h			R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-34. EPWMXLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GLDCTL2LINK	R/W	0h	GLDCTL2 Link Bits Writes to the GLDCTL2 registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's GLDCTL2 registers. 0000: ePWM1 0001: ePWM2 0010: ePWM3 0011: ePWM4 0100: ePWM5 0101: ePWM6 0110: ePWM7 0111: ePWM8 1000: ePWM9 1001: ePWM10 1010: ePWM11 1011: ePWM12 1100: Reserved ... 1111: Reserved
27-20	RESERVED	R=0	0h	Reserved

Table 12-34. EPWMXLINK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	CMPDLINK	R/W	0h	<p>CMPD Link Bits</p> <p>Writes to the CMPD registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPD registers.</p> <ul style="list-style-type: none"> 0000: ePWM1 0001: ePWM2 0010: ePWM3 0011: ePWM4 0100: ePWM5 0101: ePWM6 0110: ePWM7 0111: ePWM8 1000: ePWM9 1001: ePWM10 1010: ePWM11 1011: ePWM12 1100: Reserved ... 1111: Reserved
15-12	CMPCLINK	R/W	0h	<p>CMPC Link Bits</p> <p>Writes to the CMPC registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPC registers.</p> <ul style="list-style-type: none"> 0000: ePWM1 0001: ePWM2 0010: ePWM3 0011: ePWM4 0100: ePWM5 0101: ePWM6 0110: ePWM7 0111: ePWM8 1000: ePWM9 1001: ePWM10 1010: ePWM11 1011: ePWM12 1100: Reserved ... 1111: Reserved

Table 12-34. EPWMXLINK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	CMPBLINK	R/W	0h	<p>CMPB_CMPBHR Link Bits</p> <p>Writes to the CMPB_CMPBHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPB_CMPBHR registers.</p> <p>0000: ePWM1 0001: ePWM2 0010: ePWM3 0011: ePWM4 0100: ePWM5 0101: ePWM6 0110: ePWM7 0111: ePWM8 1000: ePWM9 1001: ePWM10 1010: ePWM11 1011: ePWM12 1100: Reserved ... 1111: Reserved</p>
7-4	CMPALINK	R/W	0h	<p>CMPA_CMPAHR Link Bits</p> <p>Writes to the CMPA_CMPAHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPA_CMPAHR registers.</p> <p>0000: ePWM1 0001: ePWM2 0010: ePWM3 0011: ePWM4 0100: ePWM5 0101: ePWM6 0110: ePWM7 0111: ePWM8 1000: ePWM9 1001: ePWM10 1010: ePWM11 1011: ePWM12 1100: Reserved ... 1111: Reserved</p>

Table 12-34. EPWMXLINK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	TBPRDLINK	R/W	0h	<p>TBPRD_TBPRDHR Link Bits</p> <p>Writes to the TBPRD:TBPRDHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's TBPRD_TBPRDHR registers.</p> <p>0000: ePWM1 0001: ePWM2 0010: ePWM3 0011: ePWM4 0100: ePWM5 0101: ePWM6 0110: ePWM7 0111: ePWM8 1000: ePWM9 1001: ePWM10 1010: ePWM11 1011: ePWM12 1100: Reserved ... 1111: Reserved</p>

12.4.2.19 AQCTLA Register (offset = 40h) [reset = 0h]

AQCTLA is shown in [Figure 12-97](#) and described in [Table 12-35](#).

Action Qualifier Control Register For Output A

Figure 12-97. AQCTLA Register

15	14	13	12	11	10	9	8
RESERVED			CBD		CBU		
R=0-0h			R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-35. AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
9-8	CBU	R/W	0h	Action When TBCTR = CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
7-6	CAD	R/W	0h	Action When TBCTR = CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
5-4	CAU	R/W	0h	Action When TBCTR = CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

Table 12-35. AQCTLA Register Field Descriptions (continued)

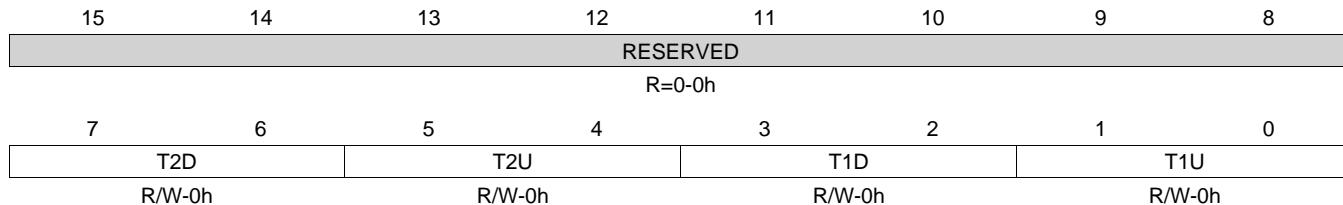
Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	<p>Action When TBCTR = TBPRD</p> <p>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.</p> <p>00: Do nothing (action disabled)</p> <p>01: Clear: force EPWMxA output low.</p> <p>10: Set: force EPWMxA output high.</p> <p>11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.</p>
1-0	ZRO	R/W	0h	<p>Action When TBCTR = 0</p> <p>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.</p> <p>00: Do nothing (action disabled)</p> <p>01: Clear: force EPWMxA output low.</p> <p>10: Set: force EPWMxA output high.</p> <p>11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.</p>

12.4.2.20 AQCTLA2 Register (offset = 41h) [reset = 0h]

AQCTLA2 is shown in [Figure 12-98](#) and described in [Table 12-36](#).

Additional Action Qualifier Control Register For Output A

Figure 12-98. AQCTLA2 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-36. AQCTLA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7-6	T2D	R/W	0h	<p>Action when event occurs on T2 in DOWN-Count</p> <p>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.</p> <p>00: Do nothing (action disabled)</p> <p>01: Clear: force EPWMxA output low.</p> <p>10: Set: force EPWMxA output high.</p> <p>11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.</p>
5-4	T2U	R/W	0h	<p>Action when event occurs on T2 in UP-Count</p> <p>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.</p> <p>00: Do nothing (action disabled)</p> <p>01: Clear: force EPWMxA output low.</p> <p>10: Set: force EPWMxA output high.</p> <p>11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.</p>
3-2	T1D	R/W	0h	<p>Action when event occurs on T1 in DOWN-Count</p> <p>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.</p> <p>00: Do nothing (action disabled)</p> <p>01: Clear: force EPWMxA output low.</p> <p>10: Set: force EPWMxA output high.</p> <p>11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.</p>
1-0	T1U	R/W	0h	<p>Action when event occurs on T1 in UP-Count</p> <p>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.</p> <p>00: Do nothing (action disabled)</p> <p>01: Clear: force EPWMxA output low.</p> <p>10: Set: force EPWMxA output high.</p> <p>11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.</p>

12.4.2.21 AQCTLB Register (offset = 42h) [reset = 0h]

AQCTLB is shown in [Figure 12-99](#) and described in [Table 12-37](#).

Action Qualifier Control Register For Output B

Figure 12-99. AQCTLB Register

15	14	13	12	11	10	9	8
RESERVED			CBD		CBU		
R=0-0h			R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-37. AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
9-8	CBU	R/W	0h	Action When TBCTR = CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
7-6	CAD	R/W	0h	Action When TBCTR = CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
5-4	CAU	R/W	0h	Action When TBCTR = CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

Table 12-37. AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
1-0	ZRO	R/W	0h	Action When TBCTR = 0 Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

12.4.2.22 AQCTLB2 Register (offset = 43h) [reset = 0h]

AQCTLB2 is shown in [Figure 12-100](#) and described in [Table 12-38](#).

Additional Action Qualifier Control Register For Output B

Figure 12-100. AQCTLB2 Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
T2D		T2U		T1D		T1U	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-38. AQCTLB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7-6	T2D	R/W	0h	Action when event occurs on T2 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
5-4	T2U	R/W	0h	Action when event occurs on T2 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
3-2	T1D	R/W	0h	Action when event occurs on T1 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
1-0	T1U	R/W	0h	Action when event occurs on T1 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

12.4.2.23 AQSFRC Register (offset = 47h) [reset = 0h]

AQSFRC is shown in [Figure 12-101](#) and described in [Table 12-39](#).

Action Qualifier Software Force Register

Figure 12-101. AQSFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RLDCSF	OTSF _B		ACTSF _B	OTSF _A		ACTSF _A	
R/W-0h	R=0/W=1-0h		R/W-0h	R=0/W=1-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

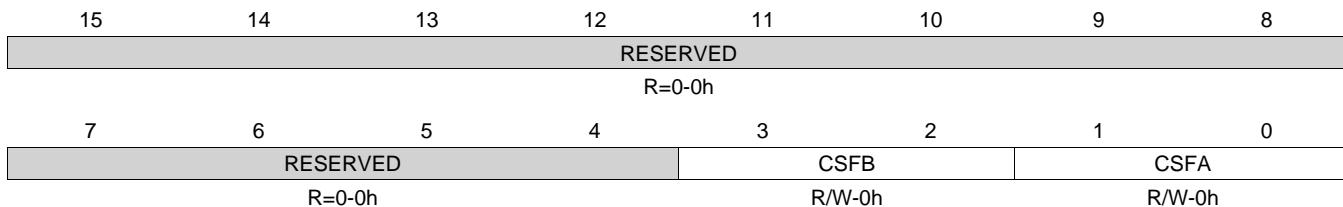
Table 12-39. AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7-6	RLDCSF	R/W	0h	AQCSFRC Active Register Reload From Shadow Options 00: Load on event counter equals zero 01: Load on event counter equals period 10: Load on event counter equals zero or counter equals period 11: Load immediately (the active register is directly accessed by the CPU and is not loaded from the shadow register).
5	OTSF _B	R=0/W=1	0h	One-Time Software Forced Event on Output B 0: Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete, i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on output B. 1: Initiates a single s/w forced event
4-3	ACTSF _B	R/W	0h	Action When One-Time Software Force B is Invoked 00: Does nothing (action disabled) 01: Clear (low) 10: Set (high) 11: Toggle (Low -> High, High -> Low) Note: This action is not qualified by counter direction (CNT_dir)
2	OTSF _A	R=0/W=1	0h	One-Time Software Forced Event on Output A 0: Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated). 1: Initiates a single software forced event
1-0	ACTSF _A	R/W	0h	Action When One-Time Software Force A Is Invoked 00: Does nothing (action disabled) 01: Clear (low) 10: Set (high) 11: Toggle (Low -> High, High -> Low) Note: This action is not qualified by counter direction (CNT_dir)

12.4.2.24 AQCSFRC Register (offset = 49h) [reset = 0h]

AQCSFRC is shown in [Figure 12-102](#) and described in [Table 12-40](#).

Action Qualifier Continuous S/W Force Register

Figure 12-102. AQCSFRC Register

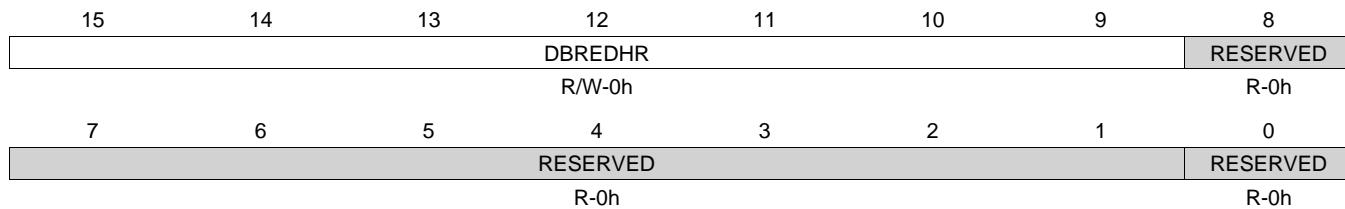
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-40. AQCSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3-2	CSFB	R/W	0h	<p>Continuous Software Force on Output B</p> <p>In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. To configure shadow mode, use AQSFRC[RLDCSF].</p> <p>00: Forcing disabled, i.e., has no effect</p> <p>01: Forces a continuous low on output B</p> <p>10: Forces a continuous high on output B</p> <p>11: Software forcing is disabled and has no effect</p>
1-0	CSFA	R/W	0h	<p>Continuous Software Force on Output A</p> <p>In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register.</p> <p>00: Forcing disabled, i.e., has no effect</p> <p>01: Forces a continuous low on output A</p> <p>10: Forces a continuous high on output A</p> <p>11: Software forcing is disabled and has no effect</p>

12.4.2.25 DBREDHR Register (offset = 50h) [reset = 0h]DBREDHR is shown in [Figure 12-103](#) and described in [Table 12-41](#).

Dead-Band Generator Rising Edge Delay High Resolution Mirror Register

Figure 12-103. DBREDHR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-41. DBREDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	DBREDHR	R/W	0h	Dead Band Rising Edge Delay High Resolution Bits
8	RESERVED	R	0h	Reserved
7-1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

12.4.2.26 DBRED Register (offset = 51h) [reset = 0h]

DBRED is shown in [Figure 12-104](#) and described in [Table 12-42](#).

Dead-Band Generator Rising Edge Delay High Resolution Mirror Register

Figure 12-104. DBRED Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-42. DBRED Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DBRED	R/W	0h	Rising edge delay value

12.4.2.27 DBFEDHR Register (offset = 52h) [reset = 0h]DBFEDHR is shown in [Figure 12-105](#) and described in [Table 12-43](#).

Dead-Band Generator Falling Edge Delay High Resolution Register

Figure 12-105. DBFEDHR Register

15	14	13	12	11	10	9	8
DBFEDHR							RESERVED
R/W-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-0h							R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

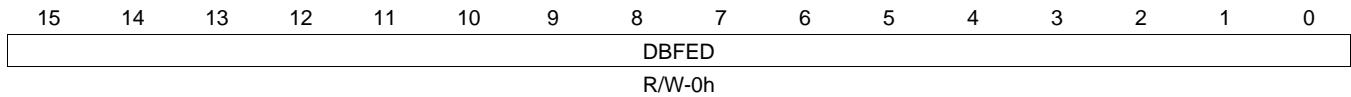
Table 12-43. DBFEDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	DBFEDHR	R/W	0h	Dead Band Falling Edge Delay High Resolution Bits
8	RESERVED	R	0h	Reserved
7-1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

12.4.2.28 DBFED Register (offset = 53h) [reset = 0h]

DBFED is shown in [Figure 12-106](#) and described in [Table 12-44](#).

Dead-Band Generator Falling Edge Delay Count Register

Figure 12-106. DBFED Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-44. DBFED Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DBFED	R/W	0h	Falling Edge Delay Count 14-bit counter

12.4.2.29 TBPHS Register (offset = 60h) [reset = 0h]TBPHS is shown in [Figure 12-107](#) and described in [Table 12-45](#).

Time Base Phase High

Figure 12-107. TBPHS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBPHS																TBPHSHRRESERVED															
R/W-0h																R/W-0hR-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-45. TBPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TBPHS	R/W	0h	<p>Phase Offset Register</p> <p>These bits set time-base counter phase of the selected ePWM relative to the time-base that is supplying the synchronization input signal.</p> <ul style="list-style-type: none">- If TBCTL[PHSEN] = 0, then the synchronization event is ignored and the time-base counter is not loaded with the phase.- If TBCTL[PHSEN] = 1, then the time-base counter (TBCTR) will be loaded with the phase (TBPHS) when a synchronization event occurs. The synchronization event can be initiated by the input synchronization signal (EPWMxSYNCl) or by a software forced synchronization.
15-0	TBPHSHR	R/W	0h	Phase Offset (High Resolution) Register

12.4.2.30 TBPRDHR Register (offset = 62h) [reset = 0h]

TBPRDHR is shown in [Figure 12-108](#) and described in [Table 12-46](#).

Time Base Period High Resolution Register

Figure 12-108. TBPRDHR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBPRDHR															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-46. TBPRDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TBPRDHR	R/W	0h	<p>Period High Resolution Bits</p> <p>These 8-bits contain the high-resolution portion of the period value. The TBPRDHR register is not affected by the TBCTL[PRDLD] bit. Reads from this register always reflect the shadow register. Likewise writes are also to the shadow register. The TBPRDHR register is only used when the high resolution period feature is enabled. This register is only available with ePWM modules which support high-resolution period control.</p>

12.4.2.31 TBPRD Register (offset = 63h) [reset = 0h]TBPRD is shown in [Figure 12-109](#) and described in [Table 12-47](#).

Time Base Period Register

Figure 12-109. TBPRD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBPRD															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-47. TBPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TBPRD	R/W	0h	<p>Time Base Period Register</p> <p>These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit. By default this register is shadowed.</p> <ul style="list-style-type: none">- If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the active register will be loaded from the shadow register when the time-base counter equals zero.- If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware.- The active and shadow registers share the same memory map address.

12.4.2.32 CMPA Register (offset = 6Ah) [reset = 0h]

CMPA is shown in [Figure 12-110](#) and described in [Table 12-48](#).

Counter Compare A Register

Figure 12-110. CMPA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPA															CMPAHRRRESERVED																
R/W-0h															R/W-0hR-0h																

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-48. CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMPA	R/W	0h	<p>Compare A Register</p> <p>The value in the active CMPA register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include:</p> <ul style="list-style-type: none"> - Do nothing the event is ignored. - Clear: Pull the EPWMxA and/or EPWMxB signal low - Set: Pull the EPWMxA and/or EPWMxB signal high - Toggle the EPWMxA and/or EPWMxB signal <p>Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> - If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register. - Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full. - If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.
15-0	CMPAHR	R/W	0h	<p>Compare A HRPWM Extension Register</p> <p>These 8-bits contain the high-resolution portion (least significant 8-bits) of the counter-compare A value. CMPA:CMPAHR can be accessed in a single 32-bit read/write. Shadowing is enabled and disabled by the CMPCTL[SHDWAMODE] bit as described for the CMPA register.</p>

12.4.2.33 CMPB Register (offset = 6Ch) [reset = 0h]

CMPB is shown in [Figure 12-111](#) and described in [Table 12-49](#).

Compare B Register

Figure 12-111. CMPB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPB															RESERVED																
R/W-0h															R-0h																

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-49. CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMPB	R/W	0h	<p>Compare B Register</p> <p>The value in the active CMPB register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare B" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include:</p> <ul style="list-style-type: none"> - Do nothing the event is ignored. - Clear: Pull the EPWMxA and/or EPWMxB signal low - Set: Pull the EPWMxA and/or EPWMxB signal high - Toggle the EPWMxA and/or EPWMxB signal <p>Shadowing of this register is enabled and disabled by the CMPCTL[SHDWBMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> - If CMPCTL[SHDWBMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADBMODE] bit field determines which event will load the active register from the shadow register. - Before a write, the CMPCTL[SHDWBFULL] bit can be read to determine if the shadow register is currently full. - If CMPCTL[SHDWBMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.
15-0	RESERVED	R	0h	Reserved

12.4.2.34 CMPC Register (offset = 6Fh) [reset = 0h]

CMPC is shown in [Figure 12-112](#) and described in [Table 12-50](#).

Counter Compare C Register

Figure 12-112. CMPC Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPC															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-50. CMPC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMPC	R/W	0h	<p>Compare C Register</p> <p>The value in the active CMPC register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare C" event.</p> <p>Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWCMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> - If CMPCTL2[SHDWCMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADCMODE] bit field determines which event will load the active register from the shadow register: - If CMPCTL2[SHDWCMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.

12.4.2.35 CMPD Register (offset = 71h) [reset = 0h]

CMPD is shown in [Figure 12-113](#) and described in [Table 12-51](#).

Counter Compare D Register

Figure 12-113. CMPD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPD															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-51. CMPD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMPD	R/W	0h	<p>Compare D Register</p> <p>The value in the active CMPD register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare D" event.</p> <p>Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWDMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> - If CMPCTL2[SHDWDMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADMODE] bit field determines which event will load the active register from the shadow register: - If CMPCTL2[SHDWDMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.

12.4.2.36 GLDCTL2 Register (offset = 74h) [reset = 0h]

GLDCTL2 is shown in [Figure 12-114](#) and described in [Table 12-52](#).

Global PWM Load Control Register 2

Figure 12-114. GLDCTL2 Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED						GFRCLD	OSHTLD
R=0-0h						R=0/W=1-0h	R=0/W=1-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-52. GLDCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R=0	0h	Reserved
1	GFRCLD	R=0/W=1	0h	Force Load Event in One Shot Mode 0: Writing of 0 will be ignored. Always reads back a 0. 1: Force one load event at the input of the event pre-scale counter as shown in the diagram below. This bit is intended to be used for testing and/or software force loading of the events in global load mode.
0	OSHTLD	R=0/W=1	0h	Enable Reload Event in One Shot Mode 0: Writing of 0 will be ignored. Always reads back a 0. 1: Turns the one shot latch condition ON. Upon occurrence of a chosen load strobe, one shadow to active reload occurs and the latch will be cleared. Hence writing 1 to this bit would allow one load strobe event to pass through and block further strobe events.

12.4.2.37 TZSEL Register (offset = 80h) [reset = 0h]

TZSEL is shown in [Figure 12-115](#) and described in [Table 12-53](#).

Trip Zone Select Register

Figure 12-115. TZSEL Register

15	14	13	12	11	10	9	8
DCBEVT1	DCAEVT1	OSHT6	OSHT5	OSHT4	OSHT3	OSHT2	OSHT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-53. TZSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Select 0: Disable DCBEVT1 as one-shot-trip source for this ePWM module. 1: Enable DCBEVT1 as one-shot-trip source for this ePWM module.
14	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Select 0: Disable DCAEVT1 as one-shot-trip source for this ePWM module. 1: Enable DCAEVT1 as one-shot-trip source for this ePWM module.
13	OSHT6	R/W	0h	Trip-zone 6 (TZ6) Select 0: Disable TZ6 as a one-shot trip source for this ePWM module 1: Enable TZ6 as a one-shot trip source for this ePWM module
12	OSHT5	R/W	0h	Trip-zone 5 (TZ5) Select 0: Disable TZ5 as a one-shot trip source for this ePWM module 1: Enable TZ5 as a one-shot trip source for this ePWM module
11	OSHT4	R/W	0h	Trip-zone 4 (TZ4) Select 0: Disable TZ4 as a one-shot trip source for this ePWM module 1: Enable TZ4 as a one-shot trip source for this ePWM module
10	OSHT3	R/W	0h	Trip-zone 3 (TZ3) Select 0: Disable TZ3 as a one-shot trip source for this ePWM module 1: Enable TZ3 as a one-shot trip source for this ePWM module
9	OSHT2	R/W	0h	Trip-zone 2 (TZ2) Select 0: Disable TZ2 as a one-shot trip source for this ePWM module 1: Enable TZ2 as a one-shot trip source for this ePWM module
8	OSHT1	R/W	0h	Trip-zone 1 (TZ1) Select 0: Disable TZ1 as a one-shot trip source for this ePWM module 1: Enable TZ1 as a one-shot trip source for this ePWM module
7	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Select 0: Disable DCBEVT2 as a CBC trip source for this ePWM module 1: Enable DCBEVT2 as a CBC trip source for this ePWM module
6	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Select 0: Disable DCAEVT2 as a CBC trip source for this ePWM module 1: Enable DCAEVT2 as a CBC trip source for this ePWM module
5	CBC6	R/W	0h	Trip-zone 6 (TZ6) Select 0: Disable TZ6 as a CBC trip source for this ePWM module 1: Enable TZ6 as a CBC trip source for this ePWM module

Table 12-53. TZSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CBC5	R/W	0h	Trip-zone 5 (TZ5) Select 0: Disable TZ5 as a CBC trip source for this ePWM module 1: Enable TZ5 as a CBC trip source for this ePWM module
3	CBC4	R/W	0h	Trip-zone 4 (TZ4) Select 0: Disable TZ4 as a CBC trip source for this ePWM module 1: Enable TZ4 as a CBC trip source for this ePWM module
2	CBC3	R/W	0h	Trip-zone 3 (TZ3) Select 0: Disable TZ3 as a CBC trip source for this ePWM module 1: Enable TZ3 as a CBC trip source for this ePWM module
1	CBC2	R/W	0h	Trip-zone 2 (TZ2) Select 0: Disable TZ2 as a CBC trip source for this ePWM module 1: Enable TZ2 as a CBC trip source for this ePWM module
0	CBC1	R/W	0h	Trip-zone 1 (TZ1) Select 0: Disable TZ1 as a CBC trip source for this ePWM module 1: Enable TZ1 as a CBC trip source for this ePWM module

12.4.2.38 TZDCSEL Register (offset = 82h) [reset = 0h]

TZDCSEL is shown in [Figure 12-116](#) and described in [Table 12-54](#).

Trip Zone Digital Comparator Select Register

Figure 12-116. TZDCSEL Register

15	14	13	12	11	10	9	8
RESERVED				DCBEVT2		DCBEVT1	
R=0-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
DCBEVT1		DCAEVT2				DCAEVT1	
R/W-0h		R/W-0h				R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-54. TZDCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11-9	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Selection 000: Event disabled 001: DCAH = low, DCAL = don't care 010: DCAH = high, DCAL = don't care 011: DCAL = low, DCAH = don't care 100: DCAL = high, DCAH = don't care 101: DCAL = high, DCAH = low 110: Reserved 111: Reserved
8-6	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Selection 000: Event disabled 001: DCAH = low, DCAL = don't care 010: DCAH = high, DCAL = don't care 011: DCAL = low, DCAH = don't care 100: DCAL = high, DCAH = don't care 101: DCAL = high, DCAH = low 110: Reserved 111: Reserved
5-3	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Selection 000: Event disabled 001: DCAH = low, DCAL = don't care 010: DCAH = high, DCAL = don't care 011: DCAL = low, DCAH = don't care 100: DCAL = high, DCAH = don't care 101: DCAL = high, DCAH = low 110: Reserved 111: Reserved

Table 12-54. TZDCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Selection 000: Event disabled 001: DCAH = low, DCAL = don't care 010: DCAH = high, DCAL = don't care 011: DCAL = low, DCAH = don't care 100: DCAL = high, DCAH = don't care 101: DCAL = high, DCAH = low 110: Reserved 111: Reserved

12.4.2.39 TZCTL Register (offset = 84h) [reset = 0h]

TZCTL is shown in [Figure 12-117](#) and described in [Table 12-55](#).

Trip Zone Control Register

Figure 12-117. TZCTL Register

15	14	13	12	11	10	9	8
RESERVED			DCBEVT2			DCBEVT1	
R=0-0h			R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
DCAEVT2		DCAEVT1			TZB	TZA	
R/W-0h		R/W-0h			R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-55. TZCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11-10	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state. 10: Force EPWMxA to a low state. 11: Do Nothing, trip action is disabled
9-8	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state. 10: Force EPWMxA to a low state. 11: Do Nothing, trip action is disabled
7-6	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state. 10: Force EPWMxA to a low state. 11: Do Nothing, trip action is disabled
5-4	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state. 10: Force EPWMxA to a low state. 11: Do Nothing, trip action is disabled
3-2	TZB	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2Trip Action On EPWMxB When a trip event occurs the following action is taken on output EPWMxB. Which trip-zone pins can cause an event is defined in the TZSEL register. 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state 10: Force EPWMxA to a low state 11: Do nothing, no action is taken on EPWMxA.

Table 12-55. TZCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	TZA	R/W	0h	<p>TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA</p> <p>When a trip event occurs the following action is taken on output EPWMxA. Which trip-zone pins can cause an event is defined in the TZSEL register.</p> <p>00: High-impedance (EPWMxA = High-impedance state)</p> <p>01: Force EPWMxA to a high state</p> <p>10: Force EPWMxA to a low state</p> <p>11: Do nothing, no action is taken on EPWMxA.</p>

12.4.2.40 TZCTL2 Register (offset = 85h) [reset = 0h]

TZCTL2 is shown in [Figure 12-118](#) and described in [Table 12-56](#).

Additional Trip Zone Control Register

Figure 12-118. TZCTL2 Register

15	14	13	12	11	10	9	8
ETZE		RESERVED			TZBD		TZBU
R/W-0h		R=0-0h			R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
TZBU			TZAD			TZAU	
R/W-0h			R/W-0h			R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-56. TZCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ETZE	R/W	0h	TZCTL2 Enable 0: Use trip action from TZCTL (legacy EPWM compatibility) 1: Use trip action defined in TZCTL2, TZCTLDCB and TZCTLDCB. Settings in TZCTL are ignored
14-12	RESERVED	R=0	0h	Reserved
11-9	TZBD	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
8-6	TZBU	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
5-3	TZAD	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled

Table 12-56. TZCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	TZAU	R/W	0h	<p>TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is UP</p> <p>000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled</p>

12.4.2.41 TZCTLDC Register (offset = 86h) [reset = 0h]

TZCTLDC is shown in [Figure 12-119](#) and described in [Table 12-57](#).

Trip Zone Control Register Digital Compare A

Figure 12-119. TZCTLDC Register

15	14	13	12	11	10	9	8
RESERVED			DCAEVT2D			DCAEVT2U	
R=0-0h			R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
DCAEVT2U	DCAEVT1D			DCAEVT1U			
R/W-0h	R/W-0h			R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-57. TZCTLDC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11-9	DCAEVT2D	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
8-6	DCAEVT2U	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA while Count direction is UP 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
5-3	DCAEVT1D	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled

Table 12-57. TZCTLDC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	DCAEVT1U	R/W	0h	<p>Digital Compare Output A Event 1 Action On EPWMxA while Count direction is UP</p> <p>000: HiZ (EPWMxA = HiZ state)</p> <p>001: Forced Hi (EPWMxA = High state)</p> <p>010: Forced Lo (EPWMxA = Lo state)</p> <p>011: Toggle (Low -> High, High -> Low)</p> <p>100: Reserved</p> <p>101: Reserved</p> <p>110: Reserved</p> <p>111: Do Nothing, trip action is disabled</p>

12.4.2.42 TZCTLDCB Register (offset = 87h) [reset = 0h]

TZCTLDCB is shown in [Figure 12-120](#) and described in [Table 12-58](#).

Trip Zone Control Register Digital Compare B

Figure 12-120. TZCTLDCB Register

15	14	13	12	11	10	9	8
RESERVED			DCBEVT2D			DCBEVT2U	
R=0-0h			R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
DCBEVT2U		DCBEVT1D			DCBEVT1U		
R/W-0h		R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-58. TZCTLDCB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R=0	0h	Reserved
11-9	DCBEVT2D	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
8-6	DCBEVT2U	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
5-3	DCBEVT1D	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled

Table 12-58. TZCTLDCB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	DCBEVT1U	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled

12.4.2.43 TZEINT Register (offset = 8Dh) [reset = 0h]

TZEINT is shown in [Figure 12-121](#) and described in [Table 12-59](#).

Trip Zone Enable Interrupt Register

Figure 12-121. TZEINT Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED	DCBEVT2	DCBEVT1	DCAEV2	DCAEV1	OST	CBC	RESERVED
R=0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R=0-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-59. TZEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R=0	0h	Reserved
6	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Interrupt Enable 0: Disabled 1: Enabled
5	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Interrupt Enable 0: Disabled 1: Enabled
4	DCAEV2	R/W	0h	Digital Compare Output A Event 2 Interrupt Enable 0: Disabled 1: Enabled
3	DCAEV1	R/W	0h	Digital Compare Output A Event 1 Interrupt Enable 0: Disabled 1: Enabled
2	OST	R/W	0h	Trip-zone One-Shot Interrupt Enable 0: Disable one-shot interrupt generation 1: Enable Interrupt generation a one-shot trip event will cause a EPWMx_TZINT PIE interrupt.
1	CBC	R/W	0h	Trip-zone Cycle-by-Cycle Interrupt Enable 0: Disable cycle-by-cycle interrupt generation. 1: Enable interrupt generation a cycle-by-cycle trip event will cause an EPWMx_TZINT PIE interrupt.
0	RESERVED	R=0	0h	Reserved

12.4.2.44 TZFLG Register (offset = 93h) [reset = 0h]

TZFLG is shown in [Figure 12-122](#) and described in [Table 12-60](#).

Trip Zone Flag Register

Figure 12-122. TZFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	INT
R=0-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-60. TZFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R=0	0h	Reserved
6	DCBEVT2	R	0h	Latched Status Flag for Digital Compare Output B Event 2 0: Indicates no trip event has occurred on DCBEVT2 1: Indicates a trip event has occurred for the event defined for DCBEVT2
5	DCBEVT1	R	0h	Latched Status Flag for Digital Compare Output B Event 1 0: Indicates no trip event has occurred on DCBEVT1 1: Indicates a trip event has occurred for the event defined for DCBEVT1
4	DCAEVT2	R	0h	Latched Status Flag for Digital Compare Output A Event 2 0: Indicates no trip event has occurred on DCAEVT2 1: Indicates a trip event has occurred for the event defined for DCAEVT2
3	DCAEVT1	R	0h	Latched Status Flag for Digital Compare Output A Event 1 0: Indicates no trip event has occurred on DCAEVT1 1: Indicates a trip event has occurred for the event defined for DCAEVT1
2	OST	R	0h	Latched Status Flag for A One-Shot Trip Event 0: No one-shot trip event has occurred. 1: Indicates a trip event has occurred on a pin selected as a one-shot trip source. This bit is cleared by writing the appropriate value to the TZCLR register.
1	CBC	R	0h	Latched Status Flag for Cycle-By-Cycle Trip Event 0: No cycle-by-cycle trip event has occurred. 1: Indicates a trip event has occurred on a signal selected as a cycle-by-cycle trip source. The TZFLG[CBC] bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the signal is automatically cleared when the ePWM time-base counter reaches zero (TBCTR = 0x00) if the trip condition is no longer present. The condition on the signal is only cleared when the TBCTR = 0x00 no matter where in the cycle the CBC flag is cleared. This bit is cleared by writing the appropriate value to the TZCLR register.

Table 12-60. TZFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R	0h	Latched Trip Interrupt Status Flag 0: Indicates no interrupt has been generated. 1: Indicates an EPWMx_TZINT PIE interrupt was generated because of a trip condition. No further EPWMx_TZINT PIE interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by writing the appropriate value to the TZCLR register.

12.4.2.45 TZCBCFLG Register (offset = 94h) [reset = 0h]

TZCBCFLG is shown in [Figure 12-123](#) and described in [Table 12-61](#).

Trip Zone CBC Flag Register

Figure 12-123. TZCBCFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-61. TZCBCFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7	DCBEVT2	R	0h	Latched Status Flag for Digital Compare B Output Event 2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCBEVT2. 1: Reading a 1 indicates a trip has occurred on the DCBEVT2 selected event.
6	DCAEVT2	R	0h	Latched Status Flag for Digital Compare A Output Event 2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCAEVT2. 1: Reading a 1 indicates a trip has occurred on the DCAEVT2 selected event.
5	CBC6	R	0h	Latched Status Flag for CBC6 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC6. 1: Reading a 1 indicates a trip has occurred on the CBC6 selected event.
4	CBC5	R	0h	Latched Status Flag for CBC5 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC5. 1: Reading a 1 indicates a trip has occurred on the CBC5 selected event.
3	CBC4	R	0h	Latched Status Flag for CBC4 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC4. 1: Reading a 1 indicates a trip has occurred on the CBC4 selected event.
2	CBC3	R	0h	Latched Status Flag for CBC3 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC3. 1: Reading a 1 indicates a trip has occurred on the CBC3 selected event.
1	CBC2	R	0h	Latched Status Flag for CBC2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC2. 1: Reading a 1 indicates a trip has occurred on the CBC2 selected event.
0	CBC1	R	0h	Latched Status Flag for CBC1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC1. 1: Reading a 1 indicates a trip has occurred on the CBC1 selected event.

12.4.2.46 TZOSTFLG Register (offset = 95h) [reset = 0h]

TZOSTFLG is shown in [Figure 12-124](#) and described in [Table 12-62](#).

Trip Zone OST Flag Register

Figure 12-124. TZOSTFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	OST6	OST5	OST4	OST3	OST2	OST1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-62. TZOSTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7	DCBEVT2	R	0h	Latched Status Flag for Digital Compare B Output Event 1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCBEVT1. 1: Reading a 1 indicates a trip has occurred on the DCBEVT1 selected event.
6	DCAEVT2	R	0h	Latched Status Flag for Digital Compare A Output Event 1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCAEVT1. 1: Reading a 1 indicates a trip has occurred on the DCAEVT1 selected event.
5	OST6	R	0h	Latched Status Flag for OST6 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST6. 1: Reading a 1 indicates a trip has occurred on the OST6 selected event.
4	OST5	R	0h	Latched Status Flag for OST5 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST5. 1: Reading a 1 indicates a trip has occurred on the OST5 selected event.
3	OST4	R	0h	Latched Status Flag for OST4 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST4. 1: Reading a 1 indicates a trip has occurred on the OST4 selected event.
2	OST3	R	0h	Latched Status Flag for OST3 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST3. 1: Reading a 1 indicates a trip has occurred on the OST3 selected event.
1	OST2	R	0h	Latched Status Flag for OST2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST2. 1: Reading a 1 indicates a trip has occurred on the OST2 selected event.
0	OST1	R	0h	Latched Status Flag for OST1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST1. 1: Reading a 1 indicates a trip has occurred on the OST1 selected event.

12.4.2.47 TZCLR Register (offset = 97h) [reset = 0h]

TZCLR is shown in [Figure 12-125](#) and described in [Table 12-63](#).

Trip Zone Clear Register

Figure 12-125. TZCLR Register

15	14	13	12	11	10	9	8
CBCPULSE	RESERVED						
R/W-0h	R=0-0h						
7	6	5	4	3	2	1	0
RESERVED	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	INT
R=0-0h	R=0/W=1-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-63. TZCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	CBCPULSE	R/W	0h	Clear Pulse for Cycle-By-Cycle (CBC) Trip Latch This bit field determines which pulse clears the CBC trip latch. 00: CTR = zero pulse clears CBC trip latch. (Same as legacy designs.) 01: CTR = PRD pulse clears CBC trip latch. 10: CTR = zero or CTR = PRD pulse clears CBC trip latch. 11: Reserved (CBC trip latch is not cleared)
13-7	RESERVED	R=0	0h	Reserved
6	DCBEVT2	R=0/W=1	0h	Clear Flag for Digital Compare Output B Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCBEVT2 event trip condition.
5	DCBEVT1	R=0/W=1	0h	Clear Flag for Digital Compare Output B Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCBEVT1 event trip condition.
4	DCAEVT2	R=0/W=1	0h	Clear Flag for Digital Compare Output A Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCAEVT2 event trip condition.
3	DCAEVT1	R=0/W=1	0h	Clear Flag for Digital Compare Output A Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCAEVT1 event trip condition.
2	OST	R=0/W=1	0h	Clear Flag for One-Shot Trip (OST) Latch 0: Has no effect. Always reads back a 0. 1: Clears this Trip (set) condition.
1	CBC	R=0/W=1	0h	Clear Flag for Cycle-By-Cycle (CBC) Trip Latch 0: Has no effect. Always reads back a 0. 1: Clears this Trip (set) condition.
0	INT	R=0/W=1	0h	Global Interrupt Clear Flag 0: Has no effect. Always reads back a 0. 1: Clears the trip-interrupt flag for this ePWM module (TZFLG[INT]). NOTE: No further EPWMx_TZINT PIE interrupts will be generated until the flag is cleared. If the TZFLG[INT] bit is cleared and any of the other flag bits are set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts.

12.4.2.48 TZCBCCLR Register (offset = 98h) [reset = 0h]

TZCBCCLR is shown in [Figure 12-126](#) and described in [Table 12-64](#).

Trip Zone CBC Clear Register

Figure 12-126. TZCBCCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-64. TZCBCCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7	DCBEVT2	R=0/W=1	0h	Clear Flag for Digital Compare Output B Event 2 selected for CBC 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[DCBEVT2] bit.
6	DCAEVT2	R=0/W=1	0h	Clear Flag for Digital Compare Output A Event 2 selected for CBC 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[DCAEVT2] bit.
5	CBC6	R=0/W=1	0h	Clear Flag for Cycle-By-Cycle (CBC6) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC6] bit.
4	CBC5	R=0/W=1	0h	Clear Flag for Cycle-By-Cycle (CBC5) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC5] bit.
3	CBC4	R=0/W=1	0h	Clear Flag for Cycle-By-Cycle (CBC4) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC4] bit.
2	CBC3	R=0/W=1	0h	Clear Flag for Cycle-By-Cycle (CBC3) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC3] bit.
1	CBC2	R=0/W=1	0h	Clear Flag for Cycle-By-Cycle (CBC2) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC2] bit.
0	CBC1	R=0/W=1	0h	Clear Flag for Cycle-By-Cycle (CBC1) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC1] bit.

12.4.2.49 TZOSTCLR Register (offset = 99h) [reset = 0h]

TZOSTCLR is shown in [Figure 12-127](#) and described in [Table 12-65](#).

Trip Zone OST Clear Register

Figure 12-127. TZOSTCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	OST6	OST5	OST4	OST3	OST2	OST1
R=0/W=1-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-65. TZOSTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7	DCBEVT2	R=0/W=1	0h	Clear Flag for Digital Compare Output B Event 1 selected for OST 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[DCBEVT1] bit.
6	DCAEVT2	R=0/W=1	0h	Clear Flag for Digital Compare Output A Event 1 selected for OST 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[DCAEVT1] bit.
5	OST6	R=0/W=1	0h	Clear Flag for Oneshot (OST6) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST6] bit.
4	OST5	R=0/W=1	0h	Clear Flag for Oneshot (OST5) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST5] bit.
3	OST4	R=0/W=1	0h	Clear Flag for Oneshot (OST4) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST4] bit.
2	OST3	R=0/W=1	0h	Clear Flag for Oneshot (OST3) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST3] bit.
1	OST2	R=0/W=1	0h	Clear Flag for Oneshot (OST2) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST2] bit.
0	OST1	R=0/W=1	0h	Clear Flag for Oneshot (OST1) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST1] bit.

12.4.2.50 TZFRC Register (offset = 9Bh) [reset = 0h]

TZFRC is shown in [Figure 12-128](#) and described in [Table 12-66](#).

Trip Zone Force Register

Figure 12-128. TZFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	RESERVED
R=0-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0/W=1-0h	R=0-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-66. TZFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R=0	0h	Reserved
6	DCBEVT2	R=0/W=1	0h	Force Flag for Digital Compare Output B Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCBEVT2 event trip condition and sets the TZFLG[DCBEVT2] bit.
5	DCBEVT1	R=0/W=1	0h	Force Flag for Digital Compare Output B Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCBEVT1 event trip condition and sets the TZFLG[DCBEVT1] bit.
4	DCAEVT2	R=0/W=1	0h	Force Flag for Digital Compare Output A Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCAEVT2 event trip condition and sets the TZFLG[DCAEVT2] bit.
3	DCAEVT1	R=0/W=1	0h	Force Flag for Digital Compare Output A Event 1 0: Writing 0 has no effect. This bit always reads back 0 1: Writing 1 forces the DCAEVT1 event trip condition and sets the TZFLG[DCAEVT1] bit.
2	OST	R=0/W=1	0h	Force a One-Shot Trip Event via Software 0: Writing of 0 is ignored. Always reads back a 0. 1: Forces a one-shot trip event and sets the TZFLG[OST] bit.
1	CBC	R=0/W=1	0h	Force a Cycle-by-Cycle Trip Event via Software 0: Writing of 0 is ignored. Always reads back a 0. 1: Forces a cycle-by-cycle trip event and sets the TZFLG[CBC] bit.
0	RESERVED	R=0	0h	Reserved

12.4.2.51 ETSEL Register (offset = A4h) [reset = 0h]

ETSEL is shown in [Figure 12-129](#) and described in [Table 12-67](#).

Event Trigger Selection Register

Figure 12-129. ETSEL Register

15	14	13	12	11	10	9	8
SOCBEN	SOCBSEL			SOCAEN	SOCASEL		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	INTSELCMP	SOCBSELCMP	SOCASELCMP	INTEN	INTSEL		
R=0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-67. ETSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOCBEN	R/W	0h	Enable the ADC Start of Conversion B (EPWMxSOCB) Pulse 0: Disable EPWMxSOCB. 1: Enable EPWMxSOCB pulse.
14-12	SOCBSEL	R/W	0h	EPWMxSOCB Selection Options These bits determine when a EPWMxSOCB pulse will be generated. 000: Enable DCBEVT1.soc event 001: Enable event time-base counter equal to zero. (TBCTR = 0x00) 010: Enable event time-base counter equal to period (TBCTR = TBPRD) 011: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD). This mode is useful in up-down count mode. 100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110: Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111: Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by SOCSELCMP bit.
11	SOCAEN	R/W	0h	Enable the ADC Start of Conversion A (EPWMxSOCA) Pulse 0: Disable EPWMxSOCA. 1: Enable EPWMxSOCA pulse.

Table 12-67. ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	SOCASEL	R/W	0h	<p>EPWMxSOCA Selection Options</p> <p>These bits determine when a EPWMxSOCA pulse will be generated.</p> <p>000: Enable DCAEVT1.soc event</p> <p>001: Enable event time-base counter equal to zero. (TBCTR = 0x00)</p> <p>010: Enable event time-base counter equal to period (TBCTR = TBPRD)</p> <p>011: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD). This mode is useful in up-down count mode.</p> <p>100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing</p> <p>101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing</p> <p>110: Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing</p> <p>111: Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by SOCASELCMP bit.</p>
7	RESERVED	R=0	0h	Reserved
6	INTSELCMP	R/W	0h	<p>EPWMxINT Compare Register Selection Options</p> <p>0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to INTSEL selection mux.</p> <p>1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to INTSEL selection mux.</p>
5	SOCBSELCMP	R/W	0h	<p>EPWMxSOCB Compare Register Selection Options</p> <p>0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCSEL selection mux.</p> <p>1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCSEL selection mux.</p>
4	SOCASELCMP	R/W	0h	<p>EPWMxSOCA Compare Register Selection Options</p> <p>0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCSEL selection mux.</p> <p>1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCSEL selection mux.</p>

Table 12-67. ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INTEN	R/W	0h	Enable ePWM Interrupt (EPWMx_INT) Generation 0: Disable EPWMx_INT generation 1: Enable EPWMx_INT generation
2-0	INTSEL	R/W	0h	ePWM Interrupt (EPWMx_INT) Selection Options 000: Reserved 001: Enable event time-base counter equal to zero. (TBCTR = 0x00) 010: Enable event time-base counter equal to period (TBCTR = TBPRD) 011: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD). This mode is useful in up-down count mode. 100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110: Enable event time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111: Enable event time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by INTSELCMP bit.

12.4.2.52 ETPS Register (offset = A6h) [reset = 0h]

ETPS is shown in [Figure 12-130](#) and described in [Table 12-68](#).

Event Trigger Pre-Scale Register

Figure 12-130. ETPS Register

15	14	13	12	11	10	9	8
SOCBCNT		SOCBPRD		SOCACNT		SOCAPRD	
R-0h		R/W-0h		R-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		SOCPSSEL	INTPSSEL	INTCNT		INTPRD	
R=0-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-68. ETPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SOCBCNT	R	0h	ePWM ADC Start-of-Conversion B Event (EPWMxSOCB) Counter Register These bits indicate how many selected ETSEL[SOCBSEL] events have occurred: 00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred.
13-12	SOCBPRD	R/W	0h	ePWM ADC Start-of-Conversion B Event (EPWMxSOCB) Period Select These bits determine how many selected ETSEL[SOCBSEL] events need to occur before an EPWMxSOCB pulse is generated. To be generated, the pulse must be enabled (ETSEL[SOCBEN] = 1). The SOCB pulse will be generated even if the status flag is set from a previous start of conversion (ETFLG[SOCB] = 1). Once the SOCB pulse is generated, the ETPS[SOCBCNT] bits will automatically be cleared. 00: Disable the SOCB event counter. No EPWMxSOCB pulse will be generated 01: Generate the EPWMxSOCB pulse on the first event: ETPS[SOCBCNT] = 0,1 10: Generate the EPWMxSOCB pulse on the second event: ETPS[SOCBCNT] = 1,0 11: Generate the EPWMxSOCB pulse on the third event: ETPS[SOCBCNT] = 1,1
11-10	SOCACNT	R	0h	ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Counter Register These bits indicate how many selected ETSEL[SOCASEL] events have occurred: 00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred.

Table 12-68. ETPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	SOCAPRD	R/W	0h	<p>ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Period Select</p> <p>These bits determine how many selected ETSEL[SOCASEL] events need to occur before an EPWMxSOCA pulse is generated. To be generated, the pulse must be enabled (ETSEL[SOCAEN] = 1). The SOCA pulse will be generated even if the status flag is set from a previous start of conversion (ETFLG[SOCA] = 1). Once the SOCA pulse is generated, the ETPS[SOCACNT] bits will automatically be cleared.</p> <p>00: Disable the SOCA event counter. No EPWMxSOCA pulse will be generated</p> <p>01: Generate the EPWMxSOCA pulse on the first event: ETPS[SOCACNT] = 0,1</p> <p>10: Generate the EPWMxSOCA pulse on the second event: ETPS[SOCACNT] = 1,0</p> <p>11: Generate the EPWMxSOCA pulse on the third event: ETPS[SOCACNT] = 1,1</p>
7-6	RESERVED	R=0	0h	Reserved
5	SOCPSSEL	R/W	0h	<p>EPWMxSOC A/B Pre-Scale Selection Bits</p> <p>0: Selects ETPS [SOCACNT/SOCBCNT] and [SOCAPRD/SOCBPRD] registers to determine frequency of events (interrupt once every 0-3 events).</p> <p>1: Selects ETSOCP [SOCACNT2/SOCBCNT2] and [SOCAPRD2/SOCBPRD2] registers to determine frequency of events (interrupt once every 0-15 events).</p>
4	INTPSSEL	R/W	0h	<p>EPWMxINTn Pre-Scale Selection Bits</p> <p>0: Selects ETPS [INTCNT, and INTPRD] registers to determine frequency of events (interrupt once every 0-3 events).</p> <p>1: Selects ETINTPS [INTCNT2, and INTPRD2] registers to determine frequency of events (interrupt once every 0-15 events).</p>
3-2	INTCNT	R	0h	<p>ePWM Interrupt Event (EPWMx_INT) Counter Register</p> <p>These bits indicate how many selected ETSEL[INTSEL] events have occurred. These bits are automatically cleared when an interrupt pulse is generated. If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD].</p> <p>00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred.</p>

Table 12-68. ETPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	INTPRD	R/W	0h	<p>ePWM Interrupt (EPWMx_INT) Period Select</p> <p>These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated. To be generated, the interrupt must be enabled (ETSEL[INT] = 1). If the interrupt status flag is set from a previous interrupt (ETFLG[INT] = 1) then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared.</p> <p>Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear.</p> <p>Writing a INTPRD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented.</p> <p>00: Disable the interrupt event counter. No interrupt will be generated and ETFRC[INT] is ignored.</p> <p>01: Generate an interrupt on the first event INTCNT = 01 (first event)</p> <p>10: Generate interrupt on ETPS[INTCNT] = 1,0 (second event)</p> <p>11: Generate interrupt on ETPS[INTCNT] = 1,1 (third event)</p>

12.4.2.53 ETFLG Register (offset = A8h) [reset = 0h]

ETFLG is shown in [Figure 12-131](#) and described in [Table 12-69](#).

Event Trigger Flag Register

Figure 12-131. ETFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
RESERVED				SOCB	SOCA	RESERVED	INT
R=0-0h				R-0h	R-0h	R=0-0h	R-0h

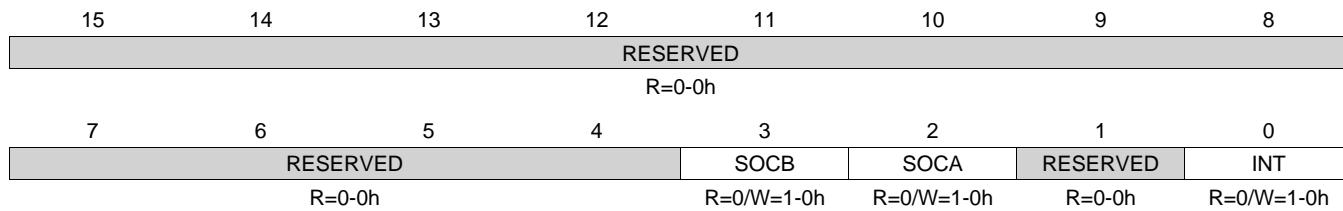
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-69. ETFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3	SOCB	R	0h	<p>Latched ePWM ADC Start-of-Conversion A (EPWMxSOCB) Status Flag</p> <p>Unlike the ETFLG[INT] flag, the EPWMxSOCB output will continue to pulse even if the flag bit is set.</p> <p>0: Indicates no event occurred</p> <p>1: Indicates that a start of conversion pulse was generated on EPWMxSOCB. The EPWMxSOCB output will continue to be generated even if the flag bit is set.</p>
2	SOCA	R	0h	<p>Latched ePWM ADC Start-of-Conversion A (EPWMxSOCA) Status Flag</p> <p>Unlike the ETFLG[INT] flag, the EPWMxSOCA output will continue to pulse even if the flag bit is set.</p> <p>0: Indicates no event occurred</p> <p>1: Indicates that a start of conversion pulse was generated on EPWMxSOCA. The EPWMxSOCA output will continue to be generated even if the flag bit is set.</p>
1	RESERVED	R=0	0h	Reserved
0	INT	R	0h	<p>Latched ePWM Interrupt (EPWMx_INT) Status Flag</p> <p>0: Indicates no event occurred</p> <p>1: Indicates that an ePWMx interrupt (EPWMx_INT) was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the ETFLG[INT] bit is still set. If an interrupt is pending, it will not be generated until after the ETFLG[INT] bit is cleared.</p>

12.4.2.54 ETCLR Register (offset = AAh) [reset = 0h]ETCLR is shown in [Figure 12-132](#) and described in [Table 12-70](#).

Event Trigger Clear Register

Figure 12-132. ETCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

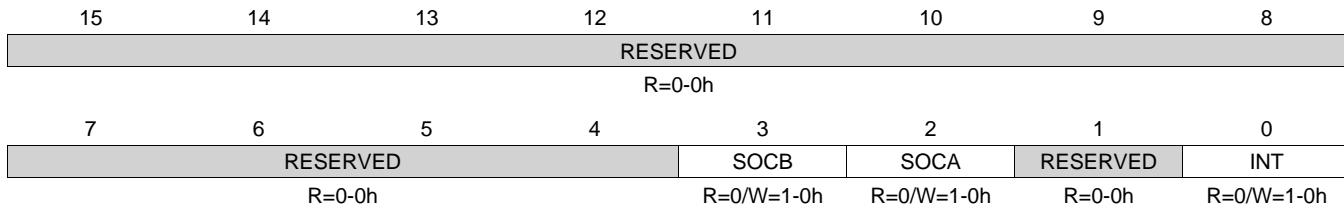
Table 12-70. ETCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3	SOCB	R=0/W=1	0h	ePWM ADC Start-of-Conversion A (EPWMxSOCB) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[SOCB] flag bit
2	SOCA	R=0/W=1	0h	ePWM ADC Start-of-Conversion A (EPWMxSOCA) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[SOCA] flag bit
1	RESERVED	R=0	0h	Reserved
0	INT	R=0/W=1	0h	ePWM Interrupt (EPWMx_INT) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[INT] flag bit and enable further interrupts pulses to be generated

12.4.2.55 ETFRC Register (offset = ACh) [reset = 0h]

ETFRC is shown in [Figure 12-133](#) and described in [Table 12-71](#).

Event Trigger Force Register

Figure 12-133. ETFRC Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

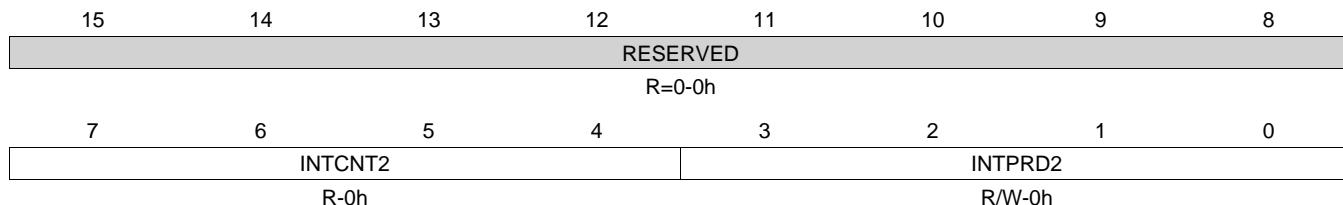
Table 12-71. ETFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R=0	0h	Reserved
3	SOCB	R=0/W=1	0h	<p>SOCB Force Bit</p> <p>The SOCB pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCB] flag bit will be set regardless.</p> <p>0: Writing 0 to this bit will be ignored. Always reads back a 0.</p> <p>1: Generates a pulse on EPWMxSOCB and set the SOCBFLG bit. This bit is used for test purposes.</p>
2	SOCA	R=0/W=1	0h	<p>SOCA Force Bit</p> <p>The SOCA pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCA] flag bit will be set regardless.</p> <p>0: Writing 0 to this bit will be ignored. Always reads back a 0.</p> <p>1: Generates a pulse on EPWMxSOCA and set the SOCAFGL bit. This bit is used for test purposes.</p>
1	RESERVED	R=0	0h	Reserved
0	INT	R=0/W=1	0h	<p>INT Force Bit</p> <p>The interrupt will only be generated if the event is enabled in the ETSEL register. The INT flag bit will be set regardless.</p> <p>0: Writing 0 to this bit will be ignored. Always reads back a 0.</p> <p>1: Generates an interrupt on EPWMxINT and set the INT flag bit. This bit is used for test purposes.</p>

12.4.2.56 ETINTPS Register (offset = AEh) [reset = 0h]

ETINTPS is shown in [Figure 12-134](#) and described in [Table 12-72](#).

Event-Trigger Interrupt Pre-Scale Register

Figure 12-134. ETINTPS Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; $-n$ = value after reset

Table 12-72. ETINTPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R=0	0h	Reserved
7-4	INTCNT2	R	0h	<p>EPWMxINT Counter 2</p> <p>When ETPS[INTPSSEL]=1, these bits indicate how many selected events have occurred:</p> <ul style="list-style-type: none"> 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events
3-0	INTPRD2	R/W	0h	<p>EPWMxINT Period 2 Select</p> <p>When ETPS[INTPSSEL] = 1, these bits select how many selected events need to occur before an interrupt is generated:</p> <ul style="list-style-type: none"> 0000: Disable counter 0001: Generate interrupt on INTCNT = 1 (first event) 0010: Generate interrupt on INTCNT = 2 (second event) 0011: Generate interrupt on INTCNT = 3 (third event) 0100: Generate interrupt on INTCNT = 4 (fourth event) ... 1111: Generate interrupt on INTCNT = 15 (fifteenth event)

12.4.2.57 ETSOCPS Register (offset = B0h) [reset = 0h]

ETSOCPS is shown in [Figure 12-135](#) and described in [Table 12-73](#).

Event-Trigger SOC Pre-Scale Register

Figure 12-135. ETSOCPS Register

15	14	13	12	11	10	9	8
SOCBCNT2				SOCBPRD2			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
SOCACNT2				SOCAPRD2			
R-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-73. ETSOCPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	SOCBCNT2	R	0h	EPWMxSOCB Counter 2 When ETPS[SOCPSEL] = 1, these bits indicate how many selected events have occurred: 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events
11-8	SOCBPRD2	R/W	0h	EPWMxSOCB Period 2 Select When ETPS[SOCPSEL] = 1, these bits select how many selected event need to occur before an SOCB pulse is generated: 0000: Disable counter 0001: Generate interrupt on SOCBCNT2 = 1 (first event) 0010: Generate interrupt on SOCBCNT2 = 2 (second event) 0011: Generate interrupt on SOCBCNT2 = 3 (third event) 0100: Generate interrupt on SOCBCNT2 = 4 (fourth event) ... 1111: Generate interrupt on SOCBCNT2 = 15 (fifteenth event)
7-4	SOCACNT2	R	0h	EPWMxSOCA Counter 2 When ETPS[SOCPSEL] = 1, these bits indicate how many selected events have occurred: 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events

Table 12-73. ETSOCPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	SOCAPRD2	R/W	0h	EPWMxSOCA Period 2 Select When ETPS[SOCPSEL] = 1, these bits select how many selected event need to occur before an SOCA pulse is generated: 0000: Disable counter 0001: Generate interrupt on SOCACNT2 = 1 (first event) 0010: Generate interrupt on SOCACNT2 = 2 (second event) 0011: Generate interrupt on SOCACNT2 = 3 (third event) 0100: Generate interrupt on SOCACNT2 = 4 (fourth event) ... 1111: Generate interrupt on SOCACNT2 = 15 (fifteenth event)

12.4.2.58 ETCNTINITCTL Register (offset = B2h) [reset = 0h]

ETCNTINITCTL is shown in [Figure 12-136](#) and described in [Table 12-74](#).

Event-Trigger Counter Initialization Control Register

Figure 12-136. ETCNTINITCTL Register

15	14	13	12	11	10	9	8
SOCBINITEN	SOCAINITEN	INTINITEN	SOCBINITFRC	SOCAINITFRC	INTINITFRC	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R=0-0h	
7	6	5	4	3	2	1	0
RESERVED							
R=0-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-74. ETCNTINITCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOCBINITEN	R/W	0h	EPWMxSOCB Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxSOCB counter with contents of ETCNTINIT[SOCBINIT] on a SYNC event or software force.
14	SOCAINITEN	R/W	0h	EPWMxSOCA Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxSOCA counter with contents of ETCNTINIT[SOCAINIT] on a SYNC event or software force.
13	INTINITEN	R/W	0h	EPWMxINT Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxINT counter 2 with contents of ETCNTINIT[INTINIT] on a SYNC event or software force.
12	SOCBINITFRC	R/W	0h	EPWMxSOCB Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxSOCB counter to be initialized with the contents of ETCNTINIT[SOCBINIT].
11	SOCAINITFRC	R/W	0h	EPWMxSOCA Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxSOCA counter to be initialized with the contents of ETCNTINIT[SOCAINIT].
10	INTINITFRC	R/W	0h	EPWMxINT Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxINT counter to be initialized with the contents of ETCNTINIT[INTINIT].
9-0	RESERVED	R=0	0h	Reserved

12.4.2.59 ETCNTINIT Register (offset = B4h) [reset = 0h]ETCNTINIT is shown in [Figure 12-137](#) and described in [Table 12-75](#).

Event-Trigger Counter Initialization Register

Figure 12-137. ETCNTINIT Register

15	14	13	12	11	10	9	8
RESERVED				SOCBINIT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
SOCAINIT				INTINIT			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-75. ETCNTINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-8	SOCBINIT	R/W	0h	EPWMxSOCB Counter 2 Initialization Bits The ET EPWMxSOCB counter is initialized with the contents of this register on an ePWM SYNC event or a software force.
7-4	SOCAINIT	R/W	0h	EPWMxSOCA Counter 2 Initialization Bits The ET EPWMxSOCA counter is initialized with the contents of this register on an ePWM SYNC event or a software force.
3-0	INTINIT	R/W	0h	EPWMxINT Counter 2 Initialization Bits The ET EPWMxINT counter is initialized with the contents of this register on an ePWM SYNC event or a software force.

12.4.2.60 DCTRIPSEL Register (offset = C0h) [reset = 0h]

DCTRIPSEL is shown in [Figure 12-138](#) and described in [Table 12-76](#).

Digital Compare Trip Select Register

Figure 12-138. DCTRIPSEL Register

15	14	13	12	11	10	9	8
DCBLCOMPSEL				DCBHCOMPSEL			
R/W-0h				R/W-0h			
DCALCOMPSEL				DCAHCOMPSEL			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-76. DCTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DCBLCOMPSEL	R/W	0h	Digital Compare B Low Input Select Bits 0000: TRIPIN1 and (TZ1 input) 0001: TRIPIN2 and (TZ2 input) 0010: TRIPIN3 and (TZ3 input) 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCBLTRIPSEL register ORed together)
11-8	DCBHCOMPSEL	R/W	0h	Digital Compare B High Input Select Bits 0000: TRIPIN1 and (TZ1 input) 0001: TRIPIN2 and (TZ2 input) 0010: TRIPIN3 and (TZ3 input) 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCBHTRIPSEL register ORed together)
7-4	DCALCOMPSEL	R/W	0h	Digital Compare A Low Input Select Bits 0000: TRIPIN1 and (TZ1 input) 0001: TRIPIN2 and (TZ2 input) 0010: TRIPIN3 and (TZ3 input) 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCALTRIPSEL register ORed together)

Table 12-76. DCTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DCAHCOMPSEL	R/W	0h	Digital Compare A High Input Select Bits 0000: TRIPIN1 and (TZ1 input) 0001: TRIPIN2 and (TZ2 input) 0010: TRIPIN3 and (TZ3 input) 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCAHTRIPSEL register ORed together)

12.4.2.61 DCACTL Register (offset = C3h) [reset = 0h]

DCACTL is shown in [Figure 12-139](#) and described in [Table 12-77](#).

Digital Compare A Control Register

Figure 12-139. DCACTL Register

15	14	13	12	11	10	9	8
RESERVED						EVT2FRCSYN CSEL	EVT2SRCSEL
R=0-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED						EVT1SYNCE	EVT1SOCE
R=0-0h						R/W-0h	R/W-0h
R=0-0h						R/W-0h	R/W-0h
R=0-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-77. DCACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R=0	0h	Reserved
9	EVT2FRCSYNCSEL	R/W	0h	DCAEV2 Force Synchronization Signal Select 0: Source Is Synchronous Signal 1: Source Is Asynchronous Signal
8	EVT2SRCSEL	R/W	0h	DCAEV2 Source Signal Select 0: Source Is DCAEV2 Signal 1: Source Is DCEVTFILT Signal
7-4	RESERVED	R=0	0h	Reserved
3	EVT1SYNCE	R/W	0h	DCAEV1 SYNC, Enable/Disable 0: SYNC Generation Disabled 1: SYNC Generation Enabled
2	EVT1SOCE	R/W	0h	DCAEV1 SOC, Enable/Disable 0: SOC Generation Disabled 1: SOC Generation Enabled
1	EVT1FRCSYNCSEL	R/W	0h	DCAEV1 Force Synchronization Signal Select 0: Source Is Synchronous Signal 1: Source Is Asynchronous Signal
0	EVT1SRCSEL	R/W	0h	DCAEV1 Source Signal Select 0: Source Is DCAEV1 Signal 1: Source Is DCEVTFILT Signal

12.4.2.62 DCBCTL Register (offset = C4h) [reset = 0h]

DCBCTL is shown in [Figure 12-140](#) and described in [Table 12-78](#).

Digital Compare B Control Register

Figure 12-140. DCBCTL Register

15	14	13	12	11	10	9	8
RESERVED						EVT2FRCSYN CSEL	EVT2SRCSEL
R=0-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				EVT1SYNCE	EVT1SOCE	EVT1FRCSYN CSEL	EVT1SRCSEL
R=0-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-78. DCBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R=0	0h	Reserved
9	EVT2FRCSYNCSEL	R/W	0h	DCBEVT2 Force Synchronization Signal Select 0: Source Is Synchronous Signal 1: Source Is Asynchronous Signal
8	EVT2SRCSEL	R/W	0h	DCBEVT2 Source Signal Select 0: Source Is DCBEVT2 Signal 1: Source Is DCEVTFILT Signal
7-4	RESERVED	R=0	0h	Reserved
3	EVT1SYNCE	R/W	0h	DCBEVT1 SYNC, Enable/Disable 0: SYNC Generation Disabled 1: SYNC Generation Enabled
2	EVT1SOCE	R/W	0h	DCBEVT1 SOC, Enable/Disable 0: SOC Generation Disabled 1: SOC Generation Enabled
1	EVT1FRCSYNCSEL	R/W	0h	DCBEVT1 Force Synchronization Signal Select 0: Source Is Synchronous Signal 1: Source Is Asynchronous Signal
0	EVT1SRCSEL	R/W	0h	DCBEVT1 Source Signal Select 0: Source Is DCBEVT1 Signal 1: Source Is DCEVTFILT Signal

12.4.2.63 DCFCTL Register (offset = C7h) [reset = 0h]

DCFCTL is shown in [Figure 12-141](#) and described in [Table 12-79](#).

Digital Compare Filter Control Register

Figure 12-141. DCFCTL Register

15	14	13	12	11	10	9	8
RESERVED			RESERVED			RESERVED	
R-0h			R-0h			R-0h	
7	6	5	4	3	2	1	0
RESERVED	RESERVED	PULSESEL		BLANKINV	BLANKE	SRCSEL	
R=0h	R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-79. DCFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-10	RESERVED	R	0h	Reserved
9-8	RESERVED	R	0h	Reserved
7	RESERVED	R=0	0h	Reserved
6	RESERVED	R	0h	Reserved
5-4	PULSESEL	R/W	0h	Pulse Select For Blanking & Capture Alignment 00: Time-base counter equal to period (TBCTR = TBPRD) 01: Time-base counter equal to zero (TBCTR = 0x00) 10: Reserved 11: Reserved
3	BLANKINV	R/W	0h	Blanking Window Inversion 0: Blanking window not inverted 1: Blanking window inverted
2	BLANKE	R/W	0h	Blanking Window Enable/Disable 0: Blanking window is disabled 1: Blanking window is enabled
1-0	SRCSEL	R/W	0h	Filter Block Signal Source Select 00: Source Is DCAEVT1 Signal 01: Source Is DCAEVT2 Signal 10: Source Is DCBEVT1 Signal 11: Source Is DCBEVT2 Signal

12.4.2.64 DCCAPCTL Register (offset = C8h) [reset = 0h]

DCCAPCTL is shown in [Figure 12-142](#) and described in [Table 12-80](#).

Digital Compare Capture Control Register

Figure 12-142. DCCAPCTL Register

15	14	13	12	11	10	9	8
CAPMODERES ERVED	CAPCLRRESE RVED	CAPSTSRESE RVED			RESERVED		
R/W-0hR-0h	R=0/W=1-0hR- 0h	R-0hR-0h			R=0-0h		
7	6	5	4	3	2	1	0
		RESERVED			SHDWMODE	CAPE	
		R=0-0h			R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-80. DCCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CAPMODE	R/W	0h	Counter Capture Mode 0: DCCAP function is controlled by PULSESEL bit in the DCFCTL register (compatible with previous EPWM versions) 1: Type-4 addition, DCCAP function is controlled by software
14	CAPCLR	R=0/W=1	0h	DC Capture Latched Status Clear Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear this CAPSTS (set) condition.
13	CAPSTS	R	0h	Latched Status Flag for Capture Event 0: No DC capture event occurred. 1: A DC capture event has occurred.
12-2	RESERVED	R=0	0h	Reserved
1	SHDWMODE	R/W	0h	TBCTR Counter Capture Shadow Select Mode 0: Enable shadow mode. The DCCAP active register is copied to shadow register on a TBCTR = TBPRD or TBCTR = zero event as defined by the DCFCTL[PULSESEL] bit. CPU reads of the DCCAP register will return the shadow register contents. 1: Active Mode. In this mode the shadow register is disabled. CPU reads from the DCCAP register will always return the active register contents.
0	CAPE	R/W	0h	TBCTR Counter Capture Enable/Disable 0: Disable the time-base counter capture. 1: Enable the time-base counter capture.

12.4.2.65 DCFOFFSET Register (offset = C9h) [reset = 0h]

DCFOFFSET is shown in [Figure 12-143](#) and described in [Table 12-81](#).

Digital Compare Filter Offset Register

Figure 12-143. DCFOFFSET Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCOFFSET															
R/W-0h															

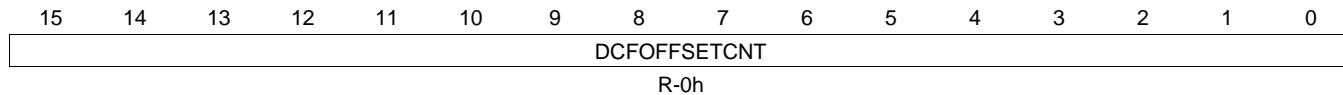
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-81. DCFOFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCOFFSET	R/W	0h	<p>Blanking Window Offset</p> <p>These 16-bits specify the number of TBCLK cycles from the blanking window reference to the point when the blanking window is applied. The blanking window reference is either period or zero as defined by the DCFCTL[PULSESEL] bit. This offset register is shadowed and the active register is loaded at the reference point defined by DCFCTL[PULSESEL]. The offset counter is also initialized and begins to count down when the active register is loaded. When the counter expires, the blanking window is applied. If the blanking window is currently active, then the blanking window counter is restarted.</p>

12.4.2.66 DCFOFFSETCNT Register (offset = CAh) [reset = 0h]DCFOFFSETCNT is shown in [Figure 12-144](#) and described in [Table 12-82](#).

Digital Compare Filter Offset Counter Register

Figure 12-144. DCFOFFSETCNT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-82. DCFOFFSETCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCFOFFSETCNT	R	0h	<p>Blanking Offset Counter</p> <p>These 16-bits are read only and indicate the current value of the offset counter. The counter counts down to zero and then stops until it is re-loaded on the next period or zero event as defined by the DCFCTL[PULSESEL] bit. The offset counter is not affected by the free/soft emulation bits. That is, it will always continue to count down if the device is halted by a emulation stop.</p>

12.4.2.67 DCFWINDOW Register (offset = CBh) [reset = 0h]

DCFWINDOW is shown in [Figure 12-145](#) and described in [Table 12-83](#).

Digital Compare Filter Window Register

Figure 12-145. DCFWINDOW Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCFWINDOW															
R/W-0h															

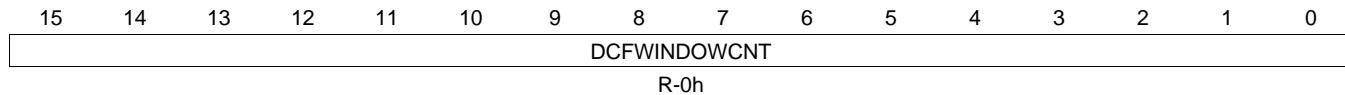
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-83. DCFWINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCFWINDOW	R/W	0h	<p>Blanking Window Width</p> <p>00h: No blanking window is generated.</p> <p>01-FFh: Specifies the width of the blanking window in TBCLK cycles. The blanking window begins when the offset counter expires. When this occurs, the window counter is loaded and begins to count down. If the blanking window is currently active and the offset counter expires, the blanking window counter is restarted. The blanking window can cross a PWM period boundary.</p>

12.4.2.68 DCFWINDOWCNT Register (offset = CCh) [reset = 0h]DCFWINDOWCNT is shown in [Figure 12-146](#) and described in [Table 12-84](#).

Digital Compare Filter Window Counter Register

Figure 12-146. DCFWINDOWCNT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

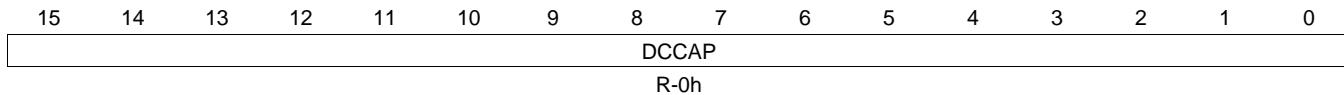
Table 12-84. DCFWINDOWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCFWINDOWCNT	R	0h	<p>Blanking Window Counter</p> <p>These 8 bits are read only and indicate the current value of the window counter. The counter counts down to zero and then stops until it is re-loaded when the offset counter reaches zero again.</p>

12.4.2.69 DCCAP Register (offset = CFh) [reset = 0h]

DCCAP is shown in [Figure 12-147](#) and described in [Table 12-85](#).

Digital Compare Counter Capture Register

Figure 12-147. DCCAP Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-85. DCCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCCAP	R	0h	<p>Digital Compare Time-Base Counter Capture</p> <p>To enable time-base counter capture, set the DCCAPCLT[CAPE] bit to 1. If enabled, reflects the value of the time-base counter (TBCTR) on the low to high edge transition of a filtered (DCEVTFLT) event. Further capture events are ignored until the next period or zero as selected by the DCFCTL[PULSESEL] bit. Shadowing of DCCAP is enabled and disabled by the DCCAPCTL[SHDWMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> - If DCCAPCTL[SHDWMODE] = 0, then the shadow is enabled. In this mode, the active register is copied to the shadow register on the TBCTR = TBPRD or TBCTR = zero as defined by the DCFCTL[PULSESEL] bit. CPU reads of this register will return the shadow register value. - If DCCAPCTL[SHDWMODE] = 1, then the shadow register is disabled. In this mode, CPU reads will return the active register value. The active and shadow registers share the same memory map address.

12.4.2.70 DCAHTRIPSEL Register (offset = D2h) [reset = 0h]DCAHTRIPSEL is shown in [Figure 12-148](#) and described in [Table 12-86](#).

Digital Compare AH Trip Select

Figure 12-148. DCAHTRIPSEL Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-86. DCAHTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAH mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAH mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAH mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAH mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAH mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAH mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAH mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAH mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAH mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAH mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAH mux

Table 12-86. DCAHTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAH mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAH mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAH mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAH mux

12.4.2.71 DCALTRIPSEL Register (offset = D3h) [reset = 0h]DCALTRIPSEL is shown in [Figure 12-149](#) and described in [Table 12-87](#).

Digital Compare AL Trip Select

Figure 12-149. DCALTRIPSEL Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-87. DCALTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAL mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAL mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAL mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAL mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAL mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAL mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAL mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAL mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAL mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAL mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAL mux

Table 12-87. DCALTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAL mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAL mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAL mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAL mux

12.4.2.72 DCBHTRIPSEL Register (offset = D4h) [reset = 0h]DCBHTRIPSEL is shown in [Figure 12-150](#) and described in [Table 12-88](#).

Digital Compare BH Trip Select

Figure 12-150. DCBHTRIPSEL Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-88. DCBHTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCBH mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCBH mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCBH mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCBH mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCBH mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCBH mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCBH mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCBH mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCBH mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCBH mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCBH mux

Table 12-88. DCBHTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCBH mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCBH mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCBH mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCBH mux

12.4.2.73 DCBLTRIPSEL Register (offset = D5h) [reset = 0h]DCBLTRIPSEL is shown in [Figure 12-151](#) and described in [Table 12-89](#).

Digital Compare BL Trip Select

Figure 12-151. DCBLTRIPSEL Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-89. DCBLTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAL mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAL mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAL mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAL mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAL mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAL mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAL mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAL mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAL mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAL mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAL mux

Table 12-89. DCBLTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAL mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAL mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAL mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAL mux

12.4.3 EPWM_XBAR_REGS Registers

Table 12-90 lists the memory-mapped registers for the EPWM_XBAR_REGS. All register offset addresses not listed in **Table 12-90** should be considered as reserved locations and the register contents should not be modified.

Table 12-90. EPWM_XBAR_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	TRIP4MUX0TO15CFG	ePWM XBAR Mux Configuration for TRIP4	Section 12.4.3.1	EALLOW
2h	TRIP4MUX16TO31CFG	ePWM XBAR Mux Configuration for TRIP4	Section 12.4.3.2	EALLOW
4h	TRIP5MUX0TO15CFG	ePWM XBAR Mux Configuration for TRIP5	Section 12.4.3.3	EALLOW
6h	TRIP5MUX16TO31CFG	ePWM XBAR Mux Configuration for TRIP5	Section 12.4.3.4	EALLOW
8h	TRIP7MUX0TO15CFG	ePWM XBAR Mux Configuration for TRIP7	Section 12.4.3.5	EALLOW
Ah	TRIP7MUX16TO31CFG	ePWM XBAR Mux Configuration for TRIP7	Section 12.4.3.6	EALLOW
Ch	TRIP8MUX0TO15CFG	ePWM XBAR Mux Configuration for TRIP8	Section 12.4.3.7	EALLOW
Eh	TRIP8MUX16TO31CFG	ePWM XBAR Mux Configuration for TRIP8	Section 12.4.3.8	EALLOW
10h	TRIP9MUX0TO15CFG	ePWM XBAR Mux Configuration for TRIP9	Section 12.4.3.9	EALLOW
12h	TRIP9MUX16TO31CFG	ePWM XBAR Mux Configuration for TRIP9	Section 12.4.3.10	EALLOW
14h	TRIP10MUX0TO15CFG	ePWM XBAR Mux Configuration for TRIP10	Section 12.4.3.11	EALLOW
16h	TRIP10MUX16TO31CFG	ePWM XBAR Mux Configuration for TRIP10	Section 12.4.3.12	EALLOW
18h	TRIP11MUX0TO15CFG	ePWM XBAR Mux Configuration for TRIP11	Section 12.4.3.13	EALLOW
1Ah	TRIP11MUX16TO31CFG	ePWM XBAR Mux Configuration for TRIP11	Section 12.4.3.14	EALLOW
1Ch	TRIP12MUX0TO15CFG	ePWM XBAR Mux Configuration for TRIP12	Section 12.4.3.15	EALLOW
1Eh	TRIP12MUX16TO31CFG	ePWM XBAR Mux Configuration for TRIP12	Section 12.4.3.16	EALLOW
20h	TRIP4MUXENABLE	ePWM XBAR Mux Enable for TRIP4	Section 12.4.3.17	EALLOW
22h	TRIP5MUXENABLE	ePWM XBAR Mux Enable for TRIP5	Section 12.4.3.18	EALLOW
24h	TRIP7MUXENABLE	ePWM XBAR Mux Enable for TRIP7	Section 12.4.3.19	EALLOW
26h	TRIP8MUXENABLE	ePWM XBAR Mux Enable for TRIP8	Section 12.4.3.20	EALLOW
28h	TRIP9MUXENABLE	ePWM XBAR Mux Enable for TRIP9	Section 12.4.3.21	EALLOW
2Ah	TRIP10MUXENABLE	ePWM XBAR Mux Enable for TRIP10	Section 12.4.3.22	EALLOW
2Ch	TRIP11MUXENABLE	ePWM XBAR Mux Enable for TRIP11	Section 12.4.3.23	EALLOW
2Eh	TRIP12MUXENABLE	ePWM XBAR Mux Enable for TRIP12	Section 12.4.3.24	EALLOW
38h	TRIPOUTINV	ePWM XBAR Output Inversion Register	Section 12.4.3.25	EALLOW
3Eh	TRIPLOCK	ePWM XBAR Configuration Lock register	Section 12.4.3.26	EALLOW

12.4.3.1 TRIP4MUX0TO15CFG Register (offset = 0h) [reset = 0h]

TRIP4MUX0TO15CFG is shown in [Figure 12-152](#) and described in [Table 12-91](#).

ePWM XBAR Mux Configuration for TRIP4

Figure 12-152. TRIP4MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-91. TRIP4MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-91. TRIP4MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-91. TRIP4MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.2 TRIP4MUX16TO31CFG Register (offset = 2h) [reset = 0h]

TRIP4MUX16TO31CFG is shown in [Figure 12-153](#) and described in [Table 12-92](#).

ePWM XBAR Mux Configuration for TRIP4

Figure 12-153. TRIP4MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-92. TRIP4MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-92. TRIP4MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-92. TRIP4MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for TRIP4 of EPWM-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.3 TRIP5MUX0TO15CFG Register (offset = 4h) [reset = 0h]

TRIP5MUX0TO15CFG is shown in [Figure 12-154](#) and described in [Table 12-93](#).

ePWM XBAR Mux Configuration for TRIP5

Figure 12-154. TRIP5MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-93. TRIP5MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-93. TRIP5MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-93. TRIP5MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.4 TRIP5MUX16TO31CFG Register (offset = 6h) [reset = 0h]

TRIP5MUX16TO31CFG is shown in [Figure 12-155](#) and described in [Table 12-94](#).

ePWM XBAR Mux Configuration for TRIP5

Figure 12-155. TRIP5MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-94. TRIP5MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-94. TRIP5MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-94. TRIP5MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for TRIP5 of EPWM-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.5 TRIP7MUX0TO15CFG Register (offset = 8h) [reset = 0h]

TRIP7MUX0TO15CFG is shown in [Figure 12-156](#) and described in [Table 12-95](#).

ePWM XBAR Mux Configuration for TRIP7

Figure 12-156. TRIP7MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-95. TRIP7MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-95. TRIP7MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-95. TRIP7MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.6 TRIP7MUX16TO31CFG Register (offset = Ah) [reset = 0h]

TRIP7MUX16TO31CFG is shown in [Figure 12-157](#) and described in [Table 12-96](#).

ePWM XBAR Mux Configuration for TRIP7

Figure 12-157. TRIP7MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-96. TRIP7MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-96. TRIP7MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-96. TRIP7MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for TRIP7 of EPWM-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.7 TRIP8MUX0TO15CFG Register (offset = Ch) [reset = 0h]

TRIP8MUX0TO15CFG is shown in [Figure 12-158](#) and described in [Table 12-97](#).

ePWM XBAR Mux Configuration for TRIP8

Figure 12-158. TRIP8MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-97. TRIP8MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-97. TRIP8MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-97. TRIP8MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.8 TRIP8MUX16TO31CFG Register (offset = Eh) [reset = 0h]

TRIP8MUX16TO31CFG is shown in [Figure 12-159](#) and described in [Table 12-98](#).

ePWM XBAR Mux Configuration for TRIP8

Figure 12-159. TRIP8MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-98. TRIP8MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-98. TRIP8MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-98. TRIP8MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for TRIP8 of EPWM-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.9 TRIP9MUX0TO15CFG Register (offset = 10h) [reset = 0h]

TRIP9MUX0TO15CFG is shown in [Figure 12-160](#) and described in [Table 12-99](#).

ePWM XBAR Mux Configuration for TRIP9

Figure 12-160. TRIP9MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-99. TRIP9MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-99. TRIP9MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-99. TRIP9MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.10 TRIP9MUX16TO31CFG Register (offset = 12h) [reset = 0h]

TRIP9MUX16TO31CFG is shown in [Figure 12-161](#) and described in [Table 12-100](#).

ePWM XBAR Mux Configuration for TRIP9

Figure 12-161. TRIP9MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-100. TRIP9MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-100. TRIP9MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-100. TRIP9MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for TRIP9 of EPWM-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.11 TRIP10MUX0TO15CFG Register (offset = 14h) [reset = 0h]

TRIP10MUX0TO15CFG is shown in [Figure 12-162](#) and described in [Table 12-101](#).

ePWM XBAR Mux Configuration for TRIP10

Figure 12-162. TRIP10MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-101. TRIP10MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-101. TRIP10MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-101. TRIP10MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	<p>Group Select Bits for Mux3: Selects 4X1 group output for TRIP10 of EPWM-XBAR</p> <p>00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3</p> <p>Refer to the EPWM X-BAR section of this chapter for more details.</p>
5-4	Mux2	R/W	0h	<p>Group Select Bits for Mux2: Selects 4X1 group output for TRIP10 of EPWM-XBAR</p> <p>00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2</p> <p>Refer to the EPWM X-BAR section of this chapter for more details.</p>
3-2	Mux1	R/W	0h	<p>Group Select Bits for Mux1: Selects 4X1 group output for TRIP10 of EPWM-XBAR</p> <p>00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1</p> <p>Refer to the EPWM X-BAR section of this chapter for more details.</p>
1-0	Mux0	R/W	0h	<p>Group Select Bits for Mux0: Selects 4X1 group output for TRIP10 of EPWM-XBAR</p> <p>00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0</p> <p>Refer to the EPWM X-BAR section of this chapter for more details.</p>

12.4.3.12 TRIP10MUX16TO31CFG Register (offset = 16h) [reset = 0h]

TRIP10MUX16TO31CFG is shown in [Figure 12-163](#) and described in [Table 12-102](#).

ePWM XBAR Mux Configuration for TRIP10

Figure 12-163. TRIP10MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-102. TRIP10MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-102. TRIP10MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-102. TRIP10MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for TRIP10 of EPWM-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.13 TRIP11MUX0TO15CFG Register (offset = 18h) [reset = 0h]

TRIP11MUX0TO15CFG is shown in [Figure 12-164](#) and described in [Table 12-103](#).

ePWM XBAR Mux Configuration for TRIP11

Figure 12-164. TRIP11MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-103. TRIP11MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-103. TRIP11MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-103. TRIP11MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.14 TRIP11MUX16TO31CFG Register (offset = 1Ah) [reset = 0h]

TRIP11MUX16TO31CFG is shown in [Figure 12-165](#) and described in [Table 12-104](#).

ePWM XBAR Mux Configuration for TRIP11

Figure 12-165. TRIP11MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-104. TRIP11MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-104. TRIP11MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-104. TRIP11MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for TRIP11 of EPWM-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.15 TRIP12MUX0TO15CFG Register (offset = 1Ch) [reset = 0h]

TRIP12MUX0TO15CFG is shown in [Figure 12-166](#) and described in [Table 12-105](#).

ePWM XBAR Mux Configuration for TRIP12

Figure 12-166. TRIP12MUX0TO15CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-105. TRIP12MUX0TO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux15	R/W	0h	Group Select Bits for Mux15: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux15 01 : Select .2 input for Mux15 10 : Select .3 input for Mux15 11 : Select .4 input for Mux15 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux14	R/W	0h	Group Select Bits for Mux14: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux14 01 : Select .2 input for Mux14 10 : Select .3 input for Mux14 11 : Select .4 input for Mux14 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux13	R/W	0h	Group Select Bits for Mux13: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux13 01 : Select .2 input for Mux13 10 : Select .3 input for Mux13 11 : Select .4 input for Mux13 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux12	R/W	0h	Group Select Bits for Mux12: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux12 01 : Select .2 input for Mux12 10 : Select .3 input for Mux12 11 : Select .4 input for Mux12 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux11	R/W	0h	Group Select Bits for Mux11: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux11 01 : Select .2 input for Mux11 10 : Select .3 input for Mux11 11 : Select .4 input for Mux11 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-105. TRIP12MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux10	R/W	0h	Group Select Bits for Mux10: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux10 01 : Select .2 input for Mux10 10 : Select .3 input for Mux10 11 : Select .4 input for Mux10 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux9	R/W	0h	Group Select Bits for Mux9: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux9 01 : Select .2 input for Mux9 10 : Select .3 input for Mux9 11 : Select .4 input for Mux9 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux8	R/W	0h	Group Select Bits for Mux8: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux8 01 : Select .2 input for Mux8 10 : Select .3 input for Mux8 11 : Select .4 input for Mux8 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux7	R/W	0h	Group Select Bits for Mux7: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux7 01 : Select .2 input for Mux7 10 : Select .3 input for Mux7 11 : Select .4 input for Mux7 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux6	R/W	0h	Group Select Bits for Mux6: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux6 01 : Select .2 input for Mux6 10 : Select .3 input for Mux6 11 : Select .4 input for Mux6 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux5	R/W	0h	Group Select Bits for Mux5: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux5 01 : Select .2 input for Mux5 10 : Select .3 input for Mux5 11 : Select .4 input for Mux5 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux4	R/W	0h	Group Select Bits for Mux4: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux4 01 : Select .2 input for Mux4 10 : Select .3 input for Mux4 11 : Select .4 input for Mux4 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-105. TRIP12MUX0TO15CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux3	R/W	0h	Group Select Bits for Mux3: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux3 01 : Select .2 input for Mux3 10 : Select .3 input for Mux3 11 : Select .4 input for Mux3 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux2	R/W	0h	Group Select Bits for Mux2: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux2 01 : Select .2 input for Mux2 10 : Select .3 input for Mux2 11 : Select .4 input for Mux2 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux1	R/W	0h	Group Select Bits for Mux1: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux1 01 : Select .2 input for Mux1 10 : Select .3 input for Mux1 11 : Select .4 input for Mux1 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux0	R/W	0h	Group Select Bits for Mux0: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux0 01 : Select .2 input for Mux0 10 : Select .3 input for Mux0 11 : Select .4 input for Mux0 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.16 TRIP12MUX16TO31CFG Register (offset = 1Eh) [reset = 0h]

TRIP12MUX16TO31CFG is shown in [Figure 12-167](#) and described in [Table 12-106](#).

ePWM XBAR Mux Configuration for TRIP12

Figure 12-167. TRIP12MUX16TO31CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24								
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16								
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-106. TRIP12MUX16TO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Mux31	R/W	0h	Group Select Bits for Mux31: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux31 01 : Select .2 input for Mux31 10 : Select .3 input for Mux31 11 : Select .4 input for Mux31 Refer to the EPWM X-BAR section of this chapter for more details.
29-28	Mux30	R/W	0h	Group Select Bits for Mux30: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux30 01 : Select .2 input for Mux30 10 : Select .3 input for Mux30 11 : Select .4 input for Mux30 Refer to the EPWM X-BAR section of this chapter for more details.
27-26	Mux29	R/W	0h	Group Select Bits for Mux29: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux29 01 : Select .2 input for Mux29 10 : Select .3 input for Mux29 11 : Select .4 input for Mux29 Refer to the EPWM X-BAR section of this chapter for more details.
25-24	Mux28	R/W	0h	Group Select Bits for Mux28: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux28 01 : Select .2 input for Mux28 10 : Select .3 input for Mux28 11 : Select .4 input for Mux28 Refer to the EPWM X-BAR section of this chapter for more details.
23-22	Mux27	R/W	0h	Group Select Bits for Mux27: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux27 01 : Select .2 input for Mux27 10 : Select .3 input for Mux27 11 : Select .4 input for Mux27 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-106. TRIP12MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	Mux26	R/W	0h	Group Select Bits for Mux26: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux26 01 : Select .2 input for Mux26 10 : Select .3 input for Mux26 11 : Select .4 input for Mux26 Refer to the EPWM X-BAR section of this chapter for more details.
19-18	Mux25	R/W	0h	Group Select Bits for Mux25: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux25 01 : Select .2 input for Mux25 10 : Select .3 input for Mux25 11 : Select .4 input for Mux25 Refer to the EPWM X-BAR section of this chapter for more details.
17-16	Mux24	R/W	0h	Group Select Bits for Mux24: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux24 01 : Select .2 input for Mux24 10 : Select .3 input for Mux24 11 : Select .4 input for Mux24 Refer to the EPWM X-BAR section of this chapter for more details.
15-14	Mux23	R/W	0h	Group Select Bits for Mux23: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux23 01 : Select .2 input for Mux23 10 : Select .3 input for Mux23 11 : Select .4 input for Mux23 Refer to the EPWM X-BAR section of this chapter for more details.
13-12	Mux22	R/W	0h	Group Select Bits for Mux22: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux22 01 : Select .2 input for Mux22 10 : Select .3 input for Mux22 11 : Select .4 input for Mux22 Refer to the EPWM X-BAR section of this chapter for more details.
11-10	Mux21	R/W	0h	Group Select Bits for Mux21: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux21 01 : Select .2 input for Mux21 10 : Select .3 input for Mux21 11 : Select .4 input for Mux21 Refer to the EPWM X-BAR section of this chapter for more details.
9-8	Mux20	R/W	0h	Group Select Bits for Mux20: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux20 01 : Select .2 input for Mux20 10 : Select .3 input for Mux20 11 : Select .4 input for Mux20 Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-106. TRIP12MUX16TO31CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	Mux19	R/W	0h	Group Select Bits for Mux19: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux19 01 : Select .2 input for Mux19 10 : Select .3 input for Mux19 11 : Select .4 input for Mux19 Refer to the EPWM X-BAR section of this chapter for more details.
5-4	Mux18	R/W	0h	Group Select Bits for Mux18: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux18 01 : Select .2 input for Mux18 10 : Select .3 input for Mux18 11 : Select .4 input for Mux18 Refer to the EPWM X-BAR section of this chapter for more details.
3-2	Mux17	R/W	0h	Group Select Bits for Mux17: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux17 01 : Select .2 input for Mux17 10 : Select .3 input for Mux17 11 : Select .4 input for Mux17 Refer to the EPWM X-BAR section of this chapter for more details.
1-0	Mux16	R/W	0h	Group Select Bits for Mux16: Selects 4X1 group output for TRIP12 of EPWM-XBAR 00 : Select .1 input for Mux16 01 : Select .2 input for Mux16 10 : Select .3 input for Mux16 11 : Select .4 input for Mux16 Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.17 TRIP4MUXENABLE Register (offset = 20h) [reset = 0h]

TRIP4MUXENABLE is shown in [Figure 12-168](#) and described in [Table 12-107](#).

ePWM XBAR Mux Enable for TRIP4

Figure 12-168. TRIP4MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-107. TRIP4MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux31 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux31 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux30 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux30 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux29 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux29 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux28 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux28 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux27 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux27 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-107. TRIP4MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux26 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux26 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux25 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux25 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux24 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux24 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux23 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux23 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux22 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux22 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux21 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux21 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux20 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux20 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux19 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux19 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux18 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux18 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-107. TRIP4MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux17 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux17 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux16 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux16 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux15 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux15 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux14 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux14 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux13 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux13 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux12 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux12 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux11 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux11 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux10 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux10 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux9 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux9 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-107. TRIP4MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux8 is enabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux8 is disabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux7 is disabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux7 is enabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux6 is disabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux6 is enabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux5 is disabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux5 is enabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux4 is disabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux4 is enabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux3 is disabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux3 is enabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux2 is disabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux2 is enabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux1 is disabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux1 is enabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive TRIP4 of EPWM-XBAR 0: Respective output of Mux0 is disabled to drive the TRIP4 of EPWM-XBAR 1: Respective output of Mux0 is enabled to drive the TRIP4 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.18 TRIP5MUXENABLE Register (offset = 22h) [reset = 0h]

TRIP5MUXENABLE is shown in [Figure 12-169](#) and described in [Table 12-108](#).

ePWM XBAR Mux Enable for TRIP5

Figure 12-169. TRIP5MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-108. TRIP5MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux31 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux31 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux30 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux30 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux29 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux29 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux28 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux28 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux27 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux27 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-108. TRIP5MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux26 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux26 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux25 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux25 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux24 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux24 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux23 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux23 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux22 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux22 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux21 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux21 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux20 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux20 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux19 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux19 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux18 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux18 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-108. TRIP5MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux17 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux17 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux16 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux16 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux15 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux15 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux14 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux14 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux13 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux13 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux12 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux12 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux11 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux11 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux10 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux10 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux9 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux9 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-108. TRIP5MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux8 is enabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux8 is disabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux7 is disabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux7 is enabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux6 is disabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux6 is enabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux5 is disabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux5 is enabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux4 is disabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux4 is enabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux3 is disabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux3 is enabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux2 is disabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux2 is enabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux1 is disabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux1 is enabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive TRIP5 of EPWM-XBAR 0: Respective output of Mux0 is disabled to drive the TRIP5 of EPWM-XBAR 1: Respective output of Mux0 is enabled to drive the TRIP5 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.19 TRIP7MUXENABLE Register (offset = 24h) [reset = 0h]

TRIP7MUXENABLE is shown in [Figure 12-170](#) and described in [Table 12-109](#).

ePWM XBAR Mux Enable for TRIP7

Figure 12-170. TRIP7MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-109. TRIP7MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux31 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux31 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux30 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux30 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux29 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux29 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux28 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux28 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux27 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux27 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-109. TRIP7MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux26 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux26 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux25 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux25 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux24 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux24 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux23 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux23 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux22 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux22 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux21 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux21 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux20 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux20 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux19 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux19 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux18 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux18 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-109. TRIP7MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux17 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux17 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux16 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux16 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux15 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux15 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux14 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux14 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux13 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux13 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux12 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux12 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux11 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux11 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux10 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux10 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux9 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux9 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-109. TRIP7MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux8 is enabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux8 is disabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux7 is disabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux7 is enabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux6 is disabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux6 is enabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux5 is disabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux5 is enabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux4 is disabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux4 is enabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux3 is disabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux3 is enabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux2 is disabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux2 is enabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux1 is disabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux1 is enabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive TRIP7 of EPWM-XBAR 0: Respective output of Mux0 is disabled to drive the TRIP7 of EPWM-XBAR 1: Respective output of Mux0 is enabled to drive the TRIP7 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.20 TRIP8MUXENABLE Register (offset = 26h) [reset = 0h]

TRIP8MUXENABLE is shown in [Figure 12-171](#) and described in [Table 12-110](#).

ePWM XBAR Mux Enable for TRIP8

Figure 12-171. TRIP8MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-110. TRIP8MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux31 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux31 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux30 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux30 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux29 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux29 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux28 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux28 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux27 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux27 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-110. TRIP8MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux26 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux26 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux25 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux25 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux24 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux24 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux23 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux23 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux22 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux22 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux21 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux21 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux20 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux20 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux19 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux19 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux18 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux18 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-110. TRIP8MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux17 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux17 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux16 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux16 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux15 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux15 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux14 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux14 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux13 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux13 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux12 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux12 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux11 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux11 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux10 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux10 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux9 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux9 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-110. TRIP8MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux8 is enabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux8 is disabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux7 is disabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux7 is enabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux6 is disabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux6 is enabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux5 is disabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux5 is enabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux4 is disabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux4 is enabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux3 is disabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux3 is enabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux2 is disabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux2 is enabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux1 is disabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux1 is enabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive TRIP8 of EPWM-XBAR 0: Respective output of Mux0 is disabled to drive the TRIP8 of EPWM-XBAR 1: Respective output of Mux0 is enabled to drive the TRIP8 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.21 TRIP9MUXENABLE Register (offset = 28h) [reset = 0h]

TRIP9MUXENABLE is shown in [Figure 12-172](#) and described in [Table 12-111](#).

ePWM XBAR Mux Enable for TRIP9

Figure 12-172. TRIP9MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-111. TRIP9MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux31 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux31 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux30 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux30 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux29 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux29 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux28 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux28 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux27 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux27 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-111. TRIP9MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux26 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux26 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux25 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux25 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux24 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux24 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux23 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux23 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux22 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux22 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux21 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux21 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux20 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux20 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux19 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux19 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux18 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux18 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-111. TRIP9MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux17 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux17 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux16 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux16 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux15 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux15 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux14 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux14 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux13 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux13 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux12 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux12 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux11 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux11 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux10 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux10 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux9 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux9 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-111. TRIP9MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux8 is enabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux8 is disabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux7 is disabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux7 is enabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux6 is disabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux6 is enabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux5 is disabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux5 is enabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux4 is disabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux4 is enabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux3 is disabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux3 is enabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux2 is disabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux2 is enabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux1 is disabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux1 is enabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive TRIP9 of EPWM-XBAR 0: Respective output of Mux0 is disabled to drive the TRIP9 of EPWM-XBAR 1: Respective output of Mux0 is enabled to drive the TRIP9 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.22 TRIP10MUXENABLE Register (offset = 2Ah) [reset = 0h]

TRIP10MUXENABLE is shown in [Figure 12-173](#) and described in [Table 12-112](#).

ePWM XBAR Mux Enable for TRIP10

Figure 12-173. TRIP10MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-112. TRIP10MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux31 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux31 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux30 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux30 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux29 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux29 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux28 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux28 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux27 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux27 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-112. TRIP10MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux26 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux26 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux25 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux25 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux24 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux24 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux23 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux23 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux22 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux22 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux21 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux21 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux20 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux20 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux19 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux19 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux18 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux18 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-112. TRIP10MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux17 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux17 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux16 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux16 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux15 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux15 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux14 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux14 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux13 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux13 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux12 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux12 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux11 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux11 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux10 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux10 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux9 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux9 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-112. TRIP10MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux8 is enabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux8 is disabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux7 is disabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux7 is enabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux6 is disabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux6 is enabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux5 is disabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux5 is enabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux4 is disabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux4 is enabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux3 is disabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux3 is enabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux2 is disabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux2 is enabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux1 is disabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux1 is enabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive TRIP10 of EPWM-XBAR 0: Respective output of Mux0 is disabled to drive the TRIP10 of EPWM-XBAR 1: Respective output of Mux0 is enabled to drive the TRIP10 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.23 TRIP11MUXENABLE Register (offset = 2Ch) [reset = 0h]

TRIP11MUXENABLE is shown in [Figure 12-174](#) and described in [Table 12-113](#).

ePWM XBAR Mux Enable for TRIP11

Figure 12-174. TRIP11MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-113. TRIP11MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux31 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux31 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux30 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux30 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux29 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux29 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux28 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux28 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux27 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux27 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-113. TRIP11MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux26 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux26 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux25 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux25 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux24 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux24 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux23 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux23 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux22 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux22 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux21 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux21 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux20 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux20 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux19 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux19 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux18 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux18 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-113. TRIP11MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux17 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux17 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux16 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux16 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux15 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux15 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux14 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux14 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux13 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux13 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux12 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux12 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux11 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux11 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux10 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux10 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux9 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux9 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-113. TRIP11MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux8 is enabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux8 is disabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux7 is disabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux7 is enabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux6 is disabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux6 is enabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux5 is disabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux5 is enabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux4 is disabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux4 is enabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux3 is disabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux3 is enabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux2 is disabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux2 is enabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux1 is disabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux1 is enabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive TRIP11 of EPWM-XBAR 0: Respective output of Mux0 is disabled to drive the TRIP11 of EPWM-XBAR 1: Respective output of Mux0 is enabled to drive the TRIP11 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.24 TRIP12MUXENABLE Register (offset = 2Eh) [reset = 0h]

TRIP12MUXENABLE is shown in [Figure 12-175](#) and described in [Table 12-114](#).

ePWM XBAR Mux Enable for TRIP12

Figure 12-175. TRIP12MUXENABLE Register

31	30	29	28	27	26	25	24
Mux31	Mux30	Mux29	Mux28	Mux27	Mux26	Mux25	Mux24
R/W-0h							
23	22	21	20	19	18	17	16
Mux23	Mux22	Mux21	Mux20	Mux19	Mux18	Mux17	Mux16
R/W-0h							
15	14	13	12	11	10	9	8
Mux15	Mux14	Mux13	Mux12	Mux11	Mux10	Mux9	Mux8
R/W-0h							
7	6	5	4	3	2	1	0
Mux7	Mux6	Mux5	Mux4	Mux3	Mux2	Mux1	Mux0
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-114. TRIP12MUXENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Mux31	R/W	0h	Selects the output of Mux31 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux31 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux31 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
30	Mux30	R/W	0h	Selects the output of Mux30 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux30 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux30 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
29	Mux29	R/W	0h	Selects the output of Mux29 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux29 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux29 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
28	Mux28	R/W	0h	Selects the output of Mux28 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux28 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux28 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
27	Mux27	R/W	0h	Selects the output of Mux27 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux27 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux27 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-114. TRIP12MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	Mux26	R/W	0h	Selects the output of Mux26 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux26 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux26 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
25	Mux25	R/W	0h	Selects the output of Mux25 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux25 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux25 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
24	Mux24	R/W	0h	Selects the output of Mux24 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux24 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux24 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
23	Mux23	R/W	0h	Selects the output of Mux23 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux23 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux23 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
22	Mux22	R/W	0h	Selects the output of Mux22 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux22 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux22 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
21	Mux21	R/W	0h	Selects the output of Mux21 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux21 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux21 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
20	Mux20	R/W	0h	Selects the output of Mux20 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux20 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux20 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
19	Mux19	R/W	0h	Selects the output of Mux19 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux19 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux19 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
18	Mux18	R/W	0h	Selects the output of Mux18 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux18 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux18 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

Table 12-114. TRIP12MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	Mux17	R/W	0h	Selects the output of Mux17 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux17 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux17 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
16	Mux16	R/W	0h	Selects the output of Mux16 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux16 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux16 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
15	Mux15	R/W	0h	Selects the output of Mux15 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux15 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux15 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
14	Mux14	R/W	0h	Selects the output of Mux14 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux14 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux14 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
13	Mux13	R/W	0h	Selects the output of Mux13 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux13 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux13 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
12	Mux12	R/W	0h	Selects the output of Mux12 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux12 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux12 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
11	Mux11	R/W	0h	Selects the output of Mux11 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux11 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux11 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
10	Mux10	R/W	0h	Selects the output of Mux10 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux10 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux10 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
9	Mux9	R/W	0h	Selects the output of Mux9 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux9 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux9 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

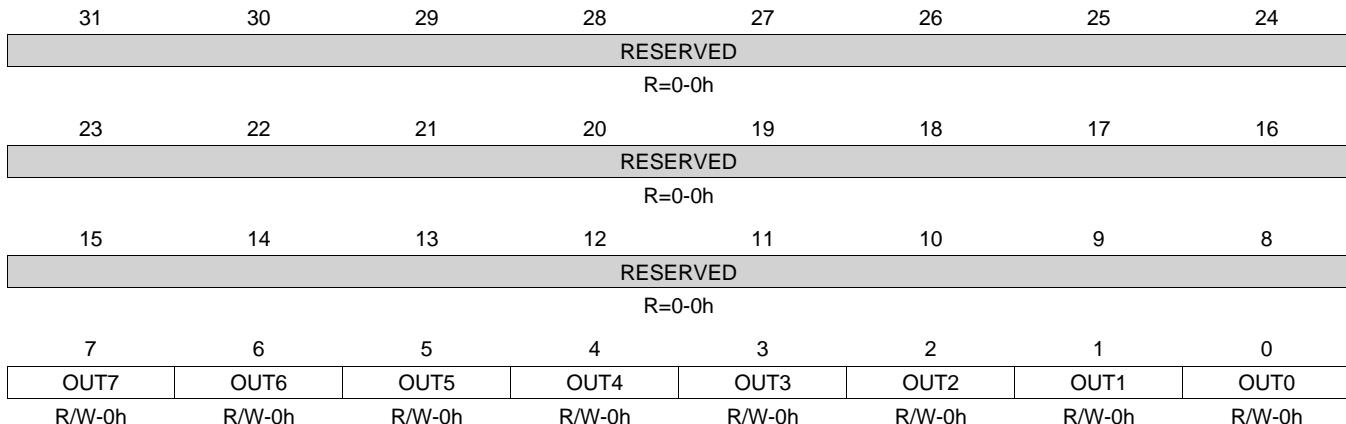
Table 12-114. TRIP12MUXENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Mux8	R/W	0h	Selects the output of Mux8 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux8 is enabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux8 is disabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
7	Mux7	R/W	0h	Selects the output of Mux7 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux7 is disabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux7 is enabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
6	Mux6	R/W	0h	Selects the output of Mux6 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux6 is disabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux6 is enabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
5	Mux5	R/W	0h	Selects the output of Mux5 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux5 is disabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux5 is enabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
4	Mux4	R/W	0h	Selects the output of Mux4 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux4 is disabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux4 is enabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
3	Mux3	R/W	0h	Selects the output of Mux3 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux3 is disabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux3 is enabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
2	Mux2	R/W	0h	Selects the output of Mux2 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux2 is disabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux2 is enabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
1	Mux1	R/W	0h	Selects the output of Mux1 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux1 is disabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux1 is enabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.
0	Mux0	R/W	0h	Selects the output of mux0 to drive TRIP12 of EPWM-XBAR 0: Respective output of Mux0 is disabled to drive the TRIP12 of EPWM-XBAR 1: Respective output of Mux0 is enabled to drive the TRIP12 of EPWM-XBAR Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.25 TRIPOUTINV Register (offset = 38h) [reset = 0h]

TRIPOUTINV is shown in [Figure 12-176](#) and described in [Table 12-115](#).

ePWM XBAR Output Inversion Register

Figure 12-176. TRIPOUTINV Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-115. TRIPOUTINV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-8	RESERVED	R=0	0h	Reserved
7	OUT7	R/W	0h	Selects polarity for TRIP12 of EPWM-XBAR 0: drives active high output 1: drives active-low output Refer to the EPWM X-BAR section of this chapter for more details.
6	OUT6	R/W	0h	Selects polarity for TRIP11 of EPWM-XBAR 0: drives active high output 1: drives active-low output Refer to the EPWM X-BAR section of this chapter for more details.
5	OUT5	R/W	0h	Selects polarity for TRIP10 of EPWM-XBAR 0: drives active high output 1: drives active-low output Refer to the EPWM X-BAR section of this chapter for more details.
4	OUT4	R/W	0h	Selects polarity for TRIP9 of EPWM-XBAR 0: drives active high output 1: drives active-low output Refer to the EPWM X-BAR section of this chapter for more details.
3	OUT3	R/W	0h	Selects polarity for TRIP8 of EPWM-XBAR 0: drives active high output 1: drives active-low output Refer to the EPWM X-BAR section of this chapter for more details.
2	OUT2	R/W	0h	Selects polarity for TRIP7 of EPWM-XBAR 0: drives active high output 1: drives active-low output Refer to the EPWM X-BAR section of this chapter for more details.

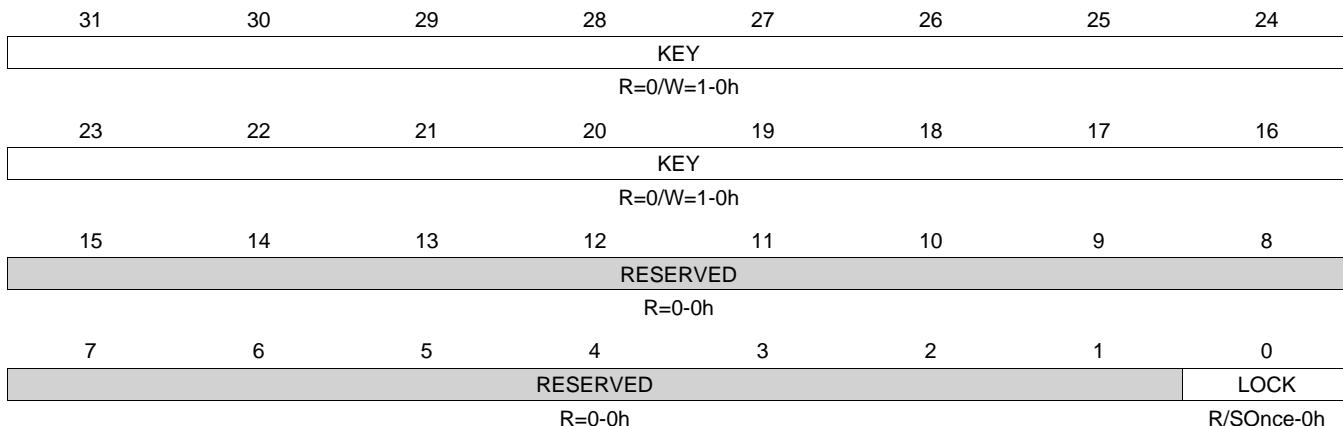
Table 12-115. TRIPOUTINV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OUT1	R/W	0h	Selects polarity for TRIP5 of EPWM-XBAR 0: drives active high output 1: drives active-low output Refer to the EPWM X-BAR section of this chapter for more details.
0	OUT0	R/W	0h	Selects polarity for TRIP4 of EPWM-XBAR 0: drives active high output 1: drives active-low output Refer to the EPWM X-BAR section of this chapter for more details.

12.4.3.26 TRIPLOCK Register (offset = 3Eh) [reset = 0h]

TRIPLOCK is shown in [Figure 12-177](#) and described in [Table 12-116](#).

ePWM XBAR Configuration Lock register

Figure 12-177. TRIPLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-116. TRIPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R=0/W=1	0h	Bit-0 of this register can be set only if KEY= 0x5a5a
15-1	RESERVED	R=0	0h	Reserved
0	LOCK	R/SOnce	0h	Locks the configuration for EPWM-XBAR. Once the configuration is locked, writes to the below registers for EPWM-XBAR is blocked. Registers Affected by the LOCK mechanism: EPWM-XBAROUTyMUX0TO15CFG EPWM-XBAROUTyMUX16TO31CFG EPWM-XBAROUTyMUXENABLE EPWM-XBAROUTLATEN EPWM-XBAROUTINV 0: Writes to the above registers are allowed 1: Writes to the above registers are blocked Note: [1] LOCK mechanism only applies to writes. Reads are never blocked.

12.4.4 TRIG_REGS Registers

Table 12-117 lists the memory-mapped registers for the TRIG_REGS. All register offset addresses not listed in Table 12-117 should be considered as reserved locations and the register contents should not be modified.

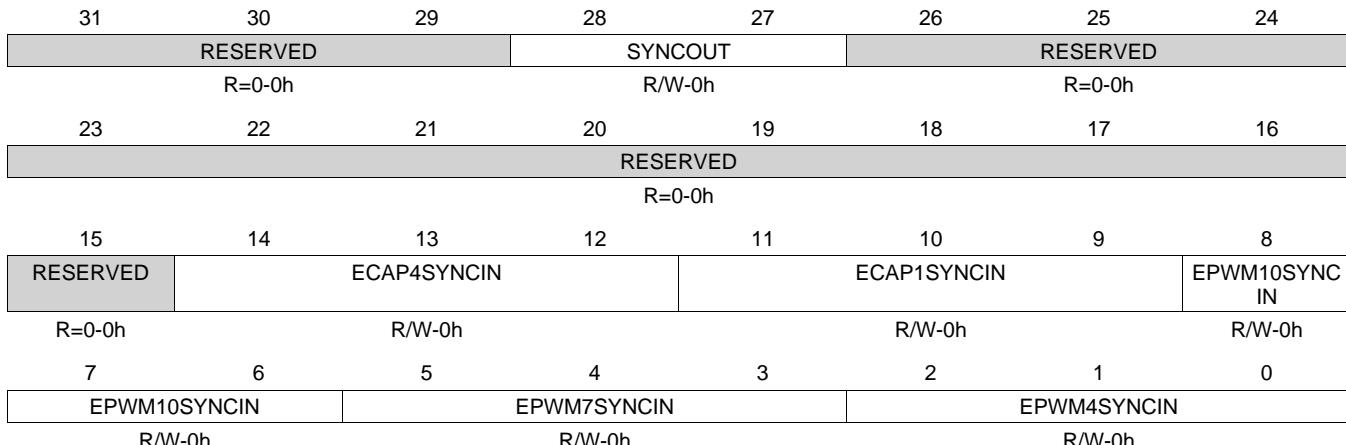
Table 12-117. TRIG_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	SYNCSELECT	Sync Input and Output Select Register	Section 12.4.4.1	EALLOW
2h	EXTADCSOCSELECT	External ADCSOC Select Register	Section 12.4.4.2	EALLOW
4h	SYNCSOCLOCK	SYNCSEL and EXTADCSOC Select Lock register	Section 12.4.4.3	EALLOW

12.4.4.1 SYNCSELECT Register (offset = 0h) [reset = 0h]

SYNCSELECT is shown in [Figure 12-178](#) and described in [Table 12-118](#).

Sync Input and Output Select Register

Figure 12-178. SYNCSELECT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-118. SYNCSELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R=0	0h	Reserved
28-27	SYNCOUT	R/W	0h	Select Syncout Source: 00: EPWM1SYNCOUT selected 01: EPWM4SYNCOUT selected 10: EPPW7SYNCOUT selected 11: EPWM10SYNCOUT selected
26-16	RESERVED	R=0	0h	Reserved
15	RESERVED	R=0	0h	Reserved
14-12	ECAP4SYNCIN	R/W	0h	Selects Sync Input Source for ECAP4: 000: EPWM1SYNCOUT selected 001: EPWM4SYNCOUT selected 010: EPPW7SYNCOUT selected 011: EPWM10SYNCOUT selected 100: ECAP1SYNCOUT selected 101: EXTSYNCIN1 selected 110: EXTSYNCIN2 selected 111: Reserved Notes: [1] Reserved position defaults to 000 selection

Table 12-118. SYNCSELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	ECAP1SYNCIN	R/W	0h	<p>Selects Sync Input Source for ECAP1:</p> <p>000: EPWM1SYNCOUT selected</p> <p>001: EPWM4SYNCOUT selected</p> <p>010: EPPW7SYNCOUT selected</p> <p>011: EPWM10SYNCOUT selected</p> <p>100: ECAP1SYNCOUT selected (Reserved)</p> <p>101: EXTSYNCIN1 selected</p> <p>110: EXTSYNCIN2 selected</p> <p>111: Reserved</p> <p>Notes:</p> <p>[1] Reserved position defaults to 000 selection</p>
8-6	EPWM10SYNCIN	R/W	0h	<p>Selects Sync Input Source for EPWM10:</p> <p>000: EPWM1SYNCOUT selected</p> <p>001: EPWM4SYNCOUT selected</p> <p>010: EPPW7SYNCOUT selected</p> <p>011: EPWM10SYNCOUT selected (Reserved)</p> <p>100: ECAP1SYNCOUT selected (Reserved)</p> <p>101: EXTSYNCIN1 selected</p> <p>110: EXTSYNCIN2 selected</p> <p>111: Reserved</p> <p>Notes:</p> <p>[1] Reserved position defaults to 000 selection</p>
5-3	EPWM7SYNCIN	R/W	0h	<p>Selects Sync Input Source for EPWM7:</p> <p>000: EPWM1SYNCOUT selected</p> <p>001: EPWM4SYNCOUT selected</p> <p>010: EPPW7SYNCOUT selected (Reserved)</p> <p>011: EPWM10SYNCOUT selected (Reserved)</p> <p>100: ECAP1SYNCOUT selected (Reserved)</p> <p>101: EXTSYNCIN1 selected</p> <p>110: EXTSYNCIN2 selected</p> <p>111: Reserved</p> <p>Notes:</p> <p>[1] Reserved position defaults to 000 selection</p>
2-0	EPWM4SYNCIN	R/W	0h	<p>Selects Sync Input Source for EPWM4:</p> <p>000: EPWM1SYNCOUT selected</p> <p>001: EPWM4SYNCOUT selected (Reserved)</p> <p>010: EPPW7SYNCOUT selected (Reserved)</p> <p>011: EPWM10SYNCOUT selected (Reserved)</p> <p>100: ECAP1SYNCOUT selected (Reserved)</p> <p>101: EXTSYNCIN1 selected</p> <p>110: EXTSYNCIN2 selected</p> <p>111: Reserved</p> <p>Notes:</p> <p>[1] Reserved position defaults to 000 selection</p>

12.4.4.2 EXTADCSOCSELECT Register (offset = 2h) [reset = 0h]

EXTADCSOCSELECT is shown in [Figure 12-179](#) and described in [Table 12-119](#).

External ADCSOC Select Register

Figure 12-179. EXTADCSOCSELECT Register

31	30	29	28	27	26	25	24
		RESERVED		PWM12SOCBE N	PWM11SOCBE N	PWM10SOCBE N	PWM9SOCBE N
		R=0-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PWM8SOCBE N	PWM7SOCBE N	PWM6SOCBE N	PWM5SOCBE N	PWM4SOCBE N	PWM3SOCBE N	PWM2SOCBE N	PWM1SOCBE N
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
	RESERVED			PWM12SOCAE N	PWM11SOCAE N	PWM10SOCAE N	PWM9SOCAE N
	R=0-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PWM8SOCAE N	PWM7SOCAE N	PWM6SOCAE N	PWM5SOCAE N	PWM4SOCAE N	PWM3SOCAE N	PWM2SOCAE N	PWM1SOCAE N
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-119. EXTADCSOCSELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R=0	0h	Reserved
27	PWM12SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
26	PWM11SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
25	PWM10SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
24	PWM9SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
23	PWM8SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
22	PWM7SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
21	PWM6SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
20	PWM5SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected

Table 12-119. EXTADCSOCSELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	PWM4SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
18	PWM3SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
17	PWM2SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
16	PWM1SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective EPWM SOCB output is not selected 1: Respective EPWM SOCB output is selected
15-12	RESERVED	R=0	0h	Reserved
11	PWM12SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
10	PWM11SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
9	PWM10SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
8	PWM9SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
7	PWM8SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
6	PWM7SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
5	PWM6SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
4	PWM5SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
3	PWM4SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
2	PWM3SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected
1	PWM2SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected

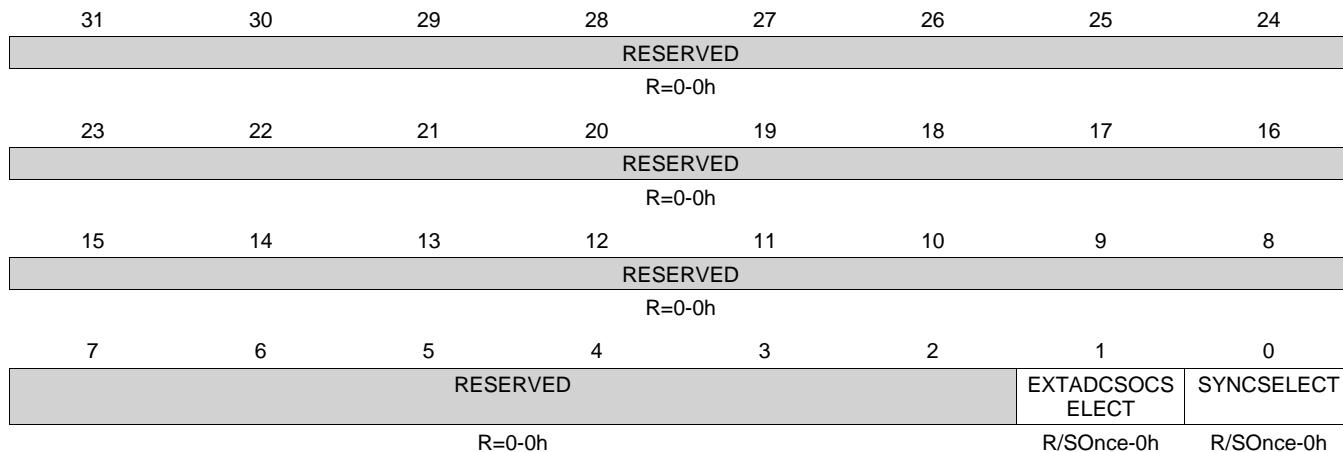
Table 12-119. EXTADCSOCSELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PWM1SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective EPWM SOCA output is not selected 1: Respective EPWM SOCA output is selected

12.4.4.3 SYNCSOCLOCK Register (offset = 4h) [reset = 0h]

SYNCSOCLOCK is shown in [Figure 12-180](#) and described in [Table 12-120](#).

SYNCSEL and EXTADCSOC Select Lock register

Figure 12-180. SYNCSOCLOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 12-120. SYNCSOCLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-2	RESERVED	R=0	0h	Reserved
1	EXTADCSOCSELECT	R/SOnce	0h	<p>EXTADCSOCSELECT Register Lock bit: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] Any bit in this register, once set can only be cleared through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect [2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed
0	SYNCSELECT	R/SOnce	0h	<p>SYNCSELECT Register Lock bit: 0: Respective register is not locked 1: Respective register is locked.</p> <p>Notes:</p> <ul style="list-style-type: none"> [1] Any bit in this register, once set can only be cleared through a CPU1.SYSRSn. Write of 0 to any bit of this register has no effect [2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed

High-Resolution Pulse Width Modulator (HRPWM)

This document is used in conjunction with the device-specific *Enhanced Pulse Width Modulator (ePWM) Module Reference Guide*. The HRPWM module described in this reference guide is a Type 2 HRPWM. See the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* ([SPRU566](#)) for a list of all devices with an HRPWM module of the same type, to determine the differences between types, and for a list of device-specific differences within a type.

Topic	Page
13.1 Introduction	1749
13.2 Operational Description of HRPWM	1751
13.3 Appendix A: SFO Library Software - SFO_TI_Build_V7.lib	1772

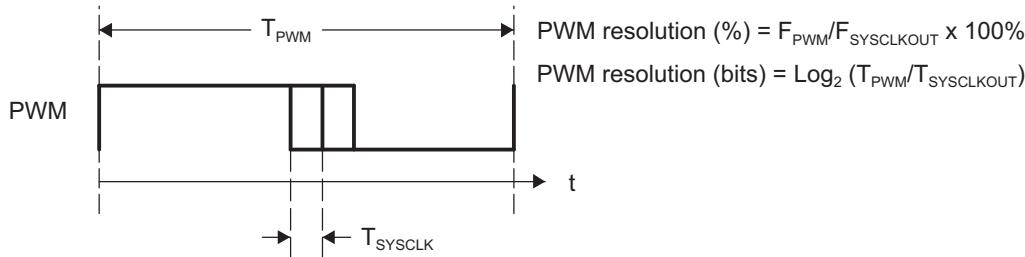
13.1 Introduction

This module extends the time resolution capabilities of the conventionally derived digital pulse width modulator (PWM). HRPWM is typically used when PWM resolution falls below ~ 9-10 bits. The key features of HRPWM are:

- Extended time resolution capability
- Used in both duty cycle and phase-shift control methods
- Finer time granularity control or edge positioning using extensions to the Compare A, Compare B and Phase registers
- Implemented using the A & B signal path of PWM, that is, on the EPWMxA and EPWMxB output.
- Dead band high-resolution control for falling and rising edge delay in half cycle clocking operation
- Self-check diagnostics software mode to check if the micro edge positioner (MEP) logic is running optimally
- Enables high resolution output swapping on the EPWMxA and EPWMxB output
- Enables high-resolution output on EPWMxB signal output via inversion of EPWMxA signal output
- Enables high-resolution period, duty and phase control on the EPWMxA and EPWMxB output on devices with an ePWM module. See the device-specific data manual to determine if your device has an ePWM module for high-resolution period support.

The ePWM peripheral is used to perform a function mathematically equivalent to a digital-to-analog converter (DAC). As shown in [Figure 13-1](#), the effective resolution for conventionally generated PWM is a function of PWM frequency (or period) and system clock frequency.

Figure 13-1. Resolution Calculations for Conventionally Generated PWM



If the required PWM operating frequency does not offer sufficient resolution in PWM mode, you may want to consider HRPWM. As an example of improved performance offered by HRPWM, [Table 13-1](#) shows resolution in bits for various PWM frequencies. These values assume a MEP step size of 180 ps. See the device-specific data sheet for typical and maximum performance specifications for the MEP.

Table 13-1. Resolution for PWM and HRPWM

PWM Freq (kHz)	Regular Resolution (PWM)		High Resolution (HRPWM)	
	Bits	%	Bits	%
100 MHz SYCLKOUT				
20	12.3	0.02	18.1	0.000
50	11	0.05	16.8	0.001
100	10	0.1	15.8	0.002
150	9.4	0.15	15.2	0.003
200	9	0.2	14.8	0.004
250	8.6	0.25	14.4	0.005
500	7.6	0.5	13.4	0.009
1000	6.6	1	12.4	0.018
1500	6.1	1.5	11.9	0.027
2000	5.6	2	11.4	0.036

Although each application may differ, typical low frequency PWM operation (below 250 kHz) may not require HRPWM. HRPWM capability is most useful for high frequency PWM requirements of power conversion topologies such as:

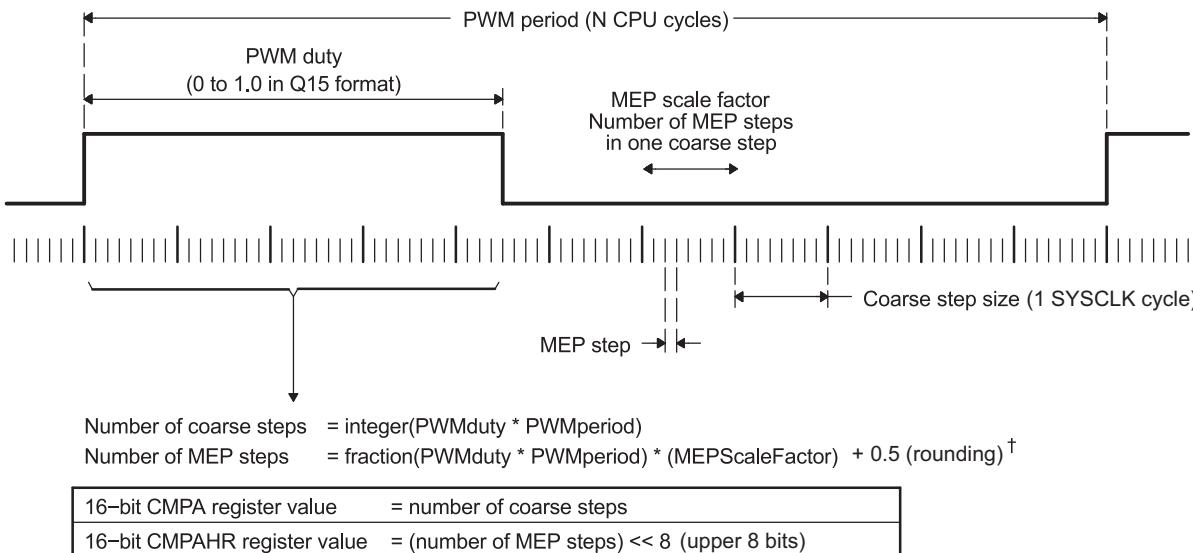
- Single-phase buck, boost, and flyback
- Multi-phase buck, boost, and flyback
- Phase-shifted full bridge
- Direct modulation of D-Class power amplifiers

13.2 Operational Description of HRPWM

The HRPWM is based on micro edge positioner (MEP) technology. MEP logic is capable of positioning an edge very finely by sub-dividing one coarse system clock of a conventional PWM generator. The time step accuracy is on the order of 150 ps. See the device-specific data sheet for the typical MEP step size on a particular device. The HRPWM also has a self-check software diagnostics mode to check if the MEP logic is running optimally, under all operating conditions. Details on software diagnostics and functions are in [Section 13.2.6](#).

[Figure 13-2](#) shows the relationship between one coarse system clock and edge position in terms of MEP steps, which are controlled via an 8-bit field in the Compare A extension register (CMPAHR). The same operating logic applies to CMPBHR as well.

Figure 13-2. Operating Logic Using MEP



[†] For MEP range and rounding adjustment. (0x0080 in Q8 format)

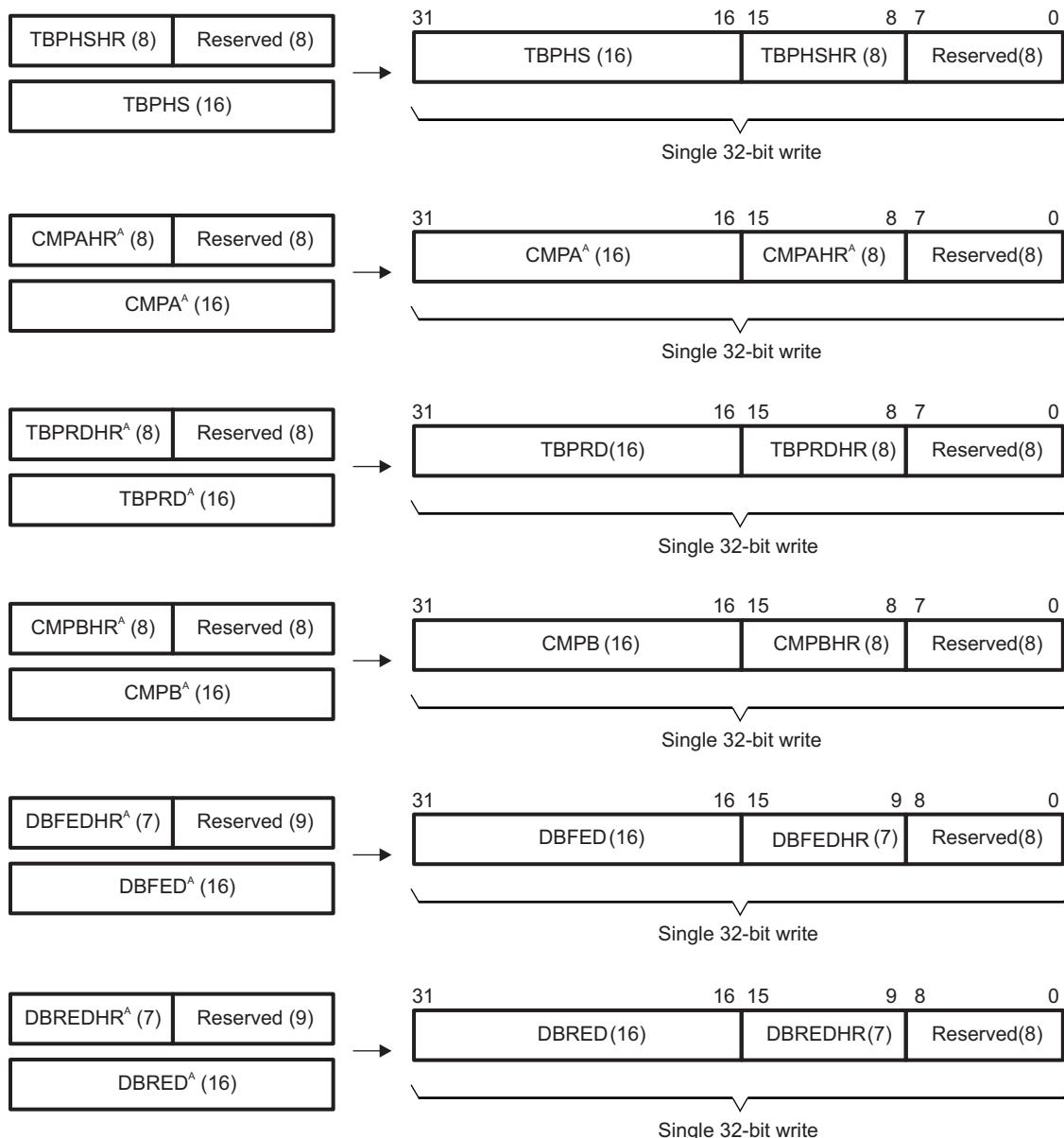
To generate an HRPWM waveform, configure the ePWM registers as you would to generate a conventional PWM of a given frequency and polarity. The HRPWM works together with the ePWM registers to extend edge resolution. Although many programming combinations are possible, only a few are needed and practical. These methods are described in [Section 13.2.7](#).

Registers discussed but not found in this document can be seen in the device-specific *Enhanced Pulse Width Modulator (ePWM) Module Reference Guide*.

13.2.1 Controlling the HRPWM Capabilities

The MEP of the HRPWM is controlled by six extension registers. These HRPWM registers are concatenated with the 16-bit TPHSHR, TBPRD, CMPA, CMPBM, DBREDM & DBFEDM registers used to control PWM operation.

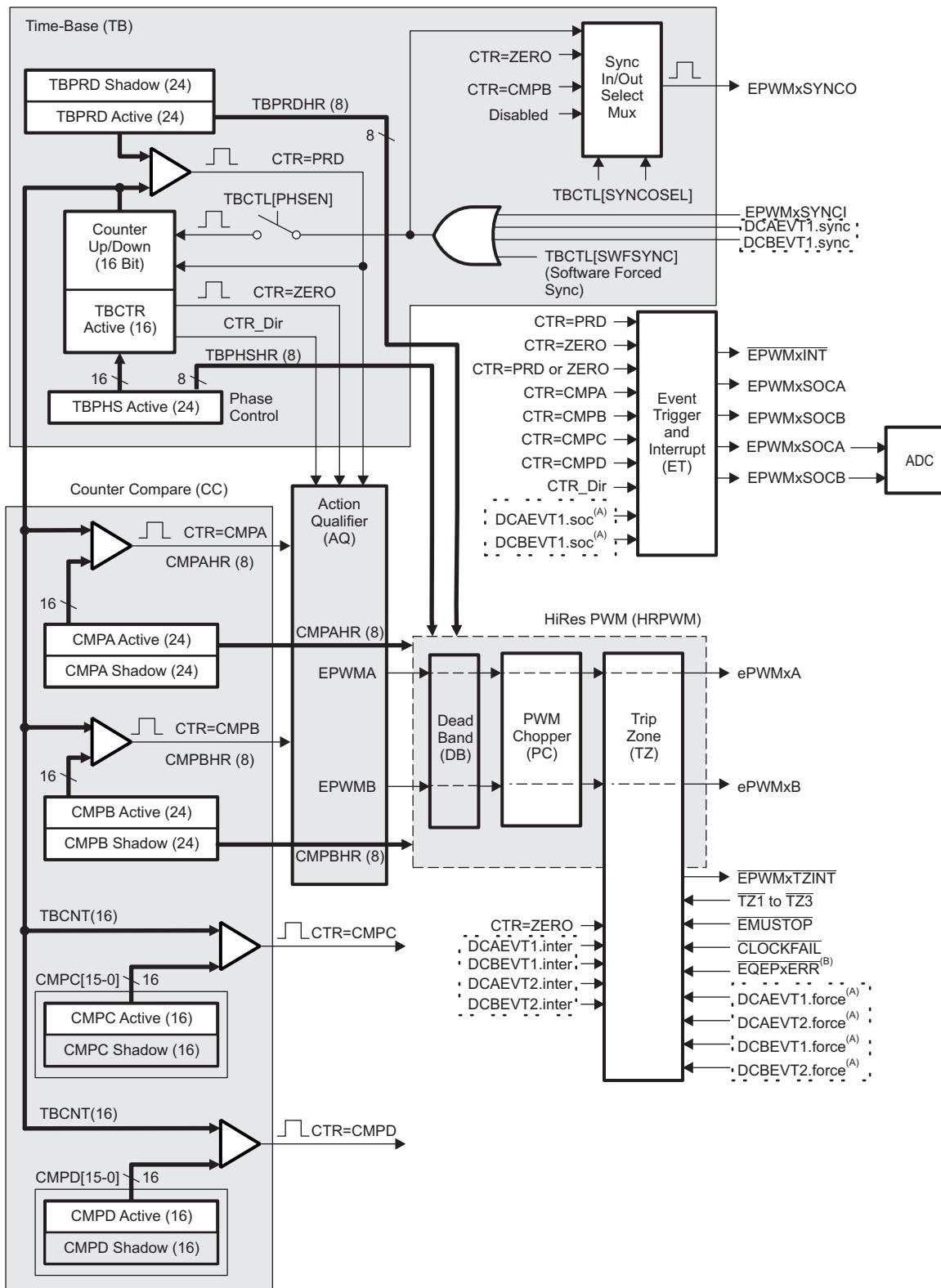
- TPHSHR - Time Base Phase High Resolution Register
- CMPAHR - Counter Compare A High Resolution Register
- TBPRDHDR - Time Base Period High Resolution Register. (available on some devices)
- CMPBHR - Compare B High Resolution Register
- DBREDHDR - Dead-Band Generator Rising Edge Delay High Resolution Register
- DBFEDHDR - Dead-Band Generator Falling Edge Delay High Resolution Register

Figure 13-3. HRPWM Extension Registers and Memory Configuration

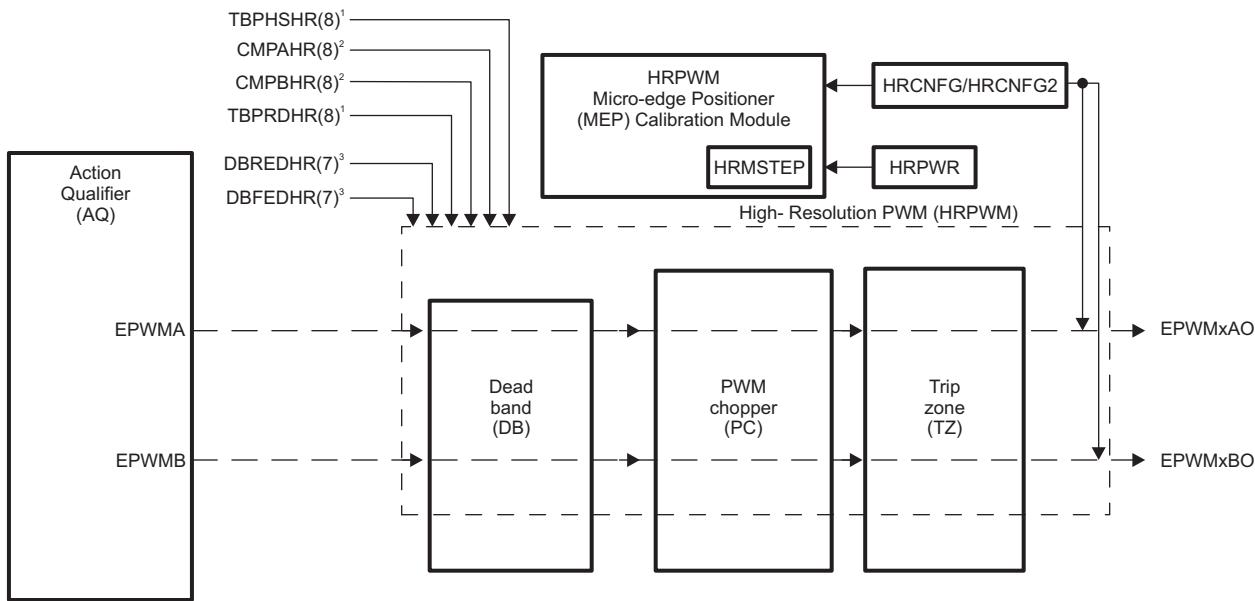
- A D dependant upon your device, these registers may be mirrored and can be written to at two different memory locations. Check the device-specific Technical Reference Manual's ePWM chapter for more details on how to read and write to these locations.

NOTE: HRPWM capabilities on Deadband Rising Edge Delay and Falling Edge Delay is applicable only during Dead Band half cycle clocking Operation. The number of MEP steps is half in size [bits 15:9]than duty and phase high resolution registers for the same reason

HRPWM capabilities are controlled using the Channel A & B PWM signal path. HRPWM support on the Dead band signal path is available by properly configuring the HRCNFG2 register. [Figure 13-4](#) shows how the HRPWM interfaces with the 8-bit extension registers.

Figure 13-4. HRPWM System Interface


A These events are generated by the ePWM digital compare (DC) submodule.

Figure 13-5. HRPWM Block Diagram

- (1) From ePWM Time-base (TB) submodule
- (2) From ePWM counter-compare (CC) submodule
- (3) From ePWM Deadband (DB) submodule

13.2.2 Configuring the HRPWM

Once the ePWM has been configured to provide conventional PWM of a given frequency and polarity, the HRPWM is configured by programming the HRCNFG register in that particular ePWM module's register space. This register provides the following configuration options:

Edge Mode — The MEP can be programmed to provide precise position control on the rising edge (RE), falling edge (FE) or both edges (BE) at the same time. FE and RE are used for power topologies requiring duty cycle control(CMPA or CMPB high-resolution control), while BE is used for topologies requiring phase shifting, for example, phase shifted full bridge (TBPHS or TBPRD high-resolution control).

Control Mode — The MEP is programmed to be controlled either from the CMPAHR / CMPBHR register in case of duty cycle control or the TBPHSHR register (phase control). RE or FE control mode should be used with CMPAHR or CMPBHR register. BE control mode should be used with TBPHSHR register. When the MEP is controlled from the TBPRDHR register (period control) the duty cycle and phase can also be controlled via their respective high-resolution registers.

Shadow Mode — This mode provides the same shadowing (double buffering) option as in regular PWM mode. This option is valid only when operating from the CMPAHR, CMPBHR and TBPRDHR registers and should be chosen to be the same as the regular load option for the CMPA, CMPB register. If TBPHSHR is used, then this option has no effect.

High-Resolution B Signal Control — The B signal path of an ePWM channel can generate a high-resolution output by outputting an inverted version of the high-resolution ePWMxA signal on the ePWMxB pin. A Type 2 HRPWM module can also enable high-resolution features on the B signal path independently of the A signal path as well.

Swap ePWMxA and ePWMxB Outputs — This mode enables the swapping of the high resolution A & B outputs . The mode selection allows either A & B Outputs Unchanged or A Output Comes Out On B and B Output Comes Out On A

Auto-conversion Mode — This mode is used in conjunction with the scale factor optimization (SFO) software only. For a type 2 HRPWM module, below is a description of the Auto-conversion Mode taking CMPAHR as an example. If auto-conversion is enabled, $\text{CMPAHR} = \text{fraction}(\text{PWMduty} * \text{PWMperiod}) << 8$. The scale factor optimization software will calculate the MEP scale factor in background code and automatically update the HRMSTEP register with the calculated number of MEP steps per coarse step. The MEP Calibration Module will then use the values in the HRMSTEP and CMPAHR register to automatically calculate the appropriate number of MEP steps represented by the fractional duty cycle and move the high-resolution ePWM signal edge accordingly. If auto-conversion is disabled, the CMPAHR register behaves like a type 0 HRPWM module and $\text{CMPAHR} = (\text{fraction}(\text{PWMduty} * \text{PWMperiod}) * \text{MEP Scale Factor} + 0.5) << 8$. All calculations will need to be performed by user code in this mode, and the HRMSTEP register is ignored. Auto-conversion for high-resolution period has the same behavior as auto-conversion for high-resolution duty cycle. Auto-conversion must always be enabled for high-resolution period mode.

NOTE: Auto-conversion Mode performs the calculation for CMPBHR , DBREDHR and DBFEDHR as well. The scale factor optimization software will calculate the MEP scale factor in background code and automatically update the HRMSTEP register with the calculated number of MEP steps per coarse step. The MEP Calibration Module will then use the values in the HRMSTEP and CMPBHR or DBREDHR / DBFEDHR register to automatically calculate the appropriate number of MEP steps represented by the fractional components and move the high-resolution ePWM signal edge accordingly. If auto-conversion is disabled, CMPBHR behaves same as CMPAHR. $\text{CMPBHR} = (\text{fraction}(\text{PWMduty} * \text{PWMperiod}) * \text{MEP Scale Factor} + 0.5) << 8$.

13.2.3 Configuring Hi-Res in Deadband Rising Edge and Falling Edge Delay

Once the ePWM has been configured to provide conventional PWM of a given frequency, polarity and deadband enabled in half cycle clocking mode, the high resolution operation on dead band RED and FED lines are enabled by programming the HRCNFG2 register in that particular ePWM module's register space. This register provides the following configuration options:

Edge Mode — The MEP can be programmed to provide precise position control on the dead band rising edge (RED), dead band falling edge (FED) or both edges (rising edge of DBRED signal and falling edge of DBFED signal) at the same time.

Control Mode — Selects the time event that loads the shadow value in active register for DBRED and DBFED in high resolution mode. The user needs to select the pulse to match the selection in the ePWM DBCTL[LOADREDMODE] & DBCTL[LOADFEDMODE] bits .

13.2.4 Principle of Operation

The MEP logic is capable of placing an edge in one of 255 (8 bits) discrete time steps (see device-specific data sheet for typical MEP step size). The MEP works with the TBM and CCM registers to be certain that time steps are optimally applied and that edge placement accuracy is maintained over a wide range of PWM frequencies, system clock frequencies and other operating conditions. Table 13-2 shows the typical range of operating frequencies supported by the HRPWM.

Table 13-2. Relationship Between MEP Steps, PWM Frequency and Resolution

System (MHz)	MEP Steps Per SYSCLKOUT ⁽¹⁾⁽²⁾⁽³⁾	PWM MIN (Hz) ⁽⁴⁾	PWM MAX (MHz)	Res. @ MAX (Bits) ⁽⁵⁾
50.0	111	763	2.50	11.1
60.0	93	916	3.00	10.9
70.0	79	1068	3.50	10.6
80.0	69	1221	4.00	10.4
90.0	62	1373	4.50	10.3
100.0	56	1526	5.00	10.1

⁽¹⁾ System frequency = SYSCLKOUT, that is, CPU clock. TBCLK = SYSCLKOUT.

⁽²⁾ Table data based on a MEP time resolution of 180 ps (this is an example value. See the device-specific data sheet for MEP limits)

⁽³⁾ MEP steps applied = $T_{SYSCLKOUT}/180$ ps in this example.

⁽⁴⁾ PWM minimum frequency is based on a maximum period value,(TBPRD = 65535). PWM mode is asymmetrical up-count.

⁽⁵⁾ Resolution in bits is given for the maximum PWM frequency stated.

13.2.4.1 Edge Positioning

NOTE: The below example is presented using [CMPA:CMPAHR] register combination. The theory of operation and equations is same if the user intends to use [CMPBM:CMPBHRM] for duty cycle control.

In a typical power control loop, a digital controller issues a duty command, usually expressed in a per unit or percentage terms. Assume that for a particular operating point, the demanded duty cycle is 0.405 or 40.5% on time and the required converter PWM frequency is 1.25 MHz. In conventional PWM generation with a system clock of 100 MHz, the duty cycle choices are in the vicinity of 40.5%. As shown in [Figure 13-6](#), a compare value of 32 counts (duty = 40%) is the closest to 40.5% that can be attained. This is equivalent to an edge position of 320 ns instead of the desired 324 ns. This data is shown in [Table 13-3](#).

By utilizing the MEP, you can achieve an edge position much closer to the desired point of 324 ns. [Table 13-3](#) shows that in addition to the CMPA value, 22 steps of the MEP (CMPAHR register) will position the edge at 323.96 ns, resulting in almost zero error. In this example, it is assumed that the MEP has a step resolution of 180 ps.

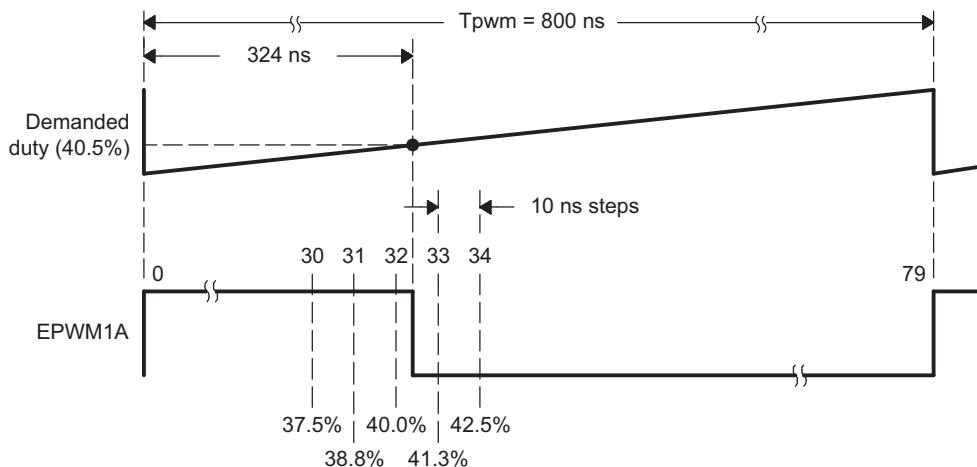
Figure 13-6. Required PWM Waveform for a Requested Duty = 40.5%

Table 13-3. CMPA vs Duty (left), and [CMPA:CMPAHR] vs Duty (right)

CMPA (count) ⁽¹⁾ ⁽²⁾ ⁽³⁾	DUTY %	High Time (ns)	CMPA (count)	CMPAHR (count)	Duty (%)	High Time (ns)
28	35.0	280	32	18	40.405	323.24
29	36.3	290	32	19	40.428	323.42
30	37.5	300	32	20	40.450	323.60
31	38.8	310	32	21	40.473	323.78
32	40.0	320	32	22	40.495	323.96
33	41.3	330	32	23	40.518	324.14
34	42.5	340	32	24	40.540	324.32
			32	25	40.563	324.50
Required			32	26	40.585	324.68
32.40	40.5	324	32	27	40.608	324.86

⁽¹⁾ System clock, SYSCLKOUT and TBCLK = 100 MHz, 10 ns

⁽²⁾ For a PWM Period register value of 80 counts, PWM Period = $80 \times 10 \text{ ns} = 800 \text{ ns}$, PWM frequency = $1/800 \text{ ns} = 1.25 \text{ MHz}$

⁽³⁾ Assumed MEP step size for the above example = 180 ps
See the device-specific data manual for typical and maximum MEP values.

13.2.4.2 Scaling Considerations

The mechanics of how to position an edge precisely in time has been demonstrated using the resources of the standard CMPA and MEP (CMPAHR) registers. In a practical application, however, it is necessary to seamlessly provide the CPU a mapping function from a per-unit (fractional) duty cycle to a final integer (non-fractional) representation that is written to the [CMPA:CMPAHR] register combination.

To do this, first examine the scaling or mapping steps involved. It is common in control software to express duty cycle in a per-unit or percentage basis. This has the advantage of performing all needed math calculations without concern for the final absolute duty cycle, expressed in clock counts or high time in ns. Furthermore, it makes the code more transportable across multiple converter types running different PWM frequencies.

To implement the mapping scheme, a two-step scaling procedure is required.

Assumptions for this example:

SYCLK, SYCLKOUT	= 10 ns (100 MHz)
PWM frequency	= 1.25 MHz (1/800 ns)
Required PWM duty cycle, PWMDuty	= 0.405 (40.5%)
PWM period in terms of coarse steps, PWMPeriod (800 ns/10 ns)	= 80
Number of MEP steps per coarse step at 180 ps (10 n/180 ps), MEP_ScaleFactor	= 55
Value to keep CMPAHR within the range of 1-255 and fractional rounding constant (default value)	= 0.5 (0080h in Q8 format)

Step 1: Percentage Integer Duty value conversion for CMPA register

CMPA register value	= int(PWMDuty * PWMPeriod); int means integer part
	= int(0.405 * 80)
	= int(32.4)
CMPA register value	= 32 (20h)

Step 2: Fractional value conversion for CMPAHR register

CMPAHR	= (frac(PWMDuty * PWMPeriod)* MEP_ScaleFactor +0.5) << 8); frac means fractional part
	= (frac(32.4) * 55 + 0.5) << 8; Shifting is to move the value to the high byte of CMPAHR.
	= (0.4 * 55 + 0.5) << 8
	= (22 + 0.5) << 8
	= 22.5 * 256; Shifting left by 8 is the same as multiplying by 256.
	= 5760 (1680h)
CMPAHR	= 1680h CMPAHR value = 1600h (lower 8 bits will be ignored by hardware).

NOTE: If the AUTOCONV bit (HRCNFG.6) is set and the MEP_ScaleFactor is in the HRMSTEP register, then CMPAHR / CMPBHR register value = frac (PWMDuty*PWMperiod<<8). The rest of the conversion calculations are performed automatically in hardware, and the correct MEP-scaled signal edge appears on the ePWM channel output. If AUTOCONV is not set, the above calculations must be performed by software.

NOTE: The MEP scale factor (MEP_ScaleFactor) varies with the system clock and DSP operating conditions. TI provides an MEP scale factor optimizing (SFO) software C function, which uses the built in diagnostics in each HRPWM and returns the best scale factor for a given operating point.

The scale factor varies slowly over a limited range so the optimizing C function can be run very slowly in a background loop.

The CMPA, CMPB, CMPAHR and CMPBHR registers are configured in memory so that the 32-bit data capability of the 28x CPU can write this as a single concatenated value, that is, [CMPA:CMPAHR] , [CMPB:CMPBHR], and so on.

The mapping scheme has been implemented in both C and assembly, as shown in [Section 13.2.7](#). The actual implementation takes advantage of the 32-bit CPU architecture of the 28xx, and is somewhat different from the steps shown in [Section 13.2.4.2](#).

For time critical control loops where every cycle counts, the assembly version is recommended. This is a cycle optimized function (11 SYSCLKOUT cycles) that takes a Q15 duty value as input and writes a single [CMPA:CMPAHR] value.

13.2.4.3 Duty Cycle Range Limitation

In high resolution mode, the MEP is not active for 100% of the PWM period. It becomes operational:

- Three SYSCLK cycles after the period starts when high-resolution period (TBPRDHR) control is not enabled.
- When high resolution period (TBPRDHR) control is enabled via the HRPCTL register:
 - In up-count mode: 3 SYSCLK cycles after the period starts until 3 SYSCLK cycles before the period ends.
 - In up-down count mode: when counting up, 3 cycles after CTR = 0 until 3 cycles before CTR = PRD, and when counting down, 3 cycles after CTR = PRD until 3 cycles before CTR = 0.

Duty cycle range limitations are illustrated in [Figure 13-7](#) to [Figure 13-10](#). This limitation imposes a duty cycle limit on the MEP. For example, precision edge control is not available all the way down to 0% duty cycle. When high-resolution period control is disabled, regular PWM duty control is fully operational down to 0% duty cycle despite the unavailability of HRPWM features in the first three cycles. In most applications this should not be an issue as the controller regulation point is usually not designed to be close to 0% duty cycle. To better understand the useable duty cycle range, see [Table 13-4](#). When high-resolution period control is enabled (HRPCTL[HRPE]=1), the duty cycle must not fall within the restricted range. Otherwise, there may be undefined behavior on the ePWMxA output.

Figure 13-7. Low % Duty Cycle Range Limitation Example (HRPCTL[HRPE] = 0)

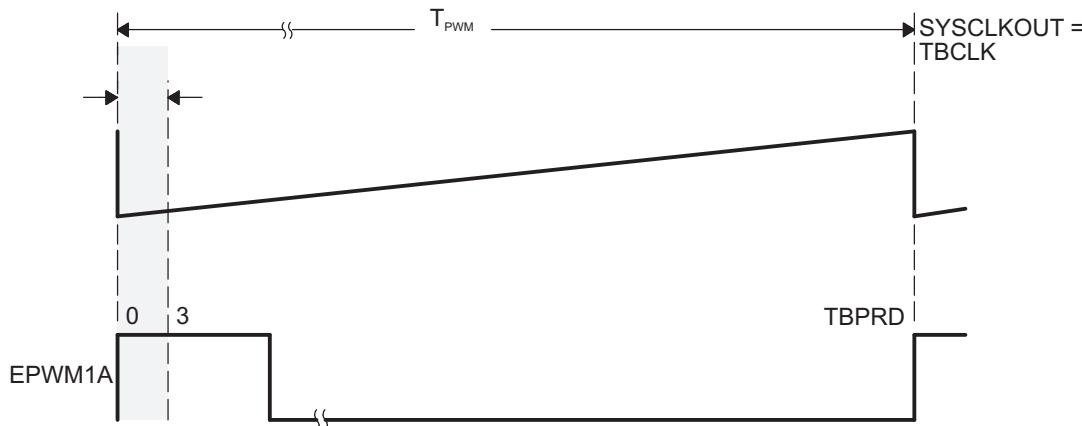


Table 13-4. Duty Cycle Range Limitation for 3 SYSCLK/TBCLK Cycles

PWM Frequency ⁽¹⁾ (kHz)	3 Cycles Minimum Duty	3 Cycles Maximum Duty ⁽²⁾
200	0.6%	99.4%
400	1.2%	98.8%
600	1.8%	98.2%
800	2.4%	97.6%
1000	3%	97%
1200	3.6%	96.4%
1400	4.2%	95.8%
1600	4.8%	95.2%
1800	5.4%	94.6%
2000	6%	94%

⁽¹⁾ System clock - $T_{SYSCLKOUT} = 10 \text{ ns}$ System clock = TBCLK = 100 MHz

⁽²⁾ This limitation applies only if high-resolution period (TBPRDHR) control is enabled.

If the application demands HRPWM operation below the minimum duty cycle limitation, then the HRPWM can be configured to operate in count-down mode with the rising edge position (REP) controlled by the MEP when high-resolution period is disabled (HRPCTL[HRPE] = 0). This is illustrated in [Figure 13-8](#). In this configuration, the minimum duty cycle limitation is no longer an issue. However, there will be a maximum duty limitation with same percent numbers as given in [Table 13-4](#).

Figure 13-8. High % Duty Cycle Range Limitation Example (HRPCTL[HRPE] = 0)

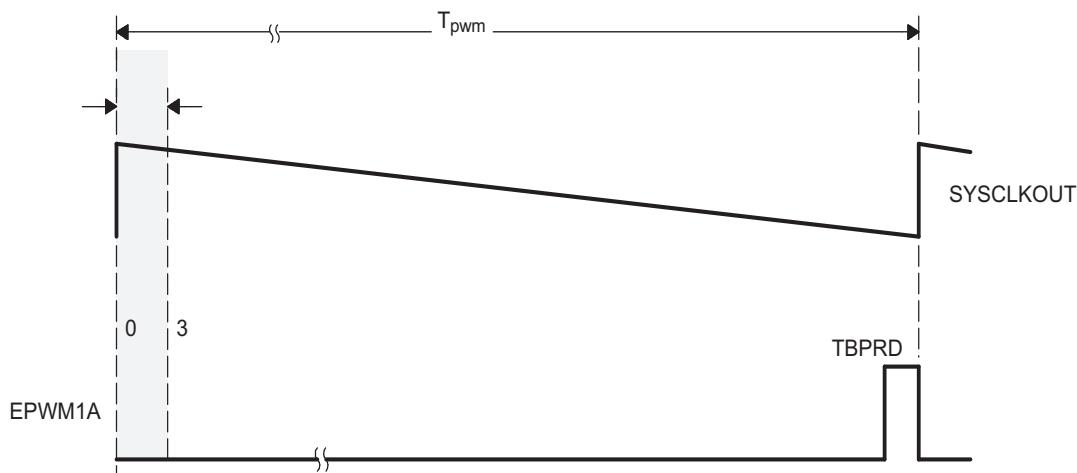


Figure 13-9. Up-Count Duty Cycle Range Limitation Example (HRPCTL[HRPE]=1)

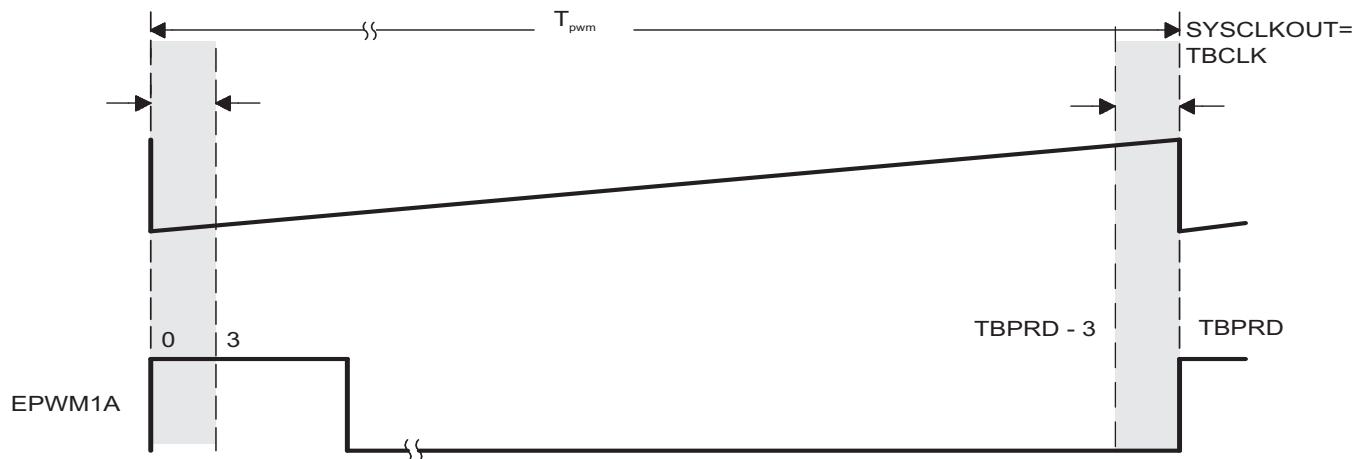
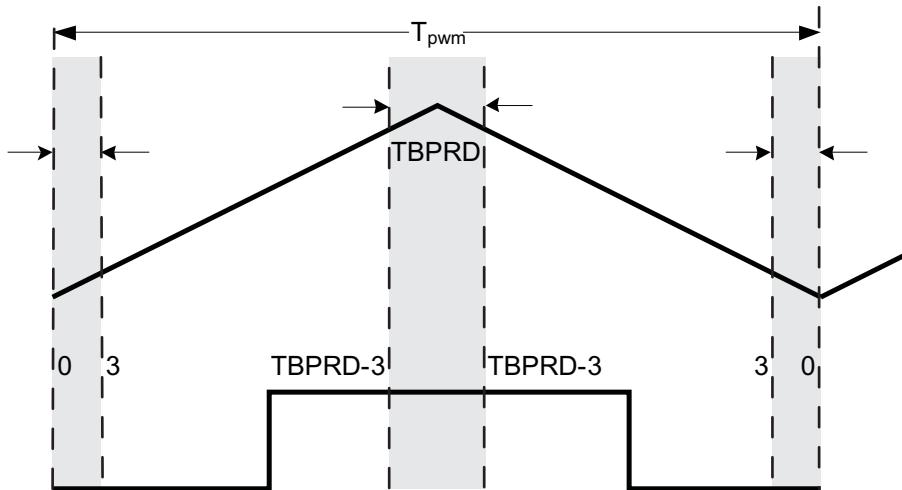


Figure 13-10. Up-Down Count Duty Cycle Range Limitation Example (HRPCTL[HRPE]=1)

NOTE: If the application has enabled high-resolution period control (HRPCTL[HRPE]=1), the duty cycle must not fall within the restricted range. Otherwise, there will be undefined behavior on the ePWM output.

13.2.4.4 High Resolution Period

High resolution period control using the MEP logic is supported on devices with a Type 1 ePWM module or greater.

NOTE: When high-resolution period control is enabled, on ePWMxA only, and not ePWMxB output and vice versa, the non hi-res output will have +/- 1 TBCLK cycle jitter in up-count mode and +/- 2 TBCLK cycle jitter in up-down count mode.

The scaling procedure described for duty cycle in [Section 13.2.4.2](#) applies for high-resolution period as well:

Assumptions for this example:

System clock , SYSCLKOUT	= 10 ns (100 MHz)
Required PWM frequency	= 175 kHz (period of 571.428)
Number of MEP steps per coarse step at 180 ps (MEP_ScaleFactor)	= 55 (10 ns / 180 ps)
Value to keep TBPRDHR within range of 1-255 and fractional rounding constant (default value)	= 0.5 (0080h in Q8 format)

Problem:

In up-count mode:

If TBPRD = 571, then PWM frequency = 174.82 kHz (period = $(571+1) * T_{TBCLK}$).

If TBPRD = 570, then PWM frequency = 175.13 kHz (period = $(570+1) * T_{TBCLK}$).

In up-down count mode:

If TBPRD = 286, then PWM frequency = 174.82 kHz (period = $(286*2) * T_{TBCLK}$).

If TBPRD = 285, then PWM frequency = 175.44 kHz (period = $(285*2) * T_{TBCLK}$).

Solution:

With 55 MEP steps per coarse step at 180 ps each:

Step 1: Percentage Integer Period value conversion for TBPRD register

Integer period value	= $571 * T_{TBCLK}$
	= int(571.428) * T_{TBCLK}
	= int(PWMperiod) * T_{TBCLK}

In up-count mode:

TBPRD	= 570 (TBPRD = period value - 1)
	= 023Ah

In up-down count mode:

TBPRD	= 285 (TBPRD = period value / 2)
	= 011Dh

Step 2: Fractional value conversion for TBPRDHR register

TBPRDHR register value	= $(\text{frac}(\text{PWMperiod}) * \text{MEP_ScaleFactor} + 0.5)$
If auto-conversion enabled and HRMSTEP = MEP_ScaleFactor value (55):	= $\text{frac}(\text{PWMperiod}) << 8$ (Shifting is to move the value to the high byte of TBPRDHR)
TBPRDHR register value	= $\text{frac}(571.428) << 8$ = 0.428×256 = 6D00h

The autoconversion will then automatically perform the calculation such that TBPRDHR MEP delay is scaled by hardware to:

$$\begin{aligned}
 &= ((TBPRDHR(15:0) \gg 8) \times HRMSTEP + 80h) \ll 8 \\
 &= (006Dh \times 55 + 80h) \gg 8 \\
 &= (17EBh) \gg 8 \\
 &= 0017h \text{ MEP Steps}
 \end{aligned}$$

Period MEP delay

13.2.4.4.1 High-Resolution Period Configuration

To use High Resolution Period, the ePWMx module must be initialized in the exact order presented.

The steps below use CMPA with shadow registers and the corresponding HRCNFG bits for hi-resolution operation on EPWMxA. For hi-resolution operation on EPWMxB, make the appropriate substitutions with the B channel fields.

1. Enable ePWMx clock
2. Enable HRPWM clock
3. Disable TBCLKSYNC
4. Configure ePWMx registers - AQ, TBPRD, CC, and so on.
 - ePWMx may only be configured for up-count or up-down count modes. High-resolution period is not compatible with down-count mode.
 - TBPRD and CC registers must be configured for shadow loads.
 - CMPCTL[LOADAMODE]
 - In up-count mode: CMPCTL[LOADAMODE] = 1 (load on CTR = PRD)
 - In up-down count mode: CMPCTL[LOADAMODE] = 2 (load on CTR=0 or CTR=PRD)
5. Configure the HRCNFG register such that:
 - HRCNFG[HRLOAD] = 2 (load on either CTR = 0 or CTR = PRD)
 - HRCNFG[AUTOCONV] = 1 (Enable auto-conversion)
 - HRCNFG[EDGEMODE] = 3 (MEP control on both edges)
6. For TBPHS:TBPHSHR synchronization with high-resolution period, set both HRPCTL[TBPSHRLLOADE] = 1 and TBCTL[PHSEN] = 1. In up-down count mode these bits must be set to 1 regardless of the contents of TBPHSHR.
7. Enable high-resolution period control (HRPCTL[HRPE] = 1)
8. Enable TBCLKSYNC
9. TBCTL[SWFSYNC] = 1
10. HRMSTEP must contain an accurate MEP scale factor (# of MEP steps per SYSCLKOUT coarse step) because auto-conversion is enabled. The MEP scale factor can be acquired via the SFO() function described in [Section 13.3](#).
11. To control high-resolution period, write to the TBPRDHR(M) registers.

NOTE: When high-resolution period mode is enabled, an EPWMxSYNC pulse will introduce +/- 1 - 2 cycle jitter to the PWM (+/- 1 cycle in up-count mode and +/- 2 cycle in up-down count mode). For this reason, TBCTL[SYNCOSEL] should not be set to 1 (CTR = 0 is EPWMxSYNCO source) or 2 (CTR = CMPB is EPWMxSYNCO source). Otherwise, the jitter will occur on every PWM cycle with the synchronization pulse.

When TBCTL[SYNCOSEL] = 0 (EPWMxSYNCI is EPWMxSYNCO source), a software synchronization pulse should be issued only once during high-resolution period initialization. If a software sync pulse is applied while the PWM is running, the jitter will appear on the PWM output at the time of the sync pulse.

13.2.5 Deadband High Resolution Operation

Assumptions for this example:

System clock	= 10 ns (100 MHz) &
Deadband Enabled in half cycle mode, TBCLK =	SYSCLK
Required PWM frequency	1.33MHz (1 / 750 ns)
Required PWM duty cycle	0.5 (50%)
Required Dead band Rising Edge Delay	5% over duty
Required Dead band Rising Edge Delay in ns	(0.05 * 375 ns) = 18.75 ns

Dead-Band Delay Values as a Function of DBFED and DBRED:

When half-cycle clocking is enabled, the formula to calculate the falling-edge-delay and rising-edge-delay becomes:

$$FED = DBFED * TBCLK / 2$$

$$RED = DBRED * TBCLK / 2$$

DBRED and DBFED Calculated Values:

Required Dead band Rising Edge Delay in ns = 18.75 ns

$$DBRED = RED / (TBCLK / 2)$$

$$DBRED = 18.75 \text{ ns} / 5 \text{ ns}$$

$$DBRED \text{ Required} = 3.75 \text{ ns}$$

With 55 MEP steps per coarse step at 180 ps each:

Step 1: Integer Dead band value conversion for DBREDM register

Integer DBRED value	= int (RED / (TBCLK / 2))
DBRED	= int (3.75)

$$= 3$$

Step 2: Fractional value conversion for Dead band high resolution register DBREDHR

DBREDHR register value	= (frac(DBRED Required) * MEP_ScaleFactor + 0.5) << 8 (Shifting is to move the value to the high byte of DBREDHR)
	= (frac (3.75) * 55 + 0.5) << 8
	= (0.75 * 55 + 0.5) << 8
	= (41.75) * 256 Shifting left by 8 is the same as multiplying by 256.
DBREDHR value	= 29C0h MEP Steps
	Hardware will ignore lower 9 bits in the above calculated DBREDHR value

NOTE: If the AUTOCONV bit (HRCNFG.6) is set and the MEP_ScaleFactor is in the HRMSTEP register, then DBREDHR:DBRED = frac((required DB value) <<8). The rest of the conversion calculations are performed automatically in hardware, and the correct MEP-scaled signal edge appears on the ePWM channel output. If AUTOCONV is not set, the above calculations must be performed by software.

13.2.6 Scale Factor Optimizing Software (SFO)

The micro edge positioner (MEP) logic is capable of placing an edge in one of 255 discrete time steps. As previously mentioned, the size of these steps is on the order of 150 ps (see device-specific data sheet for typical MEP step size on your device). The MEP step size varies based on worst-case process parameters, operating temperature, and voltage. MEP step size increases with decreasing voltage and increasing temperature and decreases with increasing voltage and decreasing temperature. Applications that use the HRPWM feature should use the TI-supplied MEP scale factor optimization (SFO) software function. The SFO function helps to dynamically determine the number of MEP steps per SYSCLKOUT period while the HRPWM is in operation.

To utilize the MEP capabilities effectively, the correct value for the MEP scaling factor needs to be known by the software. To accomplish this, the HRPWM module has built in self-check and diagnostic capabilities that can be used to determine the optimum MEP scale factor value for any operating condition. TI provides a C-callable library containing one SFO function that utilizes this hardware and determines the optimum MEP scale factor. As such, MEP control and diagnostics registers are reserved for TI use.

A detailed description of the SFO library - SFO_TI_Build_V7.lib software can be found in [Section 13.3](#).

13.2.7 HRPWM Examples Using Optimized Assembly Code.

The best way to understand how to use the HRPWM capabilities is through two real examples:

1. Simple buck converter using asymmetrical PWM (count-up) with active high polarity.
2. DAC function using simple R+C reconstruction filter.

The following examples all have initialization and configuration code written in C. To make these easier to understand, the #defines shown below are used. Note, #defines introduced in the device-specific *Pulse Width Modulator (ePWM) Module Reference Guide* are also used.

Example 13-1 This example assumes MEP step size of 150 ps and does not use the SFO library.

Example 13-1. #Defines for HRPWM Header Files

```
// HRPWM (High Resolution PWM) //
=====
// HRCNFG
#define HR_Disable 0x0
#define HR REP 0x1      // Rising Edge position
#define HR FEP 0x2      // Falling Edge position
#define HR BEP 0x3      // Both Edge position #define HR CMP 0x0 // CMPAHR controlled
#define HR PHS 0x1      // TBPHSHR controlled #define HR CTR_ZERO 0x0 // CTR = Zero event
#define HR CTR_PRD 0x1   // CTR = Period event
#define HR CTR_ZERO_PRD 0x2 // CTR = ZERO or Period event
#define HR_NORM_B 0x0     // Normal ePWMxB output
#define HR_INVERT_B 0x1   // ePWMxB is inverted ePWMxA output
```

13.2.7.1 Implementing a Simple Buck Converter

In this example, the PWM requirements are:

- PWM frequency = 1 MHz (that is, TBPRD = 100)
- PWM mode = asymmetrical, up-count
- Resolution = 12.7 bits (with a MEP step size of 150 ps)

Figure 13-11 and Figure 13-12 show the required PWM waveform. As explained previously, configuration for the ePWM1 module is almost identical to the normal case except that the appropriate MEP options need to be enabled/selected.

Figure 13-11. Simple Buck Controlled Converter Using a Single PWM

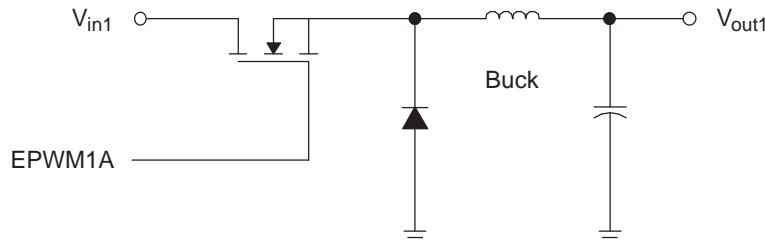
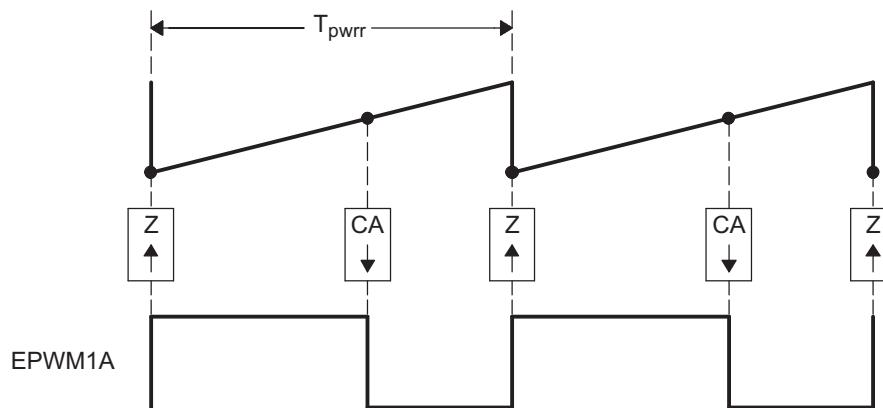


Figure 13-12. PWM Waveform Generated for Simple Buck Controlled Converter



The example code shown consists of two main parts:

- Initialization code (executed once)
- Run time code (typically executed within an ISR)

[Example 13-2](#) shows the Initialization code. The first part is configured for conventional PWM. The second part sets up the HRPWM resources.

This example assumes MEP step size of 150 ps and does not use the SFO library.

Example 13-2. HRPWM Buck Converter Initialization Code

```
void HrBuckDrvCnf(void)
{
// Config for conventional PWM first
EPwm1Regs.TBCTL.bit.PRDLD = TB_IMMEDIATE;           // set Immediate load
EPwm1Regs.TBPRD = 100;                                // Period set for 1000 kHz PWM
hrbuck_period = 200;                                  // Used for Q15 to Q0 scaling
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;                // EPWM1 is the Master
EPwm1Regs.TBCTL.bit.SYNCSEL = TB_SYNC_DISABLE;
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
// Note: ChB is initialized here only for comparison purposes, it is not required

EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;          // optional
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;            // optional

EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm1Regs.AQCTLB.bit.ZRO = AQ_SET;                     // optional
EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;                  // optional
// Now configure the HRPWM resources
EALLOW;                                                 // Note these registers are protected
// and act only on ChA
// clear all bits first
EPwm1Regs.HRCNFG.all = 0x0;                            // clear all bits first
EPwm1Regs.HRCNFG.bit.EDGMODE = HR_FEP;                 // Control Falling Edge Position
EPwm1Regs.HRCNFG.bit.CTLMODE = HR_CMP;                  // CMPAHR controls the MEP
EPwm1Regs.HRCNFG.bit.HRLOAD = HR_CTR_ZERO;              // Shadow load on CTR=Zero
EDIS;
MEP_ScaleFactor = 66*256;                             // Start with typical Scale Factor
// value for 100 MHz
// Note: Use SFO functions to update
// MEP_ScaleFactor dynamically
}
```

[Example 13-3](#) shows an assembly example of run-time code for the HRPWM buck converter.

Example 13-3. HRPWM Buck Converter Run-Time Code

```

EPWM1_BASE .set 0x6800
CMPAHR1 .set EPWM1_BASE+0x8
;=====
;=====HRBUCK_DRV; (can execute within an ISR or loop)
;=====

    MOVW DP, #_HRBUCK_In
    MOVL XAR2,@_HRBUCK_In      ; Pointer to Input Q15 Duty (XAR2)
    MOVL XAR3,#CMPAHR1         ; Pointer to HRPWM CMPA reg (XAR3)

; Output for EPWM1A (HRPWM)
    MOV T,*XAR2 ; T <= Duty
    MPYU ACC,T,@_hrbuck_period ; Q15 to Q0 scaling based on Period
    MOV T,@_MEP_ScaleFactor     ; MEP scale factor (from optimizer s/w)
    MPYU P,T,@AL                ; P <= T * AL, Optimizer scaling
    MOVH @AL,P                  ; AL <= P, move result back to ACC
    ADD ACC, #0x080              ; MEP range and rounding adjustment
    MOVL *XAR3,ACC              ; CMPA:CMPAHR(31:8) <= ACC
; Output for EPWM1B (Regular Res) Optional - for comparison purpose only
    MOV *+XAR3[2],AH            ; Store ACCH to regular CMPB

```

13.2.7.2 Implementing a DAC function Using an R+C Reconstruction Filter

In this example, the PWM requirements are:

- PWM frequency = 400 kHz (that is, TBPRD = 250)
- PWM mode = Asymmetrical, Up-count
- Resolution = 14 bits (MEP step size = 150 ps)

Figure 13-13 and Figure 13-14 show the DAC function and the required PWM waveform. As explained previously, configuration for the ePWM1 module is almost identical to the normal case except that the appropriate MEP options need to be enabled/selected.

Figure 13-13. Simple Reconstruction Filter for a PWM Based DAC

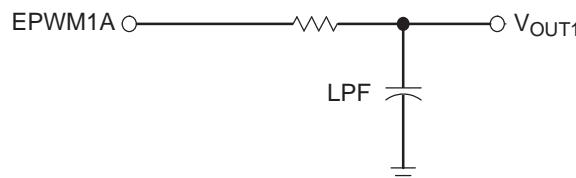
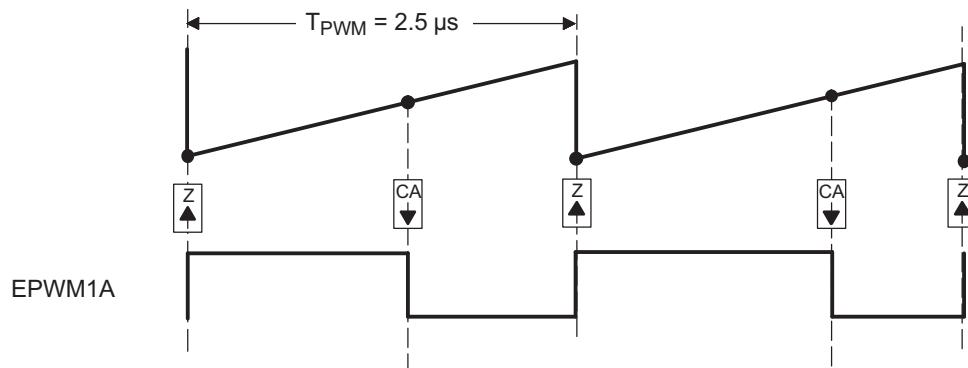


Figure 13-14. PWM Waveform Generated for the PWM DAC Function



The example code shown consists of two main parts:

- Initialization code (executed once)
- Run time code (typically executed within an ISR)

This example assumes a typical MEP_SP and does not use the SFO library.

[Example 13-4](#) shows the Initialization code. The first part is configured for conventional PWM. The second part sets up the HRPWM resources.

Example 13-4. PWM DAC Function Initialization Code

```
void HrPwmDacDrvCnf(void)
{
// Config for conventional PWM first
EPwm1Regs.TBCTL.bit.PRDLD = TB_IMMEDIATE;           // Set Immediate load
EPwm1Regs.TBPRD = 250;                                // Period set for 400 kHz PWM
hrDAC_period = 250;                                    // Used for Q15 to Q0 scaling
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;                // EPWM1 is the Master
EPwm1Regs.TBCTL.bit.SYNCSEL = TB_SYNC_DISABLE;
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
// Note: ChB is initialized here only for comparison purposes, it is not required

EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // optional
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW; // optional

EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm1Regs.AQCTLB.bit.ZRO = AQ_SET;                    // optional
EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;                  // optional
// Now configure the HRPWM resources
EALLOW;                                              // Note these registers are protected
// and act only on ChA.
EPwm1Regs.HRCNFG.all = 0x0; // Clear all bits first
EPwm1Regs.HRCNFG.bit.EDGMODE = HR_FEP;               // Control falling edge position
EPwm1Regs.HRCNFG.bit.CTLMODE = HR_CMP;                // CMPAHR controls the MEP.
EPwm1Regs.HRCNFG.bit.HRLOAD = HR_CTR_ZERO;            // Shadow load on CTR=Zero.
EDIS;
MEP_ScaleFactor = 66*256;                            // Start with typical Scale Factor
// value for 100 MHz.
// Use SFO functions to update MEP_ScaleFactor
// dynamically.
}
```

[Example 13-5](#) shows an assembly example of run-time code that can execute in a high-speed ISR loop.

Example 13-5. PWM DAC Function Run-Time Code

```

EPWM1_BASE .set 0x6800
CMPAHRL .set EPWM1_BASE+0x8
;=====
;===== HRPWM_DAC_DRV; (can execute within an ISR or loop)
;=====

    MOVW DP, #_HRDAC_In
    MOVL XAR2,@_HRDAC_In           ; Pointer to input Q15 duty (XAR2)
    MOVL XAR3,#CMPAHRL            ; Pointer to HRPWM CMPA reg (XAR3)

; Output for EPWM1A (HRPWM
    MOV T,*XAR2                  ; T <= duty
    MPY ACC,T,@_hrDAC_period      ; Q15 to Q0 scaling based on period
    ADD ACC,@_HrDAC_period<<15 ; Offset for bipolar operation
    MOV T,@_MEP_ScaleFactor       ; MEP scale factor (from optimizer s/w)
    MPYU P,T,@AL                  ; P <= T * AL, optimizer scaling
    MOVH @AL,P                    ; AL <= P, move result back to ACC
    ADD ACC, #0x080                ; MEP range and rounding adjustment
    MOVL *XAR3,ACC                ; CMPA:CMPAHRL(31:8) <= ACC

; Output for EPWM1B (Regular Res) Optional - for comparison purpose only
    MOV *+XAR3[2],AH              ; Store ACCH to regular CMPB

```

13.3 Appendix A: SFO Library Software - SFO_TI_Build_V7.lib

The following table lists several features of the SFO_TI_Build_V7.lib library.

Table 13-5. SFO Library Features

	SFO_TI_Build_V7.lib	Unit
Completion-checking?	Yes	Function return value
Typical cycles required for SFO() to update MEP_ScaleFactor if called repetitively without interrupts	130,000	SYCLK cycles

A functional description of the SFO library routine, SFO(), is found below.

13.3.1 Scale Factor Optimizer Function - int SFO()

This routine drives the micro-edge positioner (MEP) calibration module to run SFO diagnostics and determine the appropriate MEP scale factor (number of MEP steps per coarse SYCLKOUT step) for a device at any given time.

If SYCLKOUT = TBCLK = 100 MHz and assuming the MEP step size is 150 ps, the typical scale factor value at 100 MHz = 66 MEP steps per TBCLK unit (10 ns)

The function returns a MEP scale factor value:

MEP_ScaleFactor = Number of MEP steps/SYCLKOUT.

Constraints when using this function:

- SFO() can be used with a minimum SYCLKOUT = TBCLK = 50 MHz. MEP diagnostics logic uses SYCLKOUT and not TBCLK, so the SYCLKOUT restriction is an important constraint. Below 50 MHz, with device process variation, the MEP step size may decrease under cold temperature and high core voltage conditions to such a point, that 255 MEP steps will not span an entire SYCLKOUT cycle.
- At any time, SFO() can be called to run SFO diagnostics on the MEP calibration module

Usage:

- SFO() can be called at any time in the background while the ePWM channels are running in HRPWM mode. The scale factor result obtained can be applied to all ePWM channels running in HRPWM mode because the function makes use of the diagnostics logic in the MEP calibration module (which runs independently of ePWM channels).
- This routine returns a 1 when calibration is finished and a new scale factor has been calculated, or a 0 if calibration is still running. The routine returns a 2 if there is an error, and the MEP_ScaleFactor is greater than the maximum 255 fine steps per coarse SYCLKOUT cycle. In this case, the HRMSTEP register will maintain the last MEP scale factor value less than 256 for auto conversion.
- All ePWM modules operating in HRPWM incur only a 3-SYCLKOUT cycle minimum duty cycle limitation when high-resolution period control is not used. If high-resolution period control is enabled, there is an additional duty cycle limitation 3-SYCLKOUT cycles before the end of the PWM period (see [Section 13.2.4.3](#)).
- The SFO() function also updates the HRMSTEP register with the scale factor result. If the HRCNFG[AUTOCONV] bit is set, the application software is responsible only for setting CMPAHR = fraction(PWMDuty*PWMperiod) << 8 or CMPBHR = fraction(PWMDuty*PWMperiod) << 8 or TBPRDHR = fraction (PWMperiod) while running SFO() in the background. The MEP Calibration Module will then use the values in the HRMSTEP and CMPAHR/CMPBHR/TBPRDHR register to automatically calculate the appropriate number of MEP steps represented by the fractional duty cycle or period and move the high-resolution ePWM signal edge accordingly.
- If the HRCNFG[AUTOCONV] bit is clear, the HRMSTEP register is ignored. The application software will need to perform the necessary calculations manually so that:
 - CMPAHR = (fraction(PWMDuty * PWMperiod) * MEP Scale Factor) << 8 + 0x080.
 - Similar behavior applies for TBPHSHR, CMPBHR, DBREDHR, DBFEDHR. Auto-conversion must be enabled when using TBPRDHR.

The routine can be run as a background task in a slow loop requiring negligible CPU cycles. The repetition rate at which an SFO function needs to be executed depends on the application's operating environment. As with all digital CMOS devices, temperature and supply voltage variations have an effect on MEP operation. However, in most applications these parameters vary slowly and therefore it is often sufficient to execute the SFO function once every 5 to 10 seconds. If more rapid variations are expected, then execution may have to be performed more frequently to match the application. Note, there is no high limit restriction on the SFO function repetition rate, hence it can execute as quickly as the background loop is capable.

While using the HRPWM feature, HRPWM logic will not be active for the first three SYSCLKOUT cycles of the PWM period (and the last three SYSCLKOUT cycles of the PWM period if TBPRDHR is used). While running the application in this configuration, if high-resolution period control is disabled (HRPCTL[HRPE=0]) and the CMPA/CMPB register value is less than three cycles, then its CMPAHR/CMPBHR register must be cleared to zero. If high-resolution period control is enabled (HRPCTL[HRPE=1]), the CMPA register value must not fall below 3 or above TBPRD-3. This would avoid any unexpected transitions on the PWM signal.

13.3.2 Software Usage

The software library function SFO(), calculates the MEP scale factor for the HRPWM-supported ePWM modules. The scale factor is an integer value in the range 1-255, and represents the number of micro step edge positions available for a system clock period. The scale factor value is returned in an integer variable called MEP_ScaleFactor. For example, see [Table 13-6](#).

Table 13-6. Factor Values

Software Function call	Functional Description	Updated Variables
SFO()	Returns MEP scale factor in the HRMSTEP register	MEP_ScaleFactor & HRMSTEP register.

To use the HRPWM feature of the ePWMs, it is recommended that the SFO function be used as described here.

Step 1. Add "Include" Files

The SFO_V7.h file needs to be included as follows. This include file is mandatory while using the SFO library function. For the SFO() to operate, the appropriate (Device)_Device.h and (Device)_Epwm_defines.h must be included in the project. These include files are optional if customized header files are used in the end applications.

Example 13-6. A Sample of How to Add "Include" Files

```
#include "F28M35x_Device.h"      // F28M35x Headerfile
#include "F28M35x_EPwm_defines.h" // init defines
#include "SFO_V7.h"              // SFO lib functions (needed for HRPWM)
```

Step 2. Element Declaration

Declare an integer variable for the scale factor value as shown below.

Example 13-7. Declaring an Element

```
int MEP_ScaleFactor = 0; //scale factor value
volatile struct EPWM_REGS *ePWM[] = {0, &EPwm1Regs, &EPwm2Regs, &EPwm3Regs,
&EPwm4Regs};
```

Step 3. MEP_ScaleFactor Initialization

The SFO() function does not require a starting scale factor value in MEP_ScaleFactor. Prior to using the MEP_ScaleFactor variable in application code, SFO() should be called to drive the MEP calibration module to calculate an MEP_ScaleFactor value.

As part of the one-time initialization code prior to using MEP_ScaleFactor, include the following:

Example 13-8. Initializing With a Scale Factor Value

```
MEP_ScaleFactor initialized using function SFO ()
while (SFO() == 0) {} // MEP_ScaleFactor calculated by MEP Cal Module
```

Step 4. Application Code

While the application is running, fluctuations in both device temperature and supply voltage may be expected. To be sure that optimal Scale Factors are used for each ePWM module, the SFO function should be re-run periodically as part of a slower back-ground loop. Some examples of this are shown here.

NOTE: See the HRPWM_SFO example in the device-specific C/C++ header files and peripheral examples available from the TI website.

Example 13-9. SFO Function Calls

```
main ()
{
int status;
// User code
// ePWM1, 2, 3, 4 are running in HRPWM mode
// The status variable returns 1 once a new MEP_ScaleFactor has been
// calculated by the MEP Calibration Module running SFO
// diagnostics.

status = SFO();
if(status==2) {ESTOP0;} // The function returns a 2 if MEP_ScaleFactor is greater
// than the maximum 255 allowed (error condition)
}
```

Enhanced Capture (eCAP)

This chapter describes the enhanced capture (eCAP), which is used in systems where accurate timing of external events is important.

The eCAP module described in this reference guide is a Type 0 eCAP. See the *TMS320C28xx, 28xxx DSP Peripheral Reference Guide* ([SPRU566](#)) for a list of all devices with a eCAP module of the same type, to determine the differences between the types, and for a list of device-specific differences within a type.

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14.1 Introduction

Features for eCAP include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module described in this guide includes the following features:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event time-stamps
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

14.2 Description

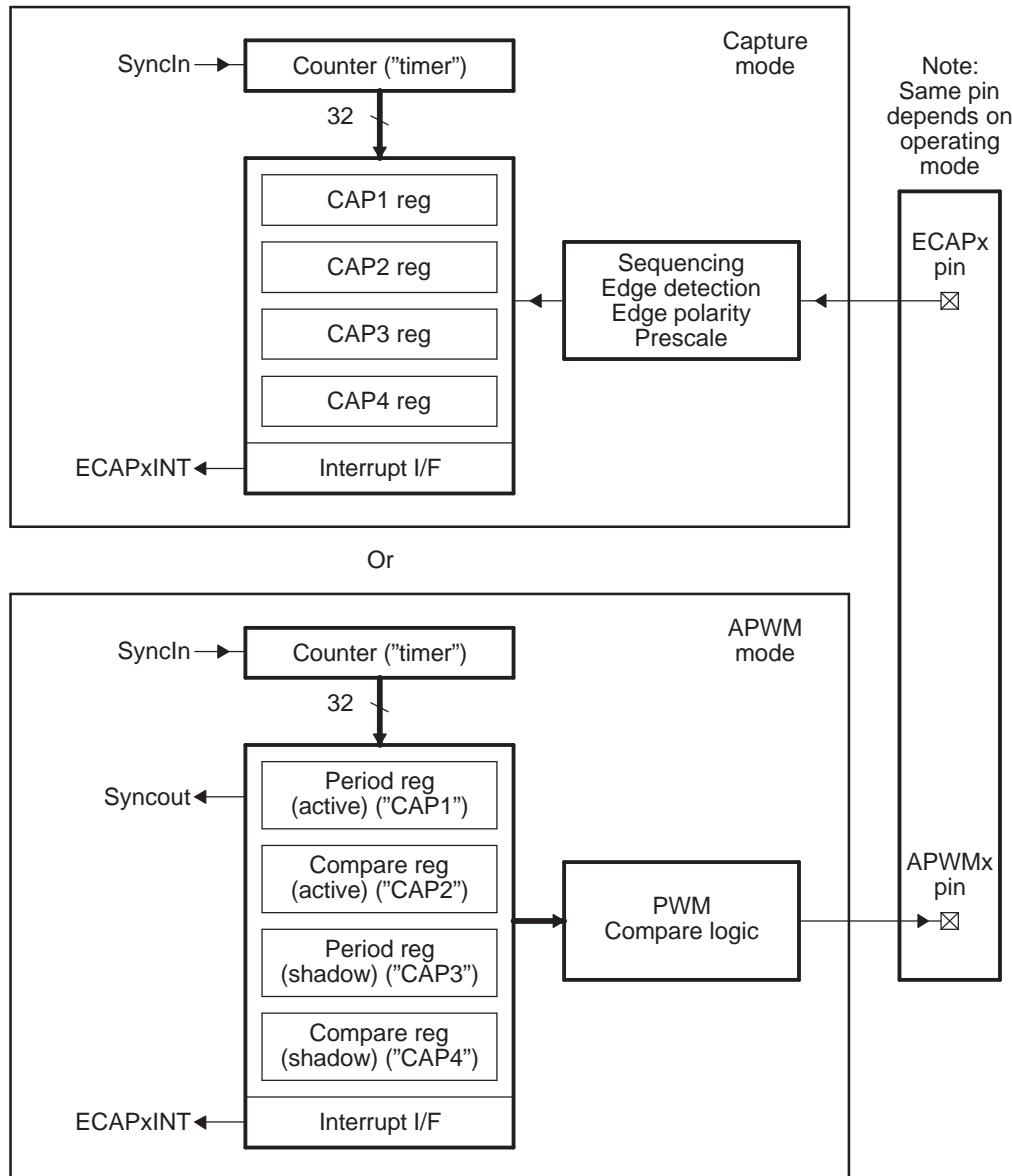
The eCAP module represents one complete capture channel that can be instantiated multiple times depending on the target device. In the context of this guide, one eCAP channel has the following independent key resources:

- Dedicated input capture pin
- 32-bit time base (counter)
- 4 x 32-bit time-stamp capture registers (CAP1-CAP4)
- 4-stage sequencer (Modulo4 counter) that is synchronized to external events, ECAP pin rising/falling edges.
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Input capture signal prescaling (from 2-62)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Control for continuous time-stamp captures using a 4-deep circular buffer (CAP1-CAP4) scheme
- Interrupt capabilities on any of the 4 capture events

14.3 Capture and APWM Operating Mode

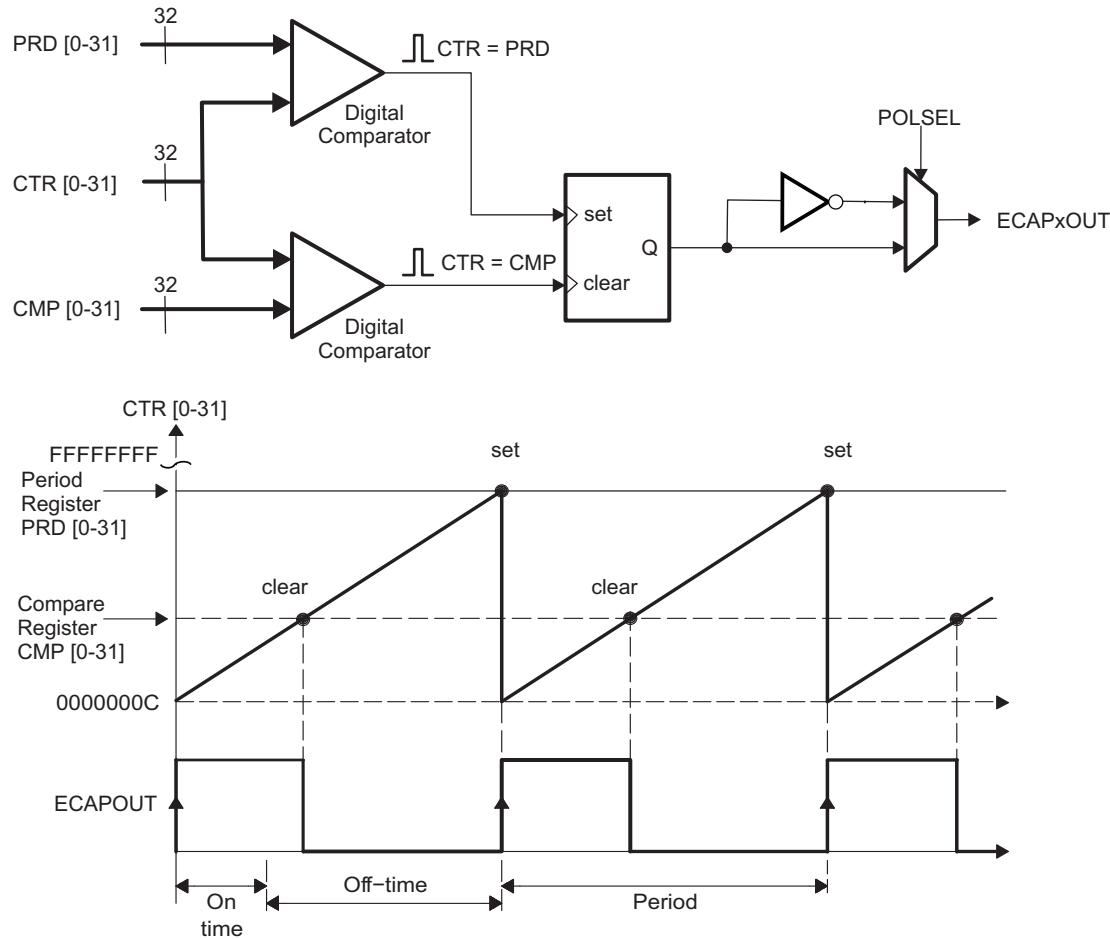
You can use the eCAP module resources to implement a single-channel PWM generator (with 32 bit capabilities) when it is not being used for input captures. The counter operates in count-up mode, providing a time-base for asymmetrical pulse width modulation (PWM) waveforms. The CAP1 and CAP2 registers become the active period and compare registers, respectively, while CAP3 and CAP4 registers become the period and capture shadow registers, respectively. [Figure 14-1](#) is a high-level view of both the capture and auxiliary pulse-width modulator (APWM) modes of operation.

Figure 14-1. Capture and APWM Modes of Operation



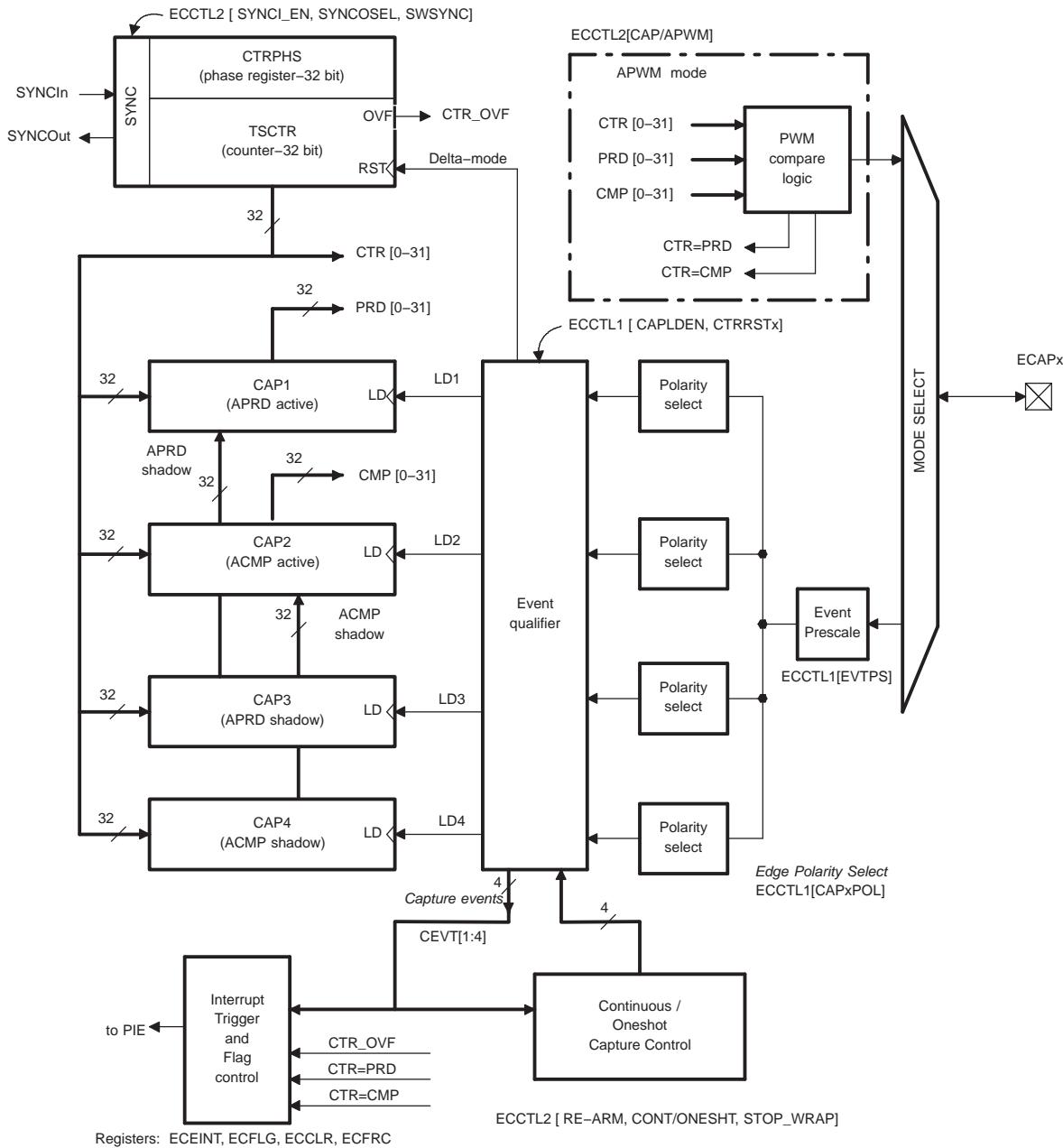
- A A single pin is shared between CAP and APWM functions. In capture mode, it is an input; in APWM mode, it is an output.
- B In APWM mode, writing any value to CAP1/CAP2 active registers also writes the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 invokes the shadow mode.

[Figure 14-2](#) further describes the output of the eCAP in APWM mode based on the CMP and PRD values.

Figure 14-2. Counter Compare and PRD Effects on the eCAP Output in APWM Mode

14.4 Capture Mode Description

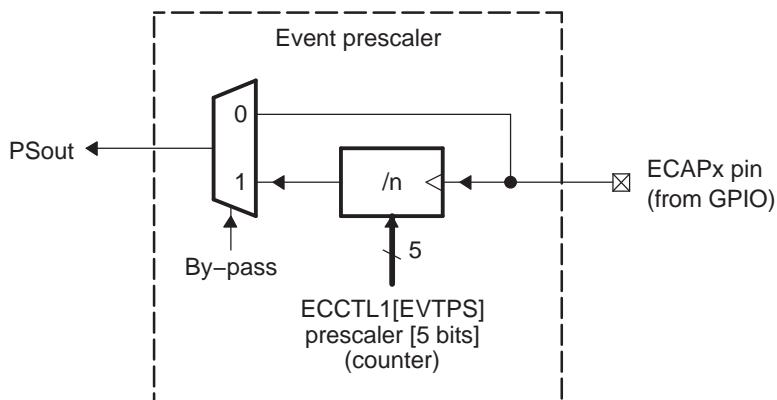
Figure 14-3 shows the various components that implement the capture function.

Figure 14-3. Capture Function Diagram


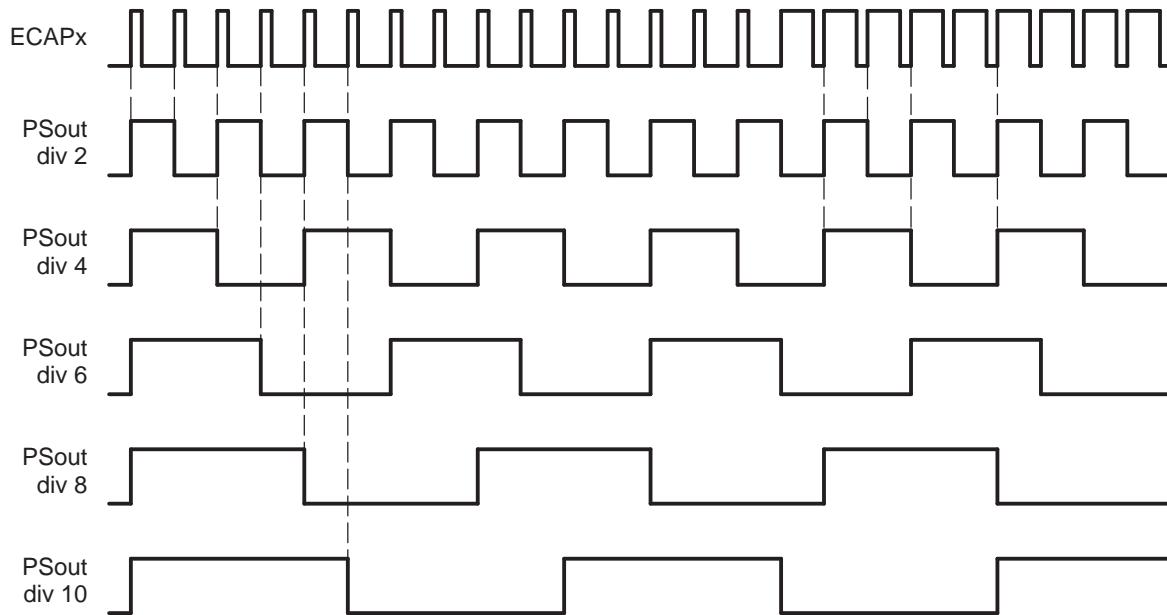
14.4.1 Event Prescaler

- An input capture signal (pulse train) can be prescaled by $N = 2-62$ (in multiples of 2) or can bypass the prescaler.

This is useful when very high frequency signals are used as inputs. [Figure 14-4](#) shows a functional diagram and [Figure 14-5](#) shows the operation of the prescale function.

Figure 14-4. Event Prescale Control

- A When a prescale value of 1 is chosen (ECCTL1[13:9] = 0,0,0,0,0) the input capture signal by-passes the prescale logic completely.

Figure 14-5. Prescale Function Waveforms

14.4.2 Edge Polarity Select and Qualifier

- Four independent edge polarity (rising edge/falling edge) selection MUXes are used, one for each capture event.
- Each edge (up to 4) is event qualified by the Modulo4 sequencer.
- The edge event is gated to its respective CAPx register by the Mod4 counter. The CAPx register is loaded on the falling edge.

14.4.3 Continuous/One-Shot Control

- The Mod4 (2 bit) counter is incremented via edge qualified events (CEVT1-CEVT4).
- The Mod4 counter continues counting (0->1->2->3->0) and wraps around unless stopped.
- A 2-bit stop register is used to compare the Mod4 counter output, and when equal stops the Mod4 counter and inhibits further loads of the CAP1-CAP4 registers. This occurs during one-shot operation.

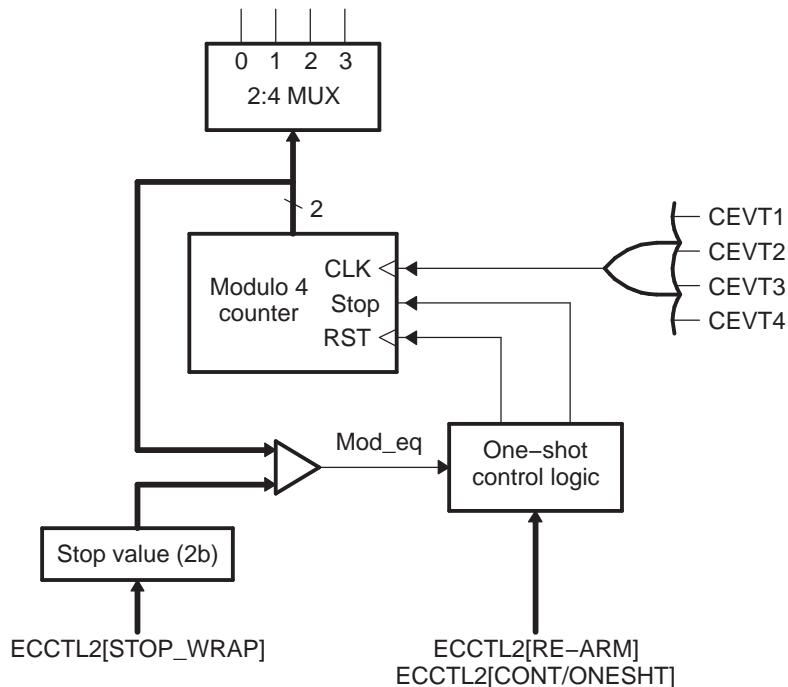
The continuous/one-shot block controls the start/stop and reset (zero) functions of the Mod4 counter via a mono-shot type of action that can be triggered by the stop-value comparator and re-armed via software control.

Once armed, the eCAP module waits for 1-4 (defined by stop-value) capture events before freezing both the Mod4 counter and contents of CAP1-4 registers (time-stamps).

Re-arming prepares the eCAP module for another capture sequence. Also re-arming clears (to zero) the Mod4 counter and permits loading of CAP1-4 registers again, providing the CAPLDEN bit is set.

In continuous mode, the Mod4 counter continues to run (0->1->2->3->0), the one-shot action is ignored, and capture values continue to be written to CAP1-4 in a circular buffer sequence.

Figure 14-6. Details of the Continuous/One-shot Block

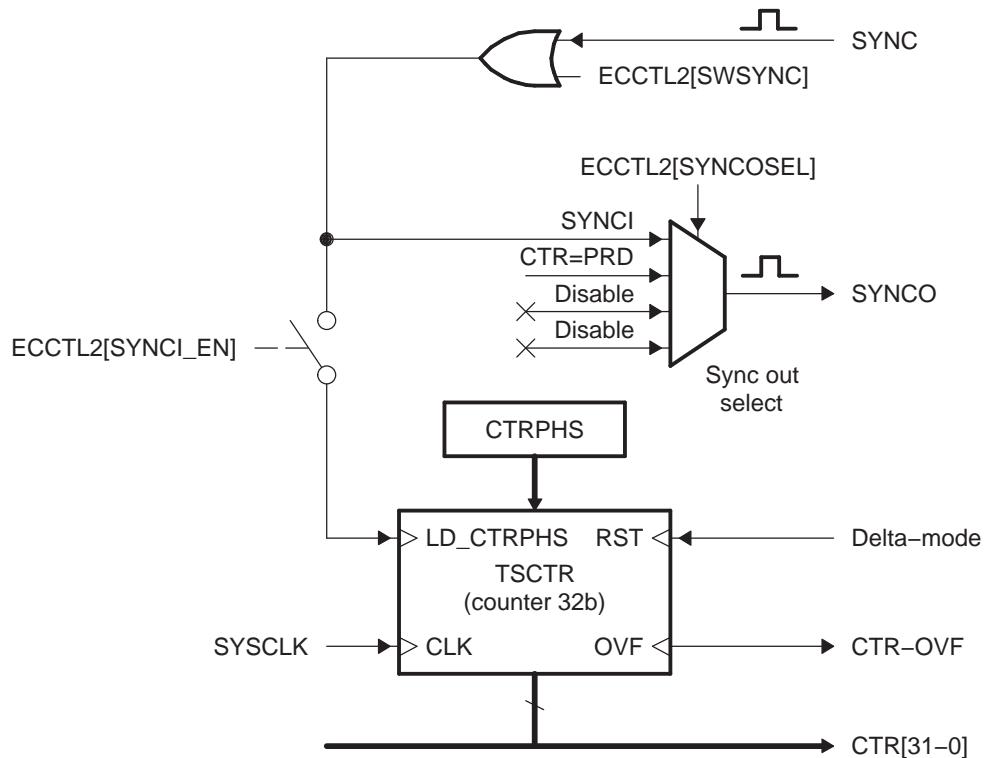


14.4.4 32-Bit Counter and Phase Control

This counter provides the time-base for event captures, and is clocked via the system clock.

A phase register is provided to achieve synchronization with other counters, via a hardware and software forced sync. This is useful in APWM mode when a phase offset between modules is needed.

On any of the four event loads, an option to reset the 32-bit counter is given. This is useful for time difference capture. The 32-bit counter value is captured first, then it is reset to 0 by any of the LD1-LD4 signals.

Figure 14-7. Details of the Counter and Synchronization Block

14.4.5 CAP1-CAP4 Registers

These 32-bit registers are fed by the 32-bit counter timer bus, CTR[0-31] and are loaded (capture a time-stamp) when their respective LD inputs are strobed.

Loading of the capture registers can be inhibited via control bit CAPLDEN. During one-shot operation, this bit is cleared (loading is inhibited) automatically when a stop condition occurs, StopValue = Mod4.

CAP1 and CAP2 registers become the active period and compare registers, respectively, in APWM mode.

CAP3 and CAP4 registers become the respective shadow registers (APRD and ACMP) for CAP1 and CAP2 during APWM operation.

14.4.6 Interrupt Control

An Interrupt can be generated on capture events (CEVT1-CEVT4, CTROVF) or APWM events (CTR = PRD, CTR = CMP).

A counter overflow event (FFFFFFFFFF->00000000) is also provided as an interrupt source (CTROVF).

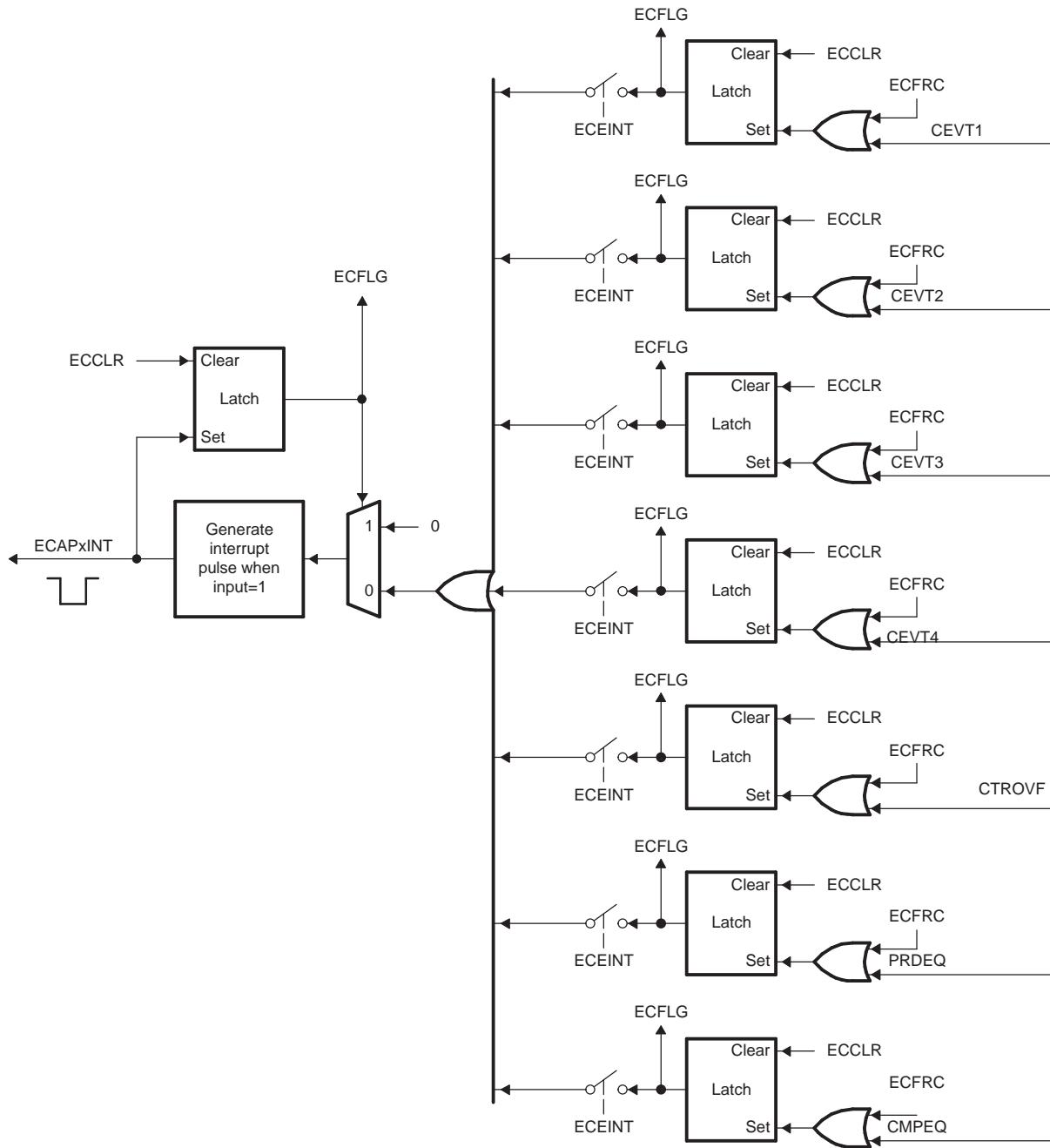
The capture events are edge and sequencer qualified (ordered in time) by the polarity select and Mod4 gating, respectively.

One of these events can be selected as the interrupt source (from the eCAPx module) going to the PIE.

Seven interrupt events (CEVT1, CEVT2, CEVT3, CEVT4, CTROVF, CTR=PRD, CTR=CMP) can be generated. The interrupt enable register (ECEINT) is used to enable/disable individual interrupt event sources. The interrupt flag register (ECFLG) indicates if any interrupt event has been latched and contains the global interrupt flag bit (INT). An interrupt pulse is generated to the PIE only if any of the interrupt events are enabled, the flag bit is 1, and the INT flag bit is 0. The interrupt service routine must clear the global interrupt flag bit and the serviced event via the interrupt clear register (ECCLR) before any other interrupt pulses are generated. You can force an interrupt event via the interrupt force register (ECFRC). This is useful for test purposes.

Note: The CEVT1, CEVT2, CEVT3, CEVT4 flags are only active in capture mode (ECCTL2[CAP/APWM == 0]). The CTR=PRD, CTR=CMP flags are only valid in APWM mode (ECCTL2[CAP/APWM == 1]). CNTOVF flag is valid in both modes.

Figure 14-8. Interrupts in eCAP Module



14.4.7 Shadow Load and Lockout Control

In capture mode, this logic inhibits (locks out) any shadow loading of CAP1 or CAP2 from APRD and ACMP registers, respectively.

In APWM mode, shadow loading is active and two choices are permitted:

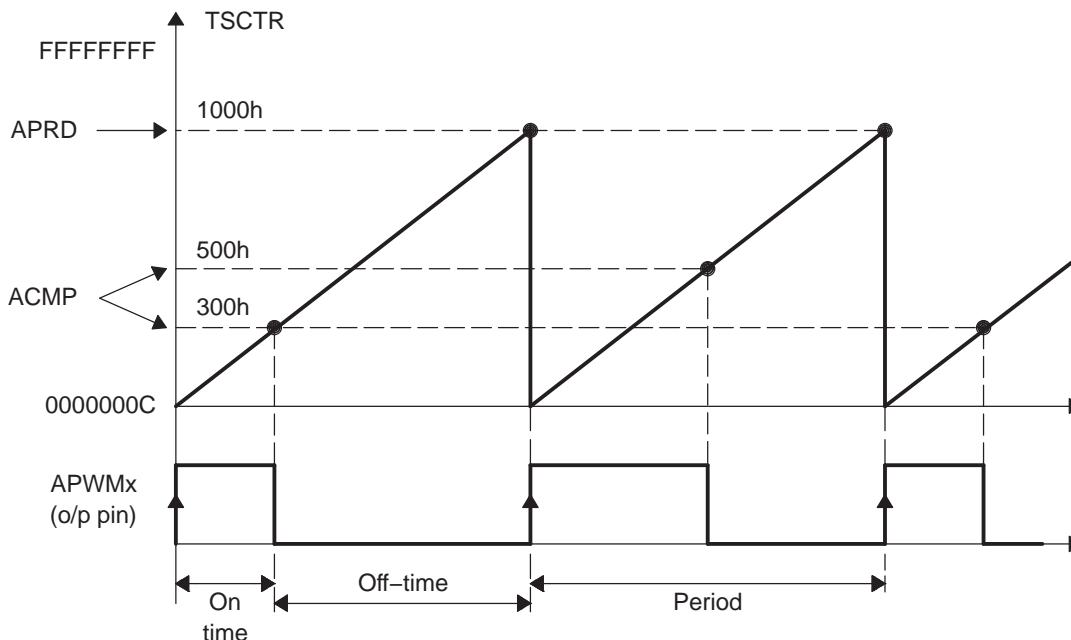
- Immediate - APRD or ACMP are transferred to CAP1 or CAP2 immediately upon writing a new value.
- On period equal, CTR[31:0] = PRD[31:0]

14.4.8 APWM Mode Operation

Main operating highlights of the APWM section:

- The time-stamp counter bus is made available for comparison via 2 digital (32-bit) comparators.
- When CAP1/2 registers are not used in capture mode, their contents can be used as Period and Compare values in APWM mode.
- Double buffering is achieved via shadow registers APRD and ACMP (CAP3/4). The shadow register contents are transferred over to CAP1/2 registers either immediately upon a write, or on a CTR = PRD trigger.
- In APWM mode, writing to CAP1/CAP2 active registers will also write the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 will invoke the shadow mode.
- During initialization, you must write to the active registers for both period and compare. This automatically copies the initial values into the shadow values. For subsequent compare updates, during run-time, you only need to use the shadow registers.

Figure 14-9. PWM Waveform Details Of APWM Mode Operation



The behavior of APWM active high mode (APWMPOL == 0) is as follows:

- CMP = 0x00000000, output low for duration of period (0% duty)
- CMP = 0x00000001, output high 1 cycle
- CMP = 0x00000002, output high 2 cycles
- CMP = PERIOD, output high except for 1 cycle (<100% duty)
- CMP = PERIOD+1, output high for complete period (100% duty)
- CMP > PERIOD+1, output high for complete period

The behavior of APWM active low mode (APWMPOL == 1) is as follows:

- CMP = 0x00000000, output high for duration of period (0% duty)
- CMP = 0x00000001, output low 1 cycle
- CMP = 0x00000002, output low 2 cycles
- CMP = PERIOD, output low except for 1 cycle (<100% duty)
- CMP = PERIOD+1, output low for complete period (100% duty)
- CMP > PERIOD+1, output low for complete period

14.5 Application of the ECAP Module

The following sections will provide Applications examples and code snippets to show how to configure and operate the eCAP module. For clarity and ease of use, the examples use the eCAP "C" header files. Below are useful #defines which will help in the understanding of the examples.

```
// ECCTL1 (ECAP Control Reg 1)

//=====
// CAPxPOL bits      #define EC_RISING 0x0      #define EC_FALLING 0x1
// CTRRSTx bits      #define EC_ABS_MODE 0x0     #define EC_DELTA_MODE 0x1
// PRESCALE bits     #define EC_BYPASS 0x0      #define EC_DIV1 0x0 #define EC_DIV2 0x1
//                           #define EC_DIV4 0x2 #define EC_DIV6 0x3
//                           #define EC_DIV8 0x4 #define EC_DIV10 0x5

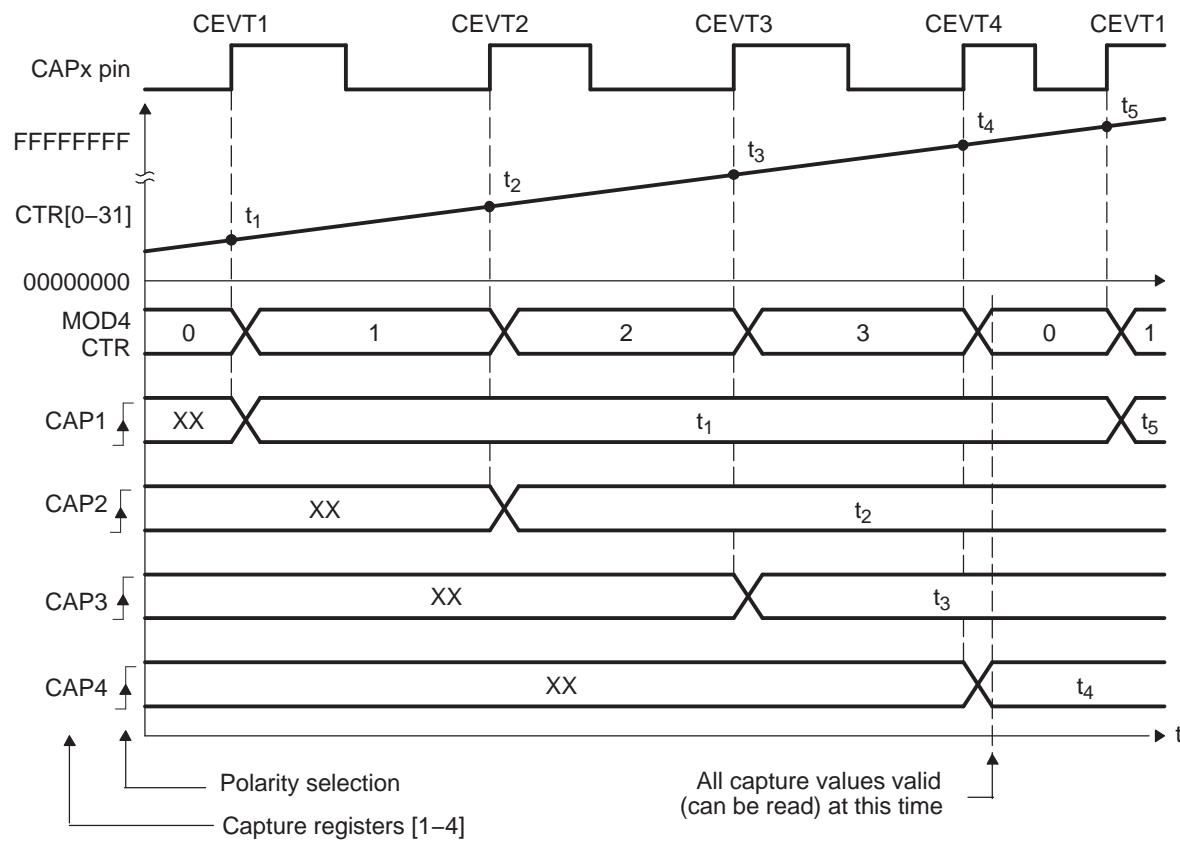
// ECCTL2 ( ECAP Control Reg 2)
//=====
// CONT/ONESHOT bit  #define EC_CONTINUOUS 0x0 #define EC_ONESHOT 0x1
// STOPVALUE bit      #define EC_EVENT1 0x0       #define EC_EVENT2 0x1 #define EC_EVENT3 0x2
//                           #define EC_EVENT4 0x3

// RE-ARM bit #define EC_ARM 0x1
// TSCTRSTOP bit    #define EC_FREEZE 0x0      #define EC_RUN 0x1
// SYNCSEL bit       #define EC_SYNCIN 0x0      #define EC_CTR_PRD 0x1
//                           #define EC_SYNC_DIS 0x2
// CAP/APWM mode bit #define EC_CAP_MODE 0x0      #define EC_APWM_MODE 0x1
// APWMMPOL bit      #define EC_ACTV_HI 0x0      #define EC_ACTV_LO 0x1
// Generic           #define EC_DISABLE 0x0      #define EC_ENABLE 0x1 #define EC_FORCE 0x1
```

14.5.1 Example 1 - Absolute Time-Stamp Operation Rising Edge Trigger

Figure 14-10 shows an example of continuous capture operation (Mod4 counter wraps around). In this figure, TSCTR counts-up without resetting and capture events are qualified on the rising edge only, this gives period (and frequency) information.

On an event, the TSCTR contents (time-stamp) is first captured, then Mod4 counter is incremented to the next state. When the TSCTR reaches FFFFFFFF (maximum value), it wraps around to 00000000 (not shown in Figure 14-10), if this occurs, the CTROVF (counter overflow) flag is set, and an interrupt (if enabled) occurs, CTROVF (counter overflow) Flag is set, and an Interrupt (if enabled) occurs. Captured Time-stamps are valid at the point indicated by the diagram (after the 4th event), hence event CEVT4 can conveniently be used to trigger an interrupt and the CPU can read data from the CAPx registers.

Figure 14-10. Capture Sequence for Absolute Time-stamp and Rising Edge Detect

14.5.1.1 Code snippet for CAP mode Absolute Time, Rising Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising edge trigger

// Initialization Time
//=====

// ECAP module 1 config ECap1Regs.ECCTL1.bit.CAP1POL = EC_RISING;

ECap1Regs.ECCTL1.bit.CAP2POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP3POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP4POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CTRRST1 = EC_ABS_MODE;
ECap1Regs.ECCTL1.bit.CTRRST2 = EC_ABS_MODE;
ECap1Regs.ECCTL1.bit.CTRRST3 = EC_ABS_MODE;
ECap1Regs.ECCTL1.bit.CTRRST4 = EC_ABS_MODE;
ECap1Regs.ECCTL1.bit.CAPLDEN = EC_ENABLE;
ECap1Regs.ECCTL1.bit.PRESCALE = EC_DIV1;
ECap1Regs.ECCTL2.bit.CAP_APWM = EC_CAP_MODE;
ECap1Regs.ECCTL2.bit.CONT_ONESHRT = EC_CONTINUOUS;
ECap1Regs.ECCTL2.bit.SYNCO_SEL = EC_SYNCO_DIS;
ECap1Regs.ECCTL2.bit.SYNCI_EN = EC_DISABLE;
ECap1Regs.ECCTL2.bit.TSCTRSTOP = EC_RUN;

// Allow TSCTR to run

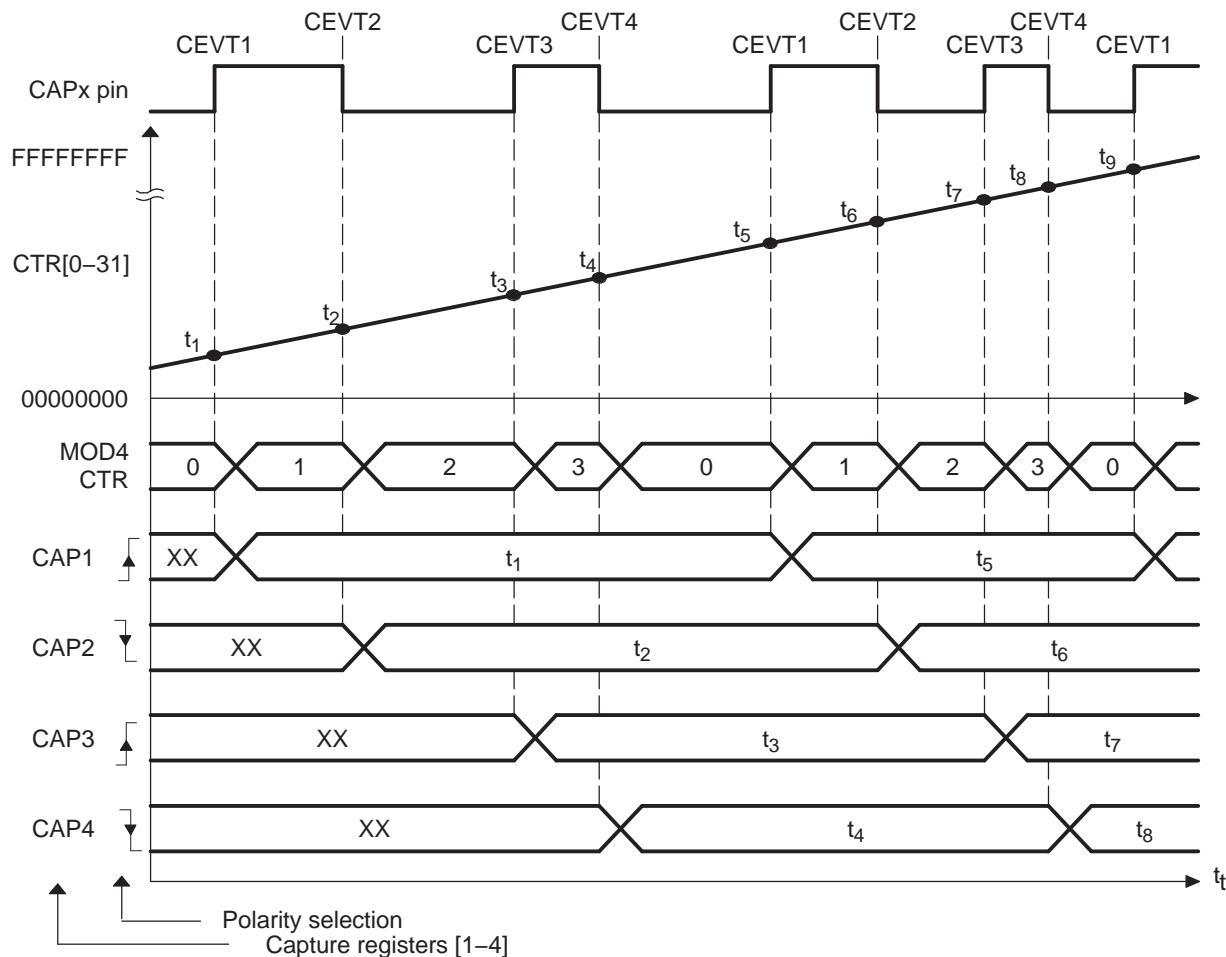
// Run Time (CEVT4 triggered ISR call)
//=====

TSt1 = ECap1Regs.CAP1;
// Fetch Time-Stamp captured at t1 TSt2 = ECap1Regs.CAP2;
// Fetch Time-Stamp captured at t2 TSt3 = ECap1Regs.CAP3;
// Fetch Time-Stamp captured at t3 TSt4 = ECap1Regs.CAP4;
// Fetch Time-Stamp captured at t4 Period1 = TSt2-TSt1;
// Calculate 1st period Period2 = TSt3-TSt2;
// Calculate 2nd period Period3 = TSt4-TSt3;
// Calculate 3rd period
```

14.5.2 Example 2 - Absolute Time-Stamp Operation Rising and Falling Edge Trigger

In Figure 14-11 the eCAP operating mode is almost the same as in the previous section except capture events are qualified as either rising or falling edge, this now gives both period and duty cycle information, i.e: Period1 = $t_3 - t_1$, Period2 = $t_5 - t_3$, ...etc. Duty Cycle1 (on-time %) = $(t_2 - t_1) / \text{Period1} \times 100\%$, etc. Duty Cycle1 (off-time %) = $(t_3 - t_2) / \text{Period1} \times 100\%$, etc.

Figure 14-11. Capture Sequence for Absolute Time-stamp With Rising and Falling Edge Detect



14.5.2.1 Code Snippet for CAP mode Absolute Time, Rising and Falling Edge Triggers

```
// Code snippet for CAP mode Absolute Time, Rising and Falling
// edge triggers // Initialization Time
//=====
// ECAP module 1 config ECap1Regs.ECCTL1.bit.CAP1POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP2POL = EC_FALLING;
ECap1Regs.ECCTL1.bit.CAP3POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP4POL = EC_FALLING;
ECap1Regs.ECCTL1.bit.CTRRST1 = EC_ABS_MODE;
ECap1Regs.ECCTL1.bit.CTRRST2 = EC_ABS_MODE;
ECap1Regs.ECCTL1.bit.CTRRST3 = EC_ABS_MODE;
ECap1Regs.ECCTL1.bit.CTRRST4 = EC_ABS_MODE;
ECap1Regs.ECCTL1.bit.CAPLDEN = EC_ENABLE;
ECap1Regs.ECCTL1.bit.PRESCALE = EC_DIV1;
ECap1Regs.ECCTL2.bit.CAP_APWM = EC_CAP_MODE;
ECap1Regs.ECCTL2.bit.CONT_ONESHRT = EC_CONTINUOUS;
ECap1Regs.ECCTL2.bit.SYNCO_SEL = EC_SYNCO_DIS;
ECap1Regs.ECCTL2.bit.SYNCI_EN = EC_DISABLE;
ECap1Regs.ECCTL2.bit.TSCTRSTOP = EC_RUN;

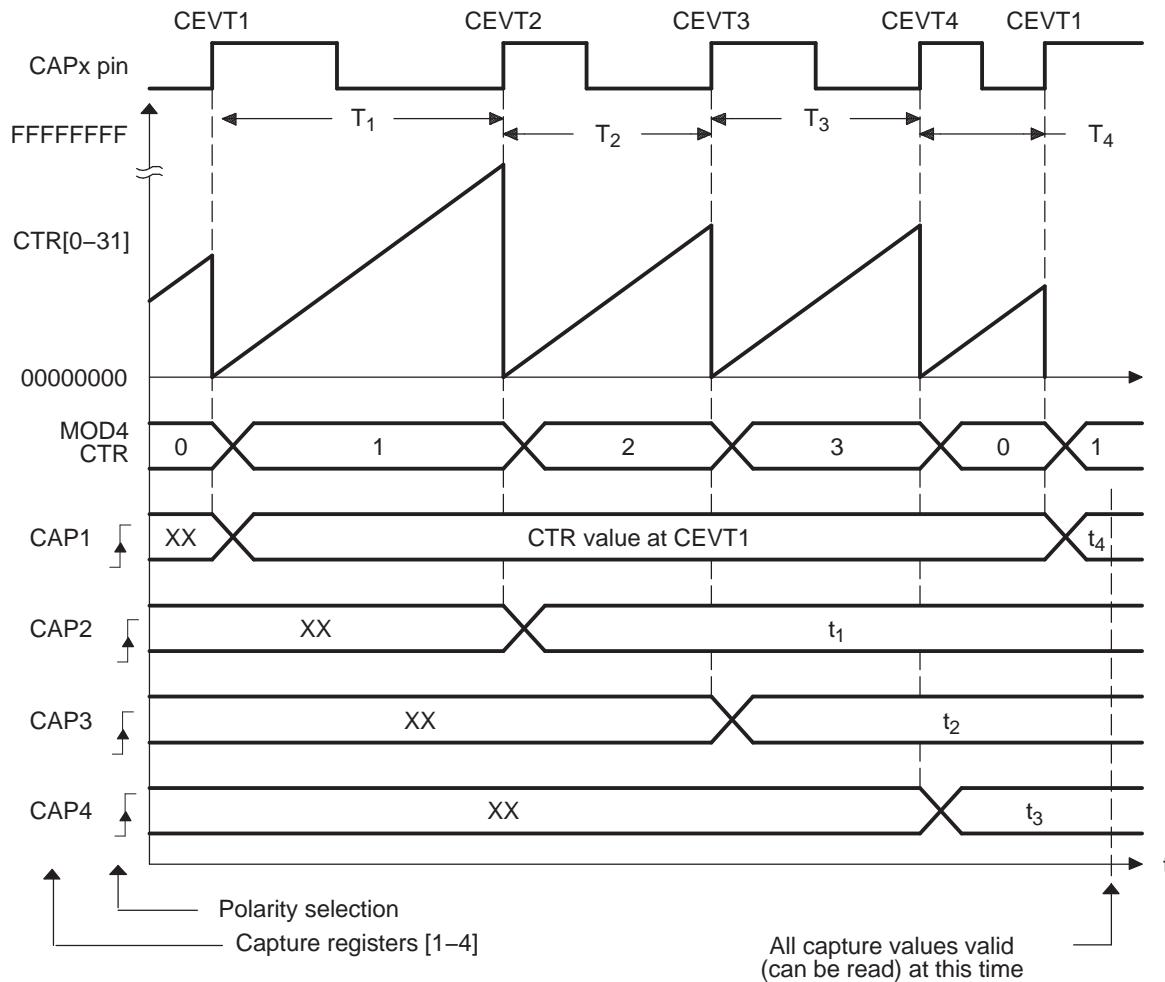
// Allow TSCTR to run
// Run Time (CEVT4 triggered ISR call)
//=====

TSt1 = ECap1Regs.CAP1;
// Fetch Time-Stamp captured at t1 TSt2 = ECap1Regs.CAP2;
// Fetch Time-Stamp captured at t2 TSt3 = ECap1Regs.CAP3;
// Fetch Time-Stamp captured at t3 TSt4 = ECap1Regs.CAP4;
// Fetch Time-Stamp captured at t4 Period1 = TSt3-TSt1;
// Calculate 1st period DutyOnTime1 = TSt2-TSt1;
// Calculate On time DutyOffTime1 = TSt3-TSt2;
// Calculate Off time
```

14.5.3 Example 3 - Time Difference (Delta) Operation Rising Edge Trigger

This example Figure 14-12 shows how the eCAP module can be used to collect Delta timing data from pulse train waveforms. Here Continuous Capture mode (TSCTR counts-up without resetting, and Mod4 counter wraps around) is used. In Delta-time mode, TSCTR is Reset back to Zero on every valid event. Here Capture events are qualified as Rising edge only. On an event, TSCTR contents (Time-Stamp) is captured first, and then TSCTR is reset to Zero. The Mod4 counter then increments to the next state. If TSCTR reaches FFFFFFFF (Max value), before the next event, it wraps around to 00000000 and continues, a CNTOVF (counter overflow) Flag is set, and an Interrupt (if enabled) occurs. The advantage of Delta-time Mode is that the CAPx contents directly give timing data without the need for CPU calculations, that is, Period1 = T_1 , Period2 = T_2 , ... etc. As shown in the diagram, the CEVT1 event is a good trigger point to read the timing data, T_1 , T_2 , T_3 , T_4 are all valid here.

Figure 14-12. Capture Sequence for Delta Mode Time-stamp and Rising Edge Detect



14.5.3.1 Code snippet for CAP mode Delta Time, Rising Edge Trigger

```
// Code snippet for CAP mode Delta Time, Rising edge trigger

// Initialization Time

//=====
// ECAP module 1 config ECap1Regs.ECCTL1.bit.CAP1POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP2POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP3POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP4POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CTRRST1 = EC_DELTA_MODE;
ECap1Regs.ECCTL1.bit.CTRRST2 = EC_DELTA_MODE;
ECap1Regs.ECCTL1.bit.CTRRST3 = EC_DELTA_MODE;
ECap1Regs.ECCTL1.bit.CTRRST4 = EC_DELTA_MODE;
ECap1Regs.ECCTL1.bit.CAPLDEN = EC_ENABLE;
ECap1Regs.ECCTL1.bit.PRESCALE = EC_DIV1;
ECap1Regs.ECCTL2.bit.CAP_APWM = EC_CAP_MODE;
ECap1Regs.ECCTL2.bit.CONT_ONESHRT = EC_CONTINUOUS;
ECap1Regs.ECCTL2.bit.SYNCO_SEL = EC_SYNC0_DIS;
ECap1Regs.ECCTL2.bit.SYNC1_EN = EC_DISABLE;
ECap1Regs.ECCTL2.bit.TSCTRSTOP = EC_RUN;

// Allow TSCTR to run

// Run Time (CEVT1 triggered ISR call)

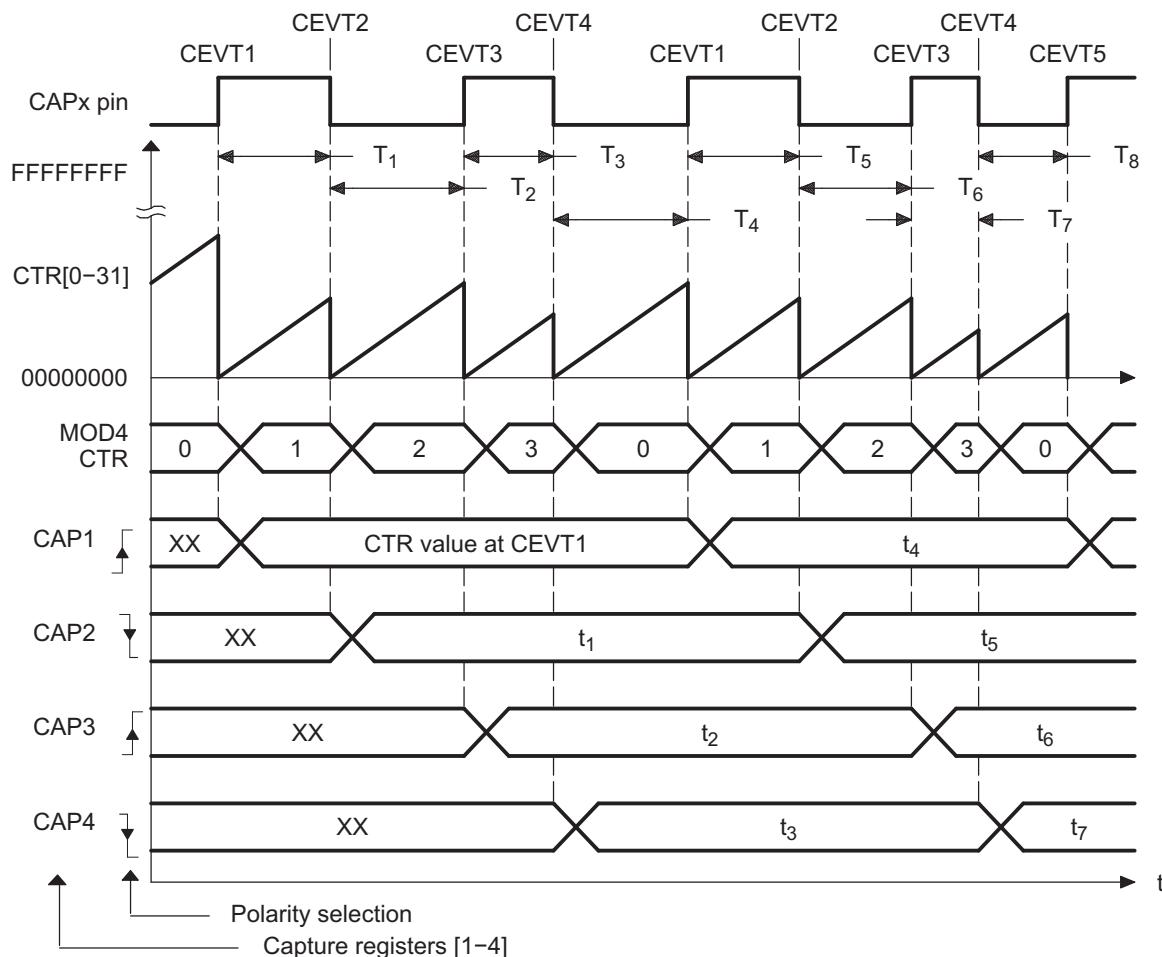
//=====

// Note: here Time-stamp directly represents the Period value. Period4 = ECap1Regs.CAP1;
// Fetch Time-Stamp captured at T1 Period1 = ECap1Regs.CAP2;
// Fetch Time-Stamp captured at T2 Period2 = ECap1Regs.CAP3;
// Fetch Time-Stamp captured at T3 Period3 = ECap1Regs.CAP4;
// Fetch Time-Stamp captured at T4
```

14.5.4 Example 4 - Time Difference (Delta) Operation Rising and Falling Edge Trigger

In Figure 14-13 the eCAP operating mode is almost the same as in previous section except Capture events are qualified as either Rising or Falling edge, this now gives both Period and Duty cycle information, i.e: Period1 = T_1+T_2 , Period2 = T_3+T_4 , ...etc Duty Cycle1 (on-time %) = $T_1 / \text{Period1} \times 100\%$, etc Duty Cycle1 (off-time %) = $T_2 / \text{Period1} \times 100\%$, etc

Figure 14-13. Capture Sequence for Delta Mode Time-stamp With Rising and Falling Edge Detect



During initialization, you must write to the active registers for both period and compare. This will then automatically copy the init values into the shadow values. For subsequent compare updates, during run-time, only the shadow registers must be used.

14.5.4.1 Code snippet for CAP mode Delta Time, Rising and Falling Edge Triggers

```
// Code snippet for CAP mode Delta Time, Rising and Falling
// edge triggers
// Initialization Time

//=====
// ECAP module 1 config ECap1Regs.ECCTL1.bit.CAP1POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP2POL = EC_FALLING;
ECap1Regs.ECCTL1.bit.CAP3POL = EC_RISING;
ECap1Regs.ECCTL1.bit.CAP4POL = EC_FALLING;
ECap1Regs.ECCTL1.bit.CTRRST1 = EC_DELTA_MODE;
ECap1Regs.ECCTL1.bit.CTRRST2 = EC_DELTA_MODE;
ECap1Regs.ECCTL1.bit.CTRRST3 = EC_DELTA_MODE;
ECap1Regs.ECCTL1.bit.CTRRST4 = EC_DELTA_MODE;
ECap1Regs.ECCTL1.bit.CAPLDEN = EC_ENABLE;
ECap1Regs.ECCTL1.bit.PRESCALE = EC_DIV1;
ECap1Regs.ECCTL2.bit.CAP_APWM = EC_CAP_MODE;
ECap1Regs.ECCTL2.bit.CONT_ONESHRT = EC_CONTINUOUS;
ECap1Regs.ECCTL2.bit.SYNCO_SEL = EC_SYNC_DIS;
ECap1Regs.ECCTL2.bit.SYNCI_EN = EC_DISABLE;
ECap1Regs.ECCTL2.bit.TSCTRSTOP = EC_RUN;

// Allow TSCTR to run

// Run Time (CEVT1 triggered ISR call)

//=====
// Note: here Time-stamp directly represents the Duty cycle values. DutyOnTime1 = ECap1Regs.CAP2;

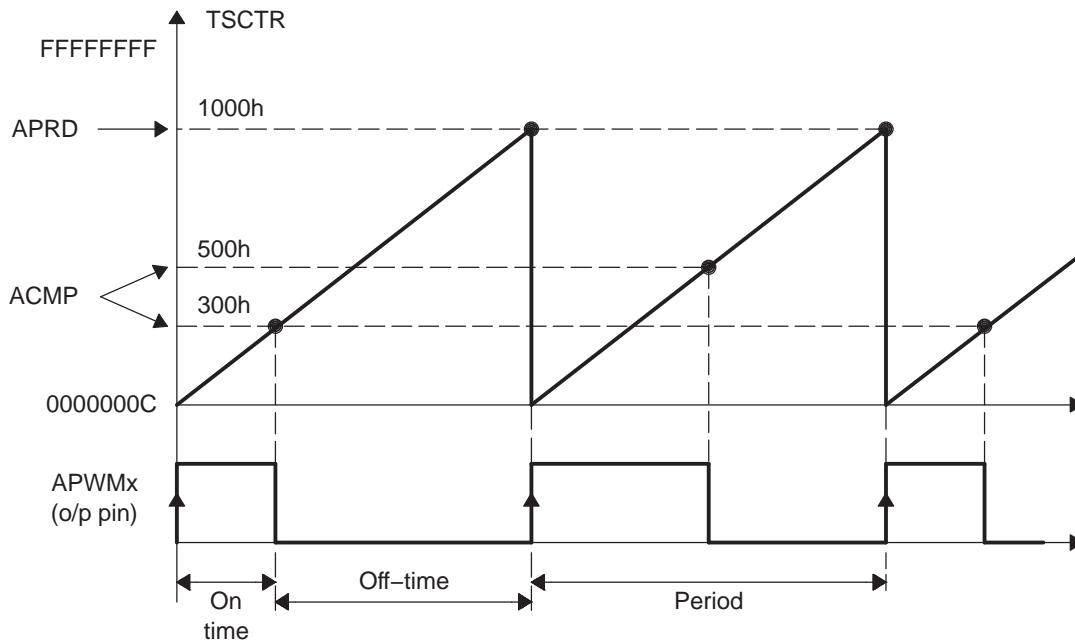
// Fetch Time-Stamp captured at T2 DutyOffTime1 = ECap1Regs.CAP3;
// Fetch Time-Stamp captured at T3 DutyOnTime2 = ECap1Regs.CAP4;
// Fetch Time-Stamp captured at T4 DutyOffTime2 = ECap1Regs.CAP1;
// Fetch Time-
Stamp captured at T1 Period1 = DutyOnTime1 + DutyOffTime1; Period2 = DutyOnTime2 + DutyOffTime2;
```

14.6 Application of the APWM Mode

In this example, the eCAP module is configured to operate as a PWM generator. Here a very simple single channel PWM waveform is generated from output pin APWMx. The PWM polarity is active high, which means that the compare value (CAP2 reg is now a compare register) represents the on-time (high level) of the period. Alternatively, if the APWMPOL bit is configured for active low, then the compare value represents the off-time. Note here values are in hexadecimal ("h") notation.

14.6.1 Example 1 - Simple PWM Generation (Independent Channel/s)

Figure 14-14. PWM Waveform Details of APWM Mode Operation



Example 14-1. Code Snippet for APWM Mode

```
// Code snippet for APWM mode Example 1

// Initialization Time
//=====
// ECAP module 1 config ECap1Regs.CAP1 = 0x1000;
// Set period value ECap1Regs.CTRPHS = 0x0;
// make phase zero ECap1Regs.ECCTL2.bit.CAP_APWM = EC_APWM_MODE;
//           ECap1Regs.ECCTL2.bit.APWMPOL = EC_ACTV_HI;
// Active high ECap1Regs.ECCTL2.bit.SYNCI_EN = EC_DISABLE;
// Synch not used ECap1Regs.ECCTL2.bit.SYNCO_SEL = EC_SYNC_DIS;
// Synch not used ECap1Regs.ECCTL2.bit.TSCTRSTOP = EC_RUN;
// Allow TSCTR to run
// Run Time (Instant 1, for example, ISR call)
//=====
ECap1Regs.CAP2 = 0x300;
```

Example 14-1. Code Snippet for APWM Mode (continued)

```
// Set Duty cycle, that is, compare value  
  
// Run Time (Instant 2, for example, another ISR call)  
  
//=====\  
ECap1Regs.CAP2 = 0x500;  
  
// Set Duty cycle, that is, compare value
```

14.7 Registers

14.7.1 eCAP Base Addresses

eCAP Base Address Table

Device Register	Register Name	Start Address	End Address
ECap1Regs	ECAP_REGS	0x0000_5000	0x0000_501F
ECap2Regs	ECAP_REGS	0x0000_5020	0x0000_503F
ECap3Regs	ECAP_REGS	0x0000_5040	0x0000_505F
ECap4Regs	ECAP_REGS	0x0000_5060	0x0000_507F
ECap5Regs	ECAP_REGS	0x0000_5080	0x0000_509F
ECap6Regs	ECAP_REGS	0x0000_50A0	0x0000_50BF
ECap7Regs	ECAP_REGS	0x0000_50C0	0x0000_50DF
ECap8Regs	ECAP_REGS	0x0000_50E0	0x0000_50FF

14.7.2 ECAP_REGS Registers

Table 14-1 lists the memory-mapped registers for the ECAP_REGS. All register offset addresses not listed in Table 14-1 should be considered as reserved locations and the register contents should not be modified.

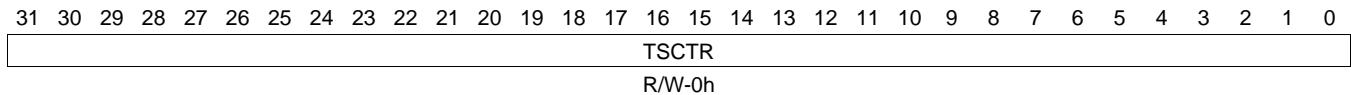
Table 14-1. ECAP_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	TSCTR	Time-Stamp Counter	Section 14.7.2.1	
2h	CTRPHS	Counter Phase Offset Value Register	Section 14.7.2.2	
4h	CAP1	Capture 1 Register	Section 14.7.2.3	
6h	CAP2	Capture 2 Register	Section 14.7.2.4	
8h	CAP3	Capture 3 Register	Section 14.7.2.5	
Ah	CAP4	Capture 4 Register	Section 14.7.2.6	
14h	ECCTL1	Capture Control Register 1	Section 14.7.2.7	
15h	ECCTL2	Capture Control Register 2	Section 14.7.2.8	
16h	ECEINT	Capture Interrupt Enable Register	Section 14.7.2.9	
17h	ECFLG	Capture Interrupt Flag Register	Section 14.7.2.10	
18h	ECCLR	Capture Interrupt Flag Register	Section 14.7.2.11	
19h	ECFRC	Capture Interrupt Force Register	Section 14.7.2.12	

14.7.2.1 TSCTR Register (offset = 0h) [reset = 0h]

TSCTR is shown in [Figure 14-15](#) and described in [Table 14-2](#).

Time-Stamp Counter

Figure 14-15. TSCTR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-2. TSCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TSCTR	R/W	0h	Active 32-bit counter register that is used as the capture time-base

14.7.2.2 CTRPHS Register (offset = 2h) [reset = 0h]CTRPHS is shown in [Figure 14-16](#) and described in [Table 14-3](#).

Counter Phase Offset Value Register

Figure 14-16. CTRPHS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRPHS																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-3. CTRPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CTRPHS	R/W	0h	Counter phase value register that can be programmed for phase lag/lead. This register shadows TSCTR and is loaded into TSCTR upon either a SYNC1 event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases.

14.7.2.3 CAP1 Register (offset = 4h) [reset = 0h]

CAP1 is shown in [Figure 14-17](#) and described in [Table 14-4](#).

Capture 1 Register

Figure 14-17. CAP1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP1																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-4. CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP1	R/W	0h	This register can be loaded (written) by : Time-Stamp (counter value TSCTR) during a capture event Software - may be useful for test purposes / initialization APRD shadow register (CAP3) when used in APWM mode

14.7.2.4 CAP2 Register (offset = 6h) [reset = 0h]

CAP2 is shown in [Figure 14-18](#) and described in [Table 14-5](#).

Capture 2 Register

Figure 14-18. CAP2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP2																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-5. CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP2	R/W	0h	This register can be loaded (written) by: - Time-Stamp (counter value) during a capture event - Software - may be useful for test purposes - APRD shadow register (CAP4) when used in APWM mode

14.7.2.5 CAP3 Register (offset = 8h) [reset = 0h]

CAP3 is shown in [Figure 14-19](#) and described in [Table 14-6](#).

Capture 3Register

Figure 14-19. CAP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP3																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-6. CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP3	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the period shadow (APRD) register. You update the PWM period value through this register. In this mode, CAP3 (APRD) shadows CAP1.

14.7.2.6 CAP4 Register (offset = Ah) [reset = 0h]CAP4 is shown in [Figure 14-20](#) and described in [Table 14-7](#).

Capture 4 Register

Figure 14-20. CAP4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP4																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-7. CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP4	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow (ACMP) register. You update the PWM compare value via this register. In this mode, CAP4 (ACMP) shadows CAP2.

14.7.2.7 ECCTL1 Register (offset = 14h) [reset = 0h]

ECCTL1 is shown in [Figure 14-21](#) and described in [Table 14-8](#).

Capture Control Register 1

Figure 14-21. ECCTL1 Register

15	14	13	12	11	10	9	8
FREE_SOFT		PRESCALE					
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-8. ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREE_SOFT	R/W	0h	Emulation Control 0h (R/W) = TSCTR counter stops immediately on emulation suspend 1h (R/W) = TSCTR counter runs until = 0 Ah (R/W) = TSCTR counter is unaffected by emulation suspend (Run Free) Bh (R/W) = TSCTR counter is unaffected by emulation suspend (Run Free)
13-9	PRESCALE	R/W	0h	Event Filter prescale select 0h (R/W) = Divide by 1 (i.e., no prescale, by-pass the prescaler) 1h (R/W) = Divide by 2 Ah (R/W) = Divide by 4 Bh (R/W) = Divide by 6 64h (R/W) = Divide by 8 65h (R/W) = Divide by 10 2B66h (R/W) = Divide by 60 2B67h (R/W) = Divide by 62
8	CAPLDEN	R/W	0h	Enable Loading of CAP1-4 registers on a capture event 0h (R/W) = Disable CAP1-4 register loads at capture event time. 1h (R/W) = Enable CAP1-4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4 0h (R/W) = Do not reset counter on Capture Event 4 (absolute time stamp operation) 1h (R/W) = Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	R/W	0h	Capture Event 4 Polarity select 0h (R/W) = Capture Event 4 triggered on a rising edge (RE) 1h (R/W) = Capture Event 4 triggered on a falling edge (FE)
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3 0h (R/W) = Do not reset counter on Capture Event 3 (absolute time stamp) 1h (R/W) = Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity select 0h (R/W) = Capture Event 3 triggered on a rising edge (RE) 1h (R/W) = Capture Event 3 triggered on a falling edge (FE)

Table 14-8. ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2 0h (R/W) = Do not reset counter on Capture Event 2 (absolute time stamp) 1h (R/W) = Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity select 0h (R/W) = Capture Event 2 triggered on a rising edge (RE) 1h (R/W) = Capture Event 2 triggered on a falling edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1 0h (R/W) = Do not reset counter on Capture Event 1 (absolute time stamp) 1h (R/W) = Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity select 0h (R/W) = Capture Event 1 triggered on a rising edge (RE) 1h (R/W) = Capture Event 1 triggered on a falling edge (FE)

14.7.2.8 ECCTL2 Register (offset = 15h) [reset = 2h]

ECCTL2 is shown in [Figure 14-22](#) and described in [Table 14-9](#).

Capture Control Register 2

Figure 14-22. ECCTL2 Register

15	14	13	12	11	10	9	8
RESERVED				APWM POL	CAP_APWM	SWSYNC	
R-0h				R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
SYNCO_SEL	SYNCI_EN	TSCTRSTOP	RE_ARM	STOP_WRAP	CONT_ONESH_T		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-9. ECCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	APWM POL	R/W	0h	APWM output polarity select. 0h (R/W) = Output is active high (Compare value defines high time) 1h (R/W) = Output is active low (Compare value defines low time)
9	CAP_APWM	R/W	0h	CAP/APWM operating mode select 0h (R/W) = ECAP module operates in capture mode. This mode forces the following configuration: - Inhibits TSCTR resets via CTR = PRD event - Inhibits shadow loads on CAP1 and 2 registers - Permits user to enable CAP1-4 register load - CAPx/APWMx pin operates as a capture input 1h (R/W) = ECAP module operates in APWM mode. This mode forces the following configuration: - Resets TSCTR on CTR = PRD event (period boundary) - Permits shadow loading on CAP1 and 2 registers - Disables loading of time-stamps into CAP1-4 registers - CAPx/APWMx pin operates as a APWM output
8	SWSYNC	R/W	0h	Software-forced Counter (TSCTR) Synchronizing. 0h (R/W) = Writing a zero has no effect. Reading always returns a zero 1h (R/W) = Writing a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0,0. After writing a 1, this bit returns to a zero. Note: Selection CTR = PRD is meaningful only in APWM mode however, you can choose it in CAP mode if you find doing so useful.
7-6	SYNCO_SEL	R/W	0h	Sync-Out Select 0h (R/W) = Select sync-in event to be the sync-out signal pass through 1h (R/W) = Select CTR = PRD event to be the sync-out signal Ah (R/W) = Disable sync out signal Bh (R/W) = Disable sync out signal

Table 14-9. ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SYNCI_EN	R/W	0h	Counter (TSCTR) Sync-In select mode 0h (R/W) = Disable sync-in option 1h (R/W) = Enable counter (TSCTR) to be loaded from CTRPHS register upon either a SYNCI signal or a S/W force event.
4	TSCTRSTOP	R/W	0h	Time Stamp (TSCTR) Counter Stop (freeze) Control 0h (R/W) = TSCTR stopped 1h (R/W) = TSCTR free-running
3	RE_ARM	R/W	0h	One-Shot Re-Arming Control, that is, wait for stop trigger. 0h (R/W) = Has no effect (reading always returns a 0) 1h (R/W) = Arms the one-shot sequence as follows: 1) Resets the Mod4 counter to zero 2) Unfreezes the Mod4 counter 3) Enables capture register loads
2-1	STOP_WRAP	R/W	1h	Stop value for one-shot mode. This is the number (between 1-4) of captures allowed to occur before the CAP(1-4) registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number (between 1-4) of the capture register in which the circular buffer wraps around and starts again. Notes: STOP_WRAP is compared to Mod4 counter and, when equal, 2 actions occur: - Mod4 counter is stopped (frozen) - Capture register loads are inhibited In one-shot mode, further interrupt events are blocked until re-armed. 0h (R/W) = Stop after Capture Event 1 in one-shot mode Wrap after Capture Event 1 in continuous mode. 1h (R/W) = Stop after Capture Event 2 in one-shot mode Wrap after Capture Event 2 in continuous mode. Ah (R/W) = Stop after Capture Event 3 in one-shot mode Wrap after Capture Event 3 in continuous mode. Bh (R/W) = Stop after Capture Event 4 in one-shot mode Wrap after Capture Event 4 in continuous mode.
0	CONT_ONESH	R/W	0h	Continuous or one-shot mode control (applicable only in capture mode) 0h (R/W) = Operate in continuous mode 1h (R/W) = Operate in one-Shot mode

14.7.2.9 ECEINT Register (offset = 16h) [reset = 0h]

ECEINT is shown in [Figure 14-23](#) and described in [Table 14-10](#).

The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ECCLR registers.

The proper procedure for configuring peripheral modes and interrupts is as follows:

- Disable global interrupts
- Stop eCAP counter
- Disable eCAP interrupts
- Configure peripheral registers
- Clear spurious eCAP interrupt flags
- Enable eCAP interrupts
- Start eCAP counter
- Enable global interrupts

Figure 14-23. ECEINT Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-10. ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved
7	CTR_CMP	R/W	0h	Counter Equal Compare Interrupt Enable 0h (R/W) = Disable Compare Equal as an Interrupt source 1h (R/W) = Enable Compare Equal as an Interrupt source
6	CTR_PRD	R/W	0h	Counter Equal Period Interrupt Enable 0h (R/W) = Disable Period Equal as an Interrupt source 1h (R/W) = Enable Period Equal as an Interrupt source
5	CTROVF	R/W	0h	Counter Overflow Interrupt Enable 0h (R/W) = Disabled counter Overflow as an Interrupt source 1h (R/W) = Enable counter Overflow as an Interrupt source
4	CEVT4	R/W	0h	Capture Event 4 Interrupt Enable 0h (R/W) = Disable Capture Event 4 as an Interrupt source 1h (R/W) = Capture Event 4 Interrupt Enable
3	CEVT3	R/W	0h	Capture Event 3 Interrupt Enable 0h (R/W) = Disable Capture Event 3 as an Interrupt source 1h (R/W) = Enable Capture Event 3 as an Interrupt source
2	CEVT2	R/W	0h	Capture Event 2 Interrupt Enable 0h (R/W) = Disable Capture Event 2 as an Interrupt source 1h (R/W) = Enable Capture Event 2 as an Interrupt source
1	CEVT1	R/W	0h	Capture Event 1 Interrupt Enable 0h (R/W) = Disable Capture Event 1 as an Interrupt source 1h (R/W) = Enable Capture Event 1 as an Interrupt source
0	RESERVED	R/W	0h	Reserved

14.7.2.10 ECFLG Register (offset = 17h) [reset = 0h]

ECFLG is shown in [Figure 14-24](#) and described in [Table 14-11](#).

Capture Interrupt Flag Register

Figure 14-24. ECFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-11. ECFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CTR_CMP	R	0h	Compare Equal Compare Status Flag. This flag is active only in APWM mode. 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the counter (TSCTR) reached the compare register value (ACMP)
6	CTR_PRD	R	0h	Counter Equal Period Status Flag. This flag is only active in APWM mode. 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the counter (TSCTR) reached the period register value (APRD) and was reset.
5	CTROVF	R	0h	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the counter (TSCTR) has made the transition from FFFFFFFF " 00000000
4	CEVT4	R	0h	Capture Event 4 Status Flag This flag is only active in CAP mode. 0h (R/W) = Indicates no event occurred 1h (R/W) = ndicates the fourth event occurred at ECAPx pin
3	CEVT3	R	0h	Capture Event 3 Status Flag. This flag is active only in CAP mode. 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the third event occurred at ECAPx pin.
2	CEVT2	R	0h	Capture Event 2 Status Flag. This flag is only active in CAP mode. 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the second event occurred at ECAPx pin.
1	CEVT1	R	0h	Capture Event 1 Status Flag. This flag is only active in CAP mode. 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the first event occurred at ECAPx pin.
0	INT	R	0h	Global Interrupt Status Flag 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates that an interrupt was generated.

14.7.2.11 ECCLR Register (offset = 18h) [reset = 0h]

ECCLR is shown in [Figure 14-25](#) and described in [Table 14-12](#).

Capture Interrupt Flag Register

Figure 14-25. ECCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-12. ECCLR Register Field Descriptions

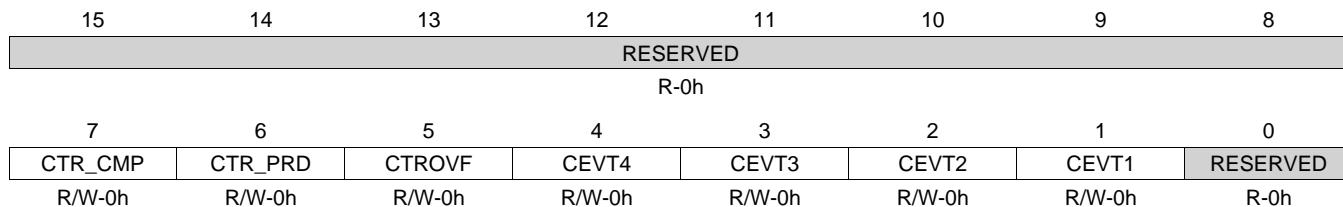
Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CTR_CMP	R/W	0h	Counter Equal Compare Status Flag 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CTR=CMP flag condition
6	CTR_PRD	R/W	0h	Counter Equal Period Status Flag 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CTR=PRD flag condition
5	CTROVF	R/W	0h	Counter Overflow Status Flag 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CTROVF flag condition
4	CEVT4	R/W	0h	Capture Event 4 Status Flag 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CEVT4 flag condition.
3	CEVT3	R/W	0h	Capture Event 3 Status Flag 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CEVT3 flag condition.
2	CEVT2	R/W	0h	Capture Event 2 Status Flag 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CEVT2 flag condition.
1	CEVT1	R/W	0h	Capture Event 1 Status Flag 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CEVT1 flag condition.
0	INT	R/W	0h	Global Interrupt Clear Flag 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1

14.7.2.12 ECFRC Register (offset = 19h) [reset = 0h]

ECFRC is shown in [Figure 14-26](#) and described in [Table 14-13](#).

Capture Interrupt Force Register

Figure 14-26. ECFRC Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 14-13. ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CTR_CMP	R/W	0h	Force Counter Equal Compare Interrupt 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CTR=CMP flag bit.
6	CTR_PRD	R/W	0h	Force Counter Equal Period Interrupt 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CTR=PRD flag bit.
5	CTROVF	R/W	0h	Force Counter Overflow 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 to this bit sets the CTROVF flag bit.
4	CEVT4	R/W	0h	Force Capture Event 4 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CEVT4 flag bit
3	CEVT3	R/W	0h	Force Capture Event 3 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CEVT3 flag bit
2	CEVT2	R/W	0h	Force Capture Event 2 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CEVT2 flag bit.
1	CEVT1	R/W	0h	Force Capture Event 1 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Sets the CEVT1 flag bit.
0	RESERVED	R	0h	Reserved

Enhanced QEP (eQEP)

The enhanced QEP (eQEP) module described here is a Type 0 eQEP. See the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* ([SPRU566](#)) for a list of all devices with a module of the same type to determine the differences between types and for a list of device-specific differences within a type.

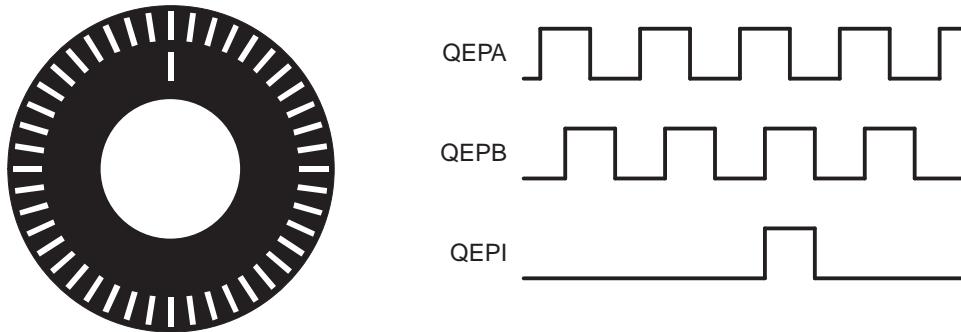
The enhanced quadrature encoder pulse (eQEP) module is used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine for use in a high-performance motion and position-control system.

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15.1 Introduction

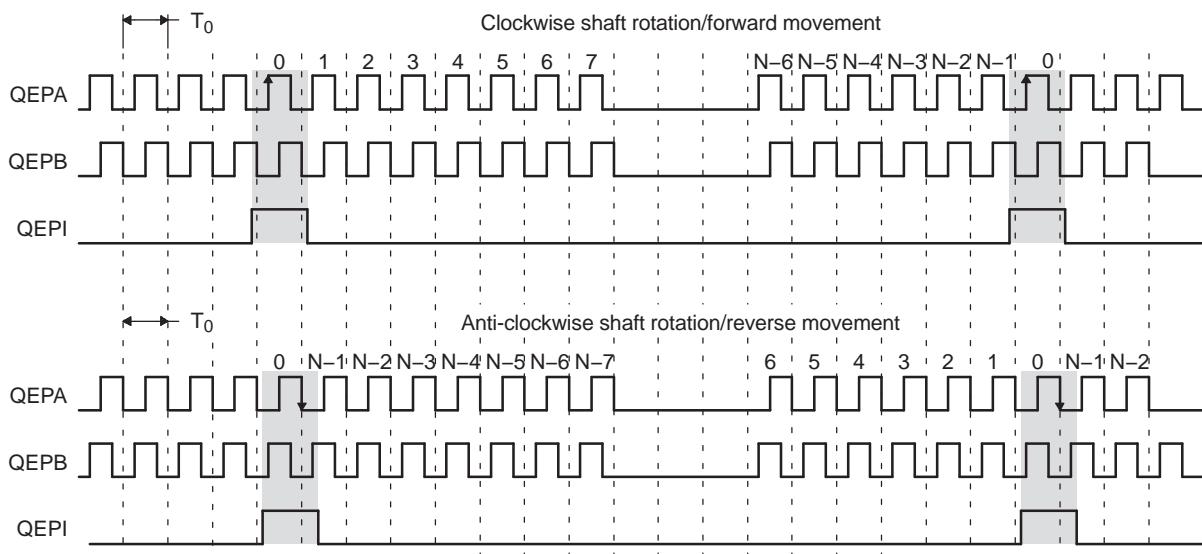
A single track of slots patterns the periphery of an incremental encoder disk, as shown in [Figure 15-1](#). These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position, and zero reference

Figure 15-1. Optical Encoder Disk



To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90° out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vice versa as shown in [Figure 15-2](#).

Figure 15-2. QEP Encoder Output Signal for Forward/Reverse Movement

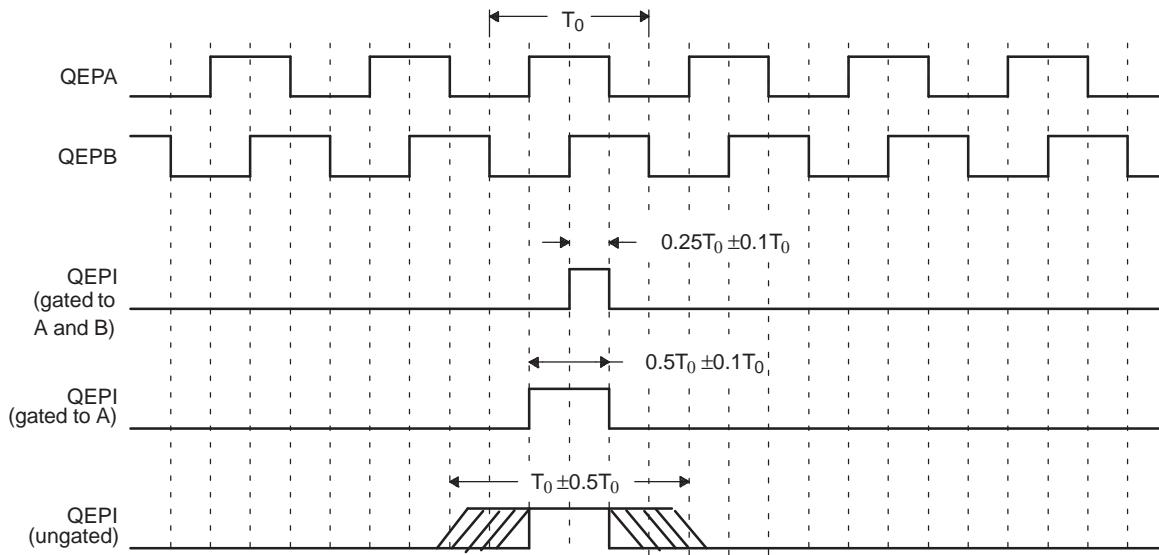


Legend: N = lines per revolution

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 KHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

Quadrature encoders from different manufacturers come with two forms of index pulse (gated index pulse or ungated index pulse) as shown in [Figure 15-3](#). A nonstandard form of index pulse is ungated. In the ungated configuration, the index edges are not necessarily coincident with A and B signals. The gated index pulse is aligned to any of the four quadrature edges and width of the index pulse and can be equal to a quarter, half, or full period of the quadrature signal.

Figure 15-3. Index Pulse Example



Some typical applications of shaft encoders include robotics and even computer input in the form of a mouse. Inside your mouse you can see where the mouse ball spins a pair of axles (a left/right, and an up/down axle). These axles are connected to optical shaft encoders that effectively tell the computer how fast and in what direction the mouse is moving.

General Issues: Estimating velocity from a digital position sensor is a cost-effective strategy in motor control. Two different first order approximations for velocity may be written as:

$$v(k) \approx \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T} \quad (2)$$

$$v(k) \approx \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \quad (3)$$

where

$v(k)$: Velocity at time instant k

$x(k)$: Position at time instant k

$x(k-1)$: Position at time instant k-1

T: Fixed unit time or inverse of velocity calculation rate

ΔX : Incremental position movement in unit time

$t(k)$: Time instant "k"

$t(k-1)$: Time instant "k-1"

X: Fixed unit position

ΔT : Incremental time elapsed for unit position movement.

[Equation 2](#) is the conventional approach to velocity estimation and it requires a time base to provide unit time event for velocity calculation. Unit time is basically the inverse of the velocity calculation rate.

The encoder count (position) is read once during each unit time event. The quantity $[x(k) - x(k-1)]$ is formed by subtracting the previous reading from the current reading. Then the velocity estimate is computed by multiplying by the known constant $1/T$ (where T is the constant time between unit time events and is known in advance).

Estimation based on [Equation 2](#) has an inherent accuracy limit directly related to the resolution of the position sensor and the unit time period T . For example, consider a 500-line per revolution quadrature encoder with a velocity calculation rate of 400 Hz. When used for position the quadrature encoder gives a four-fold increase in resolution, in this case, 2000 counts per revolution. The minimum rotation that can be detected is therefore 0.0005 revolutions, which gives a velocity resolution of 12 rpm when sampled at 400 Hz. While this resolution may be satisfactory at moderate or high speeds, e.g. 1% error at 1200 rpm, it would clearly prove inadequate at low speeds. In fact, at speeds below 12 rpm, the speed estimate would erroneously be zero much of the time.

At low speed, [Equation 3](#) provides a more accurate approach. It requires a position sensor that outputs a fixed interval pulse train, such as the aforementioned quadrature encoder. The width of each pulse is defined by motor speed for a given sensor resolution. [Equation 3](#) can be used to calculate motor speed by measuring the elapsed time between successive quadrature pulse edges. However, this method suffers from the opposite limitation, as does [Equation 2](#). A combination of relatively large motor speeds and high sensor resolution makes the time interval ΔT small, and thus more greatly influenced by the timer resolution. This can introduce considerable error into high-speed estimates.

For systems with a large speed range (that is, speed estimation is needed at both low and high speeds), one approach is to use [Equation 3](#) at low speed and have the DSP software switch over to [Equation 2](#) when the motor speed rises above some specified threshold.

15.2 Description

This section provides the eQEP inputs, memory map, and functional description.

15.2.1 EQEP Inputs

The eQEP inputs include two pins for quadrature-clock mode or direction-count mode, an index (or 0 marker), and a strobe input. The eQEP module requires that the QEPA, QEPB, and QEPI inputs are synchronized to SYSCLK prior to entering the module. The application code should enable the synchronous GPIO input feature on any eQEP-enabled GPIO pins (see the *System Control and Interrupts* chapter for more details).

- **QEPA/XCLK and QEPB/XDIR**

These two pins can be used in quadrature-clock mode or direction-count mode.

- **Quadrature-clock Mode**

The eQEP encoders provide two square wave signals (A and B) 90 electrical degrees out of phase whose phase relationship is used to determine the direction of rotation of the input shaft and number of eQEP pulses from the index position to derive the relative position information. For forward or clockwise rotation, QEPA signal leads QEPB signal and vice versa. The quadrature decoder uses these two inputs to generate quadrature-clock and direction signals.

- **Direction-count Mode**

In direction-count mode, direction and clock signals are provided directly from the external source. Some position encoders have this type of output instead of quadrature output. The QEPA pin provides the clock input and the QEPB pin provides the direction input.

- **QEPI: Index or Zero Marker**

The eQEP encoder uses an index signal to assign an absolute start position from which position information is incrementally encoded using quadrature pulses. This pin is connected to the index output of the eQEP encoder to optionally reset the position counter for each revolution. This signal can be used to initialize or latch the position counter on the occurrence of a desired event on the index pin.

- **QEPS: Strobe Input**

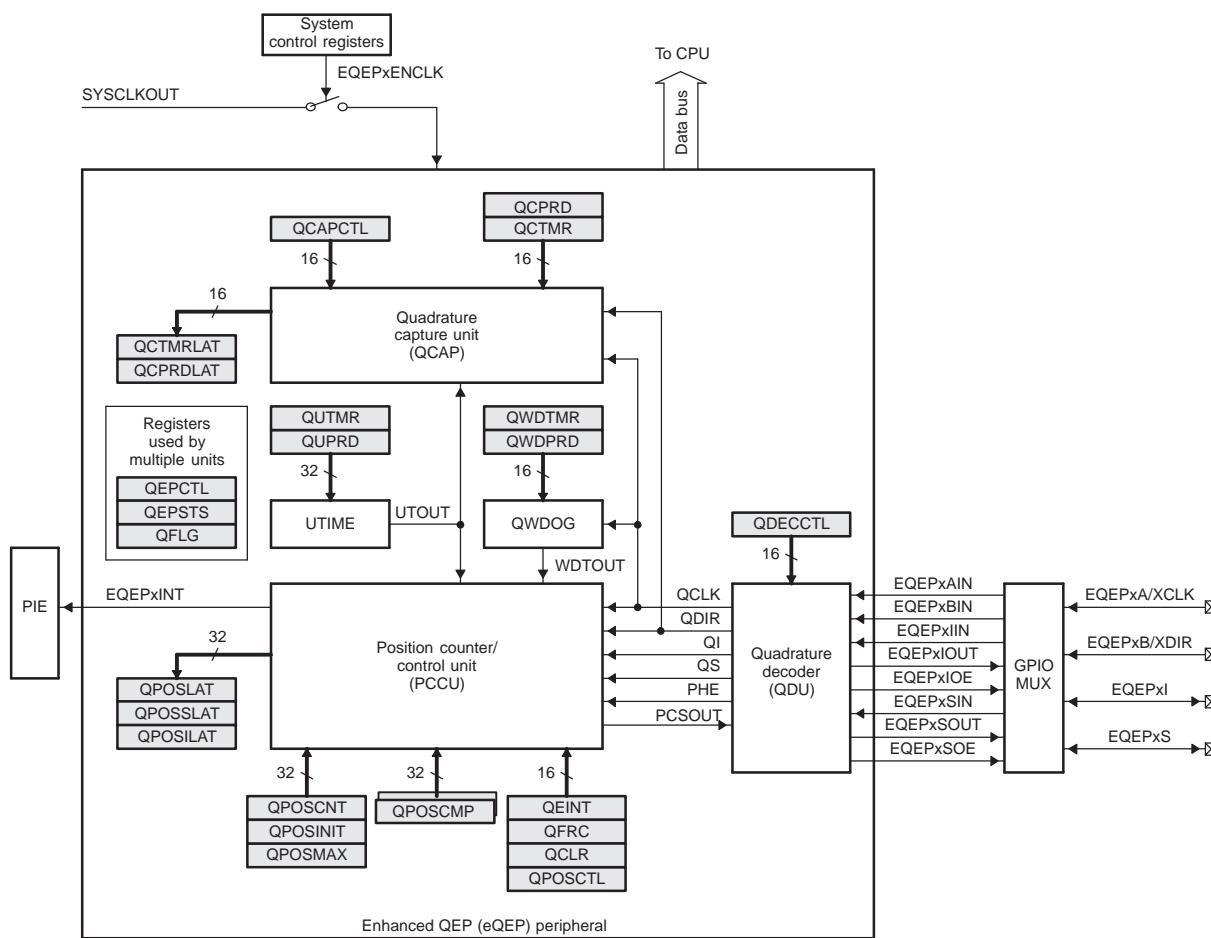
This general-purpose strobe signal can initialize or latch the position counter on the occurrence of a desired event on the strobe pin. This signal is typically connected to a sensor or limit switch to notify that the motor has reached a defined position.

15.2.2 Functional Description

The eQEP peripheral contains the following major functional units (as shown in Figure 15-4):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)

Figure 15-4. Functional Block Diagram of the eQEP Peripheral



15.2.3 eQEP Memory Map

Table 15-1 lists the registers with their memory locations, sizes, and reset values.

Table 15-1. EQEP Memory Map

Name	Offset	Size(x16)/#shadow	Reset	Register Description
QPOSCNT	0x00	2/0	0x00000000	eQEP Position Counter
QPOSINIT	0x02	2/0	0x00000000	eQEP Initialization Position Count
QPOSMAX	0x04	2/0	0x00000000	eQEP Maximum Position Count
QPOSCMP	0x06	2/1	0x00000000	eQEP Position-compare
QPOSILAT	0x08	2/0	0x00000000	eQEP Index Position Latch

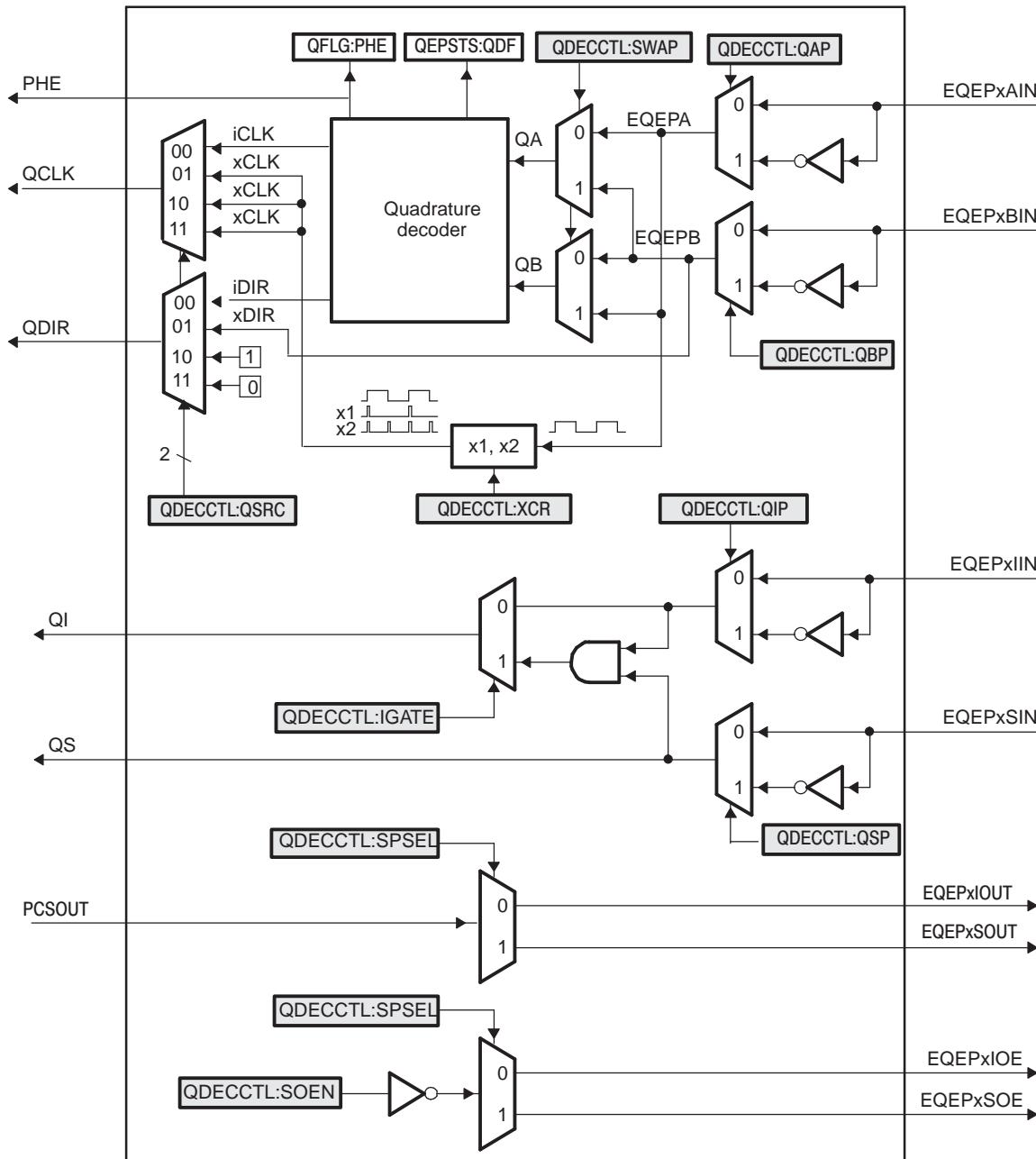
Table 15-1. EQEP Memory Map (continued)

Name	Offset	Size(x16)/#shadow	Reset	Register Description
QPOSSLAT	0x0A	2/0	0x00000000	eQEP Strobe Position Latch
QPOSLAT	0x0C	2/0	0x00000000	eQEP Position Latch
QUTMR	0x0E	2/0	0x00000000	QEP Unit Timer
QUPRD	0x10	2/0	0x00000000	eQEP Unit Period Register
QWDTMR	0x12	1/0	0x0000	eQEP Watchdog Timer
QWDPRD	0x13	1/0	0x0000	eQEP Watchdog Period Register
QDECCTL	0x14	1/0	0x0000	eQEP Decoder Control Register
QEPCCTL	0x15	1/0	0x0000	eQEP Control Register
QCAPCTL	0x16	1/0	0x0000	eQEP Capture Control Register
QPOSCTL	0x17	1/0	0x0000	eQEP Position-compare Control Register
QEINT	0x18	1/0	0x0000	eQEP Interrupt Enable Register
QFLG	0x19	1/0	0x0000	eQEP Interrupt Flag Register
QCLR	0x1A	1/0	0x0000	eQEP Interrupt Clear Register
QFRC	0x1B	1/0	0x0000	eQEP Interrupt Force Register
QEPPSTS	0x1C	1/0	0x0000	eQEP Status Register
QCTMR	0x1D	1/0	0x0000	eQEP Capture Timer
QCPRD	0x1E	1/0	0x0000	eQEP Capture Period Register
QCTMRLAT	0x1F	1/0	0x0000	eQEP Capture Timer Latch
QCPRDLAT	0x20	1/0	0x0000	eQEP Capture Period Latch
reserved	0x21 to 0x3F	31/0		

15.3 Quadrature Decoder Unit (QDU)

Figure 15-5 shows a functional block diagram of the QDU.

Figure 15-5. Functional Block Diagram of Decoder Unit



15.3.1 Position Counter Input Modes

Clock and direction input to position counter is selected using QDECCTL[QSRC] bits, based on interface input requirement as follows:

- Quadrature-count mode
- Direction-count mode
- UP-count mode
- DOWN-count mode

15.3.1.1 Quadrature Count Mode

The quadrature decoder generates the direction and clock to the position counter in quadrature count mode.

Direction Decoding— The direction decoding logic of the eQEP circuit determines which one of the sequences (QEPA, QEPB) is the leading sequence and accordingly updates the direction information in QEPSTS[QDF] bit. [Table 15-2](#) and [Figure 15-6](#) show the direction decoding logic in truth table and state machine form. Both edges of the QEPA and QEPB signals are sensed to generate count pulses for the position counter. Therefore, the frequency of the clock generated by the eQEP logic is four times that of each input sequence. [Figure 15-7](#) shows the direction decoding and clock generation from the eQEP input signals.

Table 15-2. Quadrature Decoder Truth Table

Previous Edge	Present Edge	QDIR	QPOS_CNT
QA↑	QB↑	UP	Increment
	QB↓	DOWN	Decrement
	QA↓	TOGGLE	Increment or Decrement
QA↓	QB↓	UP	Increment
	QB↑	DOWN	Decrement
	QA↑	TOGGLE	Increment or Decrement
QB↑	QA↑	DOWN	Increment
	QA↓	UP	Decrement
	QB↓	TOGGLE	Increment or Decrement
QB↓	QA↓	DOWN	Increment
	QA↑	UP	Decrement
	QB↑	TOGGLE	Increment or Decrement

Figure 15-6. Quadrature Decoder State Machine

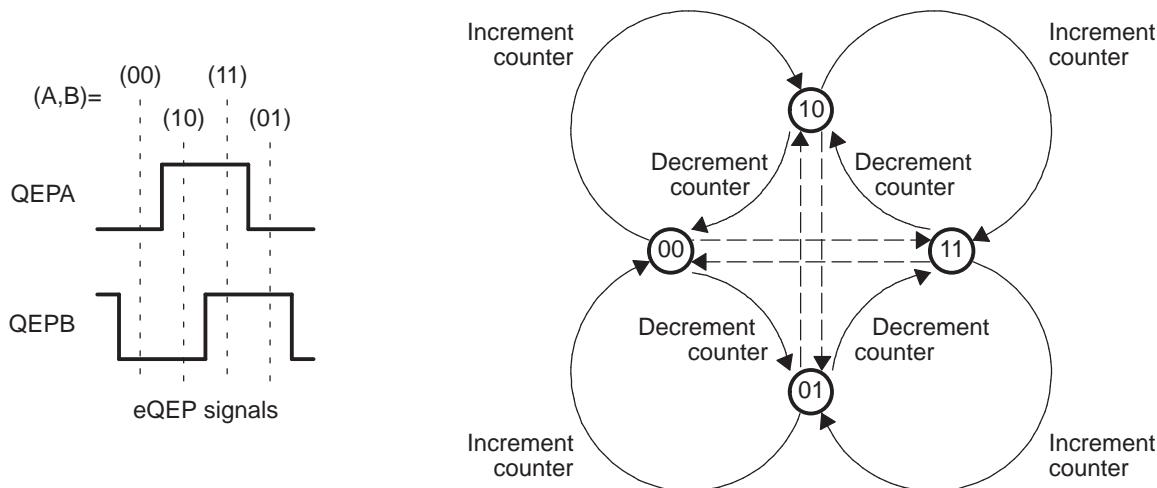
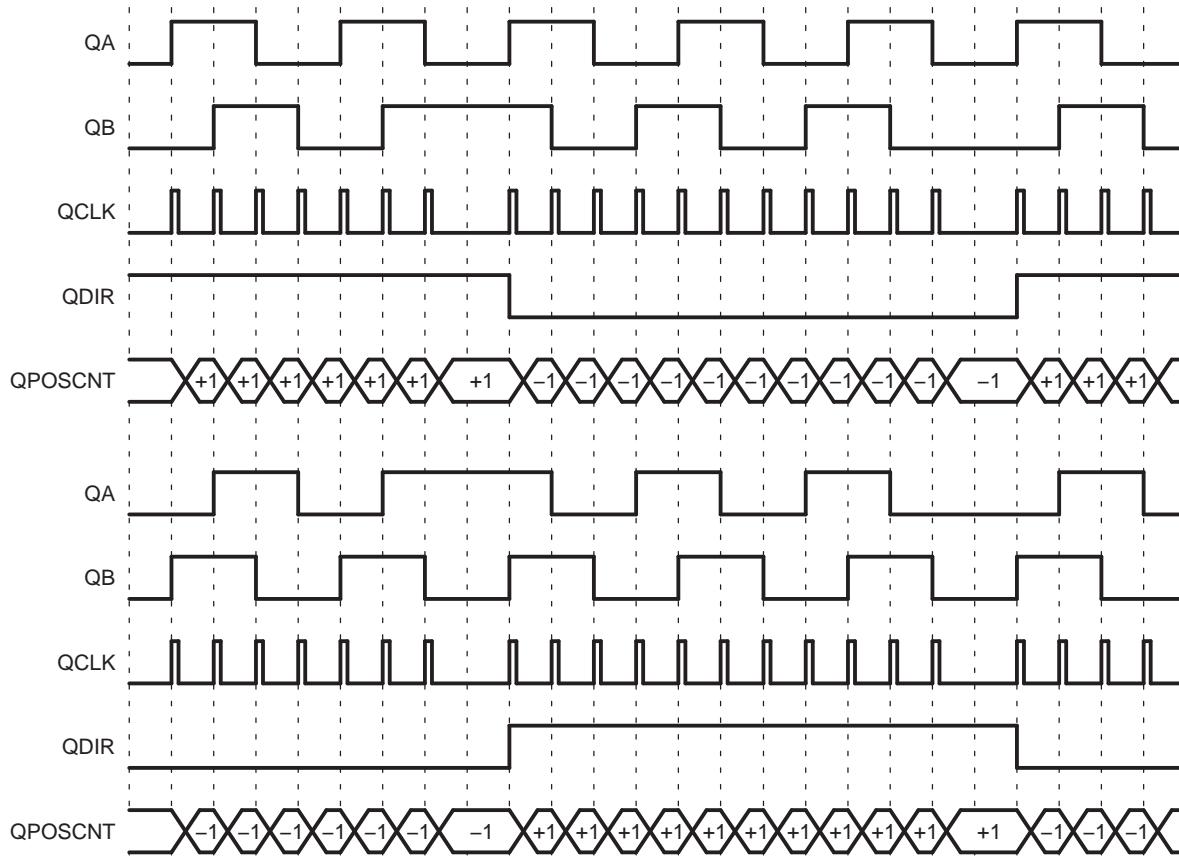


Figure 15-7. Quadrature-clock and Direction Decoding

Phase Error Flag— In normal operating conditions, quadrature inputs QEPA and QEPB will be 90 degrees out of phase. The phase error flag (PHE) is set in the QFLG register when edge transition is detected simultaneously on the QEPA and QEPB signals to optionally generate interrupts. State transitions marked by dashed lines in [Figure 15-6](#) are invalid transitions that generate a phase error.

Count Multiplication— The eQEP position counter provides 4x times the resolution of an input clock by generating a quadrature-clock (QCLK) on the rising/falling edges of both eQEP input clocks (QEPA and QEPB) as shown in [Figure 15-7](#).

Reverse Count— In normal quadrature count operation, QEPA input is fed to the QA input of the quadrature decoder and the QEPB input is fed to the QB input of the quadrature decoder. Reverse counting is enabled by setting the SWAP bit in the QDECCTL register. This will swap the input to the quadrature decoder thereby reversing the counting direction.

15.3.1.2 Direction-count Mode

Some position encoders provide direction and clock outputs, instead of quadrature outputs. In such cases, direction-count mode can be used. QEPA input will provide the clock for position counter and the QEPB input will have the direction information. The position counter is incremented on every rising edge of a QEPA input when the direction input is high and decremented when the direction input is low.

15.3.1.3 Up-Count Mode

The counter direction signal is hard-wired for up count and the position counter is used to measure the frequency of the QEPA input. Clearing the QDECCTL[XCR] bit enables clock generation to the position counter on both edges of the QEPA input, thereby increasing the measurement resolution by 2x factor. In up-count mode, it is recommended that the application not configure QEPB as a GPIO mux option, or ensure that a signal edge is not generated on the QEPB input.

15.3.1.4 Down-Count Mode

The counter direction signal is hardwired for a down count and the position counter is used to measure the frequency of the QEPA input. Setting of the QDECCTL[XCR] bit enables clock generation to the position counter on both edges of a QEPA input, thereby increasing the measurement resolution by 2x factor. In down-count mode, it is recommended that the application not configure QEPB as a GPIO mux option, or ensure that a signal edge is not generated on the QEPB input.

15.3.2 eQEP Input Polarity Selection

Each eQEP input can be inverted using QDECCTL[8:5] control bits. As an example, setting of QDECCTL[QIP] bit will invert the index input.

15.3.3 Position-Compare Sync Output

The enhanced eQEP peripheral includes a position-compare unit that is used to generate the position-compare sync signal on compare match between the position counter register (QPOS_CNT) and the position-compare register (QPOS_CMP). This sync signal can be output using an index pin or strobe pin of the EQEP peripheral.

Setting the QDECCTL[SOEN] bit enables the position-compare sync output and the QDECCTL[SPSEL] bit selects either an eQEP index pin or an eQEP strobe pin.

15.4 Position Counter and Control Unit (PCCU)

The position counter and control unit provides two configuration registers (QEPCTL and QPOSCTL) for setting up position counter operational modes, position counter initialization/latch modes and position-compare logic for sync signal generation.

15.4.1 Position Counter Operating Modes

Position counter data may be captured in different manners. In some systems, the position counter is accumulated continuously for multiple revolutions and the position counter value provides the position information with respect to the known reference. An example of this is the quadrature encoder mounted on the motor controlling the print head in the printer. Here the position counter is reset by moving the print head to the home position and then position counter provides absolute position information with respect to home position.

In other systems, the position counter is reset on every revolution using index pulse and position counter provides rotor angle with respect to index pulse position.

Position counter can be configured to operate in following four modes

- Position Counter Reset on Index Event
- Position Counter Reset on Maximum Position
- Position Counter Reset on the first Index Event
- Position Counter Reset on Unit Time Out Event (Frequency Measurement)

In all the above operating modes, position counter is reset to 0 on overflow and to QPOSMAX register value on underflow. Overflow occurs when the position counter counts up after QPOSMAX value.

Underflow occurs when position counter counts down after "0". Interrupt flag is set to indicate overflow/underflow in QFLG register.

15.4.1.1 Position Counter Reset on Index Event (QEPCTL[PCRM]=00)

If the index event occurs during the forward movement, then position counter is reset to 0 on the next eQEP clock. If the index event occurs during the reverse movement, then the position counter is reset to the value in the QPOSMAX register on the next eQEP clock.

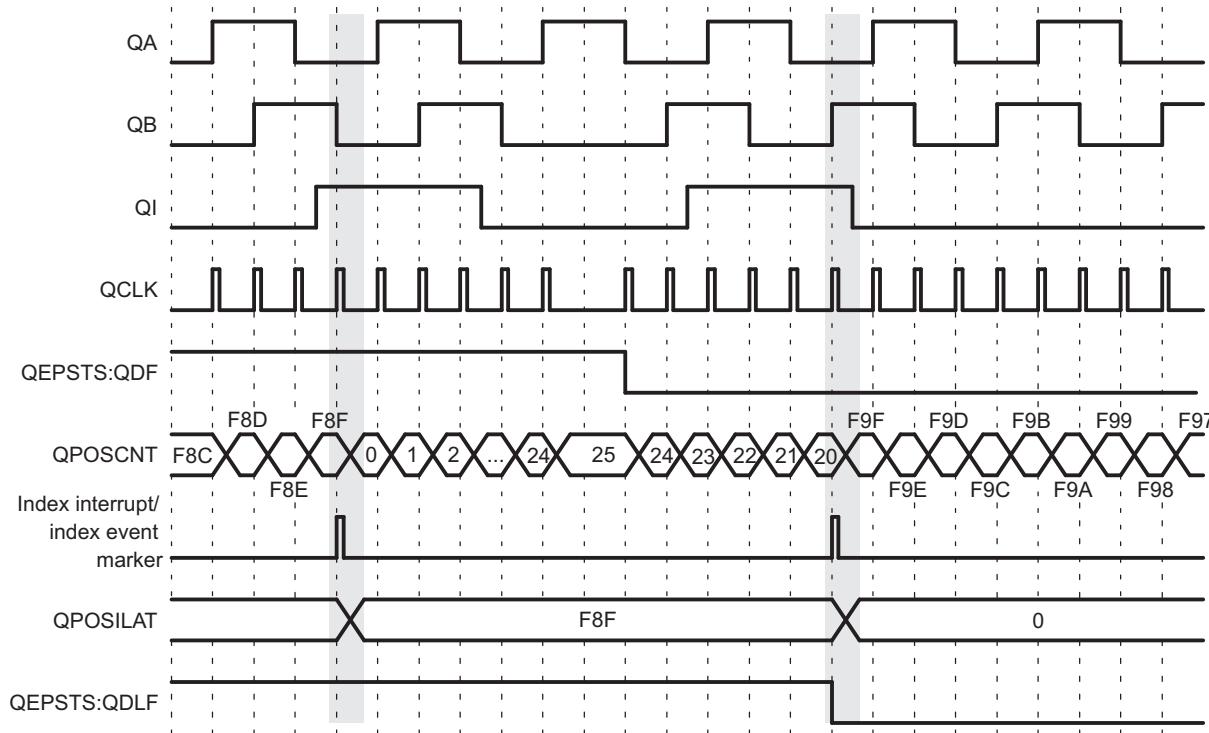
First index marker is defined as the quadrature edge following the first index edge. The eQEP peripheral records the occurrence of the first index marker (QEPSTS[FIMF]) and direction on the first index event marker (QEPSTS[FIDF]) in QEPSTS registers, it also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for index event reset operation.

For example, if the first reset operation occurs on the falling edge of QEPB during the forward direction, then all the subsequent reset must be aligned with the falling edge of QEPB for the forward rotation and on the rising edge of QEPB for the reverse rotation as shown in [Figure 15-8](#).

The position-counter value is latched to the QPOSILAT register and direction information is recorded in the QEPSTS[QDLF] bit on every index event marker. The position-counter error flag (QEPSTS[PCEF]) and error interrupt flag (QFLG[PCE]) are set if the latched value is not equal to 0 or QPOSMAX. The position-counter error flag (QEPSTS[PCEF]) is updated on every index event marker and an interrupt flag (QFLG[PCE]) will be set on error that can be cleared only through software.

The index event latch configuration QEPCTL[IEL] bits are ignored in this mode and position counter error flag/interrupt flag are generated only in index event reset mode.

Figure 15-8. Position Counter Reset by Index Pulse for 1000 Line Encoder (QPOSMAX = 3999 or 0xF9F)

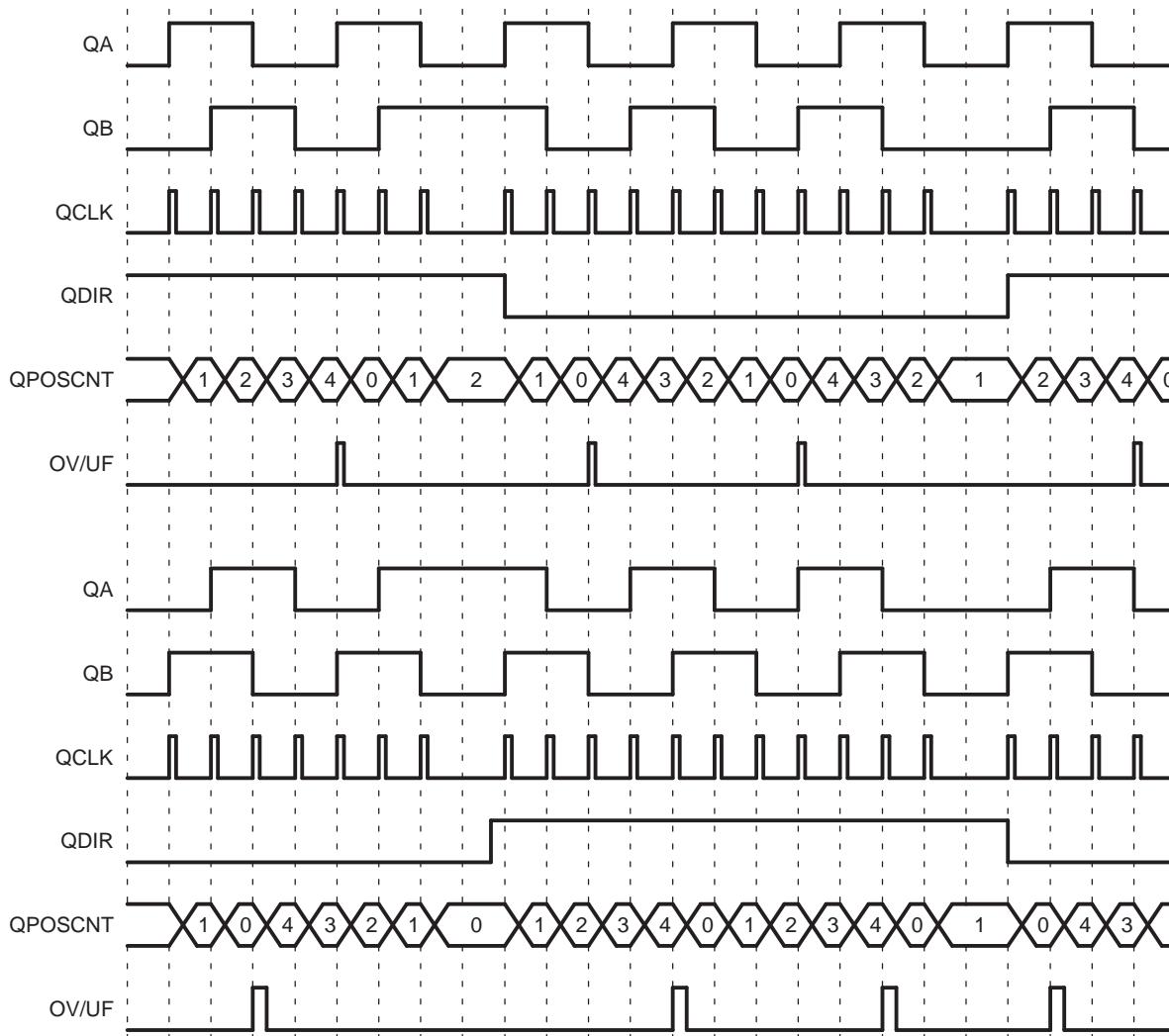


15.4.1.2 Position Counter Reset on Maximum Position (QEPCTL[PCRM]=01)

If the position counter is equal to QPOSMAX, then the position counter is reset to 0 on the next eQEP clock for forward movement and position counter overflow flag is set. If the position counter is equal to ZERO, then the position counter is reset to QPOSMAX on the next QEP clock for reverse movement and position counter underflow flag is set. [Figure 15-9](#) shows the position counter reset operation in this mode.

First index marker is defined as the quadrature edge following the first index edge. The eQEP peripheral records the occurrence of the first index marker (QEPSTS[FIMF]) and direction on the first index event marker (QEPSTS[FIDF]) in the QEPSTS registers; it also remembers the quadrature edge on the first index marker so that the same relative quadrature transition is used for the software index marker (QEPCTL[IEL]=11).

Figure 15-9. Position Counter Underflow/Overflow (QPOS MAX = 4)



15.4.1.3 Position Counter Reset on the First Index Event (QEPCTL[PCRM] = 10)

If the index event occurs during forward movement, then the position counter is reset to 0 on the next eQEP clock. If the index event occurs during the reverse movement, then the position counter is reset to the value in the QPOS MAX register on the next eQEP clock. Note that this is done only on the first occurrence and subsequently the position counter value is not reset on an index event; rather, it is reset based on maximum position as described in Section [Section 15.4.1.2](#).

First index marker is defined as the quadrature edge following the first index edge. The eQEP peripheral records the occurrence of the first index marker (QEPSTS[FIMF]) and direction on the first index event marker (QEPSTS[FIDF]) in QEPSTS registers; it also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for software index marker (QEPCTL[IEL]=11).

15.4.1.4 Position Counter Reset on Unit Time out Event (QEPCTL[PCRM] = 11)

In this mode, the QPOSCNT value is latched to the QPOSILAT register and then the QPOSCNT is reset (to 0 or QPOSMAX, depending on the direction mode selected by QDECCTL[QSRC] bits on a unit time event). This is useful for frequency measurement.

15.4.2 Position Counter Latch

The eQEP index and strobe input can be configured to latch the position counter (QPOSCNT) into QPOSILAT and QPOSSLAT, respectively, on occurrence of a definite event on these pins.

15.4.2.1 Index Event Latch

In some applications, it may not be desirable to reset the position counter on every index event and instead it may be required to operate the position counter in full 32-bit mode (QEPCTL[PCRM] = 01 and QEPCTL[PCRM] = 10 modes).

In such cases, the eQEP position counter can be configured to latch on the following events and direction information is recorded in the QEPSTS[QDLF] bit on every index event marker.

- Latch on Rising edge (QEPCTL[IEL]=01)
- Latch on Falling edge (QEPCTL[IEL]=10)
- Latch on Index Event Marker (QEPCTL[IEL]=11)

This is particularly useful as an error checking mechanism to check if the position counter accumulated the correct number of counts between index events. As an example, the 1000-line encoder must count 4000 times when moving in the same direction between the index events.

The index event latch interrupt flag (QFLG[IEL]) is set when the position counter is latched to the QPOSILAT register.

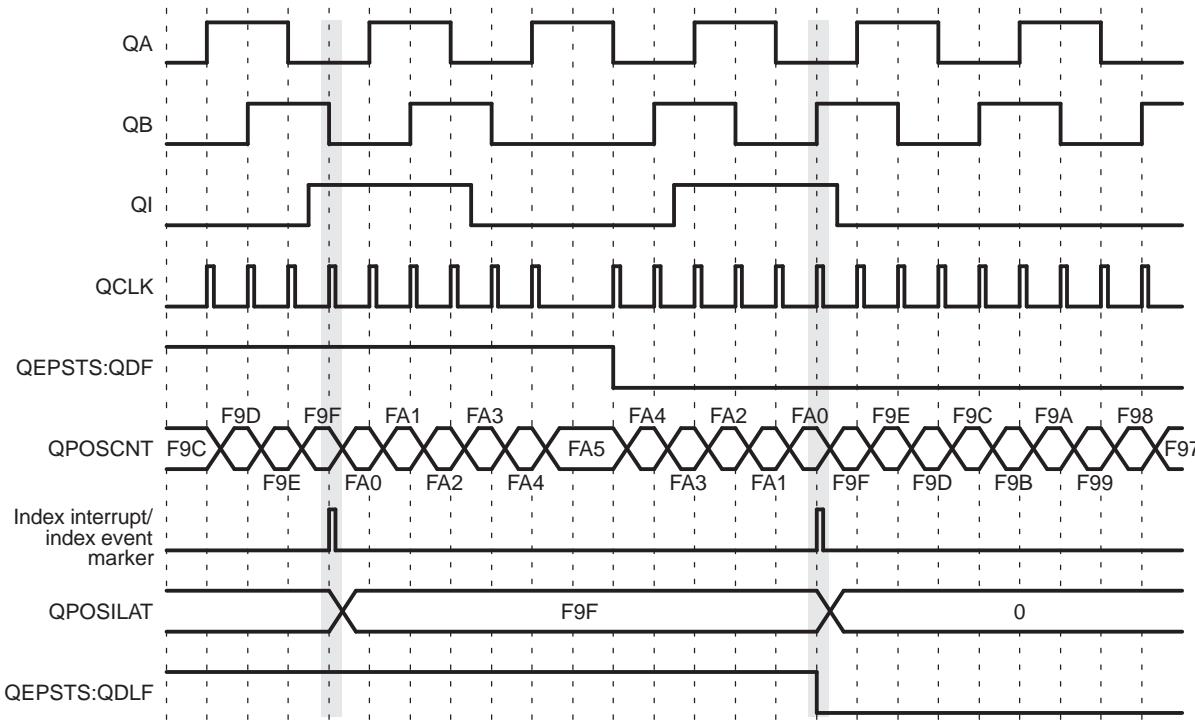
Latch on Rising Edge (QEPCTL[IEL]=01)— The position counter value (QPOSCNT) is latched to the QPOSILAT register on every rising edge of an index input.

Latch on Falling Edge (QEPCTL[IEL] = 10)— The position counter value (QPOSCNT) is latched to the QPOSILAT register on every falling edge of index input.

Latch on Index Event Marker/Software Index Marker (QEPCTL[IEL] = 11)— The first index marker is defined as the quadrature edge following the first index edge. The eQEP peripheral records the occurrence of the first index marker (QEPSTS[FIMF]) and direction on the first index event marker (QEPSTS[FIDF]) in the QEPSTS registers. It also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for latching the position counter (QEPCTL[IEL]=11).

Figure 15-10 shows the position counter latch using an index event marker.

Figure 15-10. Software Index Marker for 1000-line Encoder (QEPCTL[IEL] = 1)



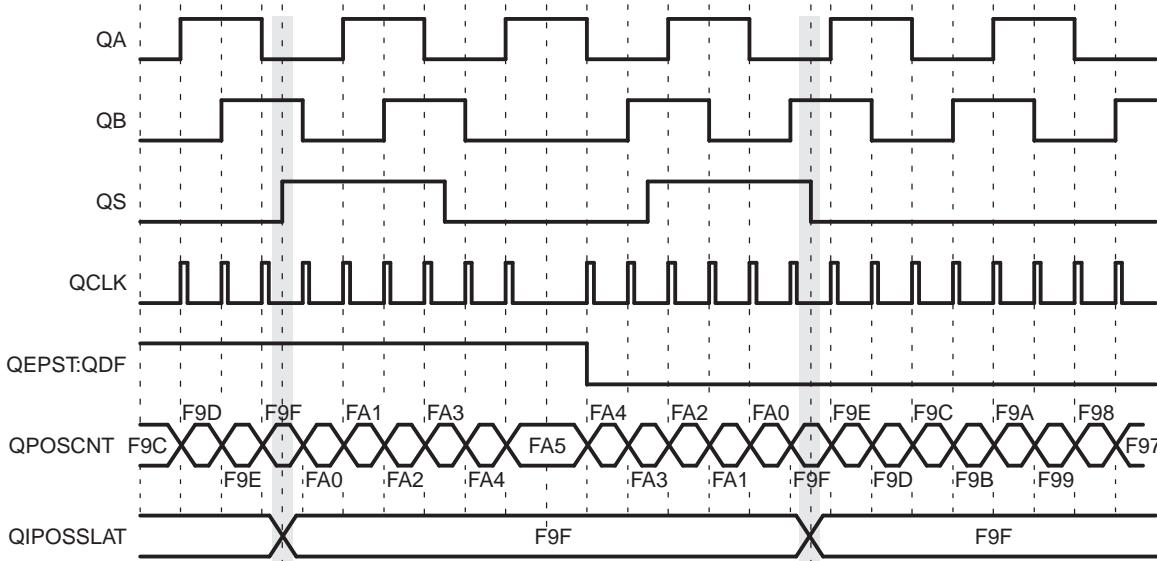
15.4.2.2 Strobe Event Latch

The position-counter value is latched to the QPOSSLAT register on the rising edge of the strobe input by clearing the QEPCCTL[SEL] bit.

If the QEPCTL[SEL] bit is set, then the position counter value is latched to the QPOSSLAT register on the rising edge of the strobe input for forward direction and on the falling edge of the strobe input for reverse direction as shown in Figure 15-11.

The strobe event latch interrupt flag (QFLG[SEL]) is set when the position counter is latched to the QPOSSLAT register.

Figure 15-11. Strobe Event Latch (QEPCTL[SEL] = 1)



15.4.3 Position Counter Initialization

The position counter can be initialized using following events:

- Index event
- Strobe event
- Software initialization

Index Event Initialization (IEI)— The QEPI index input can be used to trigger the initialization of the position counter at the rising or falling edge of the index input. If the QEPCTL[IEI] bits are 10, then the position counter (QPOS_CNT) is initialized with a value in the QPOSINIT register on the rising edge of index input. Conversely, if the QEPCTL[IEI] bits are 11, initialization will be on the falling edge of the index input.

Strobe Event Initialization (SEI)— If the QEPCTL[SEI] bits are 10, then the position counter is initialized with a value in the QPOSINIT register on the rising edge of strobe input.

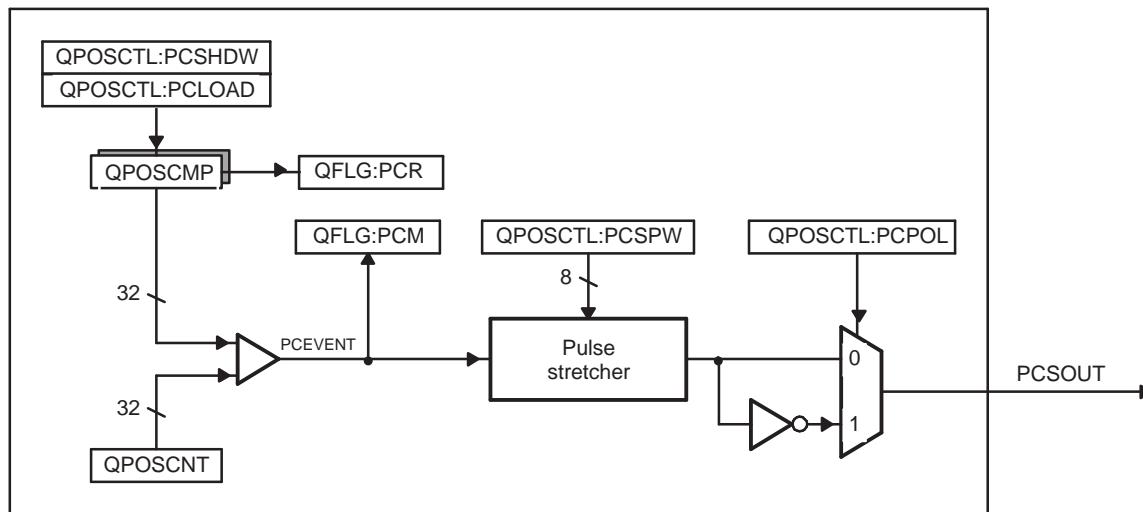
If QEPCTL[SEL] bits are 11, then the position counter is initialized with a value in the QPOSINIT register on the rising edge of strobe input for forward direction and on the falling edge of strobe input for reverse direction.

Software Initialization (SWI)— The position counter can be initialized in software by writing a 1 to the QEPCTL[SWI] bit. This bit is not automatically cleared. While the bit is still set, if a 1 is written to it again, the position counter will be re-initialized.

15.4.4 eQEP Position-compare Unit

The eQEP peripheral includes a position-compare unit that is used to generate a sync output and/or interrupt on a position-compare match. [Figure 15-12](#) shows a diagram. The position-compare (QPOS_CMP) register is shadowed and shadow mode can be enabled or disabled using the QPOSCTL[PSSHDW] bit. If the shadow mode is not enabled, the CPU writes directly to the active position compare register.

Figure 15-12. eQEP Position-compare Unit



In shadow mode, you can configure the position-compare unit (QPOSCTL[PCLOAD]) to load the shadow register value into the active register on the following events and to generate the position-compare ready (QFLG[PCR]) interrupt after loading.

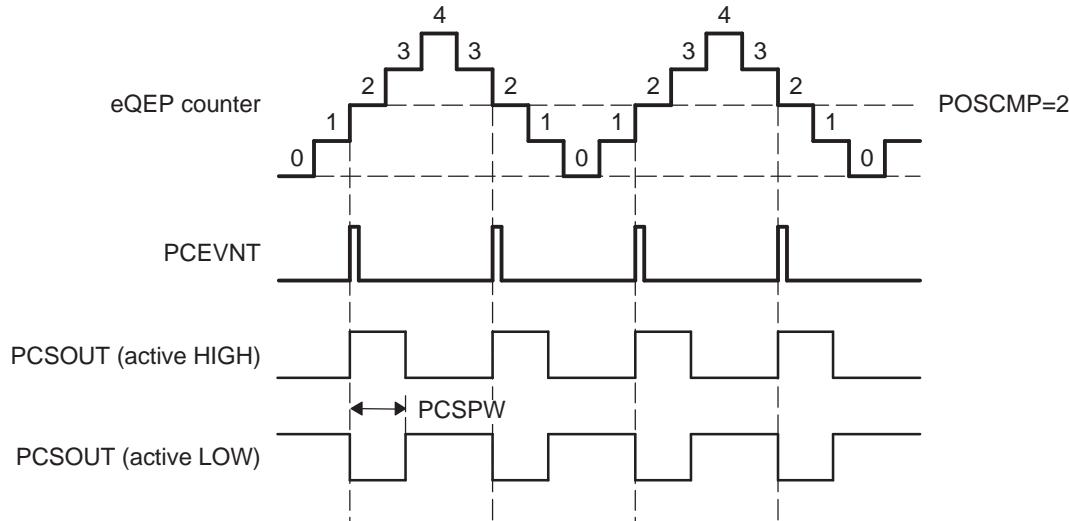
- Load on compare match
- Load on position-counter zero event

The position-compare match (QFLG[PCM]) is set when the position-counter value (QPOS_CNT) matches with the active position-compare register (QPOS_CMP) and the position-compare sync output of the programmable pulse width is generated on compare match to trigger an external device.

For example, if QPOSCMP = 2, the position-compare unit generates a position-compare event on 1 to 2 transitions of the eQEP position counter for forward counting direction and on 3 to 2 transitions of the eQEP position counter for reverse counting direction (see [Figure 15-13](#)).

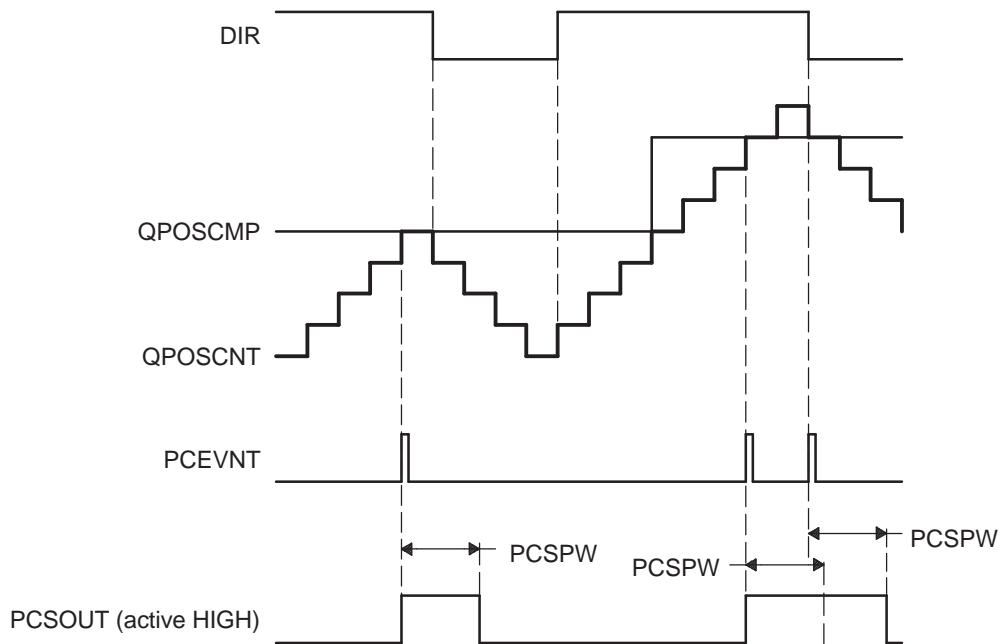
See the register section for the layout of the eQEP Position-Compare Control Register (QPOSCTL) and description of the QPOSCTL bit fields.

Figure 15-13. eQEP Position-compare Event Generation Points



The pulse stretcher logic in the position-compare unit generates a programmable position-compare sync pulse output on the position-compare match. In the event of a new position-compare match while a previous position-compare pulse is still active, then the pulse stretcher generates a pulse of specified duration from the new position-compare event as shown in [Figure 15-14](#).

Figure 15-14. eQEP Position-compare Sync Output Pulse Stretcher



15.5 eQEP Edge Capture Unit

The eQEP peripheral includes an integrated edge capture unit to measure the elapsed time between the unit position events as shown in [Figure 15-15](#). This feature is typically used for low speed measurement using the following equation:

$$v(k) = \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \quad (4)$$

where,

- X - Unit position is defined by integer multiple of quadrature edges (see [Figure 15-16](#))
- ΔT - Elapsed time between unit position events
- $v(k)$ - Velocity at time instant "k"

The eQEP capture timer (QCTMR) runs from prescaled SYSCLKOUT and the prescaler is programmed by the QCAPCTL[CCPS] bits. The capture timer (QCTMR) value is latched into the capture period register (QCPRD) on every unit position event and then the capture timer is reset, a flag is set in QEPSTS:UPEVNT to indicate that new value is latched into the QCPRD register. Software can check this status flag before reading the period register for low speed measurement and clear the flag by writing 1.

Time measurement (ΔT) between unit position events will be correct if the following conditions are met:

- No more than 65,535 counts have occurred between unit position events.
- No direction change between unit position events.

The capture unit sets the eQEP overflow error flag (QEPSTS[COEF]) in the event of capture timer overflow between unit position events. If a direction change occurs between the unit position events, then an error flag is set in the status register (QEPSTS[CDEF]).

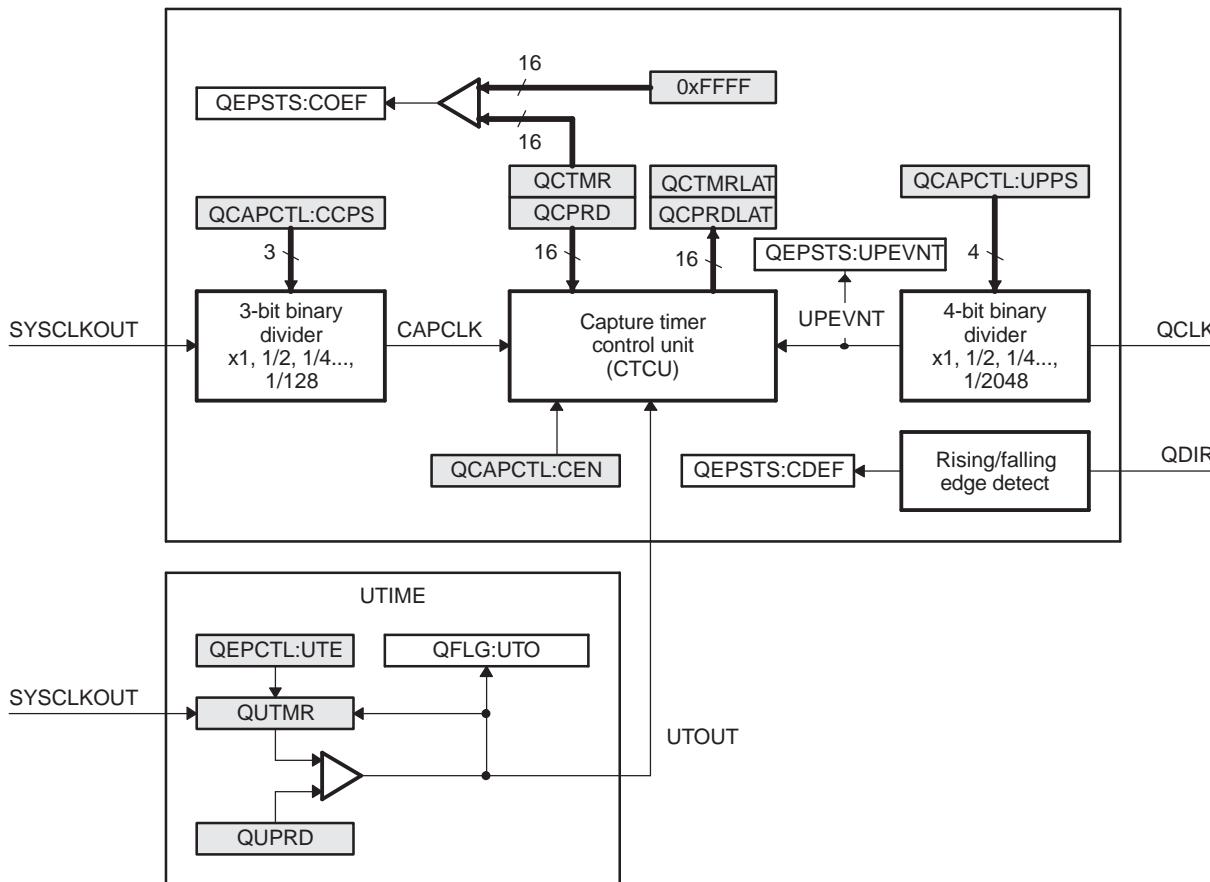
Capture Timer (QCTMR) and Capture period register (QCPRD) can be configured to latch on following events.

- CPU read of QPOS_CNT register
- Unit time-out event

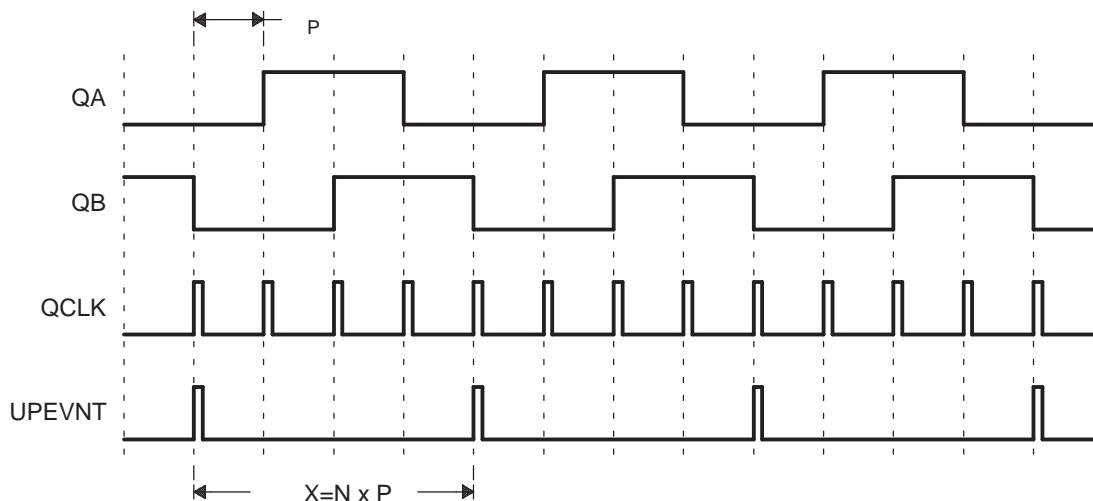
If the QEPCTL[QCLM] bit is cleared, then the capture timer and capture period values are latched into the QCTMRLAT and QCPRDLAT registers, respectively, when the CPU reads the position counter (QPOS_CNT).

If the QEPCTL[QCLM] bit is set, then the position counter, capture timer, and capture period values are latched into the QPOS LAT, QCTMRLAT and QCPRDLAT registers, respectively, on unit time out.

[Figure 15-17](#) shows the capture unit operation along with the position counter.

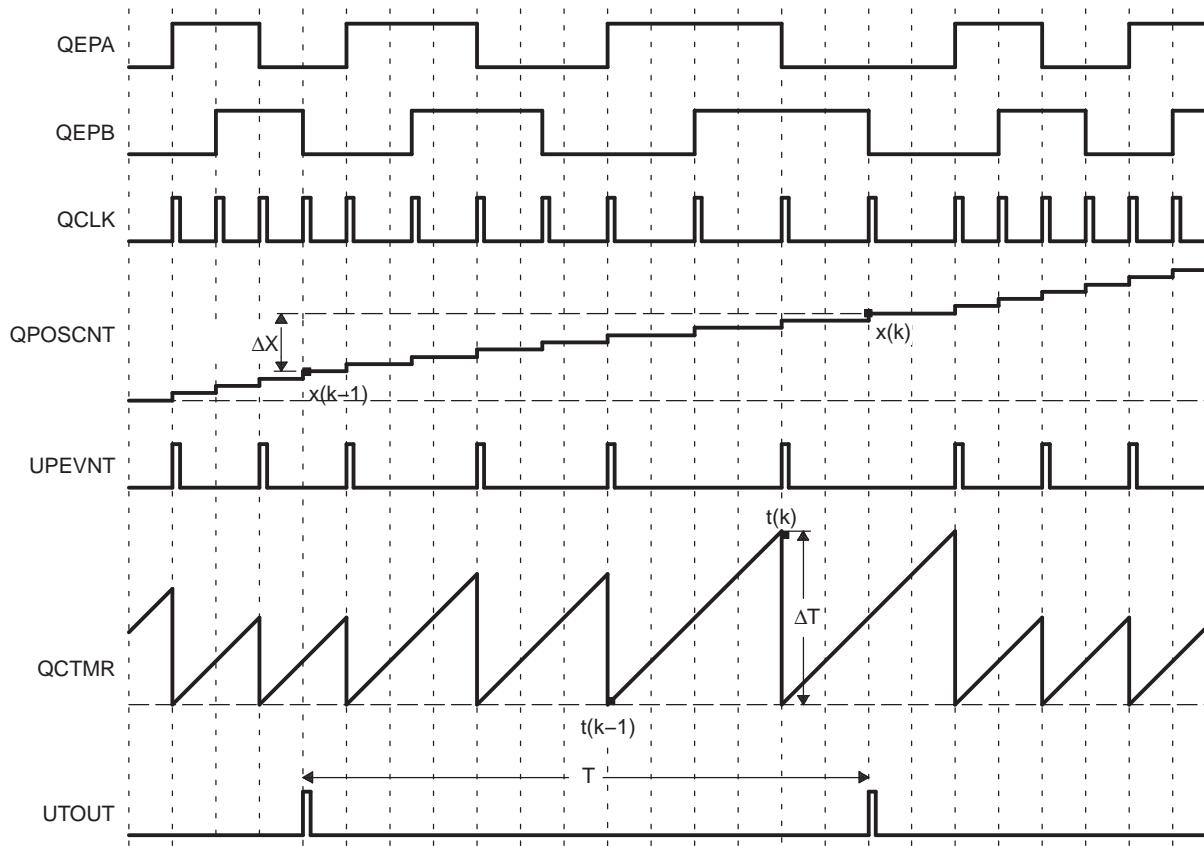
Figure 15-15. eQEP Edge Capture Unit


NOTE: The QCAPCTL[UPPS] prescaler should not be modified dynamically (such as switching the unit event prescaler from QCLK/4 to QCLK/8). Doing so may result in undefined behavior. The QCAPCTL[CPPS] prescaler can be modified dynamically (such as switching CAPCLK prescaling mode from SYSCLK/4 to SYSCLK/8) only after the capture unit is disabled.

Figure 15-16. Unit Position Event for Low Speed Measurement (QCAPCTL[UPPS] = 0010)


A N - Number of quadrature periods selected using QCAPCTL[UPPS] bits

Figure 15-17. eQEP Edge Capture Unit - Timing Details



Velocity Calculation Equations:

$$v(k) = \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T} \quad (5)$$

where

$v(k)$: Velocity at time instant k

$x(k)$: Position at time instant k

$x(k-1)$: Position at time instant $k-1$

T : Fixed unit time or inverse of velocity calculation rate

ΔX : Incremental position movement in unit time

X : Fixed unit position

ΔT : Incremental time elapsed for unit position movement

$t(k)$: Time instant "k"

$t(k-1)$: Time instant "k-1"

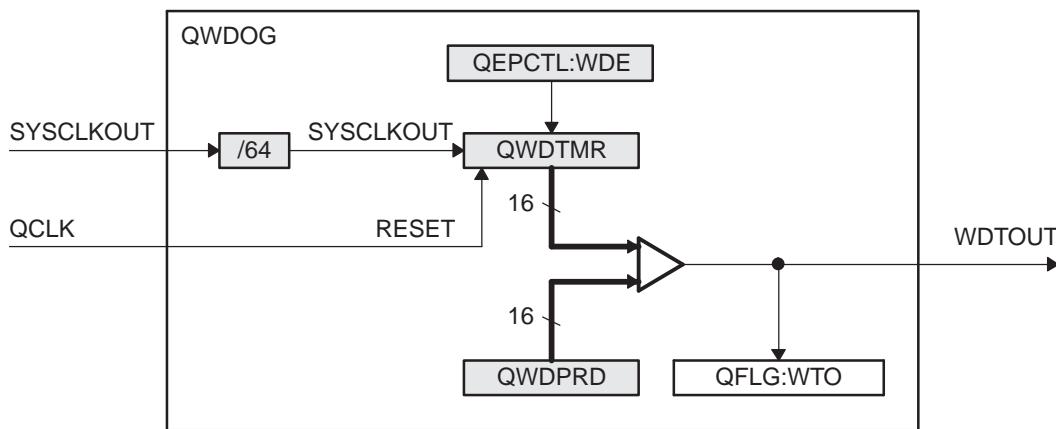
Unit time (T) and unit period(X) are configured using the QUPRD and QCAPCTL[UPPS] registers. Incremental position output and incremental time output is available in the QPOS LAT and QCPRDLAT registers.

Parameter	Relevant Register to Configure or Read the Information
T	Unit Period Register (QUPRD)
ΔX	Incremental Position = QPOSLAT(k) - QPOSLAT(K-1)
X	Fixed unit position defined by sensor resolution and ZCAPCTL[UPPS] bits
ΔT	Capture Period Latch (QCPRDLAT)

15.6 eQEP Watchdog

The eQEP peripheral contains a 16-bit watchdog timer that monitors the quadrature-clock to indicate proper operation of the motion-control system. The eQEP watchdog timer is clocked from SYSCLKOUT/64 and the quadrature clock event (pulse) resets the watchdog timer. If no quadrature-clock event is detected until a period match (QWDPRD = QWDTMR), then the watchdog timer will time out and the watchdog interrupt flag will be set (QFLG[WTO]). The time-out value is programmable through the watchdog period register (QWDPRD).

Figure 15-18. eQEP Watchdog Timer

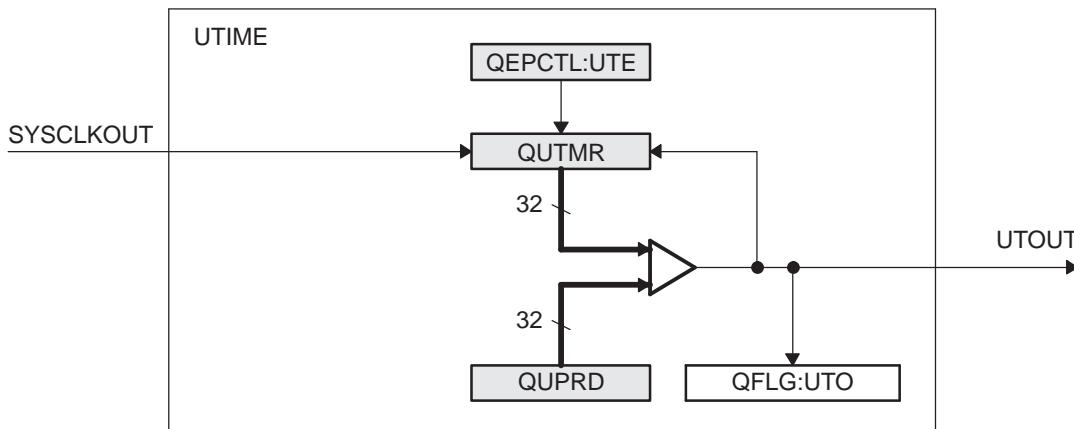


15.7 Unit Timer Base

The eQEP peripheral includes a 32-bit timer (QUTMR) that is clocked by SYSCLKOUT to generate periodic interrupts for velocity calculations. The unit time out interrupt is set (QFLG[UTO]) when the unit timer (QUTMR) matches the unit period register (QUPRD).

The eQEP peripheral can be configured to latch the position counter, capture timer, and capture period values on a unit time out event so that latched values are used for velocity calculation as described in Section [Section 15.5](#).

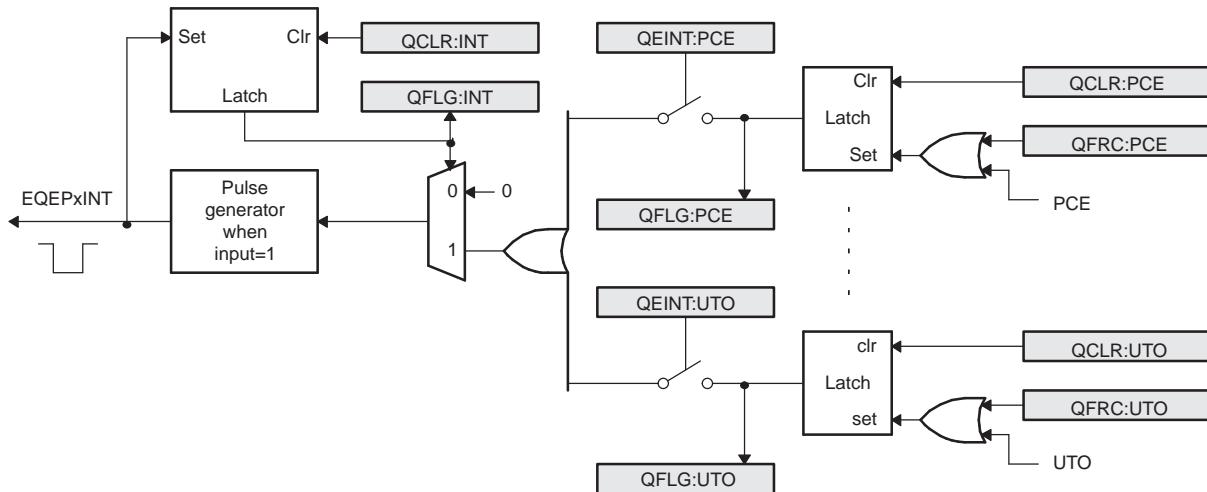
Figure 15-19. eQEP Unit Time Base



15.8 eQEP Interrupt Structure

Figure 15-20 shows how the interrupt mechanism works in the EQEP module.

Figure 15-20. EQEP Interrupt Generation



Eleven interrupt events (PCE, PHE, QDC, WTO, PCU, PCO, PCR, PCM, SEL, IEL and UTO) can be generated. The interrupt control register (QEINT) is used to enable/disable individual interrupt event sources. The interrupt flag register (QFLG) indicates if any interrupt event has been latched and contains the global interrupt flag bit (INT). An interrupt pulse is generated only to the PIE if any of the interrupt events is enabled, the flag bit is 1 and the INT flag bit is 0. The interrupt service routine will need to clear the global interrupt flag bit and the serviced event, via the interrupt clear register (QCLR), before any other interrupt pulses are generated. You can force an interrupt event by way of the interrupt force register (QFRC), which is useful for test purposes.

15.9 Registers

15.9.1 eQEP Base Addresses

Table 15-3. eQEP Base Address Table

Device Registers	Register Name	Start Address	End Address
EQep1Regs	EQEP_REGS	0x0000_5100	0x0000_513F
EQep2Regs	EQEP_REGS	0x0000_5140	0x0000_517F
EQep3Regs	EQEP_REGS	0x0000_5180	0x0000_51BF

15.9.2 EQEP_REGS Registers

Table 15-4 lists the memory-mapped registers for the EQEP_REGS. All register offset addresses not listed in **Table 15-4** should be considered as reserved locations and the register contents should not be modified.

Table 15-4. EQEP_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	QPOSCNT	Position Counter	Section 15.9.2.1	
2h	QPOSINIT	Position Counter Init	Section 15.9.2.2	
4h	QPOSMAX	Maximum Position Count	Section 15.9.2.3	
6h	QPOSCMP	Position Compare	Section 15.9.2.4	
8h	QPOSILAT	Index Position Latch	Section 15.9.2.5	
Ah	QPOSSLAT	Strobe Position Latch	Section 15.9.2.6	
Ch	QPOSLAT	Position Latch	Section 15.9.2.7	
Eh	QUTMR	QEP Unit Timer	Section 15.9.2.8	
10h	QUPRD	QEP Unit Period	Section 15.9.2.9	
12h	QWDTMR	QEP Watchdog Timer	Section 15.9.2.10	
13h	QWDPRD	QEP Watchdog Period	Section 15.9.2.11	
14h	QDECCTL	Quadrature Decoder Control	Section 15.9.2.12	
15h	QEPCCTL	QEP Control	Section 15.9.2.13	
16h	QCAPCTL	Quaudrature Capture Control	Section 15.9.2.14	
17h	QPOSCTL	Position Compare Control	Section 15.9.2.15	
18h	QEINT	QEP Interrupt Control	Section 15.9.2.16	
19h	QFLG	QEP Interrupt Flag	Section 15.9.2.17	
1Ah	QCLR	QEP Interrupt Clear	Section 15.9.2.18	
1Bh	QFRC	QEP Interrupt Force	Section 15.9.2.19	
1Ch	QEPSTS	QEP Status	Section 15.9.2.20	
1Dh	QCTMR	QEP Capture Timer	Section 15.9.2.21	
1Eh	QCPRD	QEP Capture Period	Section 15.9.2.22	
1Fh	QCTMRLAT	QEP Capture Latch	Section 15.9.2.23	
20h	QCPRDLAT	QEP Capture Period Latch	Section 15.9.2.24	

15.9.2.1 QPOSCNT Register (offset = 0h) [reset = 0h]

QPOSCNT is shown in [Figure 15-21](#) and described in [Table 15-5](#).

Position Counter

Figure 15-21. QPOSCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-5. QPOSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSCNT	R/W	0h	<p>Position Counter</p> <p>This 32-bit position counter register counts up/down on every eQEP pulse based on direction</p> <p>input. This counter acts as a position integrator whose count value is proportional to position from a give reference point.</p>

15.9.2.2 QPOSINIT Register (offset = 2h) [reset = 0h]

QPOSINIT is shown in [Figure 15-22](#) and described in [Table 15-6](#).

Position Counter Init

Figure 15-22. QPOSINIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSINIT																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-6. QPOSINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSINIT	R/W	0h	<p>Position Counter Init</p> <p>This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes.</p>

15.9.2.3 QPOSMAX Register (offset = 4h) [reset = 0h]

QPOSMAX is shown in [Figure 15-23](#) and described in [Table 15-7](#).

Maximum Position Count

Figure 15-23. QPOSMAX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSMAX																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-7. QPOSMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSMAX	R/W	0h	Maximum Position Count This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes.

15.9.2.4 QPOSCMP Register (offset = 6h) [reset = 0h]

QPOSCMP is shown in [Figure 15-24](#) and described in [Table 15-8](#).

Position Compare

Figure 15-24. QPOSCMP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSCMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

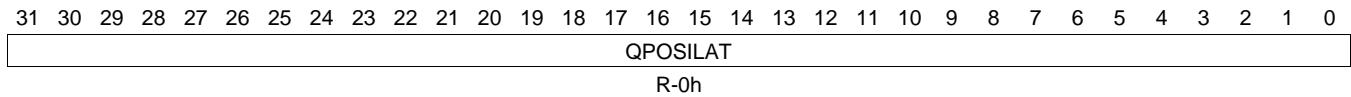
Table 15-8. QPOSCMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSCMP	R/W	0h	<p>Position Compare</p> <p>The position-compare value in this register is compared with the position counter (QPOSCNT) to generate sync output and/or interrupt on compare match.</p>

15.9.2.5 QPOSILAT Register (offset = 8h) [reset = 0h]

QPOSILAT is shown in [Figure 15-25](#) and described in [Table 15-9](#).

Index Position Latch

Figure 15-25. QPOSILAT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-9. QPOSILAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSILAT	R	0h	Index Position Latch The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits.

15.9.2.6 QPOSSLAT Register (offset = Ah) [reset = 0h]QPOSSLAT is shown in [Figure 15-26](#) and described in [Table 15-10](#).

Strobe Position Latch

Figure 15-26. QPOSSLAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSSLAT																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-10. QPOSSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSSLAT	R	0h	<p>Strobe Position Latch</p> <p>The position-counter value is latched into this register on strobe event as defined by the QEPCTL[SEL] bits.</p>

15.9.2.7 QPOSLAT Register (offset = Ch) [reset = 0h]

QPOSLAT is shown in [Figure 15-27](#) and described in [Table 15-11](#).

Position Latch

Figure 15-27. QPOSLAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSLAT																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-11. QPOSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSLAT	R	0h	Position Latch The position-counter value is latched into this register on unit time out event.

15.9.2.8 QUTMR Register (offset = Eh) [reset = 0h]QUTMR is shown in [Figure 15-28](#) and described in [Table 15-12](#).

QEP Unit Timer

Figure 15-28. QUTMR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUTMR																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-12. QUTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QUTMR	R/W	0h	<p>QEP Unit Timer</p> <p>This register acts as time base for unit time event generation. When this timer value matches with unit time period value, unit time event is generated.</p>

15.9.2.9 QUPRD Register (offset = 10h) [reset = 0h]

QUPRD is shown in [Figure 15-29](#) and described in [Table 15-13](#).

QEP Unit Period

Figure 15-29. QUPRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUPRD																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-13. QUPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QUPRD	R/W	0h	<p>QEP Unit Period</p> <p>This register contains the period count for unit timer to generate periodic unit time events to latch the eQEP position information at periodic interval and optionally to generate interrupt. Writes to this register should always be full 32-bit writes.</p>

15.9.2.10 QWDTMR Register (offset = 12h) [reset = 0h]QWDTMR is shown in [Figure 15-30](#) and described in [Table 15-14](#).

QEP Watchdog Timer

Figure 15-30. QWDTMR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QWDTMR															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

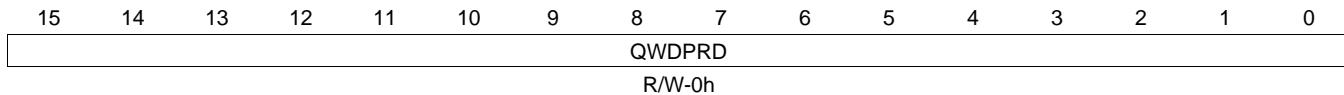
Table 15-14. QWDTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QWDTMR	R/W	0h	<p>QEP Watchdog Timer</p> <p>This register acts as time base for watch dog to detect motor stalls. When this timer value matches with watch dog period value, watch dog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion.</p>

15.9.2.11 QWDPRD Register (offset = 13h) [reset = 0h]

QWDPRD is shown in [Figure 15-31](#) and described in [Table 15-15](#).

QEP Watchdog Period

Figure 15-31. QWDPRD Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-15. QWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QWDPRD	R/W	0h	<p>QEP Watchdog Period</p> <p>This register contains the time-out count for the eQEP peripheral watch dog timer.</p> <p>When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated.</p>

15.9.2.12 QDECCTL Register (offset = 14h) [reset = 0h]

QDECCTL is shown in [Figure 15-32](#) and described in [Table 15-16](#).

Quadrature Decoder Control

Figure 15-32. QDECCTL Register

15	14	13	12	11	10	9	8
QSRC	SOEN	SPSEL	XCR	SWAP	IGATE	QAP	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
QBP	QIP	QSP		RESERVED			
R/W-0h	R/W-0h	R/W-0h		R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-16. QDECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	QSRC	R/W	0h	Position-counter source selection 0h (R/W) = Quadrature count mode (QCLK = iCLK, QDIR = iDIR) 1h (R/W) = Direction-count mode (QCLK = xCLK, QDIR = xDIR) 2h (R/W) = UP count mode for frequency measurement (QCLK = xCLK, QDIR = 1) 3h (R/W) = DOWN count mode for frequency measurement (QCLK = xCLK, QDIR = 0)
13	SOEN	R/W	0h	Sync output-enable 0h (R/W) = Disable position-compare sync output 1h (R/W) = Enable position-compare sync output
12	SPSEL	R/W	0h	Sync output pin selection 0h (R/W) = Index pin is used for sync output 1h (R/W) = Strobe pin is used for sync output
11	XCR	R/W	0h	External Clock Rate 0h (R/W) = 2x resolution: Count the rising/falling edge 1h (R/W) = 1x resolution: Count the rising edge only
10	SWAP	R/W	0h	CLK/DIR Signal Source for Position Counter 0h (R/W) = Quadrature-clock inputs are not swapped 1h (R/W) = Quadrature-clock inputs are swapped
9	IGATE	R/W	0h	Index pulse gating option 0h (R/W) = Disable gating of Index pulse 1h (R/W) = Gate the index pin with strobe
8	QAP	R/W	0h	QEPA input polarity 0h (R/W) = No effect 1h (R/W) = Negates QEPA input
7	QBP	R/W	0h	QEpb input polarity 0h (R/W) = No effect 1h (R/W) = Negates QEpb input
6	QIP	R/W	0h	QEPI input polarity 0h (R/W) = No effect 1h (R/W) = Negates QEPI input
5	QSP	R/W	0h	QEps input polarity 0h (R/W) = No effect 1h (R/W) = Negates QEps input
4-0	RESERVED	R	0h	Reserved

15.9.2.13 QEPCTL Register (offset = 15h) [reset = 0h]

QEPCTL is shown in [Figure 15-33](#) and described in [Table 15-17](#).

QEP Control

Figure 15-33. QEPCTL Register

15	14	13	12	11	10	9	8
FREE_SOFT		PCRM		SEI		IEI	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
SWI	SEL	IEL		QPEN	QCLM	UTE	WDE
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-17. QEPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREE_SOFT	R/W	0h	Emulation mode 0h (R/W) = QPOSCNT behavior Position counter stops immediately on emulation suspend QWDTMR behavior Watchdog counter stops immediately QUTMR behavior Unit timer stops immediately QCTMR behavior Capture Timer stops immediately 1h (R/W) = QPOSCNT behavior Position counter continues to count until the rollover QWDTMR behavior Watchdog counter counts until WD period match roll over QUTMR behavior Unit timer counts until period rollover QCTMR behavior Capture Timer counts until next unit period event 2h (R/W) = QPOSCNT behavior Position counter is unaffected by emulation suspend QWDTMR behavior Watchdog counter is unaffected by emulation suspend QUTMR behavior Unit timer is unaffected by emulation suspend QCTMR behavior Capture Timer is unaffected by emulation suspend 3h (R/W) = Same as FREE_SOFT_2
13-12	PCRM	R/W	0h	Position counter reset 0h (R/W) = Position counter reset on an index event 1h (R/W) = Position counter reset on the maximum position 2h (R/W) = Position counter reset on the first index event 3h (R/W) = Position counter reset on a unit time event

Table 15-17. QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	SEI	R/W	0h	<p>Strobe event init</p> <p>0h (R/W) = Does nothing (action disabled)</p> <p>1h (R/W) = Does nothing (action disabled)</p> <p>2h (R/W) = Initializes the position counter on rising edge of the QEPI signal</p> <p>3h (R/W) = Clockwise Direction:</p> <p>Initializes the position counter on the rising edge of QEPI strobe</p> <p>Counter Clockwise Direction:</p> <p>Initializes the position counter on the falling edge of QEPI strobe</p>
9-8	IEI	R/W	0h	<p>Index event init of position count</p> <p>0h (R/W) = Do nothing (action disabled)</p> <p>1h (R/W) = Do nothing (action disabled)</p> <p>2h (R/W) = Initializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT)</p> <p>3h (R/W) = Initializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT)</p>
7	SWI	R/W	0h	<p>Software init position counter</p> <p>0h (R/W) = Do nothing (action disabled)</p> <p>1h (R/W) = Initialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically</p>
6	SEL	R/W	0h	<p>Strobe event latch of position counter</p> <p>0h (R/W) = The position counter is latched on the rising edge of QEPI strobe (QPOSSLAT = POSCCNT). Latching on the falling edge can be done by inverting the strobe input using the QSP bit in the QDECCTL register</p> <p>1h (R/W) = Clockwise Direction:</p> <p>Position counter is latched on rising edge of QEPI strobe</p> <p>Counter Clockwise Direction:</p> <p>Position counter is latched on falling edge of QEPI strobe</p>
5-4	IEL	R/W	0h	<p>Index event latch of position counter (software index marker)</p> <p>0h (R/W) = Reserved</p> <p>1h (R/W) = Latches position counter on rising edge of the index signal</p> <p>2h (R/W) = Latches position counter on falling edge of the index signal</p> <p>3h (R/W) = Software index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking.</p>
3	QOPEN	R/W	0h	<p>Quadrature position counter enable/software reset</p> <p>0h (R/W) = Reset the eQEP peripheral internal operating flags/read-only registers. Control/configuration registers are not disturbed by a software reset.</p> <p>1h (R/W) = eQEP position counter is enabled</p>
2	QCLM	R/W	0h	<p>QEP capture latch mode</p> <p>0h (R/W) = Latch on position counter read by CPU. Capture timer and capture period values are latched into QCTMRLAT and QCPRDLAT registers when CPU reads the QPOSCNT register.</p> <p>1h (R/W) = Latch on unit time out. Position counter, capture timer and capture period values are latched into QPOS LAT, QCTMRLAT and QCPRDLAT registers on unit time out.</p>

Table 15-17. QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UTE	R/W	0h	QEP unit timer enable 0h (R/W) = Disable eQEP unit timer 1h (R/W) = Enable unit timer
0	WDE	R/W	0h	QEP watchdog enable 0h (R/W) = Disable the eQEP watchdog timer 1h (R/W) = Enable the eQEP watchdog timer

15.9.2.14 QCAPCTL Register (offset = 16h) [reset = 0h]

QCAPCTL is shown in [Figure 15-34](#) and described in [Table 15-18](#).

Quadrature Capture Control

Figure 15-34. QCAPCTL Register

15	14	13	12	11	10	9	8
CEN	RESERVED						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	CCPS			UPPS			
R-0h	R/W-0h			R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-18. QCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CEN	R/W	0h	Enable eQEP capture 0h (R/W) = eQEP capture unit is disabled 1h (R/W) = eQEP capture unit is enabled
14-7	RESERVED	R	0h	Reserved
6-4	CCPS	R/W	0h	eQEP capture timer clock prescaler 0h (R/W) = CAPCLK = SYSCLKOUT/1 1h (R/W) = CAPCLK = SYSCLKOUT/2 2h (R/W) = CAPCLK = SYSCLKOUT/4 3h (R/W) = CAPCLK = SYSCLKOUT/8 4h (R/W) = CAPCLK = SYSCLKOUT/16 5h (R/W) = CAPCLK = SYSCLKOUT/32 6h (R/W) = CAPCLK = SYSCLKOUT/64 7h (R/W) = CAPCLK = SYSCLKOUT/128
3-0	UPPS	R/W	0h	Unit position event prescaler 0h (R/W) = UPEVNT = QCLK/1 1h (R/W) = UPEVNT = QCLK/2 2h (R/W) = UPEVNT = QCLK/4 3h (R/W) = UPEVNT = QCLK/8 4h (R/W) = UPEVNT = QCLK/16 5h (R/W) = UPEVNT = QCLK/32 6h (R/W) = UPEVNT = QCLK/64 7h (R/W) = UPEVNT = QCLK/128 8h (R/W) = UPEVNT = QCLK/256 9h (R/W) = UPEVNT = QCLK/512 Ah (R/W) = UPEVNT = QCLK/1024 Bh (R/W) = UPEVNT = QCLK/2048 Ch (R/W) = Reserved Dh (R/W) = Reserved Eh (R/W) = Reserved Fh (R/W) = Reserved

15.9.2.15 QPOSCTL Register (offset = 17h) [reset = 0h]

QPOSCTL is shown in [Figure 15-35](#) and described in [Table 15-19](#).

Position Compare Control

Figure 15-35. QPOSCTL Register

15	14	13	12	11	10	9	8
PCSHDW	PCLOAD	PCPOL	PCE		PCSPW		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
			PCSPW				
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-19. QPOSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCSHDW	R/W	0h	Position compare of shadow enable 0h (R/W) = Shadow disabled, load Immediate 1h (R/W) = Shadow enabled
14	PCLOAD	R/W	0h	Position compare of shadow load 0h (R/W) = Load on QPOS_CNT = 0 1h (R/W) = Load when QPOS_CNT = QPOS_CMP
13	PCPOL	R/W	0h	Polarity of sync output 0h (R/W) = Active HIGH pulse output 1h (R/W) = Active LOW pulse output
12	PCE	R/W	0h	Position compare enable/disable 0h (R/W) = Disable position compare unit 1h (R/W) = Enable position compare unit
11-0	PCSPW	R/W	0h	Select-position-compare sync output pulse width 0h (R/W) = 1 * 4 * SYSCLKOUT cycles 1h (R/W) = 2 * 4 * SYSCLKOUT cycles FFFh (R/W) = 4096 * 4 * SYSCLKOUT cycles

15.9.2.16 QEINT Register (offset = 18h) [reset = 0h]

QEINT is shown in [Figure 15-36](#) and described in [Table 15-20](#).

QEP Interrupt Control

Figure 15-36. QEINT Register

15	14	13	12	11	10	9	8
		RESERVED		UTO	IEL	SEL	PCM
		R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	QPE	PCE	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-20. QEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	UTO	R/W	0h	Unit time out interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
10	IEL	R/W	0h	Index event latch interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
9	SEL	R/W	0h	Strobe event latch interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
8	PCM	R/W	0h	Position-compare match interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
7	PCR	R/W	0h	Position-compare ready interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
6	PCO	R/W	0h	Position counter overflow interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
5	PCU	R/W	0h	Position counter underflow interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
4	WTO	R/W	0h	Watchdog time out interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
3	QDC	R/W	0h	Quadrature direction change interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
2	QPE	R/W	0h	Quadrature phase error interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
1	PCE	R/W	0h	Position counter error interrupt enable 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
0	RESERVED	R	0h	Reserved

15.9.2.17 QFLG Register (offset = 19h) [reset = 0h]

QFLG is shown in [Figure 15-37](#) and described in [Table 15-21](#).

QEP Interrupt Flag

Figure 15-37. QFLG Register

15	14	13	12	11	10	9	8
RESERVED				UTO	IEL	SEL	PCM
			R-0h		R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-21. QFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	UTO	R	0h	Unit time out interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
10	IEL	R	0h	Index event latch interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
9	SEL	R	0h	Strobe event latch interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
8	PCM	R	0h	eQEP compare match event interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
7	PCR	R	0h	Position-compare ready interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
6	PCO	R	0h	Position counter overflow interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
5	PCU	R	0h	Position counter underflow interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
4	WTO	R	0h	Watchdog timeout interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
3	QDC	R	0h	Quadrature direction change interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
2	PHE	R	0h	Quadrature phase error interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
1	PCE	R	0h	Position counter error interrupt flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated

Table 15-21. QFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R	0h	Global interrupt status flag 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated

15.9.2.18 QCLR Register (offset = 1Ah) [reset = 0h]

QCLR is shown in [Figure 15-38](#) and described in [Table 15-22](#).

QEP Interrupt Clear

Figure 15-38. QCLR Register

15	14	13	12	11	10	9	8
RESERVED				UTO	IEL	SEL	PCM
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-22. QCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	UTO	R/W	0h	Clear unit time out interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
10	IEL	R/W	0h	Clear index event latch interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
9	SEL	R/W	0h	Clear strobe event latch interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
8	PCM	R/W	0h	Clear eQEP compare match event interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
7	PCR	R/W	0h	Clear position-compare ready interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
6	PCO	R/W	0h	Clear position counter overflow interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
5	PCU	R/W	0h	Clear position counter underflow interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
4	WTO	R/W	0h	Clear watchdog timeout interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
3	QDC	R/W	0h	Clear quadrature direction change interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
2	PHE	R/W	0h	Clear quadrature phase error interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
1	PCE	R/W	0h	Clear position counter error interrupt flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag

Table 15-22. QCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R/W	0h	Global interrupt clear flag 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag

15.9.2.19 QFRC Register (offset = 1Bh) [reset = 0h]

QFRC is shown in Figure 15-39 and described in Table 15-23.

QEP Interrupt Force

Figure 15-39. QFRC Register

15	14	13	12	11	10	9	8
		RESERVED		UTO	IEL	SEL	PCM
		R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-23. QFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	UTO	R/W	0h	Force unit time out interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
10	IEL	R/W	0h	Force index event latch interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
9	SEL	R/W	0h	Force strobe event latch interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
8	PCM	R/W	0h	Force position-compare match interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
7	PCR	R/W	0h	Force position-compare ready interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
6	PCO	R/W	0h	Force position counter overflow interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
5	PCU	R/W	0h	Force position counter underflow interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
4	WTO	R/W	0h	Force watchdog time out interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
3	QDC	R/W	0h	Force quadrature direction change interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
2	PHE	R/W	0h	Force quadrature phase error interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
1	PCE	R/W	0h	Force position counter error interrupt 0h (R/W) = No effect 1h (R/W) = Force the interrupt
0	RESERVED	R	0h	Reserved

15.9.2.20 QEPSTS Register (offset = 1Ch) [reset = 8Eh]

QEPSTS is shown in [Figure 15-40](#) and described in [Table 15-24](#).

QEP Status

Figure 15-40. QEPSTS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
UPEVNT	FIDF	QDF	QDLF	COEF	CDEF	FIMF	PCEF
R/W-1h	R-0h	R-0h	R-0h	R/W-1h	R/W-1h	R/W-1h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

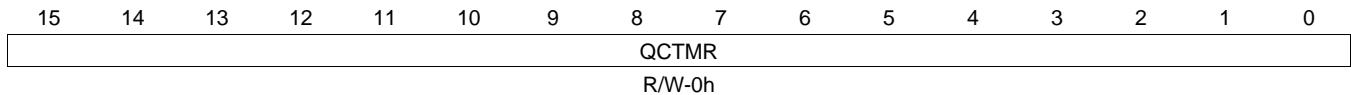
Table 15-24. QEPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	UPEVNT	R/W	1h	Unit position event flag 0h (R/W) = No unit position event detected 1h (R/W) = Unit position event detected. Write 1 to clear
6	FIDF	R	0h	Direction on the first index marker Status of the direction is latched on the first index event marker. 0h (R/W) = Counter-clockwise rotation (or reverse movement) on the first index event 1h (R/W) = Clockwise rotation (or forward movement) on the first index event
5	QDF	R	0h	Quadrature direction flag 0h (R/W) = Counter-clockwise rotation (or reverse movement) 1h (R/W) = Clockwise rotation (or forward movement)
4	QDLF	R	0h	eQEP direction latch flag 0h (R/W) = Counter-clockwise rotation (or reverse movement) on index event marker 1h (R/W) = Clockwise rotation (or forward movement) on index event marker
3	COEF	R/W	1h	Capture overflow error flag 0h (R/W) = Sticky bit, cleared by writing 1 1h (R/W) = Overflow occurred in eQEP Capture timer (QEPCPTMR)
2	CDEF	R/W	1h	Capture direction error flag 0h (R/W) = Sticky bit, cleared by writing 1 1h (R/W) = Direction change occurred between the capture position event.
1	FIMF	R/W	1h	First index marker flag 0h (R/W) = Sticky bit, cleared by writing 1 1h (R/W) = Set by first occurrence of index pulse
0	PCEF	R	0h	Position counter error flag. This bit is not sticky and it is updated for every index event. 0h (R/W) = No error occurred during the last index transition 1h (R/W) = Position counter error

15.9.2.21 QCTMR Register (offset = 1Dh) [reset = 0h]

QCTMR is shown in [Figure 15-41](#) and described in [Table 15-25](#).

QEP Capture Timer

Figure 15-41. QCTMR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-25. QCTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QCTMR	R/W	0h	This register provides time base for edge capture unit.

15.9.2.22 QCPRD Register (offset = 1Eh) [reset = 0h]

QCPRD is shown in [Figure 15-42](#) and described in [Table 15-26](#).

QEP Capture Period

Figure 15-42. QCPRD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QCPRD															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

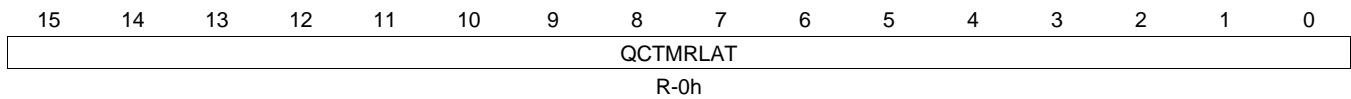
Table 15-26. QCPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QCPRD	R/W	0h	This register holds the period count value between the last successive eQEP position events

15.9.2.23 QCTMRLAT Register (offset = 1Fh) [reset = 0h]

QCTMRLAT is shown in [Figure 15-43](#) and described in [Table 15-27](#).

QEP Capture Latch

Figure 15-43. QCTMRLAT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

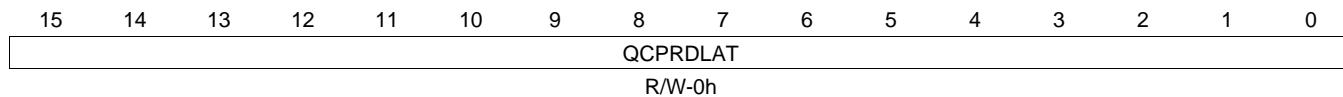
Table 15-27. QCTMRLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QCTMRLAT	R	0h	The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter.

15.9.2.24 QCPRDLAT Register (offset = 20h) [reset = 0h]

QCPRDLAT is shown in [Figure 15-44](#) and described in [Table 15-28](#).

QEP Capture Period Latch

Figure 15-44. QCPRDLAT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-28. QCPRDLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QCPRDLAT	R/W	0h	eQEP capture period value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter.

Serial Peripheral Interface (SPI)

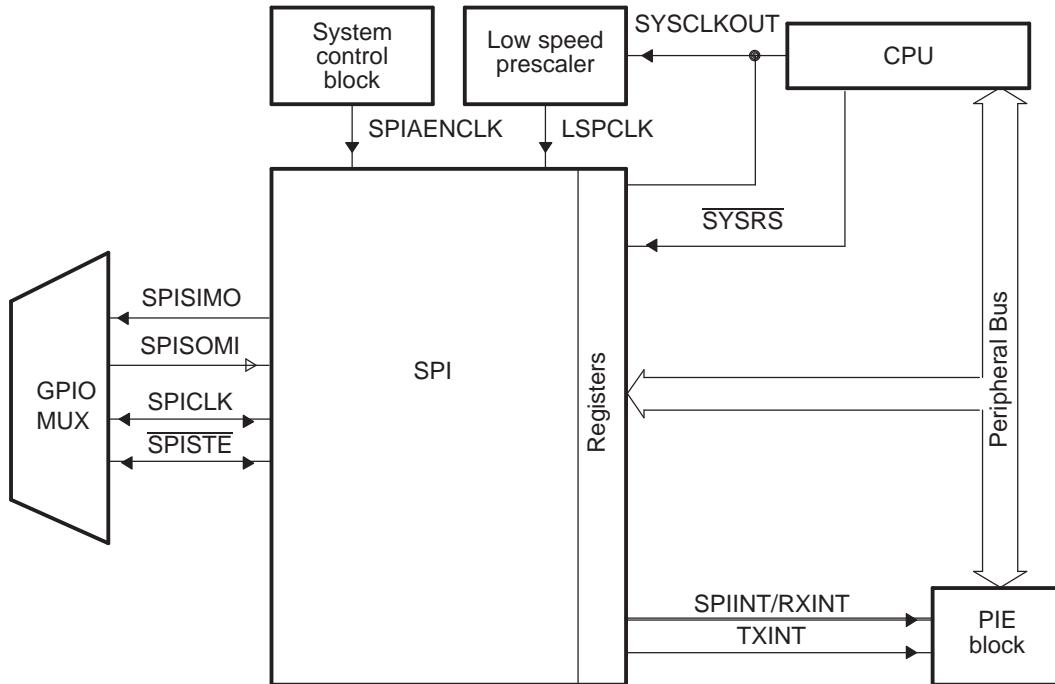
This chapter describes the serial peripheral interface (SPI). The serial peripheral interface (SPI) is a high-speed synchronous serial input/ output (I/O) port that allows a serial bit stream of programmed length (one to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the DSP controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion via devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multi-device communications are supported by the master/slave operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

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16.1 Enhanced SPI Module Overview

Figure 16-1 shows the SPI CPU interfaces.

Figure 16-1. SPI CPU Interface



The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- SPISTE: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO, if the SPI module is not used.

- Two operational modes: master and slave
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins. See the device-specific data sheet for more details.
- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
 - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
 - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt- driven or polled algorithms.
- 12 SPI module control registers: Located in control register frame beginning at address 7040h.

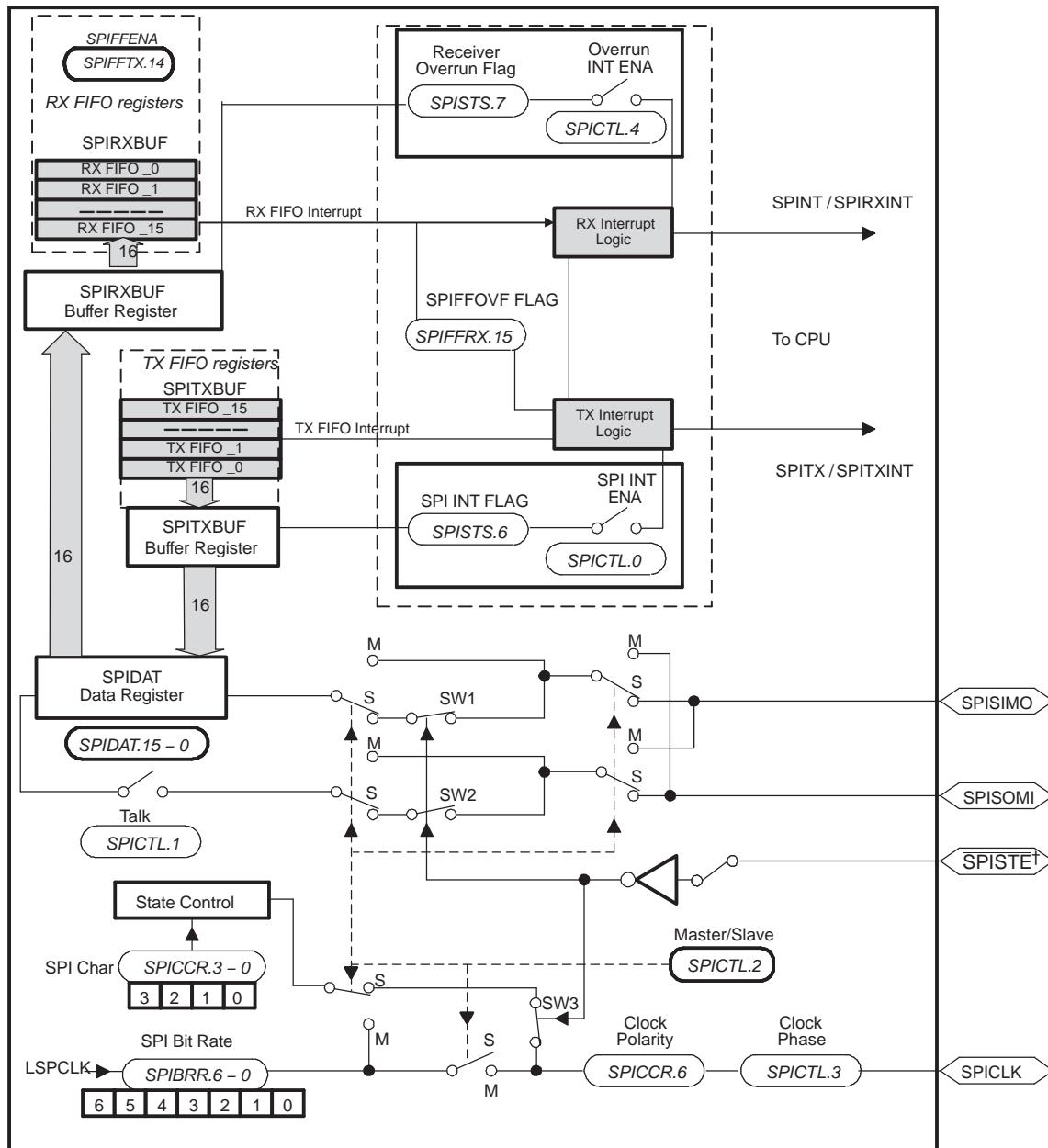
NOTE: All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced Features:

- 16 -level transmit/receive FIFO
- Delayed transmit control

16.1.1 SPI Block Diagram

Figure 16-2 is a block diagram of the SPI in slave mode, showing the basic control blocks available on the SPI module.

Figure 16-2. Serial Peripheral Interface Module Block Diagram


A SPISTE of a slave device is driven low by the master.

16.1.2 SPI Module Signal Summary

Table 16-1. SPI Module Signal Summary

Signal Name	Description
External Signals	
SPICLK	SPI clock
SPISIMO	SPI slave in, master out
SPISOMI	SPI slave out, master in
SPISTE	SPI slave transmit enable
Control	
SPI Clock Rate	LSPCLK
Interrupt signals	
SPIRXINT	Transmit interrupt/ Receive Interrupt in non FIFO mode (referred to as SPI INT) Receive in interrupt in FIFO mode
SPITXINT	Transmit interrupt – FIFO

16.1.3 Overview of SPI Module Registers

The SPI port operation is configured and controlled by the registers listed in [Table 16-2](#).

Table 16-2. SPI Registers

Name	Address Range	Size (x16)	Description
SPICCR	0x0000-7040	1	SPI Configuration Control Register
SPICCTL	0x0000-7041	1	SPI Operation Control Register
SPIST	0x0000-7042	1	SPI Status Register
SPIBRR	0x0000-7044	1	SPI Baud Rate Register
SPIEMU	0x0000-7046	1	SPI Emulation Buffer Register
SPIRXBUF	0x0000-7047	1	SPI Serial Input Buffer Register
SPITXBUF	0x0000-7048	1	SPI Serial Output Buffer Register
SPIDAT	0x0000-7049	1	SPI Serial Data Register
SPIFFTX	0x0000-704A	1	SPI FIFO Transmit Register
SPIFFRX	0x0000-704B	1	SPI FIFO Receive Register
SPIFFCFT	0x0000-704C	1	SPI FIFO Control Register
SPIPRI	0x0000-704F	1	SPI Priority Control Register

This SPI has 16-bit transmit and receive capability, with double-buffered transmit and double-buffered receive. All data registers are 16-bits wide.

The maximum transmission rate in both slave mode and master mode is now LSPCLK/4.

Writes of transmit data to the serial data register, SPIDAT (and the new transmit buffer, SPITXBUF), must be left-justified within a 16-bit register.

The control and data bits for general-purpose bit I/O multiplexing have been removed from this peripheral, along with the associated registers, SPIPC1 (704Dh) and SPIPC2 (704Eh). These bits are now in the General-Purpose I/O registers.

Twelve registers inside the SPI module control the SPI operations:

- SPICCR (SPI configuration control register). Contains control bits used for SPI configuration
 - SPI module software reset
 - SPICLK polarity selection
 - Four SPI character-length control bits
- SPICCTL (SPI operation control register). Contains control bits for data transmission

- Two SPI interrupt enable bits
- SPICLK phase selection
- Operational mode (master/slave)
- Data transmission enable
- SPISTS (SPI status register). Contains two receive buffer status bits and one transmit buffer status bit
 - RECEIVER OVERRUN
 - SPI INT FLAG
 - TX BUF FULL FLAG
- SPIBRR (SPI baud rate register). Contains seven bits that determine the bit transfer rate
- SPIRXEMU (SPI receive emulation buffer register). Contains the received data. This register is used for emulation purposes only. The SPIRXBUF should be used for normal operation
- SPIRXBUF (SPI receive buffer — the serial receive buffer register). Contains the received data
- SPITXBUF (SPI transmit buffer — the serial transmit buffer register). Contains the next character to be transmitted
- SPIDAT (SPI data register). Contains data to be transmitted by the SPI, acting as the transmit/receive shift register. Data written to SPIDAT is shifted out on subsequent SPICLK cycles. For every bit shifted out of the SPI, a bit from the receive bit stream is shifted into the other end of the shift register
- SPIPRI (SPI priority register). Contains bits that specify interrupt priority and determine SPI operation on the XDS™ emulator during program suspensions.

16.1.4 SPI Operation

This section describes the operation of the SPI. Included are explanations of the operation modes, interrupts, data format, clock sources, and initialization. Typical timing diagrams for data transfers are given.

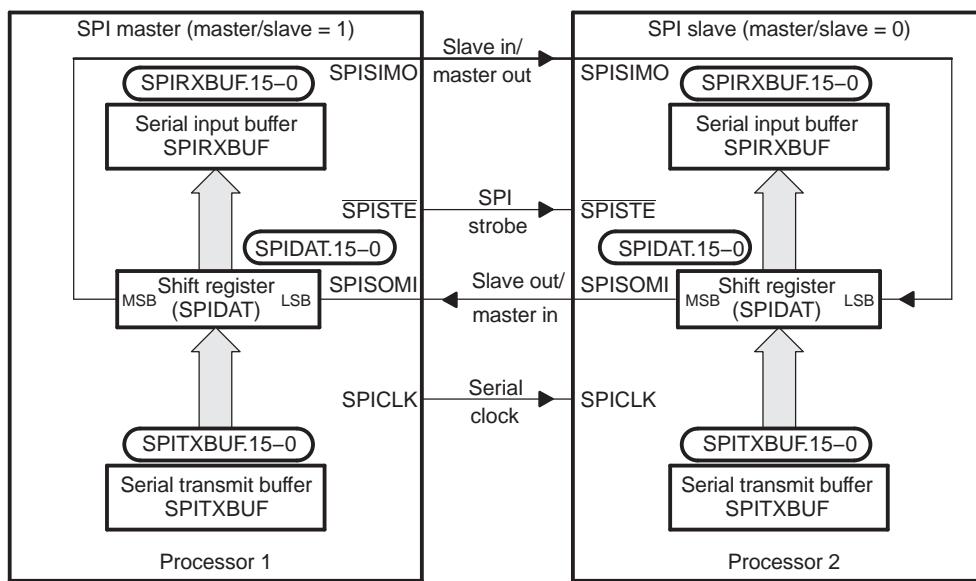
16.1.4.1 Introduction to Operation

Figure 16-3 shows typical connections of the SPI for communications between two controllers: a master and a slave.

The master initiates data transfer by sending the SPICLK signal. For both the slave and the master, data is shifted out of the shift registers on one edge of the SPICLK and latched into the shift register on the opposite SPICLK clock edge. If the CLOCK PHASE bit (SPICL3) is high, data is transmitted and received a half-cycle before the SPICLK transition (see Section 16.1.4.2). As a result, both controllers send and receive data simultaneously. The application software determines whether the data is meaningful or dummy data. There are three possible methods for data transmission:

- Master sends data; slave sends dummy data.
- Master sends data; slave sends data.
- Master sends dummy data; slave sends data.

The master can initiate data transfer at any time because it controls the SPICLK signal. The software, however, determines how the master detects when the slave is ready to broadcast data.

Figure 16-3. SPI Master/Slave Connection

16.1.4.2 SPI Module Slave and Master Operation Modes

The SPI can operate in master or slave mode. The MASTER/SLAVE bit (SPICTL.2) selects the operating mode and the source of the SPICLK signal.

16.1.4.2.1 Master Mode

In the master mode (MASTER/SLAVE = 1), the SPI provides the serial clock on the SPICLK pin for the entire serial communications network. Data is output on the SPISIMO pin and latched from the SPISOMI pin.

The SPIBRR register determines both the transmit and receive bit transfer rate for the network. SPIBRR can select 126 different data transfer rates.

Data written to SPIDAT or SPITXBUF initiates data transmission on the SPISIMO pin, MSB (most significant bit) first. Simultaneously, received data is shifted through the SPISOMI pin into the LSB (least significant bit) of SPIDAT. When the selected number of bits has been transmitted, the received data is transferred to the SPIRXBUF (buffered receiver) for the CPU to read. Data is stored right-justified in SPIRXBUF.

When the specified number of data bits has been shifted through SPIDAT, the following events occur:

- SPIDAT contents are transferred to SPIRXBUF.
- SPI INT FLAG bit (SPISTS.6) is set to 1.
- If there is valid data in the transmit buffer SPITXBUF, as indicated by the TXBUF FULL bit in SPISTS, this data is transferred to SPIDAT and is transmitted; otherwise, SPICLK stops after all bits have been shifted out of SPIDAT.
- If the SPI INT ENA bit (SPICTL.0) is set to 1, an interrupt is asserted.

In a typical application, the SPISTE pin serves as a chip-enable pin for a slave SPI device. This pin is driven low by the master before transmitting data to the slave and is taken high after the transmission is complete.

16.1.4.2.2 Slave Mode

In the slave mode (MASTER/SLAVE = 0), data shifts out on the SPISOMI pin and in on the SPISIMO pin. The SPICLK pin is used as the input for the serial shift clock, which is supplied from the external network master. The transfer rate is defined by this clock. The SPICLK input frequency should be no greater than the LSPCLK frequency divided by 4.

Data written to SPIDAT or SPITXBUF is transmitted to the network when appropriate edges of the SPICLK signal are received from the network master. Data written to the SPITXBUF register will be transferred to the SPIDAT register when all bits of the character to be transmitted have been shifted out of SPIDAT. If no character is currently being transmitted when SPITXBUF is written to, the data will be transferred immediately to SPIDAT. To receive data, the SPI waits for the network master to send the SPICLK signal and then shifts the data on the SPISIMO pin into SPIDAT. If data is to be transmitted by the slave simultaneously, and SPITXBUF has not been previously loaded, the data must be written to SPITXBUF or SPIDAT before the beginning of the SPICLK signal.

When the TALK bit (SPICTL.1) is cleared, data transmission is disabled, and the output line (SPISOMI) is put into the high-impedance state. If this occurs while a transmission is active, the current character is completely transmitted even though SPISOMI is forced into the high-impedance state. This ensures that the SPI is still able to receive incoming data correctly. This TALK bit allows many slave devices to be tied together on the network, but only one slave at a time is allowed to drive the SPISOMI line.

The **SPISTE** pin operates as the slave-select pin. An active-low signal on the **SPISTE** pin allows the slave SPI to transfer data to the serial data line; an inactive- high signal causes the slave SPI serial shift register to stop and its serial output pin to be put into the high-impedance state. This allows many slave devices to be tied together on the network, although only one slave device is selected at a time.

16.1.5 SPI DMA Transfers

On the Type 1 SPI, the DMA (if present) has access to the SPI registers. Two DMA requests DMA_TX_REQ and DMA_RX_REQ are dedicated to the SPI module (see the Direct Memory Access (DMA) chapter for more information). These requests are controlled by configuration bits TXFFIL and RXFFIL. Unlike interrupts these are level triggers meaning there is no need for clearing these triggers. DMA_TX_REQ will be active when SPIFFTX[TXFFST] ≤ SPIFFTX[TXFFIL]. When the TXFFST exceeds the interrupt level (TXFFIL), the DMA transfer will cease. DMA_RX_REQ will be active when SPIFFRX[RXFFST] ≥ SPIFFRX[RXFFIL]. When the RXFFST is less than the interrupt level (RXFFIL), the DMA transfer will cease. The DMA can only be used with the SPI when FIFO mode is active.

16.1.6 SPI Interrupts

This section includes information on the control bits that initialize interrupts, data format, clocking, initialization, and data transfer.

16.1.6.1 SPI Interrupt Control Bits

Five control bits are used to initialize the SPI interrupts:

- SPI INT ENA bit (SPICTL.0)
- SPI INT FLAG bit (SPISTS.6)
- OVERRUN INT ENA bit (SPICTL.4)
- RECEIVER OVERRUN FLAG bit (SPISTS.7)

16.1.6.1.1 SPI INT ENA Bit (SPICTL.0)

When the SPI interrupt-enable bit is set and an interrupt condition occurs, the corresponding interrupt is asserted.

- | | |
|---|------------------------|
| 0 | Disable SPI interrupts |
| 1 | Enable SPI interrupts |

16.1.6.1.2 SPI INT FLAG Bit (SPISTS.6)

This status flag indicates that a character has been placed in the SPI receiver buffer and is ready to be read.

When a complete character has been shifted into or out of SPIDAT, the SPI INT FLAG bit (SPISTS.6) is set, and an interrupt is generated if enabled by the SPI INT ENA bit (SPICTL.0). The interrupt flag remains set until it is cleared by one of the following events:

- The interrupt is acknowledged.
- The CPU reads the SPIRXBUF (reading the SPIRXEMU does not clear the SPI INT FLAG bit).
- The device enters IDLE2 or HALT mode with an IDLE instruction.
- Software clears the SPI SW RESET bit (SPICCR.7).
- A system reset occurs.

When the SPI INT FLAG bit is set, a character has been placed into the SPIRXBUF and is ready to be read. If the CPU does not read the character by the time the next complete character has been received, the new character is written into SPIRXBUF, and the RECEIVER OVERRUN Flag bit (SPISTS.7) is set.

16.1.6.1.3 OVERRUN INT ENA Bit (SPICTL.4)

Setting the overrun interrupt enable bit allows the assertion of an interrupt whenever the RECEIVER OVERRUN Flag bit (SPISTS.7) is set by hardware. Interrupts generated by SPISTS.7 and by the SPI INT FLAG bit (SPISTS.6) share the same interrupt vector.

- | | |
|---|--|
| 0 | Disable RECEIVER OVERRUN Flag bit interrupts |
| 1 | Enable RECEIVER OVERRUN Flag bit interrupts |

16.1.6.1.4 RECEIVER OVERRUN FLAG Bit (SPISTS.7)

The RECEIVER OVERRUN Flag bit is set whenever a new character is received and loaded into the SPIRXBUF before the previously received character has been read from the SPIRXBUF. The RECEIVER OVERRUN Flag bit must be cleared by software.

16.1.6.2 Data Format

Four bits (SPICCR.3–0) specify the number of bits (1 to 16) in the data character. This information directs the state control logic to count the number of bits received or transmitted to determine when a complete character has been processed. The following statements apply to characters with fewer than 16 bits:

- Data must be left-justified when written to SPIDAT and SPITXBUF.
- Data read back from SPIRXBUF is right-justified.
- SPIRXBUF contains the most recently received character, right-justified, plus any bits that remain from previous transmission(s) that have been shifted to the left (shown in [Example 16-1](#)).

Example 16-1. Transmission of Bit From SPIRXBUF

Conditions:

1. Transmission character length = 1 bit (specified in bits SPICCR.3–0)
2. The current value of SPIDAT = 737Bh

SPIDAT (before transmission)															
SPIDAT (after transmission)															
SPIRXBUF (after transmission)															
(TXed) 0 ←	1	1	1	0	0	1	1	0	1	1	1	1	0	1	1
	x ⁽¹⁾														

⁽¹⁾ x = 1 if SPISOMI data is high; x = 0 if SPISOMI data is low; master mode is assumed.

16.1.6.3 Baud Rate and Clocking Schemes

The SPI module supports 125 different baud rates and four different clock schemes. Depending on whether the SPI clock is in slave or master mode, the SPICLK pin can receive an external SPI clock signal or provide the SPI clock signal, respectively.

- In the slave mode, the SPI clock is received on the SPICLK pin from the external source, and can be no greater than the LSPCLK frequency divided by 4.
- In the master mode, the SPI clock is generated by the SPI and is output on the SPICLK pin, and can be no greater than the LSPCLK frequency divided by 4.

[Example 16-2](#) shows how to determine the SPI baud rates.

Example 16-2. Baud Rate Determination

For SPIBRR = 3 to 127:

$$\text{SPI Baud Rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \quad (6)$$

For SPIBRR = 0, 1, or 2:

$$\text{SPI Baud Rate} = \frac{\text{LSPCLK}}{4} \quad (7)$$

where:

LSPCLK = Low-speed peripheral clock frequency of the device

SPIBRR = Contents of the SPIBRR in the master SPI device

To determine what value to load into SPIBRR, you must know the device system clock (LSPCLK) frequency (which is device-specific) and the baud rate at which you will be operating.

[Example 1-2](#) shows how to determine the maximum baud rate at which a 240xA can communicate. Assume that LSPCLK = 40 MHz.

Example 16-3. Maximum Baud-Rate Calculation

$$\begin{aligned} \text{Maximum SPI Baud Rate} &= \frac{\text{LSPCLK}}{4} \\ &= \frac{40 \times 10^6}{4} \\ &= 10 \times 10^6 \text{ bps} \end{aligned} \quad (8)$$

16.1.6.3.1 SPI Clocking Schemes

The CLOCK POLARITY bit (SPICCR.6) and the CLOCK PHASE bit (SPICCTL.3) control four different clocking schemes on the SPICLK pin. The CLOCK POLARITY bit selects the active edge, either rising or falling, of the clock. The CLOCK PHASE bit selects a half-cycle delay of the clock. The four different clocking schemes are as follows:

- Falling Edge Without Delay. The SPI transmits data on the falling edge of the SPICLK and receives data on the rising edge of the SPICLK.
- Falling Edge With Delay. The SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
- Rising Edge Without Delay. The SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
- Rising Edge With Delay. The SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.

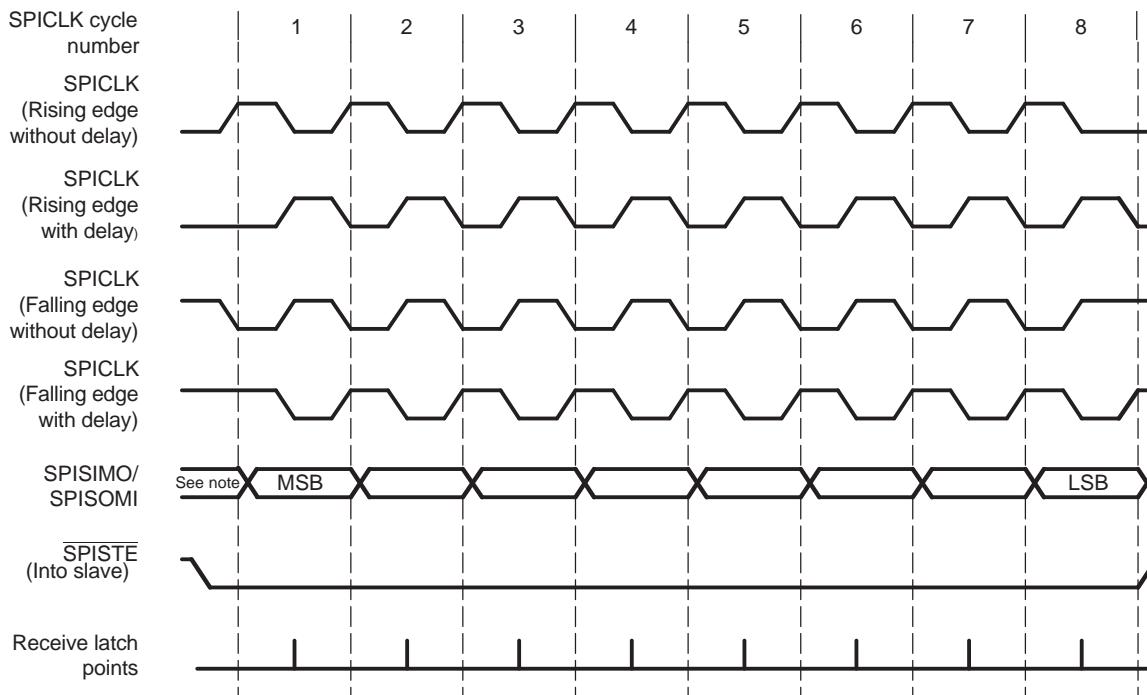
The selection procedure for the SPI clocking scheme is shown in [Table 16-3](#). Examples of these four clocking schemes relative to transmitted and received data are shown in [Figure 16-4](#).

Table 16-3. SPI Clocking Scheme Selection Guide

SPICLK Scheme	CLOCK POLARITY (SPICCR.6)	CLOCK PHASE (SPICTL.3) ⁽¹⁾
Rising edge without delay	0	0
Rising edge with delay	0	1
Falling edge without delay	1	0
Falling edge with delay	1	1

⁽¹⁾ The description of CLOCK PHASE and CLOCK POLARITY differs between manufacturers. For proper operation, select the desired waveform to determine the PHASE and POLARITY settings.

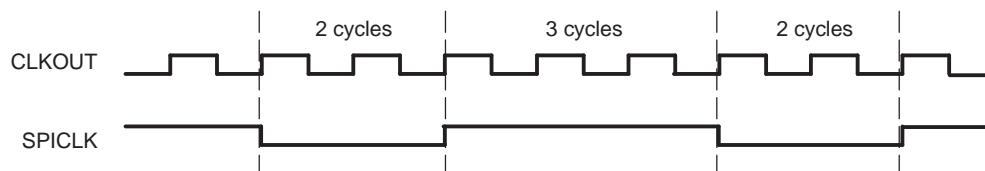
Figure 16-4. SPICLK Signal Options



Note: Previous data bit

For the SPI, SPICLK symmetry is retained only when the result of (SPIBRR+1) is an even value. When (SPIBRR + 1) is an odd value and SPIBRR is greater than 3, SPICLK becomes asymmetrical. The low pulse of SPICLK is one CLKOUT longer than the high pulse when the CLOCK POLARITY bit is clear (0). When the CLOCK POLARITY bit is set to 1, the high pulse of the SPICLK is one CLKOUT longer than the low pulse, as shown in [Figure 16-5](#).

Figure 16-5. SPI: SPICLK-CLKOUT Characteristic When (BRR + 1) is Odd, BRR > 3, and CLOCK POLARITY = 1



16.1.6.4 Initialization Upon Reset

A system reset forces the SPI peripheral module into the following default configuration:

- Unit is configured as a slave module (MASTER/SLAVE = 0)
- Transmit capability is disabled (TALK = 0)
- Data is latched at the input on the falling edge of the SPICLK signal
- Character length is assumed to be one bit
- SPI interrupts are disabled
- Data in SPIDAT is reset to 0000h
- SPI module pin functions are selected as general-purpose inputs (this is done in I/O MUX control register B [MCRB])

To change this SPI configuration:

- Step 1. Clear the SPI SW RESET bit (SPICCR.7) to 0 to force the SPI to the reset state.
- Step 2. Initialize the SPI configuration, format, baud rate, and pin functions as desired.
- Step 3. Set the SPI SW RESET bit to 1 to release the SPI from the reset state.
- Step 4. Write to SPIDAT or SPITXBUF (this initiates the communication process in the master).
- Step 5. Read SPIRXBUF after the data transmission has completed (SPISTS.6 = 1) to determine what data was received.

To prevent unwanted and unforeseen events from occurring during or as a result of initialization changes, clear the SPI SW RESET bit (SPICCR.7) before making initialization changes, and then set this bit after initialization is complete.

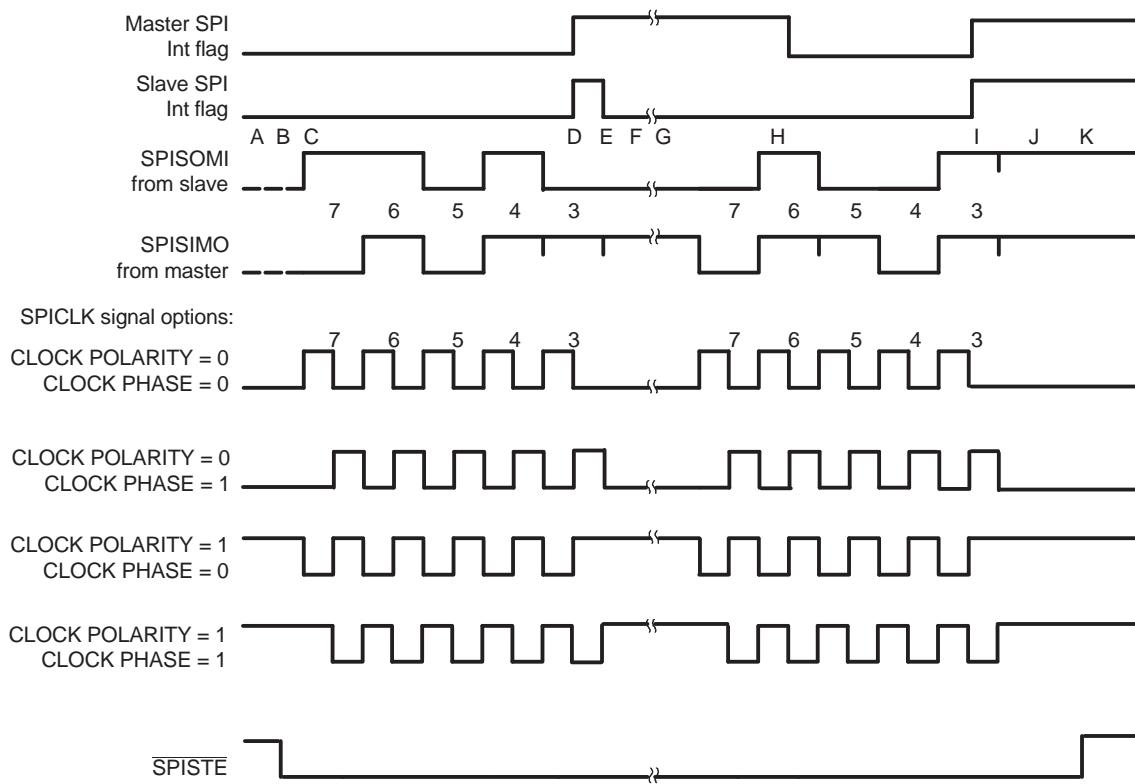
NOTE: Do not change the SPI configuration when communication is in progress.

16.1.6.5 Data Transfer Example

The timing diagram shown in [Figure 16-6](#) illustrates an SPI data transfer between two devices using a character length of five bits with the SPICLK being symmetrical.

The timing diagram with SPICLK unsymmetrical ([Figure 16-5](#)) shares similar characterizations with [Figure 16-6](#) except that the data transfer is one CLKOUT cycle longer per bit during the low pulse (CLOCK POLARITY = 0) or during the high pulse (CLOCK POLARITY = 1) of the SPICLK.

[Figure 16-6](#) is applicable for 8-bit SPI only and is not for 24x devices that are capable of working with 16-bit data. The figure is shown for illustrative purposes only.

Figure 16-6. Five Bits per Character


- A Slave writes 0D0h to SPIDAT and waits for the master to shift out the data.
- B Master sets the slave SPISTE signal low (active).
- C Master writes 058h to SPIDAT, which starts the transmission procedure.
- D First byte is finished and sets the interrupt flags.
- E Slave reads 0Bh from its SPIRXBUF (right-justified).
- F Slave writes 04Ch to SPIDAT and waits for the master to shift out the data.
- G Master writes 06Ch to SPIDAT, which starts the transmission procedure.
- H Master reads 01Ah from the SPIRXBUF (right-justified).
- I Second byte is finished and sets the interrupt flags.
- J Master reads 89h and the slave reads 8Dh from their respective SPIRXBUF. After the user's software masks off the unused bits, the master receives 09h and the slave receives 0Dh.
- K Master clears the slave SPISTE signal high (inactive).

16.1.7 SPI FIFO Description

The following steps explain the FIFO features and help with programming the SPI FIFOs:

1. Reset. At reset the SPI powers up in standard SPI mode, the FIFO function is disabled. The FIFO registers SPIFFTX, SPIFFRX and SPIFFCT remain inactive.
2. Standard SPI. The standard 240x SPI mode will work with SPIINT/SPIRXINT as the interrupt source.
3. Mode change. FIFO mode is enabled by setting the SPIFFEN bit to 1 in the SPIFFTX register. SPIRST can reset the FIFO mode at any stage of its operation.
4. Active registers. All the SPI registers and SPI FIFO registers SPIFFTX, SPIFFRX, and SPIFFCT will be active.
5. Interrupts. FIFO mode has two interrupts one for transmit FIFO, SPITXINT and one for receive FIFO, SPIINT/SPIRXINT. SPIINT/SPIRXINT is the common interrupt for SPI FIFO receive, receive error and receive FIFO overflow conditions. The single SPIINT for both transmit and receive sections of the standard SPI will be disabled and this interrupt will service as SPI receive FIFO interrupt.

6. Buffers. Transmit and receive buffers are supplemented with two 16x16 FIFOs. The one-word transmit buffer (TXBUF) of the standard SPI functions as a transition buffer between the transmit FIFO and shift register. The one-word transmit buffer will be loaded from transmit FIFO only after the last bit of the shift register is shifted out.
7. Delayed transfer. The rate at which transmit words in the FIFO are transferred to transmit shift register is programmable. The SPIFFCT register bits (7–0) FFTXDLY7–FTTXDLY0 define the delay between the word transfer. The delay is defined in number SPI serial clock cycles. The 8-bit register could define a minimum delay of 0 serial clock cycles and a maximum of 255 serial clock cycles. With zero delay, the SPI module can transmit data in continuous mode with the FIFO words shifting out back to back. With the 255 clock delay, the SPI module can transmit data in a maximum delayed mode with the FIFO words shifting out with a delay of 255 SPI clocks between each words. The programmable delay facilitates glueless interface to various slow SPI peripherals, such as EEPROMs, ADC, DAC etc.
8. FIFO status bits. Both transmit and receive FIFOs have status bits TXFFST or RXFFST (bits 12–0) that define the number of words available in the FIFOs at any time. The transmit FIFO reset bit TXFIFO and receive reset bit RXFIFO will reset the FIFO pointers to zero when these bits are set to 1. The FIFOs will resume operation from start once these bits are cleared to zero.
9. Programmable interrupt levels. Both transmit and receive FIFO can generate CPU interrupts. The interrupt trigger is generated whenever the transmit FIFO status bits TXFFST (bits 12–8) match (less than or equal to) the interrupt trigger level bits TXFFIL (bits 4–0). This provides a programmable interrupt trigger for transmit and receive sections of the SPI. The default value for these trigger level bits will be 0x11111 for receive FIFO and 0x00000 for transmit FIFO respectively.

16.1.7.1 SPI Interrupts

Figure 16-7. SPI FIFO Interrupt Flags and Enable Logic Generation

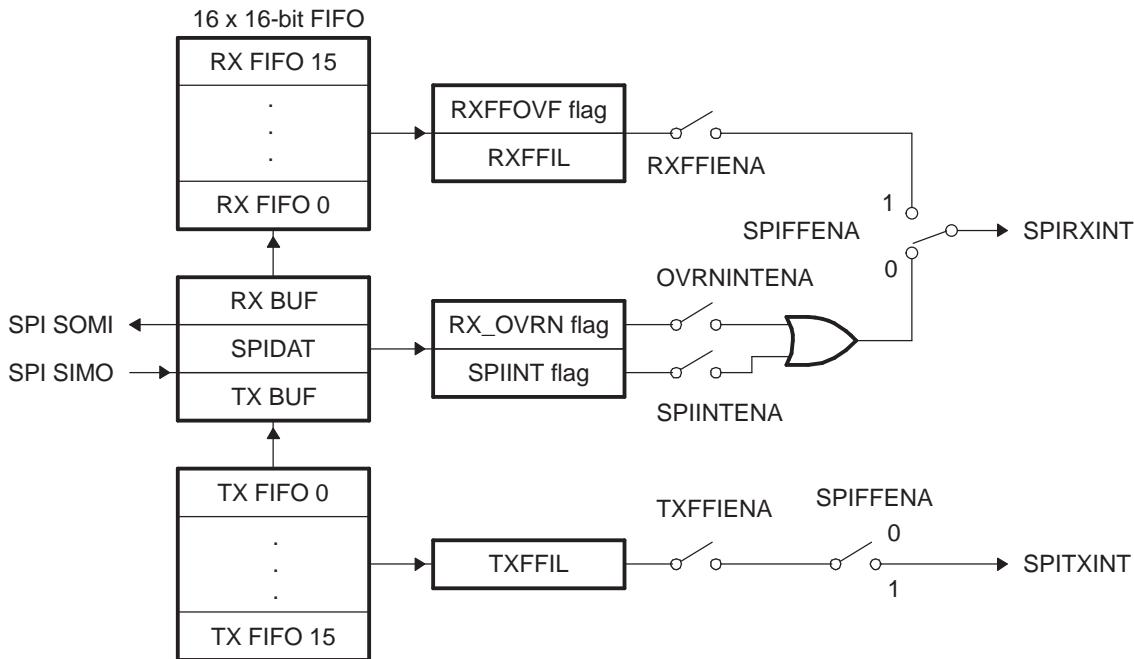


Table 16-4. SPI Interrupt Flag Modes

SPI Interrupt	Interrupt	Interrupt	FIFO Enable	Interrupt ⁽¹⁾
FIFO Options	Source	Flags	Enables	SPIFFENA
<i>SPI without FIFO</i>				line
Receive overrun	RXOVRN	OVRNINTENA	0	SPIRINT
Data receive	SPIINT	SPIINTENA	0	SPIRINT
Transmit empty	SPIINT	SPIINTENA	0	SPIRINT

⁽¹⁾ In non FIFO mode, SPIRINT is the same as the SPIINT interrupt in 240x devices.

Table 16-4. SPI Interrupt Flag Modes (continued)

SPI Interrupt	Interrupt	Interrupt	FIFO Enable	Interrupt ⁽¹⁾
SPI FIFO mode				
FIFO receive	RXFFIL	RXFFIENA	1	SPIRXINT
Transmit empty	TXFFIL	TXFFIENA	1	SPITXINT

16.1.8 SPI 3-Wire Mode Description

SPI 3-wire mode allows for SPI communication over three pins instead of the normal four pins.

In master mode, if the TRIWIRE (SPIPRI.0) bit is set, enabling 3-wire SPI mode, SPISIMOX becomes the bi-directional SPIMOMIx (SPI master out, master in) pin, and SPISOMIx is no longer used by the SPI. In slave mode, if the TRIWIRE bit is set, SPISOMIx becomes the bi-directional SPISISOX (SPI slave in, slave out) pin, and SPISIMOX is no longer used by the SPI.

The table below indicates the pin function differences between 3-wire and 4-wire SPI mode for a master and slave SPI.

Table 16-5. 4-wire vs. 3-wire SPI Pin Functions

4-wire SPI	3-wire SPI (Master)	3-wire SPI(Slave)
SPICLKx	SPICLKx	SPICLKx
SPISTEx	SPISTEx	SPISTEx
SPISIMOX	SPIMOMIx	Free
SPISOMIx	Free	SPISISOX

Because in 3-wire mode, the receive and transmit paths within the SPI are connected, any data transmitted by the SPI module is also received by itself. The application software must take care to perform a dummy read to clear the SPI data register of the additional received data.

The TALK bit (SPICTL.1) plays an important role in 3-wire SPI mode. The bit must be set to transmit data and cleared prior to reading data. In master mode, in order to initiate a read, the application software must write dummy data to the SPI data register (SPIDAT or SPIRXBUF) while the TALK bit is cleared (no data is transmitted out the SPIMOMI pin) before reading from the data register.

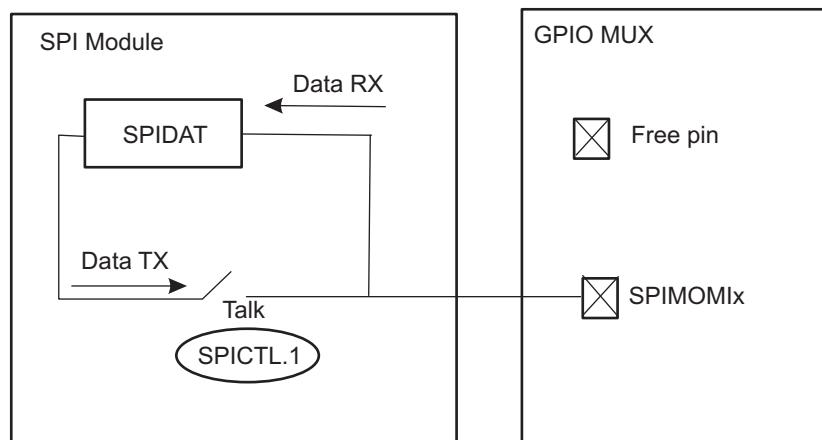
Figure 16-8. SPI 3-wire Master Mode

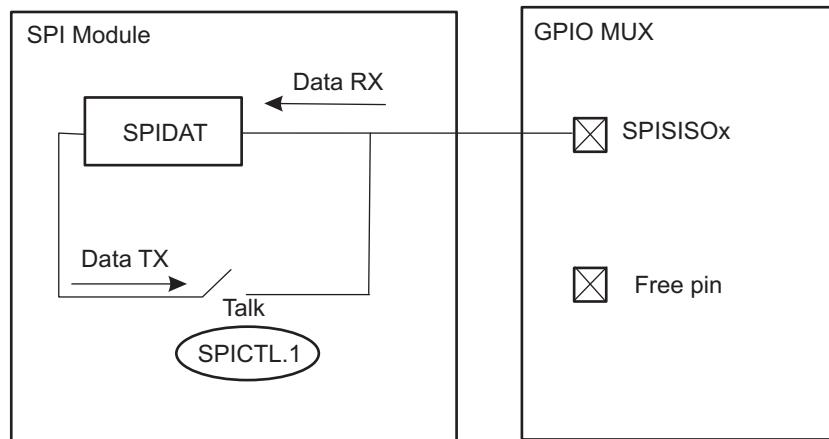
Figure 16-9. SPI 3-wire Slave Mode

Table 16-6 indicates how data is received or transmitted in the various SPI modes while the TALK bit is set or cleared.

Table 16-6. 3-Wire SPI Pin Configuration

Pin Mode	SPIPRI[TRIWIRE]	SPICL[ALK]	SPISIMO	SPISOMI
Master Mode				
4-wire	0	X	TX	RX
3-pin mode	1	0	RX	Disconnect from SPI
Slave Mode				
4-wire	0	X	RX	TX
3-pin mode	1	0	Disconnect from SPI	RX
		1		TX/RX

SPI 3-Wire Mode Code Examples

In addition to the normal SPI initialization, to configure the SPI module for 3-wire mode, the TRIWIRE bit (SPIPRI.0) must be set to 1. After initialization, there are several considerations to take into account when transmitting and receiving data in 3-wire master and slave mode. The following examples demonstrate these considerations.

In 3-wire master mode, SPICLKx, SPISTEx, and SPISIMOf pins must be configured as SPI pins (SPISOMIx pin can be configured as non-SPI pin). When the master transmits, it receives the data it transmits (because SPISIMOf and SPISOMIx are connected internally in 3-wire mode). Therefore, the junk data received must be cleared from the receive buffer every time data is transmitted.

Example 16-4. 3-Wire Master Mode Transmit

```

Uint16 data;
Uint16 dummy;

SpiaRegs.SPICTL.bit.TALK = 1;           // Enable Transmit path
SpiaRegs.SPITXBUF = data; // Master transmits data
while(SpiaRegs.SPISTS.bit.INT_FLAG !=1) {} // Waits until data rx'd
dummy = SpiaRegs.SPIRXBUF;               // Clears junk data from itself
                                         // bc it rx'd same data tx'd

```

To receive data in 3-wire master mode, the master must clear the TALK (SPICTL.1) bit to 0 to close the transmit path and then transmit dummy data in order to initiate the transfer from the slave. Because the TALK bit is 0, unlike in transmit mode, the master dummy data does not appear on the SPISIMOx pin, and the master does not receive its own dummy data. Instead, the data from the slave is received by the master.

Example 16-5. 3-Wire Master Mode Receive

```
Uint16 rdata;
Uint16 dummy;

SpiaRegs.SPICTL.bit.TALK = 0;           // Disable Transmit path
SpiaRegs.SPITXBUF = dummy;             // Send dummy to start tx
// NOTE: because TALK = 0, data does not tx onto SPISIMOA pin
while(SpiaRegs.SPISTS.bit.INT_FLAG !=1) {} // Wait until data received
rdata = SpiaRegs.SPIRXBUF;             // Master reads data
```

In 3-wire slave mode, SPICLKx, SPISTEx, and SPISOMIx pins must be configured as SPI pins (SPISIMOx pin can be configured as non-SPI pin). Like in master mode, when transmitting, the slave receives the data it transmits and must clear this junk data from its receive buffer.

Example 16-6. 3-Wire Slave Mode Transmit

```
Uint16 data;
Uint16 dummy;
SpiaRegs.SPICTL.bit.TALK = 1;           // Enable Transmit path
SpiaRegs.SPITXBUF = data;              // Slave transmits data
while(SpiaRegs.SPISTS.bit.INT_FLAG !=1) {} // Wait until data rx'd
dummy = SpiaRegs.SPIRXBUF;            // Clears junk data from itself
```

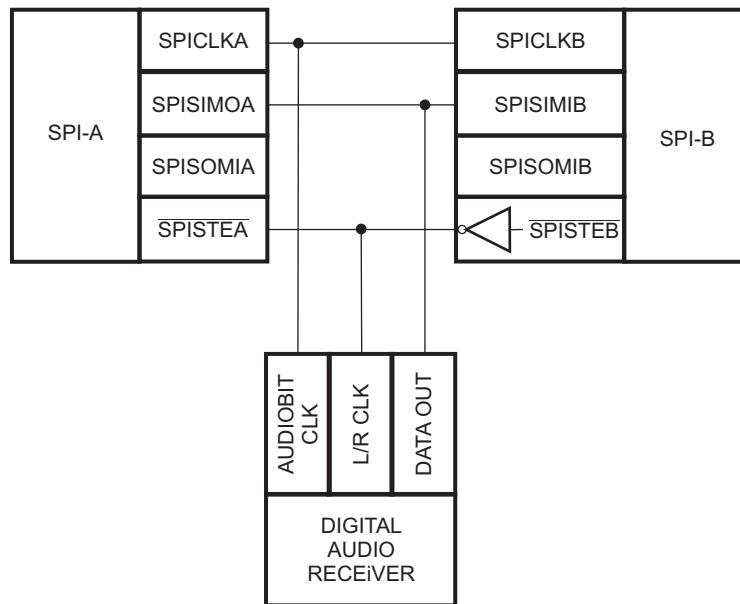
As in 3-wire master mode, the TALK bit must be cleared to 0. Otherwise, the slave receives data normally.

Example 16-7. - 3-Wire Slave Mode Receive

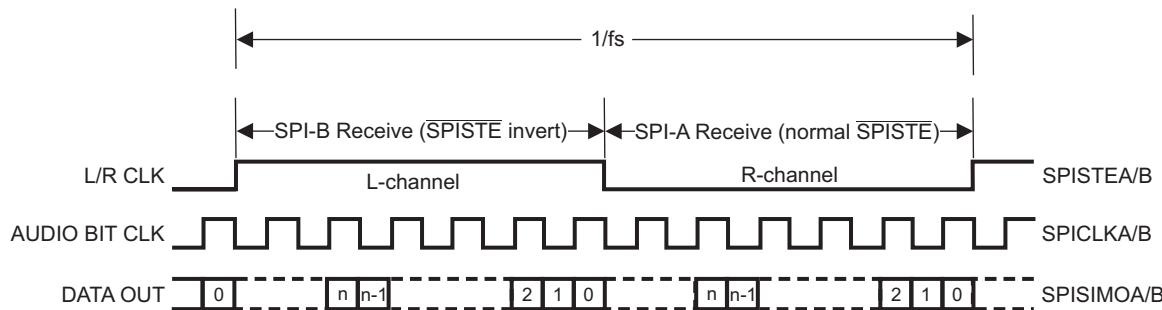
```
Uint16 rdata;
SpiaRegs.SPICTL.bit.TALK = 0;           // Disable Transmit path
while(SpiaRegs.SPISTS.bit.INT_FLAG !=1) {} // Waits until data rx'd
rdata = SpiaRegs.SPIRXBUF;             // Slave reads data
```

16.1.9 SPI STEINV Bit in Digital Audio Transfers

On those devices with two SPI modules, enabling the STEINV bit (SPIPRI.1) on one of the SPI modules allows the pair of SPIs to receive both left and right-channel digital audio data in slave mode. The SPI module that receives a normal active-low SPISTE signal stores right-channel data, and the SPI module that receives an inverted active-high SPISTE signal stores left-channel data from the master. To receive digital audio data from a digital audio interface receiver, the SPI modules can be connected as shown in Figure 16-10.

Figure 16-10. SPI Digital Audio Receiver Configuration Using 2 SPIs

Standard 28x SPI timing requirements limit the number of digital audio interface formats supported using the 2-SPI configuration with the STEINV bit. See your device-specific data sheet electricals for SPI timing requirements. With the SPI clock phase configured such that the CLOCK POLARITY (SPICCR.6) bit is 0 and the CLOCK PHASE (SPICCTL.3) bit is 1 (data latched on rising edge of clock), standard right-justified digital audio interface data format is supported as shown in [Figure 16-11](#).

Figure 16-11. Standard Right-Justified Digital Audio Data Format

16.2 SPI Waveforms

The SPI waveforms are shown in [Figure 16-12](#) through [Figure 16-17](#).

Figure 16-12. CLOCK POLARITY = 0, CLOCK PHASE = 0 (All data transitions are during the rising edge, non-delayed clock. Inactive level is low.)

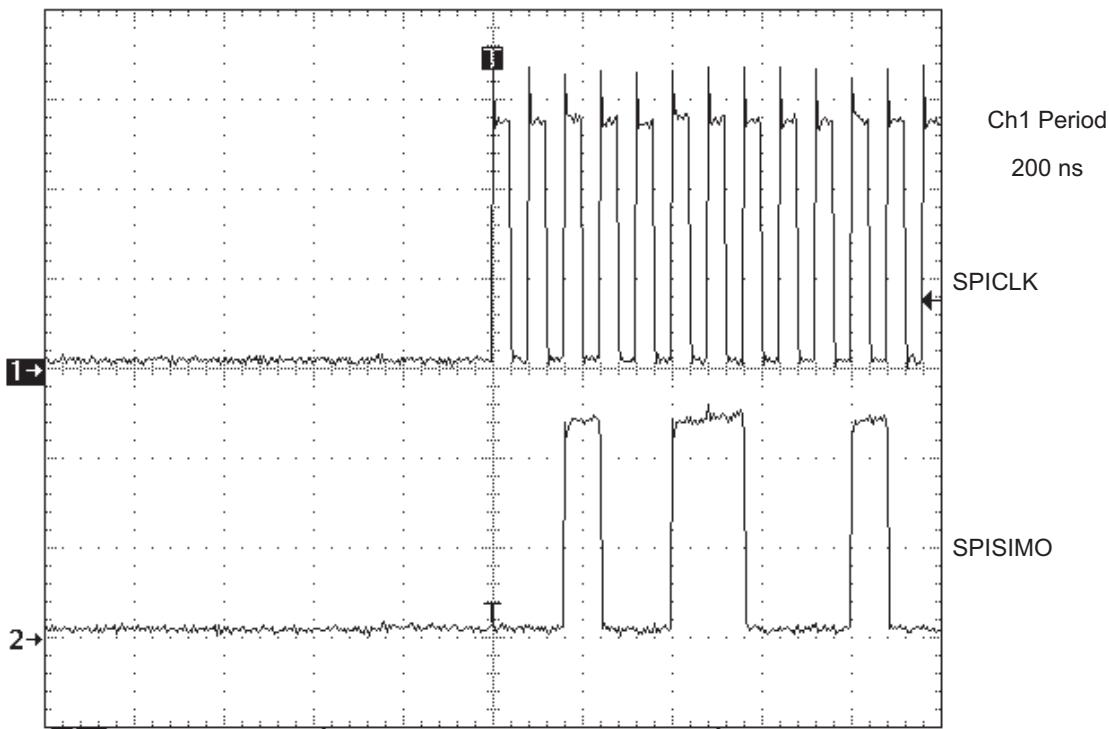
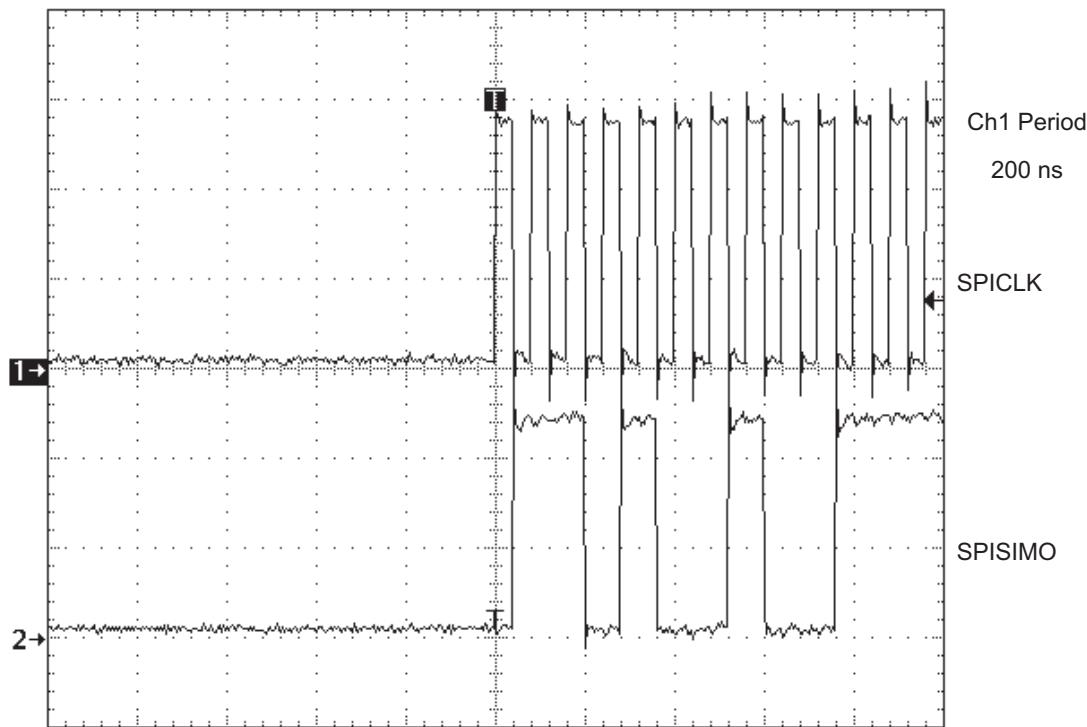


Figure 16-13. CLOCK POLARITY = 0, CLOCK PHASE = 1 (All data transitions are during the rising edge, but delayed by half clock cycle. Inactive level is low.)



**Figure 16-14. CLOCK POLARITY = 1, CLOCK PHASE = 0 (All data transitions are during the falling edge.
Inactive level is high.)**

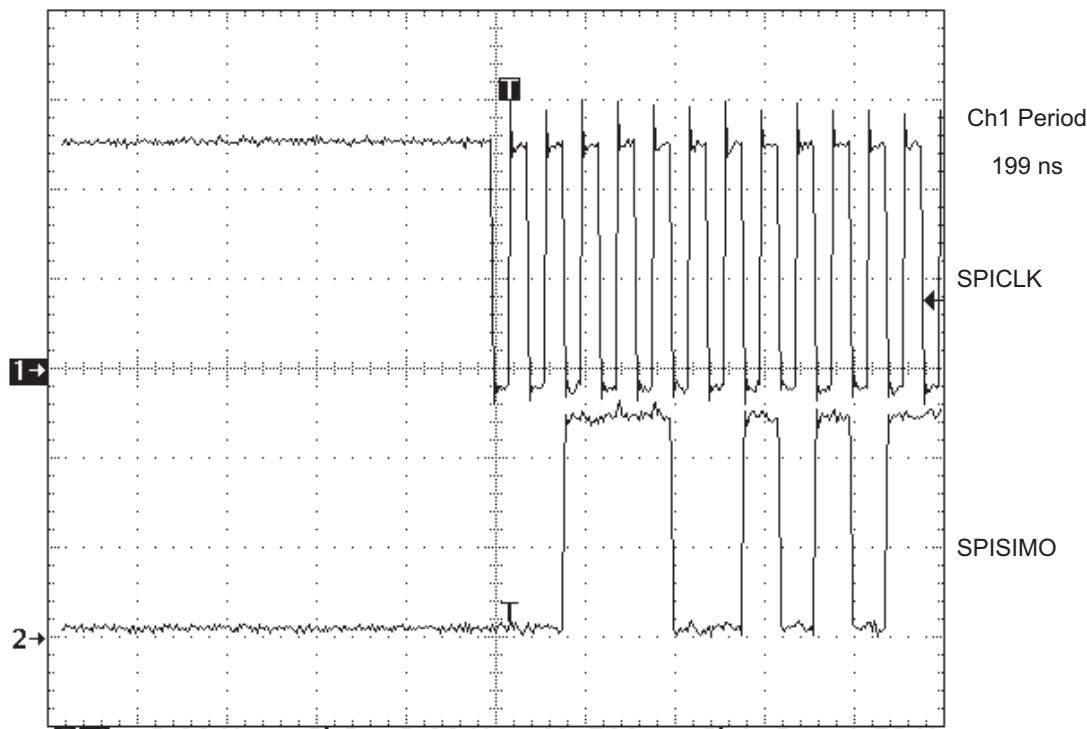


Figure 16-15. CLOCK POLARITY = 1, CLOCK PHASE = 1 (All data transitions are during the falling edge, but delayed by half clock cycle. Inactive level is high.)

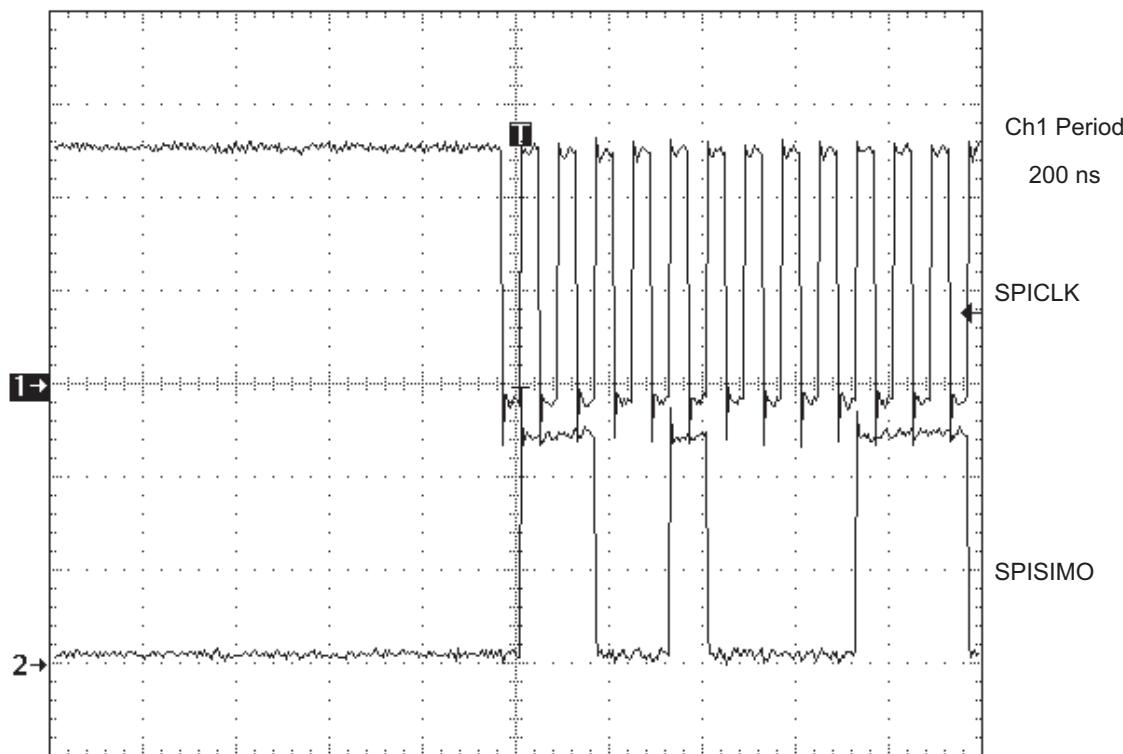


Figure 16-16. SPISTE Behavior in Master Mode (Master lowers SPISTE during the entire 16 bits of transmission.)

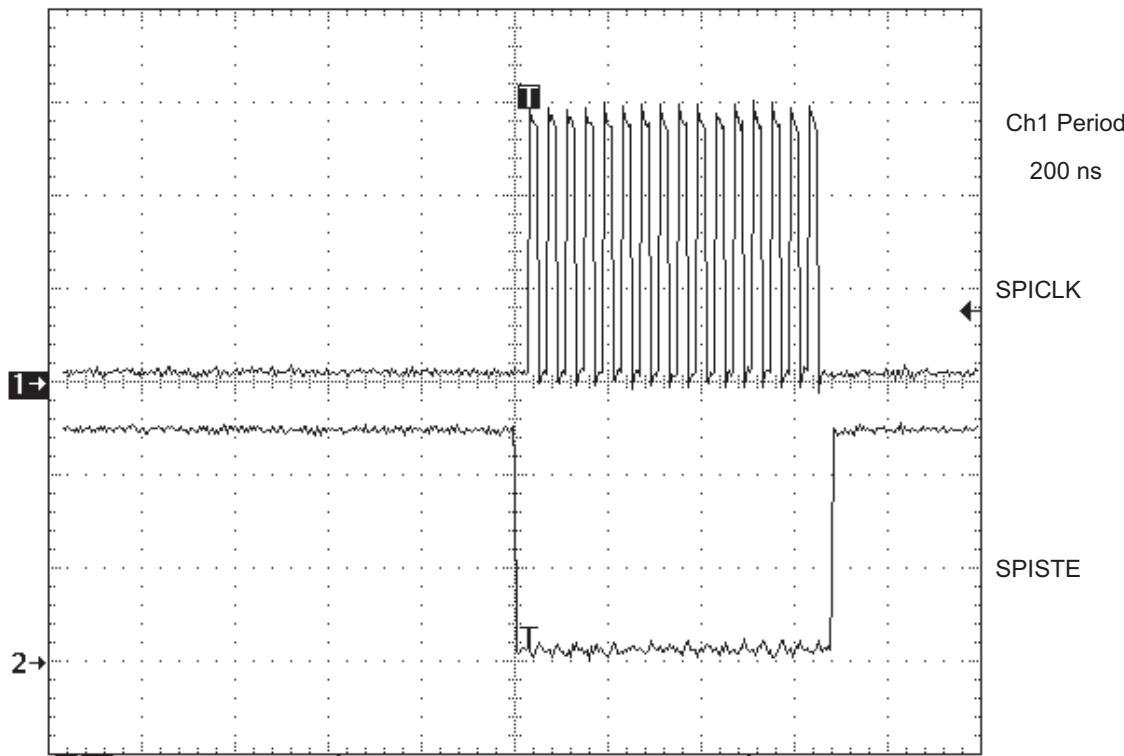
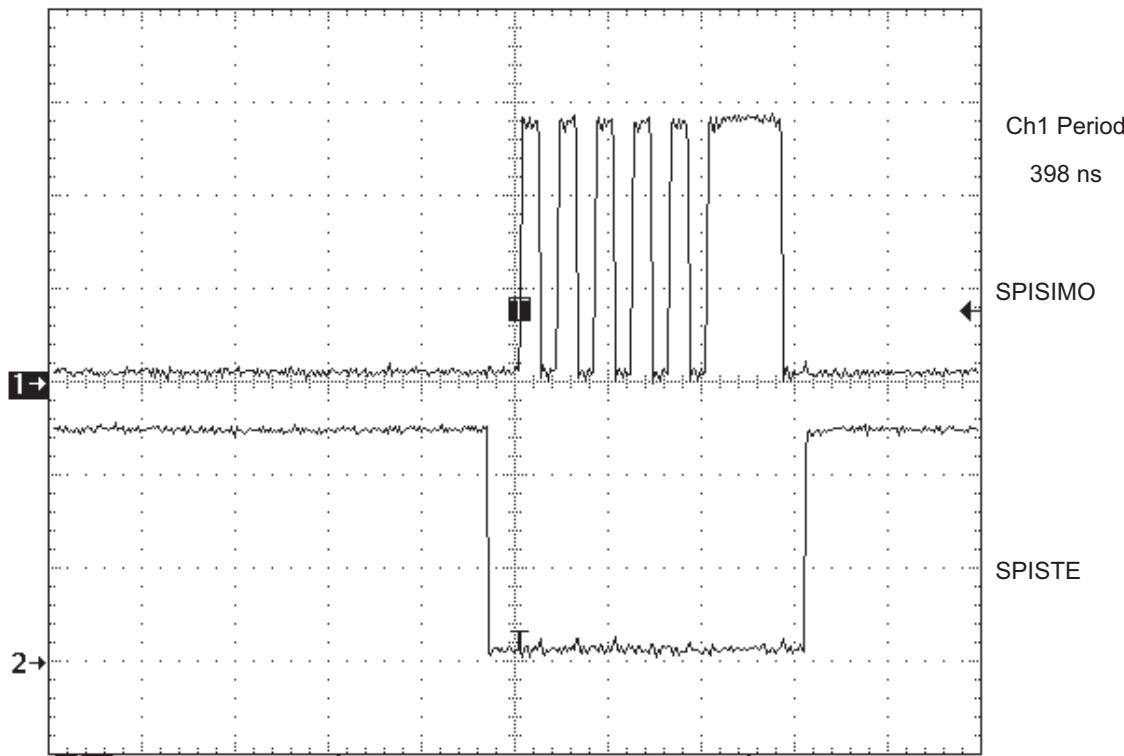


Figure 16-17. SPISTE Behavior in Slave Mode (Slave's SPISTE is lowered during the entire 16 bits of transmission.)



16.3 Registers

16.3.1 SPI Base Addresses

The base addresses for SPI are shown in [Table 16-7](#).

Table 16-7. SPI Base Address Table

Device Registers	Register Name	Start Address	End Address
SpiaRegs	SPI_REGS	0x0000_6100	0x0000_610F
SpibRegs	SPI_REGS	0x0000_6110	0x0000_611F
SpicRegs	SPI_REGS	0x0000_6120	0x0000_612F

16.3.2 SPI_REGS Registers

Table 16-8 lists the memory-mapped registers for the SPI_REGS. All register offset addresses not listed in Table 16-8 should be considered as reserved locations and the register contents should not be modified.

Table 16-8. SPI_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	SPICCR	SPI Configuration Control Register	Section 16.3.2.1	
1h	SPICTL	SPI Operation Control Register	Section 16.3.2.2	
2h	SPISTS	SPI Status Register	Section 16.3.2.3	
4h	SPIBRR	SPI Baud Rate Register	Section 16.3.2.4	
6h	SPIRXEMU	SPI Emulation Buffer Register	Section 16.3.2.5	
7h	SPIRXBUF	SPI Serial Input Buffer Register	Section 16.3.2.6	
8h	SPITXBUF	SPI Serial Output Buffer Register	Section 16.3.2.7	
9h	SPIDAT	SPI Serial Data Register	Section 16.3.2.8	
Ah	SPIFFTX	SPI FIFO Transmit Register	Section 16.3.2.9	
Bh	SPIFFRX	SPI FIFO Receive Register	Section 16.3.2.10	
Ch	SPIFFCT	SPI FIFO Control Register	Section 16.3.2.11	
Fh	SPIPRI	SPI Priority Control Register	Section 16.3.2.12	

16.3.2.1 SPICCR Register (offset = 0h) [reset = 0h]

SPICCR is shown in [Figure 16-18](#) and described in [Table 16-9](#).

SPI Configuration Control Register

Figure 16-18. SPICCR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SPISWRESET	CLKPOLARITY	RESERVED	SPILBK	SPICCHAR			
R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-9. SPICCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	SPISWRESET	R/W	0h	<p>SPI Software Reset</p> <p>When changing configuration, you should clear this bit before the changes and set this bit before resuming operation.</p> <p>0h (R/W) = Initializes the SPI operating flags to the reset condition. Specifically, the RECEIVER OVERRUN Flag bit (SPISTS.7), the SPI INT FLAG bit (SPISTS.6), and the TXBUF FULL Flag bit (SPISTS.5) are cleared. The SPI configuration remains unchanged.</p> <p>1h (R/W) = SPI is ready to transmit or receive the next character. When the SPI SW RESET bit is a 0, a character written to the transmitter will not be shifted out when this bit is set. A new character must be written to the serial data register.</p>
6	CLKPOLARITY	R	0h	<p>Shift Clock Polarity</p> <p>This bit controls the polarity of the SPICLK signal. CLOCK POLARITY and POLARITY CLOCK PHASE (SPICTL.3) control four clocking schemes on the SPICLK pin.</p> <p>0h (R/W) = Data is output on rising edge and input on falling edge. When no SPI data is sent, SPICLK is at low level. The data input and output edges depend on the value of the CLOCK PHASE bit (SPICTL.3) as follows:</p> <ul style="list-style-type: none"> - CLOCK PHASE = 0: Data is output on the rising edge of the SPICLK signal. Input data is latched on the falling edge of the SPICLK signal. - CLOCK PHASE = 1: Data is output one half-cycle before the first rising edge of the SPICLK signal and on subsequent falling edges of the SPICLK signal. Input data is latched on the rising edge of the SPICLK signal. <p>1h (R/W) = Data is output on falling edge and input on rising edge. When no SPI data is sent, SPICLK is at high level. The data input and output edges depend on the value of the CLOCK PHASE bit (SPICTL.3) as follows:</p> <ul style="list-style-type: none"> - CLOCK PHASE = 0: Data is output on the falling edge of the SPICLK signal. Input data is latched on the rising edge of the SPICLK signal. - CLOCK PHASE = 1: Data is output one half-cycle before the first falling edge of the SPICLK signal and on subsequent rising edges of the SPICLK signal. Input data is latched on the falling edge of the SPICLK signal.
5	RESERVED	R	0h	Reserved

Table 16-9. SPICCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SPILBK	R/W	0h	<p>SPI Loopback Mode Select</p> <p>Loopback mode allows module validation during device testing. This mode is valid only in master mode of the SPI.</p> <p>0h (R/W) = SPI loopback mode disabled. This is the default value after reset.</p> <p>1h (R/W) = SPI loopback mode enabled, SI MO/SOMI lines are connected internally. Used for module self-tests.</p>
3-0	SPICHAR	R/W	0h	<p>Character Length Control Bits</p> <p>These four bits determine the number of bits to be shifted in or SPI CHAR0 out as a single character during one shift sequence.</p>

16.3.2.2 SPICTL Register (offset = 1h) [reset = 0h]

SPICTL is shown in [Figure 16-19](#) and described in [Table 16-10](#).

SPI Operation Control Register

Figure 16-19. SPICTL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
RESERVED		OVERRUNINT ENA	CLK_PHASE	MASTER_SLA VE	TALK	SPIINTENA	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-10. SPICTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	OVERRUNINTENA	R/W	0h	<p>Overrun Interrupt Enable</p> <p>Overrun Interrupt Enable. Setting this bit causes an interrupt to be generated when the RECEIVER OVERRUN Flag bit (SPISTS.7) is set by hardware. Interrupts generated by the RECEIVER OVERRUN Flag bit and the SPI INT FLAG bit (SPISTS.6) share the same interrupt vector.</p> <p>0h (R/W) = Disable RECEIVER OVERRUN interrupts.</p> <p>1h (R/W) = Enable RECEIVER_OVERRUN interrupts.</p>
3	CLK_PHASE	R/W	0h	<p>SPI Clock Phase Select</p> <p>This bit controls the phase of the SPICLK signal. CLOCK PHASE and CLOCK POLARITY (SPICCR.6) make four different clocking schemes possible (see clocking figures in SPI chapter). When operating with CLOCK PHASE high, the SPI (master or slave) makes the first bit of data available after SPIDAT is written and before the first edge of the SPICLK signal, regardless of which SPI mode is being used.</p> <p>0h (R/W) = Normal SPI clocking scheme, depending on the CLOCK POLARITY bit (SPICCR.6).</p> <p>1h (R/W) = SPICLK signal delayed by one half-cycle. Polarity determined by the CLOCK POLARITY bit.</p>
2	MASTER_SLAVE	R/W	0h	<p>SPI Network Mode Control</p> <p>This bit determines whether the SPI is a network master or slave. SLAVE During reset initialization, the SPI is automatically configured as a network slave.</p> <p>0h (R/W) = SPI is configured as a slave.</p> <p>1h (R/W) = SPI is configured as a master.</p>

Table 16-10. SPICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TALK	R/W	0h	<p>Transmit Enable</p> <p>The TALK bit can disable data transmission (master or slave) by placing the serial data output in the high-impedance state. If this bit is disabled during a transmission, the transmit shift register continues to operate until the previous character is shifted out. When the TALK bit is disabled, the SPI is still able to receive characters and update the status flags. TALK is cleared (disabled) by a system reset.</p> <p>0h (R/W) = Disables transmission:</p> <ul style="list-style-type: none"> - Slave mode operation: If not previously configured as a general-purpose I/O pin, the SPISOMI pin will be put in the high-impedance state. - Master mode operation: If not previously configured as a general-purpose I/O pin, the SPISIMO pin will be put in the high-impedance state. <p>1h (R/W) = Enables transmission For the 4-pin option, ensure to enable the receiver's SPISTE_n input pin.</p>
0	SPIINTENA	R/W	0h	<p>SPI Interrupt Enable</p> <p>This bit controls the SPI's ability to generate a transmit/receive interrupt. The SPI INT FLAG bit (SPISTS.6) is unaffected by this bit.</p> <p>0h (R/W) = Disables the interrupt.</p> <p>1h (R/W) = Enables the interrupt.</p>

16.3.2.3 SPISTS Register (offset = 2h) [reset = 0h]

SPISTS is shown in [Figure 16-20](#) and described in [Table 16-11](#).

SPI Status Register

Figure 16-20. SPISTS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
OVERRUN_FLAG	INT_FLAG	BUFFULL_FLAG					RESERVED
W1toClr-0h	RtoClr-0h	RtoClr-0h					R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-11. SPISTS Register Field Descriptions

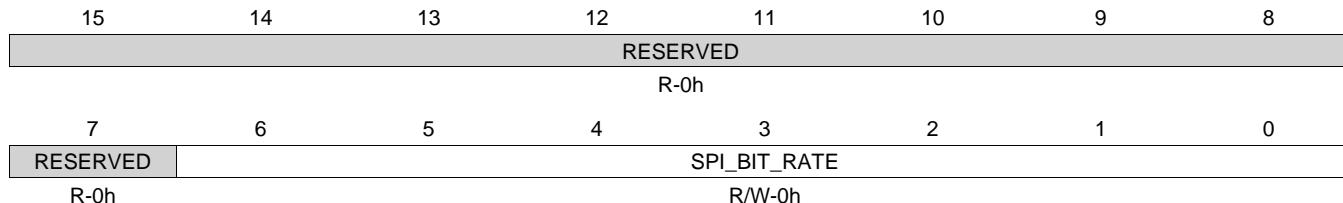
Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	OVERRUN_FLAG	W1toClr	0h	<p>SPI Receiver Overrun Flag</p> <p>This bit is a read/clear-only flag. The SPI hardware sets this bit when a receive or transmit operation completes before the previous character has been read from the buffer. The bit is cleared in one of three ways:</p> <ul style="list-style-type: none"> - Writing a 1 to this bit - Writing a 0 to SPI SW RESET (SPICCR.7) - Resetting the system <p>If the OVERRUN INT ENA bit (SPICTL.4) is set, the SPI requests only one interrupt upon the first occurrence of setting the RECEIVER OVERRUN Flag bit. Subsequent overruns will not request additional interrupts if this flag bit is already set. This means that in order to allow new overrun interrupt requests the user must clear this flag bit by writing a 1 to SPISTS.7 each time an overrun condition occurs. In other words, if the RECEIVER OVERRUN Flag bit is left set (not cleared) by the interrupt service routine, another overrun interrupt will not be immediately re-entered when the interrupt service routine is exited.</p> <p>0h (R/W) = A receive overrun condition has not occurred. 1h (R/W) = The last received character has been overwritten and therefore lost (when the SPIRXBUF was overwritten by the SPI module before the previous character was read by the user application).</p> <p>Writing a '1' will clear this bit. The RECEIVER OVERRUN Flag bit should be cleared during the interrupt service routine because the RECEIVER OVERRUN Flag bit and SPI INT FLAG bit (SPISTS.6) share the same interrupt vector. This will alleviate any possible doubt as to the source of the interrupt when the next byte is received.</p>
6	INT_FLAG	RtoClr	0h	<p>SPI Interrupt Flag</p> <p>SPI INT FLAG is a read-only flag. Hardware sets this bit to indicate that the SPI has completed sending or receiving the last bit and is ready to be serviced. This flag causes an interrupt to be requested if the SPI INT ENA bit (SPICTL.0) is set. The received character is placed in the receiver buffer at the same time this bit is set. This bit is cleared in one of three ways:</p> <ul style="list-style-type: none"> - Reading SPIRXBUF - Writing a 0 to SPI SW RESET (SPICCR.7) - Resetting the system <p>0h (R/W) = No full words have been received or transmitted. 1h (R/W) = Indicates that the SPI has completed sending or receiving the last bit and is ready to be serviced.</p>

Table 16-11. SPISTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	BUFFULL_FLAG	RtoClr	0h	<p>SPI Transmit Buffer Full Flag</p> <p>This read-only bit gets set to 1 when a character is written to the SPI Transmit buffer SPITXBUF. It is cleared when the character is automatically loaded into SPIDAT when the shifting out of a previous character is complete.</p> <p>0h (R/W) = Transmit buffer is not full. 1h (R/W) = Transmit buffer is full.</p>
4-0	RESERVED	R	0h	Reserved

16.3.2.4 SPIBRR Register (offset = 4h) [reset = 0h]SPIBRR is shown in [Figure 16-21](#) and described in [Table 16-12](#).

SPI Baud Rate Register

Figure 16-21. SPIBRR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-12. SPIBRR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved

Table 16-12. SPIBRR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	SPI_BIT_RATE	R/W	0h	<p>SPI Baud Rate Control</p> <p>These bits determine the bit transfer rate if the SPI is the network SPI BIT RATE 0 master. There are 125 data-transfer rates (each a function of the CPU clock, LSPCLK) that can be selected. One data bit is shifted per SPICLK cycle. (SPICLK is the baud rate clock output on the SPICLK pin.)</p> <p>If the SPI is a network slave, the module receives a clock on the SPICLK pin from the network master. Therefore, these bits have no effect on the SPICLK signal. The frequency of the input clock from the master should not exceed the slave SPI's SPICLK signal divided by 4.</p> <p>In master mode, the SPI clock is generated by the SPI and is output on the SPICLK pin. The SPI baud rates are determined by the following formula:</p> <p>For SPIBRR = 3 to 127: SPI Baud Rate = LSPCLK / (SPIBRR + 1)</p> <p>For SPIBRR = 0, 1, or 2: SPI Baud Rate = LSPCLK / 4</p> <p>where: LSPCLK = Function of CPU clock frequency X low-speed peripheral clock of the device SPIBRR = Contents of the SPIBRR in the master SPI device.</p> <p>3h (R/W) = SPI Baud Rate = LSPCLK/4 4h (R/W) = SPI Baud Rate = LSPCLK/5 5h (R/W) = SPI Baud Rate = LSPCLK/6 6h (R/W) = SPI Baud Rate = LSPCLK/7 7h (R/W) = SPI Baud Rate = LSPCLK/8 8h (R/W) = SPI Baud Rate = LSPCLK/9 9h (R/W) = SPI Baud Rate = LSPCLK/10 Ah (R/W) = SPI Baud Rate = LSPCLK/11 Bh (R/W) = SPI Baud Rate = LSPCLK/12 Ch (R/W) = SPI Baud Rate = LSPCLK/13 Dh (R/W) = SPI Baud Rate = LSPCLK/14 Eh (R/W) = SPI Baud Rate = LSPCLK/15 Fh (R/W) = SPI Baud Rate = LSPCLK/16 10h (R/W) = SPI Baud Rate = LSPCLK/17 11h (R/W) = SPI Baud Rate = LSPCLK/18 12h (R/W) = SPI Baud Rate = LSPCLK/19 13h (R/W) = SPI Baud Rate = LSPCLK/20 14h (R/W) = SPI Baud Rate = LSPCLK/21 15h (R/W) = SPI Baud Rate = LSPCLK/22 16h (R/W) = SPI Baud Rate = LSPCLK/23 17h (R/W) = SPI Baud Rate = LSPCLK/24 18h (R/W) = SPI Baud Rate = LSPCLK/25 19h (R/W) = SPI Baud Rate = LSPCLK/26 1Ah (R/W) = SPI Baud Rate = LSPCLK/27 1Bh (R/W) = SPI Baud Rate = LSPCLK/28 1Ch (R/W) = SPI Baud Rate = LSPCLK/29 1Dh (R/W) = SPI Baud Rate = LSPCLK/30 1Eh (R/W) = SPI Baud Rate = LSPCLK/31 1Fh (R/W) = SPI Baud Rate = LSPCLK/32 20h (R/W) = SPI Baud Rate = LSPCLK/33 21h (R/W) = SPI Baud Rate = LSPCLK/34 22h (R/W) = SPI Baud Rate = LSPCLK/35 23h (R/W) = SPI Baud Rate = LSPCLK/36 24h (R/W) = SPI Baud Rate = LSPCLK/37 25h (R/W) = SPI Baud Rate = LSPCLK/38 26h (R/W) = SPI Baud Rate = LSPCLK/39 27h (R/W) = SPI Baud Rate = LSPCLK/40 28h (R/W) = SPI Baud Rate = LSPCLK/41 29h (R/W) = SPI Baud Rate = LSPCLK/42</p>

Table 16-12. SPIBRR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Ah (R/W) = SPI Baud Rate = LSPCLK/43
				2Bh (R/W) = SPI Baud Rate = LSPCLK/44
				2Ch (R/W) = SPI Baud Rate = LSPCLK/45
				2Dh (R/W) = SPI Baud Rate = LSPCLK/46
				2Eh (R/W) = SPI Baud Rate = LSPCLK/47
				2Fh (R/W) = SPI Baud Rate = LSPCLK/48
				30h (R/W) = SPI Baud Rate = LSPCLK/49
				31h (R/W) = SPI Baud Rate = LSPCLK/50
				32h (R/W) = SPI Baud Rate = LSPCLK/51
				33h (R/W) = SPI Baud Rate = LSPCLK/52
				34h (R/W) = SPI Baud Rate = LSPCLK/53
				35h (R/W) = SPI Baud Rate = LSPCLK/54
				36h (R/W) = SPI Baud Rate = LSPCLK/55
				37h (R/W) = SPI Baud Rate = LSPCLK/56
				38h (R/W) = SPI Baud Rate = LSPCLK/57
				39h (R/W) = SPI Baud Rate = LSPCLK/58
				3Ah (R/W) = SPI Baud Rate = LSPCLK/59
				3Bh (R/W) = SPI Baud Rate = LSPCLK/60
				3Ch (R/W) = SPI Baud Rate = LSPCLK/61
				3Dh (R/W) = SPI Baud Rate = LSPCLK/62
				3Eh (R/W) = SPI Baud Rate = LSPCLK/63
				3Fh (R/W) = SPI Baud Rate = LSPCLK/64
				40h (R/W) = SPI Baud Rate = LSPCLK/65
				41h (R/W) = SPI Baud Rate = LSPCLK/66
				42h (R/W) = SPI Baud Rate = LSPCLK/67
				43h (R/W) = SPI Baud Rate = LSPCLK/68
				44h (R/W) = SPI Baud Rate = LSPCLK/69
				45h (R/W) = SPI Baud Rate = LSPCLK/70
				46h (R/W) = SPI Baud Rate = LSPCLK/71
				47h (R/W) = SPI Baud Rate = LSPCLK/72
				48h (R/W) = SPI Baud Rate = LSPCLK/73
				49h (R/W) = SPI Baud Rate = LSPCLK/74
				4Ah (R/W) = SPI Baud Rate = LSPCLK/75
				4Bh (R/W) = SPI Baud Rate = LSPCLK/76
				4Ch (R/W) = SPI Baud Rate = LSPCLK/77
				4Dh (R/W) = SPI Baud Rate = LSPCLK/78
				4Eh (R/W) = SPI Baud Rate = LSPCLK/79
				4Fh (R/W) = SPI Baud Rate = LSPCLK/80
				50h (R/W) = SPI Baud Rate = LSPCLK/81
				51h (R/W) = SPI Baud Rate = LSPCLK/82
				52h (R/W) = SPI Baud Rate = LSPCLK/83
				53h (R/W) = SPI Baud Rate = LSPCLK/84
				54h (R/W) = SPI Baud Rate = LSPCLK/85
				55h (R/W) = SPI Baud Rate = LSPCLK/86
				56h (R/W) = SPI Baud Rate = LSPCLK/87
				57h (R/W) = SPI Baud Rate = LSPCLK/88
				58h (R/W) = SPI Baud Rate = LSPCLK/89
				59h (R/W) = SPI Baud Rate = LSPCLK/90
				5Ah (R/W) = SPI Baud Rate = LSPCLK/91
				5Bh (R/W) = SPI Baud Rate = LSPCLK/92
				5Ch (R/W) = SPI Baud Rate = LSPCLK/93
				5Dh (R/W) = SPI Baud Rate = LSPCLK/94
				5Eh (R/W) = SPI Baud Rate = LSPCLK/95
				5Fh (R/W) = SPI Baud Rate = LSPCLK/96
				60h (R/W) = SPI Baud Rate = LSPCLK/97
				61h (R/W) = SPI Baud Rate = LSPCLK/98

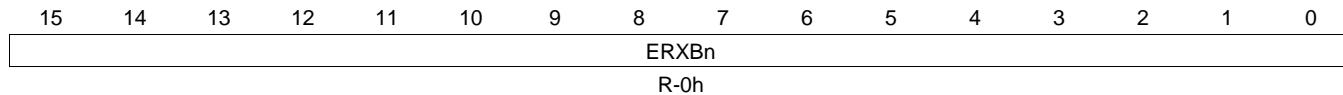
Table 16-12. SPIBRR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				62h (R/W) = SPI Baud Rate = LSPCLK/99
				63h (R/W) = SPI Baud Rate = LSPCLK/100
				64h (R/W) = SPI Baud Rate = LSPCLK/101
				65h (R/W) = SPI Baud Rate = LSPCLK/102
				66h (R/W) = SPI Baud Rate = LSPCLK/103
				67h (R/W) = SPI Baud Rate = LSPCLK/104
				68h (R/W) = SPI Baud Rate = LSPCLK/105
				69h (R/W) = SPI Baud Rate = LSPCLK/106
				6Ah (R/W) = SPI Baud Rate = LSPCLK/107
				6Bh (R/W) = SPI Baud Rate = LSPCLK/108
				6Ch (R/W) = SPI Baud Rate = LSPCLK/109
				6Dh (R/W) = SPI Baud Rate = LSPCLK/110
				6Eh (R/W) = SPI Baud Rate = LSPCLK/111
				6Fh (R/W) = SPI Baud Rate = LSPCLK/112
				70h (R/W) = SPI Baud Rate = LSPCLK/113
				71h (R/W) = SPI Baud Rate = LSPCLK/114
				72h (R/W) = SPI Baud Rate = LSPCLK/115
				73h (R/W) = SPI Baud Rate = LSPCLK/116
				74h (R/W) = SPI Baud Rate = LSPCLK/117
				75h (R/W) = SPI Baud Rate = LSPCLK/118
				76h (R/W) = SPI Baud Rate = LSPCLK/119
				77h (R/W) = SPI Baud Rate = LSPCLK/120
				78h (R/W) = SPI Baud Rate = LSPCLK/121
				79h (R/W) = SPI Baud Rate = LSPCLK/122
				7Ah (R/W) = SPI Baud Rate = LSPCLK/123
				7Bh (R/W) = SPI Baud Rate = LSPCLK/124
				7Ch (R/W) = SPI Baud Rate = LSPCLK/125
				7Dh (R/W) = SPI Baud Rate = LSPCLK/126
				7Eh (R/W) = SPI Baud Rate = LSPCLK/127
				7Fh (R/W) = SPI Baud Rate = LSPCLK/128

16.3.2.5 SPIRXEMU Register (offset = 6h) [reset = 0h]

SPIRXEMU is shown in [Figure 16-22](#) and described in [Table 16-13](#).

SPI Emulation Buffer Register

Figure 16-22. SPIRXEMU Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

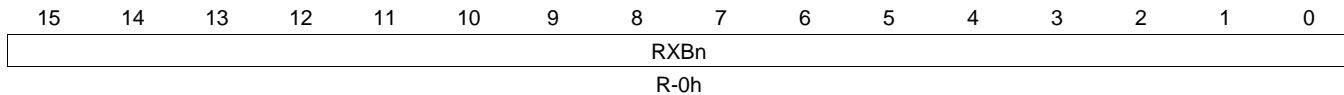
Table 16-13. SPIRXEMU Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ERXBn	R	0h	<p>Emulation Buffer Received Data</p> <p>SPIRXEMU functions almost identically to SPIRXBUF, except that reading SPIRXEMU does not clear the SPI INT FLAG bit (SPISTS.6). Once the SPIDAT has received the complete character, the character is transferred to SPIRXEMU and SPIRXBUF, where it can be read. At the same time, SPI INT FLAG is set.</p> <p>This mirror register was created to support emulation. Reading SPIRXBUF clears the SPI INT FLAG bit (SPISTS.6). In the normal operation of the emulator, the control registers are read to continually update the contents of these registers on the display screen. SPIRXEMU was created so that the emulator can read this register and properly update the contents on the display screen. Reading SPIRXEMU does not clear the SPI INT FLAG bit, but reading SPIRXBUF clears this flag. In other words, SPIRXEMU enables the emulator to emulate the true operation of the SPI more accurately.</p> <p>It is recommended that you view SPIRXEMU in the normal emulator run mode.</p>

16.3.2.6 SPIRXBUF Register (offset = 7h) [reset = 0h]

SPIRXBUF is shown in [Figure 16-23](#) and described in [Table 16-14](#).

SPI Serial Input Buffer Register

Figure 16-23. SPIRXBUF Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-14. SPIRXBUF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RXBn	R	0h	<p>Received Data</p> <p>Once SPIDAT has received the complete character, the character is transferred to SPIRXBUF, where it can be read. At the same time, the SPI INT FLAG bit (SPISTS.6) is set. Since data is shifted into the SPI's most significant bit first, it is stored right-justified in this register.</p>

16.3.2.7 SPITXBUF Register (offset = 8h) [reset = 0h]SPITXBUF is shown in [Figure 16-24](#) and described in [Table 16-15](#).

SPI Serial Output Buffer Register

Figure 16-24. SPITXBUF Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXBn															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

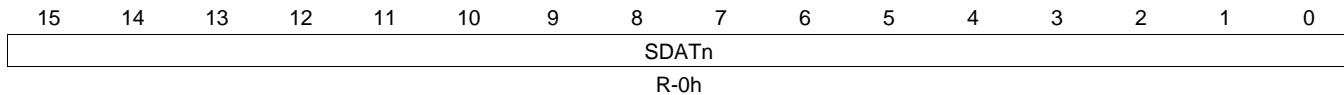
Table 16-15. SPITXBUF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TXBn	R/W	0h	<p>Transmit Data Buffer</p> <p>This is where the next character to be transmitted is stored. When the transmission of the current character has completed, if the TX BUF FULL Flag bit is set, the contents of this register is automatically transferred to SPIDAT, and the TX BUF FULL Flag is cleared. Writes to SPITXBUF must be left-justified.</p>

16.3.2.8 SPIDAT Register (offset = 9h) [reset = 0h]

SPIDAT is shown in [Figure 16-25](#) and described in [Table 16-16](#).

SPI Serial Data Register

Figure 16-25. SPIDAT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-16. SPIDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDATn	R	0h	<p>Serial Data Shift Register</p> <ul style="list-style-type: none"> - It provides data to be output on the serial output pin if the TALK bit (SPICTL.1) is set. - When the SPI is operating as a master, a data transfer is initiated. When initiating a transfer, see the CLOCK POLARITY bit (SPICCR.6) described in Section 10.2.1.1 and the CLOCK PHASE bit (SPICTL.3) described in Section 10.2.1.2, for the requirements. <p>In master mode, writing dummy data to SPIDAT initiates a receiver sequence. Since the data is not hardware-justified for characters shorter than sixteen bits, transmit data must be written in left-justified form, and received data read in right-justified form.</p>

16.3.2.9 SPIFFTX Register (offset = Ah) [reset = A000h]

SPIFFTX is shown in [Figure 16-26](#) and described in [Table 16-17](#).

SPI FIFO Transmit Register

Figure 16-26. SPIFFTX Register

15	14	13	12	11	10	9	8
SPIRST	SPIFFENA	TXFIFO			TXFFST		
R/W-1h	R/W-0h	R/W-1h			R-0h		
7	6	5	4	3	2	1	0
TXFFINT	TXFFINTCLR	TXFFIENA			TXFFIL		
R/W-0h	W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-17. SPIFFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPIRST	R/W	1h	SPI Reset 0h (R/W) = Write 0 to reset the SPI transmit and receive channels. The SPI FIFO register configuration bits will be left as is. 1h (R/W) = SPI FIFO can resume transmit or receive. No effect to the SPI registers bits.
14	SPIFFENA	R/W	0h	SPI FIFO Enhancements Enable 0h (R/W) = SPI FIFO enhancements are disabled. 1h (R/W) = SPI FIFO enhancements are enabled.
13	TXFIFO	R/W	1h	TX FIFO Reset 0h (R/W) = Write 0 to reset the FIFO pointer to zero, and hold in reset. 1h (R/W) = Release transmit FIFO from reset.
12-8	TXFFST	R	0h	Transmit FIFO Status 0h (R/W) = Transmit FIFO is empty. 1h (R/W) = Transmit FIFO has 1 word. 2h (R/W) = Transmit FIFO has 2 words. 3h (R/W) = Transmit FIFO has 3 words. 4h (R/W) = Transmit FIFO has 4 words, which is the maximum.
7	TXFFINT	R/W	0h	TX FIFO Interrupt Flag 0h (R/W) = TXFIFO interrupt has not occurred, This is a read-only bit. 1h (R/W) = TXFIFO interrupt has occurred, This is a read-only bit.
6	TXFFINTCLR	W	0h	TXFIFO Interrupt Clear 0h (R/W) = Write 0 has no effect on TXFIFINT flag bit, Bit reads back a zero. 1h (R/W) = Write 1 to clear SPIFFTX[TXFFINT] flag.
5	TXFFIENA	R/W	0h	TX FIFO Interrupt Enable 0h (R/W) = TX FIFO interrupt based on TXFFIL match (less than or equal to) will be disabled. 1h (R/W) = TX FIFO interrupt based on TXFFIL match (less than or equal to) will be enabled.

Table 16-17. SPIFFTX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	TXFFIL	R/W	0h	<p>Transmit FIFO Interrupt Level Bits</p> <p>Transmit FIFO will generate interrupt when the FIFO status bits (TXFFST4-0) and FIFO level bits (TXFFIL4-0) match (less than or equal to).</p> <p>0h (R/W) = A TX FIFO interrupt request is generated when there are no words remaining in the TX buffer.</p> <p>1h (R/W) = A TX FIFO interrupt request is generated when there is 1 word or no words remaining in the TX buffer.</p> <p>2h (R/W) = A TX FIFO interrupt request is generated when there are 2 words or fewer remaining in the TX buffer.</p> <p>3h (R/W) = A TX FIFO interrupt request is generated when there are 3 words or fewer remaining in the TX buffer.</p> <p>4h (R/W) = A TX FIFO interrupt request is generated when there are 4 words or fewer remaining in the TX buffer.</p> <p>5h (R/W) = A TX FIFO interrupt request is generated when there are 5 words or fewer remaining in the TX buffer.</p> <p>6h (R/W) = A TX FIFO interrupt request is generated when there are 6 words or fewer remaining in the TX buffer.</p> <p>7h (R/W) = A TX FIFO interrupt request is generated when there are 7 words or fewer remaining in the TX buffer.</p> <p>8h (R/W) = A TX FIFO interrupt request is generated when there are 8 words or fewer remaining in the TX buffer.</p> <p>9h (R/W) = A TX FIFO interrupt request is generated when there are 9 words or fewer remaining in the TX buffer.</p> <p>Ah (R/W) = A TX FIFO interrupt request is generated when there are 10 words or fewer remaining in the TX buffer.</p> <p>Bh (R/W) = A TX FIFO interrupt request is generated when there are 11 words or fewer remaining in the TX buffer.</p> <p>Ch (R/W) = A TX FIFO interrupt request is generated when there are 12 words or fewer remaining in the TX buffer.</p> <p>Dh (R/W) = A TX FIFO interrupt request is generated when there are 13 words or fewer remaining in the TX buffer.</p> <p>Eh (R/W) = A TX FIFO interrupt request is generated when there are 14 words or fewer remaining in the TX buffer.</p> <p>Fh (R/W) = A TX FIFO interrupt request is generated when there are 15 words or fewer remaining in the TX buffer.</p> <p>1Fh (R/W) = Reserved.</p>

16.3.2.10 SPIFFRX Register (offset = Bh) [reset = A000h]

SPIFFRX is shown in [Figure 16-27](#) and described in [Table 16-18](#).

SPI FIFO Receive Register

Figure 16-27. SPIFFRX Register

15	14	13	12	11	10	9	8
RXFFOVF	RXFFOVFCLR	RXFIFORESET			RXFFST		
R/W-1h	R/W-0h	R/W-1h			R-0h		
7	6	5	4	3	2	1	0
RXFFINT	RXFFINTCLR	RXFFIENA			RXFFIL		
R/W-0h	W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-18. SPIFFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RXFFOVF	R/W	1h	Receive FIFO Overflow Flag 0h (R/W) = Receive FIFO has not overflowed. This is a read-only bit. 1h (R/W) = Receive FIFO has overflowed, read-only bit. More than 16 words have been received in to the FIFO, and the first received word is lost.
14	RXFFOVFCLR	R/W	0h	Receive FIFO Overflow Clear 0h (R/W) = Write 0 does not affect RXFFOVF flag bit, Bit reads back a zero. 1h (R/W) = Write 1 to clear SPIFFRX[RXFFOVF].
13	RXFIFORESET	R/W	1h	Receive FIFO Reset 0h (R/W) = Write 0 to reset the FIFO pointer to zero, and hold in reset. 1h (R/W) = Re-enable receive FIFO operation.
12-8	RXFFST	R	0h	Receive FIFO Status 0h (R/W) = Receive FIFO is empty. 1h (R/W) = Receive FIFO has 1 word. 2h (R/W) = Receive FIFO has 2 words. 3h (R/W) = Receive FIFO has 3 words. 4h (R/W) = Receive FIFO has 4 words. 5h (R/W) = Receive FIFO has 5 words. 6h (R/W) = Receive FIFO has 6 words. 7h (R/W) = Receive FIFO has 7 words. 8h (R/W) = Receive FIFO has 8 words. 9h (R/W) = Receive FIFO has 9 words. Ah (R/W) = Receive FIFO has 10 words. Bh (R/W) = Receive FIFO has 11 words. Ch (R/W) = Receive FIFO has 12 words. Dh (R/W) = Receive FIFO has 13 words. Eh (R/W) = Receive FIFO has 14 words. Fh (R/W) = Receive FIFO has 15 words, which is the maximum.
7	RXFFINT	R/W	0h	Receive FIFO Interrupt Flag 0h (R/W) = RXFIFO interrupt has not occurred. This is a read-only bit. 1h (R/W) = RXFIFO interrupt has occurred. This is a read-only bit.
6	RXFFINTCLR	W	0h	Receive FIFO Interrupt Clear 0h (R/W) = Write 0 has no effect on RXFIFINT flag bit, Bit reads back a zero. 1h (R/W) = Write 1 to clear SPIFFRX[RXFFINT] flag

Table 16-18. SPIFFRX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RXFFIENA	R/W	0h	<p>RX FIFO Interrupt Enable</p> <p>0h (R/W) = RX FIFO interrupt based on RXFFIL match (greater than or equal to) will be disabled.</p> <p>1h (R/W) = RX FIFO interrupt based on RXFFIL match (greater than or equal to) will be enabled.</p>
4-0	RXFFIL	R/W	0h	<p>Receive FIFO Interrupt Level Bits</p> <p>11111 Receive FIFO generates an interrupt when the FIFO status bits (RXFFST4-0) are greater than or equal to the FIFO level bits (RXFFIL4-0). The default value of these bits after reset is 11111. This avoids frequent interrupts after reset, as the receive FIFO will be empty most of the time.</p> <p>1h (R/W) = A RX FIFO interrupt request is generated when there is 1 or more words in the RX buffer.</p> <p>2h (R/W) = A RX FIFO interrupt request is generated when there are 2 or more words in the RX buffer.</p> <p>3h (R/W) = A RX FIFO interrupt request is generated when there are 3 or more words in the RX buffer.</p> <p>4h (R/W) = A RX FIFO interrupt request is generated when there are 4 words in the RX buffer.</p>

16.3.2.11 SPIFFCT Register (offset = Ch) [reset = 0h]

SPIFFCT is shown in [Figure 16-28](#) and described in [Table 16-19](#).

SPI FIFO Control Register

Figure 16-28. SPIFFCT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
TXDLY							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-19. SPIFFCT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	TXDLY	R/W	0h	<p>FIFO Transmit Delay Bits</p> <p>These bits define the delay between every transfer from FIFO transmit buffer to transmit shift register. The delay is defined in number SPI serial clock cycles. The 8-bit register could define a minimum delay of 0 serial clock cycles and a maximum of 255 serial clock cycles. In FIFO mode, the buffer (TXBUF) between the shift register and the FIFO should be filled only after the shift register has completed shifting of the last bit. This is required to pass on the delay between transfers to the data stream. In the FIFO mode TXBUF should not be treated as one additional level of buffer.</p> <p>0h (R/W) = The next word in the TX FIFO buffer is transferred to SPITXBUF immediately upon completion of transmission of the previous word.</p> <p>1h (R/W) = The next word in the TX FIFO buffer is transferred to SPITXBUF1 serial clock cycle after completion of transmission of the previous word.</p> <p>2h (R/W) = The next word in the TX FIFO buffer is transferred to SPITXBUF 2 serial clock cycles after completion of transmission of the previous word.</p> <p>FFh (R/W) = The next word in the TX FIFO buffer is transferred to SPITXBUF 255 serial clock cycles after completion of transmission of the previous word.</p>

16.3.2.12 SPIPRI Register (offset = Fh) [reset = 0h]

SPIPRI is shown in [Figure 16-29](#) and described in [Table 16-20](#).

SPI Priority Control Register

Figure 16-29. SPIPRI Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	PRIORITY	SOFT	FREE	RESERVED	STEINV	TRIWIRE	
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 16-20. SPIPRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6	PRIORITY	R/W	0h	Interrupt Priority Select
5	SOFT	R/W	0h	<p>Emulation Soft Run</p> <p>This bit only has an effect when the FREE bit is 0.</p> <p>0h (R/W) = Transmission stops after midway in the bit stream while TSUSPEND is asserted. Once TSUSPEND is deasserted without a system reset, the remainder of the bits pending in the DATBUF are shifted. Example: If SPIDAT has shifted 3 out of 8 bits, the communication freezes right there. However, if TSUSPEND is later deasserted without resetting the SPI, SPI starts transmitting from where it had stopped (fourth bit in this case) and will transmit 8 bits from that point. The SCI module operates differently.</p> <p>1h (R/W) = If the emulation suspend occurs before the start of a transmission, (that is, before the first SPICLK pulse) then the transmission will not occur. If the emulation suspend occurs after the start of a transmission, then the data will be shifted out to completion. When the start of transmission occurs is dependent on the baud rate used.</p> <p>Standard SPI mode: Stop after transmitting the words in the shift register and buffer. That is, after TXBUF and SPIDAT are empty.</p> <p>In FIFO mode: Stop after transmitting the words in the shift register and buffer. That is, after TX FIFO and SPIDAT are empty.</p>
4	FREE	R/W	0h	<p>Emulation Free Run</p> <p>0h (R/W) = Emulation mode is selected by the SOFT bit</p> <p>1h (R/W) = Free run, continue SPI operation regardless of suspend or when the suspend occurred.</p>
3-2	RESERVED	R	0h	Reserved
1	STEINV	R/W	0h	<p>SPISTEn Inversion Bit</p> <p>On devices with 2 SPI modules, inverting the SPISTE signal on one of the modules allows the device to receive left and right- channel digital audio data.</p> <p>0h (R/W) = SPISTEn is active low (normal)</p> <p>1h (R/W) = SPISTE is active high (inverted)</p>
0	TRIWIRE	R/W	0h	<p>SPI 3-wire Mode Enable</p> <p>0h (R/W) = Normal 4-wire SPI mode.</p> <p>1h (R/W) = 3-wire SPI mode enabled. The unused pin becomes a GPIO pin. In master mode, the SPISIMO pin becomes the SPIMOMI (master receive and transmit) pin and SPISOMI is free for non-SPI use. In slave mode, the SIISOMI pin becomes the SPISO (slave receive and transmit) pin and SPISIMO is free for non-SPI use.</p>

Serial Communications Interface (SCI)

This chapter describes the features and operation of the serial communication interface (SCI) module. SCI is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter each have a 16 -level deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication.

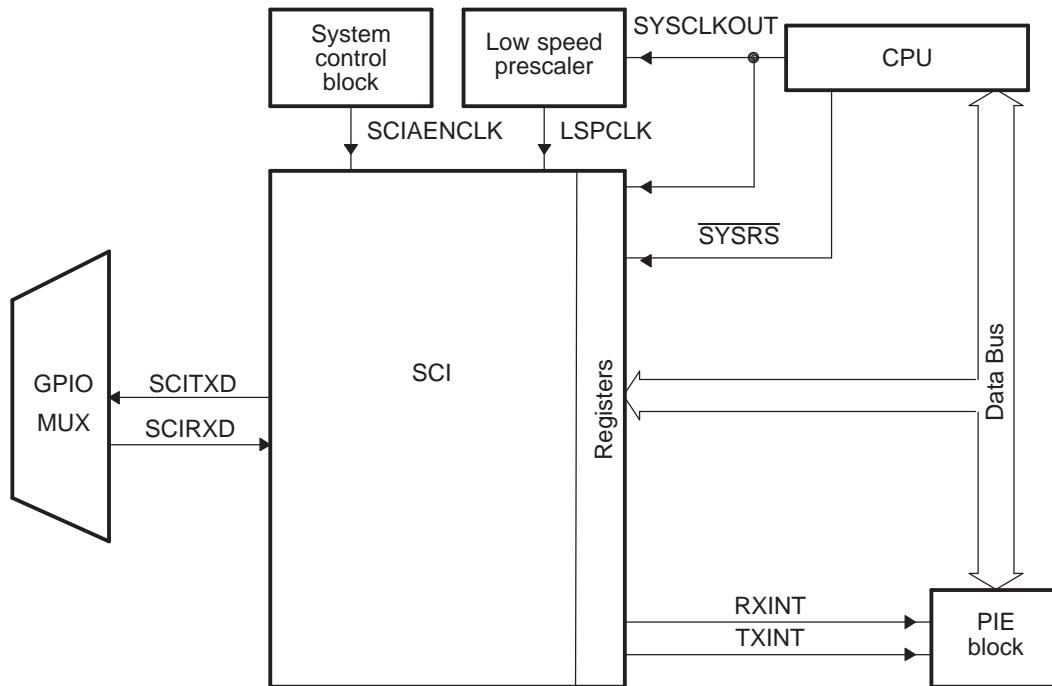
To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

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17.1 Enhanced SCI Module Overview

The SCI interfaces are shown in [Figure 17-1](#).

Figure 17-1. SCI CPU Interface



Features of the SCI module include:

- Two external pins:
 - SCITXD: SCI transmit-output pin
 - SCIRXD: SCI receive-input pin
 Both pins can be used as GPIO if not used for SCI.
- Baud rate programmable to 64K different rates
- Data-word format
 - One start bit
 - Data-word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt- driven or polled algorithms with status flags.
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format
- 13 SCI module control registers located in the control register frame beginning at address 7050h

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto-baud-detect hardware logic
 - 16 4-level transmit/receive FIFO

Figure 17-2 shows the SCI module block diagram. The SCI port operation is configured and controlled by the registers listed in [Table 17-1](#) and [Table 17-2](#).

Figure 17-2. Serial Communications Interface (SCI) Module Block Diagram

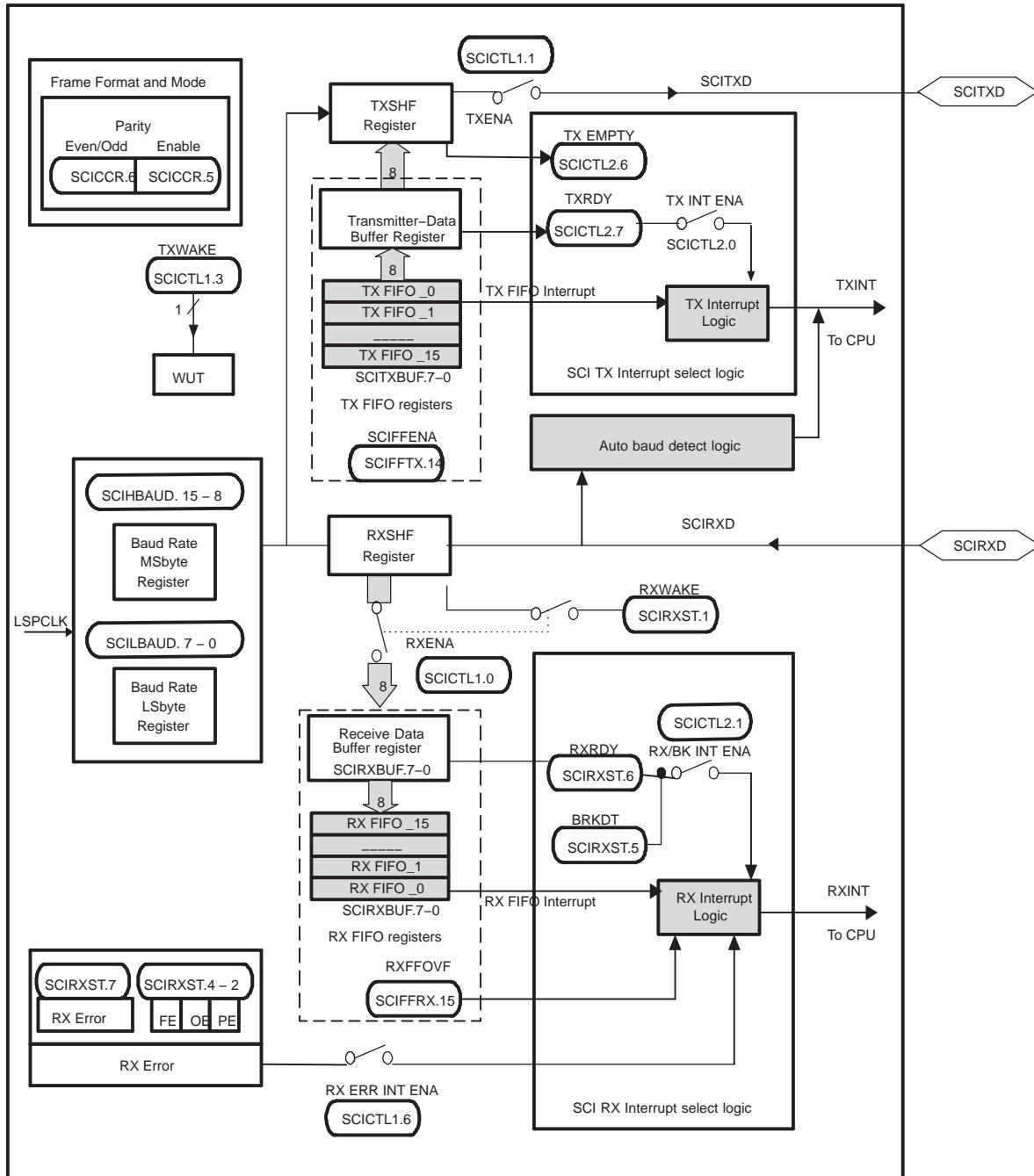


Table 17-1. SCI-A Registers

Name	Address Range	Size (x16)	Description
SCICCR	0x0000-7050	1	SCI-A Communications Control Register
SCICTL1	0x0000-7051	1	SCI-A Control Register 1
SCIHBAUD	0x0000-7052	1	SCI-A Baud Register, High Bits
SCILBAUD	0x0000-7053	1	SCI-A Baud Register, Low Bits
SCICTL2	0x0000-7054	1	SCI-A Control Register 2
SCIRXST	0x0000-7055	1	SCI-A Receive Status Register
SCIRXEMU	0x0000-7056	1	SCI-A Receive Emulation Data Buffer Register
SCIRXBUF	0x0000-7057	1	SCI-A Receive Data Buffer Register
SCITXBUF	0x0000-7059	1	SCI-A Transmit Data Buffer Register
SCIFFTX	0x0000-705A	1	SCI-A FIFO Transmit Register
SCIFFRX	0x0000-705B	1	SCI-A FIFO Receive Register
SCIFFCT	0x0000-705C	1	SCI-A FIFO Control Register
SCIPRI	0x0000-705F	1	SCI-A Priority Control Register

Table 17-2. SCI-B Registers

Name	Address Range	Size (x16)	Description ⁽¹⁾ ⁽²⁾
SCICCR	0x0000-7750	1	SCI-B Communications Control Register
SCICTL1	0x0000-7751	1	SCI-B Control Register 1
SCIHBAUD	0x0000-7752	1	SCI-B Baud Register, High Bits
SCILBAUD	0x0000-7753	1	SCI-B Baud Register, Low Bits
SCICTL2	0x0000-7754	1	SCI-B Control Register 2
SCIRXST	0x0000-7755	1	SCI-B Receive Status Register
SCIRXEMU	0x0000-7756	1	SCI-B Receive Emulation Data Buffer Register
SCIRXBUF	0x0000-7757	1	SCI-B Receive Data Buffer Register
SCITXBUF	0x0000-7759	1	SCI-B Transmit Data Buffer Register
SCIFFTX	0x0000-775A	1	SCI-B FIFO Transmit Register
SCIFFRX	0x0000-775B	1	SCI-B FIFO Receive Register
SCIFFCT	0x0000-775C	1	SCI-B FIFO Control Register
SCIPRI	0x0000-775F	1	SCI-B Priority Control Register

⁽¹⁾ The registers are mapped to peripheral frame 2. This frame allows only 16-bit accesses. Using 32-bit accesses will produce undefined results.

⁽²⁾ SCIB is an optional peripheral. In some devices this may not be present. See the device-specific data sheet for peripheral availability.

17.1.1 Architecture

The major elements used in full-duplex operation are shown in [Figure 17-2](#) and include:

- A transmitter (TX) and its major registers (upper half of [Figure 17-2](#))
 - SCITXBUF — transmitter data buffer register. Contains data (loaded by the CPU) to be transmitted
 - TXSHF register — transmitter shift register. Accepts data from register SCITXBUF and shifts data onto the SCITXD pin, one bit at a time
- A receiver (RX) and its major registers (lower half of [Figure 17-2](#))
 - RXSHF register — receiver shift register. Shifts data in from SCIRXD pin, one bit at a time
 - SCIRXBUF — receiver data buffer register. Contains data to be read by the CPU. Data from a remote processor is loaded into register RXSHF and then into registers SCIRXBUF and SCIRXEMU
- A programmable baud generator
- Data-memory-mapped control and status registers

The SCI receiver and transmitter can operate either independently or simultaneously.

17.1.1.1 SCI Module Signal Summary

Table 17-3. SCI Module Signal Summary

Signal Name	Description
External signals	
SCIRXD	SCI Asynchronous Serial Port receive data
SCITXD	SCI Asynchronous Serial Port transmit data
Control	
Baud clock	LSPCLK Prescaled clock
Interrupt signals	
TXINT	Transmit interrupt
RXINT	Receive Interrupt

17.1.1.2 Multiprocessor and Asynchronous Communication Modes

The SCI has two multiprocessor protocols, the idle-line multiprocessor mode (see [Section 17.1.1.5](#)) and the address-bit multiprocessor mode (see [Section 17.1.1.6](#)). These protocols allow efficient data transfer between multiple processors.

The SCI offers the universal asynchronous receiver/transmitter (UART) communications mode for interfacing with many popular peripherals. The asynchronous mode (see [Section 17.1.1.7](#)) requires two lines to interface with many standard devices such as terminals and printers that use RS-232-C formats. Data transmission characteristics include:

- One start bit
- One to eight data bits
- An even/odd parity bit or no parity bit
- One or two stop bits

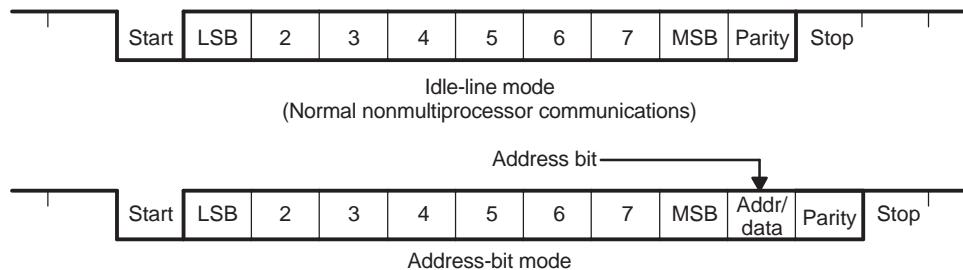
17.1.1.3 SCI Programmable Data Format

SCI data, both receive and transmit, is in NRZ (non-return-to-zero) format. The NRZ data format, shown in [Figure 17-3](#), consists of:

- One start bit
- One to eight data bits
- An even/odd parity bit (optional)
- One or two stop bits
- An extra bit to distinguish addresses from data (address-bit mode only)

The basic unit of data is called a character and is one to eight bits in length. Each character of data is formatted with a start bit, one or two stop bits, and optional parity and address bits. A character of data with its formatting information is called a frame and is shown in [Figure 17-3](#).

Figure 17-3. Typical SCI Data Frame Formats



To program the data format, use the SCICCR register. The bits used to program the data format are shown in [Table 17-4](#).

Table 17-4. Programming the Data Format Using SCICCR

Bit(s)	Bit Name	Designation	Functions
2-0	SCI CHAR2-0	SCICCR.2:0	Select the character (data) length (one to eight bits).
5	PARITY	SCICCR.5	Enables the parity function if set to 1, or disables the parity function if cleared to 0.
	ENABLE		
6	EVEN/ODD	SCICCR.6	If parity is enabled, selects odd parity if cleared to 0 or even parity if set to 1.
	PARITY		
7	STOP BITS	SCICCR.7	Determines the number of stop bits transmitted—one stop bit if cleared to 0 or two stop bits if set to 1.

17.1.1.4 SCI Multiprocessor Communication

The multiprocessor communication format allows one processor to efficiently send blocks of data to other processors on the same serial link. On one serial line, there should be only one transfer at a time. In other words, there can be only one talker on a serial line at a time.

Address Byte

The first byte of a block of information that the talker sends contains an address byte that is read by all listeners. Only listeners with the correct address can be interrupted by the data bytes that follow the address byte. The listeners with an incorrect address remain uninterrupted until the next address byte.

Sleep Bit

All processors on the serial link set the SCI SLEEP bit (bit 2 of SCICL1) to 1 so that they are interrupted only when the address byte is detected. When a processor reads a block address that corresponds to the CPU device address as set by your application software, your program must clear the SLEEP bit to enable the SCI to generate an interrupt on receipt of each data byte.

Although the receiver still operates when the SLEEP bit is 1, it does not set RXRDY, RXINT, or any of the receiver error status bits to 1 unless the address byte is detected and the address bit in the received frame is a 1 (applicable to address-bit mode). The SCI does not alter the SLEEP bit; your software must alter the SLEEP bit.

17.1.1.4.1 Recognizing the Address Byte

A processor recognizes an address byte differently, depending on the multiprocessor mode used. For example:

- The idle-line mode ([Section 17.1.1.5](#)) leaves a quiet space before the address byte. This mode does not have an extra address/data bit and is more efficient than the address-bit mode for handling blocks that contain more than ten bytes of data. The idle-line mode should be used for typical non-multiprocessor SCI communication.
- The address-bit mode ([Section 17.1.1.6](#)) adds an extra bit (that is, an address bit) into every byte to distinguish addresses from data. This mode is more efficient in handling many small blocks of data because, unlike the idle mode, it does not have to wait between blocks of data. However, at a high transmit speed, the program is not fast enough to avoid a 10-bit idle in the transmission stream.

17.1.1.4.2 Controlling the SCI TX and RX Features

The multiprocessor mode is software selectable via the ADDR/IDLE MODE bit (SCICCR, bit 3). Both modes use the TXWAKE flag bit (SCICL1, bit 3), RXWAKE flag bit (SCIRXST, bit 1), and the SLEEP flag bit (SCICL1, bit 2) to control the SCI transmitter and receiver features of these modes.

17.1.1.4.3 Receipt Sequence

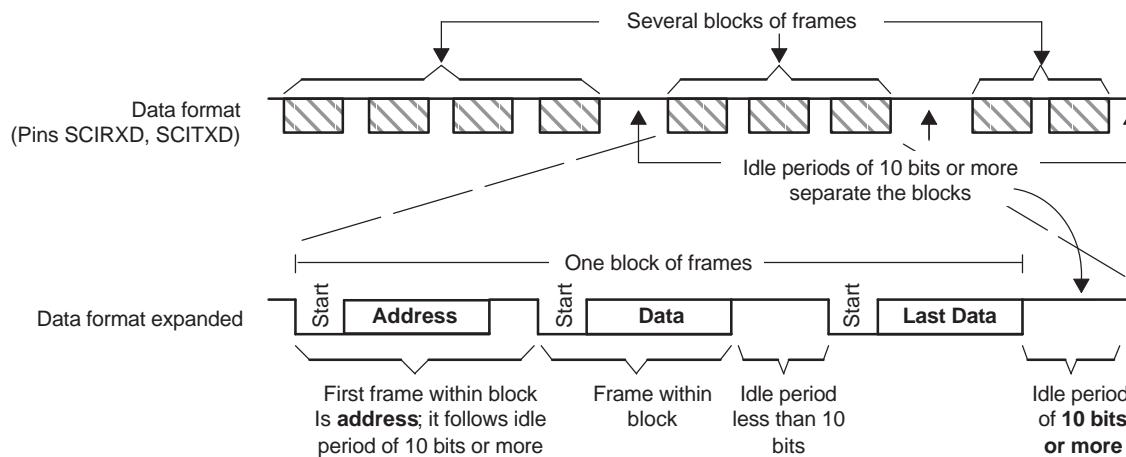
In both multiprocessor modes, the receive sequence is:

1. At the receipt of an address block, the SCI port wakes up and requests an interrupt (bit number 1 RX/BK INT ENA-of SCICL2 must be enabled to request an interrupt). It reads the first frame of the block, which contains the destination address.
2. A software routine is entered through the interrupt and checks the incoming address. This address byte is checked against its device address byte stored in memory.
3. If the check shows that the block is addressed to the device CPU, the CPU clears the SLEEP bit and reads the rest of the block; if not, the software routine exits with the SLEEP bit still set and does not receive interrupts until the next block start.

17.1.1.5 Idle-Line Multiprocessor Mode

In the idle-line multiprocessor protocol (ADDR/IDLE MODE bit=0), blocks are separated by having a longer idle time between the blocks than between frames in the blocks. An idle time of ten or more high-level bits after a frame indicates the start of a new block. The time of a single bit is calculated directly from the baud value (bits per second). The idle-line multiprocessor communication format is shown in Figure 17-4 (ADDR/IDLE MODE bit is bit 3 of SCICCR).

Figure 17-4. Idle-Line Multiprocessor Communication Format



17.1.1.5.1 Idle-Line Mode Steps

The steps followed by the idle-line mode:

- Step 1. SCI wakes up after receipt of the block-start signal.
- Step 2. The processor recognizes the next SCI interrupt.
- Step 3. The interrupt service routine compares the received address (sent by a remote transmitter) to its own.
- Step 4. If the CPU is being addressed, the service routine clears the SLEEP bit and receives the rest of the data block.
- Step 5. If the CPU is not being addressed, the SLEEP bit remains set. This lets the CPU continue to execute its main program without being interrupted by the SCI port until the next detection of a block start.

17.1.1.5.2 Block Start Signal

There are two ways to send a block-start signal:

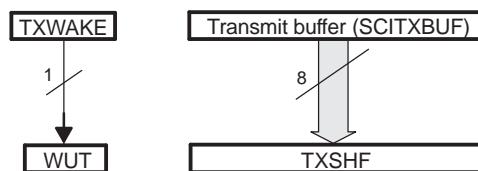
1. **Method 1:** Deliberately leave an idle time of ten bits or more by delaying the time between the transmission of the last frame of data in the previous block and the transmission of the address frame of the new block.

- 2. Method 2:** The SCI port first sets the TXWAKE bit (SCICTL1, bit 3) to 1 before writing to the SCITXBUF register. This sends an idle time of exactly 11 bits. In this method, the serial communications line is not idle any longer than necessary. (A don't care byte has to be written to SCITXBUF after setting TXWAKE, and before sending the address, so as to transmit the idle time.)

17.1.1.5.3 Wake-UP Temporary (WUT) Flag

Associated with the TXWAKE bit is the wake-up temporary (WUT) flag. WUT is an internal flag, double-buffered with TXWAKE. When TXSHF is loaded from SCITXBUF, WUT is loaded from TXWAKE, and the TXWAKE bit is cleared to 0. This arrangement is shown in [Figure 17-5](#).

Figure 17-5. Double-Buffered WUT and TXSHF



A WUT = wake-up temporary

Sending a Block Start Signal

To send out a block-start signal of exactly one frame time during a sequence of block transmissions:

1. Write a 1 to the TXWAKE bit.
2. Write a data word (content not important: a don't care) to the SCITXBUF register (transmit data buffer) to send a block-start signal. (The first data word written is suppressed while the block-start signal is sent out and ignored after that.) When the TXSHF (transmit shift register) is free again, SCITXBUF contents are shifted to TXSHF, the TXWAKE value is shifted to WUT, and then TXWAKE is cleared. Because TXWAKE was set to a 1, the start, data, and parity bits are replaced by an idle period of 11 bits transmitted following the last stop bit of the previous frame.
3. **Write a new address value to SCITXBUF**

A don't-care data word must first be written to register SCITXBUF so that the TXWAKE bit value can be shifted to WUT. After the don't-care data word is shifted to the TXSHF register, the SCITXBUF (and TXWAKE if necessary) can be written to again because TXSHF and WUT are both double-buffered.

17.1.1.5.4 Receiver Operation

The receiver operates regardless of the SLEEP bit. However, the receiver neither sets RXRDY nor the error status bits, nor does it request a receive interrupt until an address frame is detected.

17.1.1.6 Address-Bit Multiprocessor Mode

In the address-bit protocol (ADDR/IDLE MODE bit=1), frames have an extra bit called an address bit that immediately follows the last data bit. The address bit is set to 1 in the first frame of the block and to 0 in all other frames. The idle period timing is irrelevant (see [Figure 17-6](#)).

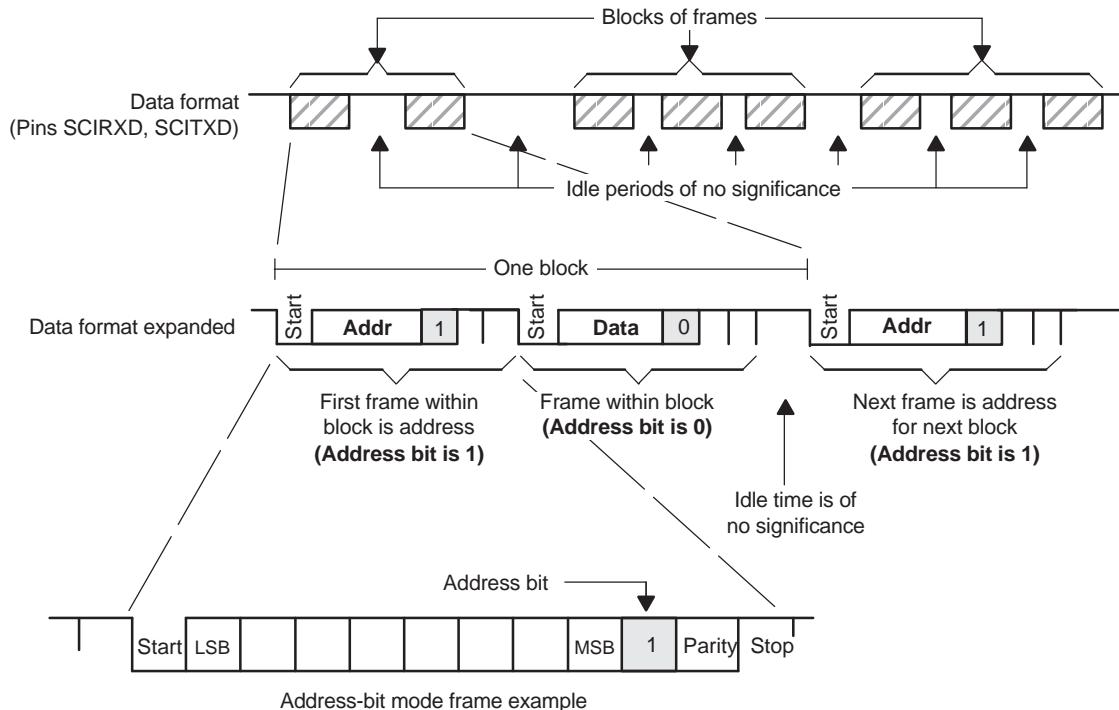
17.1.1.6.1 Sending an Address

The TXWAKE bit value is placed in the address bit. During transmission, when the SCITXBUF register and TXWAKE are loaded into the TXSHF register and WUT respectively, TXWAKE is reset to 0 and WUT becomes the value of the address bit of the current frame. Thus, to send an address:

1. Set the TXWAKE bit to 1 and write the appropriate address value to the SCITXBUF register. When this address value is transferred to the TXSHF register and shifted out, its address bit is sent as a 1. This flags the other processors on the serial link to read the address.
2. Write to SCITXBUF and TXWAKE after TXSHF and WUT are loaded. (Can be written to immediately since both TXSHF and WUT are both double-buffered.)
3. Leave the TXWAKE bit set to 0 to transmit non-address frames in the block.

NOTE: As a general rule, the address-bit format is typically used for data frames of 11 bytes or less. This format adds one bit value (1 for an address frame, 0 for a data frame) to all data bytes transmitted. The idle-line format is typically used for data frames of 12 bytes or more.

Figure 17-6. Address-Bit Multiprocessor Communication Format



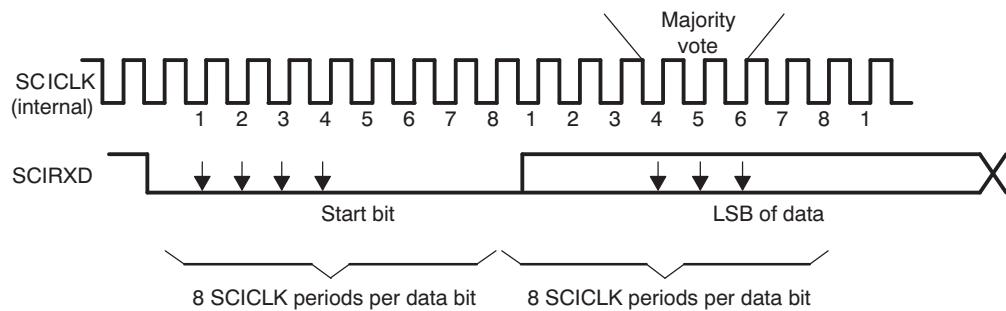
17.1.1.7 SCI Communication Format

The SCI asynchronous communication format uses either single line (one way) or two line (two way) communications. In this mode, the frame consists of a start bit, one to eight data bits, an optional even/odd parity bit, and one or two stop bits (shown in [Figure 17-7](#)). There are eight SCICLK periods per data bit.

The receiver begins operation on receipt of a valid start bit. A valid start bit is identified by four consecutive internal SCICLK periods of zero bits as shown in [Figure 17-7](#). If any bit is not zero, then the processor starts over and begins looking for another start bit.

For the bits following the start bit, the processor determines the bit value by making three samples in the middle of the bits. These samples occur on the fourth, fifth, and sixth SCICLK periods, and bit-value determination is on a majority (two out of three) basis. [Figure 17-7](#) illustrates the asynchronous communication format for this with a start bit showing where a majority vote is taken.

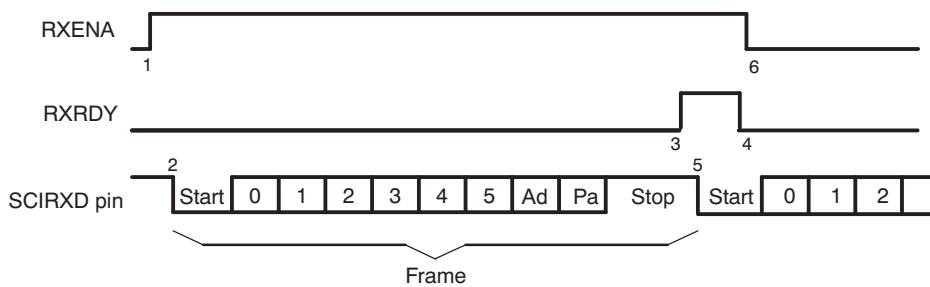
Since the receiver synchronizes itself to frames, the external transmitting and receiving devices do not have to use a synchronized serial clock. The clock can be generated locally.

Figure 17-7. SCI Asynchronous Communications Format

17.1.1.7.1 Receiver Signals in Communication Modes

Figure 17-8 illustrates an example of receiver signal timing that assumes the following conditions:

- Address-bit wake-up mode (address bit does not appear in idle-line mode)
- Six bits per character

Figure 17-8. SCI RX Signals in Communication Modes

- (1) Data arrives on the SCIRXD pin, start bit detected.
- (2) Bit RXENA is brought low to disable the receiver. Data continues to be assembled in RXSHF but is not transferred to the receiver buffer register.

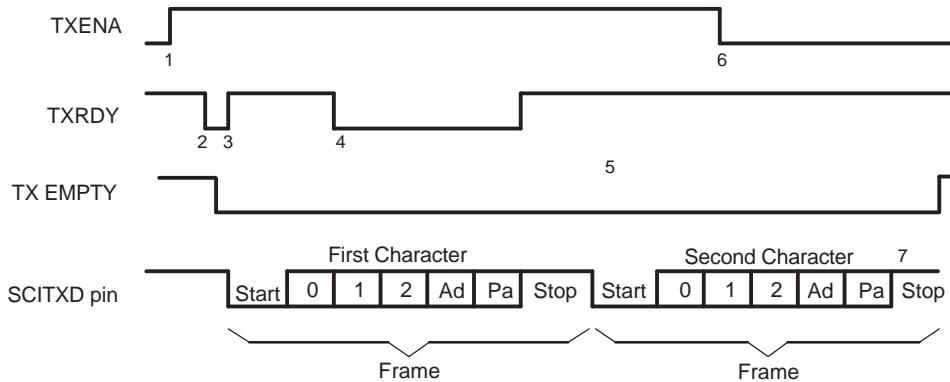
Notes:

1. Flag bit RXENA (SCICTL1, bit 0) goes high to enable the receiver.
2. Data arrives on the SCIRXD pin, start bit detected.
3. Data is shifted from RXSHF to the receiver buffer register (SCIRXBUF); an interrupt is requested. Flag bit RXRDY (SCIRXST, bit 6) goes high to signal that a new character has been received.
4. The program reads SCIRXBUF; flag RXRDY is automatically cleared.
5. The next byte of data arrives on the SCIRXD pin; the start bit is detected, then cleared.
6. Bit RXENA is brought low to disable the receiver. Data continues to be assembled in RXSHF but is not transferred to the receiver buffer register.

17.1.1.7.2 Transmitter Signals in Communication Modes

Figure 17-9 illustrates an example of transmitter signal timing that assumes the following conditions:

- Address-bit wake-up mode (address bit does not appear in idle-line mode)
- Three bits per character

Figure 17-9. SCI TX Signals in Communications Mode**Notes:**

1. Bit TXENA (SCICTL1, bit 1) goes high, enabling the transmitter to send data.
2. SCITXBUF is written to; thus, (1) the transmitter is no longer empty, and (2) TXRDY goes low.
3. The SCI transfers data to the shift register (TXSHF). The transmitter is ready for a second character (TXRDY goes high), and it requests an interrupt (to enable an interrupt, bit TX INT ENA — SCICTL2, bit 0 — must be set).
4. The program writes a second character to SCITXBUF after TXRDY goes high (item 3). (TXRDY goes low again after the second character is written to SCITXBUF.)
5. Transmission of the first character is complete. Transfer of the second character to shift register TXSHF begins.
6. Bit TXENA goes low to disable the transmitter; the SCI finishes transmitting the current character.
7. Transmission of the second character is complete; transmitter is empty and ready for new character.

17.1.1.8 SCI Port Interrupts

The SCI receiver and transmitter can be interrupt controlled. The SCICTL2 register has one flag bit (TXRDY) that indicates active interrupt conditions, and the SCIRXST register has two interrupt flag bits (RXRDY and BRKDT), plus the RX ERROR interrupt flag which is a logical OR of the FE, OE, BRKDT, and PE conditions. The transmitter and receiver have separate interrupt-enable bits. When not enabled, the interrupts are not asserted; however, the condition flags remain active, reflecting transmission and receipt status.

The SCI has independent peripheral interrupt vectors for the receiver and transmitter. Peripheral interrupt requests can be either high priority or low priority. This is indicated by the priority bits which are output from the peripheral to the PIE controller. When both RX and TX interrupt requests are made at the same priority level, the receiver always has higher priority than the transmitter, reducing the possibility of receiver overrun.

The operation of peripheral interrupts is described in the peripheral interrupt expansion controller section of the *External Peripheral Interface (ePIE)* chapter.

- If the RX/BK INT ENA bit (SCICTL2, bit 1) is set, the receiver peripheral interrupt request is asserted when one of the following events occurs:
 - The SCI receives a complete frame and transfers the data in the RXSHF register to the SCIRXBUF register. This action sets the RXRDY flag (SCIRXST, bit 6) and initiates an interrupt.
 - A break detect condition occurs (the SCIRXD is low for ten bit periods following a missing stop bit). This action sets the BRKDT flag bit (SCIRXST, bit 5) and initiates an interrupt.
- If the TX INT ENA bit (SCICTL2.0) is set, the transmitter peripheral interrupt request is asserted whenever the data in the SCITXBUF register is transferred to the TXSHF register, indicating that the CPU can write to SCITXBUF; this action sets the TXRDY flag bit (SCICTL2, bit 7) and initiates an interrupt.

NOTE: Interrupt generation due to the RXRDY and BRKDT bits is controlled by the RX/BK INT ENA bit (SCICTL2, bit 1). Interrupt generation due to the RX ERROR bit is controlled by the RX ERR INT ENA bit (SCICTL1, bit 6).

17.1.1.9 SCI Baud Rate Calculations

The internally generated serial clock is determined by the low-speed peripheral clock LSPCLK) and the baud-select registers. The SCI uses the 16-bit value of the baud-select registers to select one of the 64K different serial clock rates possible for a given LSPCLK.

See the bit descriptions in the baud-select registers, for the formula to use when calculating the SCI asynchronous baud. **Table 17-5** shows the baud-select values for common SCI bit rates.

Table 17-5. Asynchronous Baud Register Values for Common SCI Bit Rates

LSPCLK Clock Frequency, 37.5 MHz			
Ideal Baud	BRR	Actual Baud	% Error
2400	1952 (7A0h)	2400	0
4800	976 (3D0h)	4798	-0.04
9600	487 (1E7h)	9606	0.06
19200	243 (F3h)	19211	0.06
38400	121 (79h)	38422	0.06

17.1.1.10 SCI Enhanced Features

The 28x SCI features autobaud detection and transmit/receive FIFO. The following section explains the FIFO operation.

17.1.1.10.1 SCI FIFO Description

The following steps explain the FIFO features and help with programming the SCI with FIFOs.

1. *Reset.* At reset the SCI powers up in standard SCI mode and the FIFO function is disabled. The FIFO registers SCIFFTX, SCIFFRX, and SCIFFCT remain inactive.
2. *Standard SCI.* The standard F24x SCI modes will work normally with TXINT/RXINT interrupts as the interrupt source for the module.
3. *FIFO enable.* FIFO mode is enabled by setting the SCIFFEN bit in the SCIFFTX register. SCIRST can reset the FIFO mode at any stage of its operation.
4. *Active registers.* All the SCI registers and SCI FIFO registers (SCIFFTX, SCIFFRX, and SCIFFCT) are active.
5. *Interrupts.* FIFO mode has two interrupts; one for transmit FIFO, TXINT and one for receive FIFO, RXINT. RXINT is the common interrupt for SCI FIFO receive, receive error, and receive FIFO overflow conditions. The TXINT of the standard SCI will be disabled and this interrupt will service as SCI transmit FIFO interrupt.
6. *Buffers.* Transmit and receive buffers are supplemented with two 16-level FIFOs. The transmit FIFO registers are 8 bits wide and receive FIFO registers are 10 bits wide. The one-word transmit buffer of the standard SCI, functions as a transition buffer between the transmit FIFO and shift register. The one word transmit buffer is loaded from transmit FIFO only after the last bit of the shift register is shifted out. With the FIFO enabled, TXSHF is directly loaded after an optional delay value (SCIFFCT), TXBUF is not used. When FIFO mode is enabled for SCI, characters written to SCITXBUF are queued in to SCI-TXFIFO and the characters received in SCI-RXFIFO can be read using SCIRXBUF.

7. *Delayed transfer.* The rate at which words in the FIFO are transferred to the transmit shift register is programmable. The SCIFFCT register bits (7–0) FFTXDLY7–FFTXDLY0 define the delay between the word transfer. The delay is defined in the number SCI baud clock cycles. The 8 bit register can define a minimum delay of 0 baud clock cycles and a maximum of 256-baud clock cycles. With zero delay, the SCI module can transmit data in continuous mode with the FIFO words shifting out back to back. With the 256 clock delay the SCI module can transmit data in a maximum delayed mode with the FIFO words shifting out with a delay of 256 baud clocks between each words. The programmable delay facilitates communication with slow SCI/UARTs with little CPU intervention.
8. *FIFO status bits.* Both the transmit and receive FIFOs have status bits TXFFST or RXFFST (bits 12–0) that define the number of words available in the FIFOs at any time. The transmit FIFO reset bit TXFIFO and receive reset bit RXFIFO reset the FIFO pointers to zero when these bits are cleared to 0. The FIFOs resumes operation from start once these bits are set to one.
9. *Programmable interrupt levels.* Both transmit and receive FIFO can generate CPU interrupts. The interrupt trigger is generated whenever the transmit FIFO status bits TXFFST (bits 12–8) match (less than or equal to) the interrupt trigger level bits TXFFIL (bits 4–0). This provides a programmable interrupt trigger for transmit and receive sections of the SCI. Default value for these trigger level bits will be 0x11111 for receive FIFO and 0x00000 for transmit FIFO, respectively.

Figure 17-10 and Table 17-6 explain the operation/configuration of SCI interrupts in nonFIFO/FFO mode.

Figure 17-10. SCI FIFO Interrupt Flags and Enable Logic

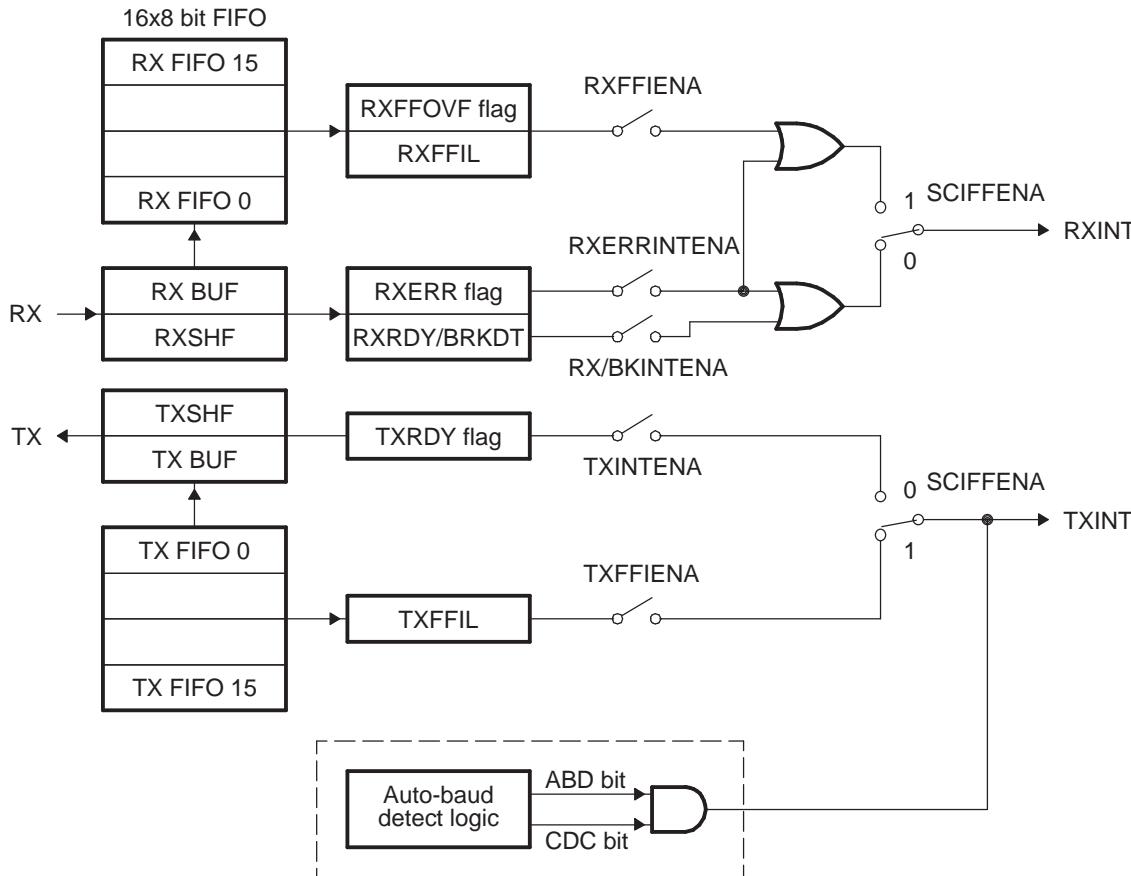


Table 17-6. SCI Interrupt Flags

FIFO Options ⁽¹⁾	SCI Interrupt Source	Interrupt Flags	Interrupt Enables	FIFO Enable SCIFFENA	Interrupt Line
SCI without FIFO	Receive error	RXERR ⁽²⁾	RXERRINTENA	0	RXINT

⁽¹⁾ FIFO mode TXSHF is directly loaded after delay value, TXBUF is not used.

⁽²⁾ RXERR can be set by BRKDT, FE, OE, PE flags. In FIFO mode, BRKDT interrupt is only through RXERR flag

Table 17-6. SCI Interrupt Flags (continued)

FIFO Options ⁽¹⁾	SCI Interrupt Source	Interrupt Flags	Interrupt Enables	FIFO Enable SCIFFENA	Interrupt Line
SCI with FIFO	Receive break	BRKDT	RX/BKINTENA	0	RXINT
	Data receive	RXRDY	RX/BKINTENA	0	RXINT
	Transmit empty	TXRDY	TXINTENA	0	TXINT
	Receive error and receive break	RXERR	RXERRINTENA	1	RXINT
	FIFO receive	RXFFIL	RXFFIENA	1	RXINT
	Transmit empty	TXFFIL	TXFFIENA	1	TXINT
	Auto-baud	ABD	Don't care	x	TXINT

17.1.1.10.2 SCI Auto-Baud

Most SCI modules do not have an auto-baud detect logic built-in hardware. These SCI modules are integrated with embedded controllers whose clock rates are dependent on PLL reset values. Often embedded controller clocks change after final design. In the enhanced feature set this module supports an autobaud-detect logic in hardware. The following section explains the enabling sequence for autobaud-detect feature.

17.1.1.10.3 Autobaud-Detect Sequence

Bits ABD and CDC in SCIFFCT control the autobaud logic. The SCIRST bit should be enabled to make autobaud logic work.

If ABD is set while CDC is 1, which indicates auto-baud alignment, SCI transmit FIFO interrupt will occur (TXINT). After the interrupt service CDC bit has to be cleared by software. If CDC remains set even after interrupt service, there should be no repeat interrupts.

1. Enable autobaud-detect mode for the SCI by setting the CDC bit (bit 13) in SCIFFCT and clearing the ABD bit (Bit 15) by writing a 1 to ABDCLR bit (bit 14).
2. Initialize the baud register to be 1 or less than a baud rate limit of 500 Kbps.
3. Allow SCI to receive either character "A" or "a" from a host at the desired baud rate. If the first character is either "A" or "a". the autobaud- detect hardware will detect the incoming baud rate and set the ABD bit.
4. The auto-detect hardware will update the baud rate register with the equivalent baud value hex. The logic will also generate an interrupt to the CPU.
5. Respond to the interrupt clear ADB bit by writing a 1 to ABD CLR (bit 14) of SCIFFCT register and disable further autobaud locking by clearing CDC bit by writing a 0.
6. Read the receive buffer for character "A" or "a" to empty the buffer and buffer status.
7. If ABD is set while CDC is 1, which indicates autobaud alignment, the SCI transmit FIFO interrupt will occur (TXINT). After the interrupt service CDC bit must be cleared by software.

NOTE: At higher baud rates, the slew rate of the incoming data bits can be affected by transceiver and connector performance. While normal serial communications may work well, this slew rate may limit reliable autobaud detection at higher baud rates (typically beyond 100k baud) and cause the auto-baudlock feature to fail.

To avoid this, the following is recommended:

- Achieve a baud-lock between the host and 28x SCI boot loader using a lower baud rate.
 - The host may then handshake with the loaded 28x application to set the SCI baud rate register to the desired higher baud rate.
-

17.2 Registers

17.2.1 SCI Base Addresses

Table 17-7. SCI Base Address Table

Device Registers	Register Name	Start Address	End Address
SciaRegs	SCI_REGS	0x0000_7200	0x0000_720F
ScibRegs	SCI_REGS	0x0000_7210	0x0000_721F
ScicRegs	SCI_REGS	0x0000_7220	0x0000_722F
ScidRegs	SCI_REGS	0x0000_7230	0x0000_723F

17.2.2 SCI_REGS Registers

Table 17-8 lists the memory-mapped registers for the SCI_REGS. All register offset addresses not listed in **Table 17-8** should be considered as reserved locations and the register contents should not be modified.

Table 17-8. SCI_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	SCICCR	Communications control register	Section 17.2.2.1	
1h	SCICTL1	Control register 1	Section 17.2.2.2	
2h	SCIHBAUD	Baud rate (high) register	Section 17.2.2.3	
3h	SCILBAUD	Baud rate (low) register	Section 17.2.2.4	
4h	SCICTL2	Control register 2	Section 17.2.2.5	
5h	SCIRXST	Receive status register	Section 17.2.2.6	
6h	SCIRXEMU	Receive emulation buffer register	Section 17.2.2.7	
7h	SCIRXBUFF	Receive data buffer	Section 17.2.2.8	
9h	SCITXBUFF	Transmit data buffer	Section 17.2.2.9	
Ah	SCIFFTX	FIFO transmit register	Section 17.2.2.10	
Bh	SCIFFRX	FIFO receive register	Section 17.2.2.11	
Ch	SCIFFCCT	FIFO control register	Section 17.2.2.12	
Fh	SCIPRI	FIFO Priority control	Section 17.2.2.13	

17.2.2.1 SCICCR Register (offset = 0h) [reset = 0h]

SCICCR is shown in [Figure 17-11](#) and described in [Table 17-9](#).

Communications control register

Figure 17-11. SCICCR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
STOPBITS	PARITY	PARITYENA	LOOPBKENA	ADDRIDLE_M ODE	SCICHAR		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-9. SCICCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	STOPBITS	R/W	0h	<p>SCI number of stop bits.</p> <p>This bit specifies the number of stop bits transmitted. The receiver checks for only one stop bit.</p> <p>0h (R/W) = One stop bit 1h (R/W) = Two stop bits</p>
6	PARITY	R/W	0h	<p>SCI parity odd/even selection.</p> <p>If the PARITY ENABLE bit (SCICCR, bit 5) is set, PARITY (bit 6) designates odd or even parity (odd or even number of bits with the value of 1 in both transmitted and received characters).</p> <p>0h (R/W) = Odd parity 1h (R/W) = Even parity</p>
5	PARITYENA	R/W	0h	<p>SCI parity enable.</p> <p>This bit enables or disables the parity function. If the SCI is in the addressbit multiprocessor mode (set using bit 3 of this register), the address bit is included in the parity calculation (if parity is enabled). For characters of less than eight bits, the remaining unused bits should be masked out of the parity calculation.</p> <p>0h (R/W) = Parity disabled no parity bit is generated during transmission or is expected during reception 1h (R/W) = Parity is enabled</p>
4	LOOPBKENA	R/W	0h	<p>Loop Back test mode enable.</p> <p>This bit enables the Loop Back test mode where the Tx pin is internally connected to the Rx pin.</p> <p>0h (R/W) = Loop Back test mode disabled 1h (R/W) = Loop Back test mode enabled</p>
3	ADDRIDLE_MODE	R/W	0h	<p>SCI multiprocessor mode control bit.</p> <p>This bit selects one of the multiprocessor protocols. Multiprocessor communication is different from the other communication modes because it uses SLEEP and TXWAKE functions (bits SCICL1, bit 2 and SCICL1, bit 3, respectively). The idle-line mode is usually used for normal communications because the address-bit mode adds an extra bit to the frame. The idle-line mode does not add this extra bit and is compatible with RS-232 type communications.</p> <p>0h (R/W) = Idle-line mode protocol selected 1h (R/W) = Address-bit mode protocol selected</p>

Table 17-9. SCICCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	SCICHAR	R/W	0h	<p>Character-length control bits 2-0.</p> <p>These bits select the SCI character length from one to eight bits. Characters of less than eight bits are right-justified in SCIRXBUF and SCIRXEMU and are padded with leading zeros in SCIRXBUF. SCITXBUF doesn't need to be padded with leading zeros.</p> <p>0h (R/W) = SCICHAR_LENGTH_1 1h (R/W) = SCICHAR_LENGTH_2 2h (R/W) = SCICHAR_LENGTH_3 3h (R/W) = SCICHAR_LENGTH_4 4h (R/W) = SCICHAR_LENGTH_5 5h (R/W) = SCICHAR_LENGTH_6 6h (R/W) = SCICHAR_LENGTH_7 7h (R/W) = SCICHAR_LENGTH_8</p>

17.2.2.2 SCICL1 Register (offset = 1h) [reset = 0h]

SCICL1 is shown in [Figure 17-12](#) and described in [Table 17-10](#).

Control register 1

Figure 17-12. SCICL1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RXERRINTEN A	SWRESET	RESERVED	TXWAKE	SLEEP	TXENA	RXENA
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-10. SCICL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6	RXERRINTENA	R/W	0h	<p>SCI receive error interrupt enable. Setting this bit enables an interrupt if the RX ERROR bit (SCIRXST, bit 7) becomes set because of errors occurring. 0h (R/W) = Receive error interrupt disabled 1h (R/W) = Receive error interrupt enabled</p>
5	SWRESET	R/W	0h	<p>SCI software reset (active low). Writing a 0 to this bit initializes the SCI state machines and operating flags (registers SCICL2 and SCIRXST) to the reset condition. The SW RESET bit does not affect any of the configuration bits. All affected logic is held in the specified reset state until a 1 is written to SW RESET (the bit values following a reset are shown beneath each register diagram in this section). Thus, after a system reset, re-enable the SCI by writing a 1 to this bit. Clear this bit after a receiver break detect (BRKDT flag, bit SCIRXST, bit 5). SW RESET affects the operating flags of the SCI, but it neither affects the configuration bits nor restores the reset values. Once SW RESET is asserted, the flags are frozen until the bit is deasserted. The affected flags are as follows: Value After SW SCI Flag Register Bit RESET 1 TXRDY SCICL2, bit 7 1 TX EMPTY SCICL2, bit 6 0 RXWAKE SCIRXST, bit 1 0 PE SCIRXST, bit 2 0 OE SCIRXST, bit 3 0 FE SCIRXST, bit 4 0 BRKDT SCIRXST, bit 5 0 RXRDY SCIRXST, bit 6 0 RX ERROR SCIRXST, bit 7 0h (R/W) = Writing a 0 to this bit initializes the SCI state machines and operating flags (registers SCICL2 and SCIRXST) to the reset condition. 1h (R/W) = After a system reset, re-enable the SCI by writing a 1 to this bit.</p>
4	RESERVED	R	0h	Reserved

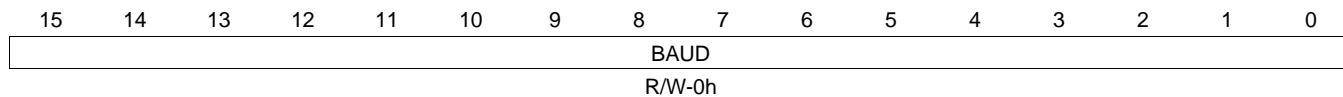
Table 17-10. SCICL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TXWAKE	R/W	0h	<p>SCI transmitter wake-up method select.</p> <p>The TXWAKE bit controls selection of the data-transmit feature, depending on which transmit mode (idle-line or address-bit) is specified at the ADDR/IDLE MODE bit (SCICCR, bit 3).</p> <p>0h (R/W) = Transmit feature is not selected. In idle-line mode: write a 1 to TXWAKE, then write data to register SCITXBUF to generate an idle period of 11 data bits. In address-bit mode: write a 1 to TXWAKE, then write data to SCITXBUF to set the address bit for that frame to 1</p> <p>1h (R/W) = Transmit feature selected is dependent on the mode, idle-line or address-bit: TXWAKE is not cleared by the SW RESET bit (SCICL1, bit 5)</p> <p>it is cleared by a system reset or the transfer of TXWAKE to the WUT flag.</p>
2	SLEEP	R/W	0h	<p>SCI sleep.</p> <p>The TXWAKE bit controls selection of the data-transmit feature, depending on which transmit mode (idle-line or address-bit) is specified at the ADDR/IDLE MODE bit (SCICCR, bit 3). In a multiprocessor configuration, this bit controls the receiver sleep function. Clearing this bit brings the SCI out of the sleep mode.</p> <p>The receiver still operates when the SLEEP bit is set however, operation does not update the receiver buffer ready bit (SCIRXST, bit 6, RXRDY) or the error status bits (SCIRXST, bit 5-2: BRKDT, FE, OE, and PE) unless the address byte is detected.</p> <p>SLEEP is not cleared when the address byte is detected.</p> <p>0h (R/W) = Sleep mode disabled</p> <p>1h (R/W) = Sleep mode enabled</p>
1	TXENA	R/W	0h	<p>SCI transmitter enable.</p> <p>Data is transmitted through the SCITXD pin only when TXENA is set. If reset, transmission is halted but only after all data previously written to SCITXBUF has been sent.</p> <p>0h (R/W) = Transmitter disabled</p> <p>1h (R/W) = Transmitter enabled</p>
0	RXENA	R/W	0h	<p>SCI receiver enable.</p> <p>Data is received on the SCIRXD pin and is sent to the receiver shift register and then the receiver buffers. This bit enables or disables the receiver (transfer to the buffers).</p> <p>Clearing RXENA stops received characters from being transferred to the two receiver buffers and also stops the generation of receiver interrupts. However, the receiver shift register can continue to assemble characters. Thus, if RXENA is set during the reception of a character, the complete character will be transferred into the receiver buffer registers, SCIRXEMU and SCIRXBUF.</p> <p>0h (R/W) = Prevent received characters from transfer into the SCIRXEMU and SCIRXBUF receiver buffers</p> <p>1h (R/W) = Send received characters to SCIRXEMU and SCIRXBUF</p>

17.2.2.3 SCIHBAUD Register (offset = 2h) [reset = 0h]

SCIHBAUD is shown in [Figure 17-13](#) and described in [Table 17-11](#).

Baud rate (high) register

Figure 17-13. SCIHBAUD Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

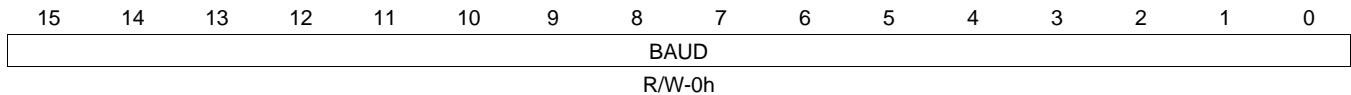
Table 17-11. SCIHBAUD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	BAUD	R/W	0h	<p>SCI 16-bit baud selection Registers SCIHBAUD (MSbyte). The internally-generated serial clock is determined by the low speed peripheral clock (LSPCLK) signal and the two baud-select registers. The SCI uses the 16-bit value of these registers to select one of 64K serial clock rates for the communication modes.</p> <p>The SCI baud rate is calculated using the following equation: $\text{SCI Asynchronous Baud} = \text{LSPCLK} / ((\text{BRR} + 1) * 8)$</p> <p>Alternatively, $\text{BRR} = \text{LSPCLK} / (\text{SCI Asynchronous Baud} * 8) - 1$ Note that the above formulas are applicable only when $0 < \text{BRR} < 65536$. If BRR = 0, then $\text{SCI Asynchronous Baud} = \text{LSPCLK} / 16$ Where: BRR = the 16-bit value (in decimal) in the baud-select registers</p>

17.2.2.4 SCILBAUD Register (offset = 3h) [reset = 0h]

SCILBAUD is shown in [Figure 17-14](#) and described in [Table 17-12](#).

Baud rate (low) register

Figure 17-14. SCILBAUD Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-12. SCILBAUD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	BAUD	R/W	0h	See SCIHB AUD Detailed Description

17.2.2.5 SCICL2 Register (offset = 4h) [reset = 0h]

SCICL2 is shown in [Figure 17-15](#) and described in [Table 17-13](#).

Control register 2

Figure 17-15. SCICL2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
TXRDY	TXEMPTY		RESERVED	R-0h		RXBKINTENA	TXINTENA
R-0h	R-0h			R-0h		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-13. SCICL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	TXRDY	R	0h	<p>Transmitter buffer register ready flag.</p> <p>When set, this bit indicates that the transmit data buffer register, SCITXBUF, is ready to receive another character. Writing data to the SCITXBUF automatically clears this bit. When set, this flag asserts a transmitter interrupt request if the interrupt-enable bit, TX INT ENA (SCICL2.0), is also set. TXRDY is set to 1 by enabling the SW RESET bit (SCICL1.5) or by a system reset.</p> <p>0h (R/W) = SCITXBUF is full</p> <p>1h (R/W) = SCITXBUF is ready to receive the next character</p>
6	TXEMPTY	R	0h	<p>Transmitter empty flag.</p> <p>This flag's value indicates the contents of the transmitter's buffer register (SCITXBUF) and shift register (TXSHF). An active SW RESET (SCICL1.5), or a system reset, sets this bit. This bit does not cause an interrupt request.</p> <p>0h (R/W) = Transmitter buffer or shift register or both are loaded with data</p> <p>1h (R/W) = Transmitter buffer and shift registers are both empty</p>
5-2	RESERVED	R	0h	Reserved
1	RXBKINTENA	R/W	0h	<p>Receiver-buffer/break interrupt enable.</p> <p>This bit controls the interrupt request caused by either the RXRDY flag or the BRKDT flag (bits SCIRXST.6 and .5) being set. However, RX/BK INT ENA does not prevent the setting of these flags.</p> <p>0h (R/W) = Disable RXRDY/BRKDT interrupt</p> <p>1h (R/W) = Enable RXRDY/BRKDT interrupt</p>
0	TXINTENA	R/W	0h	<p>SCITXBUF-register interrupt enable.</p> <p>This bit controls the interrupt request caused by setting the TXRDY flag bit (SCICL2.7). However, it does not prevent the TXRDY flag from being set (being set indicates that register SCITXBUF is ready to receive another character).</p> <p>0h (R/W) = Disable TXRDY interrupt</p> <p>1h (R/W) = Enable TXRDY interrupt</p>

17.2.2.6 SCIRXST Register (offset = 5h) [reset = 0h]

SCIRXST is shown in [Figure 17-16](#) and described in [Table 17-14](#).

Receive status register

Figure 17-16. SCIRXST Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RXERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-14. SCIRXST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	RXERROR	R	0h	<p>SCI receiver error flag. The RX ERROR flag indicates that one of the error flags in the receiver status register is set. RX ERROR is a logical OR of the break detect, framing error, overrun, and parity error enable flags (bits 5-2: BRKDT, FE, OE, and PE). A 1 on this bit will cause an interrupt if the RX ERR INT ENA bit (SCICCTL1.6) is set. This bit can be used for fast error-condition checking during the interrupt service routine. This error flag cannot be cleared directly it is cleared by an active SW RESET or by a system reset. 0h (R/W) = No error flags set 1h (R/W) = Error flag(s) set</p>
6	RXRDY	R	0h	<p>SCI receiver-ready flag. When a new character is ready to be read from the SCIRXBUT register, the receiver sets this bit, and a receiver interrupt is generated if the RX/BK INT ENA bit (SCICCTL2.1) is a 1. RXRDY is cleared by a reading of the SCIRXBUT register, by an active SW RESET, or by a system reset. 0h (R/W) = No new character in SCIRXBUT 1h (R/W) = Character ready to be read from SCIRXBUT</p>
5	BRKDT	R	0h	<p>SCI break-detect flag. The SCI sets this bit when a break condition occurs. A break condition occurs when the SCI receiver data line (SCIRXD) remains continuously low for at least ten bits, beginning after a missing first stop bit. The occurrence of a break causes a receiver interrupt to be generated if the RX/BK INT ENA bit is a 1, but it does not cause the receiver buffer to be loaded. A BRKDT interrupt can occur even if the receiver SLEEP bit is set to 1. BRKDT is cleared by an active SW RESET or by a system reset. It is not cleared by receipt of a character after the break is detected. In order to receive more characters, the SCI must be reset by toggling the SW RESET bit or by a system reset. 0h (R/W) = No break condition 1h (R/W) = Break condition occurred</p>
4	FE	R	0h	<p>SCI framing-error flag. The SCI sets this bit when an expected stop bit is not found. Only the first stop bit is checked. The missing stop bit indicates that synchronization with the start bit has been lost and that the character is incorrectly framed. The FE bit is reset by a clearing of the SW RESET bit or by a system reset. 0h (R/W) = No framing error detected 1h (R/W) = Framing error detected</p>

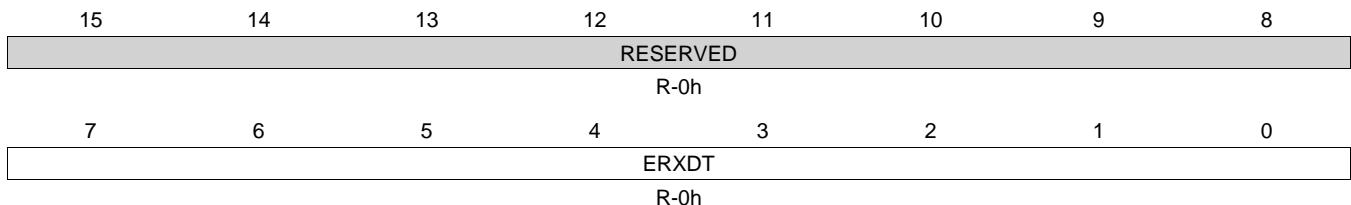
Table 17-14. SCIRXST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OE	R	0h	<p>SCI overrun-error flag. The SCI sets this bit when a character is transferred into registers SCIRXEMU and SCIRXBUF before the previous character is fully read by the CPU or DMAC. The previous character is overwritten and lost. The OE flag bit is reset by an active SW RESET or by a system reset.</p> <p>0h (R/W) = No overrun error detected 1h (R/W) = Overrun error detected</p>
2	PE	R	0h	<p>SCI parity-error flag. This flag bit is set when a character is received with a mismatch between the number of 1s and its parity bit. The address bit is included in the calculation. If parity generation and detection is not enabled, the PE flag is disabled and read as 0. The PE bit is reset by an active SW RESET or a system reset.</p> <p>0h (R/W) = No parity error or parity is disabled 1h (R/W) = Parity error is detected</p>
1	RXWAKE	R	0h	<p>Receiver wake-up-detect flag 0h (R/W) = No detection of a receiver wake-up condition 1h (R/W) = A value of 1 in this bit indicates detection of a receiver wake-up condition. In the address-bit multiprocessor mode (SCICCR.3 = 1), RXWAKE reflects the value of the address bit for the character contained in SCIRXBUF. In the idle-line multiprocessor mode, RXWAKE is set if the SCIRD data line is detected as idle. RXWAKE is a read-only flag, cleared by one of the following:</p> <ul style="list-style-type: none"> - The transfer of the first byte after the address byte to SCIRXBUF (only in non-FIFO mode) - The reading of SCIRXBUF - An active SW RESET - A system reset
0	RESERVED	R	0h	Reserved

17.2.2.7 SCIRXEMU Register (offset = 6h) [reset = 0h]

SCIRXEMU is shown in [Figure 17-17](#) and described in [Table 17-15](#).

Receive emulation buffer register

Figure 17-17. SCIRXEMU Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-15. SCIRXEMU Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	ERXDT	R	0h	Receive emulation buffer data

17.2.2.8 SCIRXBUF Register (offset = 7h) [reset = 0h]

SCIRXBUF is shown in [Figure 17-18](#) and described in [Table 17-16](#).

Recieve data buffer

Figure 17-18. SCIRXBUF Register

15	14	13	12	11	10	9	8
SCIFFFE	SCIFFPE			RESERVED			
R-0h	R-0h			R-0h			
7	6	5	4	3	2	1	0
				SAR			
				R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

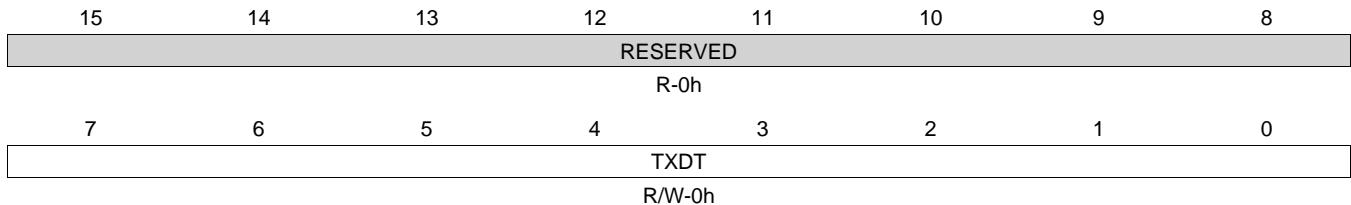
Table 17-16. SCIRXBUF Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SCIFFFE	R	0h	SCIFFFE. SCI FIFO Framing error flag bit (applicable only if the FIFO is enabled) 0h (R/W) = No parity error occurred while receiving the character, in bits 7-0. This bit is associated with the character on the top of the FIFO. 1h (R/W) = A parity error occurred while receiving the character in bits 7-0. This bit is associated with the character on the top of the FIFO.
14	SCIFFPE	R	0h	SCIFFPE. SCI FIFO parity error flag bit (applicable only if the FIFO is enabled) 0h (R/W) = No frame error occurred while receiving the character, in bits 7-0. This bit is associated with the character on the top of the FIFO. 1h (R/W) = A frame error occurred while receiving the character in bits 7-0. This bit is associated with the character on the top of the FIFO.
13-8	RESERVED	R	0h	Reserved
7-0	SAR	R	0h	Receive Character bits

17.2.2.9 SCITXBUF Register (offset = 9h) [reset = 0h]

SCITXBUF is shown in [Figure 17-19](#) and described in [Table 17-17](#).

Transmit data buffer

Figure 17-19. SCITXBUF Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-17. SCITXBUF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	TXDT	R/W	0h	Transmit data buffer

17.2.2.10 SCIFFTX Register (offset = Ah) [reset = 0h]SCIFFTX is shown in [Figure 17-20](#) and described in [Table 17-18](#).

FIFO transmit register

Figure 17-20. SCIFFTX Register

15	14	13	12	11	10	9	8
SCIRST	SCIFFENA	TXFIFOXRESET			TXFFST		
R/W-0h	R/W-0h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
TXFINT	TXFFINTCLR	TXFFIENA			TXFFIL		
R-0h	R-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-18. SCIFFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SCIRST	R/W	0h	SCI Reset
14	SCIFFENA	R/W	0h	SCI FIFO enable 0h (R/W) = SCI FIFO enhancements are disabled 1h (R/W) = SCI FIFO enhancements are enabled
13	TXFIFOXRESET	R/W	0h	Transmit FIFO reset 0h (R/W) = Reset the FIFO pointer to zero and hold in reset 1h (R/W) = Re-enable transmit FIFO operation
12-8	TXFFST	R	0h	FIFO status 0h (R/W) = Transmit FIFO is empty 1h (R/W) = Transmit FIFO has 1 words 2h (R/W) = Transmit FIFO has 2 words 3h (R/W) = Transmit FIFO has 3 words 4h (R/W) = Transmit FIFO has 4 words
7	TXFFINT	R	0h	Transmit FIFO interrupt 0h (R/W) = TX FIFO interrupt has not occurred, read-only bit 1h (R/W) = TX FIFO interrupt has occurred, read-only bit
6	TXFFINTCLR	R	0h	Transmit FIFO clear 0h (R/W) = Write 0 has no effect on TXFINT flag bit, Bit reads back a zero 1h (R/W) = Write 1 to clear TXFINT flag in bit 7
5	TXFFIENA	R/W	0h	Transmit FIFO interrupt enable 0h (R/W) = TX FIFO interrupt based on TXFFIVL match (less than or equal to) is disabled 1h (R/W) = TX FIFO interrupt based on TXFFIVL match (less than or equal to) is enabled.
4-0	TXFFIL	R/W	0h	TXFFIL4-0 Transmit FIFO interrupt level bits. Transmit FIFO will generate interrupt when the FIFO status bits (TXFFST4-0) and FIFO level bits (TXFFIL4-0) match (less than or equal to). Because the SCI has a 4-level transmit FIFO, these bits cannot be configured for an interrupt of more than 4 FIFO levels. Default value should be 0x00000.

17.2.2.11 SCIFFRX Register (offset = Bh) [reset = 0h]

SCIFFRX is shown in [Figure 17-21](#) and described in [Table 17-19](#).

FIFO receive register

Figure 17-21. SCIFFRX Register

15	14	13	12	11	10	9	8
RXFFOVF	RXFFOVRCLR	RXFIFORESET			RXFFST		
R/W-0h	R/W-0h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RXFFINT	RXFFINTCLR	RXFFIENA			RXFFIL		
R-0h	W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-19. SCIFFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RXFFOVF	R/W	0h	Receive FIFO overflow. This will function as flag, but cannot generate interrupt by itself. This condition will occur while receive interrupt is active. Receive interrupts should service this flag condition. 0h (R/W) = Receive FIFO has not overflowed, read-only bit 1h (R/W) = Receive FIFO has overflowed, read-only bit. More than 16 words have been received in to the FIFO, and the first received word is lost
14	RXFFOVRCLR	R/W	0h	RXFFOVF clear 0h (R/W) = Write 0 has no effect on RXFFOVF flag bit, Bit reads back a zero 1h (R/W) = Write 1 to clear RXFFOVF flag in bit 15
13	RXFIFORESET	R/W	0h	Receive FIFO reset 0h (R/W) = Write 0 to reset the FIFO pointer to zero, and hold in reset. 1h (R/W) = Re-enable receive FIFO operation
12-8	RXFFST	R	0h	FIFO status 0h (R/W) = Receive FIFO is empty 1h (R/W) = Receive FIFO has 1 words 2h (R/W) = Receive FIFO has 2 words 3h (R/W) = Receive FIFO has 3 words 4h (R/W) = Receive FIFO has 4 words
7	RXFFINT	R	0h	Receive FIFO interrupt 0h (R/W) = RXFIFO interrupt has not occurred, read-only bit 1h (R/W) = RXFIFO interrupt has occurred, read-only bit
6	RXFFINTCLR	W	0h	Receive FIFO interrupt clear 0h (R/W) = Write 0 has no effect on RXFFINT flag bit. Bit reads back a zero. 1h (R/W) = Write 1 to clear RXFFINT flag in bit 7
5	RXFFIENA	R/W	0h	Receive FIFO interrupt enable 0h (R/W) = RX FIFO interrupt based on RXFFIVL match (less than or equal to) will be disabled 1h (R/W) = RX FIFO interrupt based on RXFFIVL match (less than or equal to) will be enabled

Table 17-19. SCIFFRX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	RXFFIL	R/W	0h	<p>Receive FIFO interrupt level bits</p> <p>11111 - Receive FIFO generates interrupt when the FIFO status bits (RXFFST4-0) and FIFO level bits (RXFFIL4-0) match (i.e., are greater than or equal to). Default value of these bits after reset - 11111. This will avoid frequent interrupts, after reset, as the receive FIFO will be empty most of the time. Because the SCI has a 4-level receive FIFO, these bits cannot be configured for an interrupt of more than 4 FIFO levels.</p>

17.2.2.12 SCIFFCT Register (offset = Ch) [reset = 0h]

SCIFFCT is shown in [Figure 17-22](#) and described in [Table 17-20](#).

FIFO control register

Figure 17-22. SCIFFCT Register

15	14	13	12	11	10	9	8
ABD	ABDCLR	CDC			RESERVED		
R-0h	W-0h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
			FFTXDLY				
				R/W-0h			

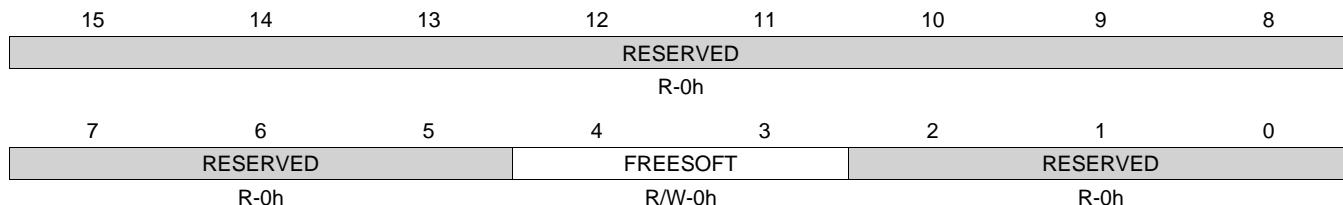
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-20. SCIFFCT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ABD	R	0h	Auto-baud detect (ABD) bit 0h (R/W) = Auto-baud detection is not complete. "A", "a" character has not been received successfully. 1h (R/W) = Auto-baud hardware has detected "A" or "a" character on the SCI receive register. Auto-detect is complete.
14	ABDCLR	W	0h	ABD-clear bit 0h (R/W) = Write 0 has no effect on ABD flag bit. Bit reads back a zero. 1h (R/W) = Write 1 to clear ABD flag in bit 15.
13	CDC	R/W	0h	CDC calibrate A-detect bit 0h (R/W) = Disables auto-baud alignment 1h (R/W) = Enables auto-baud alignment
12-8	RESERVED	R	0h	Reserved
7-0	FFTXDLY	R/W	0h	FIFO transfer delay. These bits define the delay between every transfer from FIFO transmit buffer to transmit shift register. The delay is defined in the number of SCI serial baud clock cycles. The 8 bit register could define a minimum delay of 0 baud clock cycles and a maximum of 256 baud clock cycles In FIFO mode, the buffer (TXBUF) between the shift register and the FIFO should be filled only after the shift register has completed shifting of the last bit. This is required to pass on the delay between transfers to the data stream. In FIFO mode, TXBUF should not be treated as one additional level of buffer. The delayed transmit feature will help to create an auto-flow scheme without RTS/CTS controls as in standard UARTS. When SCI is configured for one stop-bit, delay introduced by FFTXDLY between one frame and the next frame is equal to number of baud clock cycles that FFTXDLY is set to. When SCI is configured for two stop-bits, delay introduced by FFTXDLY between one frame and the next frame is equal to number of baud clock cycles that FFTXDLY is set to minus 1.

17.2.2.13 SCIPRI Register (offset = Fh) [reset = 0h]SCIPRI is shown in [Figure 17-23](#) and described in [Table 17-21](#).

FIFO Priority control

Figure 17-23. SCIPRI Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 17-21. SCIPRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-5	RESERVED	R	0h	Reserved
4-3	FREESOFT	R/W	0h	These bits determine what occurs when an emulation suspend event occurs (for example, when the debugger hits a breakpoint). The peripheral can continue whatever it is doing (free-run mode), or if in stop mode, it can either stop immediately or stop when the current operation (the current receive/transmit sequence) is complete. 0h (R/W) = Immediate stop on suspend 1h (R/W) = Complete current receive/transmit sequence before stopping 2h (R/W) = Free run 3h (R/W) = Free run
2-0	RESERVED	R	0h	Reserved

Inter-Integrated Circuit Module (I2C)

This chapter describes the features and operation of the inter-integrated circuit (I2C) module. The I2C module provides an interface between one of these devices and devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit/receive 1 to 8-bit data to/from the device through the I2C module. This guide assumes the reader is familiar with the I2C-bus specification.

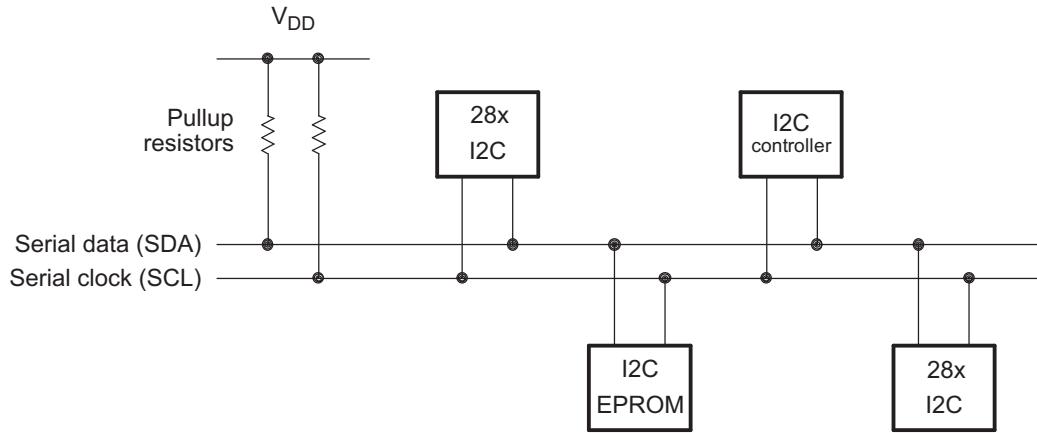
NOTE: A unit of data transmitted or received by the I2C module can have fewer than 8 bits; however, for convenience, a unit of data is called a data byte throughout this document. The number of bits in a data byte is selectable via the BC bits of the mode register, I2CMDR.

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18.1 Introduction to the I2C Module

The I2C module supports any slave or master I2C-compatible device. [Figure 18-1](#) shows an example of multiple I2C modules connected for a two-way transfer from one device to other devices.

Figure 18-1. Multiple I2C Modules Connected



18.1.1 Features

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
 - Support for 8-bit format transfers
 - 7-bit and 10-bit addressing modes
 - General call
 - START byte mode
 - Support for multiple master-transmitters and slave-receivers
 - Support for multiple slave-transmitters and master-receivers
 - Combined master transmit/receive and receive/transmit mode
 - Data transfer rate of from 10 kbps up to 400 kbps (Philips Fast-mode rate)
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- One interrupt that can always be used by the CPU. This interrupt can be generated as a result of one of the following conditions: transmit-data ready, receive-data ready, register-access ready, no-acknowledgment received, arbitration lost, stop condition detected, addressed as slave.
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

18.1.2 Features Not Supported

The I2C module does not support:

- High-speed mode (Hs-mode)
- CBUS-compatibility mode

18.1.3 Functional Overview

Each device connected to an I2C-bus is recognized by a unique address. Each device can operate as either a transmitter or a receiver, depending on the function of the device. A device connected to the I2C-bus can also be considered as the master or the slave when performing data transfers. A master device is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. During this transfer, any device addressed by this master is considered a slave. The I2C module supports the multi-master mode, in which one or more devices capable of controlling an I2C-bus can be connected to the same I2C-bus.

For data communication, the I2C module has a serial data pin (SDA) and a serial clock pin (SCL), as shown in the *Registers* section. These two pins carry information between the 28x device and other devices connected to the I2C-bus. The SDA and SCL pins both are bidirectional. They each must be connected to a positive supply voltage using a pull-up resistor. When the bus is free, both pins are high. The driver of these two pins has an open-drain configuration to perform the required wired-AND function.

There are two major transfer techniques:

- Standard Mode: Send exactly n data values, where n is a value you program in an I2C module register. See the *Register* section for more information.
- Repeat Mode: Keep sending data values until you use software to initiate a STOP condition or a new START condition. See *Registers* for RM bit information.

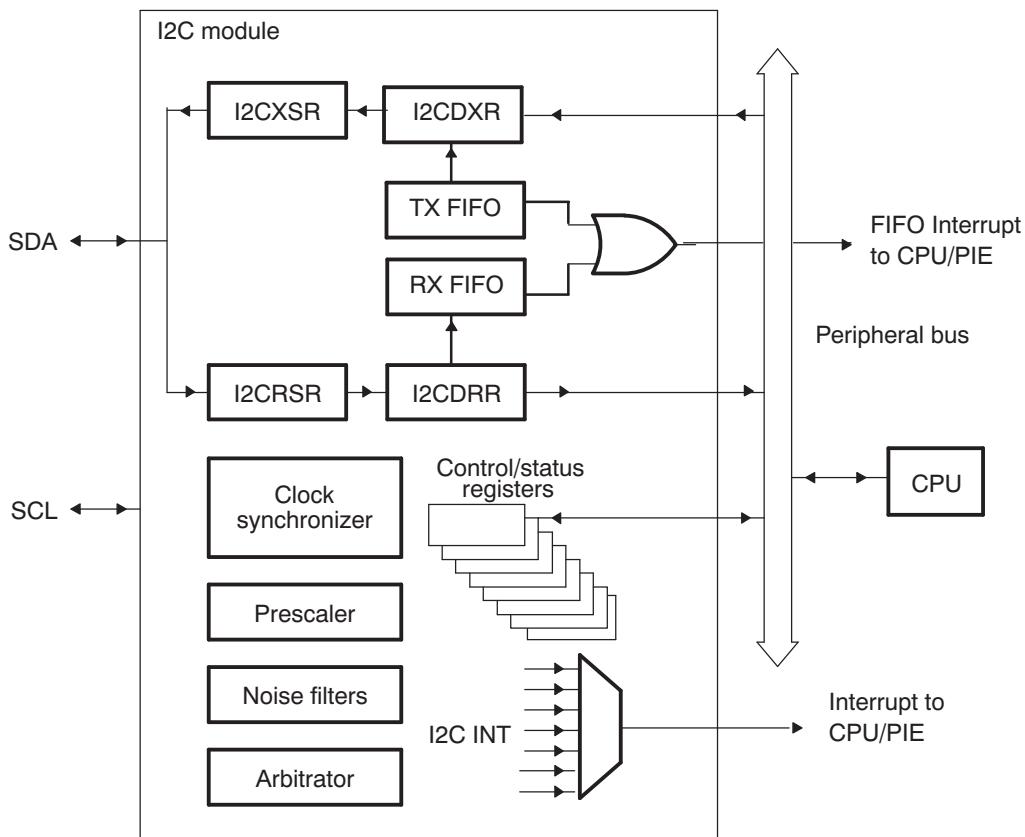
The I2C module consists of the following primary blocks:

- A serial interface: one data pin (SDA) and one clock pin (SCL)
- Data registers and FIFOs to temporarily hold receive data and transmit data traveling between the SDA pin and the CPU
- Control and status registers
- A peripheral bus interface to enable the CPU to access the I2C module registers and FIFOs.

- A clock synchronizer to synchronize the I2C input clock (from the device clock generator) and the clock on the SCL pin, and to synchronize data transfers with masters of different clock speeds
- A prescaler to divide down the input clock that is driven to the I2C module
- A noise filter on each of the two pins, SDA and SCL
- An arbitrator to handle arbitration between the I2C module (when it is a master) and another master
- Interrupt generation logic, so that an interrupt can be sent to the CPU
- FIFO interrupt generation logic, so that FIFO access can be synchronized to data reception and data transmission in the I2C module

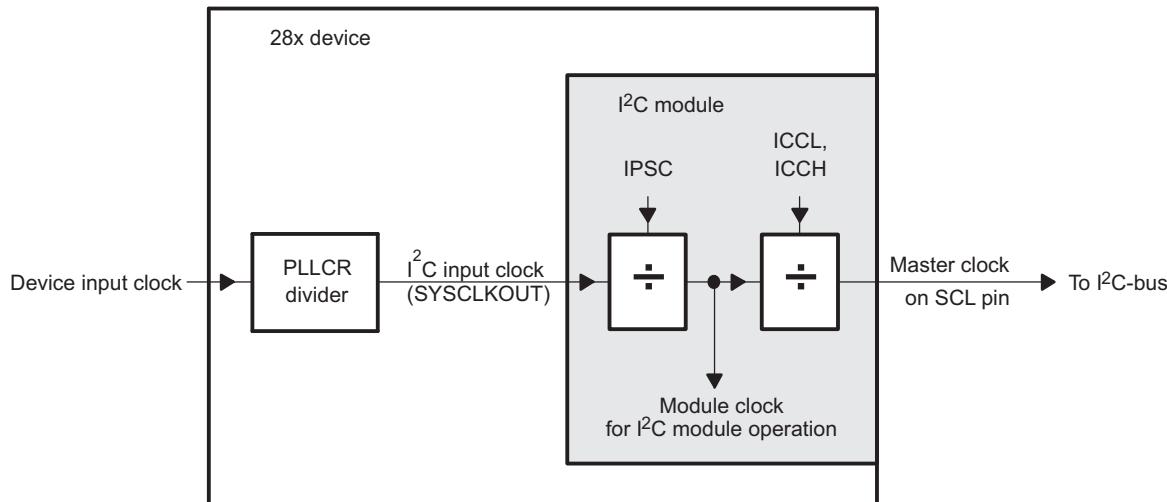
Figure 18-2 shows the four registers used for transmission and reception in non-FIFO mode. The CPU writes data for transmission to I2CDXR and reads received data from I2CDRR. When the I2C module is configured as a transmitter, data written to I2CDXR is copied to I2CXSR and shifted out on the SDA pin one bit at a time. When the I2C module is configured as a receiver, received data is shifted into I2CRSR and then copied to I2CDRR.

Figure 18-2. I2C Module Conceptual Block Diagram



18.1.4 Clock Generation

As shown in Figure 18-3, the device clock generator receives a signal from an external clock source and produces an I2C input clock with a programmed frequency. The I2C input clock is equivalent to the CPU clock and is then divided twice more inside the I2C module to produce the module clock and the master clock.

Figure 18-3. Clocking Diagram for the I²C Module

The module clock determines the frequency at which the I²C module operates. A programmable prescaler in the I²C module divides down the I²C input clock to produce the module clock. To specify the divide-down value, initialize the IPSC field of the prescaler register, I2CPSC. The resulting frequency is:

$$\text{module clock frequency} = \frac{\text{I}^2\text{C input clock frequency}}{(\text{IPSC} + 1)}$$

NOTE: To meet all of the I²C protocol timing specifications, the module clock must be configured between 7 - 12 MHz.

The prescaler must be initialized only while the I²C module is in the reset state (IRS = 0 in I2CMDR). The prescaled frequency takes effect only when IRS is changed to 1. Changing the IPSC value while IRS = 1 has no effect.

The master clock appears on the SCL pin when the I²C module is configured to be a master on the I²C-bus. This clock controls the timing of communication between the I²C module and a slave. As shown in [Figure 18-3](#), a second clock divider in the I²C module divides down the module clock to produce the master clock. The clock divider uses the ICCL value of I2CCLKL to divide down the low portion of the module clock signal and uses the ICCH value of I2CCLKH to divide down the high portion of the module clock signal. See the master clock frequency equation above.

18.2 I²C Module Operational Details

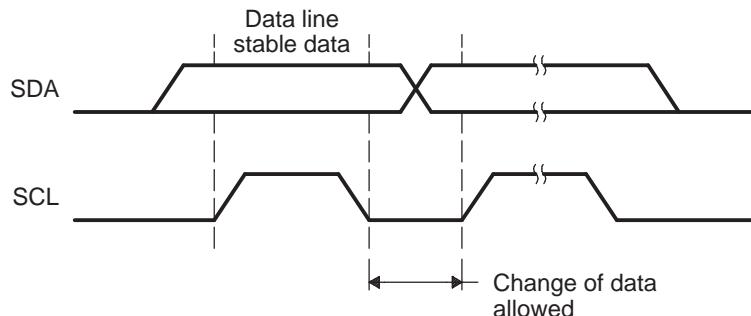
This section provides an overview of the I²C-bus protocol and how it is implemented.

18.2.1 Input and Output Voltage Levels

One clock pulse is generated by the master device for each data bit transferred. Due to a variety of different technology devices that can be connected to the I²C-bus, the levels of logic 0 (low) and logic 1 (high) are not fixed and depend on the associated level of V_{DD}. For details, see the data manual for your particular device.

18.2.2 Data Validity

The data on SDA must be stable during the high period of the clock (see [Figure 18-4](#)). The high or low state of the data line, SDA, should change only when the clock signal on SCL is low.

Figure 18-4. Bit Transfer on the I2C-Bus

18.2.3 Operating Modes

The I2C module has four basic operating modes to support data transfers as a master and as a slave. See [Table 18-1](#) for the names and descriptions of the modes.

If the I2C module is a master, it begins as a master-transmitter and typically transmits an address for a particular slave. When giving data to the slave, the I2C module must remain a master-transmitter. To receive data from a slave, the I2C module must be changed to the master-receiver mode.

If the I2C module is a slave, it begins as a slave-receiver and typically sends acknowledgment when it recognizes its slave address from a master. If the master will be sending data to the I2C module, the module must remain a slave-receiver. If the master has requested data from the I2C module, the module must be changed to the slave-transmitter mode.

Table 18-1. Operating Modes of the I2C Module

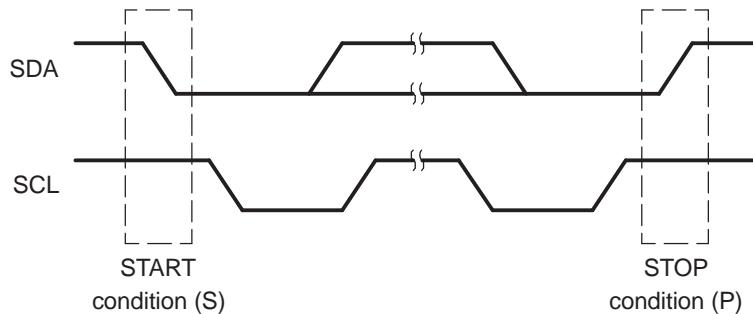
Operating Mode	Description
Slave-receiver modes	The I2C module is a slave and receives data from a master. All slaves begin in this mode. In this mode, serial data bits received on SDA are shifted in with the clock pulses that are generated by the master. As a slave, the I2C module does not generate the clock signal, but it can hold SCL low while the intervention of the device is required (RSFULL = 1 in I2CSTR) after a byte has been received. See section Section 18.2.7 for more details.
Slave-transmitter mode	The I2C module is a slave and transmits data to a master. This mode can be entered only from the slave-receiver mode; the I2C module must first receive a command from the master. When you are using any of the 7-bit/10-bit addressing formats, the I2C module enters its slave-transmitter mode if the slave address byte is the same as its own address (in I2COAR) and the master has transmitted R/W = 1. As a slave-transmitter, the I2C module then shifts the serial data out on SDA with the clock pulses that are generated by the master. While a slave, the I2C module does not generate the clock signal, but it can hold SCL low while the intervention of the device is required (XSMT = 0 in I2CSTR) after a byte has been transmitted. See section Section 18.2.7 for more details.
Master-receiver mode	The I2C module is a master and receives data from a slave. This mode can be entered only from the master-transmitter mode; the I2C module must first transmit a command to the slave. When you are using any of the 7-bit/10-bit addressing formats, the I2C module enters its master-receiver mode after transmitting the slave address byte and R/W = 1. Serial data bits on SDA are shifted into the I2C module with the clock pulses generated by the I2C module on SCL. The clock pulses are inhibited and SCL is held low when the intervention of the device is required (RSFULL = 1 in I2CSTR) after a byte has been received.
Master-transmitter modes	The IC module is a master and transmits control information and data to a slave. All masters begin in this mode. In this mode, data assembled in any of the 7-bit/10-bit addressing formats is shifted out on SDA. The bit shifting is synchronized with the clock pulses generated by the I2C module on SCL. The clock pulses are inhibited and SCL is held low when the intervention of the device is required (XSMT = 0 in I2CSTR) after a byte has been transmitted.

18.2.4 I2C Module START and STOP Conditions

START and STOP conditions can be generated by the I2C module when the module is configured to be a master on the I2C-bus. As shown in [Figure 18-5](#):

- The START condition is defined as a high-to-low transition on the SDA line while SCL is high. A master drives this condition to indicate the start of a data transfer.
- The STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. A master drives this condition to indicate the end of a data transfer.

Figure 18-5. I2C Module START and STOP Conditions



After a START condition and before a subsequent STOP condition, the I2C-bus is considered busy, and the bus busy (BB) bit of I2CSTR is 1. Between a STOP condition and the next START condition, the bus is considered free, and BB is 0.

For the I2C module to start a data transfer with a START condition, the master mode bit (MST) and the START condition bit (STT) in I2CMDR must both be 1. For the I2C module to end a data transfer with a STOP condition, the STOP condition bit (STP) must be set to 1. When the BB bit is set to 1 and the STT bit is set to 1, a repeated START condition is generated. For a description of I2CMDR and its bits (including MST, STT, and STP), see *Registers*.

18.2.5 Serial Data Formats

[Figure 18-6](#) shows an example of a data transfer on the I2C-bus. The I2C module supports 1 to 8-bit data values. In [Figure 18-6](#), 8-bit data is transferred. Each bit put on the SDA line equates to 1 pulse on the SCL line, and the values are always transferred with the most significant bit (MSB) first. The number of data values that can be transmitted or received is unrestricted. The serial data format used in [Figure 18-6](#) is the 7-bit addressing format. The I2C module supports the formats shown in [Figure 18-7](#) through [Figure 18-9](#) and described in the paragraphs that follow the figures.

NOTE: In [Figure 18-6](#) through [Figure 18-9](#), n = the number of data bits (from 1 to 8) specified by the bit count (BC) field of I2CMDR.

Figure 18-6. I2C Module Data Transfer (7-Bit Addressing with 8-bit Data Configuration Shown)

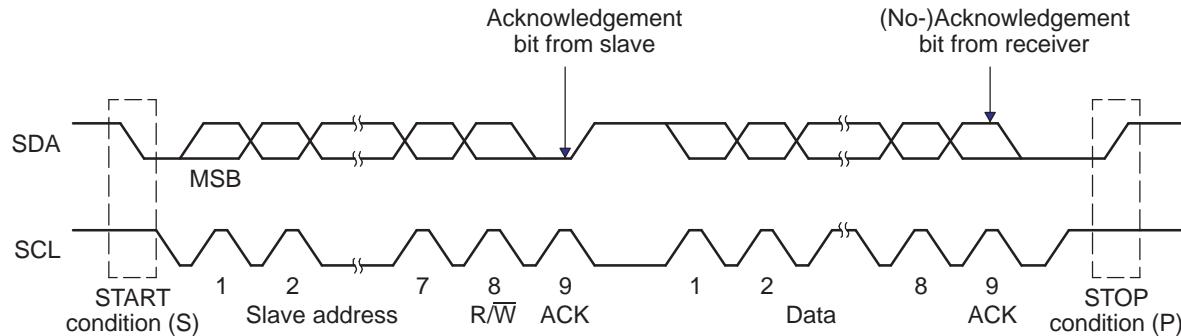


Figure 18-7. I2C Module 7-Bit Addressing Format (FDF = 0, XA = 0 in I2CMDR)

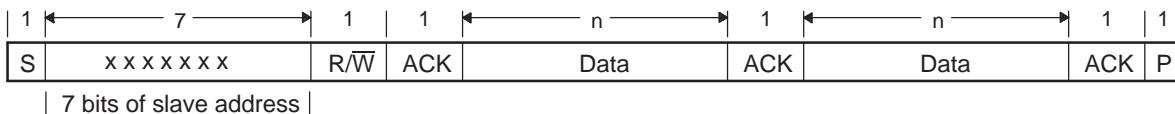


Figure 18-8. I2C Module 10-Bit Addressing Format (FDF = 0, XA = 1 in I2CMDR)

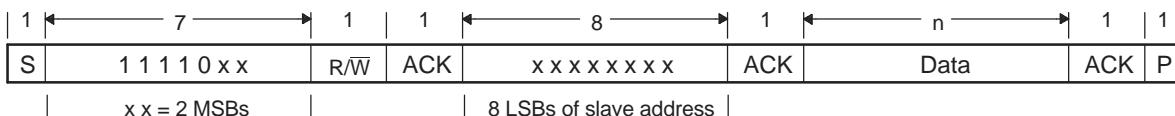
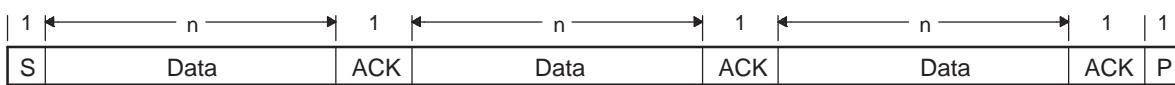


Figure 18-9. I2C Module Free Data Format (FDF = 1 in I2CMDR)



18.2.5.1 7-Bit Addressing Format

In the 7-bit addressing format (see [Figure 18-7](#)), the first byte after a START condition (S) consists of a 7-bit slave address followed by a R/W bit. R/W determines the direction of the data:

- R/W = 0: The master writes (transmits) data to the addressed slave.
- R/W = 1: The master reads (receives) data from the slave.

An extra clock cycle dedicated for acknowledgment (ACK) is inserted after each byte. If the ACK bit is inserted by the slave after the first byte from the master, it is followed by n bits of data from the transmitter (master or slave, depending on the R/W bit). n is a number from 1 to 8 determined by the bit count (BC) field of I2CMDR. After the data bits have been transferred, the receiver inserts an ACK bit.

To select the 7-bit addressing format, write 0 to the expanded address enable (XA) bit of I2CMDR, and make sure the free data format mode is off (FDF = 0 in I2CMDR).

18.2.5.2 10-Bit Addressing Format

The 10-bit addressing format (see [Figure 18-8](#)) is similar to the 7-bit addressing format, but the master sends the slave address in two separate byte transfers. The first byte consists of 11110b, the two MSBs of the 10-bit slave address, and R/W = 0 (write). The second byte is the remaining 8 bits of the 10-bit slave address. The slave must send acknowledgment after each of the two byte transfers. Once the master has written the second byte to the slave, the master can either write data or use a repeated START condition to change the data direction. For more details about using 10-bit addressing, see the Philips Semiconductors I2C-bus specification.

To select the 10-bit addressing format, write 1 to the XA bit of I2CMDR and make sure the free data format mode is off (FDF = 0 in I2CMDR).

18.2.5.3 Free Data Format

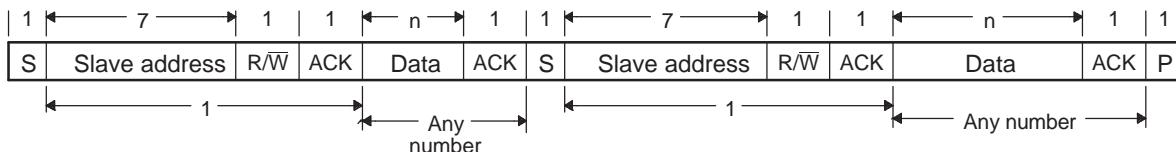
In this format (see [Figure 18-9](#)), the first byte after a START condition (S) is a data byte. An ACK bit is inserted after each data byte, which can be from 1 to 8 bits, depending on the BC field of I2CMDR. No address or data-direction bit is sent. Therefore, the transmitter and the receiver must both support the free data format, and the direction of the data must be constant throughout the transfer.

To select the free data format, write 1 to the free data format (FDF) bit of I2CMDR. The free data format is not supported in the digital loopback mode (DLB = 1 in I2CMDR).

18.2.5.4 Using a Repeated START Condition

At the end of each data byte, the master can drive another START condition. Using this capability, a master can communicate with multiple slave addresses without having to give up control of the bus by driving a STOP condition. The length of a data byte can be from 1 to 8 bits and is selected with the BC field of I2CMDR. The repeated START condition can be used with the 7-bit addressing, 10-bit addressing, and free data formats. [Figure 18-10](#) shows a repeated START condition in the 7-bit addressing format.

Figure 18-10. Repeated START Condition (in This Case, 7-Bit Addressing Format)



NOTE: In [Figure 18-10](#), n = the number of data bits (from 1 to 8) specified by the bit count (BC) field of I2CMDR.

18.2.6 NACK Bit Generation

When the I2C module is a receiver (master or slave), it can acknowledge or ignore bits sent by the transmitter. To ignore any new bits, the I2C module must send a no-acknowledge (NACK) bit during the acknowledge cycle on the bus. [Table 18-2](#) summarizes the various ways you can tell the I2C module to send a NACK bit.

Table 18-2. Ways to Generate a NACK Bit

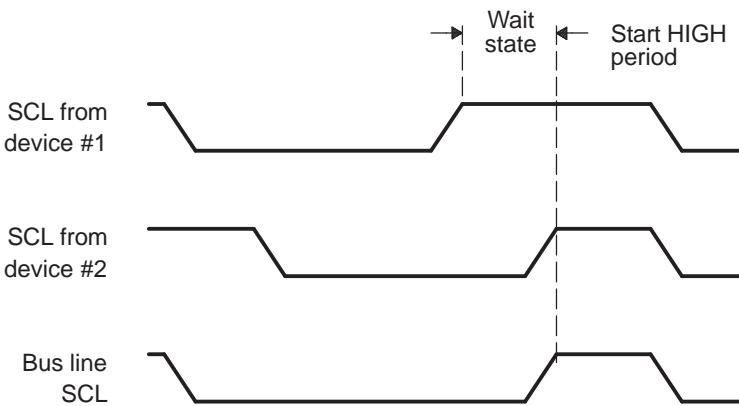
I2C Module Condition	NACK Bit Generation Options
Slave-receiver modes	<ul style="list-style-type: none"> Allow an overrun condition (RSFULL = 1 in I2CSTR) Reset the module (IRS = 0 in I2CMDR) Set the NACKMOD bit of I2CMDR before the rising edge of the last data bit you intend to receive
Master-receiver mode AND Repeat mode (RM = 1 in I2CMDR)	<ul style="list-style-type: none"> Generate a STOP condition (STP = 1 in I2CMDR) Reset the module (IRS = 0 in I2CMDR) Set the NACKMOD bit of I2CMDR before the rising edge of the last data bit you intend to receive
Master-receiver mode AND Nonrepeat mode (RM = 0 in I2CMDR)	<ul style="list-style-type: none"> If STP = 1 in I2CMDR, allow the internal data counter to count down to 0 and thus force a STOP condition If STP = 0, make STP = 1 to generate a STOP condition Reset the module (IRS = 0 in I2CMDR). = 1 to generate a STOP condition Set the NACKMOD bit of I2CMDR before the rising edge of the last data bit you intend to receive

18.2.7 Clock Synchronization

Under normal conditions, only one master device generates the clock signal, SCL. During the arbitration procedure, however, there are two or more masters and the clock must be synchronized so that the data output can be compared. [Figure 18-11](#) illustrates the clock synchronization. The wired-AND property of SCL means that a device that first generates a low period on SCL overrules the other devices. At this high-to-low transition, the clock generators of the other devices are forced to start their own low period. The SCL is held low by the device with the longest low period. The other devices that finish their low periods must wait for SCL to be released, before starting their high periods. A synchronized signal on SCL is obtained, where the slowest device determines the length of the low period and the fastest device determines the length of the high period.

If a device pulls down the clock line for a longer time, the result is that all clock generators must enter the wait state. In this way, a slave slows down a fast master and the slow device creates enough time to store a received byte or to prepare a byte to be transmitted.

Figure 18-11. Synchronization of Two I2C Clock Generators During Arbitration



18.2.8 Arbitration

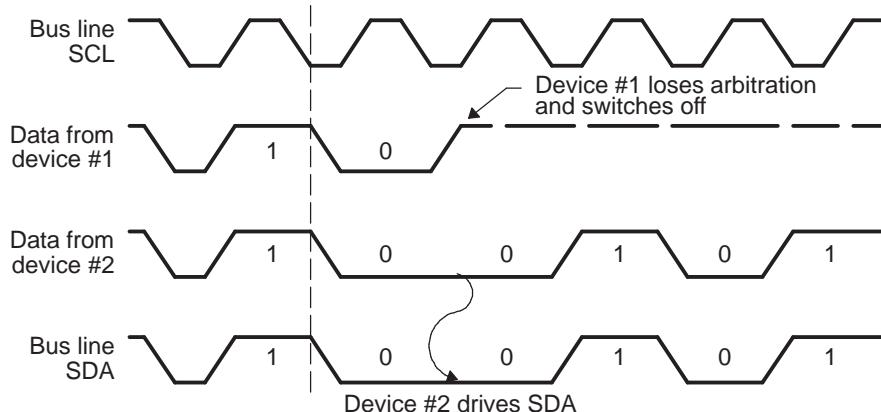
If two or more master-transmitters attempt to start a transmission on the same bus at approximately the same time, an arbitration procedure is invoked. The arbitration procedure uses the data presented on the serial data bus (SDA) by the competing transmitters. [Figure 18-12](#) illustrates the arbitration procedure between two devices. The first master-transmitter, which releases the SDA line high, is overruled by another master-transmitter that drives SDA low. The arbitration procedure gives priority to the device that transmits the serial data stream with the lowest binary value. Should two or more devices send identical first bytes, arbitration continues on the subsequent bytes.

If the I2C module is the losing master, it switches to the slave-receiver mode, sets the arbitration lost (AL) flag, and generates the arbitration-lost interrupt request.

If during a serial transfer the arbitration procedure is still in progress when a repeated START condition or a STOP condition is transmitted to SDA, the master-transmitters involved must send the repeated START condition or the STOP condition at the same position in the format frame. Arbitration is not allowed between:

- A repeated START condition and a data bit
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Figure 18-12. Arbitration Procedure Between Two Master-Transmitters



18.3 Interrupt Requests Generated by the I2C Module

The I2C module can generate seven types of basic interrupt requests, which are described in [Section 18.3.1](#). Two of these can tell the CPU when to write transmit data and when to read receive data. If you want the FIFOs to handle transmit and receive data, you can also use the FIFO interrupts described in [Section 18.3.2](#). The basic I2C interrupts are combined to form PIE Group 8, Interrupt 1 (I2CINT1A_ISR), and the FIFO interrupts are combined to form PIE Group 8, Interrupt 2 (I2CINT2A_ISR).

18.3.1 Basic I2C Interrupt Requests

The I2C module generates the interrupt requests described in [Table 18-3](#). As shown in [Figure 18-13](#), all requests are multiplexed through an arbiter to a single I2C interrupt request to the CPU. Each interrupt request has a flag bit in the status register (I2CSTR) and an enable bit in the interrupt enable register (I2CIER). When one of the specified events occurs, its flag bit is set. If the corresponding enable bit is 0, the interrupt request is blocked. If the enable bit is 1, the request is forwarded to the CPU as an I2C interrupt.

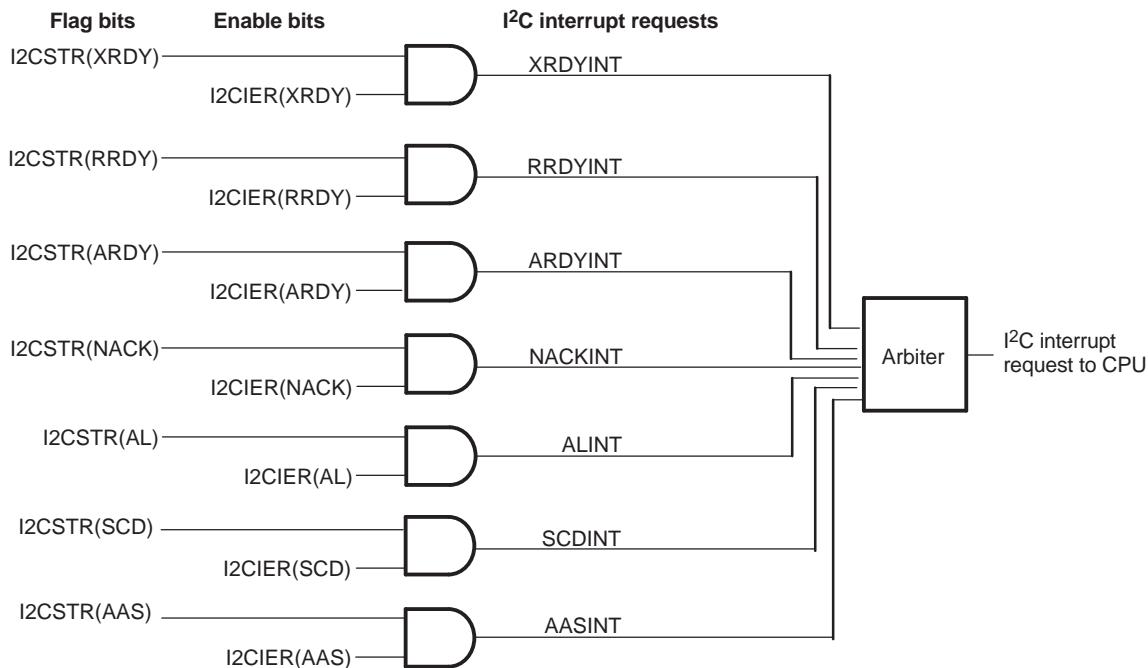
The I2C interrupt is one of the maskable interrupts of the CPU. As with any maskable interrupt request, if it is properly enabled in the CPU, the CPU executes the corresponding interrupt service routine (I2CINT1A_ISR). The I2CINT1A_ISR for the I2C interrupt can determine the interrupt source by reading the interrupt source register, I2CISRC. Then the I2CINT1A_ISR can branch to the appropriate subroutine.

After the CPU reads I2CISRC, the following events occur:

1. The flag for the source interrupt is cleared in I2CSTR. Exception: The ARDY, RRDY, and XRDY bits in I2CSTR are not cleared when I2CISRC is read. To clear one of these bits, write a 1 to it.
2. The arbiter determines which of the remaining interrupt requests has the highest priority, writes the code for that interrupt to I2CISRC, and forwards the interrupt request to the CPU.

Table 18-3. Descriptions of the Basic I2C Interrupt Requests

I2C Interrupt Request	Interrupt Source
XRDYINT	Transmit ready condition: The data transmit register (I2CDXR) is ready to accept new data because the previous data has been copied from I2CDXR to the transmit shift register (I2CXSR). As an alternative to using XRDYINT, the CPU can poll the XRDY bit of the status register, I2CSTR. XRDYINT should not be used when in FIFO mode. Use the FIFO interrupts instead.
RRDYINT	Receive ready condition: The data receive register (I2CDRR) is ready to be read because data has been copied from the receive shift register (I2CRSR) to I2CDRR. As an alternative to using RRDYINT, the CPU can poll the RRDY bit of I2CSTR. RRDYINT should not be used when in FIFO mode. Use the FIFO interrupts instead.
ARDYINT	Register-access ready condition: The I2C module registers are ready to be accessed because the previously programmed address, data, and command values have been used. The specific events that generate ARDYINT are the same events that set the ARDY bit of I2CSTR. As an alternative to using ARDYINT, the CPU can poll the ARDY bit.
NACKINT	No-acknowledgment condition: The I2C module is configured as a master-transmitter and did not receive acknowledgment from the slave-receiver. As an alternative to using NACKINT, the CPU can poll the NACK bit of I2CSTR.
ALINT	Arbitration-lost condition: The I2C module has lost an arbitration contest with another master-transmitter. As an alternative to using ALINT, the CPU can poll the AL bit of I2CSTR.
SCDINT	Stop condition detected: A STOP condition was detected on the I2C bus. As an alternative to using SCDINT, the CPU can poll the SCD bit of the status register, I2CSTR.
AASINT	Addressed as slave condition: The I2C has been addressed as a slave device by another master on the I2C bus. As an alternative to using AASINT, the CPU can poll the AAS bit of the status register, I2CSTR.

Figure 18-13. Enable Paths of the I2C Interrupt Requests

18.3.2 I2C FIFO Interrupts

In addition to the seven basic I2C interrupts, the transmit and receive FIFOs each contain the ability to generate an interrupt (I2CINT2A). The transmit FIFO can be configured to generate an interrupt after transmitting a defined number of bytes, up to 16. The receive FIFO can be configured to generate an interrupt after receiving a defined number of bytes, up to 16. These two interrupt sources are ORed together into a single maskable CPU interrupt. The interrupt service routine can then read the FIFO interrupt status flags to determine from which source the interrupt came. See the I2C transmit FIFO register (I2CFFTX) and the I2C receive FIFO register (I2CFFRX) descriptions.

18.4 Resetting/Disabling the I2C Module

You can reset/disable the I2C module in two ways:

- Write 0 to the I2C reset bit (IRS) in the I2C mode register (I2CMDR). All status bits (in I2CSTR) are forced to their default values, and the I2C module remains disabled until IRS is changed to 1. The SDA and SCL pins are in the high-impedance state.
- Initiate a device reset by driving the \overline{XRS} pin low. The entire device is reset and is held in the reset state until you drive the pin high. When \overline{XRS} is released, all I2C module registers are reset to their default values. The IRS bit is forced to 0, which resets the I2C module. The I2C module stays in the reset state until you write 1 to IRS.

IRS must be 0 while you configure/reconfigure the I2C module. Forcing IRS to 0 can be used to save power and to clear error conditions.

18.5 Registers

18.5.1 I2C Base Addresses

Table 18-4. I2C Base Address Table

Device Registers	Register Names	Start Address	End Address
I2caRegs	I2C_REGS	0x0000_7300	0x0000_733F
I2cbRegs	I2C_REGS	0x0000_7340	0x0000_737F

18.5.2 I2C_REGS Registers

Table 18-5 lists the memory-mapped registers for the I2C_REGS. All register offset addresses not listed in Table 18-5 should be considered as reserved locations and the register contents should not be modified.

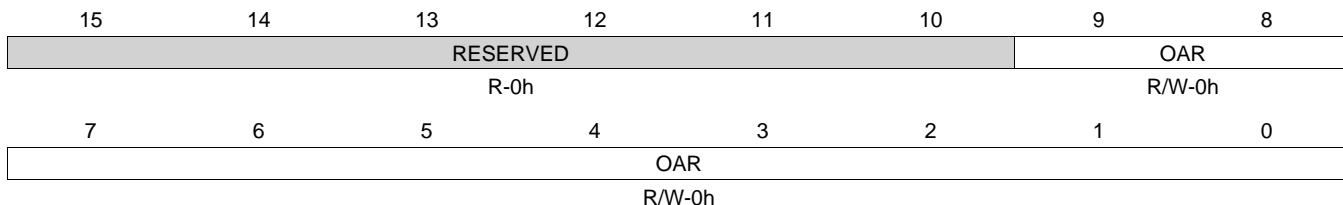
Table 18-5. I2C_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	I2COAR	I2C Own address	Section 18.5.2.1	
1h	I2CIER	I2C Interrupt Enable	Section 18.5.2.2	
2h	I2CSTR	I2C Status	Section 18.5.2.3	
3h	I2CCLKL	I2C Clock low-time divider	Section 18.5.2.4	
4h	I2CCLKH	I2C Clock high-time divider	Section 18.5.2.5	
5h	I2CCNT	I2C Data count	Section 18.5.2.6	
6h	I2CDRR	I2C Data receive	Section 18.5.2.7	
7h	I2CSAR	I2C Slave address	Section 18.5.2.8	
8h	I2CDXR	I2C Data Transmit	Section 18.5.2.9	
9h	I2CMDR	I2C Mode	Section 18.5.2.10	
Ah	I2CISRC	I2C Interrupt Source	Section 18.5.2.11	
Bh	I2CEMDR	I2C Extended Mode	Section 18.5.2.12	
Ch	I2CPSC	I2C Prescaler	Section 18.5.2.13	
20h	I2CFFTX	I2C FIFO Transmit	Section 18.5.2.14	
21h	I2CFFRX	I2C FIFO Receive	Section 18.5.2.15	

18.5.2.1 I2COAR Register (offset = 0h) [reset = 0h]

I2COAR is shown in [Figure 18-14](#) and described in [Table 18-6](#).

I2C Own address

Figure 18-14. I2COAR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-6. I2COAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	OAR	R/W	0h	In 7-bit addressing mode (XA = 0 in I2CMDR): 00h-7Fh Bits 6-0 provide the 7-bit slave address of the I2C module. Write 0s to bits 9-7. In 10-bit addressing mode (XA = 1 in I2CMDR): 000h-3FFh Bits 9-0 provide the 10-bit slave address of the I2C module.

18.5.2.2 I2CIER Register (offset = 1h) [reset = 0h]

I2CIER is shown in [Figure 18-15](#) and described in [Table 18-7](#).

I2C Interrupt Enable

Figure 18-15. I2CIER Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	AAS	SCD	XRDY	RRDY	ARDY	NACK	ARBL
R-0h	R/W-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-7. I2CIER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6	AAS	R/W	0h	Addressed as slave interrupt enable 0h (R/W) = Interrupt request disabled 1h (R/W) = Interrupt request enabled
5	SCD	R/W	0h	Stop condition detected interrupt enable 0h (R/W) = Interrupt request disabled 1h (R/W) = Interrupt request enabled
4	XRDY	R/W	0h	Transmit-data-ready interrupt enable bit. This bit should not be set when using FIFO mode. 0h (R/W) = Interrupt request disabled 1h (R/W) = Interrupt request enabled
3	RRDY	R/W	0h	Receive-data-ready interrupt enable bit. This bit should not be set when using FIFO mode. 0h (R/W) = Interrupt request disabled 1h (R/W) = Interrupt request enabled
2	ARDY	R/W	0h	Register-access-ready interrupt enable 0h (R/W) = Interrupt request disabled 1h (R/W) = Interrupt request enabled
1	NACK	R/W	0h	No-acknowledgment interrupt enable 0h (R/W) = Interrupt request disabled 1h (R/W) = Interrupt request enabled
0	ARBL	R/W	0h	Arbitration-lost interrupt enable 0h (R/W) = Interrupt request disabled 1h (R/W) = Interrupt request enabled

18.5.2.3 I2CSTR Register (offset = 2h) [reset = 0h]

I2CSTR is shown in [Figure 18-16](#) and described in [Table 18-8](#).

I2C Status

Figure 18-16. I2CSTR Register

15	14	13	12	11	10	9	8
RESERVED	SDIR	NACKSNT	BB	RSFULL	XSMY	AAS	AD0
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	SCD	XRDY	RRDY	ARDY	NACK	ARBL	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-8. I2CSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	SDIR	R/W	0h	<p>Slave direction bit</p> <p>0h (R/W) = I2C is not addressed as a slave transmitter. SDIR is cleared by one of the following events:</p> <ul style="list-style-type: none"> - It is manually cleared. To clear this bit, write a 1 to it. - Digital loopback mode is enabled. - A START or STOP condition occurs on the I2C bus. <p>1h (R/W) = I2C is addressed as a slave transmitter.</p>
13	NACKSNT	R/W	0h	<p>NACK sent bit.</p> <p>This bit is used when the I2C module is in the receiver mode. One instance in which NACKSNT is affected is when the NACK mode is used (see the description for NACKMOD in</p> <p>0h (R/W) = NACK not sent. NACKSNT bit is cleared by any one of the following events:</p> <ul style="list-style-type: none"> - It is manually cleared. To clear this bit, write a 1 to it. - The I2C module is reset (either when 0 is written to the IRS bit of I2CMDR or when the whole device is reset). <p>1h (R/W) = NACK sent: A no-acknowledge bit was sent during the acknowledge cycle on the I2C-bus.</p>
12	BB	R/W	0h	<p>Bus busy bit.</p> <p>BB indicates whether the I2C-bus is busy or is free for another data transfer. See the paragraph following the table for more information</p> <p>0h (R/W) = Bus free. BB is cleared by any one of the following events:</p> <ul style="list-style-type: none"> - The I2C module receives or transmits a STOP bit (bus free). - The I2C module is reset. <p>1h (R/W) = Bus busy: The I2C module has received or transmitted a START bit on the bus.</p>

Table 18-8. I2CSTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RSFULL	R/W	0h	<p>Receive shift register full bit.</p> <p>RSFULL indicates an overrun condition during reception. Overrun occurs when new data is received into the shift register (I2CRSR) and the old data has not been read from the receive register (I2CDRR). As new bits arrive from the SDA pin, they overwrite the bits in I2CRSR. The new data will not be copied to ICDRR until the previous data is read.</p> <p>0h (R/W) = No overrun detected. RSV is cleared by any one of the following events:</p> <ul style="list-style-type: none"> - I2CDRR is read by the CPU. Emulator reads of the I2CDRR do not affect this bit. - The I2C module is reset. <p>1h (R/W) = Overrun detected</p>
10	XSMT	R/W	0h	<p>Transmit shift register empty bit.</p> <p>XSMT = 0 indicates that the transmitter has experienced underflow. Underflow occurs when the transmit shift register (I2CXSR) is empty but the data transmit register (I2CDXR) has not been loaded since the last I2CDXR-to-I2CXSR transfer. The next I2CDXR-to-I2CXSR transfer will not occur until new data is in I2CDXR. If new data is not transferred in time, the previous data may be re-transmitted on the SDA pin.</p> <p>0h (R/W) = Underflow detected (empty)</p> <p>1h (R/W) = No underflow detected (not empty). XSMT is set by one of the following events:</p> <ul style="list-style-type: none"> - Data is written to I2CDXR. - The I2C module is reset
9	AAS	R/W	0h	<p>Addressed-as-slave bit</p> <p>0h (R/W) = In the 7-bit addressing mode, the AAS bit is cleared when receiving a NACK, a STOP condition, or a repeated START condition. In the 10-bit addressing mode, the AAS bit is cleared when receiving a NACK, a STOP condition, or by a slave address different from the I2C peripheral's own slave address.</p> <p>1h (R/W) = The I2C module has recognized its own slave address or an address of all zeros (general call). The AAS bit is also set if the first byte has been received in the free data format (FDF = 1 in I2CMDR).</p>
8	AD0	R/W	0h	<p>Address 0 bits</p> <p>0h (R/W) = AD0 has been cleared by a START or STOP condition.</p> <p>1h (R/W) = An address of all zeros (general call) is detected.</p>
7-6	RESERVED	R/W	0h	Reserved
5	SCD	R/W	0h	<p>Stop condition detected bit.</p> <p>SCD is set when the I2C sends or receives a STOP condition. The I2C module delays clearing of the I2CMDR[STP] bit until the SCD bit is set.</p> <p>0h (R/W) = STOP condition not detected since SCD was last cleared. SCD is cleared by any one of the following events:</p> <ul style="list-style-type: none"> - I2CISRC is read by the CPU when it contains the value 110b (stop condition detected). Emulator reads of the I2CISRC do not affect this bit. - SCD is manually cleared. To clear this bit, write a 1 to it. - The I2C module is reset. <p>1h (R/W) = A STOP condition has been detected on the I2C bus.</p>

Table 18-8. I2CSTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R/W	0h	<p>Transmit-data-ready interrupt flag bit.</p> <p>When not in FIFO mode, XRDY indicates that the data transmit register (I2CDXR) is ready to accept new data because the previous data has been copied from I2CDXR to the transmit shift register (I2CXSR). The CPU can poll XRDY or use the XRDY interrupt request. When in FIFO mode, use TXFFINT instead.</p> <p>0h (R/W) = I2CDXR not ready. XRDY is cleared when data is written to I2CDXR.</p> <p>1h (R/W) = I2CDXR ready: Data has been copied from I2CDXR to I2CXSR.</p> <p>XRDY is also forced to 1 when the I2C module is reset.</p>
3	RRDY	R/W	0h	<p>Receive-data-ready interrupt flag bit.</p> <p>When not in FIFO mode, RRDY indicates that the data receive register (I2CDRR) is ready to be read because data has been copied from the receive shift register (I2CRSR) to I2CDRR. The CPU can poll RRDY or use the RRDY interrupt request. When in FIFO mode, use RXFFINT instead.</p> <p>0h (R/W) = I2CDRR not ready. RRDY is cleared by any one of the following events:</p> <ul style="list-style-type: none"> - I2CDRR is read by the CPU. Emulator reads of the I2CDRR do not affect this bit. - RRDY is manually cleared. To clear this bit, write a 1 to it. - The I2C module is reset. <p>1h (R/W) = I2CDRR ready: Data has been copied from I2CRSR to I2CDRR.</p>
2	ARDY	R/W	0h	<p>Register-access-ready interrupt flag bit (only applicable when the I2C module is in the master mode).</p> <p>ARDY indicates that the I2C module registers are ready to be accessed because the previously programmed address, data, and command values have been used. The CPU can poll ARDY or use the ARDY interrupt request.</p> <p>0h (R/W) = The registers are not ready to be accessed. ARDY is cleared by any one of the following events:</p> <ul style="list-style-type: none"> - The I2C module starts using the current register contents. - ARDY is manually cleared. To clear this bit, write a 1 to it. - The I2C module is reset. <p>1h (R/W) = The registers are ready to be accessed.</p> <p>In the nonrepeat mode (RM = 0 in I2CMDR): If STP = 0 in I2CMDR, the ARDY bit is set when the internal data counter counts down to 0. If STP = 1, ARDY is not affected (instead, the I2C module generates a STOP condition when the counter reaches 0).</p> <p>In the repeat mode (RM = 1): ARDY is set at the end of each byte transmitted from I2CDXR.</p>

Table 18-8. I2CSTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NACK	R/W	0h	<p>No-acknowledgment interrupt flag bit.</p> <p>NACK applies when the I2C module is a transmitter (master or slave). NACK indicates whether the I2C module has detected an acknowledge bit (ACK) or a noacknowledge bit (NACK) from the receiver. The CPU can poll NACK or use the NACK interrupt request</p> <p>0h (R/W) = ACK received/NACK not received. This bit is cleared by any one of the following events:</p> <ul style="list-style-type: none"> - An acknowledge bit (ACK) has been sent by the receiver. - NACK is manually cleared. To clear this bit, write a 1 to it. - The CPU reads the interrupt source register (I2CISRC) and the register contains the code for a NACK interrupt. Emulator reads of the I2CISRC do not affect this bit. - The I2C module is reset. <p>1h (R/W) = NACK bit received. The hardware detects that a no-acknowledge (NACK) bit has been received.</p> <p>Note: While the I2C module performs a general call transfer, NACK is 1, even if one or more slaves send acknowledgment.</p>
0	ARBL	R/W	0h	<p>Arbitration-lost interrupt flag bit (only applicable when the I2C module is a master-transmitter).</p> <p>AL primarily indicates when the I2C module has lost an arbitration contest with another mastertransmitter. The CPU can poll AL or use the AL interrupt request</p> <p>0h (R/W) = Arbitration not lost. AL is cleared by any one of the following events:</p> <ul style="list-style-type: none"> - AL is manually cleared. To clear this bit, write a 1 to it. - The CPU reads the interrupt source register (I2CISRC) and the register contains the code for an AL interrupt. Emulator reads of the I2CISRC do not affect this bit. - The I2C module is reset. <p>1h (R/W) = Arbitration lost. AL is set by any one of the following events:</p> <ul style="list-style-type: none"> - The I2C module senses that it has lost an arbitration with two or more competing transmitters that started a transmission almost simultaneously. - The I2C module attempts to start a transfer while the BB (bus busy) bit is set to 1. <p>When AL becomes 1, the MST and STP bits of I2CMDR are cleared, and the I2C module becomes a slave-receiver.</p>

18.5.2.4 I2CCLKL Register (offset = 3h) [reset = 0h]

I2CCLKL is shown in [Figure 18-17](#) and described in [Table 18-9](#).

I2C Clock low-time divider

Figure 18-17. I2CCLKL Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2CCLKL															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-9. I2CCLKL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	I2CCLKL	R/W	0h	<p>Clock low-time divide-down value.</p> <p>To produce the low-time duration of the master clock, the period of the module clock is multiplied by (ICCL + d). d is 5, 6, or 7 as described in Section 9.5.7.1.</p> <p>Note: These bits must be set to a non-zero value for proper I2C clock operation.</p>

18.5.2.5 I2CCLKH Register (offset = 4h) [reset = 0h]I2CCLKH is shown in [Figure 18-18](#) and described in [Table 18-10](#).

I2C Clock high-time divider

Figure 18-18. I2CCLKH Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2CCLKH															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

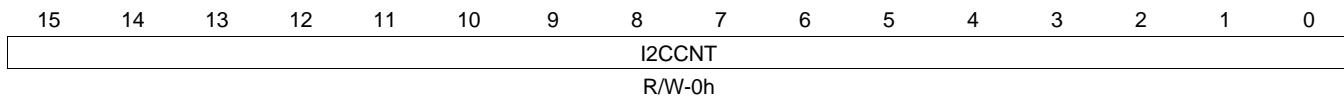
Table 18-10. I2CCLKH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	I2CCLKH	R/W	0h	<p>Clock high-time divide-down value.</p> <p>To produce the high-time duration of the master clock, the period of the module clock is multiplied by (ICCH + d). d is 5, 6, or 7 as described in Section 9.5.7.1.</p> <p>Note: These bits must be set to a non-zero value for proper I2C clock operation.</p>

18.5.2.6 I2CCNT Register (offset = 5h) [reset = 0h]

I2CCNT is shown in [Figure 18-19](#) and described in [Table 18-11](#).

I2C Data count

Figure 18-19. I2CCNT Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

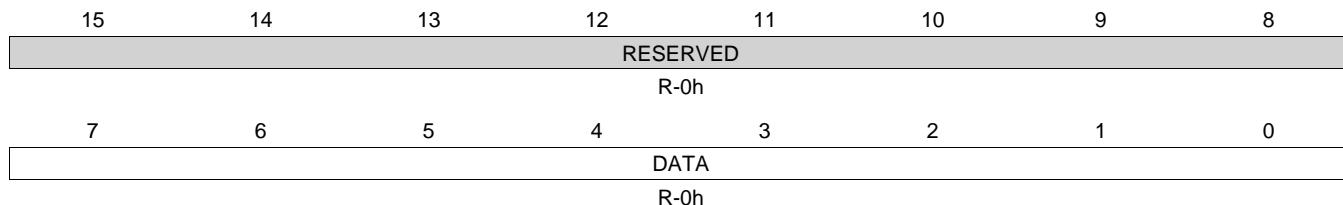
Table 18-11. I2CCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	I2CCNT	R/W	0h	<p>Data count value. ICDC indicates the number of data bytes to transfer or receive.</p> <p>The value in I2CCNT is a don't care when the RM bit in I2CMDR is set to 1.</p> <p>The start value loaded to the internal data counter is 65536.</p> <p>The start value loaded to internal data counter is 1-65535.</p>

18.5.2.7 I2CDRR Register (offset = 6h) [reset = 0h]

I2CDRR is shown in [Figure 18-20](#) and described in [Table 18-12](#).

I2C Data receive

Figure 18-20. I2CDRR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

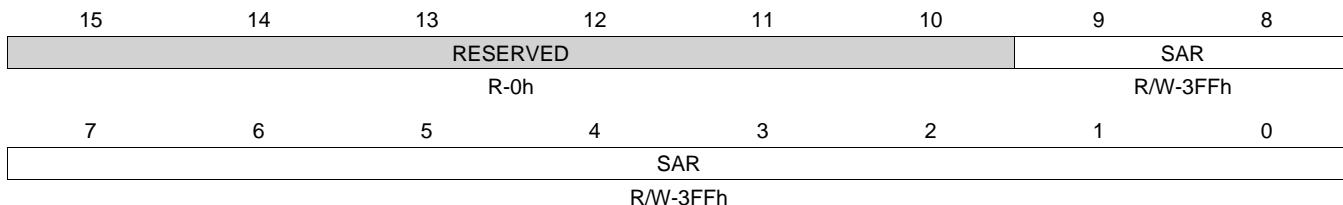
Table 18-12. I2CDRR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	DATA	R	0h	Receive data

18.5.2.8 I2CSR Register (offset = 7h) [reset = 3FFh]

I2CSR is shown in [Figure 18-21](#) and described in [Table 18-13](#).

I2C Slave address

Figure 18-21. I2CSR Register

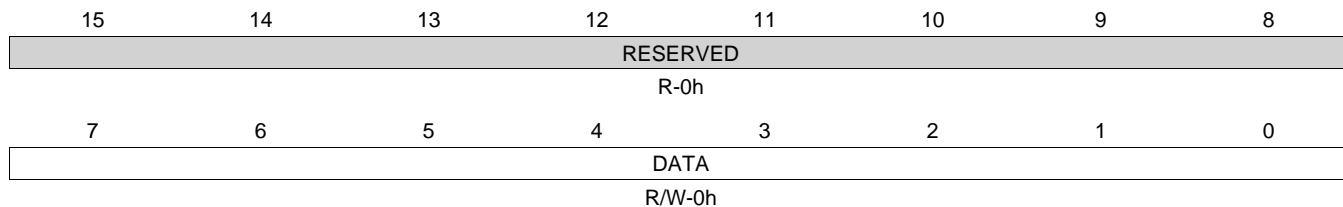
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-13. I2CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	SAR	R/W	3FFh	In 7-bit addressing mode (XA = 0 in I2CMDR): 00h-7Fh Bits 6-0 provide the 7-bit slave address that the I2C module transmits when it is in the master-transmitter mode. Write 0s to bits 9-7. In 10-bit addressing mode (XA = 1 in I2CMDR): 000h-3FFh Bits 9-0 provide the 10-bit slave address that the I2C module transmits when it is in the master transmitter mode.

18.5.2.9 I2CDXR Register (offset = 8h) [reset = 0h]I2CDXR is shown in [Figure 18-22](#) and described in [Table 18-14](#).

I2C Data Transmit

Figure 18-22. I2CDXR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-14. I2CDXR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	DATA	R/W	0h	Transmit data

18.5.2.10 I2CMDR Register (offset = 9h) [reset = 0h]

I2CMDR is shown in [Figure 18-23](#) and described in [Table 18-15](#).

I2C Mode

Figure 18-23. I2CMDR Register

15	14	13	12	11	10	9	8
NACKMOD	FREE	STT	RESERVED	STP	MST	TRX	XA
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RM	DLB	IRS	STB	FDF		BC	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-15. I2CMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NACKMOD	R/W	0h	<p>NACK mode bit.</p> <p>This bit is only applicable when the I2C module is acting as a receiver.</p> <p>0h (R/W) = In the slave-receiver mode: The I2C module sends an acknowledge (ACK) bit to the transmitter during each acknowledge cycle on the bus. The I2C module only sends a no-acknowledge (NACK) bit if you set the NACKMOD bit.</p> <p>In the master-receiver mode: The I2C module sends an ACK bit during each acknowledge cycle until the internal data counter counts down to 0. At that point, the I2C module sends a NACK bit to the transmitter. To have a NACK bit sent earlier, you must set the NACKMOD bit.</p> <p>1h (R/W) = In either slave-receiver or master-receiver mode: The I2C module sends a NACK bit to the transmitter during the next acknowledge cycle on the bus. Once the NACK bit has been sent, NACKMOD is cleared.</p> <p>Important: To send a NACK bit in the next acknowledge cycle, you must set NACKMOD before the rising edge of the last data bit.</p>
14	FREE	R/W	0h	<p>This bit controls the action taken by the I2C module when a debugger breakpoint is encountered.</p> <p>0h (R/W) = When I2C module is master:</p> <p>If SCL is low when the breakpoint occurs, the I2C module stops immediately and keeps driving SCL low, whether the I2C module is the transmitter or the receiver. If SCL is high, the I2C module waits until SCL becomes low and then stops.</p> <p>When I2C module is slave:</p> <p>A breakpoint forces the I2C module to stop when the current transmission/reception is complete.</p> <p>1h (R/W) = The I2C module runs free</p> <p>that is, it continues to operate when a breakpoint occurs.</p>
13	STT	R/W	0h	<p>START condition bit (only applicable when the I2C module is a master). The RM, STT, and STP bits determine when the I2C module starts and stops data transmissions (see Table 9-6). Note that the STT and STP bits can be used to terminate the repeat mode, and that this bit is not writable when IRS = 0.</p> <p>0h (R/W) = In the master mode, STT is automatically cleared after the START condition has been generated.</p> <p>1h (R/W) = In the master mode, setting STT to 1 causes the I2C module to generate a START condition on the I2C-bus</p>
12	RESERVED	R	0h	Reserved

Table 18-15. I2CMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	STP	R/W	0h	<p>STOP condition bit (only applicable when the I2C module is a master).</p> <p>In the master mode, the RM, STT, and STP bits determine when the I2C module starts and stops data transmissions.</p> <p>Note that the STT and STP bits can be used to terminate the repeat mode, and that this bit is not writable when IRS=0. When in non-repeat mode, at least one byte must be transferred before a stop condition can be generated. The I2C module delays clearing of this bit until after the I2CSTR[SCD] bit is set. To avoid disrupting the I2C state machine, the user must wait until this bit is clear before initiating a new message.</p> <p>0h (R/W) = STP is automatically cleared after the STOP condition has been generated</p> <p>1h (R/W) = STP has been set by the device to generate a STOP condition when the internal data counter of the I2C module counts down to 0.</p>
10	MST	R/W	0h	<p>Master mode bit.</p> <p>MST determines whether the I2C module is in the slave mode or the master mode. MST is automatically changed from 1 to 0 when the I2C master generates a STOP condition</p> <p>0h (R/W) = Slave mode. The I2C module is a slave and receives the serial clock from the master.</p> <p>1h (R/W) = Master mode. The I2C module is a master and generates the serial clock on the SCL pin.</p>
9	TRX	R/W	0h	<p>Transmitter mode bit.</p> <p>When relevant, TRX selects whether the I2C module is in the transmitter mode or the receiver mode.</p> <p>0h (R/W) = Receiver mode. The I2C module is a receiver and receives data on the SDA pin.</p> <p>1h (R/W) = Transmitter mode. The I2C module is a transmitter and transmits data on the SDA pin.</p>
8	XA	R/W	0h	<p>Expanded address enable bit.</p> <p>0h (R/W) = 7-bit addressing mode (normal address mode). The I2C module transmits 7-bit slave addresses (from bits 6-0 of I2CSAR), and its own slave address has 7 bits (bits 6-0 of I2COAR).</p> <p>1h (R/W) = 10-bit addressing mode (expanded address mode). The I2C module transmits 10-bit slave addresses (from bits 9-0 of I2CSAR), and its own slave address has 10 bits (bits 9-0 of I2COAR).</p>
7	RM	R/W	0h	<p>Repeat mode bit (only applicable when the I2C module is a master-transmitter).</p> <p>The RM, STT, and STP bits determine when the I2C module starts and stops data transmissions</p> <p>0h (R/W) = Nonrepeat mode. The value in the data count register (I2CCNT) determines how many bytes are received/transmitted by the I2C module.</p> <p>1h (R/W) = Repeat mode. A data byte is transmitted each time the I2CDXR register is written to (or until the transmit FIFO is empty when in FIFO mode) until the STP bit is manually set. The value of I2CCNT is ignored. The ARDY bit/interrupt can be used to determine when the I2CDXR (or FIFO) is ready for more data, or when the data has all been sent and the CPU is allowed to write to the STP bit.</p>

Table 18-15. I2CMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DLB	R/W	0h	<p>Digital loopback mode bit.</p> <p>0h (R/W) = Digital loopback mode is disabled.</p> <p>1h (R/W) = Digital loopback mode is enabled. For proper operation in this mode, the MST bit must be 1.</p> <p>In the digital loopback mode, data transmitted out of I2CDXR is received in I2CDRR after n device cycles by an internal path, where: n = ((I2C input clock frequency/module clock frequency) ? 8)</p> <p>The transmit clock is also the receive clock. The address transmitted on the SDA pin is the address in I2COAR.</p> <p>Note: The free data format (FDF = 1) is not supported in the digital loopback mode.</p>
5	IRS	R/W	0h	<p>I2C module reset bit.</p> <p>0h (R/W) = The I2C module is in reset/disabled. When this bit is cleared to 0, all status bits (in I2CSTR) are set to their default values.</p> <p>1h (R/W) = The I2C module is enabled. This has the effect of releasing the I2C bus if the I2C peripheral is holding it.</p>
4	STB	R/W	0h	<p>START byte mode bit. This bit is only applicable when the I2C module is a master. As described in version 2.1 of the Philips Semiconductors I2C-bus specification, the START byte can be used to help a slave that needs extra time to detect a START condition. When the I2C module is a slave, it ignores a START byte from a master, regardless of the value of the STB bit.</p> <p>0h (R/W) = The I2C module is not in the START byte mode.</p> <p>1h (R/W) = The I2C module is in the START byte mode. When you set the START condition bit (STT), the I2C module begins the transfer with more than just a START condition. Specifically, it generates:</p> <ul style="list-style-type: none"> 1. A START condition 2. A START byte (0000 0001b) 3. A dummy acknowledge clock pulse 4. A repeated START condition <p>Then, as normal, the I2C module sends the slave address that is in I2CSAR.</p>
3	FDF	R/W	0h	<p>Free data format mode bit.</p> <p>0h (R/W) = Free data format mode is disabled. Transfers use the 7-/10-bit addressing format selected by the XA bit.</p> <p>1h (R/W) = Free data format mode is enabled. Transfers have the free data (no address) format described in Section 9.2.5.</p> <p>The free data format is not supported in the digital loopback mode (DLB=1).</p>

Table 18-15. I2CMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BC	R/W	0h	<p>Bit count bits.</p> <p>BC defines the number of bits (1 to 8) in the next data byte that is to be received or transmitted by the I2C module. The number of bits selected with BC must match the data size of the other device. Notice that when BC = 000b, a data byte has 8 bits. BC does not affect address bytes, which always have 8 bits.</p> <p>Note: If the bit count is less than 8, receive data is right-justified in I2CDRR(7-0), and the other bits of I2CDRR(7-0) are undefined. Also, transmit data written to I2CDXR must be right-justified</p> <p>0h (R/W) = 8 bits per data byte 1h (R/W) = 1 bit per data byte 2h (R/W) = 2 bits per data byte 3h (R/W) = 3 bits per data byte 4h (R/W) = 4 bits per data byte 5h (R/W) = 5 bits per data byte 6h (R/W) = 6 bits per data byte 7h (R/W) = 7 bits per data byte</p>

18.5.2.11 I2CISRC Register (offset = Ah) [reset = 0h]

I2CISRC is shown in [Figure 18-24](#) and described in [Table 18-16](#).

I2C Interrupt Source

Figure 18-24. I2CISRC Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				INTCODE			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

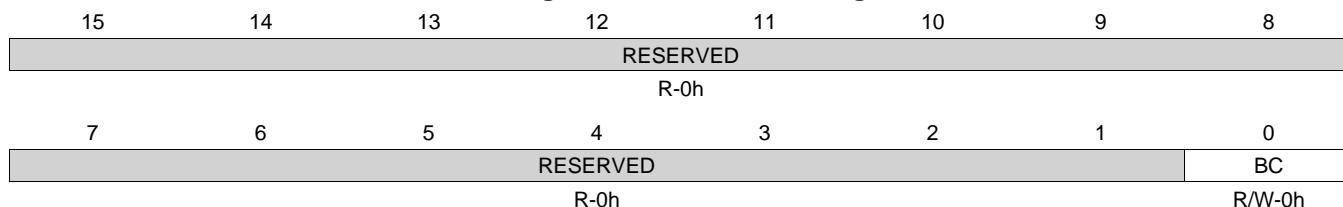
Table 18-16. I2CISRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-8	RESERVED	R/W	0h	Reserved
7-3	RESERVED	R	0h	Reserved
2-0	INTCODE	R	0h	<p>Interrupt code bits.</p> <p>The binary code in INTCODE indicates the event that generated an I2C interrupt.</p> <p>A CPU read will clear this field. If another lower priority interrupt is pending and enabled, the value corresponding to that interrupt will then be loaded. Otherwise, the value will stay cleared.</p> <p>In the case of an arbitration lost, a no-acknowledgment condition detected, or a stop condition detected, a CPU read will also clear the associated interrupt flag bit in the I2CSTR register.</p> <p>Emulator reads will not affect the state of this field or of the status bits in the I2CSTR register.</p> <p>0h (R/W) = None 1h (R/W) = Arbitration lost 2h (R/W) = No-acknowledgment condition detected 3h (R/W) = Registers ready to be accessed 4h (R/W) = Receive data ready 5h (R/W) = Transmit data ready 6h (R/W) = Stop condition detected 7h (R/W) = Addressed as slave</p>

18.5.2.12 I2CEMDR Register (offset = Bh) [reset = 0h]

I2CEMDR is shown in [Figure 18-25](#) and described in [Table 18-17](#).

I2C Extended Mode

Figure 18-25. I2CEMDR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

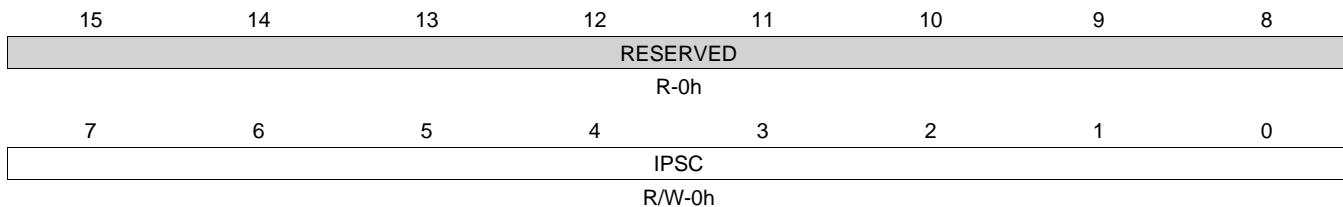
Table 18-17. I2CEMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	BC	R/W	0h	Backwards compatibility mode. This bit affects the timing of the transmit status bits (XRDY and XSMT) in the I2CSTR register when in slave transmitter mode. 0h (R/W) = See Figure 9-17 for details. 1h (R/W) = See Figure 9-17 for details.

18.5.2.13 I2CPSC Register (offset = Ch) [reset = 0h]

I2CPSC is shown in [Figure 18-26](#) and described in [Table 18-18](#).

I2C Prescaler

Figure 18-26. I2CPSC Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-18. I2CPSC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	IPSC	R/W	0h	<p>I2C prescaler divide-down value.</p> <p>IPSC determines how much the CPU clock is divided to create the module clock of the I2C module:</p> $\text{module clock frequency} = \text{I2C input clock frequency}/(\text{IPSC} + 1)$ <p>Note: IPSC must be initialized while the I2C module is in reset (IRS = 0 in I2CMDR).</p>

18.5.2.14 I2CFFTX Register (offset = 20h) [reset = 0h]

I2CFFTX is shown in [Figure 18-27](#) and described in [Table 18-19](#).

I2C FIFO Transmit

Figure 18-27. I2CFFTX Register

15	14	13	12	11	10	9	8
RESERVED	I2CFFEN	TXFFRST			TXFFST		
R-0h	R/W-0h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
TXFFINT	TXFFINTCLR	TXFFIENA			TXFFIL		
R-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-19. I2CFFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	I2CFFEN	R/W	0h	I2C FIFO mode enable bit. This bit must be enabled for either the transmit or the receive FIFO to operate correctly. 0h (R/W) = Disable the I2C FIFO mode. 1h (R/W) = Enable the I2C FIFO mode.
13	TXFFRST	R/W	0h	Transmit FIFO Reset 0h (R/W) = Reset the transmit FIFO pointer to 0000 and hold the transmit FIFO in the reset state. 1h (R/W) = Enable the transmit FIFO operation.
12-8	TXFFST	R	0h	Contains the status of the transmit FIFO: 00xx Transmit FIFO contains xxx bytes. 00000 Transmit FIFO is empty. Note: Since these bits are reset to zero, the transmit FIFO interrupt flag will be set when the transmit FIFO operation is enabled and the I2C is taken out of reset. This will generate a transmit FIFO interrupt if enabled. To avoid any detrimental effects from this, write a one to the TXFFINTCLR once the transmit FIFO operation is enabled and the I2C is taken out of reset.
7	TXFFINT	R	0h	Transmit FIFO interrupt flag. This bit cleared by a CPU write of a 1 to the TXFFINTCLR bit. If the TXFFIENA bit is set, this bit will generate an interrupt when it is set. 0h (R/W) = Transmit FIFO interrupt condition has not occurred. 1h (R/W) = Transmit FIFO interrupt condition has occurred.
6	TXFFINTCLR	R/W	0h	Transmit FIFO Interrupt Flag Clear 0h (R/W) = Writes of zeros have no effect. Reads return a 0. 1h (R/W) = Writing a 1 to this bit clears the TXFFINT flag.
5	TXFFIENA	R/W	0h	Transmit FIFO Interrupt Enable 0h (R/W) = Disabled. TXFFINT flag does not generate an interrupt when set. 1h (R/W) = Enabled. TXFFINT flag does generate an interrupt when set.

Table 18-19. I2CFFTX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	TXFFIL	R/W	0h	<p>Transmit FIFO interrupt level.</p> <p>These bits set the status level that will set the transmit interrupt flag. When the TXFFST4-0 bits reach a value equal to or less than these bits, the TXFFINT flag will be set. This will generate an interrupt if the TXFFIENA bit is set. Because the I2C on these devices has a 4-level transmit FIFO, these bits cannot be configured for an interrupt of more than 4 FIFO levels. TXFFIL4 and TXFFIL3 are tied to zero.</p>

18.5.2.15 I2CFFRX Register (offset = 21h) [reset = 0h]

I2CFFRX is shown in [Figure 18-28](#) and described in [Table 18-20](#).

I2C FIFO Receive

Figure 18-28. I2CFFRX Register

15	14	13	12	11	10	9	8
RESERVED	RXFFRST			RXFFST			
R-0h	R/W-0h			R-0h			
7	6	5	4	3	2	1	0
RXFFINT	RXFFINTCLR	RXFFIENA		RXFFIL			
R-0h	R/W-0h	R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 18-20. I2CFFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RXFFRST	R/W	0h	I2C receive FIFO reset bit 0h (R/W) = Reset the receive FIFO pointer to 0000 and hold the receive FIFO in the reset state. 1h (R/W) = Enable the receive FIFO operation.
12-8	RXFFST	R	0h	Contains the status of the receive FIFO: 00xx Receive FIFO contains xxx bytes 00000 Receive FIFO is empty.
7	RXFFINT	R	0h	Receive FIFO interrupt flag. This bit cleared by a CPU write of a 1 to the RXFFINTCLR bit. If the RXFFIENA bit is set, this bit will generate an interrupt when it is set 0h (R/W) = Receive FIFO interrupt condition has not occurred. 1h (R/W) = Receive FIFO interrupt condition has occurred.
6	RXFFINTCLR	R/W	0h	Receive FIFO interrupt flag clear bit. 0h (R/W) = Writes of zeros have no effect. Reads return a zero. 1h (R/W) = Writing a 1 to this bit clears the RXFFINT flag.
5	RXFFIENA	R/W	0h	Receive FIFO interrupt enable bit. 0h (R/W) = Disabled. RXFFINT flag does not generate an interrupt when set. 1h (R/W) = Enabled. RXFFINT flag does generate an interrupt when set.
4-0	RXFFIL	R/W	0h	Receive FIFO interrupt level. These bits set the status level that will set the receive interrupt flag. When the RXFFST4-0 bits reach a value equal to or greater than these bits, the RXFFINT flag is set. This will generate an interrupt if the RXFFIENA bit is set. Note: Since these bits are reset to zero, the receive FIFO interrupt flag will be set if the receive FIFO operation is enabled and the I2C is taken out of reset. This will generate a receive FIFO interrupt if enabled. To avoid this, modify these bits on the same instruction as or prior to setting the RXFFRST bit. Because the I2C on these devices has a 4-level receive FIFO, these bits cannot be configured for an interrupt of more than 4 FIFO levels. RXFFIL4 and RXFFIL3 are tied to zero.

Multichannel Buffered Serial Port (McBSP)

This document describes the multichannel buffered serial port (McBSP) of the F2837D device.

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19.1 Overview

This device provides up to two high-speed multichannel buffered serial ports (McBSPs) that allow direct interface to codecs and other devices in a system. The McBSP consists of a data-flow path and a control path connected to external devices by six pins as shown in [Figure 19-1](#).

Data is communicated to devices interfaced with the McBSP via the data transmit (DX) pin for transmission and via the data receive (DR) pin for reception. Control information in the form of clocking and frame synchronization is communicated via the following pins: CLKX (transmit clock), CLKR (receive clock), FSX (transmit frame synchronization), and FSR (receive frame synchronization).

The CPU and the DMA controller communicate with the McBSP through 16-bit-wide registers accessible via the internal peripheral bus. The CPU or the DMA controller writes the data to be transmitted to the data transmit registers (DXR1, DXR2). Data written to the DXRs is shifted out to DX via the transmit shift registers (XSR1, XSR2). Similarly, receive data on the DR pin is shifted into the receive shift registers (RSR1, RSR2) and copied into the receive buffer registers (RBR1, RBR2). The contents of the RBRs is then copied to the DRRs, which can be read by the CPU or the DMA controller. This allows simultaneous movement of internal and external data communications.

DRR2, RBR2, RSR2, DXR2, and XSR2 are not used (written, read, or shifted) if the serial word length is 8 bits, 12 bits, or 16 bits. For larger word lengths, these registers are needed to hold the most significant bits.

The frame and clock loop-back is implemented at chip level to enable CLKX and FSX to drive CLKR and FSR. If the loop-back is enabled, the CLKR and FSR get their signals from the CLKX and FSX pads; instead of the CLKR and FSR pins.

19.1.1 Features of the McBSPs

The McBSPs feature:

- Full-duplex communication
- Double-buffered transmission and triple-buffered reception, allowing a continuous data stream
- Independent clocking and framing for reception and transmission
- The capability to send interrupts to the CPU and to send DMA events to the DMA controller
- 128 channels for transmission and reception
- Multichannel selection modes that enable or disable block transfers in each of the channels
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices
- Support for external generation of clock signals and frame-synchronization signals
- A programmable sample rate generator for internal generation and control of clock signals and frame-synchronization signals
- Programmable polarity for frame-synchronization pulses and clock signals
- Direct interface to:
 - T1/E1 framers
 - IOM-2 compliant devices
 - AC97-compliant devices (the necessary multiphase frame capability is provided)
 - I2S compliant devices
 - SPI devices
- A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits

NOTE: A value of the chosen data size is referred to as a *serial word* or *word* throughout the McBSP documentation. Elsewhere, *word* is used to describe a 16-bit value.

- μ -law and A-law companding
- The option of transmitting/receiving 8-bit data with the LSB first
- Status bits for flagging exception/error conditions

- ABIS mode is not supported.

19.1.2 McBSP Pins/Signals

Table 19-1 describes the McBSP interface pins and some internal signals.

Table 19-1. McBSP Interface Pins/Signals

McBSP-A Pin	McBSP-B Pin	Type	Description
MCLKRA	MCLKRB	I/O	Supplying or reflecting the receive clock; supplying the input clock of the sample rate generator
MCLKXA	MCLKXB	I/O	Supplying or reflecting the transmit clock; supplying the input clock of the sample rate generator
MDRA	MDRB	I	Serial data receive pin
MDXA	MDXB	O	Serial data transmit pin
MFSRA	MFSRB	I/O	Supplying or reflecting the receive frame-sync signal; controlling sample rate generator synchronization for the case when GSYNC = 1 (see Section 19.3.3)
MFSXA	MFSXB	I/O	Supplying or reflecting the transmit frame-sync signal

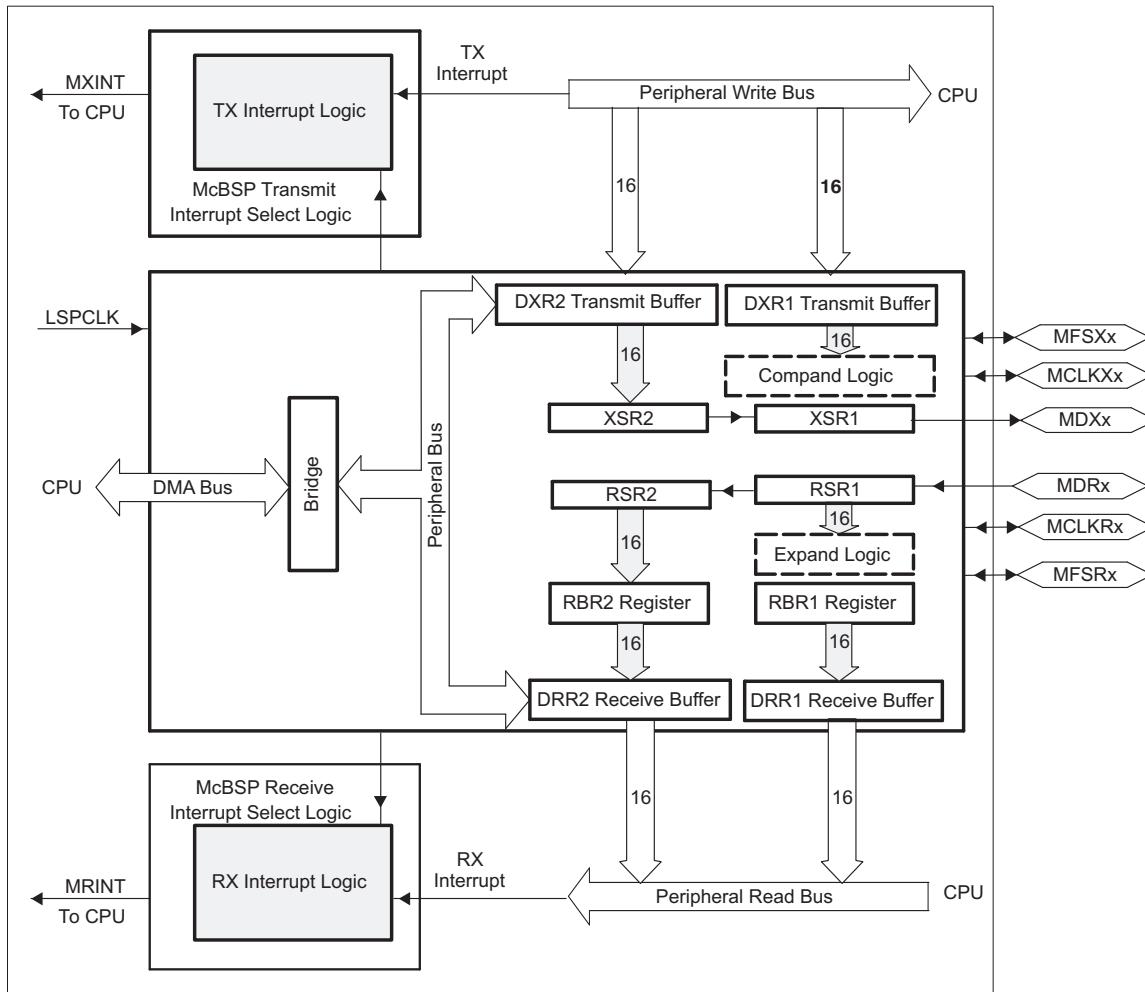
CPU Interrupt Signals	
MRINT	Receive interrupt to CPU
MXINT	Transmit interrupt to CPU

DMA Events	
REVT	Receive synchronization event to DMA
XEVN	Transmit synchronization event to DMA

19.1.2.1 McBSP Generic Block Diagram

The McBSP consists of a data-flow path and a control path connected to external devices by six pins as shown in [Figure 19-1](#). The figure and the text in this section use generic pin names.

Figure 19-1. Conceptual Block Diagram of the McBSP



A Not available in all devices. See the device-specific data sheet

19.2 McBSP Operation

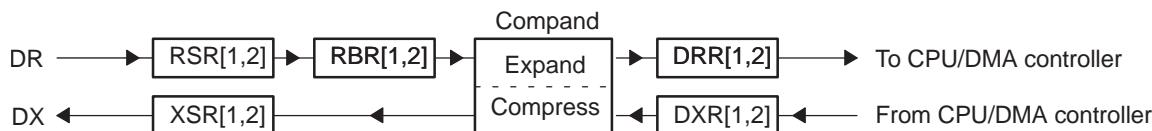
This section addresses the following topics:

- Data transfer process
- Companding (compressing and expanding) data
- Clocking and framing data
- Frame phases
- McBSP reception
- McBSP transmission
- Interrupts and DMA events generated by McBSPs

19.2.1 Data Transfer Process of McBSPs

Figure 19-2 shows a diagram of the McBSP data transfer paths. The McBSP receive operation is triple-buffered, and transmit operation is double-buffered. The use of registers varies, depending on whether the defined length of each serial word is 16 bits.

Figure 19-2. McBSP Data Transfer Paths



19.2.1.1 Data Transfer Process for Word Length of 8, 12, or 16 Bits

If the word length is 16 bits or smaller, only one 16-bit register is needed at each stage of the data transfer paths. The registers DRR2, RBR2, RSR2, DXR2, and XSR2 are not used (written, read, or shifted).

Receive data arrives on the DR pin and is shifted into receive shift register 1 (RSR1). Once a full word is received, the content of RSR1 is copied to receive buffer register 1 (RBR1) if RBR1 is not full with previous data. RBR1 is then copied to data receive register 1 (DRR1), unless the previous content of DRR1 has not been read by the CPU or the DMA controller. If the companding feature of the McBSP is implemented, the required word length is 8 bits and receive data is expanded into the appropriate format before being passed from RBR1 to DRR1. For more details about reception, see [Section 19.2.5](#).

Transmit data is written by the CPU or the DMA controller to data transmit register 1 (DXR1). If there is no previous data in transmit shift register (XSR1), the value in DXR1 is copied to XSR1; otherwise, DXR1 is copied to XSR1 when the last bit of the previous data is shifted out on the DX pin. If selected, the companding module compresses 16-bit data into the appropriate 8-bit format before passing it to XSR1. After transmit frame synchronization, the transmitter begins shifting bits from XSR1 to the DX pin. For more details about transmission, see [Section 19.2.6](#).

19.2.1.2 Data Transfer Process for Word Length of 20, 24, or 32 Bits

If the word length is larger than 16 bits, two 16-bit registers are needed at each stage of the data transfer paths. The registers DRR2, RBR2, RSR2, DXR2, and XSR2 are needed to hold the most significant bits.

Receive data arrives on the DR pin and is shifted first into RSR2 and then into RSR1. Once the full word is received, the contents of RSR2 and RSR1 are copied to RBR2 and RBR1, respectively, if RBR1 is not full. Then the contents of RBR2 and RBR1 are copied to DRR2 and DRR1, respectively, unless the previous content of DRR1 has not been read by the CPU or the DMA controller. The CPU or the DMA controller must read data from DRR2 first and then from DRR1. When DRR1 is read, the next RBR-to-DRR copy occurs. For more details about reception, see [Section 19.2.5](#).

For transmission, the CPU or the DMA controller must write data to DXR2 first and then to DXR1. When new data arrives in DXR1, if there is no previous data in XSR1, the contents of DXR2 and DXR1 are copied to XSR2 and XSR1, respectively; otherwise, the contents of the DXRs are copied to the XSRs when the last bit of the previous data is shifted out on the DX pin. After transmit frame synchronization, the transmitter begins shifting bits from the XSRs to the DX pin. For more details about transmission, see [Section 19.2.6](#).

19.2.2 Companding (Compressing and Expanding) Data

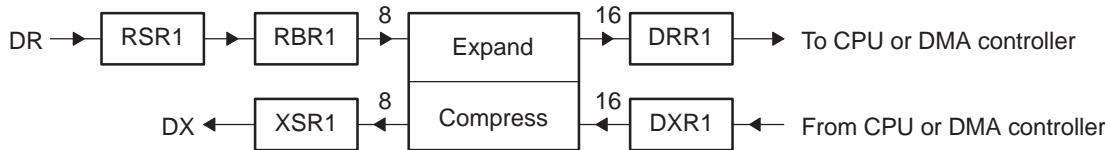
Companding (COMpressing and exPANDING) hardware allows compression and expansion of data in either μ -law or A-law format. The companding standard employed in the United States and Japan is μ -law. The European companding standard is referred to as A-law. The specifications for μ -law and A-law log PCM are part of the CCITT G.711 recommendation.

A-law and μ -law allow 13 bits and 14 bits of dynamic range, respectively. Any values outside this range are set to the most positive or most negative value. Thus, for companding to work best, the data transferred to and from the McBSP via the CPU or DMA controller must be at least 16 bits wide.

The μ -law and A-law formats both encode data into 8-bit code words. Companded data is always 8 bits wide; the appropriate word length bits (RWDLEN1, RWDLEN2, XWDLEN1, XWDLEN2) must therefore be set to 0, indicating an 8-bit wide serial data stream. If companding is enabled and either of the frame phases does not have an 8-bit word length, companding continues as if the word length is 8 bits.

Figure 19-3 illustrates the companding processes. When companding is chosen for the transmitter, compression occurs during the process of copying data from DXR1 to XSR1. The transmit data is encoded according to the specified companding law (A-law or μ -law). When companding is chosen for the receiver, expansion occurs during the process of copying data from RBR1 to DRR1. The receive data is decoded to twos-complement format.

Figure 19-3. Companding Processes

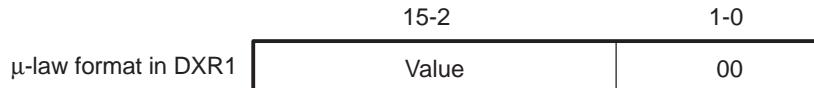


19.2.2.1 Companding Formats

For reception, the 8-bit compressed data in RBR1 is expanded to left-justified 16-bit data in DRR1. The receive sign-extension and justification mode specified in RJUST is ignored when companding is used.

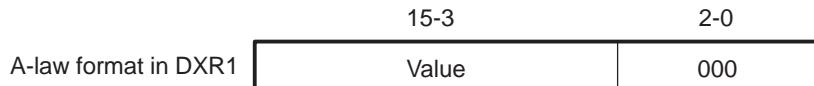
For transmission using μ -law compression, the 14 data bits must be left-justified in DXR1 and that the remaining two low-order bits are filled with 0s as shown in Figure 19-4.

Figure 19-4. μ -Law Transmit Data Companding Format



For transmission using A-law compression, the 13 data bits must be left-justified in DXR1, with the remaining three low-order bits filled with 0s as shown in Figure 19-5.

Figure 19-5. A-Law Transmit Data Companding Format



19.2.2.2 Capability to Compand Internal Data

If the McBSP is otherwise unused (the serial port transmit and receive sections are reset), the companding hardware can compand internal data. This can be used to:

- Convert linear to the appropriate μ -law or A-law format
- Convert μ -law or A-law to the linear format
- Observe the quantization effects in companding by transmitting linear data and compressing and re-expanding this data. This is useful only if both XCOMPAND and RCOMPAND enable the same companding format.

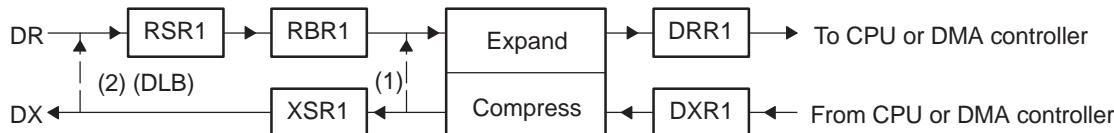
Figure 19-6 shows two methods by which the McBSP can compand internal data. Data paths for these two methods are used to indicate:

- When both the transmit and receive sections of the serial port are reset, DRR1 and DXR1 are connected internally through the companding logic. Values from DXR1 are compressed, as selected by XCOMPAND, and then expanded, as selected by RCOMPAND. RRDY and XRDY bits are not set. However, data is available in DRR1 within four CPU clocks after being written to DXR1.

The advantage of this method is its speed. The disadvantage is that there is no synchronization available to the CPU and DMA to control the flow. DRR1 and DXR1 are internally connected if the (X/R)COMPAND bits are set to 10b or 11b (compand using μ -law or A-law).

- The McBSP is enabled in digital loopback mode with companding appropriately enabled by RCOMPAND and XCOMPAND. Receive and transmit interrupts (RINT when RINTM = 0 and XINT when XINTM = 0) or synchronization events (REVT and XEV) allow synchronization of the CPU or DMA to these conversions, respectively. Here, the time for this companding depends on the serial bit rate selected.

Figure 19-6. Two Methods by Which the McBSP Can Compand Internal Data



19.2.2.3 Reversing Bit Order: Option to Transfer LSB First

Generally, the McBSP transmits or receives all data with the most significant bit (MSB) first. However, certain 8-bit data protocols (that do not use companded data) require the least significant bit (LSB) to be transferred first. If you set XCOMPAND = 01b in XCR2, the bit ordering of 8-bit words is reversed (LSB first) before being sent from the serial port. If you set RCOMPAND = 01b in RCR2, the bit ordering of 8-bit words is reversed during reception. Similar to companding, this feature is enabled only if the appropriate word length bits are set to 0, indicating that 8-bit words are to be transferred serially. If either phase of the frame does not have an 8-bit word length, the McBSP assumes the word length is eight bits, and LSB-first ordering is done.

19.2.3 Clocking and Framing Data

This section explains basic concepts and terminology important for understanding how McBSP data transfers are timed and delimited.

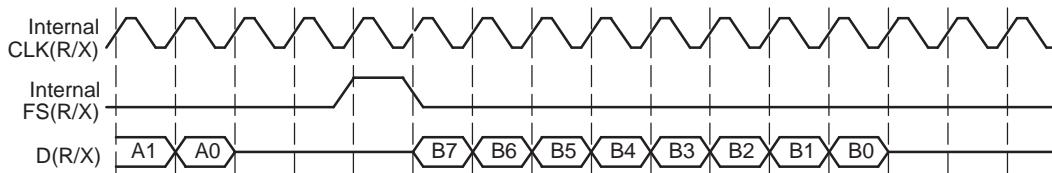
19.2.3.1 Clocking

Data is shifted one bit at a time from the DR pin to the RSR(s) or from the XSR(s) to the DX pin. The time for each bit transfer is controlled by the rising or falling edge of a clock signal.

The receive clock signal (CLKR) controls bit transfers from the DR pin to the RSR(s). The transmit clock signal (CLKX) controls bit transfers from the XSR(s) to the DX pin. CLKR or CLKX can be derived from a pin at the boundary of the McBSP or derived from inside the McBSP. The polarities of CLKR and CLKX are programmable.

In the example in Figure 19-7, the clock signal controls the timing of each bit transfer on the pin.

Figure 19-7. Example - Clock Signal Control of Bit Transfer Timing



NOTE: The McBSP cannot operate at a frequency faster than $\frac{1}{2}$ the LSPCLK frequency. When driving CLKX or CLKR at the pin, choose an appropriate input clock frequency. When using the internal sample rate generator for CLKX and/or CLKR, choose an appropriate input clock frequency and divide down value (CLKDV) (i.e., be certain that $CLKX$ or $CLKR \leq LSPCLK/2$).

19.2.3.2 Serial Words

Bits traveling between a shift register (RSR or XSR) and a data pin (DR or DX) are transferred in a group called a serial word. You can define how many bits are in a word.

Bits coming in on the DR pin are held in RSR until RSR holds a full serial word. Only then is the word passed to RBR (and ultimately to the DRR).

During transmission, XSR does not accept new data from DXR until a full serial word has been passed from XSR to the DX pin.

In the example in [Figure 19-7](#), an 8-bit word size was defined (see bits 7 through 0 of word B being transferred).

19.2.3.3 Frames and Frame Synchronization

One or more words are transferred in a group called a frame. You can define how many words are in a frame.

All of the words in a frame are sent in a continuous stream. However, there can be pauses between frame transfers. The McBSP uses frame-synchronization signals to determine when each frame is received/transmitted. When a pulse occurs on a frame-synchronization signal, the McBSP begins receiving/transmitting a frame of data. When the next pulse occurs, the McBSP receives/transmits the next frame, and so on.

Pulses on the receive frame-synchronization (FSR) signal initiate frame transfers on DR. Pulses on the transmit frame-sync (FSX) signal initiate frame transfers on DX. FSR or FSX can be derived from a pin at the boundary of the McBSP or derived from inside the McBSP.

In the example in [Figure 19-7](#), a one-word frame is transferred when a frame-synchronization pulse occurs.

In McBSP operation, the inactive-to-active transition of the frame-synchronization signal indicates the start of the next frame. For this reason, the frame-synchronization signal may be high for an arbitrary number of clock cycles. Only after the signal is recognized to have gone inactive, and then active again, does the next frame synchronization occur.

19.2.3.4 Generating Transmit and Receive Interrupts

The McBSP can send receive and transmit interrupts to the CPU to indicate specific events in the McBSP. To facilitate detection of frame synchronization, these interrupts can be sent in response to frame-synchronization pulses. Set the appropriate interrupt mode bits to 10b (for reception, RINTM = 10b; for transmission, XINTM = 10b).

19.2.3.4.1 Detecting Frame-Synchronization Pulses, Even in Reset State

Unlike other serial port interrupt modes, this mode can operate while the associated portion of the serial port is in reset (such as activating RINT when the receiver is in reset). In this case, FSRM/FSXM and FSRP/FSXP still select the appropriate source and polarity of frame synchronization. Thus, even when the serial port is in the reset state, these signals are synchronized to the CPU clock and then sent to the CPU in the form of RINT and XINT at the point at which they feed the receiver and transmitter of the serial port. Consequently, a new frame-synchronization pulse can be detected, and after this occurs the CPU can take the serial port out of reset safely.

19.2.3.5 Ignoring Frame-Synchronization Pulses

The McBSP can be configured to ignore transmit and/or receive frame-synchronization pulses. To have the receiver or transmitter recognize frame-synchronization pulses, clear the appropriate frame-synchronization ignore bit (RFIG = 0 for the receiver, XFIG = 0 for the transmitter). To have the receiver or transmitter ignore frame-synchronization pulses until the desired frame length or number of words is reached, set the appropriate frame-synchronization ignore bit (RFIG = 1 for the receiver, XFIG = 1 for the transmitter). For more details on unexpected frame-synchronization pulses, see one of the following topics:

- *Unexpected Receive Frame-Synchronization Pulse* (see [Section 19.4.3](#))
- *Unexpected Transmit Frame-Synchronization Pulse* (see [Section 19.4.6](#))

You can also use the frame-synchronization ignore function for data packing (for more details, see [Section 19.10.2](#)).

19.2.3.6 Frame Frequency

The frame frequency is determined by the period between frame-synchronization pulses and is defined as shown by Example 1.

Example 1: McBSP Frame Frequency

$$\text{Frame Frequency} = \frac{\text{Clock Frequency}}{\text{Number of Clock Cycles Between Frame-Sync Pulses}}$$

The frame frequency can be increased by decreasing the time between frame-synchronization pulses (limited only by the number of bits per frame). As the frame transmit frequency increases, the inactivity period between the data packets for adjacent transfers decreases to zero.

19.2.3.7 Maximum Frame Frequency

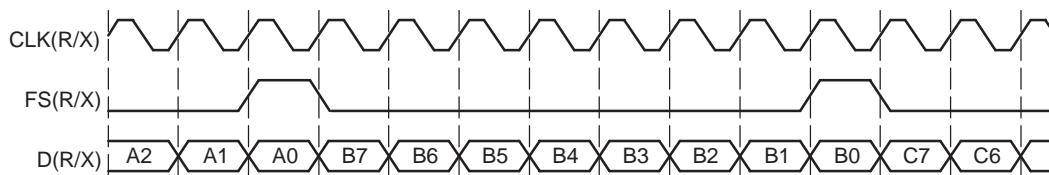
The minimum number of clock cycles between frame synchronization pulses is equal to the number of bits transferred per frame. The maximum frame frequency is defined as shown by Example 2.

Example 2: McBSP Maximum Frame Frequency

$$\text{Maximum Frame Frequency} = \frac{\text{Clock Frequency}}{\text{Number of Bits Per Frame}}$$

[Figure 19-8](#) shows the McBSP operating at maximum packet frequency. At maximum packet frequency, the data bits in consecutive packets are transmitted contiguously with no inactivity between bits.

Figure 19-8. McBSP Operating at Maximum Packet Frequency



If there is a 1-bit data delay as shown in this figure, the frame-synchronization pulse overlaps the last bit transmitted in the previous frame. Effectively, this permits a continuous stream of data, making frame-synchronization pulses redundant. Theoretically, only an initial frame-synchronization pulse is required to initiate a multipacket transfer.

The McBSP supports operation of the serial port in this fashion by ignoring the successive frame-synchronization pulses. Data is clocked into the receiver or clocked out of the transmitter during every clock cycle.

NOTE: For XDATDLY = 0 (0-bit data delay), the first bit of data is transmitted asynchronously to the internal transmit clock signal (CLKX). For more details, see [Section 19.8.12](#).

19.2.4 Frame Phases

The McBSP allows you to configure each frame to contain one or two phases. The number of words and the number of bits per word can be specified differently for each of the two phases of a frame, allowing greater flexibility in structuring data transfers. For example, you might define a frame as consisting of one phase containing two words of 16 bits each, followed by a second phase consisting of 10 words of 8 bits each. This configuration permits you to compose frames for custom applications or, in general, to maximize the efficiency of data transfers.

19.2.4.1 Number of Phases, Words, and Bits Per Frame

[Table 19-2](#) shows which bit-fields in the receive control registers (RCR1 and RCR2) and in the transmit control registers (XCR1 and XCR2) determine the number of phases per frame, the number of words per frame, and number of bits per word for each phase, for the receiver and transmitter. The maximum number of words per frame is 128 for a single-phase frame and 256 for a dual-phase frame. The number of bits per word can be 8, 12, 16, 20, 24, or 32 bits.

Table 19-2. Register Bits That Determine the Number of Phases, Words, and Bits

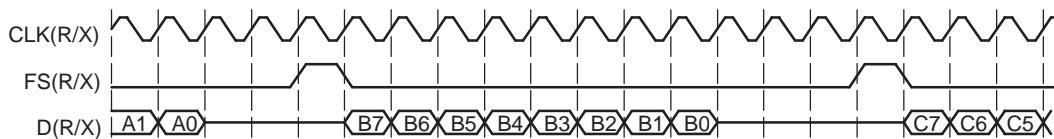
Operation	Number of Phases	Words per Frame Set With	Bits per Word Set With
Reception	1 (RPHASE = 0)	RFRLEN1	RWDLEN1
Reception	2 (RPHASE = 1)	RFRLEN1 and RFRLEN2	RWDLEN1 for phase 1 RWDLEN2 for phase 2
Transmission	1 (XPHASE = 0)	XFRLEN1	XWDLEN1
Transmission	2 (XPHASE = 1)	XFRLEN1 and XFRLEN2	XWDLEN1 for phase 1 XWDLEN2 for phase 2

19.2.4.2 Single-Phase Frame Example

[Figure 19-9](#) shows an example of a single-phase data frame containing one 8-bit word. Because the transfer is configured for one data bit delay, the data on the DX and DR pins are available one clock cycle after FS(R/X) goes active. The figure makes the following assumptions:

- (R/X)PHASE = 0: Single-phase frame
- (R/X)FRLLEN1 = 0b: 1 word per frame
- (R/X)WDLEN1 = 000b: 8-bit word length
- (R/X)FRLLEN2 and (R/X)WDLEN2 are ignored
- CLK(X/R)P = 0: Receive data clocked on falling edge; transmit data clocked on rising edge
- FS(R/X)P = 0: Active-high frame-synchronization signals
- (R/X)DATDLY = 01b: 1-bit data delay

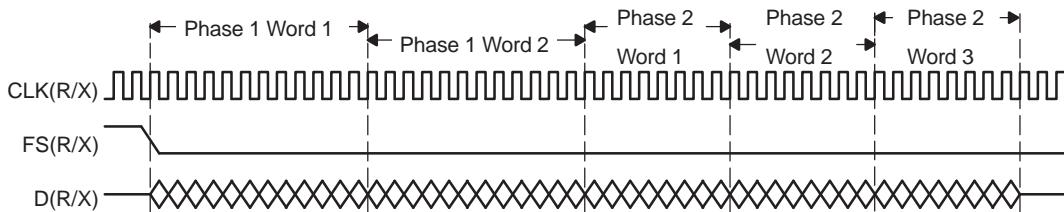
Figure 19-9. Single-Phase Frame for a McBSP Data Transfer



19.2.4.3 Dual-Phase Frame Example

[Figure 19-10](#) shows an example of a frame where the first phase consists of two words of 12 bits each, followed by a second phase of three words of 8 bits each. The entire bit stream in the frame is contiguous. There are no gaps either between words or between phases.

Figure 19-10. Dual-Phase Frame for a McBSP Data Transfer

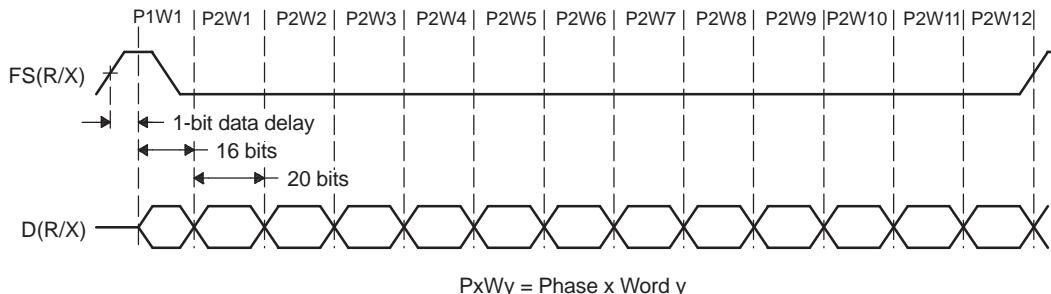


A XRDY gets asserted once per phase. So, if there are 2 phases, XRDY gets asserted twice (once per phase).

19.2.4.4 Implementing the AC97 Standard With a Dual-Phase Frame

Figure 19-11 shows an example of the Audio Codec '97 (AC97) standard, which uses the dual-phase frame feature. Notice that words, not individual bits, are shown on the D(R/X) signal. The first phase (P1) consists of a single 16-bit word. The second phase (P2) consists of twelve 20-bit words. The phase configurations are listed after the figure.

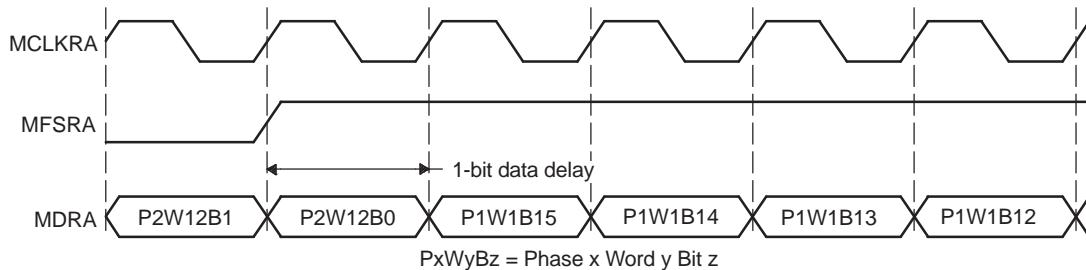
Figure 19-11. Implementing the AC97 Standard With a Dual-Phase Frame



- (R/X)PHASE = 1: Dual-phase frame
- (R/X)FRLEN1 = 0000000b: 1 word in phase 1
- (R/X)WDLEN1 = 010b: 16 bits per word in phase 1
- (R/X)FRLEN2 = 0001011b: 12 words in phase 2
- (R/X)WDLEN2 = 011b: 20 bits per word in phase 2
- CLKRP/CLKXP= 0: Receive data sampled on falling edge of internal CLKR / transmit data clocked on rising edge of internal CLKX
- FSRP/FSXP = 0: Active-high frame-sync signal
- (R/X)DATDLY = 01b: Data delay of 1 clock cycle (1-bit data delay)

Figure 19-12 shows the timing of an AC97-standard data transfer near frame synchronization. In this figure, individual bits are shown on D(R/X). Specifically, the figure shows the last two bits of phase 2 of one frame and the first four bits of phase 1 of the next frame. Regardless of the data delay, data transfers can occur without gaps. The first bit of the second frame (P1W1B15) immediately follows the last bit of the first frame (P2W12B0). Because a 1-bit data delay has been chosen, the transition on the frame-sync signal can occur when P2W12B0 is transferred.

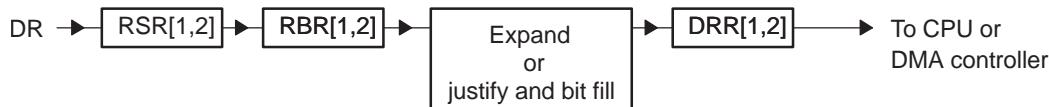
Figure 19-12. Timing of an AC97-Standard Data Transfer Near Frame Synchronization



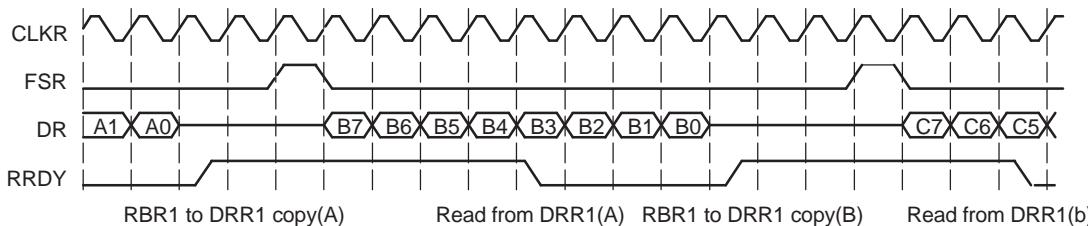
19.2.5 McBSP Reception

This section explains the fundamental process of reception in the McBSP. For details about how to program the McBSP receiver, see [Section 19.7](#).

Figure 19-13 and Figure 19-14 show how reception occurs in the McBSP. Figure 19-13 shows the physical path for the data. Figure 19-14 is a timing diagram showing signal activity for one possible reception scenario. A description of the process follows the figures.

Figure 19-13. McBSP Reception Physical Data Path

- A RSR[1,2]: Receive shift registers 1 and 2
- B RBR[1,2]: Receive buffer registers 1 and 2
- C DRR[1,2]: Data receive registers 1 and 2

Figure 19-14. McBSP Reception Signal Activity

- A CLKR: Internal receive clock
- B FSR: Internal receive frame-synchronization signal
- C DR: Data on DR pin
- D RRDY: Status of receiver ready bit (high is 1)

The following process describes how data travels from the DR pin to the CPU or to the DMA controller:

1. The McBSP waits for a receive frame-synchronization pulse on internal FSR.
2. When the pulse arrives, the McBSP inserts the appropriate data delay that is selected with the RDATDLY bits of RCR2.
In the preceding timing diagram, a 1-bit data delay is selected.
3. The McBSP accepts data bits on the DR pin and shifts them into the receive shift register(s). If the word length is 16 bits or smaller, only RSR1 is used. If the word length is larger than 16 bits, RSR2 and RSR1 are used and RSR2 contains the most significant bits. For details on choosing a word length, see [Section 19.7.8, Set the Receive Word Length\(s\)](#).
4. When a full word is received, the McBSP copies the contents of the receive shift register(s) to the receive buffer register(s), provided that RBR1 is not full with previous data.
If the word length is 16 bits or smaller, only RBR1 is used. If the word length is larger than 16 bits, RBR2 and RBR1 are used and RBR2 contains the most significant bits.
5. The McBSP copies the contents of the receive buffer register(s) into the data receive register(s), provided that DRR1 is not full with previous data. When DRR1 receives new data, the receiver ready bit (RRDY) is set in SPCR1. This indicates that received data is ready to be read by the CPU or the DMA controller.
If the word length is 16 bits or smaller, only DRR1 is used. If the word length is larger than 16 bits, DRR2 and DRR1 are used and DRR2 contains the most significant bits.
If companding is used during the copy (RCOMPAND = 10b or 11b in RCR2), the 8-bit compressed data in RBR1 is expanded to a left-justified 16-bit value in DRR1. If companding is disabled, the data copied from RBR[1,2] to DRR[1,2] is justified and bit filled according to the RJUST bits.
6. The CPU or the DMA controller reads the data from the data receive register(s). When DRR1 is read, RRDY is cleared and the next RBR-to-DRR copy is initiated.

NOTE: If both DRRs are required (word length larger than 16 bits), the CPU or the DMA controller must read from DRR2 first and then from DRR1. As soon as DRR1 is read, the next RBR-to-DRR copy is initiated. If DRR2 is not read first, the data in DRR2 is lost.

When activity is not properly timed, errors can occur. See the following topics for more details:

- [Overrun in the Receiver](#) (see [Section 19.4.2](#))

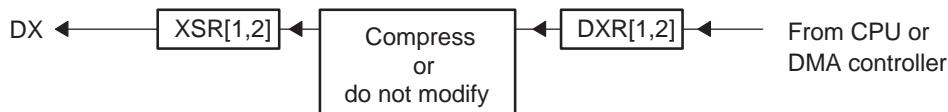
- *Unexpected Receive Frame-Synchronization Pulse (see [Section 19.4.3](#))*

19.2.6 McBSP Transmission

This section explains the fundamental process of transmission in the McBSP. For details about how to program the McBSP transmitter, see [Section 19.8](#).

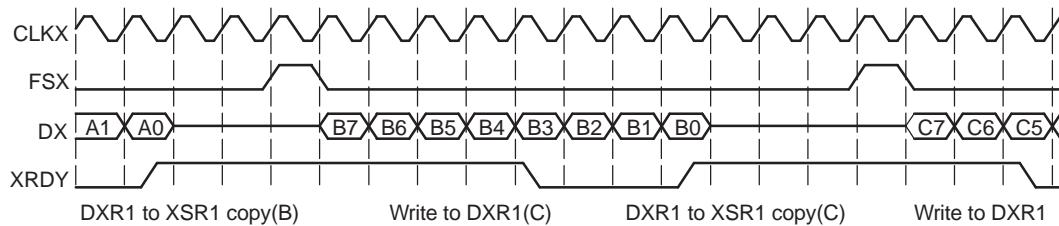
[Figure 19-15](#) and [Figure 19-16](#) show how transmission occurs in the McBSP. [Figure 19-15](#) shows the physical path for the data. [Figure 19-16](#) is a timing diagram showing signal activity for one possible transmission scenario. A description of the process follows the figures.

Figure 19-15. McBSP Transmission Physical Data Path



- A XSR[1,2]: Transmit shift registers 1 and 2
- B DXR[1,2]: Data transmit registers 1 and 2

Figure 19-16. McBSP Transmission Signal Activity



- A CLKX: Internal transmit clock
- B FSX: Internal transmit frame-synchronization signal
- C DX: Data on DX pin
- D XRDY: Status of transmitter ready bit (high is 1)

1. The CPU or the DMA controller writes data to the data transmit register(s). When DXR1 is loaded, the transmitter ready bit (XRDY) is cleared in SPCR2 to indicate that the transmitter is not ready for new data.

If the word length is 16 bits or smaller, only DXR1 is used. If the word length is larger than 16 bits, DXR2 and DXR1 are used and DXR2 contains the most significant bits. For details on choosing a word length, see [Section 19.8.8](#).

NOTE: If both DXRs are needed (word length larger than 16 bits), the CPU or the DMA controller must load DXR2 first and then load DXR1. As soon as DXR1 is loaded, the contents of both DXRs are copied to the transmit shift registers (XSRs), as described in the next step. If DXR2 is not loaded first, the previous content of DXR2 is passed to the XSR2.

2. When new data arrives in DXR1, the McBSP copies the content of the data transmit register(s) to the transmit shift register(s). In addition, the transmit ready bit (XRDY) is set. This indicates that the transmitter is ready to accept new data from the CPU or the DMA controller.

If the word length is 16 bits or smaller, only XSR1 is used. If the word length is larger than 16 bits, XSR2 and XSR1 are used and XSR2 contains the most significant bits.

If companding is used during the transfer (XCOMPAND = 10b or 11b in XCR2), the McBSP compresses the 16-bit data in DXR1 to 8-bit data in the μ-law or A-law format in XSR1. If companding is disabled, the McBSP passes data from the DXR(s) to the XSR(s) without modification.

3. The McBSP waits for a transmit frame-synchronization pulse on internal FSX.
4. When the pulse arrives, the McBSP inserts the appropriate data delay that is selected with the XDATDLY bits of XCR2.

In the preceding timing diagram ([Figure 19-16](#)), a 1-bit data delay is selected.

5. The McBSP shifts data bits from the transmit shift register(s) to the DX pin.

When activity is not properly timed, errors can occur. See the following topics for more details:

- Overwrite in the Transmitter ([Section 19.4.4](#))
- Underflow in the Transmitter ([Section 19.4.5](#))
- Unexpected Transmit Frame-Synchronization Pulse ([Section 19.4.6](#))

19.2.7 Interrupts and DMA Events Generated by a McBSP

The McBSP sends notification of important events to the CPU and DMA via the internal signals shown in [Table 19-3](#).

Table 19-3. Interrupts and DMA Events Generated by a McBSP

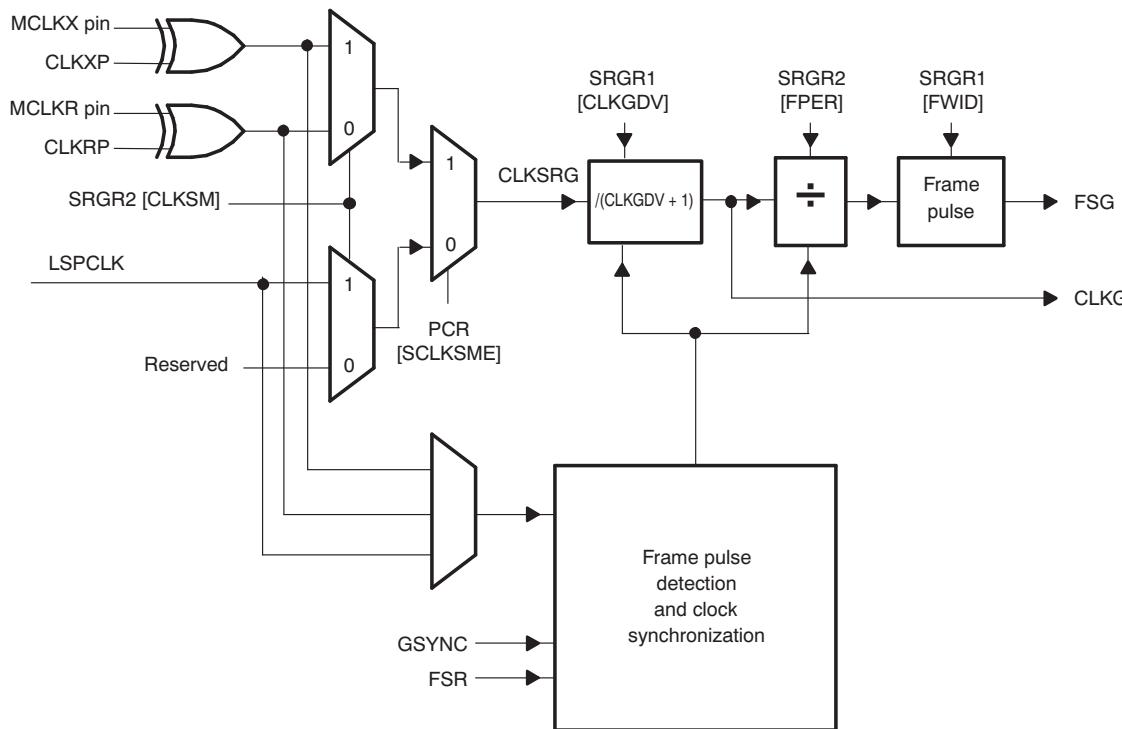
Internal Signal	Description
RINT	Receive interrupt The McBSP can send a receive interrupt request to CPU based upon a selected condition in the receiver of the McBSP (a condition selected by the RINTM bits of SPCR1).
XINT	Transmit interrupt The McBSP can send a transmit interrupt request to CPU based upon a selected condition in the transmitter of the McBSP (a condition selected by the XINTM bits of SPCR2).
REVT	Receive synchronization event An REVT signal is sent to the DMA when data has been received in the data receive registers (DRRs).
XEVT	Transmit synchronization event An XEVT signal is sent to the DMA when the data transmit registers (DXRs) are ready to accept the next serial word for transmission.

19.3 McBSP Sample Rate Generator

Each McBSP contains a sample rate generator (SRG) that can be programmed to generate an internal data clock (CLKG) and an internal frame-synchronization signal (FSG). CLKG can be used for bit shifting on the data receive (DR) pin and/or the data transmit (DX) pin. FSG can be used to initiate frame transfers on DR and/or DX. [Figure 19-17](#) is a conceptual block diagram of the sample rate generator.

19.3.1 Block Diagram

Figure 19-17. Conceptual Block Diagram of the Sample Rate Generator



The source clock for the sample rate generator (labeled CLKSRG in the diagram) can be supplied by the LSPCLK, or by an external pin (MCLKX or MCLKR). The source is selected with the SCLKME bit of PCR and the CLKSM bit of SRGR2. If a pin is used, the polarity of the incoming signal can be inverted with the appropriate polarity bit (CLKXP of PCR or CLKRP of PCR).

The sample rate generator has a three-stage clock divider that gives CLKG and FSG programmability. The three stages provide:

- Clock divide-down. The source clock is divided according to the CLKGDV bits of SRGR1 to produce CLKG.
- Frame period divide-down. CLKG is divided according to the FPER bits of SRGR2 to control the period from the start of a frame-pulse to the start of the next pulse.
- Frame-synchronization pulse-width countdown. CLKG cycles are counted according to the FWID bits of SRGR1 to control the width of each frame-synchronization pulse.

NOTE: The McBSP cannot operate at a frequency faster than $\frac{1}{2}$ the source clock frequency. Choose an input clock frequency and a CLKGDV value such that CLKG is less than or equal to $\frac{1}{2}$ the source clock frequency.

In addition to the three-stage clock divider, the sample rate generator has a frame-synchronization pulse detection and clock synchronization module that allows synchronization of the clock divide down with an incoming frame-synchronization pulse on the FSR pin. This feature is enabled or disabled with the GSYNC bit of SRGR2.

For details on getting the sample rate generator ready for operation, see [Section 19.3.4](#).

19.3.1.1 Clock Generation in the Sample Rate Generator

The sample rate generator can produce a clock signal (CLKG) for use by the receiver, the transmitter, or both. Use of the sample rate generator to drive clocking is controlled by the clock mode bits (CLKRM and CLKXM) in the pin control register (PCR). When a clock mode bit is set to 1 (CLKRM = 1 for reception, CLKXM = 1 for transmission), the corresponding data clock (CLKR for reception, CLKX for transmission) is driven by the internal sample rate generator output clock (CLKG).

The effects of CLKRM = 1 and CLKXM = 1 on the McBSP are partially affected by the use of the digital loopback mode and the clock stop (SPI) mode, respectively, as described in [Table 19-4](#). The digital loopback mode (described in [Section 19.7.4](#)) is selected with the DLB bit of SPCR1. The clock stop mode (described in [Section 19.6.2](#)) is selected with the CLKSTP bits of SPCR1.

When using the sample rate generator as a clock source, make sure the sample rate generator is enabled (GRST = 1).

Table 19-4. Effects of DLB and CLKSTP on Clock Modes

Mode Bit Settings		Effect
CLKRM = 1	DLB = 0 (Digital loopback mode disabled)	CLKR is an output pin driven by the sample rate generator output clock (CLKG).
	DLB = 1 (Digital loopback mode enabled)	CLKR is an output pin driven by internal CLKX. The source for CLKX depends on the CLKXM bit.
CLKXM = 1	CLKSTP = 00b or 01b (Clock stop (SPI) mode disabled)	CLKX is an output pin driven by the sample rate generator output clock (CLKG).
	CLKSTP = 10b or 11b (Clock stop (SPI) mode enabled)	The McBSP is a master in an SPI system. Internal CLKX drives internal CLKR and the shift clocks of any SPI-compliant slave devices in the system. CLKX is driven by the internal sample rate generator.

19.3.1.2 Choosing an Input Clock

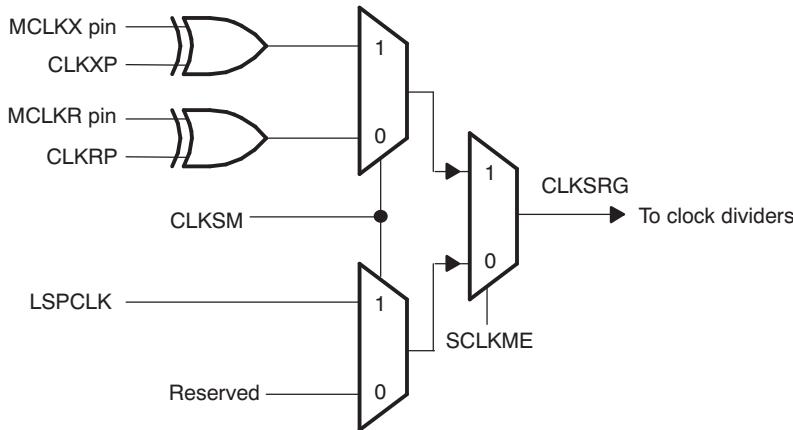
The sample rate generator must be driven by an input clock signal from one of the three sources selectable with the SCLKME bit of PCR and the CLKSM bit of SRGR2 (see [Table 19-5](#)). When CLKSM = 1, the minimum divide down value in CLKGDV bits is 1. CLKGDV is described in [Section 19.3.1.4](#).

Table 19-5. Choosing an Input Clock for the Sample Rate Generator with the SCLKME and CLKSM Bits

SCLKME	CLKSM	Input Clock for Sample Rate Generator
0	0	Reserved
0	1	LSPCLK
1	0	Signal on MCLKR pin
1	1	Signal on MCLKX pin

19.3.1.3 Choosing a Polarity for the Input Clock

As shown in [Figure 19-18](#), when the input clock is received from a pin, you can choose the polarity of the input clock. The rising edge of CLKSRG generates CLKG and FSG, but you can determine which edge of the input clock causes a rising edge on CLKSRG. The polarity options and their effects are described in [Table 19-6](#).

Figure 19-18. Possible Inputs to the Sample Rate Generator and the Polarity Bits**Table 19-6. Polarity Options for the Input to the Sample Rate Generator**

Input Clock	Polarity Option	Effect
LSPCLK	Always positive polarity	Rising edge of CPU clock generates transitions on CLKG and FSG.
Signal on MCLKR pin	CLKRP = 0 in PCR	Falling edge on MCLKR pin generates transitions on CLKG and FSG.
	CLKRP = 1 in PCR	Rising edge on MCLKR pin generates transitions on CLKG and FSG.
Signal on MCLKX pin	CLKXP = 0 in PCR	Rising edge on MCLKX pin generates transitions on CLKG and FSG.
	CLKXP = 1 in PCR	Falling edge on MCLKX pin generates transitions on CLKG and FSG.

19.3.1.4 Choosing a Frequency for the Output Clock (CLKG)

The input clock (LSPCLK or external clock) can be divided down by a programmable value to drive CLKG. Regardless of the source to the sample rate generator, the rising edge of CLKSRG (see [Figure 19-1](#)) generates CLKG and FSG.

The first divider stage of the sample rate generator creates the output clock from the input clock. This divider stage uses a counter that is preloaded with the divide down value in the CLKGDV bits of SRGR1. The output of this stage is the data clock (CLKG). CLKG has the frequency represented by the equation.

Equation 1: CLKG Frequency

$$\text{CLKG frequency} = \frac{\text{Input clock frequency}}{(\text{CLKGDV} + 1)}$$

19.3.1.4.1 CLKG Frequency

Thus, the input clock frequency is divided by a value between 1 and 256. When CLKGDV is odd or equal to 0, the CLKG duty cycle is 50%. When CLKGDV is an even value, $2p$, representing an odd divide down, the high-state duration is $p+1$ cycles and the low-state duration is p cycles.

19.3.1.5 Keeping CLKG Synchronized to External MCLKR

When the MCLKR pin is used to drive the sample rate generator (see [Section 19.3.1.2](#)), the GSYNC bit in SRGR2 and the FSR pin can be used to configure the timing of the output clock (CLKG) relative to the input clock. Note that this feature is available only when the MCLKR pin is used to feed the external clock.

GSYNC = 1 ensures that the McBSP and an external device are dividing down the input clock with the same phase relationship. If GSYNC = 1, an inactive-to-active transition on the FSR pin triggers a resynchronization of CLKG and generation of FSG.

For more details about synchronization, see [Section 19.3.3](#).

19.3.2 Frame Synchronization Generation in the Sample Rate Generator

The sample rate generator can produce a frame-synchronization signal (FSG) for use by the receiver, the transmitter, or both.

If you want the receiver to use FSG for frame synchronization, make sure FSRM = 1. (When FSRM = 0, receive frame synchronization is supplied via the FSR pin.)

If you want the transmitter to use FSG for frame synchronization, you must set:

- FSXM = 1 in PCR: This indicates that transmit frame synchronization is supplied by the McBSP itself rather than from the FSX pin.
- FSGM = 1 in SRGR2: This indicates that when FSXM = 1, transmit frame synchronization is supplied by the sample rate generator. (When FSGM = 0 and FSXM = 1, the transmitter uses frame-synchronization pulses generated every time data is transferred from DXR[1,2] to XSR[1,2].)

In either case, the sample rate generator must be enabled (GRST = 1) and the frame-synchronization logic in the sample rate generator must be enabled (FRST = 1).

19.3.2.1 Choosing the Width of the Frame-Synchronization Pulse on FSG

Each pulse on FSG has a programmable width. You program the FWID bits of SRGR1, and the resulting pulse width is (FWID + 1) CLKG cycles, where CLKG is the output clock of the sample rate generator.

19.3.2.2 Controlling the Period Between the Starting Edges of Frame-Synchronization Pulses on FSG

You can control the amount of time from the starting edge of one FSG pulse to the starting edge of the next FSG pulse. This period is controlled in one of two ways, depending on the configuration of the sample rate generator:

- If the sample rate generator is using an external input clock and GSYNC = 1 in SRGR2, FSG pulses in response to an inactive-to-active transition on the FSR pin. Thus, the frame-synchronization period is controlled by an external device.
- Otherwise, you program the FPER bits of SRGR2, and the resulting frame-synchronization period is (FPER + 1) CLKG cycles, where CLKG is the output clock of the sample rate generator.

19.3.2.3 Keeping FSG Synchronized to an External Clock

When an external signal is selected to drive the sample rate generator (see [Section 19.3.1.2](#) on page [Section 19.3.1.2](#)), the GSYNC bit of SRGR2 and the FSR pin can be used to configure the timing of FSG pulses.

GSYNC = 1 ensures that the McBSP and an external device are dividing down the input clock with the same phase relationship. If GSYNC = 1, an inactive-to-active transition on the FSR pin triggers a resynchronization of CLKG and generation of FSG.

See [Section 19.3.3](#) for more details about synchronization.

19.3.3 Synchronizing Sample Rate Generator Outputs to an External Clock

The sample rate generator can produce a clock signal (CLKG) and a frame-synchronization signal (FSG) based on an input clock signal that is either the CPU clock signal or a signal at the MCLKR or MCLKX pin. When an external clock is selected to drive the sample rate generator, the GSYNC bit of SRGR2 and the FSR pin can be used to control the timing of CLKG and the pulsing of FSG relative to the chosen input clock.

Make GSYNC = 1 when you want the McBSP and an external device to divide down the input clock with the same phase relationship. If GSYNC = 1:

- An inactive-to-active transition on the FSR pin triggers a resynchronization of CLKG and a pulsing of FSG.
- CLKG always begins with a high state after synchronization.
- FSR is always detected at the same edge of the input clock signal that generates CLKG, no matter how long the FSR pulse is.

- The FPER bits of SRGR2 are ignored because the frame-synchronization period on FSG is determined by the arrival of the next frame-synchronization pulse on the FSR pin.

If GSYNC = 0, CLKG runs freely and is not resynchronized, and the frame-synchronization period on FSG is determined by FPER.

19.3.3.1 Operating the Transmitter Synchronously with the Receiver

When GSYNC = 1, the transmitter can operate synchronously with the receiver, provided that:

- FSX is programmed to be driven by FSG (FSGM = 1 in SRGR2 and FSXM = 1 in PCR). If the input FSR has appropriate timing so that it can be sampled by the falling edge of CLKG, it can be used, instead, by setting FSXM = 0 and connecting FSR to FSX externally.
- The sample rate generator clock drives the transmit and receive clocking (CLKRM = CLKXM = 1 in PCR).

19.3.3.2 Synchronization Examples

Figure 19-19 and Figure 19-20 show the clock and frame-synchronization operation with various polarities of CLKR and FSR. These figures assume FWID = 0 in SRGR1, for an FSG pulse that is one CLKG cycle wide. The FPER bits of SRGR2 are not programmed; the period from the start of a frame-synchronization pulse to the start of the next pulse is determined by the arrival of the next inactive-to-active transition on the FSR pin. Each of the figures shows what happens to CLKG when it is initially synchronized and GSYNC = 1, and when it is not initially synchronized and GSYNC = 1. The second figure has a slower CLKG frequency (it has a larger divide-down value in the CLKGDV bits of SRGR1).

Figure 19-19. CLKG Synchronization and FSG Generation When GSYNC = 1 and CLKGDV = 1

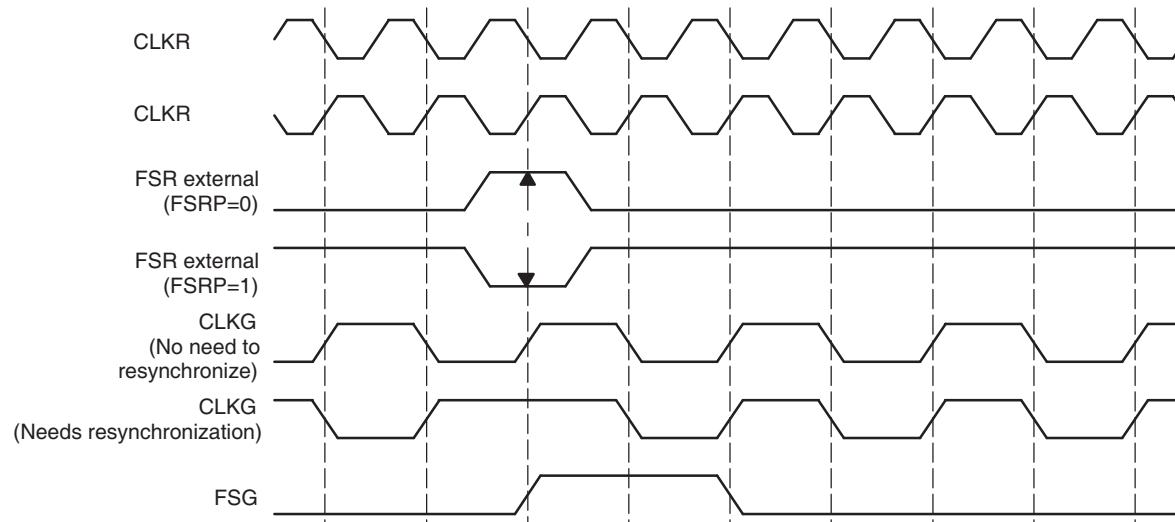
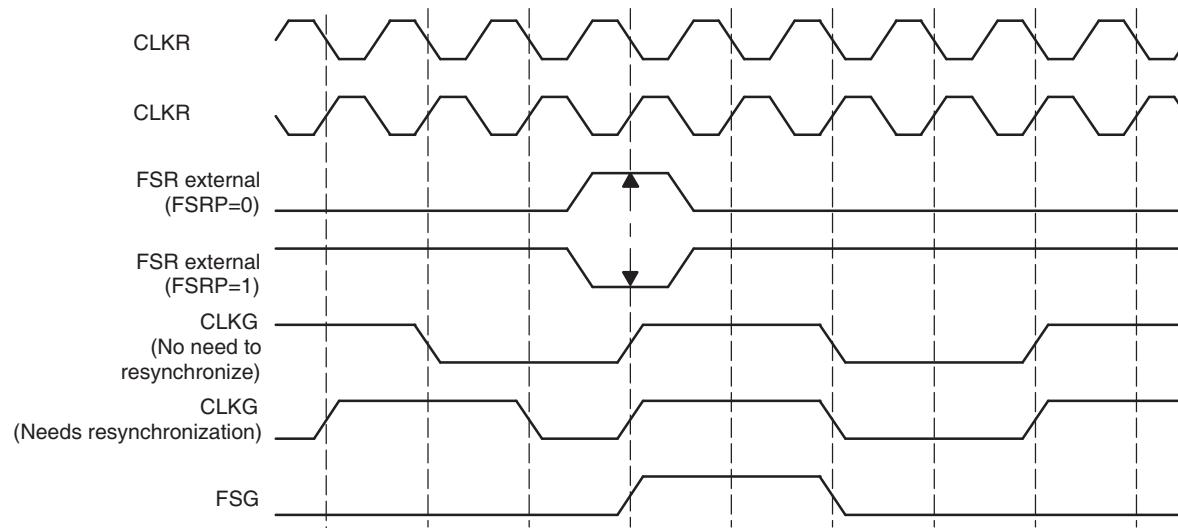


Figure 19-20. CLKG Synchronization and FSG Generation When GSYNC = 1 and CLKGDV = 3

19.3.4 Reset and Initialization Procedure for the Sample Rate Generator

To reset and initialize the sample rate generator:

Step 1. Place the McBSP/sample rate generator in reset.

During a DSP reset, the sample rate generator, the receiver, and the transmitter reset bits (GRST, RRST, and XRST) are automatically forced to 0. Otherwise, during normal operation, the sample rate generator can be reset by making GRST = 0 in SPCR2, provided that CLKG and/or FSG is not used by any portion of the McBSP. Depending on your system you may also want to reset the receiver (RRST = 0 in SPCR1) and reset the transmitter (XRST = 0 in SPCR2).

If GRST = 0 due to a device reset, CLKG is driven by the CPU clock divided by 2, and FSG is driven inactive-low. If GRST = 0 due to program code, CLKG and FSG are driven low (inactive).

Step 2. Program the registers that affect the sample rate generator.

Program the sample rate generator registers (SRGR1 and SRGR2) as required for your application. If necessary, other control registers can be loaded with desired values, provided the respective portion of the McBSP (the receiver or transmitter) is in reset.

After the sample rate generator registers are programmed, wait 2 CLKSRG cycles. This ensures proper synchronization internally.

Step 3. Enable the sample rate generator (take it out of reset).

In SPCR2, make GRST = 1 to enable the sample rate generator.

After the sample rate generator is enabled, wait two CLKG cycles for the sample rate generator logic to stabilize.

On the next rising edge of CLKSRG, CLKG transitions to 1 and starts clocking with a frequency equal to the CLKG Frequency equation below.

Table 19-7. Input Clock Selection for Sample Rate Generator

SCLKME	CLKSM	Input Clock for Sample Rate Generator
0	0	Reserved
0	1	LSPCLK
1	0	Signal on MCLKR pin
1	1	Signal on MCLKX pin

Step 4. If necessary, enable the receiver and/or the transmitter.

If necessary, remove the receiver and/or transmitter from reset by setting RRST and/or XRST = 1.

Step 5. If necessary, enable the frame-synchronization logic of the sample rate generator.

After the required data acquisition setup is done (DXR[1,2] is loaded with data), set GRST = 1 in SPCR2 if an internally generated frame-synchronization pulse is required. FSG is generated with an active-high edge after the programmed number of CLKG clocks (FPER + 1) have elapsed.

Equation 2: CLKG Frequency

$$\text{CLKG frequency} = \frac{\text{Input clock frequency}}{(\text{CLKGDV} + 1)}$$

where the input clock is selected with the SCLKME bit of PCR and the CLKSM bit of SRGR2 in one of the configurations shown in [Table 19-7](#).

19.4 McBSP Exception/Error Conditions

This chapter describes exception/error conditions and how to handle them.

19.4.1 Types of Errors

There are five serial port events that can constitute a system error:

- Receiver overrun (RFULL = 1)

This occurs when DRR1 has not been read since the last RBR-to-DRR copy. Consequently, the receiver does not copy a new word from the RBR(s) to the DRR(s) and the RSR(s) are now full with another new word shifted in from DR. Therefore, RFULL = 1 indicates an error condition wherein any new data that can arrive at this time on DR replaces the contents of the RSR(s), and the previous word is lost. The RSRs continue to be overwritten as long as new data arrives on DR and DRR1 is not read. For more details about overrun in the receiver, see [Section 19.4.2](#).

- Unexpected receive frame-synchronization pulse (RSYNCERR = 1)

This occurs during reception when RFIG = 0 and an unexpected frame-synchronization pulse occurs. An unexpected frame-synchronization pulse is one that begins the next frame transfer before all the bits of the current frame have been received. Such a pulse causes data reception to abort and restart. If new data has been copied into the RBR(s) from the RSR(s) since the last RBR-to-DRR copy, this new data in the RBR(s) is lost. This is because no RBR-to-DRR copy occurs; the reception has been restarted. For more details about receive frame-synchronization errors, see [Section 19.4.3](#).

- Transmitter data overwrite

This occurs when the CPU or DMA controller overwrites data in the DXR(s) before the data is copied to the XSR(s). The overwritten data never reaches the DX pin. For more details about overwrite in the transmitter, see [Section 19.4.4](#).

- Transmitter underflow ($\overline{\text{XEMPTY}} = 0$)

If a new frame-synchronization signal arrives before new data is loaded into DXR1, the previous data in the DXR(s) is sent again. This procedure continues for every new frame-synchronization pulse that arrives until DXR1 is loaded with new data. For more details about underflow in the transmitter, see [Section 19.4.5](#).

- Unexpected transmit frame-synchronization pulse (XSYNCERR = 1)

This occurs during transmission when XFIG = 0 and an unexpected frame-synchronization pulse occurs. An unexpected frame-synchronization pulse is one that begins the next frame transfer before all the bits of the current frame have been transferred. Such a pulse causes the current data transmission to abort and restart. If new data has been written to the DXR(s) since the last DXR-to-XSR copy, the current value in the XSR(s) is lost. For more details about transmit frame-synchronization errors, see [Section 19.4.6](#).

19.4.2 Overrun in the Receiver

RFULL = 1 in SPCR1 indicates that the receiver has experienced overrun and is in an error condition.

RFULL is set when all of the following conditions are met:

1. DRR1 has not been read since the last RBR-to-DRR copy ($RRDY = 1$).
2. RBR1 is full and an RBR-to-DRR copy has not occurred.
3. RSR1 is full and an RSR1-to-RBR copy has not occurred.

As described in the [Section 19.2.5](#), data arriving on DR is continuously shifted into RSR1 (for word length of 16 bits or smaller) or RSR2 and RSR1 (for word length larger than 16 bits). Once a complete word is shifted into the RSR(s), an RSR-to-RBR copy can occur only if the previous data in RBR1 has been copied to DRR1. The $RRDY$ bit is set when new data arrives in DRR1 and is cleared when that data is read from DRR1. Until $RRDY = 0$, the next RBR-to-DRR copy does not take place, and the data is held in the RSR(s). New data arriving on the DR pin is shifted into RSR(s), and the previous content of the RSR(s) is lost.

You can prevent the loss of data if DRR1 is read no later than 2.5 cycles before the end of the third word is shifted into the RSR1.

NOTE: If both DRRs are needed (word length larger than 16 bits), the CPU or the DMA controller must read from DRR2 first and then from DRR1. As soon as DRR1 is read, the next RBR-to-DRR copy is initiated. If DRR2 is not read first, the data in DRR2 is lost.

After the receiver starts running from reset, a minimum of three words must be received before RFULL is set. Either of the following events clears the RFULL bit and allows subsequent transfers to be read properly:

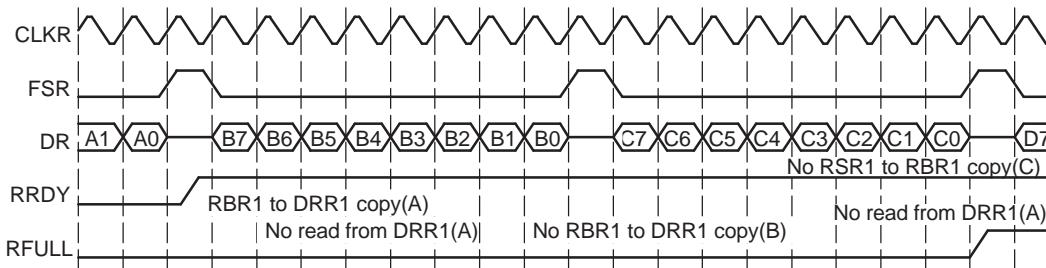
- The CPU or DMA controller reads DRR1.
- The receiver is reset individually ($RRST = 0$) or as part of a device reset.

Another frame-synchronization pulse is required to restart the receiver.

19.4.2.1 Example of Overrun Condition

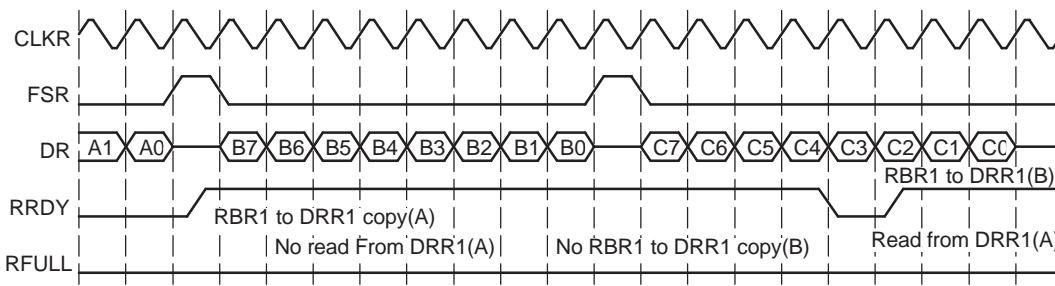
[Figure 19-21](#) shows the receive overrun condition. Because serial word A is not read from DRR1 before serial word B arrives in RBR1, B is not transferred to DRR1 yet. Another new word © arrives and RSR1 is full with this data. DRR1 is finally read, but not earlier than 2.5 cycles before the end of word C. Therefore, new data (D) overwrites word C in RSR1. If DRR1 is not read in time, the next word can overwrite D.

Figure 19-21. Overrun in the McBSP Receiver



19.4.2.2 Example of Preventing Overrun Condition

[Figure 19-22](#) shows the case where RFULL is set, but the overrun condition is prevented by a read from DRR1 at least 2.5 cycles before the next serial word © is completely shifted into RSR1. This ensures that an RBR1-to-DRR1 copy of word B occurs before receiver attempts to transfer word C from RSR1 to RBR1.

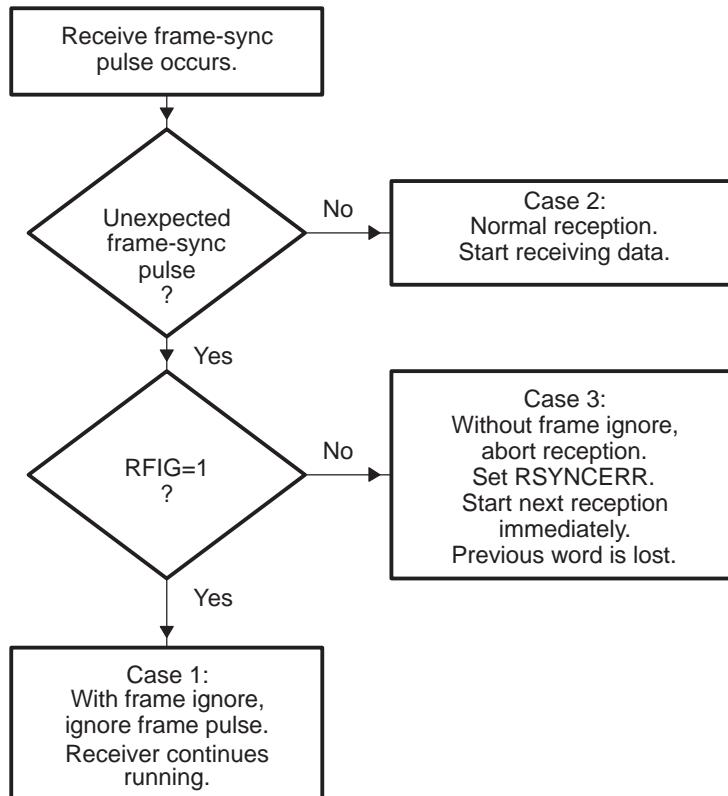
Figure 19-22. Overrun Prevented in the McBSP Receiver

19.4.3 Unexpected Receive Frame-Synchronization Pulse

Section 19.4.3.1 shows how the McBSP responds to any receive frame-synchronization pulses, including an unexpected pulse. Section 19.4.3.2 and Section 19.4.3.3 show an examples of a frame-synchronization error and an example of how to prevent such an error, respectively.

19.4.3.1 Possible Responses to Receive Frame-Synchronization Pulses

Figure 19-23 shows the decision tree that the receiver uses to handle all incoming frame-synchronization pulses. The figure assumes that the receiver has been started (RRST = 1 in SPCR1). Case 3 in the figure is the case in which an error occurs.

Figure 19-23. Possible Responses to Receive Frame-Synchronization Pulses

Any one of three cases can occur:

- Case 1: Unexpected internal FSR pulses with RFIG = 1 in RCR2. Receive frame-synchronization pulses are ignored, and the reception continues.
- Case 2: Normal serial port reception. Reception continues normally because the frame-synchronization

pulse is not unexpected. There are three possible reasons why a receive operation might *not* be in progress when the pulse occurs:

- The FSR pulse is the first after the receiver is enabled (RRST = 1 in SPCR1).
- The FSR pulse is the first after DRR[1,2] is read, clearing a receiver full (RFULL = 1 in SPCR1) condition.
- The serial port is in the interpacket intervals. The programmed data delay for reception (programmed with the RDATDLY bits in RCR2) may start during these interpacket intervals for the first bit of the next word to be received. Thus, at maximum frame frequency, frame synchronization can still be received 0 to 2 clock cycles before the first bit of the synchronized frame.
- Case 3: Unexpected receive frame synchronization with RFIG = 0 (frame-synchronization pulses not ignored). Unexpected frame-synchronization pulses can originate from an external source or from the internal sample rate generator.

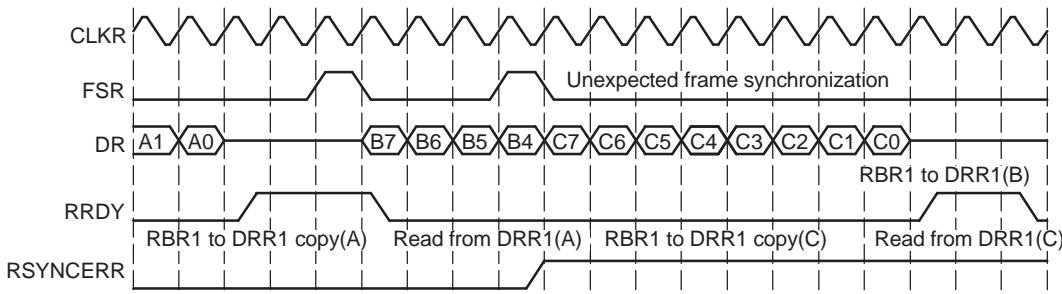
If a frame-synchronization pulse starts the transfer of a new frame before the current frame is fully received, this pulse is treated as an unexpected frame-synchronization pulse, and the receiver sets the receive frame-synchronization error bit (RSYNCERR) in SPCR1. RSYNCERR can be cleared only by a receiver reset or by a write of 0 to this bit.

If you want the McBSP to notify the CPU of receive frame-synchronization errors, you can set a special receive interrupt mode with the RINTM bits of SPCR1. When RINTM = 11b, the McBSP sends a receive interrupt (RINT) request to the CPU each time that RSYNCERR is set.

19.4.3.2 Example of Unexpected Receive Frame-Synchronization Pulse

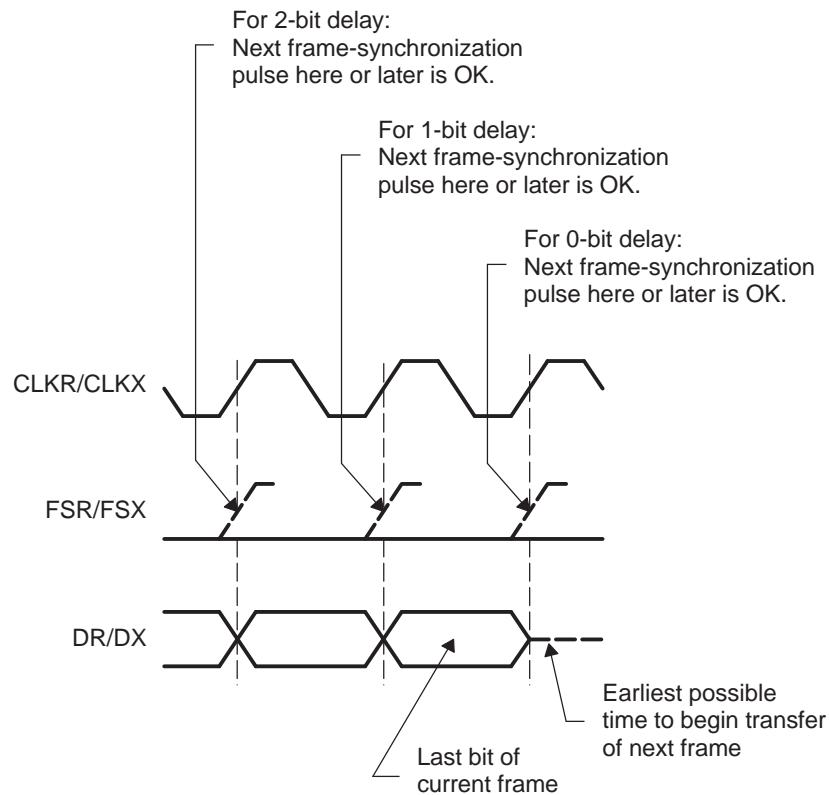
[Figure 19-30](#) shows an unexpected receive frame-synchronization pulse during normal operation of the serial port, with time intervals between data packets. When the unexpected frame-synchronization pulse occurs, the RSYNCERR bit is set, the reception of data B is aborted, and the reception of data C begins. In addition, if RINTM = 11b, the McBSP sends a receive interrupt (RINT) request to the CPU.

Figure 19-24. An Unexpected Frame-Synchronization Pulse During a McBSP Reception



19.4.3.3 Preventing Unexpected Receive Frame-Synchronization Pulses

Each frame transfer can be delayed by 0, 1, or 2 MCLKR cycles, depending on the value in the RDATDLY bits of RCR2. For each possible data delay, [Figure 19-25](#) shows when a new frame-synchronization pulse on FSR can safely occur relative to the last bit of the current frame.

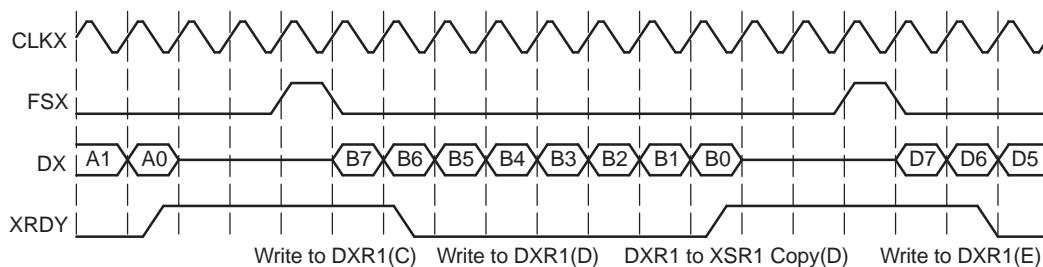
Figure 19-25. Proper Positioning of Frame-Synchronization Pulses

19.4.4 Overwrite in the Transmitter

As described in the section on McBSP transmission (page [Section 19.2.6](#)), the transmitter must copy the data previously written to the DXR(s) by the CPU or DMA controller into the XSR(s) and then shift each bit from the XSR(s) to the DX pin. If new data is written to the DXR(s) before the previous data is copied to the XSR(s), the previous data in the DXR(s) is overwritten and thus lost.

19.4.4.1 Example of Overwrite Condition

[Figure 19-26](#) shows what happens if the data in DXR1 is overwritten before being transmitted. Initially, DXR1 is loaded with data C. A subsequent write to DXR1 overwrites C with D before C is copied to XSR1. Thus, C is never transmitted on DX.

Figure 19-26. Data in the McBSP Transmitter Overwritten and Thus Not Transmitted

19.4.4.2 Preventing Overwrites

You can prevent CPU overwrites by making the CPU:

- Poll for XRDY = 1 in SPCR2 before writing to the DXR(s). XRDY is set when data is copied from DXR1 to XSR1 and is cleared when new data is written to DXR1.

- Wait for a transmit interrupt (XINT) before writing to the DXR(s). When XINTM = 00b in SPCR2, the transmitter sends XINT to the CPU each time XRDY is set.

You can prevent DMA overwrites by synchronizing DMA transfers to the transmit synchronization event XEV_T. The transmitter sends an XEV_T signal each time XRDY is set.

19.4.5 Underflow in the Transmitter

The McBSP indicates a transmitter empty (or underflow) condition by clearing the XEMPTY bit in SPCR2. Either of the following events activates XEMPTY (XEMPTY = 0):

- DXR1 has not been loaded since the last DXR-to-XSR copy, and all bits of the data word in the XSR(s) have been shifted out on the DX pin.
- The transmitter is reset (by forcing XRST = 0 in SPCR2, or by a device reset) and is then restarted.

In the underflow condition, the transmitter continues to transmit the old data that is in the DXR(s) for every new transmit frame-synchronization signal until a new value is loaded into DXR1 by the CPU or the DMA controller.

NOTE: If both DXRs are needed (word length larger than 16 bits), the CPU or the DMA controller must load DXR2 first and then load DXR1. As soon as DXR1 is loaded, the contents of both DXRs are copied to the transmit shift registers (XSRs). If DXR2 is not loaded first, the previous content of DXR2 is passed to the XSR2.

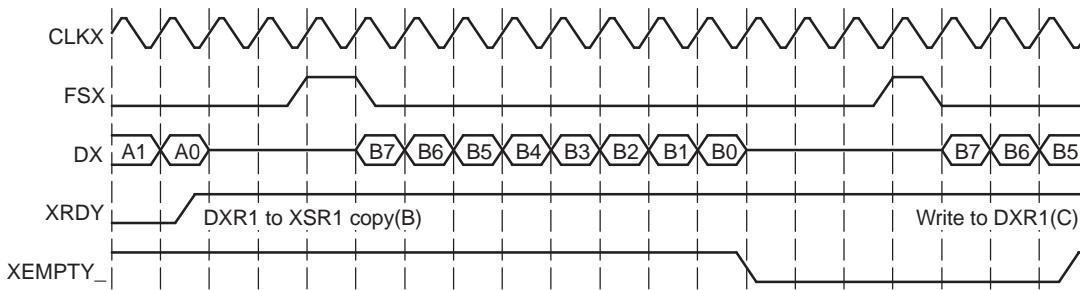
XEMPTY is deactivated (XEMPTY = 1) when a new word in DXR1 is transferred to XSR1. If FSXM = 1 in PCR and FSGM = 0 in SRGR2, the transmitter generates a single internal FSX pulse in response to a DXR-to-XSR copy. Otherwise, the transmitter waits for the next frame-synchronization pulse before sending out the next frame on DX.

When the transmitter is taken out of reset (XRST = 1), it is in a transmitter ready (XRDY = 1 in SPCR2) and transmitter empty (XEMPTY = 0) state. If DXR1 is loaded by the CPU or the DMA controller before internal FSX goes active high, a valid DXR-to-XSR transfer occurs. This allows for the first word of the first frame to be valid even before the transmit frame-synchronization pulse is generated or detected. Alternatively, if a transmit frame-synchronization pulse is detected before DXR1 is loaded, zeros are output on DX.

19.4.5.1 Example of the Underflow Condition

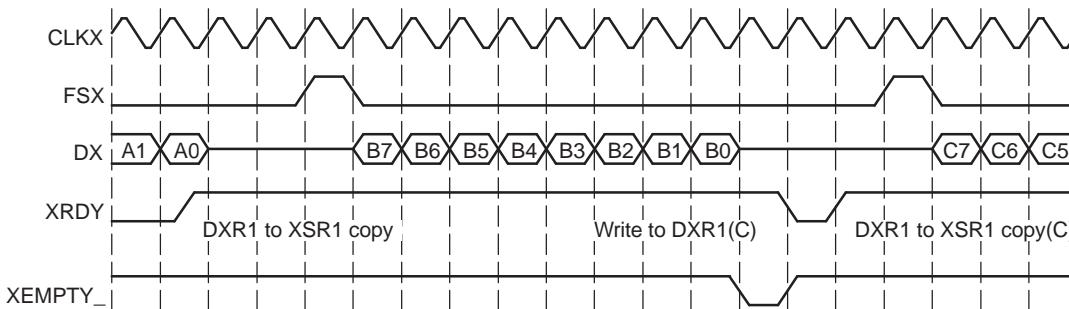
Figure 19-27 shows an underflow condition. After B is transmitted, DXR1 is not reloaded before the subsequent frame-synchronization pulse. Thus, B is again transmitted on DX.

Figure 19-27. Underflow During McBSP Transmission



19.4.5.2 Example of Preventing Underflow Condition

Figure 19-28 shows the case of writing to DXR1 just before an underflow condition would otherwise occur. After B is transmitted, C is written to DXR1 before the next frame-synchronization pulse. As a result, there is no underflow; B is not transmitted twice.

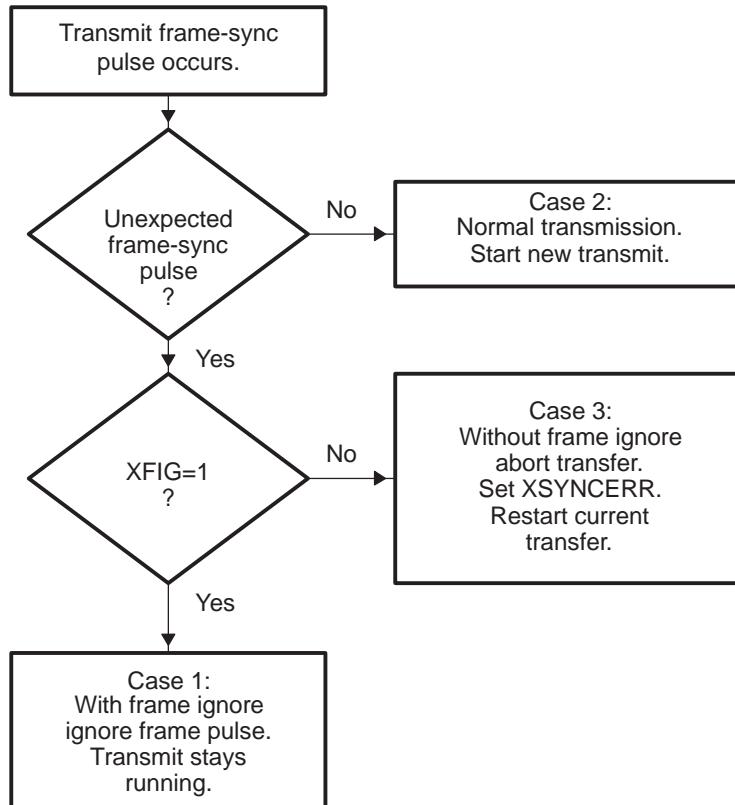
Figure 19-28. Underflow Prevented in the McBSP Transmitter

19.4.6 Unexpected Transmit Frame-Synchronization Pulse

[Section 19.4.6.1](#) shows how the McBSP responds to any transmit frame-synchronization pulses, including an unexpected pulse. [Section 19.4.6.2](#) and [Section 19.4.6.3](#) show examples of a frame-synchronization error and an example of how to prevent such an error, respectively.

19.4.6.1 Possible Responses to Transmit Frame-Synchronization Pulses

[Figure 19-29](#) shows the decision tree that the transmitter uses to handle all incoming frame-synchronization pulses. The figure assumes that the transmitter has been started (XRST = 1 in SPCR2). Case 3 in the figure is the case in which an error occurs.

Figure 19-29. Possible Responses to Transmit Frame-Synchronization Pulses

Any one of three cases can occur:

- Case 1: Unexpected internal FSX pulses with XFIG = 1 in XCR2. Transmit frame-synchronization pulses are ignored, and the transmission continues.
- Case 2: Normal serial port transmission. Transmission continues normally because the frame-

synchronization pulse is not unexpected. There are two possible reasons why a transmit operations might *not* be in progress when the pulse occurs:

This FSX pulse is the first after the transmitter is enabled ($XRST = 1$).

The serial port is in the interpacket intervals. The programmed data delay for transmission (programmed with the XDATDLY bits of XCR2) may start during these interpacket intervals before the first bit of the previous word is transmitted. Thus, at maximum packet frequency, frame synchronization can still be received 0 to 2 clock cycles before the first bit of the synchronized frame.

- Case 3: Unexpected transmit frame synchronization with $XFIG = 0$ (frame-synchronization pulses not ignored). Unexpected frame-synchronization pulses can originate from an external source or from the internal sample rate generator.

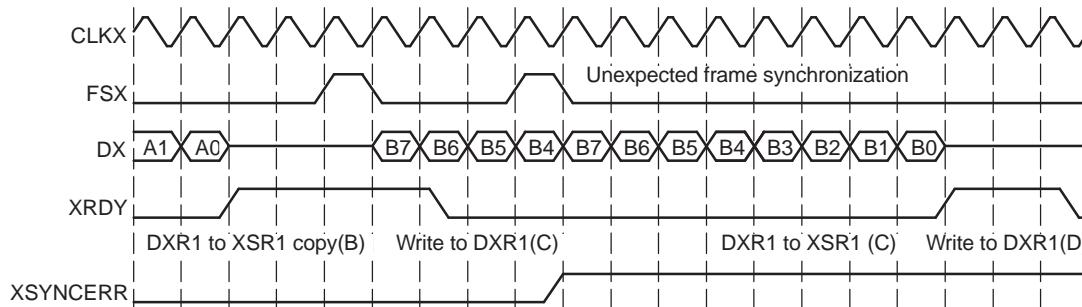
If a frame-synchronization pulse starts the transfer of a new frame before the current frame is fully transmitted, this pulse is treated as an unexpected frame-synchronization pulse, and the transmitter sets the transmit frame-synchronization error bit (XSYNCERR) in SPCR2. XSYNCERR can be cleared only by a transmitter reset or by a write of 0 to this bit.

If you want the McBSP to notify the CPU of frame-synchronization errors, you can set a special transmit interrupt mode with the XINTM bits of SPCR2. When $XINTM = 11b$, the McBSP sends a transmit interrupt (XINT) request to the CPU each time that XSYNCERR is set.

19.4.6.2 Example of Unexpected Transmit Frame-Synchronization Pulse

[Section 19.4.3.2](#) shows an unexpected transmit frame-synchronization pulse during normal operation of the serial port with intervals between the data packets. When the unexpected frame-synchronization pulse occurs, the XSYNCERR bit is set and the transmission of data B is restarted because no new data has been passed to XSR1 yet. In addition, if $XINTM = 11b$, the McBSP sends a transmit interrupt (XINT) request to the CPU.

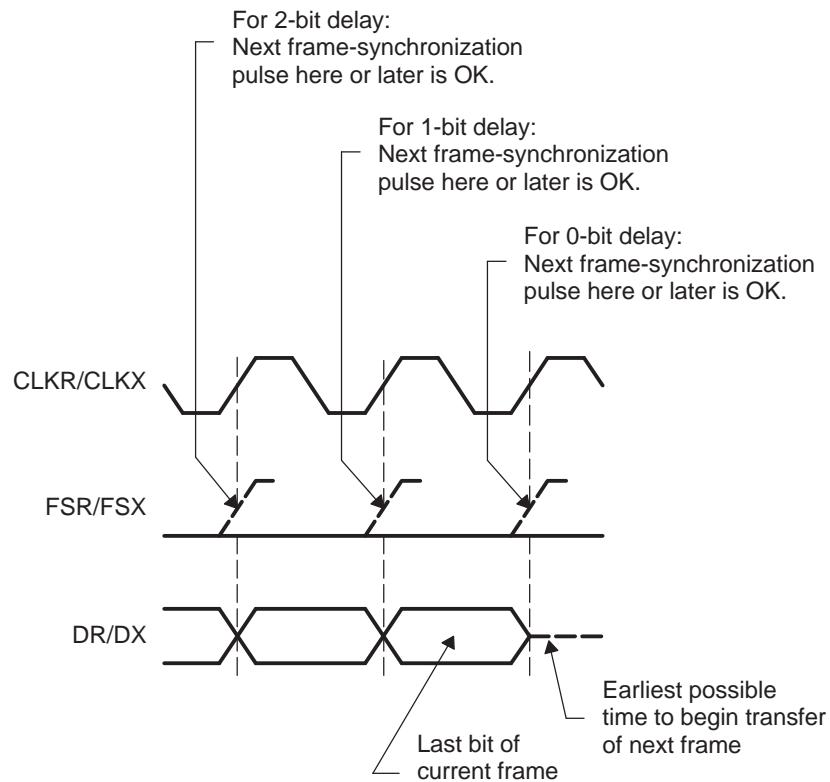
Figure 19-30. An Unexpected Frame-Synchronization Pulse During a McBSP Transmission



19.4.6.3 Preventing Unexpected Transmit Frame-Synchronization Pulses

Each frame transfer can be delayed by 0, 1, or 2 CLKX cycles, depending on the value in the XDATDLY bits of XCR2. For each possible data delay, [Figure 19-31](#) shows when a new frame-synchronization pulse on FSX can safely occur relative to the last bit of the current frame.

Figure 19-31. Proper Positioning of Frame-Synchronization Pulses



19.5 Multichannel Selection Modes

This section discusses the multichannel selection modes for the McBSP.

19.5.1 *Channels, Blocks, and Partitions*

A McBSP channel is a time slot for shifting in/out the bits of one serial word. Each McBSP supports up to 128 channels for reception and 128 channels for transmission.

In the receiver and in the transmitter, the 128 available channels are divided into eight blocks that each contain 16 contiguous channels (see [Table 19-8](#) through [Table 19-10](#)) :

- It is possible to have two receive partitions (A & B) and 8 transmit partitions (A – H).
- McBSP can transmit/receive on selected channels.
- Each channel partition has a dedicated channel-enable register. Each bit controls whether data flow is allowed or prevented in one of the channels assigned to that partition.
- There are three transmit multichannel modes and one receive multichannel mode.

Table 19-8. Block - Channel Assignment

Block	Channels
0	0 -15
1	16 - 31
2	32 - 47
3	48 - 63
4	64 - 79
5	80 - 95
6	96 - 111
7	112 - 127

The blocks are assigned to partitions according to the selected partition mode. In the two-partition mode (described in [Section 19.5.4](#)), you assign one even-numbered block (0, 2, 4, or 6) to partition A and one odd-numbered block (1, 3, 5, or 7) to partition B. In the 8-partition mode (described in [Section 19.5.5](#)), blocks 0 through 7 are automatically assigned to partitions, A through H, respectively.

Table 19-9. 2-Partition Mode

Partition	Blocks
A	0 or 2 or 4 or 6
B	1 or 3 or 5 or 7

Table 19-10. 8-Partition mode

Partition	Blocks	Channels
A	0	0 - 15
B	1	16 - 31
C	2	32 - 47
D	3	48 - 63
E	4	64 - 79
F	5	80 - 95
G	6	96 - 111
H	7	112 - 127

The number of partitions for reception and the number of partitions for transmission are independent. For example, it is possible to use two receive partitions (A and B) and eight transmit partitions (A-H).

19.5.2 Multichannel Selection

When a McBSP uses a time-division multiplexed (TDM) data stream while communicating with other McBSPs or serial devices, the McBSP may need to receive and/or transmit on only a few channels. To save memory and bus bandwidth, you can use a multichannel selection mode to prevent data flow in some of the channels.

Each channel partition has a dedicated channel enable register. If the appropriate multichannel selection mode is on, each bit in the register controls whether data flow is allowed or prevented in one of the channels that is assigned to that partition.

The McBSP has one receive multichannel selection mode (described in [Section 19.5.6](#)) and three transmit multichannel selection modes (described in [Section 19.5.7](#)).

19.5.3 Configuring a Frame for Multichannel Selection

Before you enable a multichannel selection mode, make sure you properly configure the data frame:

- Select a single-phase frame (RPHASE/XPHASE = 0). Each frame represents a TDM data stream.
- Set a frame length (in RFRLEN1/XFRLEN1) that includes the highest-numbered channel to be used. For example, if you plan to use channels 0, 15, and 39 for reception, the receive frame length must be at least 40 (RFRLEN1 = 39). If XFRLEN1 = 39 in this case, the receiver creates 40 time slots per frame but only receives data during time slots 0, 15, and 39 of each frame.

19.5.4 Using Two Partitions

For multichannel selection operation in the receiver and/or the transmitter, you can use two partitions or eight partitions (described in [Section 19.5.5](#)). If you choose the 2-partition mode (RMCME = 0 for reception, XMCME = 0 for transmission), McBSP channels are activated using an alternating scheme. In response to a frame-synchronization pulse, the receiver or transmitter begins with the channels in partition A and then alternates between partitions B and A until the complete frame has been transferred. When the next frame-synchronization pulse occurs, the next frame is transferred beginning with the channels in partition A.

19.5.4.1 Assigning Blocks to Partitions A and B

For reception, any two of the eight receive-channel blocks can be assigned to receive partitions A and B, which means up to 32 receive channels can be enabled at any given point in time. Similarly, any two of the eight transmit-channel blocks (up 32 enabled transmit channels) can be assigned to transmit partitions A and B.

For reception:

- Assign an even-numbered channel block (0, 2, 4, or 6) to receive partition A by writing to the RPABLK bits. In the receive multichannel selection mode (described in [Section 19.5.6](#)), the channels in this partition are controlled by receive channel enable register A (RCERA).
- Assign an odd-numbered block (1, 3, 5, or 7) to receive partition B with the RPBBLK bits. In the receive multichannel selection mode, the channels in this partition are controlled by receive channel enable register B (RCERB).

For transmission:

- Assign an even-numbered channel block (0, 2, 4, or 6) to transmit partition A by writing to the XPABLK bits. In one of the transmit multichannel selection modes (described in [Section 19.5.7](#)), the channels in this partition are controlled by transmit channel enable register A (XCERA).
- Assign an odd-numbered block (1, 3, 5, or 7) to transmit partition B with the XPBBLK bits. In one of the transmit multichannel selection modes, the channels in this partition are controlled by transmit channel enable register B (XCERB).

[Figure 19-32](#) shows an example of alternating between the channels of partition A and the channels of partition B. Channels 0-15 have been assigned to partition A, and channels 16-31 have been assigned to partition B. In response to a frame-synchronization pulse, the McBSP begins a frame transfer with partition A and then alternates between partitions B and A until the complete frame is transferred.

Figure 19-32. Alternating Between the Channels of Partition A and the Channels of Partition B

Two-partition mode. Example with fixed block assignments

Partition	A	B	A	B	A	B	A	B	A
Block	0	1	0	1	0	1	0	1	0
Channels	0-15	16-31	0-15	16-31	0-15	16-31	0-15	16-31	0-15
FS(R/X)	1	0	1	0	1	0	1	0	1

As explained in [Section 19.5.4.2](#), you can dynamically change which blocks of channels are assigned to the partitions.

19.5.4.2 Reassigning Blocks During Reception/Transmission

If you want to use more than 32 channels, you can change which channel blocks are assigned to partitions A and B during the course of a data transfer. However, these changes must be carefully timed. While a partition is being transferred, its associated block assignment bits cannot be modified and its associated channel enable register cannot be modified. For example, if block 3 is being transferred and block 3 is assigned to partition A, you can modify neither (R/X)PABLK to assign different channels to partition A nor (R/X)CERA to change the channel configuration for partition A.

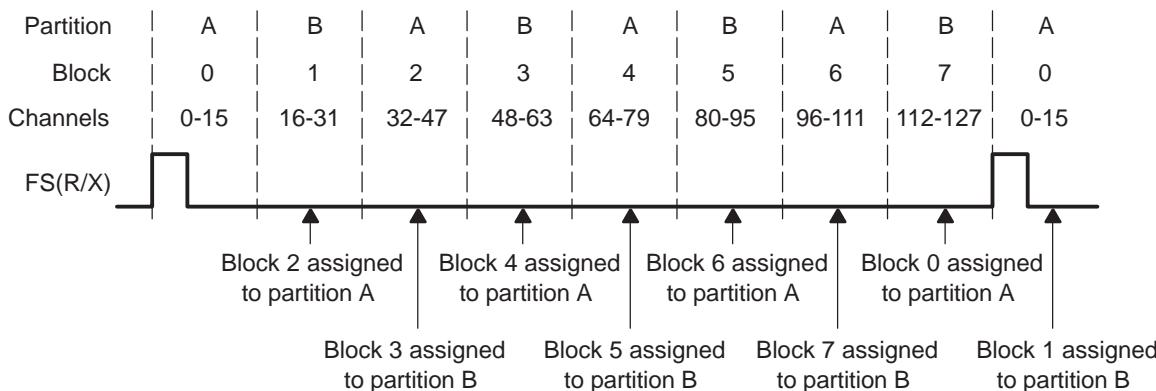
Several features of the McBSP help you time the reassignment:

- The block of channels currently involved in reception/transmission (the current block) is reflected in the RCBLK/XCBLK bits. Your program can poll these bits to determine which partition is active. When a partition is not active, it is safe to change its block assignment and channel configuration.
- At the end of every block (at the boundary of two partitions), an interrupt can be sent to the CPU. In response to the interrupt, the CPU can then check the RCBLK/XCBLK bits and update the inactive partition. See [Section 19.5.8](#).

[Figure 19-33](#) shows an example of reassigning channels throughout a data transfer. In response to a frame-synchronization pulse, the McBSP alternates between partitions A and B. Whenever partition B is active, the CPU changes the block assignment for partition A. Whenever partition A is active, the CPU changes the block assignment for partition B.

Figure 19-33. Reassigning Channel Blocks Throughout a McBSP Data Transfer

Two-partition mode. Example with changing block assignments



19.5.5 Using Eight Partitions

For multichannel selection operation in the receiver and/or the transmitter, you can use eight partitions or two partitions (described in [Section 19.5.4](#)). If you choose the 8-partition mode (RMCME = 1 for reception, XMCME = 1 for transmission), McBSP channels are activated in the following order: A, B, C, D, E, F, G, H. In response to a frame-synchronization pulse, the receiver or transmitter begins with the channels in partition A and then continues with the other partitions in order until the complete frame has been transferred. When the next frame-synchronization pulse occurs, the next frame is transferred, beginning with the channels in partition A.

In the 8-partition mode, the (R/X)PABLK and (R/X)PBBLK bits are ignored and the 16-channel blocks are assigned to the partitions as shown in [Table 19-11](#) and [Table 19-12](#). These assignments cannot be changed. The tables also show the registers used to control the channels in the partitions.

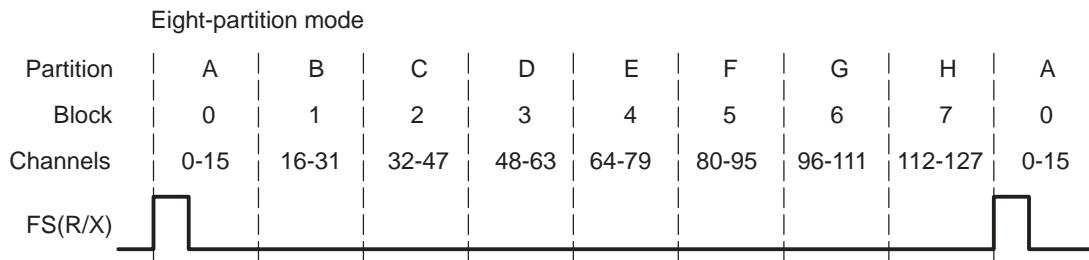
Table 19-11. Receive Channel Assignment and Control With Eight Receive Partitions

Receive Partition	Assigned Block of Receive Channels	Register Used For Channel Control
A	Block 0: channels 0 through 15	RCERA
B	Block 1: channels 16 through 31	RCERB
C	Block 2: channels 32 through 47	RCERC
D	Block 3: channels 48 through 63	RCERD
E	Block 4: channels 64 through 79	RCERE
F	Block 5: channels 80 through 95	RCERF
G	Block 6: channels 96 through 111	RCERG
H	Block 7: channels 112 through 127	RCERH

Table 19-12. Transmit Channel Assignment and Control When Eight Transmit Partitions Are Used

Transmit Partition	Assigned Block of Transmit Channels	Register Used For Channel Control
A	Block 0: channels 0 through 15	XCERA
B	Block 1: channels 16 through 31	XCERB
C	Block 2: channels 32 through 47	XCERC
D	Block 3: channels 48 through 63	XCERD
E	Block 4: channels 64 through 79	XCERE
F	Block 5: channels 80 through 95	XCERF
G	Block 6: channels 96 through 111	XCERG
H	Block 7: channels 112 through 127	XCERH

Figure 19-34 shows an example of the McBSP using the 8-partition mode. In response to a frame-synchronization pulse, the McBSP begins a frame transfer with partition A and then activates B, C, D, E, F, G, and H to complete a 128-word frame.

Figure 19-34. McBSP Data Transfer in the 8-Partition Mode

19.5.6 Receive Multichannel Selection Mode

The RMCM bit of MCR1 determines whether all channels or only selected channels are enabled for reception. When RMCM = 0, all 128 receive channels are enabled and cannot be disabled. When RMCM = 1, the receive multichannel selection mode is enabled. In this mode:

- Channels can be individually enabled or disabled. The only channels enabled are those selected in the appropriate receive channel enable registers (RCERs). The way channels are assigned to the RCERs depends on the number of receive channel partitions (2 or 8), as defined by the RMCME bit of MCR1.
- If a receive channel is disabled, any bits received in that channel are passed only as far as the receive buffer register(s) (RBR(s)). The receiver does not copy the content of the RBR(s) to the DRR(s), and as a result, does not set the receiver ready bit (RRDY). Therefore, no DMA synchronization event (REVT) is generated and, if the receiver interrupt mode depends on RRDY (RINTM = 00b), no interrupt is generated.

As an example of how the McBSP behaves in the receive multichannel selection mode, suppose you enable only channels 0, 15, and 39 and that the frame length is 40. The McBSP:

1. Accepts bits shifted in from the DR pin in channel 0
2. Ignores bits received in channels 1-14
3. Accepts bits shifted in from the DR pin in channel 15
4. Ignores bits received in channels 16-38
5. Accepts bits shifted in from the DR pin in channel 39

19.5.7 Transmit Multichannel Selection Modes

The XMCM bits of XCR2 determine whether all channels or only selected channels are enabled and unmasked for transmission. More details on enabling and masking are in [Section 19.5.7.1](#). The McBSP has three transmit multichannel selection modes (XMCM = 01b, XMCM = 10b, and XMCM = 11b), which are described in the following table.

Table 19-13. Selecting a Transmit Multichannel Selection Mode With the XMCM Bits

XMCM	Transmit Multichannel Selection Mode
00b	No transmit multichannel selection mode is on. All channels are enabled and unmasked. No channels can be disabled or masked.
01b	All channels are disabled unless they are selected in the appropriate transmit channel enable registers (XCERs). If enabled, a channel in this mode is also unmasked.
10b	The XMCME bit of MCR2 determines whether 32 channels or 128 channels are selectable in XCERs.
11b	All channels are enabled, but they are masked unless they are selected in the appropriate transmit channel enable registers (XCERs).
	The XMCME bit of MCR2 determines whether 32 channels or 128 channels are selectable in XCERs.
	This mode is used for symmetric transmission and reception.
	All channels are disabled for transmission unless they are enabled for reception in the appropriate receive channel enable registers (RCERs). Once enabled, they are masked unless they are also selected in the appropriate transmit channel enable registers (XCERs).
	The XMCME bit of MCR2 determines whether 32 channels or 128 channels are selectable in RCERs and XCERs.

As an example of how the McBSP behaves in a transmit multichannel selection mode, suppose that XMCM = 01b (all channels disabled unless individually enabled) and that you have enabled only channels 0, 15, and 39. Suppose also that the frame length is 40. The McBSP:...

1. Shifts data to the DX pin in channel 0
2. Places the DX pin in the high impedance state in channels 1-14
3. Shifts data to the DX pin in channel 15
4. Places the DX pin in the high impedance state in channels 16-38
5. Shifts data to the DX pin in channel 39

19.5.7.1 Disabling/Enabling Versus Masking/Unmasking

For transmission, a channel can be:

- Enabled and unmasked (transmission can begin and can be completed)
- Enabled but masked (transmission can begin but cannot be completed)
- Disabled (transmission cannot occur)

The following definitions explain the channel control options:

Enabled channel	A channel that can begin transmission by passing data from the data transmit register(s) (DXR(s)) to the transmit shift registers (XSR(s)).
Masked channel	A channel that cannot complete transmission. The DX pin is held in the high impedance state; data cannot be shifted out on the DX pin.
Disabled channel	In systems where symmetric transmit and receive provides software benefits, this feature allows transmit channels to be disabled on a shared serial bus. A similar feature is not needed for reception because multiple receptions cannot cause serial bus contention.
Unmasked channel	A channel that is not enabled. A disabled channel is also masked. Because no DXR-to-XSR copy occurs, the XRDY bit of SPCR2 is not set. Therefore, no DMA synchronization event (XEVT) is generated, and if the transmit interrupt mode depends on XRDY (XINTM = 00b in SPCR2), no interrupt is generated. The XEMPTY bit of SPCR2 is not affected.

19.5.7.2 Activity on McBSP Pins for Different Values of XMCM

Figure 19-35 shows the activity on the McBSP pins for the various XMCM values. In all cases, the transmit frame is configured as follows:

- XPHASE = 0: Single-phase frame (required for multichannel selection modes)
- XFRLEN1 = 0000011b: 4 words per frame
- XWDLEN1 = 000b: 8 bits per word

- XMCME = 0: 2-partition mode (only partitions A and B used)

In the case where XMCM = 11b, transmission and reception are symmetric, which means the corresponding bits for the receiver (RPHASE, RFRLLEN1, RWDLEN1, and RMCME) must have the same values as XPHASE, XFRLEN1, and XWDLEN1, respectively.

In the figure, the arrows showing where the various events occur are only sample indications. Wherever possible, there is a time window in which these events can occur.

19.5.8 Using Interrupts Between Block Transfers

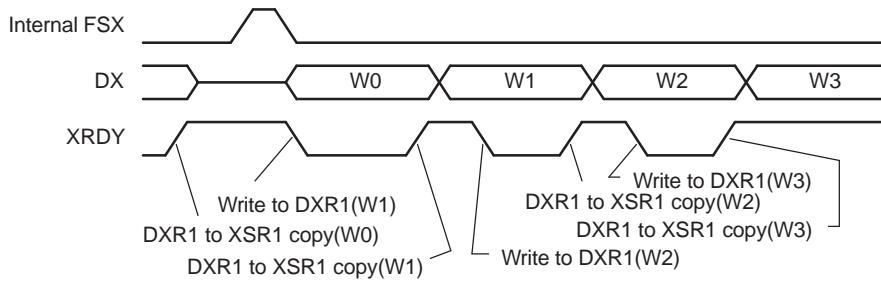
When a multichannel selection mode is used, an interrupt request can be sent to the CPU at the end of every 16-channel block (at the boundary between partitions and at the end of the frame). In the receive multichannel selection mode, a receive interrupt (RINT) request is generated at the end of each block transfer if RINTM = 01b. In any of the transmit multichannel selection modes, a transmit interrupt (XINT) request is generated at the end of each block transfer if XINTM = 01b. When RINTM/XINTM = 01b, no interrupt is generated unless a multichannel selection mode is on.

These interrupt pulses are active high and last for two CPU clock cycles.

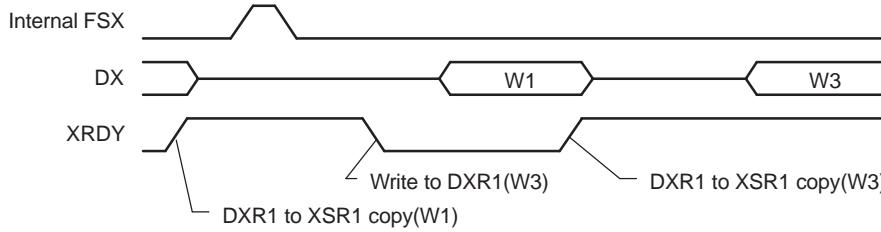
This type of interrupt is especially helpful if you are using the two-partition mode (described in [Section 19.5.4](#)) and you want to know when you can assign a different block of channels to partition A or B.

Figure 19-35. Activity on McBSP Pins for the Possible Values of XMCM

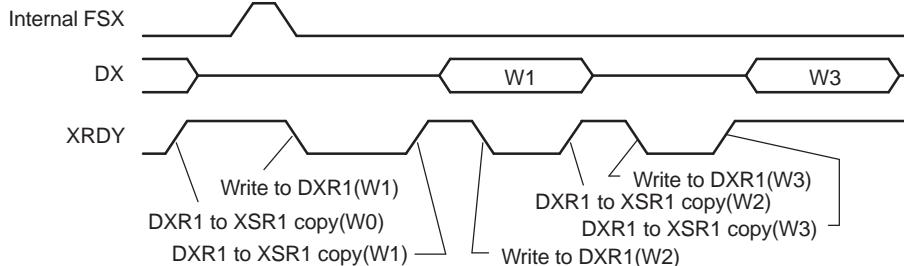
(a) XMCM = 00b: All channels enabled and unmasked



(b) XMCM = 01b, XPABLK = 00b, XCERA = 1010b: Only channels 1 and 3 enabled and unmasked

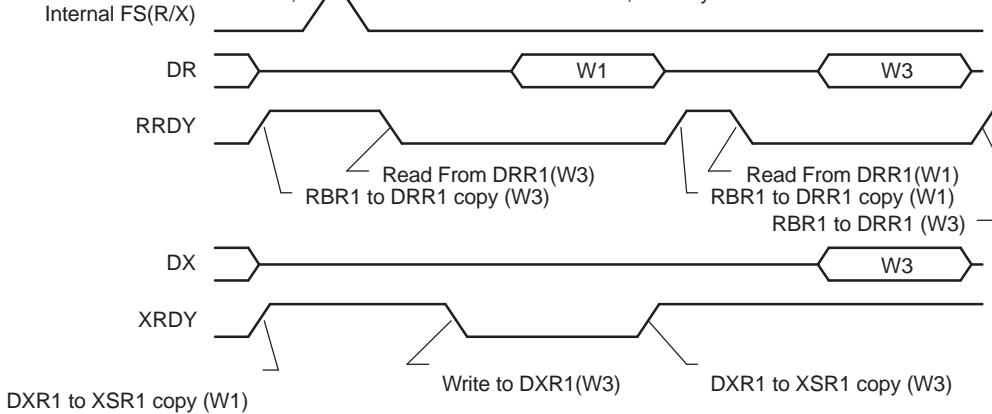


(c) XMCM = 10b, XPABLK = 00b, XCERA = 1010b: All channels enabled, only 1 and 3 unmasked



(d) XMCM = 11b, RPABLK = 00b, XPABLK = X, RCERA = 1010b, XCERA = 1000b:

Receive channels: 1 and 3 enabled; transmit channels: 1 and 3 enabled, but only 3 unmasked



19.6 SPI Operation Using the Clock Stop Mode

This chapter explains how to use the McBSP in SPI mode.

19.6.1 SPI Protocol

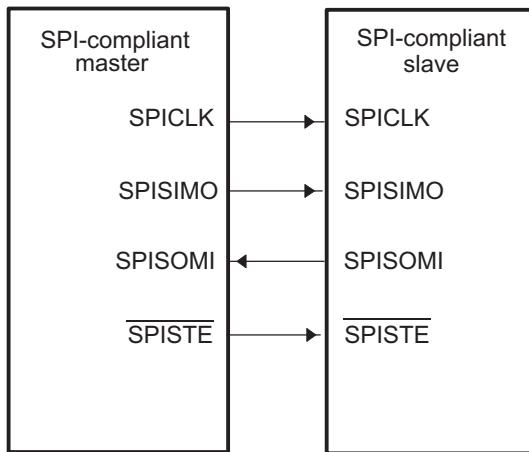
The SPI protocol is a master-slave configuration with one master device and one or more slave devices. The interface consists of the following four signals:

- Serial data input (also referred to as master in/slave out, or SPISOMI)

- Serial data output (also referred to as master out/slave in, or SPISIMO)
- Shift-clock (also referred to as SPICLK)
- Slave-enable signal (also referred to as SPISTE)

A typical SPI interface with a single slave device is shown in [Figure 19-36](#).

Figure 19-36. Typical SPI Interface



The master device controls the flow of communication by providing shift-clock and slave-enable signals. The slave-enable signal is an optional active-low signal that enables the serial data input and output of the slave device (device not sending out the clock).

In the absence of a dedicated slave-enable signal, communication between the master and slave is determined by the presence or absence of an active shift-clock. When the McBSP is operating in SPI master mode and the SPISTE signal is not used by the slave SPI port, the slave device must remain enabled at all times, and multiple slaves cannot be used.

19.6.2 Clock Stop Mode

The clock stop mode of the McBSP provides compatibility with the SPI protocol. When the McBSP is configured in clock stop mode, the transmitter and receiver are internally synchronized so that the McBSP functions as an SPI master or slave device. The transmit clock signal (CLKX) corresponds to the serial clock signal (SPICLK) of the SPI protocol, while the transmit frame-synchronization signal (FSX) is used as the slave-enable signal (SPISTE).

The receive clock signal (MCLKR) and receive frame-synchronization signal (FSR) are not used in the clock stop mode because these signals are internally connected to their transmit counterparts, CLKX and FSX.

19.6.3 Bits Used to Enable and Configure the Clock Stop Mode

The bits required to configure the McBSP as an SPI device are introduced in [Table 19-14](#). [Table 19-15](#) shows how the various combinations of the CLKSTP bit and the polarity bits CLKXP and CLKRP create four possible clock stop mode configurations. The timing diagrams in [Section 19.6.4](#) show the effects of CLKSTP, CLKXP, and CLKRP.

Table 19-14. Bits Used to Enable and Configure the Clock Stop Mode

Bit Field	Description
CLKSTP bits of SPCR1	Use these bits to enable the clock stop mode and to select one of two timing variations. (See also Table 19-15 .)
CLKXP bit of PCR	This bit determines the polarity of the CLKX signal. (See also Table 19-15 .)
CLKRP bit of PCR	This bit determines the polarity of the MCLKR signal. (See also Table 19-15 .)
CLKXM bit of PCR	This bit determines whether CLKX is an input signal (McBSP as slave) or an output signal (McBSP as master).

Table 19-14. Bits Used to Enable and Configure the Clock Stop Mode (continued)

Bit Field	Description
XPHASE bit of XCR2	You must use a single-phase transmit frame (XPHASE = 0).
RPHASE bit of RCR2	You must use a single-phase receive frame (RPHASE = 0).
XFRLEN1 bits of XCR1	You must use a transmit frame length of 1 serial word (XFRLEN1 = 0).
RFRLEN1 bits of RCR1	You must use a receive frame length of 1 serial word (RFRLEN1 = 0).
XWDLEN1 bits of XCR1	The XWDLEN1 bits determine the transmit packet length. XWDLEN1 must be equal to RWDLEN1 because in the clock stop mode. The McBSP transmit and receive circuits are synchronized to a single clock.
RWDLEN1 bits of RCR1	The RWDLEN1 bits determine the receive packet length. RWDLEN1 must be equal to XWDLEN1 because in the clock stop mode. The McBSP transmit and receive circuits are synchronized to a single clock.

Table 19-15. Effects of CLKSTP, CLKXP, and CLKRP on the Clock Scheme

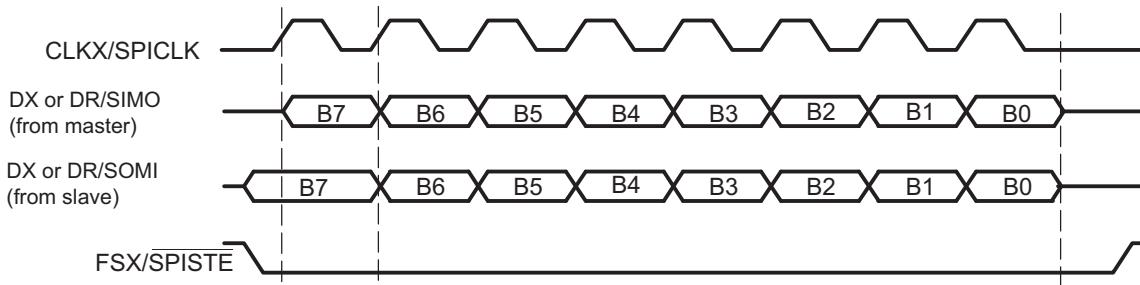
Bit Settings	Clock Scheme
CLKSTP = 00b or 01b	Clock stop mode disabled. Clock enabled for non-SPI mode.
CLKXP = 0 or 1	
CLKRP = 0 or 1	
CLKSTP = 10b	Low inactive state without delay: The McBSP transmits data on the rising edge of CLKX and receives data on the falling edge of MCLKR.
CLKXP = 0	
CLKRP = 0	
CLKSTP = 11b	Low inactive state with delay: The McBSP transmits data one-half cycle ahead of the rising edge of CLKX and receives data on the rising edge of MCLKR.
CLKXP = 0	
CLKRP = 1	
CLKSTP = 10b	High inactive state without delay: The McBSP transmits data on the falling edge of CLKX and receives data on the rising edge of MCLKR.
CLKXP = 1	
CLKRP = 0	
CLKSTP = 11b	High inactive state with delay: The McBSP transmits data one-half cycle ahead of the falling edge of CLKX and receives data on the falling edge of MCLKR.
CLKXP = 1	
CLKRP = 1	

19.6.4 Clock Stop Mode Timing Diagrams

The timing diagrams for the four possible clock stop mode configurations are shown here. Notice that the frame-synchronization signal used in clock stop mode is active throughout the entire transmission as a slave-enable signal. Although the timing diagrams show 8-bit transfers, the packet length can be set to 8, 12, 16, 20, 24, or 32 bits per packet. The receive packet length is selected with the RWDLEN1 bits of RCR1, and the transmit packet length is selected with the XWDLEN1 bits of XCR1. For clock stop mode, the values of RWDLEN1 and XWDLEN1 must be the same because the McBSP transmit and receive circuits are synchronized to a single clock.

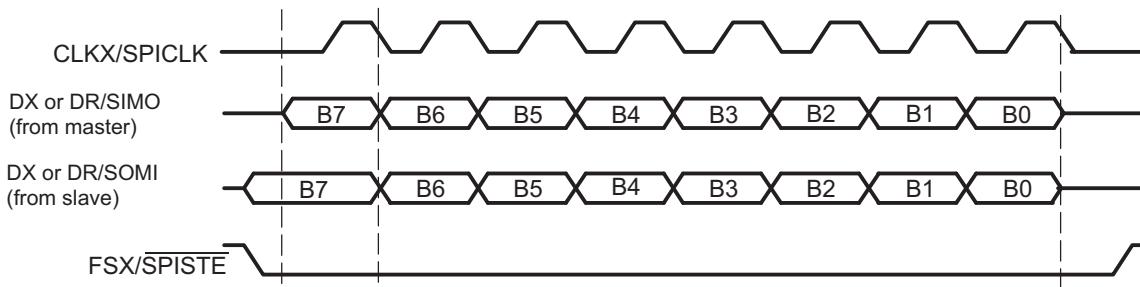
NOTE: Even if multiple words are consecutively transferred, the CLKX signal is always stopped and the FSX signal returns to the inactive state after a packet transfer. When consecutive packet transfers are performed, this leads to a minimum idle time of two bit-periods between each packet transfer.

Figure 19-37. SPI Transfer With CLKSTP = 10b (No Clock Delay), CLKXP = 0, and CLKRP = 0



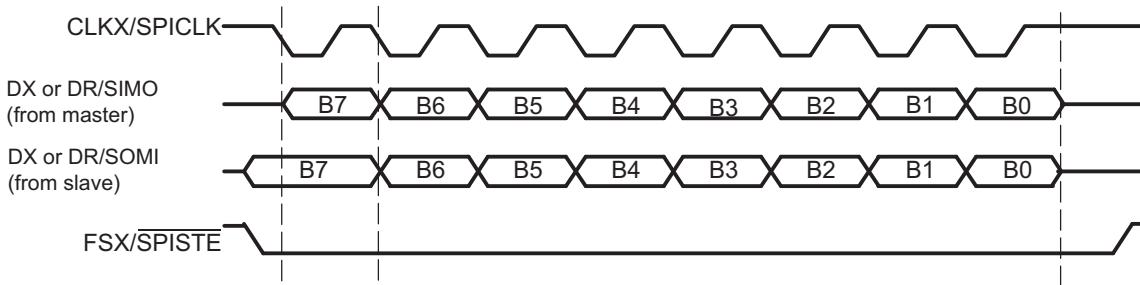
- A If the McBSP is the SPI master ($\text{CLKXM} = 1$), $\text{SIMO} = \text{DX}$. If the McBSP is the SPI slave ($\text{CLKXM} = 0$), $\text{SIMO} = \text{DR}$.
- B If the McBSP is the SPI master ($\text{CLKXM} = 1$), $\text{SOMI} = \text{DR}$. If the McBSP is the SPI slave ($\text{CLKXM} = 0$), $\text{SOMI} = \text{DX}$.

Figure 19-38. SPI Transfer With CLKSTP = 11b (Clock Delay), CLKXP = 0, CLKRP = 1



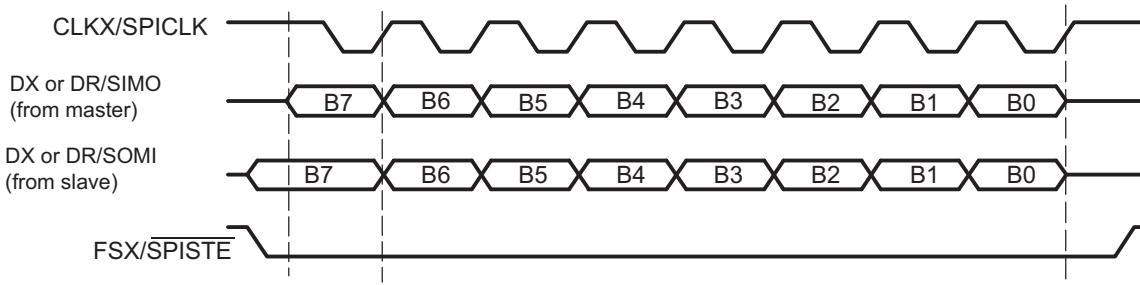
- A If the McBSP is the SPI master ($\text{CLKXM} = 1$), $\text{SIMO} = \text{DX}$. If the McBSP is the SPI slave ($\text{CLKXM} = 0$), $\text{SIMO} = \text{DR}$.
- B If the McBSP is the SPI master ($\text{CLKXM} = 1$), $\text{SOMI} = \text{DR}$. If the McBSP is the SPI slave ($\text{CLKXM} = 0$), $\text{SOMI} = \text{DX}$.

Figure 19-39. SPI Transfer With CLKSTP = 10b (No Clock Delay), CLKXP = 1, and CLKRP = 0



- A If the McBSP is the SPI master ($\text{CLKXM} = 1$), $\text{SIMO} = \text{DX}$. If the McBSP is the SPI slave ($\text{CLKXM} = 0$), $\text{SIMO} = \text{DR}$.
- B If the McBSP is the SPI master ($\text{CLKXM} = 1$), $\text{SOMI} = \text{DR}$. If the McBSP is the SPI slave ($\text{CLKXM} = 0$), $\text{SOMI} = \text{DX}$.

Figure 19-40. SPI Transfer With CLKSTP = 11b (Clock Delay), CLKXP = 1, CLKRP = 1



- A If the McBSP is the SPI master ($\text{CLKXM} = 1$), $\text{SIMO} = \text{DX}$. If the McBSP is the SPI slave ($\text{CLKXM} = 0$), $\text{SIMO} = \text{DR}$.
- B If the McBSP is the SPI master ($\text{CLKXM} = 1$), $\text{SOMI} = \text{DR}$. If the McBSP is the SPI slave ($\text{CLKXM} = 0$), $\text{SOMI} = \text{DX}$.

19.6.5 Procedure for Configuring a McBSP for SPI Operation

To configure the McBSP for SPI master or slave operation:

Step 1. Place the transmitter and receiver in reset.

Clear the transmitter reset bit ($XRST = 0$) in SPCR2 to reset the transmitter. Clear the receiver reset bit ($RRST = 0$) in SPCR1 to reset the receiver.

Step 2. Place the sample rate generator in reset.

Clear the sample rate generator reset bit ($GRST = 0$) in SPCR2 to reset the sample rate generator.

Step 3. Program registers that affect SPI operation.

Program the appropriate McBSP registers to configure the McBSP for proper operation as an SPI master or an SPI slave. For a list of important bits settings, see one of the following topics:

- *McBSP as the SPI Master* ([Section 19.6.6](#))
- *McBSP as an SPI Slave* ([Section 19.6.7](#))

Step 4. Enable the sample rate generator.

To release the sample rate generator from reset, set the sample rate generator reset bit ($GRST = 1$) in SPCR2.

Make sure that during the write to SPCR2, you only modify GRST. Otherwise, you modify the McBSP configuration you selected in the previous step.

Step 5. Enable the transmitter and receiver.

After the sample rate generator is released from reset, wait two sample rate generator clock periods for the McBSP logic to stabilize.

If the CPU services the McBSP transmit and receive buffers, then you can immediately enable the transmitter ($XRST = 1$ in SPCR2) and enable the receiver ($RRST = 1$ in SPCR1).

If the DMA controller services the McBSP transmit and receive buffers, then you must first configure the DMA controller (this includes enabling the channels that service the McBSP buffers). When the DMA controller is ready, make $XRST = 1$ and $RRST = 1$.

In either case, make sure you only change XRST and RRST when you write to SPCR2 and SPCR1. Otherwise, you modify the bit settings you selected earlier in this procedure.

After the transmitter and receiver are released from reset, wait two sample rate generator clock periods for the McBSP logic to stabilize.

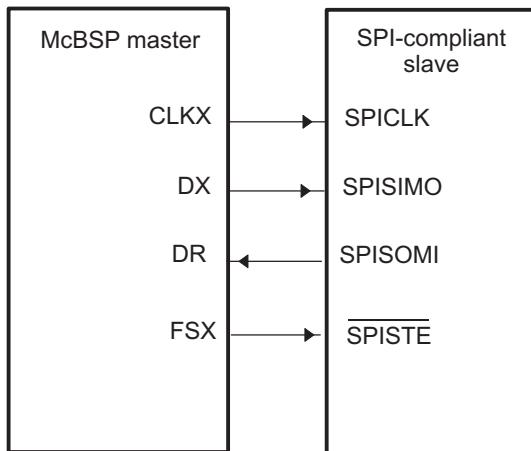
Step 6. If necessary, enable the frame-synchronization logic of the sample rate generator.

After the required data acquisition setup is done ($DXR[1,2]$ is loaded with data), set $FRST = 1$ if an internally generated frame-synchronization pulse is required (that is, if the McBSP is the SPI master).

19.6.6 McBSP as the SPI Master

An SPI interface with the McBSP used as the master is shown in [Figure 19-41](#). When the McBSP is configured as a master, the transmit output signal (DX) is used as the SPISIMO signal of the SPI protocol and the receive input signal (DR) is used as the SPISOMI signal.

The register bit values required to configure the McBSP as a master are listed in [Table 19-16](#). After the table are more details about the configuration requirements.

Figure 19-41. SPI Interface with McBSP Used as Master**Table 19-16. Bit Values Required to Configure the McBSP as an SPI Master**

Required Bit Setting	Description
CLKSTP = 10b or 11b	The clock stop mode (without or with a clock delay) is selected.
CLKXP = 0 or 1	The polarity of CLKX as seen on the MCLKX pin is positive (CLKXP = 0) or negative (CLKXP = 1).
CLKRP = 0 or 1	The polarity of MCLR as seen on the MCLR pin is positive (CLKRP = 0) or negative (CLKRP = 1).
CLKXM = 1	The MCLKX pin is an output pin driven by the internal sample rate generator. Because CLKSTP is equal to 10b or 11b, MCLR is driven internally by CLKX.
SCLKME = 0	The clock generated by the sample rate generator (CLKG) is derived from the CPU clock.
CLKSM = 1	
CLKGDV is a value from 1 to 255	CLKGDV defines the divide down value for CLKG.
FSXM = 1	The FSX pin is an output pin driven according to the FSGM bit.
FSGM = 0	The transmitter drives a frame-synchronization pulse on the FSX pin every time data is transferred from DXR1 to XSR1.
FSXP = 1	The FSX pin is active low.
XDATDLY = 01b	This setting provides the correct setup time on the FSX signal.
RDATDLY = 01b	

When the McBSP functions as the SPI master, it controls the transmission of data by producing the serial clock signal. The clock signal on the MCLKX pin is enabled only during packet transfers. When packets are not being transferred, the MCLKX pin remains high or low depending on the polarity used.

For SPI master operation, the MCLKX pin must be configured as an output. The sample rate generator is then used to derive the CLKX signal from the CPU clock. The clock stop mode internally connects the MCLKX pin to the MCLR signal so that no external signal connection is required on the MCLR pin and both the transmit and receive circuits are clocked by the master clock (CLKX).

The data delay parameters of the McBSP (XDATDLY and RDATDLY) must be set to 1 for proper SPI master operation. A data delay value of 0 or 2 is undefined in the clock stop mode.

The McBSP can also provide a slave-enable signal (SS_{_}) on the FSX pin. If a slave-enable signal is required, the FSX pin must be configured as an output and the transmitter must be configured so that a frame-synchronization pulse is generated automatically each time a packet is transmitted (FSGM = 0). The polarity of the FSX pin is programmable high or low; however, in most cases the pin must be configured active low.

When the McBSP is configured as described for SPI-master operation, the bit fields for frame-synchronization pulse width (FWID) and frame-synchronization period (FPER) are overridden, and custom frame-synchronization waveforms are not allowed. To see the resulting waveform produced on the FSX pin, see the timing diagrams in [Section 19.6.4](#). The signal becomes active before the first bit of a packet transfer, and remains active until the last bit of the packet is transferred. After the packet transfer is complete, the FSX signal returns to the inactive state.

19.6.7 McBSP as an SPI Slave

An SPI interface with the McBSP used as a slave is shown in [Figure 19-42](#). When the McBSP is configured as a slave, DX is used as the SPISOMI signal and DR is used as the SPISIMO signal.

The register bit values required to configure the McBSP as a slave are listed in [Table 19-17](#). Following the table are more details about configuration requirements.

Figure 19-42. SPI Interface With McBSP Used as Slave

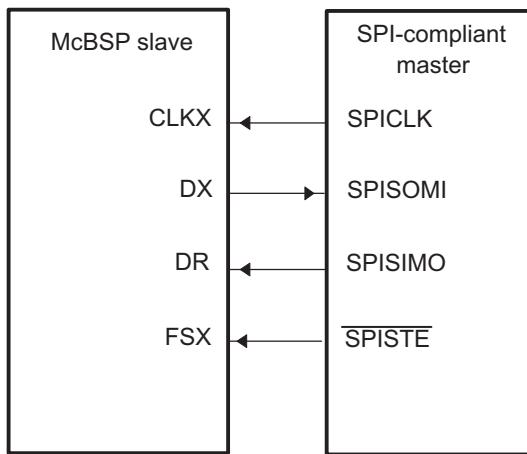


Table 19-17. Bit Values Required to Configure the McBSP as an SPI Slave

Required Bit Setting	Description
CLKSTP = 10b or 11b	The clock stop mode (without or with a clock delay) is selected.
CLKXP = 0 or 1	The polarity of CLKX as seen on the MCLKX pin is positive (CLKXP = 0) or negative (CLKXP = 1).
CLKRP = 0 or 1	The polarity of MCLKR as seen on the MCLKR pin is positive (CLKRP = 0) or negative (CLKRP = 1).
CLKXM = 0	The MCLKX pin is an input pin, so that it can be driven by the SPI master. Because CLKSTP = 10b or 11b, MCLKR is driven internally by CLKX.
SCLKME = 0	The clock generated by the sample rate generator (CLKG) is derived from the CPU clock. (The sample rate generator is used to synchronize the McBSP logic with the externally-generated master clock.)
CLKSM = 1	
CLKGDV = 1	The sample rate generator divides the CPU clock before generating CLKG.
FSXM = 0	The FSX pin is an input pin, so that it can be driven by the SPI master.
FSXP = 1	The FSX pin is active low.
XDATDLY = 00b	These bits must be 0s for SPI slave operation.
RDATDLY = 00b	

When the McBSP is used as an SPI slave, the master clock and slave-enable signals are generated externally by a master device. Accordingly, the CLKX and FSX pins must be configured as inputs. The MCLKX pin is internally connected to the MCLKR signal, so that both the transmit and receive circuits of the McBSP are clocked by the external master clock. The FSX pin is also internally connected to the FSR signal, and no external signal connections are required on the MCLKR and FSR pins.

Although the CLKX signal is generated externally by the master and is asynchronous to the McBSP, the sample rate generator of the McBSP must be enabled for proper SPI slave operation. The sample rate generator must be programmed to its maximum rate of half the CPU clock rate. The internal sample rate clock is then used to synchronize the McBSP logic to the external master clock and slave-enable signals.

The McBSP requires an active edge of the slave-enable signal on the FSX input for each transfer. This means that the master device must assert the slave-enable signal at the beginning of each transfer, and deassert the signal after the completion of each packet transfer; the slave-enable signal cannot remain active between transfers. Unlike the standard SPI, this pin cannot be tied low all the time.

The data delay parameters of the McBSP must be set to 0 for proper SPI slave operation. A value of 1 or 2 is undefined in the clock stop mode.

19.7 Receiver Configuration

To configure the McBSP receiver, perform the following procedure:

1. Place the McBSP/receiver in reset (see [Section 19.7.2](#)).
2. Program McBSP registers for the desired receiver operation (see [Section 19.7.1](#)).
3. Take the receiver out of reset (see [Section 19.7.2](#)).

19.7.1 Programming the McBSP Registers for the Desired Receiver Operation

The following is a list of important tasks to be performed when you are configuring the McBSP receiver. Each task corresponds to one or more McBSP register bit fields.

- Global behavior:
 - Set the receiver pins to operate as McBSP pins.
 - Enable/disable the digital loopback mode.
 - Enable/disable the clock stop mode.
 - Enable/disable the receive multichannel selection mode.
- Data behavior:
 - Choose 1 or 2 phases for the receive frame.
 - Set the receive word length(s).
 - Set the receive frame length.
 - Enable/disable the receive frame-synchronization ignore function.
 - Set the receive companding mode.
 - Set the receive data delay.
 - Set the receive sign-extension and justification mode.
 - Set the receive interrupt mode.
- Frame-synchronization behavior:
 - Set the receive frame-synchronization mode.
 - Set the receive frame-synchronization polarity.
 - Set the sample rate generator (SRG) frame-synchronization period and pulse width.
- Clock behavior:
 - Set the receive clock mode.
 - Set the receive clock polarity.
 - Set the SRG clock divide-down value.
 - Set the SRG clock synchronization mode.
 - Set the SRG clock mode (choose an input clock).
 - Set the SRG input clock polarity.

19.7.2 Resetting and Enabling the Receiver

The first step of the receiver configuration procedure is to reset the receiver, and the last step is to enable the receiver (to take it out of reset). [Table 19-18](#) describes the bits used for both of these steps.

Table 19-18. Register Bits Used to Reset or Enable the McBSP Receiver Field Descriptions

Register	Bit	Field	Value	Description
SPCR2	7	FRST	0	Frame-synchronization logic reset
			1	Frame-synchronization logic is reset. The sample rate generator does not generate frame-synchronization signal FSG, even if GRST = 1.
			1	If GRST = 1, frame-synchronization signal FSG is generated after (FPER + 1) number of CLKG clock cycles; all frame counters are loaded with their programmed values.
SPCR2	6	GRST	0	Sample rate generator reset
			1	Sample rate generator is enabled. CLKG is driven according to the configuration programmed in the sample rate generator registers (SRGR[1,2]). If FRST = 1, the generator also generates the frame-synchronization signal FSG as programmed in the sample rate generator registers.
SPCR1	0	RRST	0	Receiver reset
			1	The serial port receiver is disabled and in the reset state.
			1	The serial port receiver is enabled.

19.7.2.1 Reset Considerations

The serial port can be reset in the following two ways:

1. The DSP reset (\overline{XRS} signal driven low) places the receiver, transmitter, and sample rate generator in reset. When the device reset is removed (\overline{XRS} signal released), $GRST = FRST = RRST = XRST = 0$ keep the entire serial port in the reset state, provided the McBSP clock is turned on.
2. The serial port transmitter and receiver can be reset directly using the RRST and XRST bits in the serial port control registers. The sample rate generator can be reset directly using the GRST bit in SPCR2.

[Table 19-19](#) shows the state of McBSP pins when the serial port is reset due to a device reset and a direct receiver/transmitter reset.

For more details about McBSP reset conditions and effects, see [Section 19.9.2](#).

Table 19-19. Reset State of Each McBSP Pin

Pin	Possible State(s)	State Forced By Device Reset	State Forced By Receiver Reset (RRST = 0 and GRST = 1)
MDRx	I	GPIO Input	Input
MCLKRx	I/O/Z	GPIO Input	Known state if input; MCLKR running if output
MFSRx	I/O/Z	GPIO Input	Known state if input; FSRP inactive state if output
			Transmitter reset (XRST = 0 and GRST = 1)
MDXx	O/Z	GPIO Input	Low impedance after transmit bit clock provided
MCLKXx	I/O/Z	GPIO Input	Known state if input; CLKX running if output
MFSXx	I/O/Z	GPIO Input	Known state if input; FSXP inactive state if output

19.7.3 Set the Receiver Pins to Operate as McBSP Pins

To configure a pin for its McBSP function, you should configure the bits of the GPxMUXn register appropriately. In addition to this, bits 12 and 13 of the PCR register must be set to 0. These bits are defined as reserved.

19.7.4 Enable/Disable the Digital Loopback Mode

The DLB bit determines whether the digital loopback mode is on. DLB is described in [Table 19-20](#).

Table 19-20. Register Bit Used to Enable/Disable the Digital Loopback Mode

Register	Bit	Name	Function	Type	Reset Value
SPCR1	15	DLB	Digital loopback mode	R/W	0
		DLB = 0	Digital loopback mode is disabled.		
		DLB = 1	Digital loopback mode is enabled.		

19.7.4.1 Digital Loopback Mode

In the digital loopback mode, the receive signals are connected internally through multiplexers to the corresponding transmit signals, as shown in [Table 19-21](#). This mode allows testing of serial port code with a single DSP device; the McBSP receives the data it transmits.

Table 19-21. Receive Signals Connected to Transmit Signals in Digital Loopback Mode

This Receive Signal	Is Fed Internally by This Transmit Signal
MDR (receive data)	MDX (transmit data)
MFSR (receive frame synchronization)	MFSX (transmit frame synchronization)
MCLKR (receive clock)	MCLKX (transmit clock)

19.7.5 Enable/Disable the Clock Stop Mode

The CLKSTP bits determine whether the clock stop mode is on. CLKSTP is described in [Table 19-22](#).

Table 19-22. Register Bits Used to Enable/Disable the Clock Stop Mode

Register	Bit	Name	Function	Type	Reset Value
SPCR1	12-11	CLKSTP	Clock stop mode	R/W	00
			CLKSTP = 0Xb		
			Clock stop mode disabled; normal clocking for non-SPI mode		
			CLKSTP = 10b		
			Clock stop mode enabled, without clock delay		
			CLKSTP = 11b		
			Clock stop mode enabled, with clock delay		

19.7.5.1 Clock Stop Mode

The clock stop mode supports the SPI master-slave protocol. If you do not plan to use the SPI protocol, you can clear CLKSTP to disable the clock stop mode.

In the clock stop mode, the clock stops at the end of each data transfer. At the beginning of each data transfer, the clock starts immediately (CLKSTP = 10b) or after a half-cycle delay (CLKSTP = 11b). The CLKXP bit determines whether the starting edge of the clock on the MCLKX pin is rising or falling. The CLKRP bit determines whether receive data is sampled on the rising or falling edge of the clock shown on the MCLKR pin.

[Table 19-23](#) summarizes the impact of CLKSTP, CLKXP, and CLKRP on serial port operation. In the clock stop mode, the receive clock is tied internally to the transmit clock, and the receive frame-synchronization signal is tied internally to the transmit frame-synchronization signal.

Table 19-23. Effects of CLKSTP, CLKXP, and CLKRP on the Clock Scheme

Bit Settings	Clock Scheme
CLKSTP = 00b or 01b	Clock stop mode disabled. Clock enabled for non-SPI mode.
CLKXP = 0 or 1	
CLKRP = 0 or 1	
CLKSTP = 10b	Low inactive state without delay: The McBSP transmits data on the rising edge of CLKX and receives data on the falling edge of MCLKR.
CLKXP = 0	
CLKRP = 0	
CLKSTP = 11b	Low inactive state with delay: The McBSP transmits data one-half cycle ahead of the rising edge of CLKX and receives data on the rising edge of MCLKR.
CLKXP = 0	
CLKRP = 1	
CLKSTP = 10b	High inactive state without delay: The McBSP transmits data on the falling edge of CLKX and receives data on the rising edge of MCLKR.
CLKXP = 1	
CLKRP = 0	
CLKSTP = 11b	High inactive state with delay: The McBSP transmits data one-half cycle ahead of the falling edge of CLKX and receives data on the falling edge of MCLKR.
CLKXP = 1	
CLKRP = 1	

19.7.6 Enable/Disable the Receive Multichannel Selection Mode

The RMCM bit determines whether the receive multichannel selection mode is on. RMCM is described in [Table 19-24](#). For more details, see [Section 19.5.6](#).

Table 19-24. Register Bit Used to Enable/Disable the Receive Multichannel Selection Mode

Register	Bit	Name	Function	Type	Reset Value
MCR1	0	RMCM	Receive multichannel selection mode	R/W	0
			RMCM = 0 The mode is disabled. All 128 channels are enabled.		
			RMCM = 1 The mode is enabled. Channels can be individually enabled or disabled. The only channels enabled are those selected in the appropriate receive channel enable registers (RCERs). The way channels are assigned to the RCERs depends on the number of receive channel partitions (2 or 8), as defined by the RMCME bit.		

19.7.7 Choose One or Two Phases for the Receive Frame

The RPHASE bit (see [Table 19-25](#)) determines whether the receive data frame has one or two phases.

Table 19-25. Register Bit Used to Choose One or Two Phases for the Receive Frame

Register	Bit	Name	Function	Type	Reset Value
RCR2	15	RPHASE	Receive phase number	R/W	0
			Specifies whether the receive frame has 1 or 2 phases.		
			RPHASE = 0 Single-phase frame		
			RPHASE = 1 Dual-phase frame		

19.7.8 Set the Receive Word Length(s)

The RWDLEN1 and RWDLEN2 bit fields (see [Table 19-26](#)) determine how many bits are in each serial word in phase 1 and in phase 2, respectively, of the receive data frame.

Table 19-26. Register Bits Used to Set the Receive Word Length(s)

Register	Bit	Name	Function	Type	Reset Value
RCR1	7-5	RWDLEN1	Receive word length 1 Specifies the length of every serial word in phase 1 of the receive frame.	R/W	000
			RWDLEN1 = 000 8 bits		
			RWDLEN1 = 001 12 bits		
			RWDLEN1 = 010 16 bits		
			RWDLEN1 = 011 20 bits		
			RWDLEN1 = 100 24 bits		
			RWDLEN1 = 101 32 bits		
			RWDLEN1 = 11X Reserved		
RCR2	7-5	RWDLEN2	Receive word length 2 If a dual-phase frame is selected, RWDLEN2 specifies the length of every serial word in phase 2 of the frame.	R/W	000
			RWDLEN2 = 000 8 bits		
			RWDLEN2 = 001 12 bits		
			RWDLEN2 = 010 16 bits		
			RWDLEN2 = 011 20 bits		
			RWDLEN2 = 100 24 bits		
			RWDLEN2 = 101 32 bits		
			RWDLEN2 = 11X Reserved		

19.7.8.1 Word Length Bits

Each frame can have one or two phases, depending on the value that you load into the RPHASE bit. If a single-phase frame is selected, RWDLEN1 selects the length for every serial word received in the frame. If a dual-phase frame is selected, RWDLEN1 determines the length of the serial words in phase 1 of the frame and RWDLEN2 determines the word length in phase 2 of the frame.

19.7.9 Set the Receive Frame Length

The RFRLLEN1 and RFRLLEN2 bit fields (see [Table 19-27](#)) determine how many serial words are in phase 1 and in phase 2, respectively, of the receive data frame.

Table 19-27. Register Bits Used to Set the Receive Frame Length

Register	Bit	Name	Function	Type	Reset Value
RCR1	14-8	RFRLLEN1	Receive frame length 1 (RFRLLEN1 + 1) is the number of serial words in phase 1 of the receive frame.	R/W	000 0000
			RFRLLEN1 = 000 0000 1 word in phase 1		
			RFRLLEN1 = 000 0001 2 words in phase 1		
			RFRLLEN1 = 111 1111 128 words in phase 1		

Table 19-27. Register Bits Used to Set the Receive Frame Length (continued)

Register	Bit	Name	Function	Type	Reset Value
RCR2	14-8	RFRLEN2	Receive frame length 2	R/W	000 0000
			If a dual-phase frame is selected, (RFRLEN2 + 1) is the number of serial words in phase 2 of the receive frame.		
			RFRLEN2 = 000 0000	1 word in phase 2	
			RFRLEN2 = 000 0001	2 words in phase 2	
			RFRLEN2 = 111 1111	128 words in phase 2	

19.7.9.1 Selected Frame Length

The receive frame length is the number of serial words in the receive frame. Each frame can have one or two phases, depending on value that you load into the RPHASE bit.

If a single-phase frame is selected (RPHASE = 0), the frame length is equal to the length of phase 1. If a dual-phase frame is selected (RPHASE = 1), the frame length is the length of phase 1 plus the length of phase 2.

The 7-bit RFRLEN fields allow up to 128 words per phase. See [Table 19-28](#) for a summary of how to calculate the frame length. This length corresponds to the number of words or logical time slots or channels per frame-synchronization pulse.

Program the RFRLEN fields with [w minus 1], where w represents the number of words per phase. For the example, if you want a phase length of 128 words in phase 1, load 127 into RFRLEN1.

Table 19-28. How to Calculate the Length of the Receive Frame

RPHASE	RFRLEN1	RFRLEN2	Frame Length
0	0 ≤ RFRLEN1 ≤ 127	Don't care	(RFRLEN1 + 1) words
1	0 ≤ RFRLEN1 ≤ 127	0 ≤ RFRLEN2 ≤ 127	(RFRLEN1 + 1) + (RFRLEN2 + 1) words

19.7.10 Enable/Disable the Receive Frame-Synchronization Ignore Function

The RFIG bit (see [Table 19-29](#)) controls the receive frame-synchronization ignore function.

Table 19-29. Register Bit Used to Enable/Disable the Receive Frame-Synchronization Ignore Function

Register	Bit	Name	Function	Type	Reset Value
RCR2	2	RFIG	Receive frame-synchronization ignore	R/W	0
			RFIG = 0 An unexpected receive frame-synchronization pulse causes the McBSP to restart the frame transfer.		
			RFIG = 1 The McBSP ignores unexpected receive frame-synchronization pulses.		

19.7.10.1 Unexpected Frame-Synchronization Pulses and the Frame-Synchronization Ignore Function

If a frame-synchronization pulse starts the transfer of a new frame before the current frame is fully received, this pulse is treated as an unexpected frame-synchronization pulse.

When RFIG = 1, reception continues, ignoring the unexpected frame-synchronization pulses.

When RFIG = 0, an unexpected FSR pulse causes the McBSP to discard the contents of RSR[1,2] in favor of the new incoming data. Therefore, if RFIG = 0 and an unexpected frame-synchronization pulse occurs, the serial port:

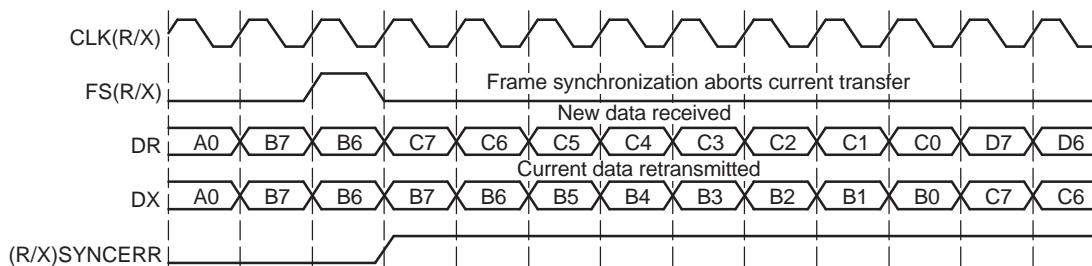
1. Aborts the current data transfer
2. Sets RSYNCERR in SPCR1 to 1
3. Begins the transfer of a new data word

For more details about the frame-synchronization error condition, see [Section 19.4.3](#).

19.7.10.2 Examples of Effects of RFIG

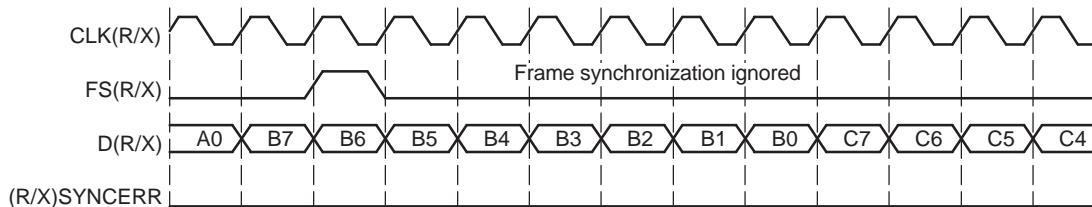
[Figure 19-43](#) shows an example in which word B is interrupted by an unexpected frame-synchronization pulse when (R/X)FIG = 0. In the case of reception, the reception of B is aborted (B is lost), and a new data word © in this example) is received after the appropriate data delay. This condition is a receive synchronization error, which sets the RSYNCERR bit.

Figure 19-43. Unexpected Frame-Synchronization Pulse With (R/X)FIG = 0



In contrast with [Figure 19-43](#), [Figure 19-44](#) shows McBSP operation when unexpected frame-synchronization signals are ignored (when (R/X)FIG = 1). Here, the transfer of word B is not affected by an unexpected pulse.

Figure 19-44. Unexpected Frame-Synchronization Pulse With (R/X)FIG = 1



19.7.11 Set the Receive Companding Mode

The RCOMPAND bits (see [Table 19-30](#)) determine whether companding or another data transfer option is chosen for McBSP reception.

Table 19-30. Register Bits Used to Set the Receive Companding Mode

Register	Bit	Name	Function	Type	Reset Value
RCR2	4-3	RCOMPAND	Receive companding mode Modes other than 00b are enabled only when the appropriate RWDLEN is 000b, indicating 8-bit data. RCOMPAND = 00 No companding, any size data, MSB received first RCOMPAND = 01 No companding, 8-bit data, LSB received first (for details, see Section 19.7.11.4). RCOMPAND = 10 µ-law companding, 8-bit data, MSB received first RCOMPAND = 11 A-law companding, 8-bit data, MSB received first	R/W	00

19.7.11.1 Companding

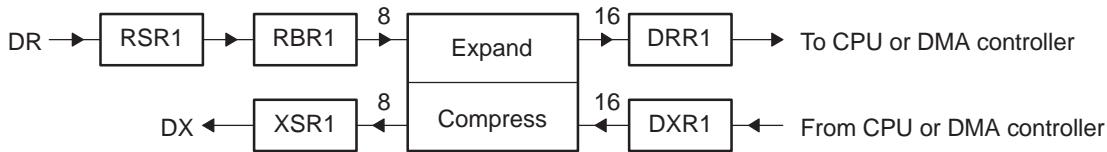
Companding (COMpressing and exPANDing) hardware allows compression and expansion of data in either μ -law or A-law format. The companding standard employed in the United States and Japan is μ -law. The European companding standard is referred to as A-law. The specifications for μ -law and A-law log PCM are part of the CCITT G.711 recommendation.

A-law and μ -law allow 13 bits and 14 bits of dynamic range, respectively. Any values outside this range are set to the most positive or most negative value. Thus, for companding to work best, the data transferred to and from the McBSP via the CPU or DMA controller must be at least 16 bits wide.

The μ -law and A-law formats both encode data into 8-bit code words. Companded data is always 8 bits wide; the appropriate word length bits (RWDLEN1, RWDLEN2, XWDLEN1, XWDLEN2) must therefore be set to 0, indicating an 8-bit wide serial data stream. If companding is enabled and either of the frame phases does not have an 8-bit word length, companding continues as if the word length is 8 bits.

[Figure 19-45](#) illustrates the companding processes. When companding is chosen for the transmitter, compression occurs during the process of copying data from DXR1 to XSR1. The transmit data is encoded according to the specified companding law (A-law or μ -law). When companding is chosen for the receiver, expansion occurs during the process of copying data from RBR1 to DRR1. The receive data is decoded to 2's-complement format.

Figure 19-45. Companding Processes for Reception and for Transmission



19.7.11.2 Format of Expanded Data

For reception, the 8-bit compressed data in RBR1 is expanded to left-justified 16-bit data in DRR1. The RJUST bit of SPCR1 is ignored when companding is used.

19.7.11.3 Companding Internal Data

If the McBSP is otherwise unused (the serial port transmit and receive sections are reset), the companding hardware can compand internal data. See [Section 19.2.2.2](#).

19.7.11.4 Option to Receive LSB First

Normally, the McBSP transmits or receives all data with the most significant bit (MSB) first. However, certain 8-bit data protocols (that do not use companded data) require the least significant bit (LSB) to be transferred first. If you set RCOMPAND = 01b in RCR2, the bit ordering of 8-bit words is reversed during reception. Similar to companding, this feature is enabled only if the appropriate word length bits are set to 0, indicating that 8-bit words are to be transferred serially. If either phase of the frame does not have an 8-bit word length, the McBSP assumes the word length is eight bits and LSB-first ordering is done.

19.7.12 Set the Receive Data Delay

The RDATDLY bits (see [Table 19-31](#)) determine the length of the data delay for the receive frame.

Table 19-31. Register Bits Used to Set the Receive Data Delay

Register	Bit	Name	Function	Type	Reset Value
RCR2	1-0	RDATDLY	Receive data delay	R/W	00
			RDATDLY = 00 0-bit data delay		
			RDATDLY = 01 1-bit data delay		
			RDATDLY = 10 2-bit data delay		
			RDATDLY = 11 Reserved		

19.7.12.1 Data Delay

The start of a frame is defined by the first clock cycle in which frame synchronization is found to be active. The beginning of actual data reception or transmission with respect to the start of the frame can be delayed if required. This delay is called data delay.

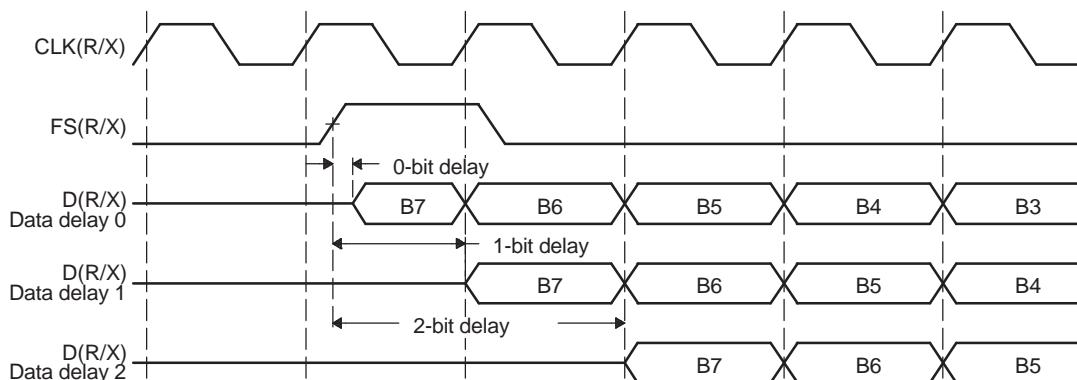
RDATDLY specifies the data delay for reception. The range of programmable data delay is zero to two bit-clocks (RDATDLY = 00b-10b), as described in [Table 19-31](#) and shown in [Figure 19-46](#). In this figure, the data transferred is an 8-bit value with bits labeled B7, B6, B5, and so on. Typically a 1-bit delay is selected, because data often follows a 1-cycle active frame-synchronization pulse.

19.7.12.2 0-Bit Data Delay

Normally, a frame-synchronization pulse is detected or sampled with respect to an edge of internal serial clock CLK(R/X). Thus, on the following cycle or later (depending on the data delay value), data may be received or transmitted. However, in the case of 0-bit data delay, the data must be ready for reception and/or transmission on the same serial clock cycle.

For reception, this problem is solved because receive data is sampled on the first falling edge of MCLKR where an active-high internal FSR is detected. However, data transmission must begin on the rising edge of the internal CLKX clock that generated the frame synchronization. Therefore, the first data bit is assumed to be present in XSR1, and thus on DX. The transmitter then asynchronously detects the frame-synchronization signal (FSX) going active high and immediately starts driving the first bit to be transmitted on the DX pin.

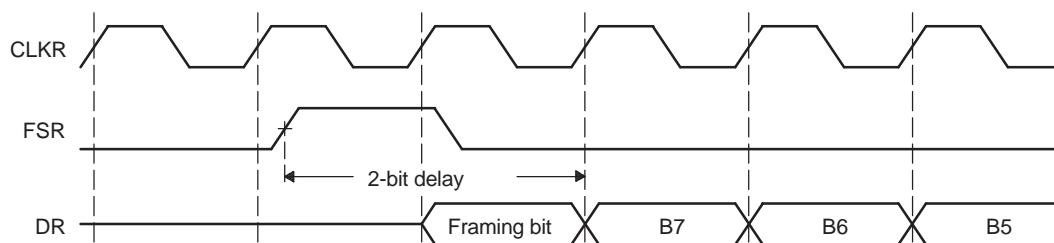
Figure 19-46. Range of Programmable Data Delay



19.7.12.3 2-Bit Data Delay

A data delay of two bit periods allows the serial port to interface to different types of T1 framing devices where the data stream is preceded by a framing bit. During reception of such a stream with data delay of two bits (framing bit appears after a 1-bit delay and data appears after a 2-bit delay), the serial port essentially discards the framing bit from the data stream, as shown in [Figure 19-47](#). In this figure, the data transferred is an 8-bit value with bits labeled B7, B6, B5, and so on.

Figure 19-47. 2-Bit Data Delay Used to Skip a Framing Bit



19.7.13 Set the Receive Sign-Extension and Justification Mode

The RJUST bits (see [Table 19-32](#)) determine whether data received by the McBSP is sign-extended and how it is justified.

Table 19-32. Register Bits Used to Set the Receive Sign-Extension and Justification Mode

Register	Bit	Name	Function	Type	Reset Value
SPCR1	14-13	RJUST	Receive sign-extension and justification mode	R/W	00
		RJUST = 00	Right justify data and zero fill MSBs in DRR[1,2]		
		RJUST = 01	Right justify data and sign extend it into the MSBs in DRR[1,2]		
		RJUST = 10	Left justify data and zero fill LSBs in DRR[1,2]		
		RJUST = 11	Reserved		

19.7.13.1 Sign-Extension and the Justification

RJUST in SPCR1 selects whether data in RBR[1,2] is right- or left-justified (with respect to the MSB) in DRR[1,2] and whether unused bits in DRR[1,2] are filled with zeros or with sign bits.

[Table 19-33](#) and [Table 19-34](#) show the effects of various RJUST values. The first table shows the effect on an example 12-bit receive-data value ABCCh. The second table shows the effect on an example 20-bit receive-data value ABCDEh.

Table 19-33. Example: Use of RJUST Field With 12-Bit Data Value ABCCh

RJUST	Justification	Extension	Value in DRR2	Value in DRR1
00b	Right	Zero fill MSBs	0000h	0ABCCh
01b	Right	Sign extend data into MSBs	FFFFh	FABCCh
10b	Left	Zero fill LSBs	0000h	ABC0h
11b	Reserved	Reserved	Reserved	Reserved

Table 19-34. Example: Use of RJUST Field With 20-Bit Data Value ABCDEh

RJUST	Justification	Extension	Value in DRR2	Value in DRR1
00b	Right	Zero fill MSBs	000Ah	BCDEh
01b	Right	Sign extend data into MSBs	FFFAh	BCDEh
10b	Left	Zero fill LSBs	ABCDh	E000h
11b	Reserved	Reserved	Reserved	Reserved

19.7.14 Set the Receive Interrupt Mode

The RINTM bits (see [Table 19-35](#)) determine which event generates a receive interrupt request to the CPU.

The receive interrupt (RINT) informs the CPU of changes to the serial port status. Four options exist for configuring this interrupt. The options are set by the receive interrupt mode bits, RINTM, in SPCR1.

Table 19-35. Register Bits Used to Set the Receive Interrupt Mode

Register	Bit	Name	Function	Type	Reset Value
SPCR1	5-4	RINTM	Receive interrupt mode	R/W	00
		RINTM = 00	RINT generated when RRDY changes from 0 to 1. Interrupt on every serial word by tracking the RRDY bit in SPCR1. Regardless of the value of RINTM, RRDY can be read to detect the RRDY = 1 condition.		
		RINTM = 01	RINT generated by an end-of-block or end-of-frame condition in the receive multichannel selection mode. In the multichannel selection mode, interrupt after every 16-channel block boundary has been crossed within a frame and at the end of the frame. For details, see Section 19.5.8 . In any other serial transfer case, this setting is not applicable and, therefore, no interrupts are generated.		
		RINTM = 10	RINT generated by a new receive frame-synchronization pulse. Interrupt on detection of receive frame-synchronization pulses. This generates an interrupt even when the receiver is in its reset state. This is done by synchronizing the incoming frame-synchronization pulse to the CPU clock and sending it to the CPU via RINT.		
		RINTM = 11	RINT generated when RSYNCERR is set. Interrupt on frame-synchronization error. Regardless of the value of RINTM, RSYNCERR can be read to detect this condition. For information on using RSYNCERR, see Section 19.4.3 .		

19.7.15 Set the Receive Frame-Synchronization Mode

The bits described in [Table 19-36](#) determine the source for receive frame synchronization and the function of the FSR pin.

19.7.15.1 Receive Frame-Synchronization Modes

[Table 19-37](#) shows how you can select various sources to provide the receive frame-synchronization signal and the effect on the FSR pin. The polarity of the signal on the FSR pin is determined by the FSOP bit.

In digital loopback mode (DLB = 1), the transmit frame-synchronization signal is used as the receive frame-synchronization signal.

Also in the clock stop mode, the internal receive clock signal (MCLKR) and the internal receive frame-synchronization signal (FSR) are internally connected to their transmit counterparts, CLKX and FSX.

Table 19-36. Register Bits Used to Set the Receive Frame Synchronization Mode

Register	Bit	Name	Function	Type	Reset Value
PCR	10	FSRM	Receive frame-synchronization mode	R/W	0
		FSRM = 0	Receive frame synchronization is supplied by an external source via the FSR pin.		
		FSRM = 1	Receive frame synchronization is supplied by the sample rate generator. FSR is an output pin reflecting internal FSR, except when GSYNC = 1 in SRGR2.		

Table 19-36. Register Bits Used to Set the Receive Frame Synchronization Mode (continued)

Register	Bit	Name	Function	Type	Reset Value
SRGR2	15	GSYNC	Sample rate generator clock synchronization mode If the sample rate generator creates a frame-synchronization signal (FSG) that is derived from an external input clock, the GSYNC bit determines whether FSG is kept synchronized with pulses on the FSR pin.	R/W	0
			GSYNC = 0 No clock synchronization is used: CLKG oscillates without adjustment, and FSG pulses every (FPER + 1) CLKG cycles.		
			GSYNC = 1 Clock synchronization is used. When a pulse is detected on the FSR pin: <ul style="list-style-type: none">• CLKG is adjusted as necessary so that it is synchronized with the input clock on the MCLKR pin.• FSG pulses FSG only pulses in response to a pulse on the FSR pin. The frame-synchronization period defined in FPER is ignored. For more details, see Section 19.3.3 .		
SPCR1	15	DLB	Digital loopback mode DLB = 0 Digital loopback mode is disabled. DLB = 1 Digital loopback mode is enabled. The receive signals, including the receive frame-synchronization signal, are connected internally through multiplexers to the corresponding transmit signals.	R/W	0
SPCR1	12-11	CLKSTP	Clock stop mode CLKSTP = 0Xb Clock stop mode disabled; normal clocking for non-SPI mode. CLKSTP = 10b Clock stop mode enabled without clock delay. The internal receive clock signal (MCLKR) and the internal receive frame-synchronization signal (FSR) are internally connected to their transmit counterparts, CLKX and FSX. CLKSTP = 11b Clock stop mode enabled with clock delay. The internal receive clock signal (MCLKR) and the internal receive frame-synchronization signal (FSR) are internally connected to their transmit counterparts, CLKX and FSX.	R/W	00

Table 19-37. Select Sources to Provide the Receive Frame-Synchronization Signal and the Effect on the FSR Pin

DLB	FSRM	GSYNC	Source of Receive Frame Synchronization	FSR Pin Status
0	0	0 or 1	An external frame-synchronization signal enters the McBSP through the FSR pin. The signal is then inverted as determined by FSRP before being used as internal FSR.	Input
0	1	0	Internal FSR is driven by the sample rate generator frame-synchronization signal (FSG).	Output. FSG is inverted as determined by FSRP before being driven out on the FSR pin.
0	1	1	Internal FSR is driven by the sample rate generator frame-synchronization signal (FSG).	Input. The external frame-synchronization input on the FSR pin is used to synchronize CLKG and generate FSG pulses.
1	0	0	Internal FSX drives internal FSR.	High impedance

Table 19-37. Select Sources to Provide the Receive Frame-Synchronization Signal and the Effect on the FSR Pin (continued)

DLB	FSRM	GSYNC	Source of Receive Frame Synchronization	FSR Pin Status
1	0 or 1	1	Internal FSX drives internal FSR.	Input. If the sample rate generator is running, external FSR is used to synchronize CLKG and generate FSG pulses.
1	1	0	Internal FSX drives internal FSR.	Output. Receive (same as transmit) frame synchronization is inverted as determined by FSRP before being driven out on the FSR pin.

19.7.16 Set the Receive Frame-Synchronization Polarity

The FSRP bit (see [Table 19-38](#)) determines whether frame-synchronization pulses are active high or active low on the FSR pin.

Table 19-38. Register Bit Used to Set Receive Frame-Synchronization Polarity

Register	Bit	Name	Function	Type	Reset Value
PCR	2	FSRP	Receive frame-synchronization polarity FSRP = 0 Frame-synchronization pulse FSR is active high. FSRP = 1 Frame-synchronization pulse FSR is active low.	R/W	0

19.7.16.1 Frame-Synchronization Pulses, Clock Signals, and Their Polarities

Receive frame-synchronization pulses can be generated internally by the sample rate generator (see [Section 19.3.2](#)) or driven by an external source. The source of frame synchronization is selected by programming the mode bit, FSRM, in PCR. FSR is also affected by the GSYNC bit in SRGR2. For information about the effects of FSRM and GSYNC, see [Section 19.7.15](#). Similarly, receive clocks can be selected to be inputs or outputs by programming the mode bit, CLKRM, in the PCR (see [Section 19.7.17](#)).

When FSR and FSX are inputs (FSXM = FSRM= 0, external frame-synchronization pulses), the McBSP detects them on the internal falling edge of clock, internal MCLKR, and internal CLKX, respectively. The receive data arriving at the DR pin is also sampled on the falling edge of internal MCLKR. These internal clock signals are either derived from an external source via CLK(R/X) pins or driven by the sample rate generator clock (CLKG) internal to the McBSP.

When FSR and FSX are outputs, implying that they are driven by the sample rate generator, they are generated (transition to their active state) on the rising edge of the internal clock, CLK(R/X). Similarly, data on the DX pin is output on the rising edge of internal CLKX.

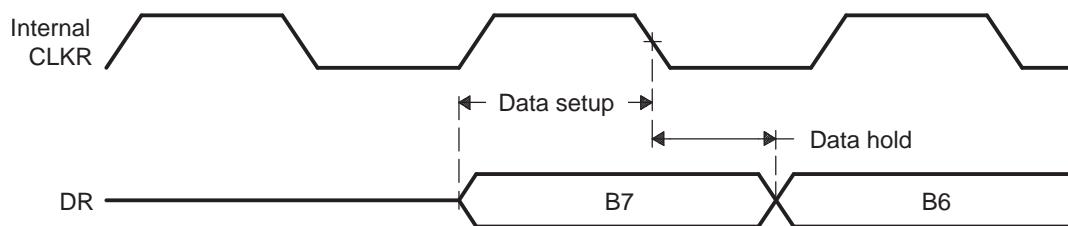
FSRP, FSXP, CLKRP, and CLKXP in the pin control register (PCR) configure the polarities of the FSR, FSX, MCLKR, and CLKX signals, respectively. All frame-synchronization signals (internal FSR, internal FSX) that are internal to the serial port are active high. If the serial port is configured for external frame synchronization (FSR/FSX are inputs to McBSP), and FSRP = FSXP = 1, the external active-low frame-synchronization signals are inverted before being sent to the receiver (internal FSR) and transmitter (internal FSX). Similarly, if internal synchronization (FSR/FSX are output pins and GSYNC = 0) is selected, the internal active-high frame-synchronization signals are inverted, if the polarity bit FS(R/X)P = 1, before being sent to the FS(R/X) pin.

On the transmit side, the transmit clock polarity bit, CLKXP, sets the edge used to shift and clock out transmit data. Data is always transmitted on the rising edge of internal CLKX. If CLKXP = 1 and external clocking is selected (CLKXM = 0 and CLKX is an input), the external falling-edge triggered input clock on CLKX is inverted to a rising-edge triggered clock before being sent to the transmitter. If CLKXP = 1, and internal clocking selected (CLKXM = 1 and CLKX is an output pin), the internal (rising-edge triggered) clock, internal CLKX, is inverted before being sent out on the MCLKX pin.

Similarly, the receiver can reliably sample data that is clocked with a rising edge clock (by the transmitter). The receive clock polarity bit, CLKRP, sets the edge used to sample received data. The receive data is always sampled on the falling edge of internal MCLKR. Therefore, if CLKRP = 1 and external clocking is selected (CLKRM = 0 and MCLKR is an input pin), the external rising-edge triggered input clock on MCLKR is inverted to a falling-edge triggered clock before being sent to the receiver. If CLKRP = 1 and internal clocking is selected (CLKRM = 1), the internal falling-edge triggered clock is inverted to a rising-edge triggered clock before being sent out on the MCLKR pin.

MCLKRP = CLKXP in a system where the same clock (internal or external) is used to clock the receiver and transmitter. The receiver uses the opposite edge as the transmitter to ensure valid setup and hold of data around this edge. [Figure 19-48](#) shows how data clocked by an external serial device using a rising edge can be sampled by the McBSP receiver on the falling edge of the same clock.

Figure 19-48. Data Clocked Externally Using a Rising Edge and Sampled by the McBSP Receiver on a Falling Edge



Set the SRG Frame-Synchronization Period and Pulse Width

19.7.16.2 Frame-Synchronization Period and the Frame-Synchronization Pulse Width

The sample rate generator can produce a clock signal, CLKG, and a frame-synchronization signal, FSG. If the sample rate generator is supplying receive or transmit frame synchronization, you must program the bit fields FPER and FWID.

On FSG, the period from the start of a frame-synchronization pulse to the start of the next pulse is (FPER + 1) CLKG cycles. The 12 bits of FPER allow a frame-synchronization period of 1 to 4096 CLKG cycles, which allows up to 4096 data bits per frame. When GSYNC = 1, FPER is a don't care value.

Each pulse on FSG has a width of (FWID + 1) CLKG cycles. The eight bits of FWID allow a pulse width of 1 to 256 CLKG cycles. It is recommended that FWID be programmed to a value less than the programmed word length.

The values in FPER and FWID are loaded into separate down-counters. The 12-bit FPER counter counts down the generated clock cycles from the programmed value (4095 maximum) to 0. The 8-bit FWID counter counts down from the programmed value (255 maximum) to 0. [Table 19-39](#) shows settings for FPER and FWID.

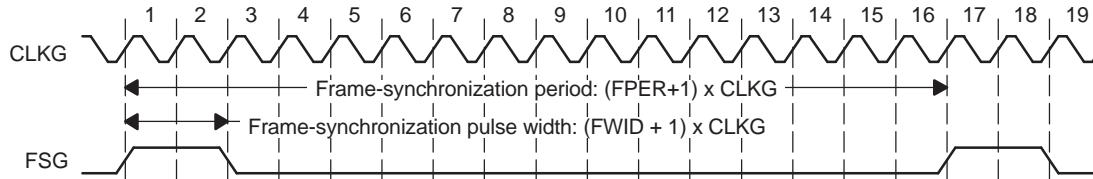
[Figure 19-49](#) shows a frame-synchronization period of 16 CLKG periods (FPER = 15 or 00001111b) and a frame-synchronization pulse with an active width of 2 CLKG periods (FWID = 1).

Table 19-39. Register Bits Used to Set the SRG Frame-Synchronization Period and Pulse Width

Register	Bit	Name	Function	Type	Reset Value
SRGR2	11-0	FPER	Sample rate generator frame-synchronization period For the frame-synchronization signal FSG, (FPER + 1) determines the period from the start of a frame-synchronization pulse to the start of the next frame-synchronization pulse. Range for (FPER + 1): 1 to 4096 CLKG cycles	R/W	0000 0000 0000
SRGR1	15-8	FWID	Sample rate generator frame-synchronization pulse width This field plus 1 determines the width of each frame-synchronization pulse on FSG.	R/W	0000 0000

Table 19-39. Register Bits Used to Set the SRG Frame-Synchronization Period and Pulse Width (continued)

Register	Bit	Name	Function	Type	Reset Value
			Range for (FWID + 1): 1 to 256 CLKG cycles		

Figure 19-49. Frame of Period 16 CLKG Periods and Active Width of 2 CLKG Periods


When the sample rate generator comes out of reset, FSG is in its inactive state. Then, when GRST = 1 and FSGM = 1, a frame-synchronization pulse is generated. The frame width value (FWID + 1) is counted down on every CLKG cycle until it reaches 0, at which time FSG goes low. At the same time, the frame period value (FPER + 1) is also counting down. When this value reaches 0, FSG goes high, indicating a new frame.

19.7.17 Set the Receive Clock Mode

Table 19-40 shows the settings for bits used to set receive clock mode.

Table 19-40. Register Bits Used to Set the Receive Clock Mode

Register	Bit	Name	Function	Type	Reset Value
PCR	8	CLKRM	Receive clock mode Case 1: Digital loopback mode not set (DLB = 0) in SPCR1. CLKRM = 0 The MCLKR pin is an input pin that supplies the internal receive clock (MCLKR). CLKRM = 1 Internal MCLKR is driven by the sample rate generator of the McBSP. The MCLKR pin is an output pin that reflects internal MCLKR. Case 2: Digital loopback mode set (DLB = 1) in SPCR1. CLKRM = 0 The MCLKR pin is in the high impedance state. The internal receive clock (MCLKR) is driven by the internal transmit clock (CLKX). Internal CLKX is derived according to the CLKXM bit of PCR. CLKRM = 1 Internal MCLKR is driven by internal CLKX. The MCLKR pin is an output pin that reflects internal MCLKR. Internal CLKX is derived according to the CLKXM bit of PCR.	R/W	0
SPCR1	15	DLB	Digital loopback mode DLB = 0 Digital loopback mode is disabled. DLB = 1 Digital loopback mode is enabled. The receive signals, including the receive frame-synchronization signal, are connected internally through multiplexers to the corresponding transmit signals.	R/W	00

Table 19-40. Register Bits Used to Set the Receive Clock Mode (continued)

Register	Bit	Name	Function	Type	Reset Value
SPCR1	12-11	CLKSTP	Clock stop mode	R/W	00
			CLKSTP = 0Xb		
			CLKSTP = 10b		
			CLKSTP = 11b		

19.7.17.1 Selecting a Source for the Receive Clock and a Data Direction for the MCLKR Pin

Table 19-41 shows how you can select various sources to provide the receive clock signal and affect the MCLKR pin. The polarity of the signal on the MCLKR pin is determined by the CLKRP bit.

In the digital loopback mode (DLB = 1), the transmit clock signal is used as the receive clock signal.

Also, in the clock stop mode, the internal receive clock signal (MCLKR) and the internal receive frame-synchronization signal (FSR) are internally connected to their transmit counterparts, CLKX and FSX.

Table 19-41. Receive Clock Signal Source Selection

DLB in SPCR1	CLKRM in PCR	Source of Receive Clock	MCLKR Pin Status
0	0	The MCLKR pin is an input driven by an external clock. The external clock signal is inverted as determined by CLKRP before being used.	Input
0	1	The sample rate generator clock (CLKG) drives internal MCLKR.	Output. CLKG, inverted as determined by CLKRP, is driven out on the MCLKR pin.
1	0	Internal CLKX drives internal MCLKR. To configure CLKX, see Section 19.8.18 .	High impedance
1	1	Internal CLKX drives internal MCLKR. To configure CLKX, see Section 19.8.18 .	Output. Internal MCLKR (same as internal CLKX) is inverted as determined by CLKRP before being driven out on the MCLKR pin.

19.7.18 Set the Receive Clock Polarity

Table 19-42. Register Bit Used to Set Receive Clock Polarity

Register	Bit	Name	Function	Type	Reset Value
PCR	0	CLKRP	Receive clock polarity	R/W	0
			CLKRP = 0 Receive data sampled on falling edge of MCLKR		
			CLKRP = 1 Receive data sampled on rising edge of MCLKR		

19.7.18.1 Frame Synchronization Pulses, Clock Signals, and Their Polarities

Receive frame-synchronization pulses can be generated internally by the sample rate generator (see [Section 19.3.2](#)) or driven by an external source. The source of frame synchronization is selected by programming the mode bit, FSRM, in PCR. FSR is also affected by the GSYNC bit in SRGR2. For information about the effects of FSRM and GSYNC, see [Section 19.7.15](#). Similarly, receive clocks can be selected to be inputs or outputs by programming the mode bit, CLKRM, in the PCR (see [Section 19.7.17](#)).

When FSR and FSX are inputs (FSXM = FSRM = 0, external frame-synchronization pulses), the McBSP detects them on the internal falling edge of clock, internal MCLKR, and internal CLKX, respectively. The receive data arriving at the DR pin is also sampled on the falling edge of internal MCLKR. These internal clock signals are either derived from external source via CLK(R/X) pins or driven by the sample rate generator clock (CLKG) internal to the McBSP.

When FSR and FSX are outputs, implying that they are driven by the sample rate generator, they are generated (transition to their active state) on the rising edge of internal clock, CLK(R/X). Similarly, data on the DX pin is output on the rising edge of internal CLKX.

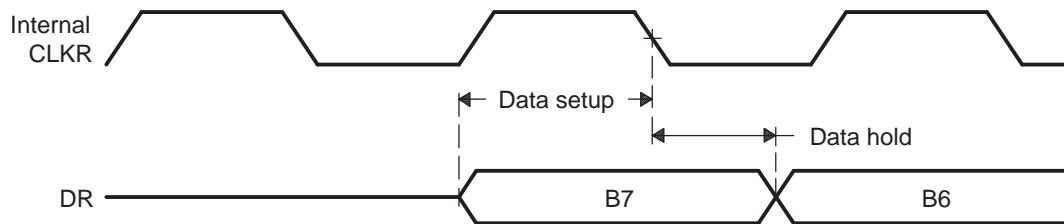
FSRP, FSXP, CLKRP, and CLKXP in the pin control register (PCR) configure the polarities of the FSR, FSX, MCLKR, and CLKX signals, respectively. All frame-synchronization signals (internal FSR, internal FSX) that are internal to the serial port are active high. If the serial port is configured for external frame synchronization (FSR/FSX are inputs to McBSP) and FSRP = FSXP = 1, the external active-low frame-synchronization signals are inverted before being sent to the receiver (internal FSR) and transmitter (internal FSX). Similarly, if internal synchronization (FSR/FSX are output pins and GSYNC = 0) is selected, the internal active-high frame-synchronization signals are inverted, if the polarity bit FS(R/X)P = 1, before being sent to the FS(R/X) pin.

On the transmit side, the transmit clock polarity bit, CLKXP, sets the edge used to shift and clock out transmit data. Data is always transmitted on the rising edge of internal CLKX. If CLKXP = 1 and external clocking is selected (CLKXM = 0 and CLKX is an input), the external falling-edge triggered input clock on CLKX is inverted to a rising-edge triggered clock before being sent to the transmitter. If CLKXP = 1 and internal clocking is selected (CLKXM = 1 and CLKX is an output pin), the internal (rising-edge triggered) clock, internal CLKX, is inverted before being sent out on the MCLKX pin.

Similarly, the receiver can reliably sample data that is clocked with a rising edge clock (by the transmitter). The receive clock polarity bit, CLKRP, sets the edge used to sample received data. The receive data is always sampled on the falling edge of internal MCLKR. Therefore, if CLKRP = 1 and external clocking is selected (CLKRM = 0 and MCLKR is an input pin), the external rising-edge triggered input clock on MCLKR is inverted to a falling-edge triggered clock before being sent to the receiver. If CLKRP = 1 and internal clocking is selected (CLKRM = 1), the internal falling-edge triggered clock is inverted to a rising-edge triggered clock before being sent out on the MCLKR pin.

CLKRP = CLKXP in a system where the same clock (internal or external) is used to clock the receiver and transmitter. The receiver uses the opposite edge as the transmitter to ensure valid setup and hold of data around this edge. [Figure 19-50](#) shows how data clocked by an external serial device using a rising edge can be sampled by the McBSP receiver on the falling edge of the same clock.

Figure 19-50. Data Clocked Externally Using a Rising Edge and Sampled by the McBSP Receiver on a Falling Edge



19.7.19 Set the SRG Clock Divide-Down Value

Table 19-43. Register Bits Used to Set the Sample Rate Generator (SRG) Clock Divide-Down Value

Register	Bit	Name	Function	Type	Reset Value
SRGR1	7-0	CLKGDV	Sample rate generator clock divide-down value The input clock of the sample rate generator is divided by (CLKGDV + 1) to generate the required sample rate generator clock frequency. The default value of CLKGDV is 1 (divide input clock by 2).	R/W	0000 0001

19.7.19.1 Sample Rate Generator Clock Divider

The first divider stage generates the serial data bit clock from the input clock. This divider stage utilizes a counter, preloaded by CLKGDV, that contains the divide ratio value.

The output of the first divider stage is the data bit clock, which is output as CLKG and which serves as the input for the second and third stages of the divider.

CLKG has a frequency equal to $1/(CLKGDV + 1)$ of sample rate generator input clock. Thus, the sample generator input clock frequency is divided by a value between 1 and 256. When CLKGDV is odd or equal to 0, the CLKG duty cycle is 50%. When CLKGDV is an even value, $2p$, representing an odd divide-down, the high-state duration is $p + 1$ cycles and the low-state duration is p cycles.

19.7.20 Set the SRG Clock Synchronization Mode

For more details on using the clock synchronization feature, see [Section 19.3.3](#).

Table 19-44. Register Bit Used to Set the SRG Clock Synchronization Mode

Register	Bit	Name	Function	Type	Reset Value
SRGR2	15	GSYNC	Sample rate generator clock synchronization GSYNC is used only when the input clock source for the sample rate generator is external—on the MCLKR or MCLKX pin. GSYNC = 0 The sample rate generator clock (CLKG) is free running. CLKG oscillates without adjustment, and FSG pulses every (FPER + 1) CLKG cycles. GSYNC = 1 Clock synchronization is performed. When a pulse is detected on the FSR pin: <ul style="list-style-type: none">• CLKG is adjusted as necessary so that it is synchronized with the input clock on the MCLKR or MCLKX pin.• FSG pulses. FSG only pulses in response to a pulse on the FSR pin. The frame-synchronization period defined in FPER is ignored.	R/W	0

19.7.21 Set the SRG Clock Mode (Choose an Input Clock)**Table 19-45. Register Bits Used to Set the SRG Clock Mode (Choose an Input Clock)**

Register	Bit	Name	Function	Type	Reset Value
PCR	7	SCLKME	Sample rate generator clock mode	R/W	0
SRGR2	13	CLKSM	SCLKME = 0 Reserved CLKSM = 0 SCLKME = 0 Sample rate generator clock derived from LSPCLK (default) CLKSM = 1	R/W	1

Table 19-45. Register Bits Used to Set the SRG Clock Mode (Choose an Input Clock) (continued)

Register	Bit	Name	Function	Type	Reset Value
		SCLKME = 1 CLKSM = 0	Sample rate generator clock derived from MCLKR pin		
		SCLKME = 1 CLKSM = 1	Sample rate generator clock derived from MCLKX pin		

19.7.21.1 SRG Clock Mode

The sample rate generator can produce a clock signal (CLKG) for use by the receiver, the transmitter, or both, but CLKG is derived from an input clock. [Table 19-45](#) shows the four possible sources of the input clock. For more details on generating CLKG, see [Section 19.3.1.1](#).

19.7.22 Set the SRG Input Clock Polarity

Table 19-46. Register Bits Used to Set the SRG Input Clock Polarity

Register	Bit	Name	Function	Type	Reset Value
PCR	1	CLKXP	MCLKX pin polarity	R/W	0
			CLKXP determines the input clock polarity when the MCLKX pin supplies the input clock (SCLKME = 1 and CLKSM = 1).		
			CLKXP = 0 Rising edge on MCLKX pin generates transitions on CLKG and FSG.		
			CLKXP = 1 Falling edge on MCLKX pin generates transitions on CLKG and FSG.		
PCR	0	CLKRP	MCLKR pin polarity	R/W	0
			CLKRP determines the input clock polarity when the MCLKR pin supplies the input clock (SCLKME = 1 and CLKSM = 0).		
			CLKRP = 0 Falling edge on MCLKR pin generates transitions on CLKG and FSG.		
			CLKRP = 1 Rising edge on MCLKR pin generates transitions on CLKG and FSG.		

19.7.22.1 Using CLKXP/CLKRP to Choose an Input Clock Polarity

The sample rate generator can produce a clock signal (CLKG) and a frame-synchronization signal (FSG) for use by the receiver, the transmitter, or both. To produce CLKG and FSG, the sample rate generator must be driven by an input clock signal derived from the CPU clock or from an external clock on the CLKX or MCLKR pin. If you use a pin, choose a polarity for that pin by using the appropriate polarity bit (CLKXP for the MCLKX pin, CLKRP for the MCLKR pin). The polarity determines whether the rising or falling edge of the input clock generates transitions on CLKG and FSG.

19.8 Transmitter Configuration

To configure the McBSP transmitter, perform the following procedure:

1. Place the McBSP/transmitter in reset (see [Section 19.8.2](#)).
2. Program the McBSP registers for the desired transmitter operation (see [Section 19.8.1](#)).
3. Take the transmitter out of reset (see [Section 19.8.2](#)).

19.8.1 Programming the McBSP Registers for the Desired Transmitter Operation

The following is a list of important tasks to be performed when you are configuring the McBSP transmitter. Each task corresponds to one or more McBSP register bit fields.

- Global behavior:
 - Set the transmitter pins to operate as McBSP pins.
 - Enable/disable the digital loopback mode.
 - Enable/disable the clock stop mode.
 - Enable/disable transmit multichannel selection.
- Data behavior:
 - Choose 1 or 2 phases for the transmit frame.
 - Set the transmit word length(s).
 - Set the transmit frame length.
 - Enable/disable the transmit frame-synchronization ignore function.
 - Set the transmit companding mode.
 - Set the transmit data delay.

- Set the transmit DXENA mode.
- Set the transmit interrupt mode.
- Frame-synchronization behavior:
 - Set the transmit frame-synchronization mode.
 - Set the transmit frame-synchronization polarity.
 - Set the SRG frame-synchronization period and pulse width.
- Clock behavior:
 - Set the transmit clock mode.
 - Set the transmit clock polarity.
 - Set the SRG clock divide-down value.
 - Set the SRG clock synchronization mode.
 - Set the SRG clock mode (choose an input clock).
 - Set the SRG input clock polarity.

19.8.2 Resetting and Enabling the Transmitter

The first step of the transmitter configuration procedure is to reset the transmitter, and the last step is to enable the transmitter (to take it out of reset). [Table 19-47](#) describes the bits used for both of these steps.

Table 19-47. Register Bits Used to Place Transmitter in Reset Field Descriptions

Register	Bit	Field	Value	Description
SPCR2	7	FRST	0	Frame-synchronization logic reset
			1	Frame-synchronization logic is reset. The sample rate generator does not generate frame-synchronization signal FSG, even if GRST = 1.
SPCR2	6	GRST	0	Sample rate generator reset
			1	Sample rate generator is reset. If GRST = 0 due to a device reset, CLKG is driven by the CPU clock divided by 2, and FSG is driven low (inactive). If GRST = 0 due to program code, CLKG and FSG are both driven low (inactive).
SPCR2	0	XRST	0	Transmitter reset
			1	The serial port transmitter is disabled and in the reset state.
				The serial port transmitter is enabled.

19.8.2.1 Reset Considerations

The serial port can be reset in the following two ways:

1. A DSP reset (~~XRS~~ signal driven low) places the receiver, transmitter, and sample rate generator in reset. When the device reset is removed, GRST = FRST = RRST = XRST = 0, keeping the entire serial port in the reset state.
2. The serial port transmitter and receiver can be reset directly using the RRST and XRST bits in the serial port control registers. The sample rate generator can be reset directly using the GRST bit in SPCR2.
3. When using the DMA, the order in which McBSP events must occur is important. DMA channel and peripheral interrupts must be configured prior to releasing the McBSP transmitter from reset.

The reason for this is that an XRDY is fired when XRST = 1. The XRDY signals the DMA to start copying data from the buffer into the transmit register. If the McBSP transmitter is released from reset before the DMA channel and peripheral interrupts are configured, the XRDY signals before the DMA channel can receive the signal; therefore, the DMA does not move the data from the buffer to the

transmit register. The DMA PERINTFLG is edge-sensitive and will fail to recognize the XRDY, which is continuously high.

For more details about McBSP reset conditions and effects, see [Section 19.9.2](#).

19.8.3 Set the Transmitter Pins to Operate as McBSP Pins

To configure a pin for its McBSP function , you should configure the bits of the GPxMUXn register appropriately. In addition to this, bits 12 and 13 of the PCR register must be set to 0. These bits are defined as reserved.

19.8.4 Enable/Disable the Digital Loopback Mode

The DLB bit determines whether the digital loopback mode is on. DLB is described in [Table 19-48](#).

Table 19-48. Register Bit Used to Enable/Disable the Digital Loopback Mode

Register	Bit	Name	Function	Type	Reset Value
SPCR1	15	DLB	Digital loopback mode	R/W	0
		DLB = 0	Digital loopback mode is disabled.		
		DLB = 1	Digital loopback mode is enabled.		

19.8.4.1 Digital Loopback Mode

In the digital loopback mode, the receive signals are connected internally through multiplexers to the corresponding transmit signals, as shown in [Table 19-49](#). This mode allows testing of serial port code with a single DSP device; the McBSP receives the data it transmits.

Table 19-49. Receive Signals Connected to Transmit Signals in Digital Loopback Mode

This Receive Signal	Is Fed Internally by This Transmit Signal
DR (receive data)	DX (transmit data)
FSR (receive frame synchronization)	FSX (transmit frame synchronization)
MCLKR (receive clock)	CLKX (transmit clock)

19.8.5 Enable/Disable the Clock Stop Mode

The CLKSTP bits determine whether the clock stop mode is on. CLKSTP is described in [Table 19-50](#).

Table 19-50. Register Bits Used to Enable/Disable the Clock Stop Mode

Register	Bit	Name	Function	Type	Reset Value
SPCR1	12-11	CLKSTP	Clock stop mode	R/W	00
			CLKSTP = 0xb		
			Clock stop mode disabled; normal clocking for non-SPI mode.		
			CLKSTP = 10b		
			Clock stop mode enabled without clock delay		
			CLKSTP = 11b		
			Clock stop mode enabled with clock delay		

19.8.5.1 Clock Stop Mode

The clock stop mode supports the SPI master-slave protocol. If you do not plan to use the SPI protocol, you can clear CLKSTP to disable the clock stop mode.

In the clock stop mode, the clock stops at the end of each data transfer. At the beginning of each data transfer, the clock starts immediately (CLKSTP = 10b) or after a half-cycle delay (CLKSTP = 11b). The CLKXP bit determines whether the starting edge of the clock on the MCLKX pin is rising or falling. The CLKRP bit determines whether receive data is sampled on the rising or falling edge of the clock shown on the MCLKR pin.

Table 19-51 summarizes the impact of CLKSTP, CLKXP, and CLKRP on serial port operation. In the clock stop mode, the receive clock is tied internally to the transmit clock, and the receive frame-synchronization signal is tied internally to the transmit frame-synchronization signal.

Table 19-51. Effects of CLKSTP, CLKXP, and CLKRP on the Clock Scheme

Bit Settings	Clock Scheme
CLKSTP = 00b or 01b	Clock stop mode disabled. Clock enabled for non-SPI mode.
CLKXP = 0 or 1	
CLKRP = 0 or 1	
CLKSTP = 10b CLKXP = 0	Low inactive state without delay: The McBSP transmits data on the rising edge of CLKX and receives data on the falling edge of MCLKR.
CLKRP = 0	
CLKSTP = 11b CLKXP = 0	Low inactive state with delay: The McBSP transmits data one-half cycle ahead of the rising edge of CLKX and receives data on the rising edge of MCLKR.
CLKRP = 1	
CLKSTP = 10b CLKXP = 1	High inactive state without delay: The McBSP transmits data on the falling edge of CLKX and receives data on the rising edge of MCLKR.
CLKRP = 0	
CLKSTP = 11b CLKXP = 1	High inactive state with delay: The McBSP transmits data one-half cycle ahead of the falling edge of CLKX and receives data on the falling edge of MCLKR.
CLKRP = 1	

19.8.6 Enable/Disable Transmit Multichannel Selection

For more details, see [Section 19.5.7](#).

Table 19-52. Register Bits Used to Enable/Disable Transmit Multichannel Selection

Register	Bit	Name	Function	Type	Reset Value
MCR2	1-0	XMCM	Transmit multichannel selection	R/W	00
		XMCM = 00b	No transmit multichannel selection mode is on. All channels are enabled and unmasked. No channels can be disabled or masked.		
		XMCM = 01b	All channels are disabled unless they are selected in the appropriate transmit channel enable registers (XCERs). If enabled, a channel in this mode is also unmasked. The XMCME bit determines whether 32 channels or 128 channels are selectable in XCERs.		
		XMCM = 10b	All channels are enabled, but they are masked unless they are selected in the appropriate transmit channel enable registers (XCERs). The XMCME bit determines whether 32 channels or 128 channels are selectable in XCERs.		
		XMCM = 11b	This mode is used for symmetric transmission and reception. All channels are disabled for transmission unless they are enabled for reception in the appropriate receive channel enable registers (RCERs). Once enabled, they are masked unless they are also selected in the appropriate transmit channel enable registers (XCERs). The XMCME bit determines whether 32 channels or 128 channels are selectable in RCERs and XCERs.		

19.8.7 Choose One or Two Phases for the Transmit Frame

Table 19-53. Register Bit Used to Choose 1 or 2 Phases for the Transmit Frame

Register	Bit	Name	Function	Type	Reset Value
XCR2	15	XPHASE	Transmit phase number Specifies whether the transmit frame has 1 or 2 phases. XPHASE = 0 Single-phase frame XPHASE = 1 Dual-phase frame	R/W	0

19.8.8 Set the Transmit Word Length(s)

Table 19-54. Register Bits Used to Set the Transmit Word Length(s)

Register	Bit	Name	Function	Type	Reset Value
XCR1	7-5	XWDLEN1	Transmit word length of frame phase 1 XWDLEN1 = 000b 8 bits XWDLEN1 = 001b 12 bits XWDLEN1 = 010b 16 bits XWDLEN1 = 011b 20 bits XWDLEN1 = 100b 24 bits XWDLEN1 = 101b 32 bits XWDLEN1 = 11Xb Reserved	R/W	000
XCR2	7-5	XWDLEN2	Transmit word length of frame phase 2 XWDLEN2 = 000b 8 bits XWDLEN2 = 001b 12 bits XWDLEN2 = 010b 16 bits XWDLEN2 = 011b 20 bits XWDLEN2 = 100b 24 bits XWDLEN2 = 101b 32 bits XWDLEN2 = 11Xb Reserved	R/W	000

19.8.8.1 Word Length Bits

Each frame can have one or two phases, depending on the value that you load into the RPHASE bit. If a single-phase frame is selected, XWDLEN1 selects the length for every serial word transmitted in the frame. If a dual-phase frame is selected, XWDLEN1 determines the length of the serial words in phase 1 of the frame, and XWDLEN2 determines the word length in phase 2 of the frame.

19.8.9 Set the Transmit Frame Length

Table 19-55. Register Bits Used to Set the Transmit Frame Length

Register	Bit	Name	Function	Type	Reset Value
XCR1	14-8	XFRLEN1	Transmit frame length 1 (XFRLEN1 + 1) is the number of serial words in phase 1 of the transmit frame. XFRLEN1 = 000 0000 1 word in phase 1 XFRLEN1 = 000 0001 2 words in phase 1 XFRLEN1 = 111 1111 128 words in phase 1	R/W	000 0000
XCR2	14-8	XFRLEN2	Transmit frame length 2 If a dual-phase frame is selected, (XFRLEN2 + 1) is the number of serial words in phase 2 of the transmit frame. XFRLEN2 = 000 0000 1 word in phase 2 XFRLEN2 = 000 0001 2 words in phase 2 XFRLEN2 = 111 1111 128 words in phase 2	R/W	000 0000

19.8.9.1 Selected Frame Length

The transmit frame length is the number of serial words in the transmit frame. Each frame can have one or two phases, depending on the value that you load into the XPHASE bit.

If a single-phase frame is selected (XPHASE = 0), the frame length is equal to the length of phase 1. If a dual-phase frame is selected (XPHASE = 1), the frame length is the length of phase 1 plus the length of phase 2.

The 7-bit XFRLEN fields allow up to 128 words per phase. See [Table 19-56](#) for a summary of how to calculate the frame length. This length corresponds to the number of words or logical time slots or channels per frame-synchronization pulse.

NOTE: Program the XFRLEN fields with [w minus 1], where w represents the number of words per phase. For example, if you want a phase length of 128 words in phase 1, load 127 into XFRLEN1.

Table 19-56. How to Calculate Frame Length

XPHASE	XFRLEN1	XFRLEN2	Frame Length
0	$0 \leq \text{XFRLEN1} \leq 127$	Don't care	(XFRLEN1 + 1) words
1	$0 \leq \text{XFRLEN1} \leq 127$	$0 \leq \text{XFRLEN2} \leq 127$	(XFRLEN1 + 1) + (XFRLEN2 + 1) words

19.8.10 Enable/Disable the Transmit Frame-Synchronization Ignore Function

Table 19-57. Register Bit Used to Enable/Disable the Transmit Frame-Synchronization Ignore Function

Register	Bit	Name	Function	Type	Reset Value
XCR2	2	XFIG	Transmit frame-synchronization ignore	R/W	0
			XFIG = 0 An unexpected transmit frame-synchronization pulse causes the McBSP to restart the frame transfer.		
			XFIG = 1 The McBSP ignores unexpected transmit frame-synchronization pulses.		

19.8.10.1 Unexpected Frame-Synchronization Pulses and Frame-Synchronization Ignore

If a frame-synchronization pulse starts the transfer of a new frame before the current frame is fully transmitted, this pulse is treated as an unexpected frame-synchronization pulse.

When XFIG = 1, normal transmission continues with unexpected frame-synchronization signals ignored.

When XFIG = 0 and an unexpected frame-synchronization pulse occurs, the serial port:

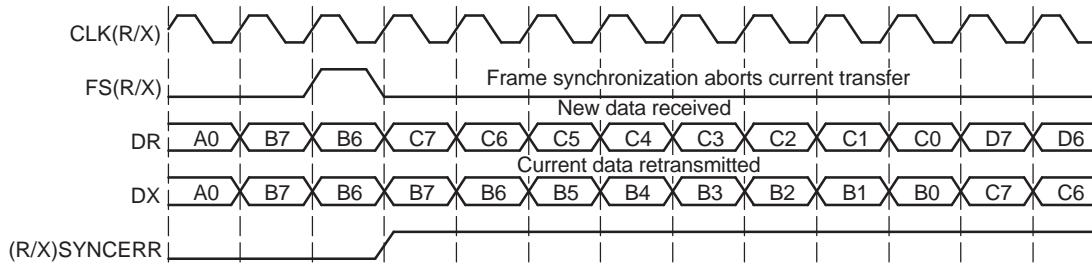
1. Aborts the present transmission
2. Sets XSYNCERR to 1 in SPCR2
3. Reinitiates transmission of the current word that was aborted

For more details about the frame-synchronization error condition, see [Section 19.4.6](#).

19.8.10.2 Examples Showing the Effects of XFIG

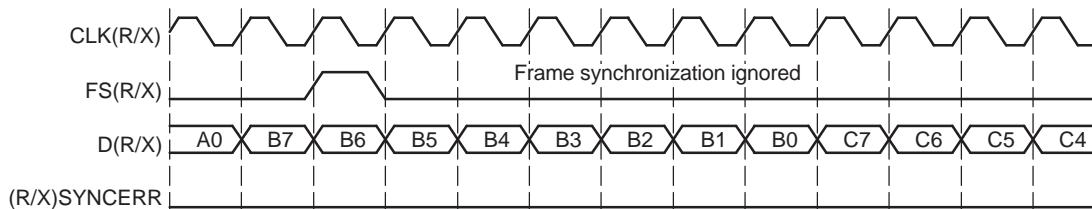
[Figure 19-51](#) shows an example in which word B is interrupted by an unexpected frame-synchronization pulse when (R/X)FIG = 0. In the case of transmission, the transmission of B is aborted (B is lost). This condition is a transmit synchronization error, which sets the XSYNCERR bit. No new data has been written to DXR[1,2]; therefore, the McBSP transmits B again.

Figure 19-51. Unexpected Frame-Synchronization Pulse With (R/X) FIG = 0



In contrast with [Figure 19-51](#), [Figure 19-52](#) shows McBSP operation when unexpected frame-synchronization signals are ignored (when (R/X)FIG = 1). Here, the transfer of word B is not affected by an unexpected frame-synchronization pulse.

Figure 19-52. Unexpected Frame-Synchronization Pulse With (R/X) FIG = 1



19.8.11 Set the Transmit Companding Mode

Table 19-58. Register Bits Used to Set the Transmit Companding Mode

Register	Bit	Name	Function	Type	Reset Value
XCR2	4-3	XCOMPAND	Transmit companding mode	R/W	00
			Modes other than 00b are enabled only when the appropriate XWDLEN is 000b, indicating 8-bit data.		
		XCOMPAND = 00b	No companding, any size data, MSB transmitted first		
		XCOMPAND = 01b	No companding, 8-bit data, LSB transmitted first (for details, see Section 19.7.11.4, Option to Receive LSB First)		
		XCOMPAND = 10b	μ -law companding, 8-bit data, MSB transmitted first		
		XCOMPAND = 11b	A-law companding, 8-bit data, MSB transmitted first		

19.8.11.1 Companding

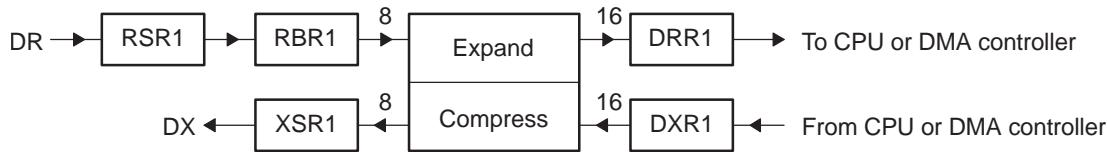
Companding (COMpressing and exPANDING) hardware allows compression and expansion of data in either μ -law or A-law format. The companding standard employed in the United States and Japan is μ -law. The European companding standard is referred to as A-law. The specifications for μ -law and A-law log PCM are part of the CCITT G.711 recommendation.

A-law and μ -law allow 13 bits and 14 bits of dynamic range, respectively. Any values outside this range are set to the most positive or most negative value. Thus, for companding to work best, the data transferred to and from the McBSP via the CPU or DMA controller must be at least 16 bits wide.

The μ -law and A-law formats both encode data into 8-bit code words. Companded data is always 8 bits wide; the appropriate word length bits (RWDLEN1, RWDLEN2, XWDLEN1, XWDLEN2) must therefore be set to 0, indicating an 8-bit wide serial data stream. If companding is enabled and either of the frame phases does not have an 8-bit word length, companding continues as if the word length is 8 bits.

[Figure 19-53](#) illustrates the companding processes. When companding is chosen for the transmitter, compression occurs during the process of copying data from DXR1 to XSR1. The transmit data is encoded according to the specified companding law (A-law or μ -law). When companding is chosen for the receiver, expansion occurs during the process of copying data from RBR1 to DRR1. The receive data is decoded to two's-complement format.

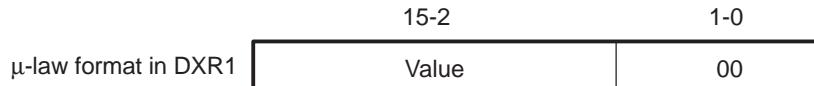
Figure 19-53. Companding Processes for Reception and for Transmission



19.8.11.2 Format for Data To Be Compressed

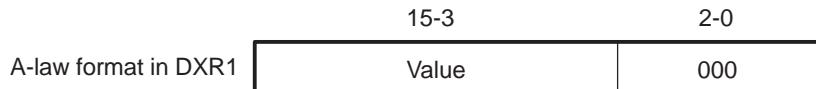
For transmission using μ -law compression, make sure the 14 data bits are left-justified in DXR1, with the remaining two low-order bits filled with 0s as shown in [Figure 19-54](#).

Figure 19-54. μ -Law Transmit Data Companding Format



For transmission using A-law compression, make sure the 13 data bits are left-justified in DXR1, with the remaining three low-order bits filled with 0s as shown in [Figure 19-55](#).

Figure 19-55. A-Law Transmit Data Companding Format



19.8.11.3 Capability to Compand Internal Data

If the McBSP is otherwise unused (the serial port transmit and receive sections are reset), the companding hardware can compand internal data. See [Section 19.2.2.2, Capability to Compand Internal Data](#).

19.8.11.4 Option to Transmit LSB First

Normally, the McBSP transmit or receives all data with the most significant bit (MSB) first. However, certain 8-bit data protocols (that do not use companded data) require the least significant bit (LSB) to be transferred first. If you set XCOMPAND = 01b in XCR2, the bit ordering of 8-bit words is reversed (LSB first) before being sent from the serial port. Similar to companding, this feature is enabled only if the appropriate word length bits are set to 0, indicating that 8-bit words are to be transferred serially. If either phase of the frame does not have an 8-bit word length, the McBSP assumes the word length is eight bits and LSB-first ordering is done.

19.8.12 Set the Transmit Data Delay

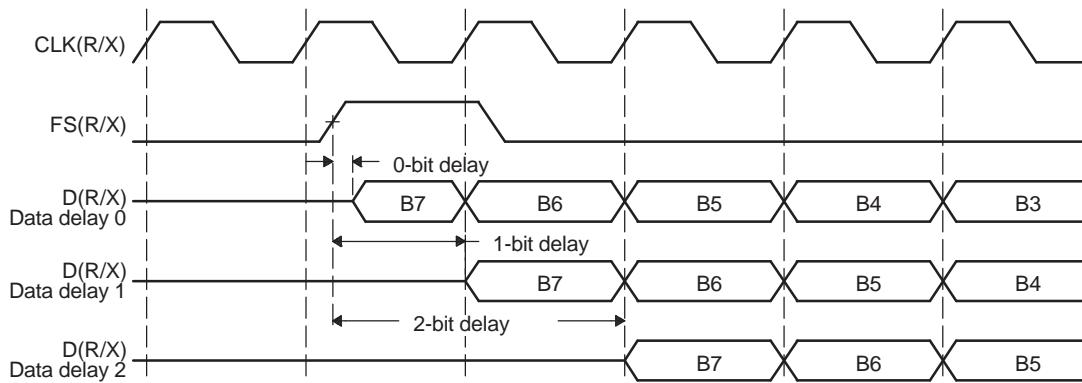
Table 19-59. Register Bits Used to Set the Transmit Data Delay

Register	Bit	Name	Function	Type	Reset Value
XCR2	1-0	XDATDLY	Transmitter data delay	R/W	00
			XDATDLY = 00 0-bit data delay		
			XDATDLY = 01 1-bit data delay		
			XDATDLY = 10 2-bit data delay		
			XDATDLY = 11 Reserved		

19.8.12.1 Data Delay

The start of a frame is defined by the first clock cycle in which frame synchronization is found to be active. The beginning of actual data reception or transmission with respect to the start of the frame can be delayed if necessary. This delay is called data delay.

XDATDLY specifies the data delay for transmission. The range of programmable data delay is zero to two bit-clocks (XDATDLY = 00b-10b), as described in [Table 19-59](#) and [Figure 19-56](#). In this figure, the data transferred is an 8-bit value with bits labeled B7, B6, B5, and so on. Typically a 1-bit delay is selected, because data often follows a 1-cycle active frame-synchronization pulse.

Figure 19-56. Range of Programmable Data Delay

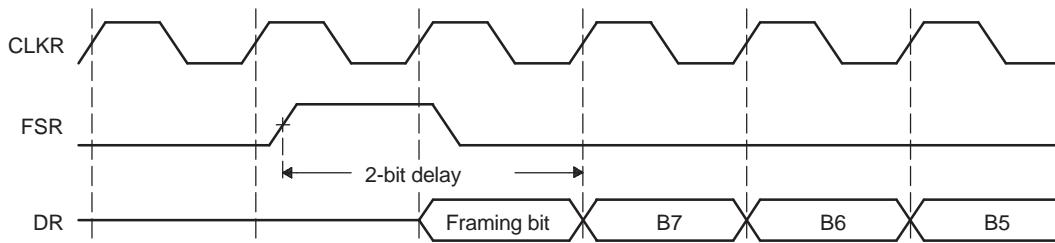
19.8.12.2 0-Bit Data Delay

Normally, a frame-synchronization pulse is detected or sampled with respect to an edge of serial clock internal CLK(R/X). Thus, on the following cycle or later (depending on the data delay value), data can be received or transmitted. However, in the case of 0-bit data delay, the data must be ready for reception and/or transmission on the same serial clock cycle.

For reception this problem is solved because receive data is sampled on the first falling edge of MCLKR where an active-high internal FSR is detected. However, data transmission must begin on the rising edge of the internal CLKX clock that generated the frame synchronization. Therefore, the first data bit is assumed to be present in XSR1, and thus DX. The transmitter then asynchronously detects the frame synchronization, FSX, going active high and immediately starts driving the first bit to be transmitted on the DX pin.

19.8.12.3 2-Bit Data Delay

A data delay of two bit-periods allows the serial port to interface to different types of T1 framing devices where the data stream is preceded by a framing bit. During reception of such a stream with data delay of two bits (framing bit appears after a 1-bit delay and data appears after a 2-bit delay), the serial port essentially discards the framing bit from the data stream, as shown in the following figure. In this figure, the data transferred is an 8-bit value with bits labeled B7, B6, B5, and so on.

Figure 19-57. 2-Bit Data Delay Used to Skip a Framing Bit

19.8.13 Set the Transmit DXENA Mode

Table 19-60. Register Bit Used to Set the Transmit DXENA (DX Delay Enabler) Mode

Register	Bit	Name	Function	Type	Reset Value
SPCR1	7	DXENA	DX delay enabler mode	R/W	0
			DXENA = 0 DX delay enabler is off.		
			DXENA = 1 DX delay enabler is on.		

19.8.13.1 DXENA Mode

The DXENA bit controls the delay enabler on the DX pin. Set DXENA to enable an extra delay for turn-on time. This bit does not control the data itself, so only the first bit is delayed.

If you tie together the DX pins of multiple McBSPs, make sure DXENA = 1 to avoid having more than one McBSP transmit on the data line at one time.

19.8.14 Set the Transmit Interrupt Mode

The transmitter interrupt (XINT) signals the CPU of changes to the serial port status. Four options exist for configuring this interrupt. The options are set by the transmit interrupt mode bits, XINTM, in SPCR2.

Table 19-61. Register Bits Used to Set the Transmit Interrupt Mode

Register	Bit	Name	Function	Type	Reset Value
SPCR2	5-4	XINTM	Transmit interrupt mode	R/W	00
			XINTM = 00 XINT generated when XRDY changes from 0 to 1.		
			XINTM = 01 XINT generated by an end-of-block or end-of-frame condition in a transmit multichannel selection mode. In any of the transmit multichannel selection modes, interrupt after every 16-channel block boundary has been crossed within a frame and at the end of the frame. For details, see Section 19.5.8 . In any other serial transfer case, this setting is not applicable and, therefore, no interrupts are generated.		
			XINTM = 10 XINT generated by a new transmit frame-synchronization pulse. Interrupt on detection of each transmit frame-synchronization pulse. This generates an interrupt even when the transmitter is in its reset state. This is done by synchronizing the incoming frame-synchronization pulse to the CPU clock and sending it to the CPU via XINT.		
			XINTM = 11 XINT generated when XSYNCERR is set. Interrupt on frame-synchronization error. Regardless of the value of XINTM, XSYNCERR can be read to detect this condition. For more information on using XSYNCERR, see Section 19.4.6 .		

19.8.15 Set the Transmit Frame-Synchronization Mode

Table 19-62. Register Bits Used to Set the Transmit Frame-Synchronization Mode

Register	Bit	Name	Function	Type	Reset Value
PCR	11	FSXM	Transmit frame-synchronization mode FSXM = 0 Transmit frame synchronization is supplied by an external source via the FSX pin. FSXM = 1 Transmit frame synchronization is supplied by the McBSP, as determined by the FSGM bit of SRGR2.	R/W	0
SRGR2	12	FSGM	Sample rate generator transmit frame-synchronization mode Used when FSXM = 1 in PCR. FSGM = 0 The McBSP generates a transmit frame-synchronization pulse when the content of DXR[1,2] is copied to XSR[1,2]. FSGM = 1 The transmitter uses frame-synchronization pulses generated by the sample rate generator. Program the FWID bits to set the width of each pulse. Program the FPER bits to set the frame-synchronization period.	R/W	0

19.8.15.1 Transmit Frame-Synchronization Modes

Table 19-63 shows how FSXM and FSGM select the source of transmit frame-synchronization pulses. The three choices are:

- External frame-synchronization input
- Sample rate generator frame-synchronization signal (FSG)
- Internal signal that indicates a DXR-to-XSR copy has been made

Table 19-63 also shows the effect of each bit setting on the FSX pin. The polarity of the signal on the FSX pin is determined by the FSXP bit.

Table 19-63. How FSXM and FSGM Select the Source of Transmit Frame-Synchronization Pulses

FSXM	FSGM	Source of Transmit Frame Synchronization	FSX Pin Status
0	0 or 1	An external frame-synchronization signal enters the McBSP through the FSX pin. The signal is then inverted by FSXP before being used as internal FSX.	Input
1	1	Internal FSX is driven by the sample rate generator frame-synchronization signal (FSG).	Output. FSG is inverted by FSXP before being driven out on FSX pin.
1	0	A DXR-to-XSR copy causes the McBSP to generate a transmit frame-synchronization pulse that is 1 cycle wide.	Output. The generated frame-synchronization pulse is inverted as determined by FSXP before being driven out on FSX pin.

19.8.15.2 Other Considerations

If the sample rate generator creates a frame-synchronization signal (FSG) that is derived from an external input clock, the GSYNC bit determines whether FSG is kept synchronized with pulses on the FSR pin. For more details, see [Section 19.3.3](#).

In the clock stop mode (CLKSTP = 10b or 11b), the McBSP can act as a master or as a slave in the SPI protocol. If the McBSP is a master and must provide a slave-enable signal (SPISTE) on the FSX pin, make sure that FSXM = 1 and FSGM = 0 so that FSX is an output and is driven active for the duration of each transmission. If the McBSP is a slave, make sure that FSXM = 0 so that the McBSP can receive the slave-enable signal on the FSX pin.

19.8.16 Set the Transmit Frame-Synchronization Polarity

Table 19-64. Register Bit Used to Set Transmit Frame-Synchronization Polarity

Register	Bit	Name	Function	Type	Reset Value
PCR	3	FSXP	Transmit frame-synchronization polarity FSXP = 0 Frame-synchronization pulse FSX is active high. FSXP = 1 Frame-synchronization pulse FSX is active low.	R/W	0

19.8.16.1 Frame Synchronization Pulses, Clock Signals, and Their Polarities

Transmit frame-synchronization pulses can be generated internally by the sample rate generator (see [Section 19.3.2](#)) or driven by an external source. The source of frame synchronization is selected by programming the mode bit, FSXM, in PCR. FSX is also affected by the FSGM bit in SRGR2. For information about the effects of FSXM and FSGM, see [Section 19.8.15](#)). Similarly, transmit clocks can be selected to be inputs or outputs by programming the mode bit, CLKXM, in the PCR (see [Section 19.8.18](#)).

When FSR and FSX are inputs (FSXM = FSRM= 0, external frame-synchronization pulses), the McBSP detects them on the internal falling edge of clock, internal MCLKR, and internal CLKX, respectively. The receive data arriving at the DR pin is also sampled on the falling edge of internal MCLKR. These internal clock signals are either derived from external source via CLK(R/X) pins or driven by the sample rate generator clock (CLKG) internal to the McBSP.

When FSR and FSX are outputs, implying that they are driven by the sample rate generator, they are generated (transition to their active state) on the rising edge of internal clock, CLK(R/X). Similarly, data on the DX pin is output on the rising edge of internal CLKX.

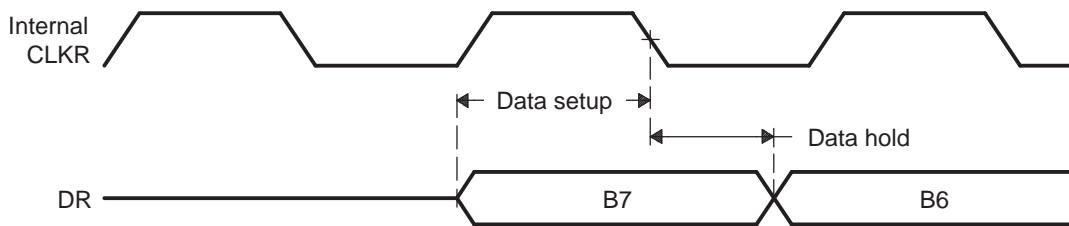
FSRP, FSXP, CLKRP, and CLKXP in the pin control register (PCR) configure the polarities of the FSR, FSX, MCLKR, and CLKX signals, respectively. All frame-synchronization signals (internal FSR, internal FSX) that are internal to the serial port are active high. If the serial port is configured for external frame synchronization (FSR/FSX are inputs to McBSP) and FSRP = FSXP = 1, the external active-low frame-synchronization signals are inverted before being sent to the receiver (internal FSR) and transmitter (internal FSX). Similarly, if internal synchronization (FSR/FSX are output pins and GSYNC = 0) is selected and the polarity bit FS(R/X)P = 1, the internal active-high frame-synchronization signals are inverted before being sent to the FS(R/X) pin.

On the transmit side, the transmit clock polarity bit, CLKXP, sets the edge used to shift and clock out transmit data. Data is always transmitted on the rising edge of internal CLKX. If CLKXP = 1 and external clocking is selected (CLKXM = 0 and CLKX is an input), the external falling-edge triggered input clock on CLKX is inverted to a rising-edge triggered clock before being sent to the transmitter. If CLKXP = 1, and internal clocking selected (CLKXM = 1 and CLKX is an output pin), the internal (rising-edge triggered) clock, internal CLKX, is inverted before being sent out on the MCLKX pin.

Similarly, the receiver can reliably sample data that is clocked with a rising edge clock (by the transmitter). The receive clock polarity bit, CLKRP, sets the edge used to sample received data. The receive data is always sampled on the falling edge of internal MCLKR. Therefore, if CLKRP = 1 and external clocking is selected (CLKRM = 0 and MCLKR is an input pin), the external rising-edge triggered input clock on MCLKR is inverted to a falling-edge triggered clock before being sent to the receiver. If CLKRP = 1 and internal clocking is selected (CLKRM = 1), the internal falling-edge triggered clock is inverted to a rising-edge triggered clock before being sent out on the MCLKR pin.

CLKRP = CLKXP in a system where the same clock (internal or external) is used to clock the receiver and transmitter. The receiver uses the opposite edge as the transmitter to ensure valid setup and hold of data around this edge. [Figure 19-58](#) shows how data clocked by an external serial device using a rising edge can be sampled by the McBSP receiver on the falling edge of the same clock.

Figure 19-58. Data Clocked Externally Using a Rising Edge and Sampled by the McBSP Receiver on a Falling Edge



19.8.17 Set the SRG Frame-Synchronization Period and Pulse Width

Table 19-65. Register Bits Used to Set SRG Frame-Synchronization Period and Pulse Width

Register	Bit	Name	Function	Type	Reset Value
SRGR2	11-0	FPER	Sample rate generator frame-synchronization period For the frame-synchronization signal FSG, (FPER + 1) determines the period from the start of a frame-synchronization pulse to the start of the next frame-synchronization pulse. Range for (FPER + 1): 1 to 4096 CLKG cycles.	R/W	0000 0000 0000
SRGR1	15-8	FWID	Sample rate generator frame-synchronization pulse width This field plus 1 determines the width of each frame-synchronization pulse on FSG. Range for (FWID + 1): 1 to 256 CLKG cycles.	R/W	0000 0000

19.8.17.1 Frame-Synchronization Period and Frame-Synchronization Pulse Width

The sample rate generator can produce a clock signal, CLKG, and a frame-synchronization signal, FSG. If the sample rate generator is supplying receive or transmit frame synchronization, you must program the bit fields FPER and FWID.

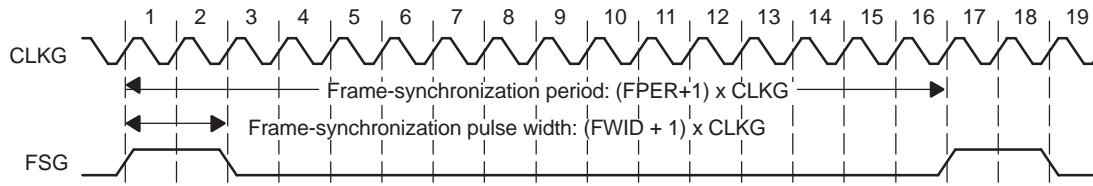
On FSG, the period from the start of a frame-synchronization pulse to the start of the next pulse is (FPER + 1) CLKG cycles. The 12 bits of FPER allow a frame-synchronization period of 1 to 4096 CLKG cycles, which allows up to 4096 data bits per frame. When GSYNC = 1, FPER is a don't care value.

Each pulse on FSG has a width of (FWID + 1) CLKG cycles. The eight bits of FWID allow a pulse width of 1 to 256 CLKG cycles. It is recommended that FWID be programmed to a value less than the programmed word length.

The values in FPER and FWID are loaded into separate down-counters. The 12-bit FPER counter counts down the generated clock cycles from the programmed value (4095 maximum) to 0. The 8-bit FWID counter counts down from the programmed value (255 maximum) to 0.

Figure 19-59 shows a frame-synchronization period of 16 CLKG periods (FPER = 15 or 00001111b) and a frame-synchronization pulse with an active width of 2 CLKG periods (FWID = 1).

Figure 19-59. Frame of Period 16 CLKG Periods and Active Width of 2 CLKG Periods



When the sample rate generator comes out of reset, FSG is in its inactive state. Then, when GRST = 1 and FSGM = 1, a frame-synchronization pulse is generated. The frame width value (FWID + 1) is counted down on every CLKG cycle until it reaches 0, at which time FSG goes low. At the same time, the frame period value (FPER + 1) is also counting down. When this value reaches 0, FSG goes high, indicating a new frame.

19.8.18 Set the Transmit Clock Mode

Table 19-66. Register Bit Used to Set the Transmit Clock Mode

Register	Bit	Name	Function	Type	Reset Value
PCR	9	CLKXM	Transmit clock mode	R/W	0
		CLKXM = 0	The transmitter gets its clock signal from an external source via the MCLKX pin.		
		CLKXM = 1	The MCLKX pin is an output pin driven by the sample rate generator of the McBSP.		

19.8.18.1 Selecting a Source for the Transmit Clock and a Data Direction for the MCLKX pin

Table 19-67 shows how the CLKXM bit selects the transmit clock and the corresponding status of the MCLKX pin. The polarity of the signal on the MCLKX pin is determined by the CLKXP bit.

Table 19-67. How the CLKXM Bit Selects the Transmit Clock and the Corresponding Status of the MCLKX pin

CLKXM in PCR	Source of Transmit Clock	MCLKX pin Status
0	Internal CLKX is driven by an external clock on the MCLKX pin. CLKX is inverted as determined by CLKXP before being used.	Input
1	Internal CLKX is driven by the sample rate generator clock, CLKG.	Output. CLKG, inverted as determined by CLKXP, is driven out on CLKX.

19.8.18.2 Other Considerations

If the sample rate generator creates a clock signal (CLKG) that is derived from an external input clock, the GSYNC bit determines whether CLKG is kept synchronized with pulses on the FSR pin. For more details, see [Section 19.3.3](#).

In the clock stop mode (CLKSTP = 10b or 11b), the McBSP can act as a master or as a slave in the SPI protocol. If the McBSP is a master, make sure that CLKXM = 1 so that CLKX is an output to supply the master clock to any slave devices. If the McBSP is a slave, make sure that CLKXM = 0 so that CLKX is an input to accept the master clock signal.

19.8.19 Set the Transmit Clock Polarity

Table 19-68. Register Bit Used to Set Transmit Clock Polarity

Register	Bit	Name	Function	Type	Reset Value
PCR	1	CLKXP	Transmit clock polarity	R/W	0
		CLKXP = 0	Transmit data sampled on rising edge of CLKX.		
		CLKXP = 1	Transmit data sampled on falling edge of CLKX.		

19.8.19.1 Frame Synchronization Pulses, Clock Signals, and Their Polarities

Transmit frame-synchronization pulses can be either generated internally by the sample rate generator (see [Section 19.3.2](#)) or driven by an external source. The source of frame synchronization is selected by programming the mode bit, FSXM, in PCR. FSX is also affected by the FSGM bit in SRGR2. For information about the effects of FSXM and FSGM, see [Section 19.8.15](#)). Similarly, transmit clocks can be selected to be inputs or outputs by programming the mode bit, CLKXM, in the PCR (see [Section 19.8.18](#)).

When FSR and FSX are inputs (FSXM = FSRM= 0, external frame-synchronization pulses), the McBSP detects them on the internal falling edge of clock, internal MCLKR, and internal CLKX, respectively. The receive data arriving at the DR pin is also sampled on the falling edge of internal MCLKR. These internal clock signals are either derived from external source via CLK(R/X) pins or driven by the sample rate generator clock (CLKG) internal to the McBSP.

When FSR and FSX are outputs, implying that they are driven by the sample rate generator, they are generated (transition to their active state) on the rising edge of internal clock, CLK(R/X). Similarly, data on the DX pin is output on the rising edge of internal CLKX.

FSRP, FSXP, CLKRP, and CLKXP in the pin control register (PCR) configure the polarities of the FSR, FSX, MCLKR, and CLKX signals, respectively. All frame-synchronization signals (internal FSR, internal FSX) that are internal to the serial port are active high. If the serial port is configured for external frame synchronization (FSR/FSX are inputs to McBSP), and FSRP = FSXP = 1, the external active-low frame-synchronization signals are inverted before being sent to the receiver (internal FSR) and transmitter (internal FSX). Similarly, if internal synchronization (FSR/FSX are output pins and GSYNC = 0) is selected, the internal active-high frame-synchronization signals are inverted, if the polarity bit FS(R/X)P = 1, before being sent to the FS(R/X) pin.

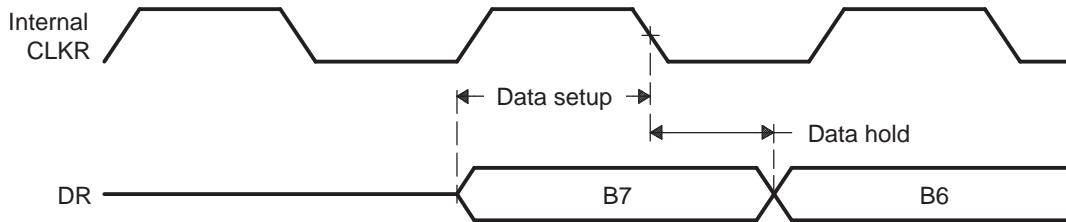
On the transmit side, the transmit clock polarity bit, CLKXP, sets the edge used to shift and clock out transmit data. Data is always transmitted on the rising edge of internal CLKX. If CLKXP = 1 and external clocking is selected (CLKXM = 0 and CLKX is an input), the external falling-edge triggered input clock on CLKX is inverted to a rising-edge triggered clock before being sent to the transmitter. If CLKXP = 1 and internal clocking is selected (CLKXM = 1 and CLKX is an output pin), the internal (rising-edge triggered) clock, internal CLKX, is inverted before being sent out on the MCLKX pin.

Similarly, the receiver can reliably sample data that is clocked with a rising edge clock (by the transmitter). The receive clock polarity bit, CLKRP, sets the edge used to sample received data. The receive data is always sampled on the falling edge of internal MCLKR. Therefore, if CLKRP = 1 and external clocking is selected (CLKRM = 0 and CLKR is an input pin), the external rising-edge triggered input clock on CLKR is inverted to a falling-edge triggered clock before being sent to the receiver. If CLKRP = 1 and internal clocking is selected (CLKRM = 1), the internal falling-edge triggered clock is inverted to a rising-edge triggered clock before being sent out on the MCLKR pin.

CLKRP = CLKXP in a system where the same clock (internal or external) is used to clock the receiver and transmitter. The receiver uses the opposite edge as the transmitter to ensure valid setup and hold of data around this edge (see [Figure 19-58](#)).

[Figure 19-60](#) shows how data clocked by an external serial device using a rising edge can be sampled by the McBSP receiver on the falling edge of the same clock.

Figure 19-60. Data Clocked Externally Using a Rising Edge and Sampled by the McBSP Receiver on a Falling Edge



19.9 Emulation and Reset Considerations

This section covers the following topics:

- How to program McBSP response to a breakpoint in the high-level language debugger (see [Section 19.9.1](#))
- How to reset and initialize the various parts of the McBSP (see [Section 19.9.2](#))

19.9.1 McBSP Emulation Mode

FREE and SOFT are special emulation bits in SPCR2 that determine the state of the McBSP when a breakpoint is encountered in the high-level language debugger. If FREE = 1, the clock continues to run upon a software breakpoint and data is still shifted out. When FREE = 1, the SOFT bit is a *don't care*.

If FREE = 0, the SOFT bit takes effect. If SOFT = 0 when breakpoint occurs, the clock stops immediately, aborting a transmission. If SOFT = 1 and a breakpoint occurs while transmission is in progress, the transmission continues until completion of the transfer and then the clock halts. These options are listed in [Table 19-69](#).

The McBSP receiver functions in a similar fashion. If a mode other than the immediate stop mode (SOFT = FREE = 0) is chosen, the receiver continues running and an overrun error is possible.

Table 19-69. McBSP Emulation Modes Selectable with FREE and SOFT Bits of SPCR2

FREE	SOFT	McBSP Emulation Mode
0	0	Immediate stop mode (reset condition) The transmitter or receiver stops immediately in response to a breakpoint.
0	1	Soft stop mode When a breakpoint occurs, the transmitter stops after completion of the current word. The receiver is not affected.
1	0 or 1	Free run mode The transmitter and receiver continue to run when a breakpoint occurs.

19.9.2 Resetting and Initializing McBSPs

19.9.2.1 McBSP Pin States: DSP Reset Versus Receiver/Transmitter Reset

[Table 19-70](#) shows the state of McBSP pins when the serial port is reset due to direct receiver or transmitter reset on the 2833x device.

Table 19-70. Reset State of Each McBSP Pin

Pin	Possible State(s) ⁽¹⁾	State Forced by Device Reset	State Forced by Receiver/Transmitter Reset
Receiver reset (RRST = 0 and GRST = 1)			
MDRx	I	GPIO-input	Input
MCLKRx	I/O/Z	GPIO-input	Known state if input; MCLKR running if output
MFSRx	I/O/Z	GPIO-input	Known state if input; FSRP inactive state if output
Transmitter reset (XRST = 0 and GRST = 1)			
MDXx	O/Z	GPIO Input	High impedance
MCLKXx	I/O/Z	GPIO-input	Known state if input; CLKX running if output
MFSXx	I/O/Z	GPIO-input	Known state if input; FSXP inactive state if output

⁽¹⁾ In Possible State(s) column, I = Input, O = Output, Z = High impedance. In the 28x family, at device reset, all I/Os default to GPIO function and generally as inputs.

19.9.2.2 Device Reset, McBSP Reset, and Sample Rate Generator Reset

When the McBSP is reset in either of the above two ways, the machine is reset to its initial state, including reset of all counters and status bits. The receive status bits include RFULL, RRDY, and RSYNCERR. The transmit status bits include XEMPTY, XRDY, and XSYNCERR.

- Device reset. When the whole DSP is reset (\overline{XRS} signal is driven low), all McBSP pins are in GPIO

mode. When the device is pulled out of reset, the clock to the McBSP modules remains disabled.

- McBSP reset. When the receiver and transmitter reset bits, RRST and XRST, are loaded with 0s, the respective portions of the McBSP are reset and activity in the corresponding section of the serial port stops. Input-only pins such as MDRx, and all other pins that are configured as inputs are in a known state. The MFSRx and MFSXx pins are driven to their inactive state if they are not outputs. If the MCLKR and MCLKX pins are programmed as outputs, they are driven by CLKG, provided that GRST = 1. Lastly, the MDXx pin is in the high-impedance state when the transmitter and/or the device is reset.

During normal operation, the sample rate generator is reset if the GRST bit is cleared. GRST must be 0 only when neither the transmitter nor the receiver is using the sample rate generator. In this case, the internal sample rate generator clock (CLKG) and its frame-synchronization signal (FSG) are driven inactive low.

When the sample rate generator is not in the reset state (GRST = 1), pins MFSRx and MFSXx are in an inactive state when RRST = 0 and XRST = 0, respectively, even if they are outputs driven by FSG. This ensures that when only one portion of the McBSP is in reset, the other portion can continue operation when GRST = 1 and its frame synchronization is driven by FSG.

- Sample rate generator reset. The sample rate generator is reset when GRST is loaded with 0.

When neither the transmitter nor the receiver is fed by CLKG and FSG, you can reset the sample rate generator by clearing GRST. In this case, CLKG and FSG are driven inactive low. If you then set GRST, CLKG starts and runs as programmed. Later, if GRST = 1, FSG pulses active high after the programmed number of CLKG cycles has elapsed.

19.9.2.3 McBSP Initialization Procedure

The serial port initialization procedure is as follows:

1. Make XRST = RRST = GRST = 0 in SPCR[1,2]. If coming out of a device reset, this step is not required.
2. While the serial port is in the reset state, program only the McBSP configuration registers (not the data registers) as required.
3. Wait for two clock cycles. This ensures proper internal synchronization.
4. Set up data acquisition as required (such as writing to DXR[1,2]).
5. Make XRST = RRST = 1 to enable the serial port. Make sure that as you set these reset bits, you do not modify any of the other bits in SPCR1 and SPCR2. Otherwise, you change the configuration you selected in step 2.
6. Set FRST = 1, if internally generated frame synchronization is required.
7. Wait two clock cycles for the receiver and transmitter to become active.

Alternatively, on either write (step 1 or 5), the transmitter and receiver can be placed in or taken out of reset individually by modifying the desired bit.

The above procedure for reset/initialization can be applied in general when the receiver or transmitter must be reset during its normal operation and when the sample rate generator is not used for either operation.

NOTE:

1. The necessary duration of the active-low period of XRST or RRST is at least two MCLKR/CLKX cycles.
2. The appropriate bits in serial port configuration registers SPCR[1,2], PCR, RCR[1,2], XCR[1,2], and SRGR[1,2] must only be modified when the affected portion of the serial port is in its reset state.
3. In most cases, the data transmit registers (DXR[1,2]) must be loaded by the CPU or by the DMA controller only when the transmitter is enabled (XRST = 1). An exception to this rule is when these registers are used for companding internal data (see [Section 19.2.2.2](#)).
4. The bits of the channel control registers—MCR[1,2], RCER[A-H], XCER[A-H]—can be modified at any time as long as they are not being used by the current reception/transmission in a multichannel selection mode.

19.9.2.4 Resetting the Transmitter While the Receiver is Running

shows values in the control registers that reset and configure the transmitter while the receiver is running.

Example 19-1. Resetting and Configuring McBSP Transmitter While McBSP Receiver Running

```
SPCR1 = 0001h SPCR2 = 0030h
; The receiver is running with the receive interrupt (RINT) triggered by the
; receiver ready bit (RRDY). The transmitter is in its reset state
; The transmit interrupt (XINT) will be triggered by the transmit frame-sync
; error bit (XSYNCERR). PCR = 0900h
; Transmit frame synchronization is generated internally according to the
; FSGM bit of SRGR2.
; The transmit clock is driven by an external source.
; The receive clock continues to be driven by sample rate generator. The input clock
; of the sample rate generator is supplied by the CPU clock SRGR1 = 0001h SRGR2 = 2000h
; The CPU clock is the input clock for the sample rate generator. The sample
; rate generator divides the CPU clock by 2 to generate its output clock (CLKG).
; Transmit frame synchronization is tied to the automatic copying of data from
; the DXR(s) to the XSR(s). XCR1 = 0740h XCR2 = 8321h
; The transmit frame has two phases. Phase 1 has eight 16-bit words. Phase 2
; has four 12-bit words. There is 1-bit data delay between the start of a
; frame-sync pulse and the first data bit
; transmitted. SPCR2 = 0031h
; The transmitter is taken out of reset.
```

19.10 Data Packing Examples

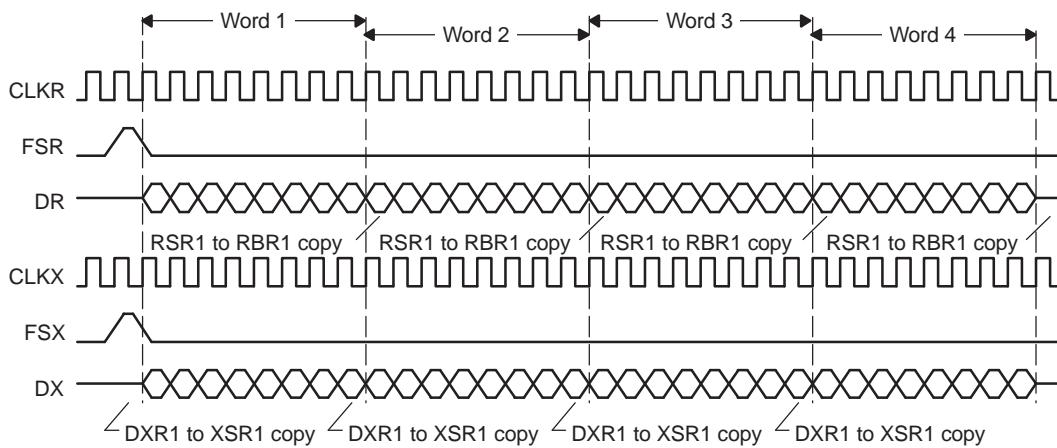
This section shows two ways to implement data packing in the McBSP.

19.10.1 Data Packing Using Frame Length and Word Length

Frame length and word length can be manipulated to effectively pack data. For example, consider a situation where four 8-bit words are transferred in a single-phase frame as shown in [Figure 19-61](#). In this case:

- (R/X)PHASE = 0: Single-phase frame
- (R/X)FRLEN1 = 0000011b: 4-word frame
- (R/X)WDLEN1 = 000b: 8-bit words

Four 8-bit data words are transferred to and from the McBSP by the CPU or by the DMA controller. Thus, four reads from DRR1 and four writes to DXR1 are necessary for each frame.

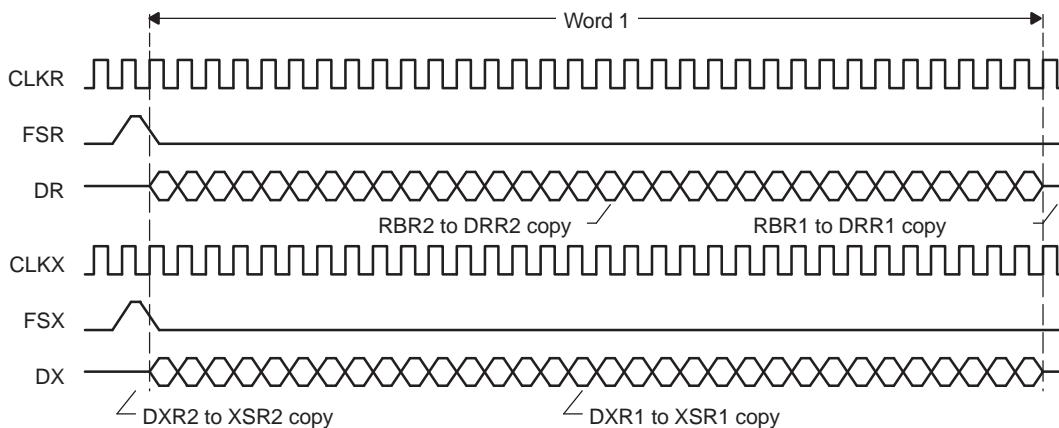
Figure 19-61. Four 8-Bit Data Words Transferred To/From the McBSP

This data can also be treated as a single-phase frame consisting of one 32-bit data word, as shown in [Figure 19-62](#). In this case:

- (R/X)PHASE = 0: Single-phase frame
- (R/X)FRLEN1 = 0000000b: 1-word frame
- (R/X)WDLEN1 = 101b: 32-bit word

Two 16-bit data words are transferred to and from the McBSP by the CPU or DMA controller. Thus, two reads, from DRR2 and DRR1, and two writes, to DXR2 and DXR1, are necessary for each frame. This results in only half the number of transfers compared to the previous case. This manipulation reduces the percentage of bus time required for serial port data movement.

NOTE: When the word length is larger than 16 bits, make sure you access DRR2/DXR2 before you access DRR1/DXR1. McBSP activity is tied to accesses of DRR1/DXR1. During the reception of 24-bit or 32-bit words, read DRR2 and then read DRR1. Otherwise, the next RBR[1,2]-to-DRR[1,2] copy occurs before DRR2 is read. Similarly, during the transmission of 24-bit or 32-bit words, write to DXR2 and then write to DXR1. Otherwise, the next DXR[1,2]-to-XSR[1,2] copy occurs before DXR2 is loaded with new data.

Figure 19-62. One 32-Bit Data Word Transferred To/From the McBSP

19.10.2 Data Packing Using Word Length and the Frame-Synchronization Ignore Function

When there are multiple words per frame, you can implement data packing by increasing the word length (defining a serial word with more bits) and by ignoring frame-synchronization pulses. First, consider Figure 19-63, which shows the McBSP operating at the maximum packet frequency. Here, each frame only has a single 8-bit word. Notice the frame-synchronization pulse that initiates each frame transfer for reception and for transmission. For reception, this configuration requires one read operation for each word. For transmission, this configuration requires one write operation for each word.

Figure 19-63. 8-Bit Data Words Transferred at Maximum Packet Frequency

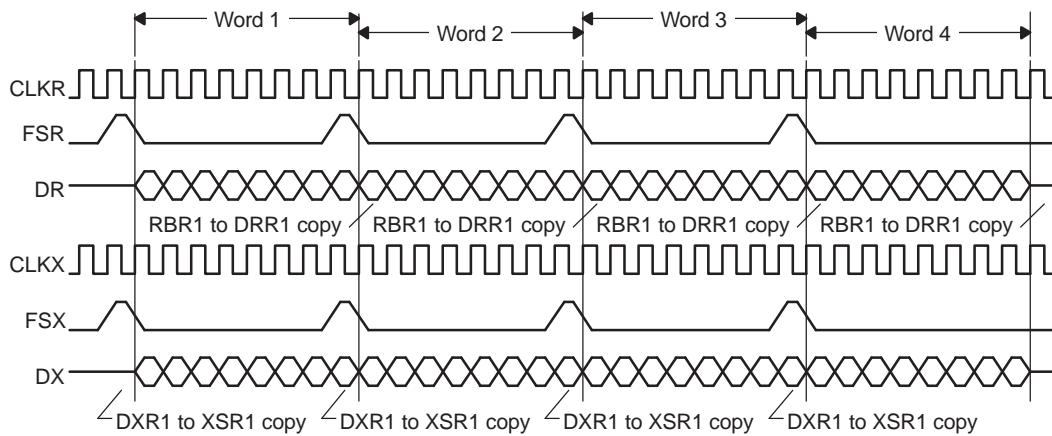
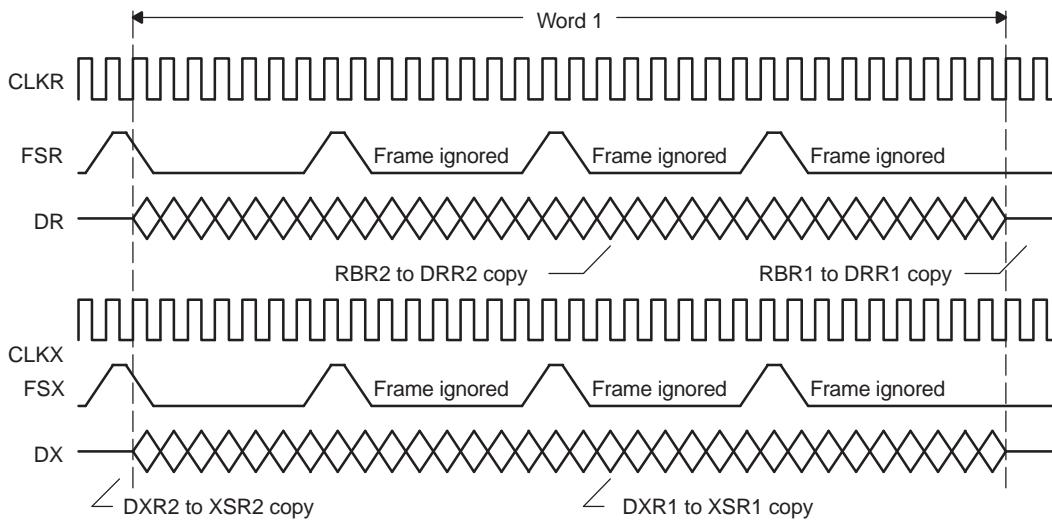


Figure 19-64 shows the McBSP configured to treat this data stream as a continuous 32-bit word. In this example, the McBSP responds to an initial frame-synchronization pulse. However, (R/X)FIG = 1 so that the McBSP ignores subsequent pulses. Only two read transfers or two write transfers are needed every 32 bits. This configuration effectively reduces the required bus bandwidth to half the bandwidth needed to transfer four 8-bit words.

Figure 19-64. Configuring the Data Stream of Figure 19-63 as a Continuous 32-Bit Word



19.11 Interrupt Generation

McBSP registers can be programmed to receive and transmit data through DRR2/DRR1 and DXR2/DXR1 registers, respectively. The CPU can directly access these registers to move data from memory to these registers. Interrupt signals will be based on these register pair contents and its related flags. MRINT/MXINT will generate CPU interrupts for receive and transmit conditions.

19.11.1 McBSP Receive Interrupt Generation

In the McBSP module, data receive and error conditions generate two sets of interrupt signals. One set is used for the CPU and the other set is for DMA.

Figure 19-65. Receive Interrupt Generation

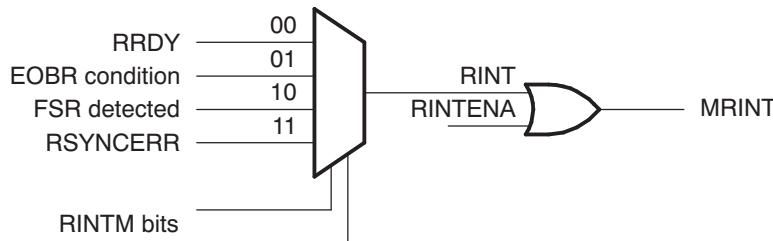


Table 19-71. Receive Interrupt Sources and Signals

McBSP Interrupt Signal	Interrupt Flags	Interrupt Enables in SPCR1	Interrupt Enables	Type of Interrupt	Interrupt Line
	RINTM				
	Bits				
RINT	RRDY	0	RINTENA	Every word receive	MRINT
	EOBR	1	RINTENA	Every 16 channel block boundary	
	FSR	10	RINTENA	On every FSR	
	RSYNCERR	11	RINTENA	Frame sync error	

NOTE: Since X/RINT, X/REVTA, and X/RXFFINT share the same CPU interrupt, it is recommended that all applications use one of the above selections for interrupt generation. If multiple interrupt enables are selected at the same time, there is a likelihood of interrupts being masked or not recognized.

19.11.2 McBSP Transmit Interrupt Generation

McBSP module data transmit and error conditions generate two sets of interrupt signals. One set is used for the CPU and the other set is for DMA.

Figure 19-66. Transmit Interrupt Generation

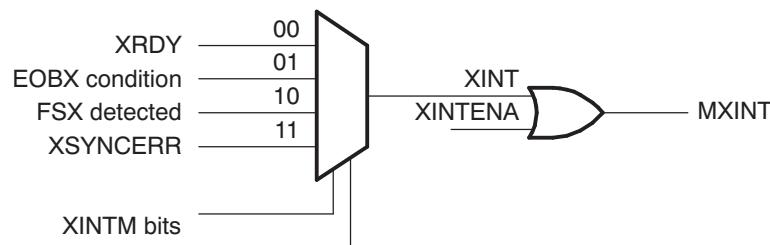


Table 19-72. Transmit Interrupt Sources and Signals

McBSP Interrupt Signal	Interrupt Flags	Interrupt Enables in SPCR1	Interrupt Enables	Type of Interrupt	Interrupt Line
	XINTM Bits				
XINT	XRDY	0	XINTENA	Every word receive	MXINT
	EOBOX	1	XINTENA	Every 16-channel block boundary	

Table 19-72. Transmit Interrupt Sources and Signals (continued)

McBSP Interrupt Signal	Interrupt Flags	Interrupt Enables in SPCR1	Interrupt Enables	Type of Interrupt	Interrupt Line
	FSX	10	XINTENA	On every FSX	
	XSYNCERR	11	XINTENA	Frame sync error	

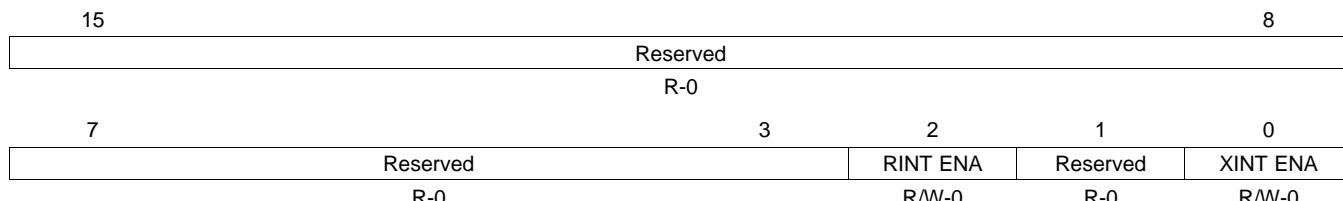
19.11.3 Error Flags

The McBSP has several error flags both on receive and transmit channel. [Table 19-73](#) explains the error flags and their meaning.

Table 19-73. Error Flags

Error Flags	Function
RFULL	Indicates DRR2/DRR1 are not read and RXR register is overwritten
RSYNCERR	Indicates unexpected frame-sync condition, current data reception will abort and restart. Use RINTM bit 11 for interrupt generation on this condition.
XSYNCERR	Indicates unexpected frame-sync condition, current data transmission will abort and restart. Use XINTM bit 11 for interrupt generation on this condition.

19.11.4 McBSP Interrupt Enable Register

Figure 19-67. McBSP Interrupt Enable Register (MFFINT)


LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-74. McBSP Interrupt Enable Register (MFFINT) Field Descriptions

Bit	Field	Value	Description
15:3	Reserved		Reserved
2	RINT ENA	0	Enable for Receive Interrupt Receive interrupt on RRDY is disabled. 1 Receive interrupt on RRDY is enabled.
1	Reserved		
0	XINT ENA	0	Enable for transmit Interrupt Transmit interrupt on XRDY is disabled. 1 Transmit interrupt on XRDY is enabled.

19.12 McBSP Modes

McBSP, in its normal mode, communicates with various types of Codecs with variable word size. Apart from this mode, the McBSP uses time-division multiplexed (TDM) data stream while communicating with other McBSPs or serial devices. The multichannel mode provides flexibility while transmitting/receiving selected channels or all the channels in a TDM stream.

[Table 19-75](#) provides a quick reference to McBSP mode selection.

Table 19-75. McBSP Mode Selection

No.	McBSP Word Size	Register Bits Used for Mode Selection				Mode and Function Description	
		MCR1 bit 9,0		MCR2 bit 9,1,0			
		RMCME	RMCM	XMCME	XMCM		
1	8/12/16/20/24/32 bit words	0	0	0	0	Normal Mode All types of Codec interface will use this selection	
Multichannel Mode							
2	8-bit words	0	1	0	1	2 Partition or 32-channel Mode All channels are disabled,unless selected in X/RCERA/B	
		0	1	0	10	All channels are enabled,but masked unless selected in X/RCERA/B	
		0	1	0	11	Symmetric transmit, receive 8 Partition or 128 Channel Mode Transmit/ Receive Channels selected by X/RCERA to X/RCERH bits	
Multichannel Mode is ON							
		1	1	1	1	All channels are disabled,unless selected in XCERs	
		1	1	1	10	All channels are enabled,but masked unless selected in XCERs	
		1	1	1	11	Symmetric transmit, receive	
Continuous Mode - Transmit							
Multi-Channel Mode is OFF							
All 128 channels are active and enabled							

19.13 McBSP Registers

This section describes the McBSP registers.

19.13.1 McBSP Base Addresses

Table 19-76. McBSP Base Address Table

McbspaRegs	MCBSP_REGS	0x0000_6000	0x0000_603F
McbspbRegs	MCBSP_REGS	0x0000_6040	0x0000_607F

Table 19-77 shows the registers accessible on each McBSP. Section 19.13.2 through Section 19.13.11 describe the register bits.

Table 19-77. McBSP Register Summary

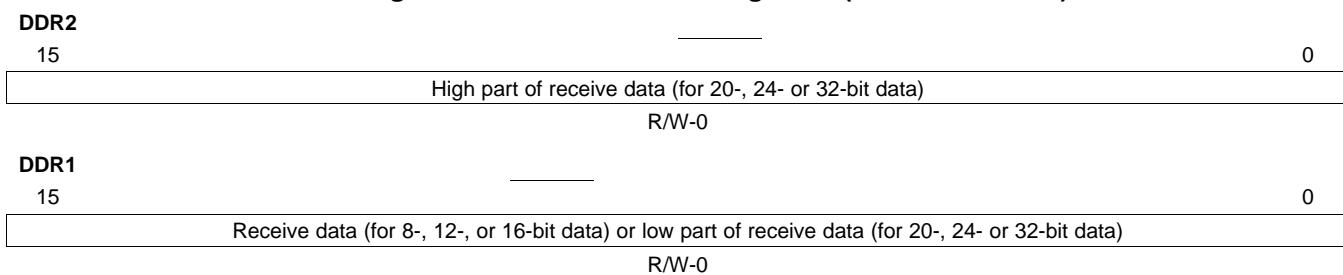
Name	McBSP-A Address	McBSP-B Address	Type	Reset Value	Description
Data Registers, Receive, Transmit					
DRR2	0x6000	0x6040	R	0x0000	McBSP Data Receive Register 2
DRR1	0x6001	0x6041	R	0x0000	McBSP Data Receive Register 1
DXR2	0x6002	0x6042	W	0x0000	McBSP Data Transmit Register 2
DXR1	0x6003	0x6043	W	0x0000	McBSP Data Transmit Register 1

Table 19-77. McBSP Register Summary (continued)

Name	McBSP-A Address	McBSP-B Address	Type	Reset Value	Description
McBSP Control Registers					
SPCR2	0x6004	0x6044	R/W	0x0000	McBSP Serial Port Control Register 2
SPCR1	0x6005	0x6045	R/W	0x0000	McBSP Serial Port Control Register 1
RCR2	0x6006	0x6046	R/W	0x0000	McBSP Receive Control Register 2
RCR1	0x6007	0x6047	R/W	0x0000	McBSP Receive Control Register 1
XCR2	0x6008	0x6048	R/W	0x0000	McBSP Transmit Control Register 2
XCR1	0x6009	0x6049	R/W	0x0000	McBSP Transmit Control Register 1
SRGR2	0x600A	0x604A	R/W	0x0000	McBSP Sample Rate Generator Register 2
SRGR1	0x600B	0x604B	R/W	0x0000	McBSP Sample Rate Generator Register 1
Multichannel Control Registers					
MCR2	0x600C	0x604C	R/W	0x0000	McBSP Multichannel Register 2
MCR1	0x600D	0x604D	R/W	0x0000	McBSP Multichannel Register 1
RCERA	0x600E	0x604E	R/W	0x0000	McBSP Receive Channel Enable Register Partition A
RCERB	0x600F	0x604F	R/W	0x0000	McBSP Receive Channel Enable Register Partition B
XCERA	0x6010	0x6050	R/W	0x0000	McBSP Transmit Channel Enable Register Partition A
XCERB	0x6011	0x6051	R/W	0x0000	McBSP Transmit Channel Enable Register Partition B
PCR	0x6012	0x6052	R/W	0x0000	McBSP Pin Control Register
RCERC	0x6013	0x6053	R/W	0x0000	McBSP Receive Channel Enable Register Partition C
RCERD	0x6014	0x6054	R/W	0x0000	McBSP Receive Channel Enable Register Partition D
XCERC	0x6015	0x6055	R/W	0x0000	McBSP Transmit Channel Enable Register Partition C
XCERD	0x6016	0x6056	R/W	0x0000	McBSP Transmit Channel Enable Register Partition D
RCERE	0x6017	0x6057	R/W	0x0000	McBSP Receive Channel Enable Register Partition E
RCERF	0x6018	0x6058	R/W	0x0000	McBSP Receive Channel Enable Register Partition F
XCERE	0x6019	0x6059	R/W	0x0000	McBSP Transmit Channel Enable Register Partition E
XCERF	0x601A	0x605A	R/W	0x0000	McBSP Transmit Channel Enable Register Partition F
RCERG	0x601B	0x605B	R/W	0x0000	McBSP Receive Channel Enable Register Partition G
RCERH	0x601C	0x605C	R/W	0x0000	McBSP Receive Channel Enable Register Partition H
XCERG	0x601D	0x605D	R/W	0x0000	McBSP Transmit Channel Enable Register Partition G
XCERH	0x601E	0x605E	R/W	0x0000	McBSP Transmit Channel Enable Register Partition H
MFFINT	0x6023	0x6063	R/W	0x0000	McBSP Interrupt Enable Register

19.13.2 Data Receive Registers (DRR[1,2])

The CPU or the DMA controller reads received data from one or both of the data receive registers (see [Figure 19-68](#)). If the serial word length is 16 bits or smaller, only DRR1 is used. If the serial length is larger than 16 bits, both DRR1 and DRR2 are used and DRR2 holds the most significant bits. Each frame of receive data in the McBSP can have one phase or two phases, each with its own serial word length.

Figure 19-68. Data Receive Registers (DRR2 and DRR1)

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

19.13.2.1 Data Travel From Data Receive Pins to the Registers

If the serial word length is 16 bits or smaller, receive data on the MDRx pin is shifted into receive shift register 1 (RSR1) and then copied into receive buffer register 1 (RBR1). The content of RBR1 is then copied to DRR1, which can be read by the CPU or by the DMA controller. The RSRs and RBRs are not accessible to the user.

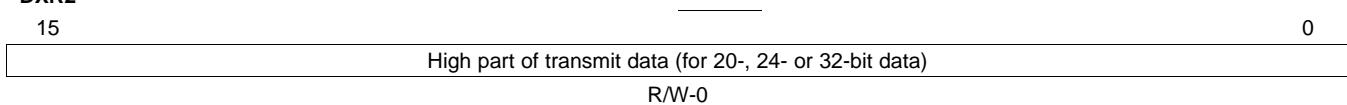
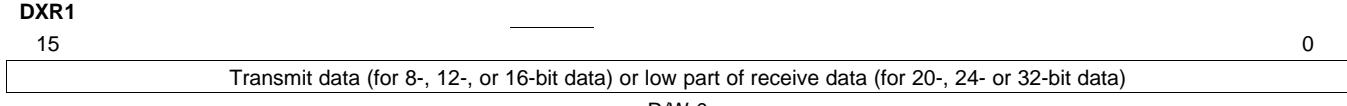
If the serial word length is larger than 16 bits, receive data on the MDRx pin is shifted into both of the receive shift registers (RSR2, RSR1) and then copied into both of the receive buffer registers (RBR2, RBR1). The content of the RBRs is then copied into both of the DRRs, which can be read by the CPU or by the DMA controller.

If companding is used during the copy from RBR1 to DRR1 (XCOMPAND = 10b or 11b), the 8-bit compressed data in RBR1 is expanded to a left-justified 16-bit value in DRR1. If companding is disabled, the data copied from RBR[1,2] to DRR[1,2] is justified and bit filled according to the RJUST bits.

19.13.3 Data Transmit Registers (DXR[1,2])

For transmission, the CPU or the DMA controller writes data to one or both of the data transmit registers (see [Figure 19-69](#)). If the serial word length is 16 bits or smaller, only DXR1 is used. If the word length is larger than 16 bits, both DXR1 and DXR2 are used and DXR2 holds the most significant bits. Each frame of transmit data in the McBSP can have one phase or two phases, each with its own serial word length.

Figure 19-69. Data Transmit Registers (DXR2 and DXR1)

DXR2 	
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset	

19.13.3.1 Data Travel From Registers to Data Transmit (DX) Pins

If the serial word length is 16 bits or fewer, data written to DXR1 is copied to transmit shift register 1 (XSR1). From XSR1, the data is shifted onto the DX pin one bit at a time. The XSRs are not accessible.

If the serial word length is more than 16 bits, data written to DXR1 and DXR2 is copied to both transmit shift registers (XSR2, XSR1). From the XSRs, the data is shifted onto the DX pin one bit at a time.

If companding is used during the transfer from DXR1 to XSR1 (XCOMPAND = 10b or 11b), the McBSP compresses the 16-bit data in DXR1 to 8-bit data in the μ -law or A-law format in XSR1. If companding is disabled, the McBSP passes data from the DXR(s) to the XSR(s) without modification.

19.13.4 Serial Port Control Registers (SPCR[1,2])

Each McBSP has two serial port control registers, SPCR1 ([Table 19-78](#)) and SPCR2 ([Table 19-79](#)). These registers enable you to:

- Control various McBSP modes: digital loopback mode (DLB), sign-extension and justification mode for reception (RJUST), clock stop mode (CLKSTP), interrupt modes (RINTM and XINTM), emulation mode (FREE and SOFT)
- Turn on and off the DX-pin delay enabler (DXENA)
- Check the status of receive and transmit operations (RSYNCERR, XSYNCERR, RFULL, XEMPTY, RRDY, XRDY)
- Reset portions of the McBSP (RRST, XRST, FRST, GRST)

19.13.4.1 Serial Port Control 1 Register (SPCR1)

The serial port control 1 register (SPCR1) is shown in [Figure 19-70](#) and described in [Table 19-78](#).

Figure 19-70. Serial Port Control 1 Register (SPCR1)

15	14	13	12	11	10	8
DLB	RJUST		CLKSTP			Reserved
R/W-0	R/W-0			R/W-0		
7	6	5	4	3	2	1 0
DXENA	Reserved	RINTM		RSYNCERR	RFULL	RRDY RRST
R/W-0	R/W-0	R/W-0		R/W-0	R-0	R-0 R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-78. Serial Port Control 1 Register (SPCR1) Field Descriptions

Bit	Field	Value	Description
15	DLB	0	Digital loopback mode bit. DLB disables or enables the digital loopback mode of the McBSP: Disabled Internal DR is supplied by the MDRx pin. Internal FSR and internal MCLKR can be supplied by their respective pins or by the sample rate generator, depending on the mode bits FSRM and CLKRM. Internal DX is supplied by the MDXx pin. Internal FSX and internal CLKX are supplied by their respective pins or are generated internally, depending on the mode bits FSXM and CLKXM.
		1	Enabled Internal receive signals are supplied by internal transmit signals: MDRx connected to MDXx MFSRx connected to MFSXx MCLKR connected to MCLKXx This mode allows you to test serial port code with a single DSP. The McBSP transmitter directly supplies data, frame synchronization, and clocking to the McBSP receiver.
14-13	RJUST	0-3h	Receive sign-extension and justification mode bits. During reception, RJUST determines how data is justified and bit filled before being passed to the data receive registers (DRR1, DRR2). RJUST is ignored if you enable a companding mode with the RCOMPAND bits. In a companding mode, the 8-bit compressed data in RBR1 is expanded to left-justified 16-bit data in DRR1. For more details about the effects of RJUST, see Section 19.7.13 . 0 Right justify the data and zero fill the MSBs. 1h Right justify the data and sign-extend the data into the MSBs. 2h Left justify the data and zero fill the LSBs. 3h Reserved (do not use)
12-11	CLKSTP	0-3h	Clock stop mode bits. CLKSTP allows you to use the clock stop mode to support the SPI master-slave protocol. If you will not be using the SPI protocol, you can clear CLKSTP to disable the clock stop mode. In the clock stop mode, the clock stops at the end of each data transfer. At the beginning of each data transfer, the clock starts immediately (CLKSTP = 10b) or after a half-cycle delay (CLKSTP = 11b). For more details, see Section 19.7.5 . 0-1h Clock stop mode is disabled. 2h Clock stop mode, without clock delay 3h Clock stop mode, with half-cycle clock delay
10-8	Reserved	0	Reserved bits (not available for your use). They are read-only bits and return 0s when read.
7	DXENA	0	DX delay enabler mode bit. DXENA controls the delay enabler for the DX pin. The enabler creates an extra delay for turn-on time (for the length of the delay, see the device-specific data sheet). For more details about the effects of DXENA, see Section 19.8.13 . 0 DX delay enabler off 1 DX delay enabler on
6	Reserved	0	Reserved

Table 19-78. Serial Port Control 1 Register (SPCR1) Field Descriptions (continued)

Bit	Field	Value	Description
5-4	RINTM	0-3h	<p>Receive interrupt mode bits. RINTM determines which event in the McBSP receiver generates a receive interrupt (RINT) request. If RINT is properly enabled inside the CPU, the CPU services the interrupt request; otherwise, the CPU ignores the request.</p> <p>0 The McBSP sends a receive interrupt (RINT) request to the CPU when the RRDY bit changes from 0 to 1, indicating that receive data is ready to be read (the content of RBR[1,2] has been copied to DRR[1,2]):</p> <p>Regardless of the value of RINTM, you can check RRDY to determine whether a word transfer is complete.</p> <p>The McBSP sends a RINT request to the CPU when 16 enabled bits have been received on the DR pin.</p> <p>1h In the multichannel selection mode, the McBSP sends a RINT request to the CPU after every 16-channel block is received in a frame.</p> <p>Outside of the multichannel selection mode, no interrupt request is sent.</p> <p>2h The McBSP sends a RINT request to the CPU when each receive frame-synchronization pulse is detected. The interrupt request is sent even if the receiver is in its reset state.</p> <p>3h The McBSP sends a RINT request to the CPU when the RSYNCERR bit is set, indicating a receive frame-synchronization error.</p> <p>Regardless of the value of RINTM, you can check RSYNCERR to determine whether a receive frame-synchronization error occurred.</p>
3	RSYNCERR		<p>Receive frame-sync error bit. RSYNCERR is set when a receive frame-sync error is detected by the McBSP. If RINTM = 11b, the McBSP sends a receive interrupt (RINT) request to the CPU when RSYNCERR is set. The flag remains set until you write a 0 to it or reset the receiver.</p> <p>0 No error</p> <p>1 Receive frame-synchronization error. For more details about this error, see Section 19.4.3.</p>
2	RFULL		<p>Receiver full bit. RFULL is set when the receiver is full with new data and the previously received data has not been read (receiver-full condition). For more details about this condition, see Section 19.4.2.</p> <p>0 No receiver-full condition</p> <p>1 Receiver-full condition: RSR[1,2] and RBR[1,2] are full with new data, but the previous data in DRR[1,2] has not been read.</p>
1	RRDY		<p>Receiver ready bit. RRDY is set when data is ready to be read from DRR[1,2]. Specifically, RRDY is set in response to a copy from RBR1 to DRR1.</p> <p>If the receive interrupt mode is RINTM = 00b, the McBSP sends a receive interrupt request to the CPU when RRDY changes from 0 to 1.</p> <p>Also, when RRDY changes from 0 to 1, the McBSP sends a receive synchronization event (REVT) signal to the DMA controller.</p> <p>0 Receiver not ready</p> <p>When the content of DRR1 is read, RRDY is automatically cleared.</p> <p>1 Receiver ready: New data can be read from DRR[1,2].</p> <p>Important: If both DRRs are required (word length larger than 16 bits), the CPU or the DMA controller must read from DRR2 first and then from DRR1. As soon as DRR1 is read, the next RBR-to-DRR copy is initiated. If DRR2 is not read first, the data in DRR2 is lost.</p>
0	RRST		<p>Receiver reset bit. You can use RRST to take the McBSP receiver into and out of its reset state. This bit has a negative polarity; RRST = 0 indicates the reset state.</p> <p>To read about the effects of a receiver reset, see Section 19.9.2.</p> <p>0 If you read a 0, the receiver is in its reset state.</p> <p>If you write a 0, you reset the receiver.</p> <p>1 If you read a 1, the receiver is enabled.</p> <p>If you write a 1, you enable the receiver by taking it out of its reset state.</p>

19.13.4.2 Serial Port Control 2 Register (SPCR2)

The serial port control 2 register (SPCR2) is shown in [Figure 19-71](#) and described in [Table 19-79](#).

Figure 19-71. Serial Port Control 2 Register (SPCR2)

15	Reserved				10	9	8
	R-0				R/W-0	R/W-0	
7	6	5	4	3	2	1	0
FRST	GRST	XINTM	XSYNCERR	XEMPTY	XRDY	XRST	
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-79. Serial Port Control 2 Register (SPCR2) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved bits (not available for your use). They are read-only bits and return 0s when read.
9	FREE		Free run bit. When a breakpoint is encountered in the high-level language debugger, FREE determines whether the McBSP transmit and receive clocks continue to run or whether they are affected as determined by the SOFT bit. When one of the clocks stops, the corresponding data transfer (transmission or reception) stops.
8	SOFT		Soft stop bit. When FREE = 0, SOFT determines the response of the McBSP transmit and receive clocks when a breakpoint is encountered in the high-level language debugger. When one of the clocks stops, the corresponding data transfer (transmission or reception) stops.
7	FRST	0	Frame-synchronization logic reset bit. The sample rate generator of the McBSP includes frame-synchronization logic to generate an internal frame-synchronization signal. You can use FRST to take the frame-synchronization logic into and out of its reset state. This bit has a negative polarity; FRST = 0 indicates the reset state. If you read a 0, the frame-synchronization logic is in its reset state. If you write a 0, you reset the frame-synchronization logic. In the reset state, the frame-synchronization logic does not generate a frame-synchronization signal (FSG). 1 If you read a 1, the frame-synchronization logic is enabled. If you write a 1, you enable the frame-synchronization logic by taking it out of its reset state. When the frame-synchronization logic is enabled (FRST = 1) and the sample rate generator as a whole is enabled (GRST = 1), the frame-synchronization logic generates the frame-synchronization signal FSG as programmed.
6	GRST	0	Sample rate generator reset bit. You can use GRST to take the McBSP sample rate generator into and out of its reset state. This bit has a negative polarity; GRST = 0 indicates the reset state. To read about the effects of a sample rate generator reset, see Section 19.9.2 . If you read a 0, the sample rate generator is in its reset state. If you write a 0, you reset the sample rate generator. If GRST = 0 due to a reset, CLKG is driven by the CPU clock divided by 2, and FSG is driven low (inactive). If GRST = 0 due to program code, CLKG and FSG are both driven low (inactive). 1 If you read a 1, the sample rate generator is enabled. If you write a 1, you enable the sample rate generator by taking it out of its reset state. When enabled, the sample rate generator generates the clock signal CLKG as programmed in the sample rate generator registers. If FRST = 1, the generator also generates the frame-synchronization signal FSG as programmed in the sample rate generator registers.

Table 19-79. Serial Port Control 2 Register (SPCR2) Field Descriptions (continued)

Bit	Field	Value	Description
5-4	XINTM	0-3h	Transmit interrupt mode bits. XINTM determines which event in the McBSP transmitter generates a transmit interrupt (XINT) request. If XINT is properly enabled, the CPU services the interrupt request; otherwise, the CPU ignores the request.
		0	The McBSP sends a transmit interrupt (XINT) request to the CPU when the XRDY bit changes from 0 to 1, indicating that transmitter is ready to accept new data (the content of DXR[1,2] has been copied to XSR[1,2]). Regardless of the value of XINTM, you can check XRDY to determine whether a word transfer is complete. The McBSP sends an XINT request to the CPU when 16 enabled bits have been transmitted on the DX pin.
		1h	In the multichannel selection mode, the McBSP sends an XINT request to the CPU after every 16-channel block is transmitted in a frame.
		2h	Outside of the multichannel selection mode, no interrupt request is sent.
		3h	The McBSP sends an XINT request to the CPU when each transmit frame-synchronization pulse is detected. The interrupt request is sent even if the transmitter is in its reset state. The McBSP sends an XINT request to the CPU when the XSYNCERR bit is set, indicating a transmit frame-synchronization error. Regardless of the value of XINTM, you can check XSYNCERR to determine whether a transmit frame-synchronization error occurred.
3	XSYNCERR		Transmit frame-synchronization error bit. XSYNCERR is set when a transmit frame-synchronization error is detected by the McBSP. If XINTM = 11b, the McBSP sends a transmit interrupt (XINT) request to the CPU when XSYNCERR is set. The flag remains set until you write a 0 to it or reset the transmitter. If XINTM = 11b, writing a 1 to XSYNCERR triggers a transmit interrupt just as if a transmit frame-synchronization error occurred. For details about this error see Section 19.4.6 .
		0	No error
		1	Transmit frame-synchronization error
2	XEMPTY	0	Transmitter empty bit. XEMPTY is cleared when the transmitter is ready to send new data but no new data is available (transmitter-empty condition). This bit has a negative polarity; a transmitter-empty condition is indicated by XEMPTY = 0. Typically this indicates that all the bits of the current word have been transmitted but there is no new data in DXR1. XEMPTY is also cleared if the transmitter is reset and then restarted. For more details about this error condition, see Section 19.4.5 .
		1	No transmitter-empty condition
1	XRDY		Transmitter ready bit. XRDY is set when the transmitter is ready to accept new data in DXR[1,2]. Specifically, XRDY is set in response to a copy from DXR1 to XSR1. If the transmit interrupt mode is XINTM = 00b, the McBSP sends a transmit interrupt (XINT) request to the CPU when XRDY changes from 0 to 1. Also, when XRDY changes from 0 to 1, the McBSP sends a transmit synchronization event (XEVT) signal to the DMA controller. 0 Transmitter not ready When DXR1 is loaded, XRDY is automatically cleared. 1 Transmitter ready: DXR[1,2] is ready to accept new data. If both DXRs are needed (word length larger than 16 bits), the CPU or the DMA controller must load DXR2 first and then load DXR1. As soon as DXR1 is loaded, the contents of both DXRs are copied to the transmit shift registers (XSRs), as described in the next step. If DXR2 is not loaded first, the previous content of DXR2 is passed to the XSR2.

Table 19-79. Serial Port Control 2 Register (SPCR2) Field Descriptions (continued)

Bit	Field	Value	Description
0	XRST	0 1	Transmitter reset bit. You can use XRST to take the McBSP transmitter into and out of its reset state. This bit has a negative polarity; XRST = 0 indicates the reset state. To read about the effects of a transmitter reset, see Section 19.9.2 . If you read a 0, the transmitter is in its reset state. If you write a 0, you reset the transmitter. If you read a 1, the transmitter is enabled. If you write a 1, you enable the transmitter by taking it out of its reset state.

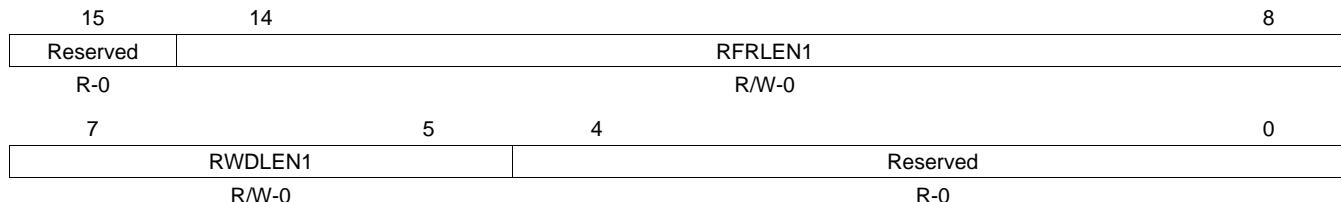
19.13.5 Receive Control Registers (RCR[1, 2])

Each McBSP has two receive control registers, RCR1 ([Table 19-80](#)) and RCR2 ([Table 19-82](#)). These registers enable you to:

- Specify one or two phases for each frame of receive data (RPHASE)
- Define two parameters for phase 1 and (if necessary) phase 2: the serial word length (RWDLEN1, RWDLEN2) and the number of words (RFRLEN1, RFRLEN2)
- Choose a receive companding mode, if any (RCOMPAND)
- Enable or disable the receive frame-synchronization ignore function (RFIG)
- Choose a receive data delay (RDATDLY)

19.13.5.1 Receive Control Register 1 (RCR1)

The receive control register 1 (RCR1) is shown in [Figure 19-72](#) and described in [Table 19-80](#).

Figure 19-72. Receive Control Register 1 (RCR1)

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-80. Receive Control Register 1 (RCR1) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved bits (not available for your use). They are read-only bits and return 0s when read.
14-8	RFRLEN1	0-7Fh	Receive frame length 1 (1 to 128 words). Each frame of receive data can have one or two phases, depending on value that you load into the RPHASE bit. If a single-phase frame is selected, RFRLEN1 in RCR1 selects the number of serial words (8, 12, 16, 20, 24, or 32 bits per word) in the frame. If a dual-phase frame is selected, RFRLEN1 determines the number of serial words in phase 1 of the frame, and RFRLEN2 in RCR2 determines the number of words in phase 2 of the frame. The 7-bit RFRLEN fields allow up to 128 words per phase. See Table 19-81 for a summary of how you determine the frame length. This length corresponds to the number of words or logical time slots or channels per frame-synchronization period. Program the RFRLEN fields with [w minus 1], where w represents the number of words per phase. For example, if you want a phase length of 128 words in phase 1, load 127 into RFRLEN1.

Table 19-80. Receive Control Register 1 (RCR1) Field Descriptions (continued)

Bit	Field	Value	Description
7-5	RWDLEN1	0-7h	Receive word length 1. Each frame of receive data can have one or two phases, depending on the value that you load into the RPHASE bit. If a single-phase frame is selected, RWDLEN1 in RCR1 selects the length for every serial word received in the frame. If a dual-phase frame is selected, RWDLEN1 determines the length of the serial words in phase 1 of the frame, and RWDLEN2 in RCR2 determines the word length in phase 2 of the frame.
		0	8 bits
		1h	12 bits
		2h	16 bits
		3h	20 bits
		4h	24 bits
		5h	32 bits
		6h-7h	Reserved (do not use)
4-0	Reserved	0	Reserved bits (not available for your use). They are read-only bits and return 0s when read.

Table 19-81. Frame Length Formula for Receive Control 1 Register (RCR1)

RPHASE	RFRLEN1	RFRLEN2	Frame Length
0	$0 \leq RFRLEN1 \leq 127$	Not used	(RFRLEN1 + 1) words
1	$0 \leq RFRLEN1 \leq 127$	$0 \leq RFRLEN2 \leq 127$	(RFRLEN1 + 1) + (RFRLEN2 + 1) words

19.13.5.2 Receive Control Register 2 (RCR2)

The receive control register 2 (RCR2) is shown in [Figure 19-73](#) and described in [Table 19-82](#).

Figure 19-73. Receive Control Register 2 (RCR2)

15	14						8
RPHASE		RFRLEN2					
R/W-0		R/W-0					
7	5	4	3	2	1	0	
RWDLEN2		RCOMPAND		RFIG		RDATDLY	
R/W-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-82. Receive Control Register 2 (RCR2) Field Descriptions

Bit	Field	Value	Description
15	RPHASE	0	Receive phase number bit. RPHASE determines whether the receive frame has one phase or two phases. For each phase you can define the serial word length and the number of serial words in the phase. To set up phase 1, program RWDLEN1 (word length) and RFRLEN1 (number of words). To set up phase 2 (if there are two phases), program RWDLEN2 and RFRLEN2. 0 Single-phase frame The receive frame has only one phase, phase 1. 1 Dual-phase frame The receive frame has two phases, phase 1 and phase 2.
14-8		0-7Fh	Receive frame length 2 (1 to 128 words). Each frame of receive data can have one or two phases, depending on value that you load into the RPHASE bit. If a single-phase frame is selected, RFRLEN1 in RCR1 selects the number of serial words (8, 12, 16, 20, 24, or 32 bits per word) in the frame. If a dual-phase frame is selected, RFRLEN1 determines the number of serial words in phase 1 of the frame, and RFRLEN2 in RCR2 determines the number of words in phase 2 of the frame. The 7-bit RFRLEN fields allow up to 128 words per phase. See Table 19-83 for a summary of how to determine the frame length. This length corresponds to the number of words or logical time slots or channels per frame-synchronization period. Program the RFRLEN fields with [w minus 1], where w represents the number of words per phase. For example, if you want a phase length of 128 words in phase 2, load 127 into RFRLEN2.

Table 19-82. Receive Control Register 2 (RCR2) Field Descriptions (continued)

Bit	Field	Value	Description
7-5	RWDLEN2	0-7h	Receive word length 2. Each frame of receive data can have one or two phases, depending on the value that you load into the RPHASE bit. If a single-phase frame is selected, RWDLEN1 in RCR1 selects the length for every serial word received in the frame. If a dual-phase frame is selected, RWDLEN1 determines the length of the serial words in phase 1 of the frame, and RWDLEN2 in RCR2 determines the word length in phase 2 of the frame.
		0	8 bits
		1h	12 bits
		2h	16 bits
		3h	20 bits
		4h	24 bits
		5h	32 bits
		6h-7h	Reserved (do not use)
4-3	RCOMPAND	0-3h	Receive companding mode bits. Companding (COMpress and exPAND) hardware allows compression and expansion of data in either μ -law or A-law format. RCOMPAND allows you to choose one of the following companding modes for the McBSP receiver: For more details about these companding modes, see Section 19.2.2 .
		0	No companding, any size data, MSB received first
		1h	No companding, 8-bit data, LSB received first
		2h	μ -law companding, 8-bit data, MSB received first
		3h	A-law companding, 8-bit data, MSB received first
2	RFIG	0	Receive frame-synchronization ignore bit. If a frame-synchronization pulse starts the transfer of a new frame before the current frame is fully received, this pulse is treated as an unexpected frame-synchronization pulse. For more details about the frame-synchronization error condition, see Figure 19-30 . Setting RFIG causes the serial port to ignore unexpected frame-synchronization signals during reception. For more details on the effects of RFIG, see Section 19.7.10.1 .
		0	Frame-synchronization detect. An unexpected FSR pulse causes the receiver to discard the contents of RSR[1,2] in favor of the new incoming data. The receiver: <ol style="list-style-type: none">1. Aborts the current data transfer2. Sets RSYNCERR in SPCR13. Begins the transfer of a new data word
		1	Frame-synchronization ignore. An unexpected FSR pulse is ignored. Reception continues uninterrupted.
1-0	RDATDLY	0-3h	Receive data delay bits. RDATDLY specifies a data delay of 0, 1, or 2 receive clock cycles after frame-synchronization and before the reception of the first bit of the frame. For more details, see Section 19.7.12 .
		0	0-bit data delay
		1h	1-bit data delay
		2h	2-bit data delay
		3h	Reserved (do not use)

Table 19-83. Frame Length Formula for Receive Control 2 Register (RCR2)

RPHASE	RFRLLEN1	RFRLLEN2	Frame Length
0	$0 \leq RFRLLEN1 \leq 127$	Not used	(RFRLLEN1 + 1) words
1	$0 \leq RFRLLEN1 \leq 127$	$0 \leq RFRLLEN2 \leq 127$	(RFRLLEN1 + 1) + (RFRLLEN2 + 1) words

19.13.6 Transmit Control Registers (XCR1 and XCR2)

Each McBSP has two transmit control registers, XCR1 ([Table 19-84](#)) and XCR2 ([Table 19-86](#)). These registers enable you to:

- Specify one or two phases for each frame of transmit data (XPHASE)
- Define two parameters for phase 1 and (if necessary) phase 2: the serial word length (XWDLEN1,

XWDLEN2) and the number of words (XFRLEN1, XFRLEN2)

- Choose a transmit companding mode, if any (XCOMPAND)
- Enable or disable the transmit frame-sync ignore function (XFIG)
- Choose a transmit data delay (XDATDLY)

19.13.6.1 Transmit Control 1 Register (XCR1)

The transmit control 1 register (XCR1) is shown in [Figure 19-74](#) and described in [Table 19-84](#).

Figure 19-74. Transmit Control 1 Register (XCR1)

15	14				8
Reserved		XFRLEN1			
R-0		R/W-0			
7	5	4			
XWDLEN1		Reserved			0
R/W-0					R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-84. Transmit Control 1 Register (XCR1) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved bit. Read-only; returns 0 when read.
14-8	XFRLEN1	0-7Fh	Transmit frame length 1 (1 to 128 words). Each frame of transmit data can have one or two phases, depending on value that you load into the XPHASE bit. If a single-phase frame is selected, XFRLEN1 in XCR1 selects the number of serial words (8, 12, 16, 20, 24, or 32 bits per word) in the frame. If a dual-phase frame is selected, XFRLEN1 determines the number of serial words in phase 1 of the frame and XFRLEN2 in XCR2 determines the number of words in phase 2 of the frame. The 7-bit XFRLEN fields allow up to 128 words per phase. See Table 19-85 for a summary of how you determine the frame length. This length corresponds to the number of words or logical time slots or channels per frame-synchronization period. Program the XFRLEN fields with [w minus 1], where w represents the number of words per phase. For example, if you want a phase length of 128 words in phase 1, load 127 into XFRLEN1.
7-5	XWDLEN1	0-3h	Transmit word length 1. Each frame of transmit data can have one or two phases, depending on the value that you load into the XPHASE bit. If a single-phase frame is selected, XWDLEN1 in XCR1 selects the length for every serial word transmitted in the frame. If a dual-phase frame is selected, XWDLEN1 determines the length of the serial words in phase 1 of the frame and XWDLEN2 in XCR2 determines the word length in phase 2 of the frame. 0 8 bits 1h 12 bits 2h 16 bits 3h 20 bits 4h 24 bits 5h 32 bits 6h-7h Reserved (do not use)
4-0	Reserved	0	Reserved bits. They are read-only bits and return 0s when read.

Table 19-85. Frame Length Formula for Transmit Control 1 Register (XCR1)

XPHASE	XFRLEN1	XFRLEN2	Frame Length
0	$0 \leq \text{XFRLEN1} \leq 127$	Not used	(XFRLEN1 + 1) words
1	$0 \leq \text{XFRLEN1} \leq 127$	$0 \leq \text{XFRLEN2} \leq 127$	$(\text{XFRLEN1} + 1) + (\text{XFRLEN2} + 1)$ words

19.13.6.2 Transmit Control 2 Register (XCR2)

The transmit control 2 register (XCR2) is shown in [Figure 19-75](#) and described in [Table 19-86](#).

Figure 19-75. Transmit Control 2 Register (XCR2)

	15	14					8
XPHASE			XFRLEN2				
R/W-0			R/W-0				
7	5	4	3	2	1	0	
XWDLEN2			XCOMPAND		XFIG		XDATDLY
R/W-0			R/W-0		R/W-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-86. Transmit Control 2 Register (XCR2) Field Descriptions

Bit	Field	Value	Description
15	XPHASE	0	Transmit phase number bit. XPHASE determines whether the transmit frame has one phase or two phases. For each phase you can define the serial word length and the number of serial words in the phase. To set up phase 1, program XWDLEN1 (word length) and XFRLEN1 (number of words). To set up phase 2 (if there are two phases), program XWDLEN2 and XFRLEN2.
		1	Single-phase frame The transmit frame has only one phase, phase 1. Dual-phase frame The transmit frame has two phases, phase 1 and phase 2.
14-8	XFRLEN2	0-7Fh	Transmit frame length 2 (1 to 128 words). Each frame of transmit data can have one or two phases, depending on value that you load into the XPHASE bit. If a single-phase frame is selected, XFRLEN1 in XCR1 selects the number of serial words (8, 12, 16, 20, 24, or 32 bits per word) in the frame. If a dual-phase frame is selected, XFRLEN1 determines the number of serial words in phase 1 of the frame and XFRLEN2 in XCR2 determines the number of words in phase 2 of the frame. The 7-bit XFRLEN fields allow up to 128 words per phase. See Table 19-87 for a summary of how to determine the frame length. This length corresponds to the number of words or logical time slots or channels per frame-synchronization period. Program the XFRLEN fields with [w minus 1], where w represents the number of words per phase. For example, if you want a phase length of 128 words in phase 1, load 127 into XFRLEN1.
7-5	XWDLEN2	0-7h	Transmit word length 2. Each frame of transmit data can have one or two phases, depending on the value that you load into the XPHASE bit. If a single-phase frame is selected, XWDLEN1 in XCR1 selects the length for every serial word transmitted in the frame. If a dual-phase frame is selected, XWDLEN1 determines the length of the serial words in phase 1 of the frame and XWDLEN2 in XCR2 determines the word length in phase 2 of the frame. 0 8 bits 1h 12 bits 2h 16 bits 3h 20 bits 4h 24 bits 5h 32 bits 6h-7h Reserved (do not use)
4-3	XCOMPAND	0-3h	Transmit companding mode bits. Companding (COMpress and exPAND) hardware allows compression and expansion of data in either μ -law or A-law format. For more details, see Section 19.2.2 . XCOMPAND allows you to choose one of the following companding modes for the McBSP transmitter. For more details about these companding modes, see Section 19.2.2 . 0 No companding, any size data, MSB transmitted first 1h No companding, 8-bit data, LSB transmitted first 2h μ -law companding, 8-bit data, MSB transmitted first 3h A-law companding, 8-bit data, MSB transmitted first

Table 19-86. Transmit Control 2 Register (XCR2) Field Descriptions (continued)

Bit	Field	Value	Description
2	XFIG	0	<p>Transmit frame-synchronization ignore bit. If a frame-synchronization pulse starts the transfer of a new frame before the current frame is fully transmitted, this pulse is treated as an unexpected frame-synchronization pulse.</p> <p>Setting XFIG causes the serial port to ignore unexpected frame-synchronization pulses during transmission.</p>
		1	<p>Frame-synchronization detect. An unexpected FSX pulse causes the transmitter to discard the content of XSR[1,2]. The transmitter:</p> <ol style="list-style-type: none"> 1. Aborts the present transmission 2. Sets XSYNCERR in SPCR2 3. Begins a new transmission from DXR[1,2]. If new data was written to DXR[1,2] since the last DXR[1,2]-to-XSR[1,2] copy, the current value in XSR[1,2] is lost. Otherwise, the same data is transmitted. <p>Frame-synchronization ignore. An unexpected FSX pulse is ignored. Transmission continues uninterrupted.</p>

Table 19-87. Frame Length Formula for Transmit Control 2 Register (XCR2)

XPHASE	XFRLEN1	XFRLEN2	Frame Length
0	$0 \leq \text{XFRLEN1} \leq 127$	Not used	(XFRLEN1 + 1) words
1	$0 \leq \text{XFRLEN1} \leq 127$	$0 \leq \text{XFRLEN2} \leq 127$	(XFRLEN1 + 1) + (XFRLEN2 + 1) words

19.13.7 Sample Rate Generator Registers (SRGR1 and SRGR2)

Each McBSP has two sample rate generator registers, SRGR1 ([Table 19-88](#)) and SRGR2 ([Table 19-89](#)). The sample rate generator can generate a clock signal (CLKG) and a frame-synchronization signal (FSG). The registers SRGR1 and SRGR2 enable you to:

- Select the input clock source for the sample rate generator (CLKSM, in conjunction with the SCLKME bit of PCR)
- Divide down the frequency of CLKG (CLKGDV)
- Select whether internally-generated transmit frame-synchronization pulses are driven by FSG or by activity in the transmitter (FSGM).
- Specify the width of frame-synchronization pulses on FSG (FWID) and specify the period between those pulses (FPER)

When an external source (via the MCLKR or MCLKX pin) provides the input clock source for the sample rate generator:

- If the CLKX/MCLKR pin is used, the polarity of the input clock is selected with CLKXP/CLKRP of PCR.
- The GSYNC bit of SRGR2 allows you to make CLKG synchronized to an external frame-synchronization signal on the FSR pin, so that CLKG is kept in phase with the input clock.

19.13.7.1 Sample Rate Generator 1 Register (SRGR1)

The sample rate generator 1 register is shown in [Figure 19-76](#) and described in [Table 19-88](#).

Figure 19-76. Sample Rate Generator 1 Register (SRGR1)

15	FWID	8
	R/W-0	
7	CLKGDV	0
	R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-88. Sample Rate Generator 1 Register (SRGR1) Field Descriptions

Bit	Field	Value	Description															
15-8	FWID	0-FFh	<p>Frame-synchronization pulse width bits for FSG</p> <p>The sample rate generator can produce a clock signal, CLKG, and a frame-synchronization signal, FSG. For frame-synchronization pulses on FSG, (FWID + 1) is the pulse width in CLKG cycles. The eight bits of FWID allow a pulse width of 1 to 256 CLKG cycles:</p> <p>$0 \leq \text{FWID} \leq 255$</p> <p>$1 \leq (\text{FWID} + 1) \leq 256$ CLKG cycles</p> <p>The period between the frame-synchronization pulses on FSG is defined by the FPER bits.</p>															
7-0	CLKGDV	0-FFh	<p>Divide-down value for CLKG. The sample rate generator can accept an input clock signal and divide it down according to CLKGDV to produce an output clock signal, CLKG. The frequency of CLKG is:</p> <p>$\text{CLKG frequency} = (\text{Input clock frequency}) / (\text{CLKGDV} + 1)$</p> <p>The input clock is selected by the SCLKME and CLKSM bits:</p> <table> <thead> <tr> <th>SCLKME</th> <th>CLKSM</th> <th>Input Clock For Sample Rate Generator</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>LSPCLK</td> </tr> <tr> <td>1</td> <td>0</td> <td>Signal on MCLKR pin</td> </tr> <tr> <td>1</td> <td>1</td> <td>Signal on MCLKX pin</td> </tr> </tbody> </table>	SCLKME	CLKSM	Input Clock For Sample Rate Generator	0	0	Reserved	0	1	LSPCLK	1	0	Signal on MCLKR pin	1	1	Signal on MCLKX pin
SCLKME	CLKSM	Input Clock For Sample Rate Generator																
0	0	Reserved																
0	1	LSPCLK																
1	0	Signal on MCLKR pin																
1	1	Signal on MCLKX pin																

19.13.7.2 Sample Rate Generator 2 Register (SRGR2)

The sample rate generator 2 register (SRGR2) is shown in [Figure 19-77](#) and described in [Table 19-89](#).

Figure 19-77. Sample Rate Generator 2 Register (SRGR2)

15	14	13	12	11	8
GSYNC	Reserved	CLKSM	FSGM		FPER
R/W-0	R/W-0	R/W-1	R/W-0		R/W-0
7			FPER		0
			R/W-0		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-89. Sample Rate Generator 2 Register (SRGR2) Field Descriptions

Bit	Field	Value	Description																		
15	GSYNC		<p>Clock synchronization mode bit for CLKG. GSYNC is used only when the input clock source for the sample rate generator is external—on the MCLKR pin.</p> <p>When GSYNC = 1, the clock signal (CLKG) and the frame-synchronization signal (FSG) generated by the sample rate generator are made dependent on pulses on the FSR pin.</p> <p>0 No clock synchronization</p> <p>CLKG oscillates without adjustment, and FSG pulses every (FPER + 1) CLKG cycles.</p> <p>1 Clock synchronization</p> <ul style="list-style-type: none"> CLKG is adjusted as necessary so that it is synchronized with the input clock on the MCLKR pin. FSG pulses. FSG only pulses in response to a pulse on the FSR pin. <p>The frame-synchronization period defined in FPER is ignored.</p> <p>For more details, see Section 19.3.3.</p>																		
14	Reserved		Reserved																		
13	CLKSM	0	<p>Sample rate generator input clock mode bit. The sample rate generator can accept an input clock signal and divide it down according to CLKGDV to produce an output clock signal, CLKG. The frequency of CLKG is:</p> $\text{CLKG frequency} = (\text{input clock frequency}) / (\text{CLKGDV} + 1)$ <p>CLKSM is used in conjunction with the SCLKME bit to determine the source for the input clock.</p> <p>A reset selects the CPU clock as the input clock and forces the CLKG frequency to $\frac{1}{2}$ the LSPCLK frequency.</p> <p>The input clock for the sample rate generator is taken from the MCLKR pin, depending on the value of the SCLKME bit of PCR:</p> <table> <thead> <tr> <th>SCLKME</th> <th>CLKSM</th> <th>Input Clock For Sample Rate Generator</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>Signal on MCLKR pin</td> </tr> </tbody> </table> <p>1 The input clock for the sample rate generator is taken from the LSPCLK or from the MCLKX pin, depending on the value of the SCLKME bit of PCR:</p> <table> <thead> <tr> <th>SCLKME</th> <th>CLKSM</th> <th>Input Clock For Sample Rate Generator</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>LSPCLK</td> </tr> <tr> <td>1</td> <td>1</td> <td>Signal on MCLKX pin</td> </tr> </tbody> </table>	SCLKME	CLKSM	Input Clock For Sample Rate Generator	0	0	Reserved	1	0	Signal on MCLKR pin	SCLKME	CLKSM	Input Clock For Sample Rate Generator	0	1	LSPCLK	1	1	Signal on MCLKX pin
SCLKME	CLKSM	Input Clock For Sample Rate Generator																			
0	0	Reserved																			
1	0	Signal on MCLKR pin																			
SCLKME	CLKSM	Input Clock For Sample Rate Generator																			
0	1	LSPCLK																			
1	1	Signal on MCLKX pin																			
12	FSGM		<p>Sample rate generator transmit frame-synchronization mode bit. The transmitter can get frame synchronization from the FSX pin (FSXM = 0) or from inside the McBSP (FSXM = 1). When FSXM = 1, the FSGM bit determines how the McBSP supplies frame-synchronization pulses.</p> <p>0 If FSXM = 1, the McBSP generates a transmit frame-synchronization pulse when the content of DXR[1,2] is copied to XSR[1,2].</p> <p>1 If FSXM = 1, the transmitter uses frame-synchronization pulses generated by the sample rate generator. Program the FWID bits to set the width of each pulse. Program the FPER bits to set the period between pulses.</p>																		
11-0	FPER	0-FFFh	<p>Frame-synchronization period bits for FSG. The sample rate generator can produce a clock signal, CLKG, and a frame-synchronization signal, FSG. The period between frame-synchronization pulses on FSG is (FPER + 1) CLKG cycles. The 12 bits of FPER allow a frame-synchronization period of 1 to 4096 CLKG cycles:</p> $0 \leq \text{FPER} \leq 4095$ $1 \leq (\text{FPER} + 1) \leq 4096 \text{ CLKG cycles}$ <p>The width of each frame-synchronization pulse on FSG is defined by the FWID bits.</p>																		

19.13.8 Multichannel Control Registers (MCR[1,2])

Each McBSP has two multichannel control registers. MCR1 ([Table 19-90](#)) has control and status bits (with an R prefix) for multichannel selection operation in the receiver. MCR2 ([Table 19-91](#)) contains the same type of bits (bit with an X prefix) for the transmitter. These registers enable you to:

- Enable all channels or only selected channels for reception (RMCM)
- Choose which channels are enabled/disabled and masked/unmasked for transmission (XMCM)
- Specify whether two partitions (32 channels at a time) or eight partitions (128 channels at a time) can be used (RMCME for reception, XMCME for transmission)
- Assign blocks of 16 channels to partitions A and B when the 2-partition mode is selected (RPABLK and RPBLK for reception, XPABLK and XPBLK for transmission)
- Determine which block of 16 channels is currently involved in a data transfer (RCBLK for reception, XCBLK for transmission)

19.13.8.1 Multichannel Control 1 Register (MCR1)

The multichannel control 1 register (MCR1) is shown in [Figure 19-78](#) and described in [Table 19-90](#).

Figure 19-78. Multichannel Control 1 Register (MCR1)

15	Reserved				10	9	8
7	6	5	4	R-0	2	1	0
RPBBLK	RPABLK			RCBLK		Reserved	RMCM
R/W-0	R/W-0			R-0		R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-90. Multichannel Control 1 Register (MCR1) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved bits (not available for your use). They are read-only bits and return 0s when read.
9	RMCME	0	<p>Receive multichannel partition mode bit. RMCME is only applicable if channels can be individually enabled or disabled for reception (RMCM = 1).</p> <p>RMCME determines whether only 32 channels or all 128 channels are to be individually selectable.</p> <p>2-partition mode</p> <p>Only partitions A and B are used. You can control up to 32 channels in the receive multichannel selection mode (RMCM = 1).</p> <p>Assign 16 channels to partition A with the RPABLK bits.</p> <p>Assign 16 channels to partition B with the RPBLK bits.</p> <p>You control the channels with the appropriate receive channel enable registers:</p> <p>RCERA: Channels in partition A</p> <p>RCERB: Channels in partition B</p>
		1	<p>8-partition mode</p> <p>All partitions (A through H) are used. You can control up to 128 channels in the receive multichannel selection mode. You control the channels with the appropriate receive channel enable registers:</p> <p>RCERA: Channels 0 through 15</p> <p>RCERB: Channels 16 through 31</p> <p>RCERC: Channels 32 through 47</p> <p>RCERD: Channels 48 through 63</p> <p>RCERE: Channels 64 through 79</p> <p>RCERF: Channels 80 through 95</p> <p>RCERG: Channels 96 through 111</p> <p>RCERH: Channels 112 through 127</p>

Table 19-90. Multichannel Control 1 Register (MCR1) Field Descriptions (continued)

Bit	Field	Value	Description
8-7	RPBBLK	0-3h	<p>Receive partition B block bits</p> <p>RPBBLK is only applicable if channels can be individually enabled or disabled (RMCM = 1) and the 2-partition mode is selected (RMCME = 0). Under these conditions, the McBSP receiver can accept or ignore data in any of the 32 channels that are assigned to partitions A and B of the receiver.</p> <p>The 128 receive channels of the McBSP are divided equally among 8 blocks (0 through 7). When RPBBLK is applicable, use RPBBLK to assign one of the odd-numbered blocks (1, 3, 5, or 7) to partition B. Use the RPABLK bits to assign one of the even-numbered blocks (0, 2, 4, or 6) to partition A.</p> <p>If you want to use more than 32 channels, you can change block assignments dynamically. You can assign a new block to one partition while the receiver is handling activity in the other partition. For example, while the block in partition A is active, you can change which block is assigned to partition B. The RCBLK bits are regularly updated to indicate which block is active.</p> <p>When XMCM = 11b (for symmetric transmission and reception), the transmitter uses the receive block bits (RPABLK and RPBBLK) rather than the transmit block bits (XPABLK and XPBBLK).</p> <ul style="list-style-type: none"> 0 Block 1: channels 16 through 31 1h Block 3: channels 48 through 63 2h Block 5: channels 80 through 95 3h Block 7: channels 112 through 127
6-5	RPABLK	0-3h	<p>Receive partition A block bits</p> <p>RPABLK is only applicable if channels can be individually enabled or disabled (RMCM = 1) and the 2-partition mode is selected (RMCME = 0). Under these conditions, the McBSP receiver can accept or ignore data in any of the 32 channels that are assigned to partitions A and B of the receiver. See the description for RPBBLK (bits 8-7) for more information about assigning blocks to partitions A and B.</p> <ul style="list-style-type: none"> 0 Block 0: channels 0 through 15 1h Block 2: channels 32 through 47 2h Block 5: channels 64 through 79 3h Block 7: channels 96 through 111
4-2	RCBLK	0-7h	<p>Receive current block indicator. RCBLK indicates which block for 16 channels is involved in the current McBSP reception:</p> <ul style="list-style-type: none"> 0 Block 0: channels 0 through 15 1h Block 1: channels 16 through 31 2h Block 2: channels 32 through 47 3h Block 3: channels 48 through 63 4h Block 4: channels 64 through 79 5h Block 5: channels 80 through 95 6h Block 6: channels 96 through 111 7h Block 7: channels 112 through 127
1	Reserved	0	Reserved bits (not available for your use). They are read-only bits and return 0s when read.
0	RMCM		<p>Receive multichannel selection mode bit. RMCM determines whether all channels or only selected channels are enabled for reception:</p> <ul style="list-style-type: none"> 0 All 128 channels are enabled. 1 Multichanneled selection mode. Channels can be individually enabled or disabled. <p>The only channels enabled are those selected in the appropriate receive channel enable registers (RCERs). The way channels are assigned to the RCERs depends on the number of receive channel partitions (2 or 8), as defined by the RMCME bit.</p>

19.13.8.2 Multichannel Control 2 Register (MCR2)

The multichannel control 2 register (MCR2) is shown in [Figure 19-79](#) and described in [Table 19-91](#).

Figure 19-79. Multichannel Control 2 Register (MCR2)

15	Reserved				10	9	8
	R-0					R/W-0	R/W-0
7	6	5	4		2	1	0
XPBBLK	XPABLK		XCBLK			XMCM	
R/W-0	R/W-0		R-0			R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-91. Multichannel Control 2 Register (MCR2) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved bits (not available for your use). They are read-only bits and return 0s when read.
9	XMCME	0	<p>Transmit multichannel partition mode bit. XMCME determines whether only 32 channels or all 128 channels are to be individually selectable. XMCME is only applicable if channels can be individually disabled/enabled or masked/unmasked for transmission (XMCM is nonzero).</p> <p>2-partition mode. Only partitions A and B are used. You can control up to 32 channels in the transmit multichannel selection mode selected with the XMCM bits.</p> <p>If XMCM = 01b or 10b, assign 16 channels to partition A with the XPABLK bits. Assign 16 channels to partition B with the XPBBLK bits.</p> <p>If XMCM = 11b(for symmetric transmission and reception), assign 16 channels to receive partition A with the RPABLK bits. Assign 16 channels to receive partition B with the RPBBLK bits.</p> <p>You control the channels with the appropriate transmit channel enable registers:</p> <p>XCERA: Channels in partition A</p> <p>XCERB: Channels in partition B</p>
		1	<p>8-partition mode. All partitions (A through H) are used. You can control up to 128 channels in the transmit multichannel selection mode selected with the XMCM bits.</p> <p>You control the channels with the appropriate transmit channel enable registers:</p> <p>XCERA: Channels 0 through 15</p> <p>XCERB: Channels 16 through 31</p> <p>XCERC: Channels 32 through 47</p> <p>XCERD: Channels 48 through 63</p> <p>XCERE: Channels 64 through 79</p> <p>XCERF: Channels 80 through 95</p> <p>XCERG: Channels 96 through 111</p> <p>XCERH: Channels 112 through 127</p>

Table 19-91. Multichannel Control 2 Register (MCR2) Field Descriptions (continued)

Bit	Field	Value	Description																
8-7	XPBBLK	0-3h	<p>Transmit partition B block bits</p> <p>XPBBLK is only applicable if channels can be individually disabled/enabled and masked/unmasked (XMCM is nonzero) and the 2-partition mode is selected (XMCME = 0). Under these conditions, the McBSP transmitter can transmit or withhold data in any of the 32 channels that are assigned to partitions A and B of the transmitter.</p> <p>The 128 transmit channels of the McBSP are divided equally among 8 blocks (0 through 7). When XPBBLK is applicable, use XPBBLK to assign one of the odd-numbered blocks (1, 3, 5, or 7) to partition B, as shown in the following table. Use the XPABLK bit to assign one of the even-numbered blocks (0, 2, 4, or 6) to partition A.</p> <p>If you want to use more than 32 channels, you can change block assignments dynamically. You can assign a new block to one partition while the transmitter is handling activity in the other partition. For example, while the block in partition A is active, you can change which block is assigned to partition B. The XCBLK bits are regularly updated to indicate which block is active.</p> <p>When XMCM = 11b (for symmetric transmission and reception), the transmitter uses the receive block bits (RPABLK and RPBBLK) rather than the transmit block bits (XPABLK and XPBBLK).</p> <table> <tr> <td>0</td><td>Block 1: channels 16 through 31</td></tr> <tr> <td>1h</td><td>Block 3: channels 48 through 63</td></tr> <tr> <td>2h</td><td>Block 5: channels 80 through 95</td></tr> <tr> <td>3h</td><td>Block 7: channels 112 through 127</td></tr> </table>	0	Block 1: channels 16 through 31	1h	Block 3: channels 48 through 63	2h	Block 5: channels 80 through 95	3h	Block 7: channels 112 through 127								
0	Block 1: channels 16 through 31																		
1h	Block 3: channels 48 through 63																		
2h	Block 5: channels 80 through 95																		
3h	Block 7: channels 112 through 127																		
6-5	XPABLK		<p>Transmit partition A block bits. XPABLK is only applicable if channels can be individually disabled/enabled and masked/unmasked (XMCM is nonzero) and the 2-partition mode is selected (XMCME = 0). Under these conditions, the McBSP transmitter can transmit or withhold data in any of the 32 channels that are assigned to partitions A and B of the transmitter. See the description for XPBBLK (bits 8-7) for more information about assigning blocks to partitions A and B.</p> <table> <tr> <td>0</td><td>Block 0: channels 0 through 15</td></tr> <tr> <td>1h</td><td>Block 2: channels 32 through 47</td></tr> <tr> <td>2h</td><td>Block 4: channels 64 through 79</td></tr> <tr> <td>3h</td><td>Block 6: channels 96 through 111</td></tr> </table>	0	Block 0: channels 0 through 15	1h	Block 2: channels 32 through 47	2h	Block 4: channels 64 through 79	3h	Block 6: channels 96 through 111								
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1h	Block 2: channels 32 through 47																		
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3h	Block 6: channels 96 through 111																		
4-2	XCBLK		<p>Transmit current block indicator. XCBLK indicates which block of 16 channels is involved in the current McBSP transmission:</p> <table> <tr> <td>0</td><td>Block 0: channels 0 through 15</td></tr> <tr> <td>1h</td><td>Block 1: channels 16 through 31</td></tr> <tr> <td>2h</td><td>Block 2: channels 32 through 47</td></tr> <tr> <td>3h</td><td>Block 3: channels 48 through 63</td></tr> <tr> <td>4h</td><td>Block 4: channels 64 through 79</td></tr> <tr> <td>5h</td><td>Block 5: channels 80 through 95</td></tr> <tr> <td>6h</td><td>Block 6: channels 96 through 111</td></tr> <tr> <td>7h</td><td>Block 7: channels 112 through 127</td></tr> </table>	0	Block 0: channels 0 through 15	1h	Block 1: channels 16 through 31	2h	Block 2: channels 32 through 47	3h	Block 3: channels 48 through 63	4h	Block 4: channels 64 through 79	5h	Block 5: channels 80 through 95	6h	Block 6: channels 96 through 111	7h	Block 7: channels 112 through 127
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1h	Block 1: channels 16 through 31																		
2h	Block 2: channels 32 through 47																		
3h	Block 3: channels 48 through 63																		
4h	Block 4: channels 64 through 79																		
5h	Block 5: channels 80 through 95																		
6h	Block 6: channels 96 through 111																		
7h	Block 7: channels 112 through 127																		
1-0	XMCM	0-3h	<p>Transmit multichannel selection mode bits. XMCM determines whether all channels or only selected channels are enabled and unmasked for transmission. For more details on how the channels are affected, see Section 19.5.7.</p> <table> <tr> <td>0</td><td>No transmit multichannel selection mode is on. All channels are enabled and unmasked. No channels can be disabled or masked.</td></tr> <tr> <td>1h</td><td>All channels are disabled unless they are selected in the appropriate transmit channel enable registers (XCERs). If enabled, a channel in this mode is also unmasked.</td></tr> <tr> <td>2h</td><td>The XMCME bit determines whether 32 channels or 128 channels are selectable in XCERs.</td></tr> <tr> <td>3h</td><td>All channels are enabled, but they are masked unless they are selected in the appropriate transmit channel enable registers (XCERs).</td></tr> </table> <p>The XMCME bit determines whether 32 channels or 128 channels are selectable in XCERs.</p> <p>This mode is used for symmetric transmission and reception.</p> <p>All channels are disabled for transmission unless they are enabled for reception in the appropriate receive channel enable registers (RCERs). Once enabled, they are masked unless they are also selected in the appropriate transmit channel enable registers (XCERs).</p> <p>The XMCME bit determines whether 32 channels or 128 channels are selectable in RCERs and XCERs.</p>	0	No transmit multichannel selection mode is on. All channels are enabled and unmasked. No channels can be disabled or masked.	1h	All channels are disabled unless they are selected in the appropriate transmit channel enable registers (XCERs). If enabled, a channel in this mode is also unmasked.	2h	The XMCME bit determines whether 32 channels or 128 channels are selectable in XCERs.	3h	All channels are enabled, but they are masked unless they are selected in the appropriate transmit channel enable registers (XCERs).								
0	No transmit multichannel selection mode is on. All channels are enabled and unmasked. No channels can be disabled or masked.																		
1h	All channels are disabled unless they are selected in the appropriate transmit channel enable registers (XCERs). If enabled, a channel in this mode is also unmasked.																		
2h	The XMCME bit determines whether 32 channels or 128 channels are selectable in XCERs.																		
3h	All channels are enabled, but they are masked unless they are selected in the appropriate transmit channel enable registers (XCERs).																		

19.13.9 Pin Control Register (PCR)

Each McBSP has one pin control register (PCR). [Table 19-92](#) describes the bits of PCR. This register enables you to:

- Choose a frame-synchronization mode for the transmitter (FSXM) and for the receiver (FSRM)
- Choose a clock mode for transmitter (CLKXM) and for the receiver (CLKRM)
- Select the input clock source for the sample rate generator (SCLKME, in conjunction with the CLKSM bit of SRGR2)
- Choose whether frame-synchronization signals are active low or active high (FSXP for transmission, FSRP for reception)
- Specify whether data is sampled on the falling edge or the rising edge of the clock signals (CLKXP for transmission, CLKRP for reception)

The pin control register (PCR) is shown in [Figure 19-80](#) and described in [Table 19-92](#).

Figure 19-80. Pin Control Register (PCR)

15	12	11	10	9	8
Reserved		FSXM	FSRM	CLKXM	CLKRM
R-0		R/W-0	R/W-0	R/W-0	R/W-0
7	6	4	3	2	1
SCLKME	Reserved	FSXP	FSRP	CLKXP	CLKRP
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-92. Pin Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
15:12	Reserved	0	Reserved bit (not available for your use). It is a read-only bit and returns a 0 when read.
11	FSXM	0	Transmit frame-synchronization mode bit. FSXM determines whether transmit frame-synchronization pulses are supplied externally or internally. The polarity of the signal on the FSX pin is determined by the FSXP bit.
		1	Transmit frame synchronization is supplied by an external source via the FSX pin. Transmit frame synchronization is generated internally by the Sample Rate generator, as determined by the FSGM bit of SRGR2.
10	FSRM	0	Receive frame-synchronization mode bit. FSRM determines whether receive frame-synchronization pulses are supplied externally or internally. The polarity of the signal on the FSR pin is determined by the FSRP bit.
		1	Receive frame synchronization is supplied by an external source via the FSR pin. Receive frame synchronization is supplied by the sample rate generator. FSR is an output pin reflecting internal FSR, except when GSYNC = 1 in SRGR2.

Table 19-92. Pin Control Register (PCR) Field Descriptions (continued)

Bit	Field	Value	Description																
9	CLKXM	0	Transmit clock mode bit. CLKXM determines whether the source for the transmit clock is external or internal, and whether the MCLKX pin is an input or an output. The polarity of the signal on the MCLKX pin is determined by the CLKXP bit. In the clock stop mode (CLKSTP = 10b or 11b), the McBSP can act as a master or as a slave in the SPI protocol. If the McBSP is a master, make sure that CLKX is an output. If the McBSP is a slave, make sure that CLKX is an input. Not in clock stop mode (CLKSTP = 00b or 01b): The transmitter gets its clock signal from an external source via the MCLKX pin.																
			Internal CLKX is driven by the sample rate generator of the McBSP. The MCLKX pin is an output pin that reflects internal CLKX.																
			In clock stop mode (CLKSTP = 10b or 11b): The McBSP is a slave in the SPI protocol. The internal transmit clock (CLKX) is driven by the SPI master via the MCLKX pin. The internal receive clock (MCLKR) is driven internally by CLKX, so that both the transmitter and the receiver are controlled by the external master clock.																
		0	The McBSP is a master in the SPI protocol. The sample rate generator drives the internal transmit clock (CLKX). Internal CLKX is reflected on the MCLKX pin to drive the shift clock of the SPI-compliant slaves in the system. Internal CLKX also drives the internal receive clock (MCLKR), so that both the transmitter and the receiver are controlled by the internal master clock.																
			1																
		1	Receive clock mode bit. The role of CLKRM and the resulting effect on the MCLKR pin depend on whether the McBSP is in the digital loopback mode (DLB = 1). The polarity of the signal on the MCLKR pin is determined by the CLKRP bit. Not in digital loopback mode (DLB = 0): The MCLKR pin is an input pin that supplies the internal receive clock (MCLKR). Internal MCLKR is driven by the sample rate generator of the McBSP. The MCLKR pin is an output pin that reflects internal MCLKR.																
			In digital loopback mode (DLB = 1): The MCLKR pin is in the high impedance state. The internal receive clock (MCLKR) is driven by the internal transmit clock (CLKX). CLKX is derived according to the CLKXM bit. Internal MCLKR is driven by internal CLKX. The MCLKR pin is an output pin that reflects internal MCLKR. CLKX is derived according to the CLKXM bit.																
			0																
			1																
		7	Sample rate generator input clock mode bit. The sample rate generator can produce a clock signal, CLKG. The frequency of CLKG is: $\text{CLKG freq.} = (\text{Input clock frequency}) / (\text{CLKGDV} + 1)$ SCLKME is used in conjunction with the CLKSM bit to select the input clock. <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SCLKME</th> <th>CLKSM</th> <th>Input Clock For Sample Rate Generator</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>LSPCLK</td> </tr> </tbody> </table> The input clock for the sample rate generator is taken from the MCLKR pin or from the MCLKX pin, depending on the value of the CLKSM bit of SRGR2: <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SCLKME</th> <th>CLKSM</th> <th>Input Clock For Sample Rate Generator</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>Signal on MCLKR pin</td> </tr> <tr> <td>1</td> <td>1</td> <td>Signal on MCLKX pin</td> </tr> </tbody> </table>	SCLKME	CLKSM	Input Clock For Sample Rate Generator	0	0	Reserved	0	1	LSPCLK	SCLKME	CLKSM	Input Clock For Sample Rate Generator	1	0	Signal on MCLKR pin	1
SCLKME	CLKSM	Input Clock For Sample Rate Generator																	
0	0	Reserved																	
0	1	LSPCLK																	
SCLKME	CLKSM	Input Clock For Sample Rate Generator																	
1	0	Signal on MCLKR pin																	
1	1	Signal on MCLKX pin																	
1																			
0																			
1																			
0																			
1																			
6-4	Reserved		Reserved																
3	FSXP	0	Transmit frame-synchronization polarity bit. FSXP determines the polarity of FSX as seen on the FSX pin. Transmit frame-synchronization pulses are active high.																
			Transmit frame-synchronization pulses are active low.																
2	FSRP	0	Receive frame-synchronization polarity bit. FSRP determines the polarity of FSR as seen on the FSR pin. Receive frame-synchronization pulses are active high.																
			Receive frame-synchronization pulses are active low.																
1		1																	

Table 19-92. Pin Control Register (PCR) Field Descriptions (continued)

Bit	Field	Value	Description
1	CLKXP	0	Transmit clock polarity bit. CLKXP determines the polarity of CLKX as seen on the MCLKX pin. Transmit data is sampled on the rising edge of CLKX.
		1	Transmit data is sampled on the falling edge of CLKX.
0	CLKRP	0	Receive clock polarity bit. CLKRP determines the polarity of CLKR as seen on the MCLKR pin. Receive data is sampled on the falling edge of MCLKR.
		1	Receive data is sampled on the rising edge of MCLKR.

Table 19-93. Pin Configuration

Pin	Selected as Output When ...	Selected as Input When ...
CLKX	CLKXM = 1	CLKXM = 0
FSX	FSXM = 1	FSXM = 0
CLKR	CLKRM = 1	CLKRM = 0
FSR	FSRM = 1	FSRM = 0

19.13.10 Receive Channel Enable Registers (RCERA, RCERB, RCERC, RCERD, RCERE, RCERF, RCERG, RCERH)

Each McBSP has eight receive channel enable registers of the format shown in [Figure 19-81](#). There is one enable register for each of the receive partitions: A, B, C, D, E, F, G, and H. [Table 19-94](#) provides a summary description that applies to any bit x of a receive channel enable register.

These memory-mapped registers are only used when the receiver is configured to allow individual enabling and disabling of the channels (RMCM = 1). For more details about the way these registers are used, see [Section 19.13.10.1](#).

The receive channel enable registers (RCERA...RCERH) are shown in [Figure 19-81](#) and described in [Table 19-94](#).

Figure 19-81. Receive Channel Enable Registers (RCERA...RCERH)

15	14	13	12	11	10	9	8
RCE15	RCE14	RCE13	RCE12	RCE11	RCE10	RCE9	RCE8
R/W-0							
7	6	5	4	3	2	1	0
RCE7	RCE6	RCE5	RCE4	RCE3	RCE2	RCE1	RCE0
R/W-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-94. Receive Channel Enable Registers (RCERA...RCERH) Field Descriptions

Bit	Field	Value	Description
15-0	RCE _x	0	Receive channel enable bit. For receive multichannel selection mode (RMCM = 1): Disable the channel that is mapped to RCE _x . Enable the channel that is mapped to RCE _x .

19.13.10.1 RCERs Used in the Receive Multichannel Selection Mode

For multichannel selection operation, the assignment of channels to the RCERs depends on whether 32 or 128 channels are individually selectable, as defined by the RMCM bit. For each of these two cases, [Table 19-95](#) shows which block of channels is assigned to each of the RCERs used. For each RCER, the table shows which channel is assigned to each of the bits.

Table 19-95. Use of the Receive Channel Enable Registers

Number of Selectable Channels	Block Assignments		Channel Assignments	
	RCERx	Block Assigned	Bit in RCERx	Channel Assigned
32 (RMCME = 0)	RCERA	Channels n to (n + 15) The block of channels is chosen with the RPABLK bits.	RCE0 RCE1 RCE2 : RCE15	Channel n Channel (n + 1) Channel (n + 2) : Channel (n + 15)
	RCERB	Channels m to (m + 15) The block of channels is chosen with the RPBBLK bits.	RCE0 RCE1 RCE2 : RCE15	Channel m Channel (m + 1) Channel (m + 2) : Channel (m + 15)
128 (RMCME = 1)	RCERA	Block 0	RCE0 RCE1 RCE2 : RCE15	Channel 0 Channel 1 Channel 2 : Channel 15
	RCERB	Block 1	RCE0 RCE1 RCE2 : RCE15	Channel 16 Channel 17 Channel 18 : Channel 31
	RCERC	Block 2	RCE0 RCE1 RCE2 : RCE15	Channel 32 Channel 33 Channel 34 : Channel 47
	RCERD	Block 3	RCE0 RCE1 RCE2 : RCE15	Channel 48 Channel 49 Channel 50 : Channel 63
	RCERE	Block 4	RCE0 RCE1 RCE2 : RCE15	Channel 64 Channel 65 Channel 66 : Channel 79
	RCERF	Block 5	RCE0 RCE1 RCE2 : RCE15	Channel 80 Channel 81 Channel 82 : Channel 95
	RCERG	Block 6	RCE0 RCE1 RCE2 : RCE15	Channel 96 Channel 97 Channel 98 : Channel 111

Table 19-95. Use of the Receive Channel Enable Registers (continued)

Number of Selectable Channels	Block Assignments		Channel Assignments	
	RCERx	Block Assigned	Bit in RCERx	Channel Assigned
	RCERH	Block 7	RCE0	Channel 112
			RCE1	Channel 113
			RCE2	Channel 114
			:	:
			RCE15	Channel 127

19.13.11 Transmit Channel Enable Registers (XCERA, XCERB, XCERC, XCERD, XCERE, XCERF, XCERG, XCERH)

Each McBSP has eight transmit channel enable registers of the form shown in [Figure 19-82](#). There is one for each of the transmit partitions: A, B, C, D, E, F, G, and H. [Table 19-96](#) provides a summary description that applies to each bit XCE_x of a transmit channel enable register.

The XCERs are only used when the transmitter is configured to allow individual disabling/enabling and masking/unmasking of the channels (XMCM is nonzero).

The transmit channel enable registers (XCERA...XCERH) are shown in [Figure 19-82](#) and described in [Table 19-96](#).

Figure 19-82. Transmit Channel Enable Registers (XCERA...XCERH)

15	14	13	12	11	10	9	8
XCE15	XCE14	XCE13	XCE12	XCE11	XCE10	XCE9	XCE8
R/W-0							
7	6	5	4	3	2	1	0
XCE7	XCE6	XCE5	XCE4	XCE3	XCE2	XCE1	XCE0
R/W-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19-96. Transmit Channel Enable Registers (XCERA...XCERH) Field Descriptions

Bit	Field	Value	Description
15-0	XCE _x		Transmit channel enable bit. The role of this bit depends on which transmit multichannel selection mode is selected with the XMCM bits. For multichannel selection when XMCM = 01b (all channels disabled unless selected): 0 Disable and mask the channel that is mapped to XCE _x . 1 Enable and unmask the channel that is mapped to XCE _x .
		0	For multichannel selection when XMCM = 10b (all channels enabled but masked unless selected): 0 Mask the channel that is mapped to XCE _x . 1 Unmask the channel that is mapped to XCE _x .
		1	For multichannel selection when XMCM = 11b (all channels masked unless selected): 0 Mask the channel that is mapped to XCE _x . Even if the channel is enabled by the corresponding receive channel enable bit, this channel's data cannot appear on the DX pin. 1 Unmask the channel that is mapped to XCE _x . If the channel is also enabled by the corresponding receive channel enable bit, full transmission can occur.

19.13.11.1 XCERs Used in a Transmit Multichannel Selection Mode

For multichannel selection operation, the assignment of channels to the XCERs depends on whether 32 or 128 channels are individually selectable, as defined by the XMCME bit. These two cases are shown in [Table 19-97](#). The table shows which block of channels is assigned to each XCER that is used. For each XCER, the table shows which channel is assigned to each of the bits.

NOTE: When XMCM = 11b (for symmetric transmission and reception), the transmitter uses the receive channel enable registers (RCERs) to enable channels and uses the XCERs to unmask channels for transmission.

Table 19-97. Use of the Transmit Channel Enable Registers

Number of Selectable Channels	Block Assignments			Channel Assignments
	XCERx	Block Assigned	Bit in XCERx	Channel Assigned
32 (XMCME = 0)	XCERA	Channels n to (n + 15)	XCE0	Channel n
			XCE1	Channel (n + 1)
			XCE2	Channel (n + 2)
			:	:
			XCE15	Channel (n + 15)
	XCERB	Channels m to (m + 15)	XCE0	Channel m
			XCE1	Channel (m + 1)
			XCE2	Channel (m + 2)
			:	:
			XCE15	Channel (m + 15)
128 (XMCME = 1)	XCERA	Block 0	XCE0	Channel 0
			XCE1	Channel 1
			XCE2	Channel 2
			:	:
			XCE15	Channel 15
	XCERB	Block 1	XCE0	Channel 16
			XCE1	Channel 17
			XCE2	Channel 18
			:	:
			XCE15	Channel 31
	XCERC	Block 2	XCE0	Channel 32
			XCE1	Channel 33
			XCE2	Channel 34
			:	:
			XCE15	Channel 47
	XCERD	Block 3	XCE0	Channel 48
			XCE1	Channel 49
			XCE2	Channel 50
			:	:
			XCE15	Channel 63

Table 19-97. Use of the Transmit Channel Enable Registers (continued)

Number of Selectable Channels	Block Assignments		Channel Assignments	
	XCERx	Block Assigned	Bit in XCERx	Channel Assigned
XCERE	Block 4		XCE0	Channel 64
			XCE1	Channel 65
			XCE2	Channel 66
			:	:
			XCE15	Channel 79
XCERF	Block 5		XCE0	Channel 80
			XCE1	Channel 81
			XCE2	Channel 82
			:	:
			XCE15	Channel 95
XCERG	Block 6		XCE0	Channel 96
			XCE1	Channel 97
			XCE2	Channel 98
			:	:
			XCE15	Channel 111
XCERH	Block 7		XCE0	Channel 112
			XCE1	Channel 113
			XCE2	Channel 114
			:	:
			XCE15	Channel 127

Controller Area Network (CAN)

This chapter contains a general description of the Controller Area Network (CAN) module. CAN is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. The CAN module supports bit-rates up to 1 Mbit/s and is compliant with the CAN 2.0B protocol specification.

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20.1 Overview

20.1.1 Features

CAN implements the following features:

- CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- Multiple clock sources
- 32 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM parity check mechanism
- Two interrupt lines
- Global power down and wakeup support

20.1.2 Functional Description

CAN performs CAN protocol communication according to ISO 11898-1 (identical to Bosch CAN protocol specification 2.0 A, B). The bit rate can be programmed to values up to 1 MBit/s. Additional transceiver hardware is required for the connection to the physical layer (CAN bus).

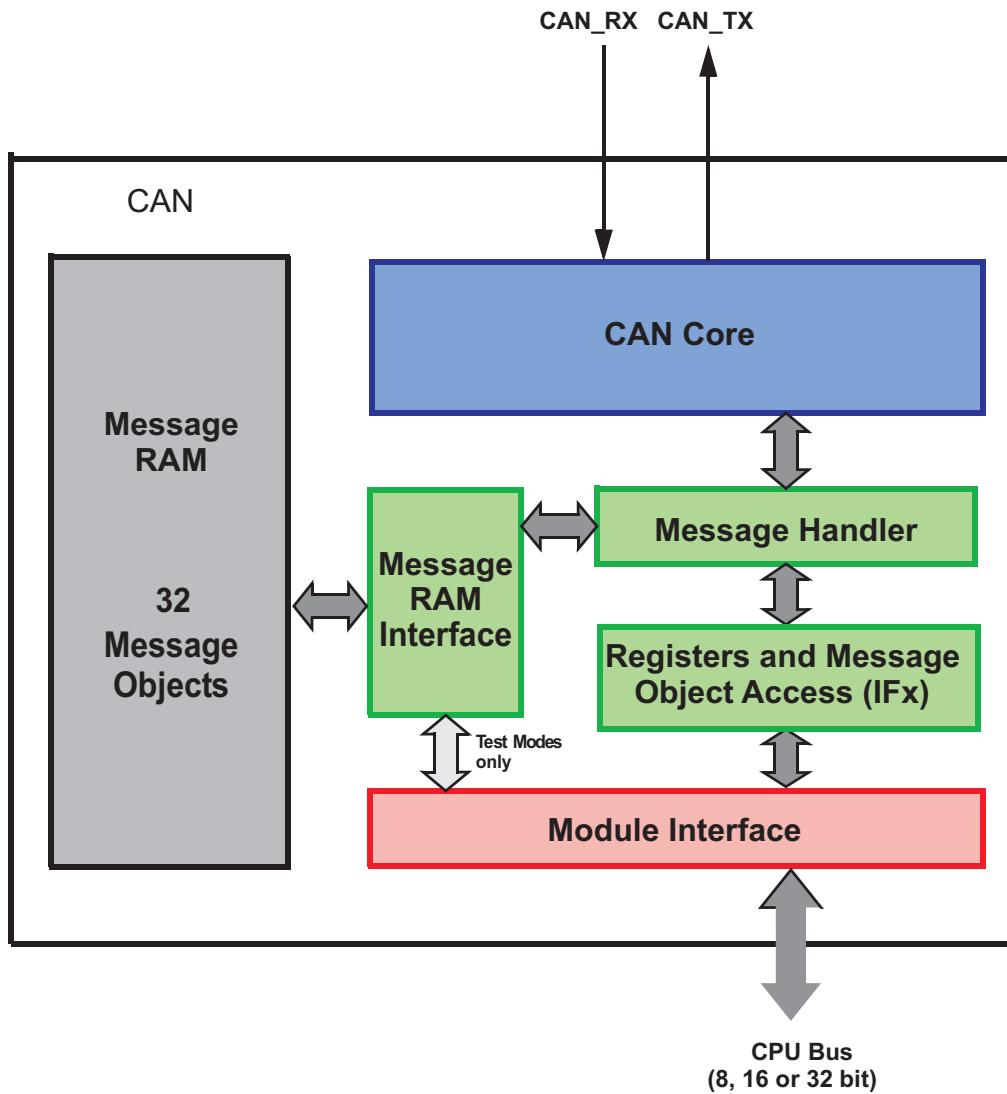
For communication on a CAN network, individual message objects can be configured. The message objects and identifier masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the message handler. Those functions are acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests.

The register set of the CAN can be accessed directly by the CPU via the module interface. These registers are used to control/configure the CAN Core and the message handler, and to access the message RAM.

20.1.3 Block Diagram

Figure 20-1. CAN Block Diagram



20.1.3.1 CAN Core

The CAN core consists of the CAN Protocol Controller and the Rx/Tx Shift register. It handles all ISO 11898-1 protocol functions.

20.1.3.2 Message Handler

The message handler is a state machine which controls the data transfer between the single ported Message RAM and the CAN Core's Rx/Tx Shift register. It also handles acceptance filtering and the interrupt request generation as programmed in the control registers.

20.1.3.3 Message RAM

The CAN message RAM enables the storage of 32 CAN messages.

20.1.3.4 Registers and Message Object Access (IFx)

Data consistency is ensured by indirect accesses to the message objects. During normal operation, all CPU accesses to the message RAM are done through Interface registers.

Three Interface Register sets control the CPU read and write accesses to the Message RAM. There are two Interface register sets for read/write access (IF1 and IF2) and one Interface Register set for read access only (IF3). See also [Section 20.13](#). The Interface registers have the same word-length as the message RAM.

In a dedicated test mode, the message RAM is memory mapped and can be directly accessed.

20.2 Operating Modes

20.2.1 Software Initialization

The software initialization mode is entered by setting the **Init** bit in the CAN Control register, either by software, by hardware reset or by going bus-off. While the Init bit is set, the message transfer from and to the CAN bus is stopped, and the status of the CAN_TX output is recessive (high). The CAN error counters are not updated. Setting the Init bit does not change any other configuration register.

To initialize the CAN Controller, the CPU has to set up the CAN Bit timing and those message objects which have to be used for CAN communication. Message objects which are not needed, can be deactivated by with their MsgVal bits cleared.

The access to the Bit Timing Register for the configuration of the Bit timing is enabled when both **Init** and CCE bits in the CAN Control Register are set.

Resetting the Init bit finishes the software initialization. Afterwards the Bit Stream Processor (BSP, for more details see [Section 20.12](#)) synchronizes itself to the data transfer on the CAN bus by waiting for the occurrence of a sequence of 11 consecutive recessive bits (= Bus Idle) before it can take part in bus activities and start the message transfer.

The initialization of the message objects is independent of the Init bit, however all message objects should be configured to particular identifiers or set to not valid before the message transfer is started.

It is possible to change the configuration of message objects during normal operation by the CPU. After setup and subsequent transfer of message object from interface registers to message RAM, the acceptance filtering will be applied to it, when the modified message object number is same or smaller than the previously found message object. This assures data consistency, even when changing message objects e.g. while a pending CAN frame reception.

20.2.2 CAN Message Transfer (Normal Operation)

Once the CAN is initialized and **Init** bit is reset to zero, the CAN Core synchronizes itself to the CAN bus and starts the message transfer.

Received messages are stored into their appropriate message objects if they pass acceptance filtering. The whole message (including all arbitration bits, DLC and up to eight data bytes) is stored into the message object. As a consequence, when e.g. the identifier mask is used, the arbitration bits which are masked to "don't care" may change in the message object when a received message is stored.

The CPU may read or write each message at any time via the Interface registers, as the message handler guarantees data consistency in case of concurrent accesses.

Messages to be transmitted can be updated by the CPU. If a permanent message object (arbitration and control bits set up during configuration and leaving unchanged for multiple CAN transfers) exists for the message, it is possible to only update the data bytes. If several transmit messages should be assigned to one message object, the whole message object has to be configured before the transmission of this message is requested.

The transmission of multiple message objects may be requested at the same time. They are subsequently transmitted, according to their internal priority. Messages may be updated or set to not valid at any time, even if a requested transmission is still pending. However, the data bytes will be discarded if a message is updated before a pending transmission has started.

Depending on the configuration of the message object, a transmission may be automatically requested by the reception of a remote frame with a matching identifier.

20.2.2.1 Disabled Automatic Retransmission

According to the CAN Specification (see ISO11898, 6.3.3 Recovery Management), the CAN provides a mechanism to automatically retransmit frames which have lost arbitration or have been disturbed by errors during transmission. The frame transmission service will not be confirmed to the user before the transmission is successfully completed.

By default, this automatic retransmission is enabled. It can be disabled by setting bit DAR in the CAN Control register. Further details to this mode are provided in [Section 20.11.3](#).

20.2.2.2 Auto-Bus-On

Per default, after the CAN has entered bus-off state, the CPU can start a bus-off-recovery sequence by resetting Init bit. If this is not done, the module will stay in bus-off state.

The CAN provides an automatic auto-bus-on feature which is enabled by bit ABO. If set, the CAN will automatically start the bus-off-recovery sequence. The sequence can be delayed by a user-defined number of clock cycles.

NOTE: If the CAN goes Bus-Off due to massive occurrence of CAN bus errors, it stops all bus activities and automatically sets the Init bit. Once the Init bit has been reset by the CPU or due to the auto-bus-on feature, the device will wait for 129 occurrences of Bus Idle (equal to $129 * 11$ consecutive recessive bits) before resuming normal operation. At the end of the bus-off recovery sequence, the error counters will be reset.

20.2.3 Test Modes

The CAN provides several test modes which are mainly intended for self test.

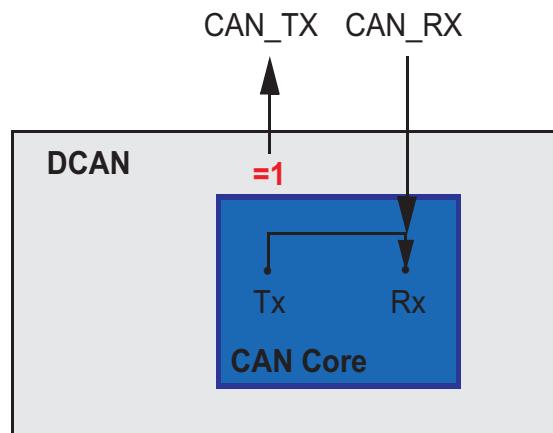
For all test modes, bit **Test** in the CAN Control register needs to be set to one. This enables write access to the Test register.

20.2.3.1 Silent Mode

The silent mode may be used to analyze the traffic on the CAN bus without affecting it by sending dominant bits (e.g., acknowledge bit, overload flag, active error flag). The CAN is still able to receive valid data frames and valid remote frames, but it will not send any dominant bits. However, these are internally routed to the CAN Core.

[Figure 20-2](#) shows the connection of signals CAN_TX and CAN_RX to the CAN core in silent mode. Silent mode can be activated by setting the **Silent** bit in test register to one. In ISO 11898-1, the silent mode is called the bus monitoring mode.

Figure 20-2. CAN Core in Silent Mode



20.2.3.2 Loopback Mode

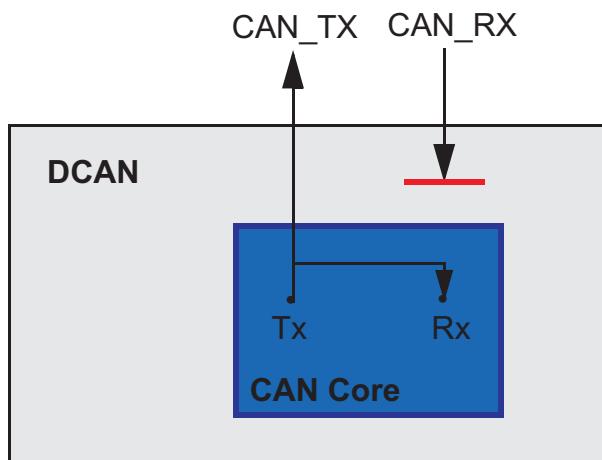
The loopback mode is mainly intended for hardware self-test functions. In this mode, the CAN core uses internal feedback from Tx output to Rx input. Transmitted messages are treated as received messages, and can be stored into message objects if they pass acceptance filtering. The actual value of the CAN_RX input pin is disregarded by the CAN core. Transmitted messages still can be monitored at the CAN_TX pin.

In order to be independent from external stimulation, the CAN core ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in loopback mode.

Figure 20-3 shows the connection of signals CAN_TX and CAN_RX to the CAN core in loopback mode. Loopback mode can be activated by setting bit **LBack** in the TTST register to one.

NOTE: In loopback mode, the signal path from CAN core to Tx pin, the Tx pin itself, and the signal path from Tx pin back to CAN Core are disregarded. For including these into the testing, see Section 20.2.3.3.

Figure 20-3. CAN Core in Loopback Mode

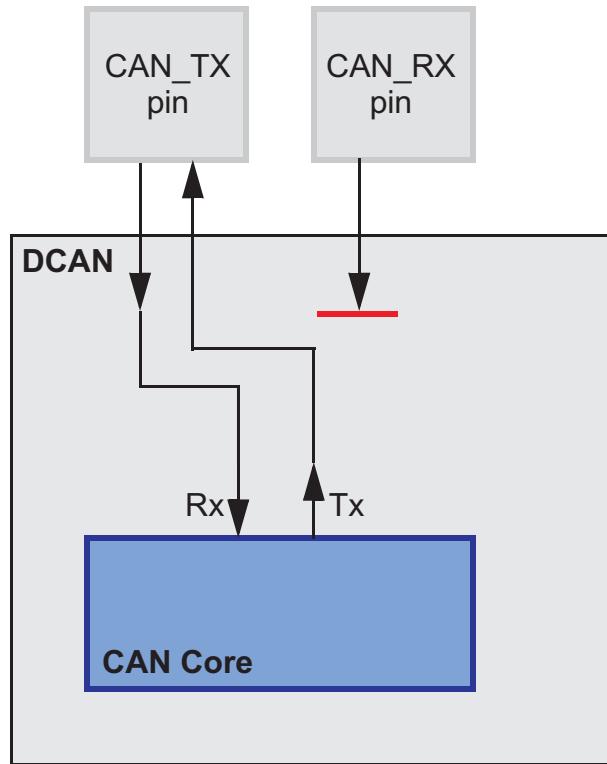


20.2.3.3 External Loopback Mode

The external loopback mode is similar to the loopback mode; however, it includes the signal path from CAN Core to Tx pin, the Tx pin itself, and the signal path from Tx pin back to CAN Core. When external loopback mode is selected, the input of the CAN core is connected to the input buffer of the Tx pin. With this configuration, the Tx pin IO circuit can be tested. External loopback mode can be activated by setting bit **ExL** in Test Register to one.

Figure 20-4 shows the connection of signals CAN_TX and CAN_RX to the CAN Core in external loopback mode.

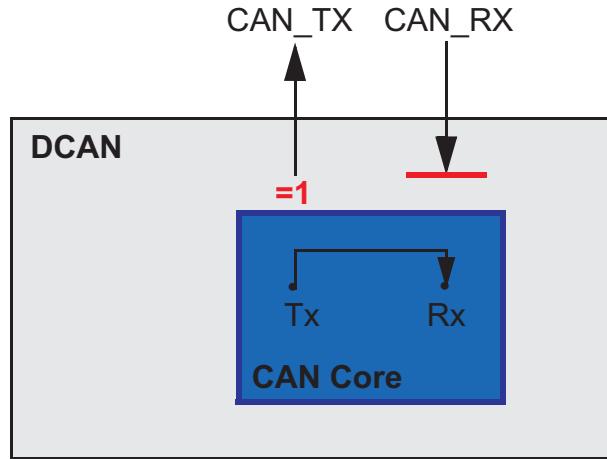
NOTE: When loopback mode is active (LBack bit set), the ExL bit will be ignored.

Figure 20-4. CAN Core in External Loopback Mode

20.2.3.4 Loopback Combined with Silent Mode

It is also possible to combine loopback mode and silent mode by setting bits LBack and Silent at the same time. This mode can be used for a "Hot Selftest," that is, the CAN hardware can be tested without affecting the CAN network. In this mode, the CAN_RX pin is disconnected from the CAN Core and no dominant bits will be sent on the CAN_TX pin.

[Figure 20-5](#) shows the connection of the signals CAN_TX and CAN_RX to the CAN Core in case of the combination of loopback mode with silent mode.

Figure 20-5. CAN Core in Loopback Combined with Silent Mode

20.3 Multiple Clock Source

Three clock domains are provided to the CAN module for generating the CAN bit timing: the external oscillator clock (X1/X2), the system clock, and the GPIO XCLKIN.

The system module reference guide and the device data manual provide for more information on how to configure the relevant clock source registers in the system module.

NOTE: The CAN core has to be programmed to at least eight clock cycles per bit time. To achieve a transfer rate of 1 MBaud an oscillator frequency of 8 MHz or higher has to be used.

20.4 Interrupt Functionality

Interrupts can be generated on two interrupt lines in the: CAN0INT line and CAN1INT line. These lines can be enabled by setting IE0 resp. IE1 bits in CAN Control register.

The CAN provides three groups of interrupt sources: message object interrupts, status change interrupts and error interrupts. The source of an interrupt can be determined by the interrupt identifiers Int0ID / Int1ID in the Interrupt register. When no interrupt is pending, the register will hold the value zero. Each interrupt line remains active until the dedicated field in the Interrupt register (Int0ID / Int1ID) again reach zero (this means the cause of the interrupt is reset), or until IE0 / IE1 are reset. The value 0x8000 in the Int0ID field indicates that an interrupt is pending because the CAN Core has updated (not necessarily changed) the Error and Status Register (Error Interrupt or Status Interrupt). This interrupt has the highest priority. The CPU can update (reset) the status bits WakeUpPnd, RxOk, TxOk and LEC by reading the Error and Status Register, but a write access of the CPU will never generate or reset an interrupt.

Values between 1 and the number of the last message object indicates that the source of the interrupt is one of the message objects, Int0ID resp. Int1ID will point to the pending message interrupt with the highest priority. The Message Object 1 has the highest priority, the last message object has the lowest priority.

An interrupt service routine which reads the message that is the source of the interrupt, may read the message and reset the message object's IntPnd at the same time (ClrlntPnd bit in the IF1/IF2 Command register). When IntPnd is cleared, the Interrupt register will point to the next message object with a pending interrupt.

The CAN module features a module-level interrupt enable and acknowledge mechanism. To enable the CAN0 and CAN1 interrupts, set the appropriate bits in the CAN_GLB_INT_EN register. When handling an interrupt, the individual message or status change flag must be cleared prior to acknowledging the interrupt via CAN_GLB_INT_CLR and PIEACK.

20.4.1 Message Object Interrupts

Message object interrupts are generated by events from the message objects. They are controlled by the flags IntPND, TxE and RxE which are described in [Section 20.14.1](#). Message object interrupts can be routed to either CAN0INT or CAN1INT line, controlled by the Interrupt Multiplexer register.

20.4.2 Status Change Interrupts

The events WakeUpPnd, RxOk, TxOk and LEC in Error and Status register belong to the status change interrupts. The status change interrupt group can be enabled by bit SIE in CAN Control Register. If SIE is set, a status change interrupt will be generated at each CAN frame, independent of bus errors or valid CAN communication, and also independent of the Message RAM configuration. Status Change interrupts can only be routed to interrupt line CAN0INT which has to be enabled by setting IE0 in the CAN Control Register.

NOTE: Reading the Error and Status register will clear the WakeUpPnd flag. If in global power down mode, the WakeUpPnd flag is cleared by such a read access before the CAN module has been waken up by the system, the CAN may re-assert the WakeUpPnd flag, and a second interrupt may occur. (see also [Section 20.5.2](#)).

20.4.3 Error Interrupts

The events PER, BOff and EWarn, belong to the error interrupts. The error interrupt group can be enabled by setting bit EIE. Also, error interrupts can only be routed to interrupt line CAN0INT which has to be enabled by setting IE0 in this register.

20.5 Global Power-down Mode

The Delfino™ architecture supports a centralized global power-down control over the peripheral modules through the sleep and deep sleep modes present in the system control peripheral.

20.5.1 Entering Global Power-down Mode

The global power down mode for the CAN is requested by configuring the appropriate bits in the sleep mode clock gating control(SCGC) or deep sleep mode clock gating Control(DCGC) register and enabled either of these modes (sleep or deep sleep).

The CAN then finishes all transmit requests of the message objects. When all requests are done, the CAN waits until a bus idle state is recognized. Then it will automatically set the Init bit to indicate that the global power-down mode has been entered.

20.5.2 Wakeup from Global Power-down Mode

If the CAN module is in global power-down mode, a CAN bus activity detection circuit is active. On occurrence of a dominant CAN bus level, the CAN will set the WakeUpPnd bit in Error and Status register.

If status interrupts are enabled, also an interrupt will be generated. This interrupt could be used by the application to wakeup the CAN. For this, the application needs to clear the Init bit in CAN Control register.

After the Init bit has been cleared, the CAN module waits until it detects 11 consecutive recessive bits on the CAN_RX pin and then goes bus-active again.

NOTE: The CAN transceiver circuit has to stay active during CAN bus activity detection. The first CAN message, which initiates the bus activity, cannot be received. This means that the first message received in power down mode is lost.

20.6 Local Power-down Mode

Besides from the centralized power-down mechanism controlled by the system control module, the CAN supports a local power-down mode which can be controlled within the DCAN control registers.

20.6.1 Entering Local Power-down Mode

The local power down mode is requested by setting the PDR bit in CAN Control register.

The CAN then finishes all transmit requests of the message objects. When all requests are done, CAN waits until a bus idle state is recognized. Then it will automatically set the Init bit in CAN Control register to prevent any further CAN transfers, and it will also set the PDA bit in CAN Error and Status register. With setting the PDA bits, the CAN module indicates that the local power down mode has been entered.

During local power down mode, the internal clocks of the CAN module are turned off, but there is a wake up logic which can be active, if enabled. Also the actual contents of the control registers can be read back.

20.6.2 Wakeup from Local Power-down Mode

There are two ways to wake up the CAN from local power down mode:

1. The application could wake up the CAN module manually by clearing the PDR bit and then clearing the Init bit in CAN Control register
2. A CAN bus activity detection circuit can be activated by setting the wake up on bus activity bit (WUBA) in CAN Control register.

If this circuit is active, on occurrence of a dominant CAN bus level, the CAN will automatically start the

wake up sequence. It will clear the PDR bit in CAN Control register and also clear the PDA bit in Error and Status register. The WakeUpPnd bit in CAN Error and Status register will be set. If Status Interrupts are enabled, also an interrupt will be generated. Finally the Init bit in CAN control register will be cleared.

After the Init bit has been cleared, the module waits until it detects 11 consecutive recessive bits on the CAN_RX pin and then goes bus-active again.

NOTE: In local low power mode, the application should not clear the Init bit while PDR is set. If there are any messages in the Message RAM configured as to be transmitted and the application resets the init bit, these messages may be sent. In local low power mode, the application should not clear the Init bit while PDR is set. If there are any messages in the Message RAM configured as to be transmitted and the application resets the init bit, these messages may be sent.

20.7 Parity Check Mechanism

The CAN provides a parity check mechanism to ensure data integrity of message RAM data. For each word (32 bits) in Message RAM, one parity bit will be calculated.

Parity information is stored in the Message RAM on write accesses and will be checked against the stored parity bit from Message RAM on read accesses.

The parity check functionality can be enabled or disabled by PMD bit field in CAN Control register. In case of disabled parity check, the parity bits in message RAM will be left unchanged on write access to data area and no check will be done on read access.

If parity checking is enabled, parity bits will be automatically generated and checked by the CAN. A parity bit will be set, if the modulo-2-sum of the data bits is 1. This definition is equivalent to: The parity bit will be set, if the number of 1 bits in the data is odd.

20.7.1 Behavior on Parity Error

On any read access to Message RAM, for example, during the start of a CAN frame transmission, the parity of the message object will be checked. If a parity error is detected, the PER bit in Error and Status register will be set. If error interrupts are enabled, an interrupt would also be generated. In order to avoid the transmission of invalid data over the CAN bus, the MsgVal bit of the message object will be reset.

The message object data can be read by the CPU, independently of parity errors. Thus, the application has to ensure that the read data is valid, e.g., by immediately checking the Parity Error Code register on parity error interrupt.

20.8 Debug Mode

The module supports the usage of an external debug unit by providing functions like pausing CAN activities and making message RAM content accessible from the debugger. Debug mode is entered automatically when an external debugger is connected and the core is halted.

Before entering Debug mode, the circuit will either wait until a started transmission or reception will be finished and Bus idle state is recognized, or immediately interrupt a current transmission or reception. This is depending on bit IDS. Afterwards, the CAN enters Debug mode, indicated by the InitDbg flag, in the CAN Control register. During debug mode, all CAN registers can be accessed. Reading reserved bits will return '0'. Writing to reserved bits will have no effect. Also, the message RAM will be memory mapped. This allows the external debug unit to read the message RAM. For the memory organization, see [Section 20.14.3](#)).

NOTE: During debug mode, the Message RAM cannot be accessed via the IFx register sets.

NOTE: Writing to control registers in Debug mode may influence the CAN state machine and further message handling.

For debug support, the auto clear functionality of the following CAN registers is disabled:

- Error and Status register (clear of status flags by read)
- IF1/IF2 Command registers (clear of DMAActive flag by r/w)

20.9 Module Initialization

After hardware reset, the Init bit in the CAN Control register is set and all CAN protocol functions are disabled. The configuration of the bit timing and of the message objects should be completed before the CAN protocol functions are enabled.

For the configuration of the message objects, see [Section 20.10](#).

For the configuration of the Bit Timing, see [Section 20.12.2](#).

The bits MsgVal, NewDat, IntPnd, and TxRqst of the message objects are reset to '0' by a hardware reset. The configuration of a message object is done by programming Mask, Arbitration, Control and Data bits of one of the IF1/IF2 Interface register sets to the desired values. By writing the message object number to bits [7:0] of the corresponding IF1/IF2 Command register, the IF1/IF2 Interface Register content is loaded into the addressed message object in the Message RAM.

The configuration of the bit timing requires that the CCE bit in the CAN Control register is set additionally to Init. This is not required for the configuration of the message objects.

When the Init bit in the CAN Control register is cleared, the CAN Protocol Controller state machine of the CAN Core and the message handler State Machine start to control the CAN's internal data flow. Received messages which pass the acceptance filtering are stored into the Message RAM; messages with pending transmission request are loaded into the CAN Core's Shift register and are transmitted via the CAN bus.

The CPU may enable the interrupt lines (setting IE0 and IE1 to '1') at the same time when it clears Init and CCE. The status interrupts EIE and SIE may be enabled simultaneously.

The CAN communication may be controlled interrupt-driven or in polling mode. The Interrupt Register points to those message objects with IntPnd = '1'. It is updated even if the interrupt lines to the CPU are disabled (IE0 / IE1 are zero).

The CPU may poll all MessageObject's NewDat and TxRqst bits in parallel from the NewData registers and the Transmission Request registers. Polling can be made easier if all Transmit Objects are grouped at the low numbers, all Receive Objects are grouped at the high numbers.

20.10 Configuration of Message Objects

The whole Message RAM should to be configured before the end of the initialization; however, it is also possible to change the configuration of message objects during CAN communication.

20.10.1 Configuration of a Transmit Object for Data Frames

[Figure 20-6](#) shows how a transmit object can be initialized.

Figure 20-6. Initialization of a Transmit Object

MsgVal	Arb	Data	Mask	EoB	Dir	NewDat	MsgLst	RxIE	TxIE	IntPnd	RmtEn	TxRqst
1	appl.	appl.	appl.	1	1	0	0	0	appl.	0	appl.	0

- The arbitration bits (ID[28:0] and Xtd bit) are given by the application. They define the identifier and type of the outgoing message. If an 11-bit Identifier (standard frame) is used (Xtd = '0'), it is programmed to ID[28:18]. In this case, ID[17:0] can be ignored.
- The data registers (DLC[3:0] and Data0-7) are given by the application, TxRqst and RmtEn should not be set before the data is valid.
- If the TxIE bit is set, the IntPnd bit will be set after a successful transmission of the message object.
- If the RmtEn bit is set, a matching received remote frame will cause the TxRqst bit to be set; the remote frame will autonomously be answered by a data frame.
- The Mask bits (Msk[28:0], UMask, MXtd, and MDir bits) may be used (UMask='1') to allow groups of remote frames with similar identifiers to set the TxRqst bit. The Dir bit should not be masked. For

details see [Section 20.11.8](#). Identifier masking must be disabled (UMask = '0') if no remote frames are allowed to set the TxRqst bit (RmtEn = '0').

20.10.2 Configuration of a Transmit Object for Remote Frames

It is not necessary to configure transmit objects for the transmission of remote frames. Setting TxRqst for a receive object will cause the transmission of a remote frame with the same identifier as the data frame for which this receive object is configured.

20.10.3 Configuration of a Single Receive Object for Data Frames

Figure 15-7 shows how a receive object for data frames can be initialized.

Figure 20-7. Initialization of a single Receive Object for Data Frames

MsgVal	Arb	Data	Mask	EoB	Dir	NewDat	MsgLst	RxIE	TxIE	IntPnd	RmtEn	TxRqst
1	appl.	appl.	appl.	1	0	0	0	appl.	0	0	0	0

- The arbitration bits (ID[28:0] and Xtd bit) are given by the application. They define the identifier and type of accepted received messages. If an 11-bit Identifier (Standard Frame) is used (Xtd = '0'), it is programmed to ID[28:18]. In this case, ID[17:0] can be ignored. When a data frame with an 11-bit Identifier is received, ID[17:0] will be set to '0'.
- The data length code (DLC[3:0]) is given by the application. When the message handler stores a data frame in the message object, it will store the received data length code and eight data bytes. If the data length code is less than 8, the remaining bytes of the message object may be overwritten by non specified values.
- The mask bits (Msk[28:0], UMask, MXtd, and MDir bits) may be used (UMask = '1') to allow groups of data frames with similar identifiers to be accepted. The Dir bit should not be masked in typical applications. If some bits of the Mask bits are set to "don't care", the corresponding bits of the Arbitration Register will be overwritten by the bits of the stored data frame.
- If the RxIE bit is set, the IntPnd bit will be set when a received data frame is accepted and stored in the message object.
- If the TxRqst bit is set, the transmission of a remote frame with the same identifier as actually stored in the Arbitration bits will be triggered. The content of the Arbitration bits may change if the Mask bits are used (UMask = '1') for acceptance filtering.

20.10.4 Configuration of a Single Receive Object for Remote Frames

Figure 20-8 shows how a receive object for remote frames can be initialized.

Figure 20-8. Initialization of a single Receive Object for Remote Frames

MsgVal	Arb	Data	Mask	EoB	Dir	NewDat	MsgLst	RxIE	TxIE	IntPnd	RmtEn	TxRqst
1	appl.	appl.	appl.	1	1	0	0	appl.	0	0	0	0

- Receive objects for remote frames may be used to monitor remote frames on the CAN bus. The remote frame stored in the receive object will not trigger the transmission of a data frame. Receive objects for remote frames may be expanded to a FIFO buffer, see [Section 20.10.5](#).
- UMask must be set to '1'. The Mask bits (Msk[28:0], UMask, MXtd, and MDir bits) may be set to "must-match" or to "don't care", to allow groups of remote frames with similar identifiers to be accepted. The Dir bit should not be masked in typical applications. For details see [Section 20.11.8](#).
- The arbitration bits (ID[28:0] and Xtd bit) may be given by the application. They define the identifier and type of accepted received remote frames. If some bits of the Mask bits are set to "don't care", the corresponding bits of the arbitration bits will be overwritten by the bits of the stored remote frame. If an 11-bit Identifier (standard frame) is used (Xtd = '0'), it is programmed to ID[28:18]. In this case, ID[17:0] can be ignored. When a remote frame with an 11-bit Identifier is received, ID[17:0] will be set to '0'.
- The data length code (DLC[3:0]) may be given by the application. When the message handler stores a remote frame in the message object, it will store the received data length code. The data bytes of the message object will remain unchanged.
- If the RxIE bit is set, the IntPnd bit will be set when a received remote frame is accepted and stored in

the message object.

20.10.5 Configuration of a FIFO Buffer

With the exception of the EoB bit, the configuration of receive objects belonging to a FIFO buffer is the same as the configuration of a single receive object.

To concatenate multiple message objects to a FIFO buffer, the identifiers and masks (if used) of these message objects have to be programmed to matching values. Due to the implicit priority of the message objects, the message object with the lowest number will be the first message object of the FIFO buffer. The EoB bit of all message objects of a FIFO buffer except the last one have to be programmed to zero. The EoB bits of the last message object of a FIFO buffer is set to one, configuring it as the end of the block.

20.11 Message Handling

When initialization is finished, the CAN module synchronizes itself to the traffic on the CAN bus. It does acceptance filtering on received messages and stores those frames that are accepted into the designated message objects. The application has to update the data of the messages to be transmitted and to enable and request their transmission. The transmission is requested automatically when a matching remote frame is received.

The application may read messages which are received and accepted. Messages that are not read before the next messages is accepted for the same message object will be overwritten. Messages may be read interrupt-driven or after polling of NewDat.

20.11.1 Message Handler Overview

The message handler state machine controls the data transfer between the Rx/Tx Shift Register of the CAN Core and the Message RAM. It performs the following tasks:

- Data transfer from Message RAM to CAN Core (messages to be transmitted).
- Data transfer from CAN Core to the Message RAM (received messages).
- Data transfer from CAN Core to the Acceptance Filtering unit.
- Scanning of Message RAM for a matching message object (acceptance filtering).
- Scanning the same message object after being changed by IF1/IF2 registers when priority is same or higher as message the object found by last scanning.
- Handling of TxRqst flags.
- Handling of interrupt flags.

The message handler registers contains status flags of all message objects grouped into the following topics:

- Transmission request flags
- New data flags
- Interrupt pending flags
- Message valid registers

Instead of collecting above listed status information of each message object via IFx registers separately, these message handler registers provides a fast and easy way to get an overview e.g. about all pending transmission requests.

All message handler registers are read-only.

20.11.2 Receive/Transmit Priority

The receive/transmit priority for the message objects is attached to the message number, not to the CAN identifier. Message object 1 has the highest priority, while message object 32 has the lowest priority. If more than one transmission request is pending, they are serviced due to the priority of the corresponding message object, so e.g., messages with the highest priority can be placed in the message objects with the lowest numbers.

The acceptance filtering for received data frames or remote frames is also done in ascending order of message objects, so a frame that has been accepted by a message object cannot be accepted by another message object with a higher message number. The last message object may be configured to accept any data frame or remote frame that was not accepted by any other message object, for nodes that need to log the complete message traffic on the CAN bus.

20.11.3 Transmission of Messages in Event Driven CAN Communication

If the shift register of the CAN Core is ready for loading and if there is no data transfer between the IFx registers and Message RAM, the MsgVal bits in the Message Valid register and the TxRqst bits in the transmission request register are evaluated. The valid message object with the highest priority pending transmission request is loaded into the shift register by the message handler and the transmission is started. The message object's NewDat bit is reset.

After a successful transmission and if no new data was written to the message object (NewDat = '0') since the start of the transmission, the TxRqst bit will be reset. If TxIE is set, IntPnd will be set after a successful transmission. If the CAN has lost the arbitration or if an error occurred during the transmission, the message will be retransmitted as soon as the CAN bus is free again. If meanwhile the transmission of a message with higher priority has been requested, the messages will be transmitted in the order of their priority.

If automatic retransmission mode is disabled by setting the DAR bit in the CAN Control register, the behavior of bits TxRqst and NewDat in the Message Control register of the Interface register set is as follows:

- When a transmission starts, the TxRqst bit of the respective Interface register set is reset, while bit NewDat remains set.
- When the transmission has been successfully completed, the NewDat bit is reset.

When a transmission failed (lost arbitration or error) bit NewDat remains set. To restart the transmission, the application has to set TxRqst again.

Received remote frames do not require a receive object. They will automatically trigger the transmission of a data frame, if in the matching Transmit Object the RmtEn bit is set.

20.11.4 Updating a Transmit Object

The CPU may update the data bytes of a transmit object any time via the IF1/IF2 interface registers, neither MsgVal nor TxRqst have to be reset before the update.

Even if only a part of the data bytes are to be updated, all four bytes in the corresponding IF1/IF2 Data A register or IF1/IF2 Data B register have to be valid before the content of that register is transferred to the message object. Either the CPU has to write all four bytes into the IF1/IF2 Data register or the message object is transferred to the IF1/IF2 Data Register before the CPU writes the new data bytes.

When only the data bytes are updated, first 0x87 can be written to bits [23:16] of the Command register and then the number of the message object is written to bits [7:0] of the Command register, concurrently updating the data bytes and setting TxRqst with NewDat.

To prevent the reset of TxRqst at the end of a transmission that may already be in progress while the data is updated, NewDat has to be set together with TxRqst in event driven CAN communication. For details see [Section 20.11.3](#).

When NewDat is set together with TxRqst, NewDat will be reset as soon as the new transmission has started.

20.11.5 Changing a Transmit Object

If the number of implemented message objects is not sufficient to be used as permanent message objects only, the transmit objects may be managed dynamically. The CPU can write the whole message (Arbitration,

Control, and Data) into the Interface register. The bits [23:16] of the Command register can be set to 0xB7 for the transfer of the whole message object content into the message object. Neither MsgVal nor TxRqst have to be reset before this operation.

If a previously requested transmission of this message object is not completed but already in progress, it will be continued; however it will not be repeated if it is disturbed.

To only update the data bytes of a message to be transmitted, bits [23:16] of the Command register should be set to 0x87.

NOTE: After the update of the transmit object, the interface register set will contain a copy of the actual contents of the object, including the part that had not been updated.

20.11.6 Acceptance Filtering of Received Messages

When the arbitration and control bits (Identifier + IDE + RTR + DLC) of an incoming message is completely shifted into the shift register of the CAN Core, the message handler starts to scan of the message RAM for a matching valid message object:

- The acceptance filtering unit is loaded with the arbitration bits from the CAN Core shift register.
- Then the arbitration and mask bits (including MsgVal, UMask, NewDat, and EoB) of Message Object 1 are loaded into the Acceptance Filtering unit and are compared with the arbitration bits from the shift register. This is repeated for all following message objects until a matching message object is found, or until the end of the Message RAM is reached.
- If a match occurs, the scanning is stopped and the message handler proceeds depending on the type of the frame (data frame or remote frame) received.

20.11.7 Reception of Data Frames

The message handler stores the message from the CAN Core shift register into the respective message object in the Message RAM. Not only the data bytes, but all arbitration bits and the data length code are stored into the corresponding message object. This ensures that the data bytes stay associated to the identifier even if arbitration mask registers are used.

The NewDat bit is set to indicate that new data (not yet seen by the CPU) has been received. The CPU should reset the NewDat bit when it reads the message object. If at the time of the reception the NewDat bit was already set, MsgLst is set to indicate that the previous data (supposedly not seen by the CPU) is lost. If the RxIE bit is set, the IntPnd bit is set, causing the Interrupt Register to point to this message object.

The TxRqst bit of this message object is reset to prevent the transmission of a remote frame, while the requested data frame has just been received.

20.11.8 Reception of Remote Frames

When a remote frame is received, three different configurations of the matching message object have to be considered:

1. Dir = '1' (direction = transmit), RmtEn = '1', UMask = '1' or '0'
The TxRqst bit of this message object is set at the reception of a matching remote frame. The rest of the message object remains unchanged.
2. Dir = '1' (direction = transmit), RmtEn = '0', UMask = '0'
The remote frame is ignored, this message object remains unchanged.
3. Dir = '1' (direction = transmit), RmtEn = '0', UMask = '1'
The remote frame is treated similar to a received data frame. At the reception of a matching remote frame, the TxRqst bit of this message object is reset. The arbitration and control bits (Identifier + IDE + RTR + DLC) from the shift register are stored in the message object in the Message RAM and the NewDat bit of this message object is set. The data bytes of the message object remain unchanged

20.11.9 Reading Received Messages

The CPU may read a received message any time via the IFx interface registers, the data consistency is guaranteed by the message handler state machine.

Typically the CPU will write first 0x7F to bits [23:16] and then the number of the message object to bits [7:0] of the Command Register. That combination will transfer the whole received message from the Message RAM into the Interface Register set. Additionally, the bits NewDat and IntPnd are cleared in the Message RAM (not in the Interface Register set). The values of these bits in the Message Control Register always reflect the status before resetting the bits.

If the message object uses masks for acceptance filtering, the arbitration bits show which of the different matching messages has been received.

The actual value of NewDat shows whether a new message has been received since last time when this message object was read. The actual value of MsgLst shows whether more than one message have been received since the last time when this message object was read. MsgLst will not be automatically reset.

20.11.10 Requesting New Data for a Receive Object

By means of a remote frame, the CPU may request another CAN node to provide new data for a receive object. Setting the TxRqst bit of a receive object will cause the transmission of a remote frame with the receive object's identifier. This remote frame triggers the other CAN node to start the transmission of the matching data frame. If the matching data frame is received before the remote frame could be transmitted, the TxRqst bit is automatically reset.

Setting the TxRqst bit without changing the contents of a message object requires the value 0x84 in bits [23:16] of the Command Register.

20.11.11 Storing Received Messages in FIFO Buffers

Several message objects may be grouped to form one or more FIFO Buffers. Each FIFO Buffer configured to store received messages with a particular (group of) Identifier(s). Arbitration and Mask registers of the FIFO Buffer's message objects are identical. The EoB (End of Buffer) bits of all but the last of the FIFO Buffer's message objects are '0', in the last one the EoB bit is '1'.

Received messages with identifiers matching to a FIFO Buffer are stored into a message object of this FIFO Buffer, starting with the message object with the lowest message number.

When a message is stored into a message object of a FIFO Buffer the NewDat bit of this message object is set. By setting NewDat while EoB is '0' the message object is locked for further write accesses by the message handler until the CPU has cleared the NewDat bit.

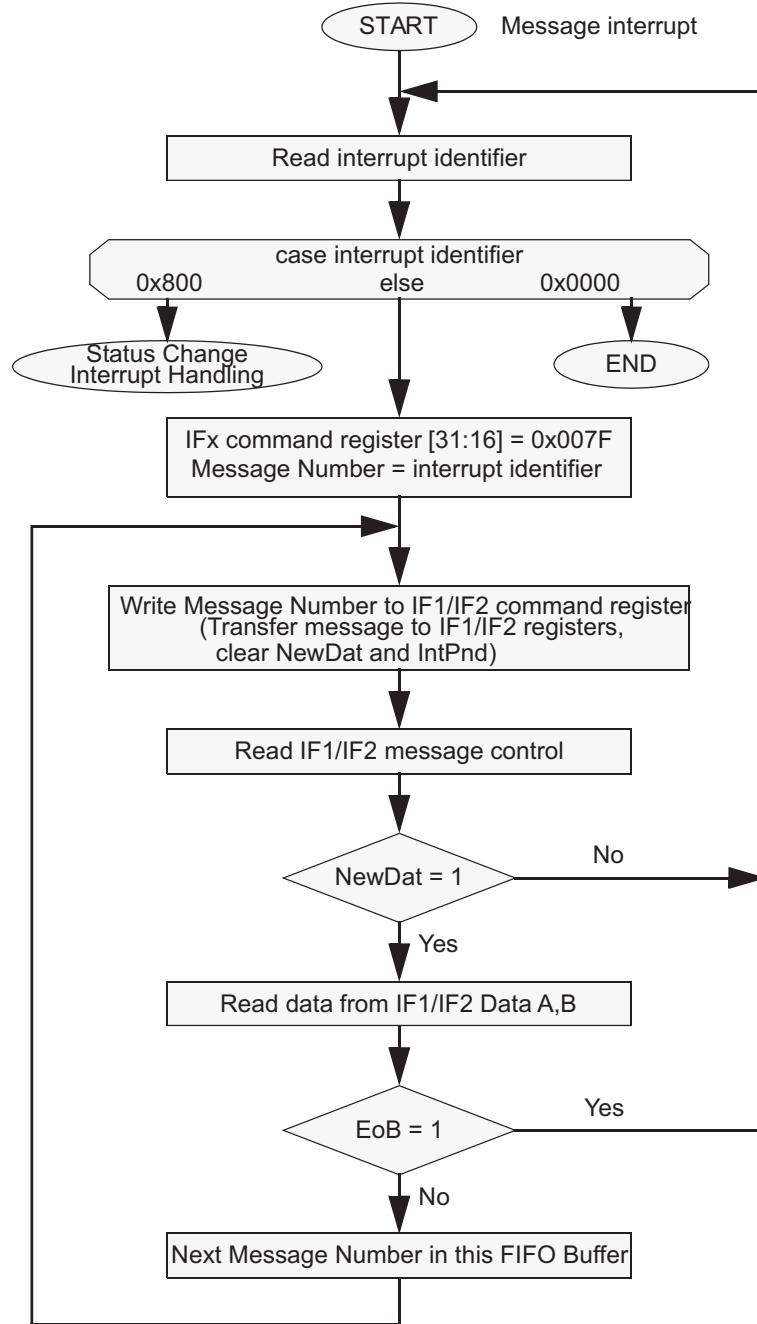
Messages are stored into a FIFO Buffer until the last message object of this FIFO Buffer is reached. If none of the preceding message objects is released by writing NewDat to '0', all further messages for this FIFO Buffer will be written into the last message object of the FIFO Buffer (EoB = '1') and therefore overwrite previous messages in this message object.

20.11.12 Reading from a FIFO Buffer

Several messages may be accumulated in a set of message objects which are concatenated to form a FIFO Buffer before the application program is required (in order to avoid the loss of data) to empty the buffer. A FIFO Buffer of length N will store N-1 plus the last received message since last time it was cleared. A FIFO Buffer is cleared by reading and resetting the NewDat bits of all its message objects, starting at the FIFO Object with the lowest message number. This should be done in a subroutine following the example shown in [Figure 20-9](#).

NOTE: All message objects of a FIFO buffer needs to be read and cleared before the next batch of messages can be stored. Otherwise true FIFO functionality can not be guaranteed, since the message objects of a partly read buffer will be re-filled according to the normal (descending) priority.

Reading from a FIFO Buffer message object and resetting its NewDat bit is handled the same way as reading from a single message object.

Figure 20-9. CPU Handling of a FIFO Buffer (Interrupt Driven)

20.12 CAN Bit Timing

The CAN supports bit rates between less than 1 kBit/s and 1000 kBit/s.

Each member of the CAN network has its own clock generator, typically derived from a crystal oscillator. The Bit timing parameters can be configured individually for each CAN node, creating a common Bit rate even though the CAN nodes' oscillator periods (f_{osc}) may be different.

The frequencies of these oscillators are not absolutely stable. Small variations are caused by changes in temperature or voltage and by deteriorating components. As long as the variations remain inside a specific oscillator tolerance range (Δf), the CAN nodes are able to compensate for the different bit rates by resynchronizing to the bit stream.

In many cases, the CAN bit synchronization will amend a faulty configuration of the CAN bit timing to such a degree that only occasionally an error frame is generated. In the case of arbitration however, when two or more CAN nodes simultaneously try to transmit a frame, a misplaced sample point may cause one of the transmitters to become error passive.

The analysis of such sporadic errors requires a detailed knowledge of the CAN bit synchronization inside a CAN node and of the CAN nodes' interaction on the CAN bus.

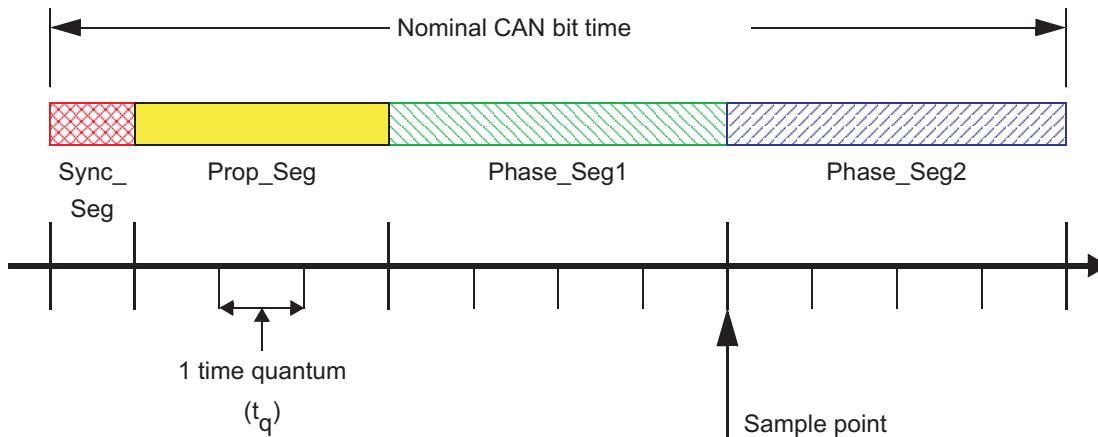
Even if minor errors in the configuration of the CAN bit timing do not result in immediate failure, the performance of a CAN network can be reduced significantly.

20.12.1 Bit Time and Bit Rate

According to the CAN specification, the Bit time is divided into four segments (see [Figure 20-10](#)[Figure 15-10](#)):

- Synchronization Segment (Sync_Seg)
- Propagation Time Segment (Prop_Seg)
- Phase Buffer Segment 1 (Phase_Seg1)
- Phase Buffer Segment 2 (Phase_Seg2)

Figure 20-10. Bit Timing



Each segment consists of a specific number of time quanta. The length of one time quantum (t_q), which is the basic time unit of the bit time, is given by the CAN_CLK and the Baud Rate Prescalers (BRPE and BRP). With these two Baud Rate Prescalers combined, divider values from 1 to 1024 can be programmed:

$$t_q = \text{Baud Rate Prescaler} / \text{CAN_CLK}$$

Apart from the fixed length of the synchronization segment, these numbers are programmable. [Table 20-1](#) describes the minimum programmable ranges required by the CAN protocol.

A given bit rate may be met by different bit time configurations.

Table 20-1. Programmable Ranges Required by CAN Protocol

Parameter	Range	Remark
Sync_Seg	$1 t_q$ (fixed)	Synchronization of bus input to CAN_CLK
Prop_Seg	$[1 \dots 8] t_q$	Compensates for the physical delay times
Phase_Seg1	$[1 \dots 8] t_q$	May be lengthened temporarily by synchronization
Phase_Seg2	$[1 \dots 8] t_q$	May be shortened temporarily by synchronization
Synchronization Jump Width (SJW)	$[1 \dots 4] t_q$	May not be longer than either Phase Buffer Segment

NOTE: For proper functionality of the CAN network, the physical delay times and the oscillator's tolerance range have to be considered.

20.12.1.1 Synchronization Segment

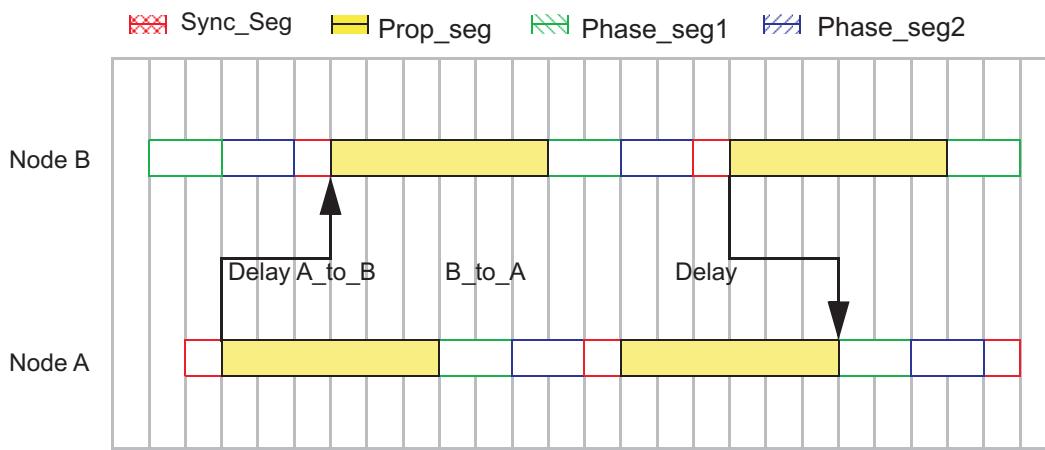
The Synchronization Segment (Sync_Seg) is the part of the bit time where edges of the CAN bus level are expected to occur. If an edge occurs outside of Sync_Seg, its distance to the Sync_Seg is called the phase error of this edge.

20.12.1.2 Propagation Time Segment

This part of the bit time is used to compensate physical delay times within the CAN network. These delay times consist of the signal propagation time on the bus and the internal delay time of the CAN nodes.

Any CAN node synchronized to the bit stream on the CAN bus can be out of phase with the transmitter of the bit stream, caused by the signal propagation time between the two nodes. The CAN protocol's nondestructive bitwise arbitration and the dominant acknowledge bit provided by receivers of CAN messages require that a CAN node transmitting a bit stream must also be able to receive dominant bits transmitted by other CAN nodes that are synchronized to that bit stream. The example in [Figure 20-11](#) shows the phase shift and propagation times between two CAN nodes.

Figure 20-11. The Propagation Time Segment



$$\text{Delay A_to_B} \geq \text{node output delay(A)} + \text{bus line delay(A}\setminus\text{B)} + \text{node input delay(B)}$$

$$\text{Prop_Seg} \geq \text{Delay A_to_B} + \text{Delay B_to_A}$$

$$\text{Prop_Seg} \geq 2 \cdot [\max(\text{node output delay} + \text{bus line delay} + \text{node input delay})]$$

In this example, both nodes A and B are transmitters performing an arbitration for the CAN bus. The node A has sent its Start of Frame bit less than one bit time earlier than node B, therefore node B has synchronized itself to the received edge from recessive to dominant. Since node B has received this edge delay(A_to_B) after it has been transmitted, node B's bit timing segments are shifted with regard to node A. Node B sends an identifier with higher priority and so it will win the arbitration at a specific identifier bit when it transmits a dominant bit while node A transmits a recessive bit. The dominant bit transmitted by node B will arrive at node A after the delay(B_to_A).

Due to oscillator tolerances, the actual position of node A's Sample Point can be anywhere inside the nominal range of node A's Phase Buffer Segments, so the bit transmitted by node B must arrive at node A before the start of Phase_Seg1. This condition defines the length of Prop_Seg.

If the edge from recessive to dominant transmitted by node B would arrive at node A after the start of Phase_Seg1, it could happen that node A samples a recessive bit instead of a dominant bit, resulting in a bit error and the destruction of the current frame by an error flag.

This error only occurs when two nodes arbitrate for the CAN bus which have oscillators of opposite ends of the tolerance range and are separated by a long bus line; this is an example of a minor error in the Bit timing configuration (Prop_Seg too short) that causes sporadic bus errors.

Some CAN implementations provide an optional 3 Sample Mode. The CAN does not. In this mode, the CAN bus input signal passes a digital low-pass filter, using three samples and a majority logic to determine the valid bit value. This results in an additional input delay of $1 t_q$, requiring a longer Prop_Seg.

20.12.1.3 Phase Buffer Segments and Synchronization

The phase buffer segments (Phase_Seg1 and Phase_Seg2) and the synchronization jump width (SJW) are used to compensate for the oscillator tolerance.

The phase buffer segments surround the sample point. The phase buffer segments may be lengthened or shortened by synchronization.

The synchronization jump width (SJW) defines how far the resynchronizing mechanism may move the sample point inside the limits defined by the phase buffer segments to compensate for edge phase errors.

Synchronizations occur on edges from recessive to dominant. Their purpose is to control the distance between edges and sample points.

Edges are detected by sampling the actual bus level in each time quantum and comparing it with the bus level at the previous sample point. A synchronization may be done only if a recessive bit was sampled at the previous sample point and if the actual time quantum's bus level is dominant.

An edge is synchronous if it occurs inside of Sync_Seg, otherwise its distance to the Sync_Seg is the edge phase error, measured in time quanta. If the edge occurs before Sync_Seg, the phase error is negative, else it is positive.

Two types of synchronization exist: hard synchronization and resynchronizing. A hard synchronization is done once at the start of a frame; inside a frame only resynchronization is possible.

- Hard Synchronization

After a hard synchronization, the bit time is restarted with the end of Sync_Seg, regardless of the edge phase error. Thus hard synchronization forces the edge which has caused the hard synchronization to lie within the synchronization segment of the restarted bit time.

- Bit Resynchronizations

Resynchronization leads to a shortening or lengthening of the bit time such that the position of the sample point is shifted with regard to the edge.

When the phase error of the edge which causes resynchronization is positive, Phase_Seg1 is lengthened. If the magnitude of the phase error is less than SJW, Phase_Seg1 is lengthened by the magnitude of the phase error, else it is lengthened by SJW.

When the phase error of the edge which causes Resynchronization is negative, Phase_Seg2 is shortened. If the magnitude of the phase error is less than SJW, Phase_Seg2 is shortened by the magnitude of the phase error, else it is shortened by SJW.

If the magnitude of the phase error of the edge is less than or equal to the programmed value of SJW, the results of hard synchronization and resynchronization are the same. If the magnitude of the phase error is larger than SJW, the resynchronization cannot compensate the phase error completely, and an error of (phase error - SJW) remains.

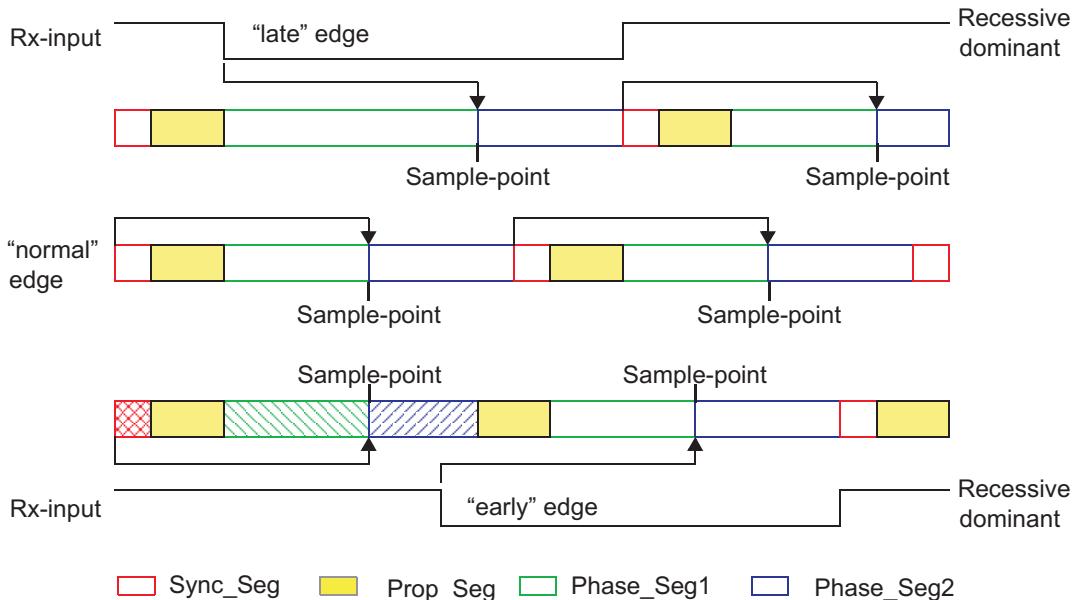
Only one synchronization may be done between two sample points. The synchronizations maintain a minimum distance between edges and sample points, giving the bus level time to stabilize and filtering out spikes that are shorter than (Prop_Seg + Phase_Seg1).

Apart from noise spikes, most synchronizations are caused by arbitration. All nodes synchronize "hard" on the edge transmitted by the "leading" transceiver that started transmitting first, but due to propagation delay times, they cannot become ideally synchronized. The "leading" transmitter does not necessarily win the arbitration, therefore the receivers have to synchronize themselves to different transmitters that subsequently "take the lead" and that are differently synchronized to the previously "leading" transmitter. The same happens at the acknowledge field, where the transmitter and some of the receivers will have to synchronize to that receiver that "takes the lead" in the transmission of the dominant acknowledge bit.

Synchronizations after the end of the arbitration will be caused by oscillator tolerance, when the differences in the oscillator's clock periods of transmitter and receivers sum up during the time between synchronizations (at most ten bits). These summarized differences may not be longer than the SJW, limiting the oscillator's tolerance range.

The examples in [Figure 20-12](#) show how the phase buffer segments are used to compensate for phase errors. There are three drawings of each two consecutive bit timings. The upper drawing shows the synchronization on a "late" edge, the lower drawing shows the synchronization on an "early" edge, and the middle drawing is the reference without synchronization.

Figure 20-12. Synchronization on Late and Early Edges



In the first example, an edge from recessive to dominant occurs at the end of Prop_Seg. The edge is "late" since it occurs after the Sync_Seg. Reacting to the "late" edge, Phase_Seg1 is lengthened so that the distance from the edge to the sample point is the same as it would have been from the Sync_Seg to the sample point if no edge had occurred. The phase error of this "late" edge is less than SJW, so it is fully compensated and the edge from dominant to recessive at the end of the bit, which is one nominal bit time long, occurs in the Sync_Seg.

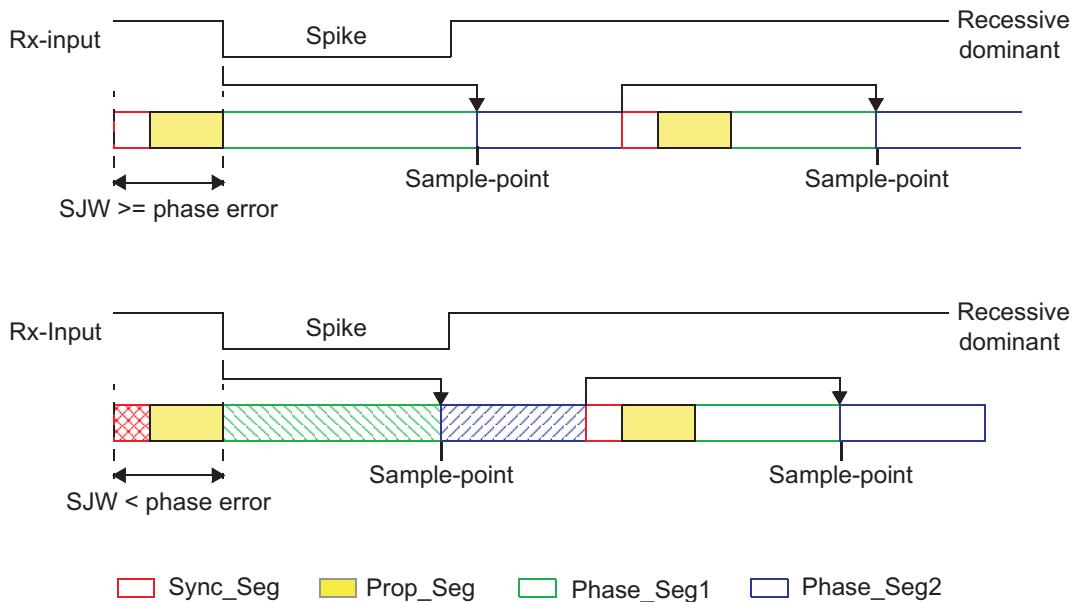
In the second example, an edge from recessive to dominant occurs during Phase_Seg2. The edge is "early" since it occurs before a Sync_Seg. Reacting to the "early" edge, Phase_Seg2 is shortened and Sync_Seg is omitted, so that the distance from the edge to the sample point is the same as it would have been from a Sync_Seg to the sample point if no edge had occurred. As in the previous example, the magnitude of this "early" edge's phase error is less than SJW, so it is fully compensated.

The phase buffer segments are lengthened or shortened temporarily only; at the next bit time, the segments return to their nominal programmed values.

In these examples, the bit timing is seen from the point of view of the CAN implementation's state machine, where the bit time starts and ends at the sample points. The state machine omits Sync_Seg when synchronizing on an "early" edge because it cannot subsequently redefine that time quantum of Phase_Seg2 where the edge occurs to be the Sync_Seg.

The examples in [Figure 20-13](#) show how short dominant noise spikes are filtered by synchronizations. In both examples, the spike starts at the end of Prop_Seg and has the length of (Prop_Seg + Phase_Seg1). In the first example, the synchronization jump width is greater than or equal to the phase error of the spike's edge from recessive to dominant. Therefore the sample point is shifted after the end of the spike; a recessive bus level is sampled.

In the second example, SJW is shorter than the phase error, so the sample point cannot be shifted far enough; the dominant spike is sampled as actual bus level.

Figure 20-13. Filtering of Short Dominant Spikes


20.12.1.4 Oscillator Tolerance Range

With the introduction of CAN protocol version 1.2, the option to synchronize on edges from dominant to recessive became obsolete. Only edges from recessive to dominant are considered for synchronization. The protocol update to version 2.0 (A and B) had no influence on the oscillator tolerance.

The tolerance range df for an oscillator's frequency f_{osc} around the nominal frequency f_{nom} with

$$(1 - df) \cdot f_{nom} \leq f_{osc} \leq (1 + df) \cdot f_{nom}$$

depends on the proportions of Phase_Seg1, Phase_Seg2, SJW, and the bit time. The maximum tolerance df is defined by two conditions (both shall be met):

(9)

$$\text{I: } df \leq \frac{\min(T\text{Seg1}, T\text{seg2})}{2x(13x(\text{bit_time} - T\text{Seg2}))}$$

(10)

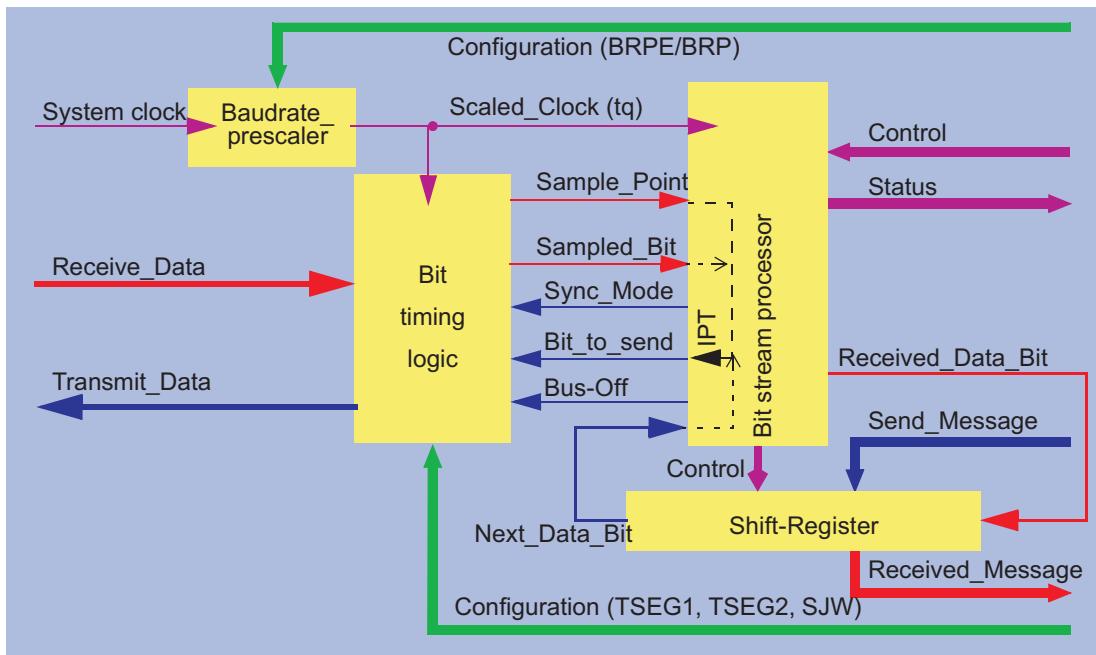
$$\text{II: } df \leq \frac{SJW}{20x\text{bit_time}}$$

It has to be considered that SJW may not be larger than the smaller of the phase buffer segments and that the propagation time segment limits that part of the bit time that may be used for the phase buffer segments.

The combination Prop_Seg = 1 and Phase_Seg1 = Phase_Seg2 = SJW = 4 allows the largest possible oscillator tolerance of 1.58%. This combination with a Propagation Time Segment of only 10% of the bit time is not suitable for short bit times; it can be used for bit rates of up to 125 kBit/s (bit time = 8 μ s) with a bus length of 40 m.

20.12.2 Configuration of the CAN Bit Timing

In the CAN, the bit timing configuration is programmed in two register bytes, additionally a third byte for a baud rate prescaler extension of 4 bits (BRPE) is provided. The sum of Prop_Seg and Phase_Seg1 (as TSEG1) is combined with Phase_Seg2 (as TSEG2) in one byte, SJW and BRP (plus BRPE in third byte) are combined in the other byte (see [Figure 20-14](#)).

Figure 20-14. Structure of the CAN Core's CAN Protocol Controller

In this bit timing register, the components TSEG1, TSEG2, SJW and BRP have to be programmed to a numerical value that is one less than its functional value; so instead of values in the range of [1...n], values in the range of [0...n-1] are programmed. That way, e.g. SJW (functional range of [1...4]) is represented by only two bits.

Therefore the length of the Bit time is (programmed values) $[TSEG1 + TSEG2 + 3] t_q$ or (functional values) $[Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] t_q$.

The data in the Bit Timing Register is the configuration input of the CAN protocol controller. The baud rate prescaler (configured by BRPE/BRP) defines the length of the time quantum (the basic time unit of the bit time); the bit timing logic (configured by TSEG1, TSEG2, and SJW) defines the number of time quanta in the bit time.

The processing of the bit time, the calculation of the position of the Sample Point, and occasional synchronizations are controlled by the Bit timing state machine, which is evaluated once each time quantum. The rest of the CAN protocol controller, the Bit Stream Processor (BSP) state machine, is evaluated once each bit time, at the Sample Point.

The Shift register serializes the messages to be sent and parallelizes received messages. Its loading and shifting is controlled by the BSP.

The BSP translates messages into frames and vice versa. It generates and discards the enclosing fixed format bits, inserts and extracts stuff bits, calculates and checks the CRC code, performs the error management, and decides which type of synchronization is to be used. It is evaluated at the sample point and processes the sampled bus input bit. The time after the sample point that is needed to calculate the next bit to be sent (e.g. data bit, CRC bit, stuff bit, error flag, or idle) is called the Information Processing Time (IPT), which is $0 t_q$ for the CAN.

Generally, the IPT is CAN controller specific, but may not be longer than $2 t_q$. The IPC length is the lower limit of the programmed length of Phase_Seg2. In case of a synchronization, Phase_Seg2 may be shortened to a value less than IPT, which does not affect bus timing.

20.12.2.1 Calculation of the Bit Timing Parameters

Usually, the calculation of the bit timing configuration starts with a desired bit rate or bit time. The resulting Bit time ($1 / \text{Bit rate}$) must be an integer multiple of the CAN clock period.

NOTE: 8 MHz is the minimum CAN clock frequency required to operate the CAN at a bit rate of 1 MBit/s.

The bit time may consist of 8 to 25 time quanta. The length of the time quantum t_q is defined by the Baud Rate Prescaler with $t_q = (\text{Baud Rate Prescaler}) / \text{CAN_CLK}$. Several combinations may lead to the desired bit time, allowing iterations of the following steps.

First part of the bit time to be defined is the Prop_Seg. Its length depends on the delay times measured in the system. A maximum bus length as well as a maximum node delay has to be defined for expandible CAN bus systems. The resulting time for Prop_Seg is converted into time quanta (rounded up to the nearest integer multiple of t_q).

The Sync_Seg is 1 t_q long (fixed), leaving (bit time - Prop_Seg - 1) t_q for the two Phase Buffer Segments. If the number of remaining t_q is even, the Phase Buffer Segments have the same length, Phase_Seg2 = Phase_Seg1, else Phase_Seg2 = Phase_Seg1 + 1.

The minimum nominal length of Phase_Seg2 has to be regarded as well. Phase_Seg2 may not be shorter than any CAN controller's Information Processing Time in the network, which is device dependent and can be in the range of [0...2] t_q .

The length of the synchronization jump width is set to its maximum value, which is the minimum of 4 and Phase_Seg1.

The oscillator tolerance range necessary for the resulting configuration is calculated by the formulas given in [Section 20.12.1.4](#).

If more than one configurations are possible to reach a certain Bit rate, it is recommended to choose the configuration which allows the highest oscillator tolerance range.

CAN nodes with different clocks require different configurations to come to the same bit rate. The calculation of the propagation time in the CAN network, based on the nodes with the longest delay times, is done once for the whole network.

The CAN system's oscillator tolerance range is limited by the node with the lowest tolerance range.

The calculation may show that bus length or bit rate have to be decreased or that the oscillator frequencies' stability has to be increased in order to find a protocol compliant configuration of the CAN bit timing.

The resulting configuration is written into the Bit Timing register:

(Phase_Seg2-1)&(Phase_Seg1+Prop_Seg-1)&
(SynchronizationJumpWidth-1)&(Prescaler-1)

20.12.2.2 Example for Bit Timing at high Baudrate

In this example, the frequency of CAN_CLK is 10 MHz, BRP is 0, the bit rate is 1 MBit/s.

t_q	100 ns	=	$t_{\text{CAN_CLK}}$
delay of bus driver	90 ns	=	
delay of receiver circuit	40 ns	=	
delay of bus line (40m)	220 ns	=	
t_{Prop}	700 ns	=	$2^* \text{delays} = 7 \cdot t_q$
t_{SJW}	100 ns	=	$1 \cdot t_q$
t_{TSeg1}	800 ns	=	$t_{\text{Prop}} + t_{\text{SJW}}$
t_{TSeg2}	100 ns	=	Information Processing Time + $1 \cdot t_q$
$t_{\text{Sync-Seg}}$	100 ns	=	$1 \cdot t_q$
bit time	1000 ns	=	$t_{\text{Sync-Seg}} + t_{\text{TSeg1}} + t_{\text{TSeg2}}$
tolerance for CAN_CLK	0.43 %	=	$\frac{\min(\text{TSeg1}, \text{Tseg2})}{2x(13x(\text{bit_time}-\text{TSeg2}))}$

$$= \frac{0,1\mu s}{2x(13x(1\mu s 0,1\mu s))}$$

In this example, the concatenated bit time parameters are $(1\text{-}1)_3\&(8\text{-}1)_4\&(1\text{-}1)_2\&(1\text{-}1)_6$, so the Bit Timing Register is programmed to = 0x00000700.

20.12.2.3 Example for Bit Timing at low Baudrate

In this example, the frequency of CAN_CLK is 2 MHz, BRP is 1, the bit rate is 100 KBit/s.

t_q	1 μs	=	$2 \cdot t_{CAN_CLK}$
delay of bus driver	200 ns	=	
delay of receiver circuit	80 ns	=	
delay of bus line (40m)	220 ns	=	
t_{Prop}	1 μs	=	$1 \cdot t_q$
t_{SJW}	4 μs	=	$4 \cdot t_q$
t_{TSeg1}	5 μs	=	$t_{Prop} + t_{SJW}$
t_{TSeg2}	4 μs	=	Information Processing Time + $4 \cdot t_q$
$t_{Sync-Seg}$	1 μs	=	$1 \cdot t_q$
bit time	10 μs	=	$t_{Sync-Seg} + t_{TSeg1} + t_{TSeg2}$
tolerance for CAN_CLK	3.08 %	=	$\frac{\min(TSeg1, TSeg2)}{2x(13x(bit_time-TSeg2))}$
		=	$\frac{4\mu s}{2x(13x(9\mu s - 4\mu s))}$

In this example, the concatenated bit time parameters are $(4\text{-}1)_3\&(5\text{-}1)_4\&(4\text{-}1)_2\&(2\text{-}1)_6$, so the Bit Timing register is programmed to = 0x000034C1.

20.13 Message Interface Register Sets

The interface register sets control the CPU read and write accesses to the Message RAM. There are two interface register sets for read / write access (IF1 and IF2) and one Interface Register Set for read access only (IF3).

Due to the structure of the Message RAM, it is not possible to change single bits or bytes of a message object. Instead, always a complete message object in the Message RAM is accessed. Therefore the data transfer from the IF1/IF2 registers to the Message RAM requires the message handler to perform a read-modifywrite cycle: First those parts of the message object that are not to be changed are read from the Message RAM into the Interface Register set, and after the update the whole content of the Interface Register set is written into the message object.

After the partial write of a message object, those parts of the Interface Register set which are not selected in the Command Register, will be set to the actual contents of the selected message object. After the partial read of a message object, those parts of the Interface Register set which are not selected in the Command Register, will be left unchanged.

By buffering the data to be transferred, the Interface Register sets avoid conflicts between concurrent CPU accesses to the Message RAM and CAN message reception and transmission. A complete message object (see [Section 20.14.1](#)) or parts of the message object may be transferred between the Message RAM and the IF1/IF2 Register set in one single transfer. This transfer, performed in parallel on all selected parts of the message object, guarantees the data consistency of the CAN message.

That being said, there is one condition that can cause a write access to the message RAM to be lost. If $MsgVal = 1$ for the message object which is accessed and CAN communication is ongoing, a transfer from the IFx register to message RAM may be lost. The reason for this is that it might happen that the IFx register write to the message RAM occurs in between a read-modify-write access of the Host Message Handler when it is in the process of receiving a message for the same message object.

To avoid this issue with receive mail boxes, reset MsgVal before changing any of the following: Id28-0, Xtd, Dir, DLC3-0, RxIE, TxIE, RmtEn, EoB, Umask, Msk28-0, MXtd, and MDir.

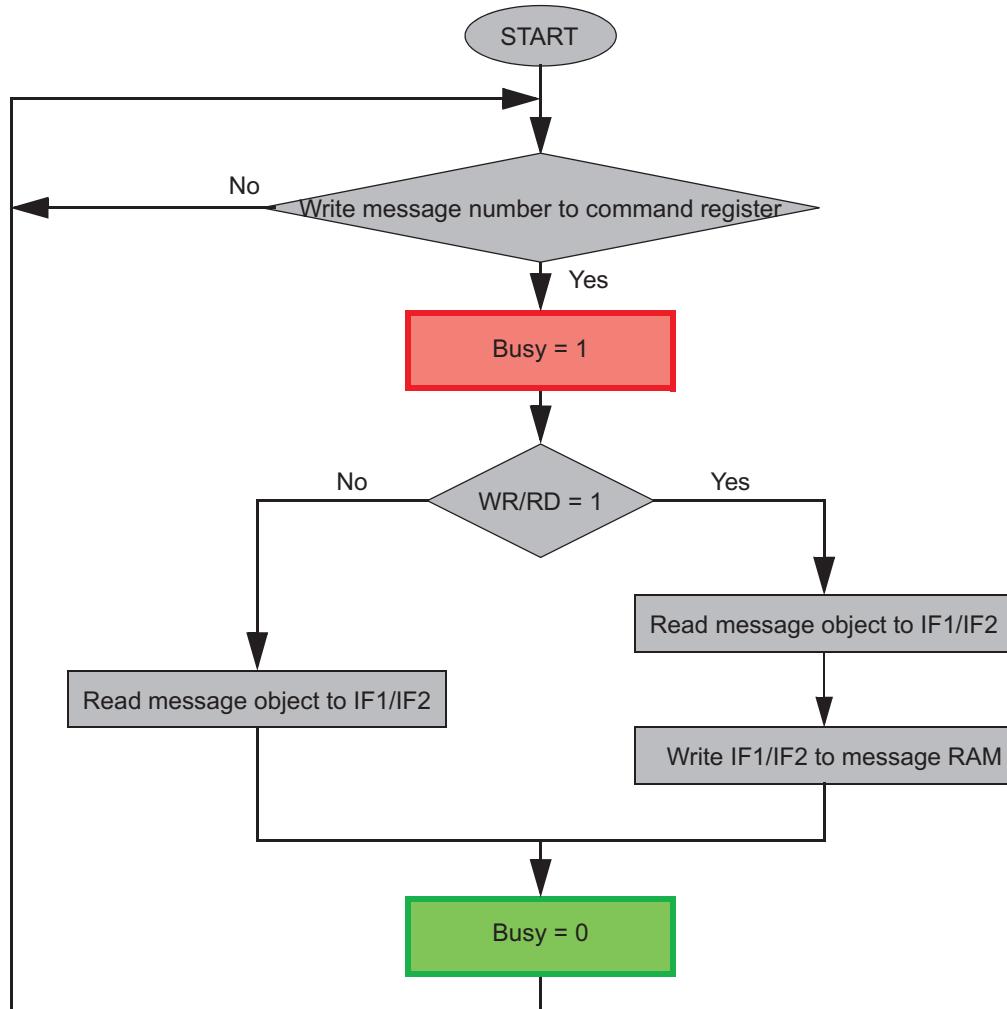
To avoid this issue with transmit mail boxes, reset MsgVal before changing any of the following: Dir, RxIE, TxIE, RmtEn, EoB, Umask, Msk28-0, MXtd, and MDir. Other fields not listed above, like Data, may be changed without fear of losing a write to the message RAM.

20.13.1 Message Interface Register Sets 1 and 2

The IF1 and IF2 registers Sets control the data transfer to and from the message object. The Command Register addresses the desired message object in the Message RAM and specifies whether a complete message object or only parts should be transferred. The data transfer is initiated by writing the message number to the bits [7:0] of the Command Register.

When the CPU initiates a data transfer between the IF1/IF2 registers and Message RAM, the message handler sets the Busy bit in the respective Command Register to '1'. After the transfer has completed, the Busy bit is set back to '0' (see [Figure 20-15](#)).

Figure 20-15. Data Transfer Between IF1 / IF2 Registers and Message RAM



20.13.2 IF3 Register Set

The IF3 register set can automatically be updated with received message objects without the need to initiate the transfer from Message RAM by CPU. The automatic update functionality can be programmed for each message object (see IF3 Update Enable register).

All valid message objects in Message RAM which are configured for automatic update, will be checked for active NewDat flags. If such a message object is found, it will be transferred to the IF3 register, controlled by IF3 Observation register. If more than one NewDat flag is active, the message object with the lowest number has the highest priority for automatic IF3 update.

The NewDat bit in the message object will be reset by a transfer to IF3.

If CAN internal IF3 update is complete, an IF3 interrupt can also be generated.

NOTE: The IF3 register set can not be used for transferring data into message objects.

20.14 Message RAM

The CAN Message RAM contains message objects and parity bits for the message objects. There are 32 message objects in the Message RAM.

During normal operation, accesses to the Message RAM are performed via the Interface Register sets, and the CPU cannot directly access the Message RAM.

The Interface Register sets IF1 and IF2 provide indirect read/write access from the CPU to the Message RAM. The IF1 and IF2 register sets can buffer control and user data to be transferred to and from the message objects.

The third Interface Register set IF3 can be configured to automatically receive control and user data from the Message RAM when a message object has been updated after reception of a CAN message. The CPU does not need to initiate the transfer from Message RAM to IF3 Register set.

The message handler avoids potential conflicts between concurrent accesses to Message RAM and CAN frame reception/transmission.

The message RAM can only be accessed in debug mode. The message RAM base address is 0x2000 above the base address of the CAN peripheral.

20.14.1 Structure of Message Objects

Figure 20-16 shows the structure of a message object.

The grayed fields are those parts of the message object which are represented in dedicated registers. For example, the transmit request flags of all message objects are represented in centralized transmit request registers.

Figure 20-16. Structure of a Message Object

Message Object												
UMask	Msk[28:0]	MXtd	MDir	EoB	unused	NewDat	MsgLst	RxE	TxE	IntPnd	RmtEn	TxRqst
MsgVal	ID[28:0]	Xtd	Dir	DLC[3:0]	Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7

Table 20-2. Message Object Field Descriptions

Name	Value	Description
MsgVal	0	Message valid The message object is ignored by the message handler.
	1	The message object is to be used by the message handler. Note: This bit may be kept at level '1' even when the identifier bits ID[28:0], the control bits Xtd, Dir, or the data length code DLC[3:0] are changed. It should be reset if the Messages Object is no longer required.
UMask	0	Use Acceptance Mask Mask bits (Msk[28:0], MXtd and MDir) are ignored and not used for acceptance filtering.
	1	Mask bits are used for acceptance filtering. Note: If the UMask bit is set to one, the message object's mask bits have to be programmed during initialization of the message object before MsgVal is set to one.

Table 20-2. Message Object Field Descriptions (continued)

Name	Value	Description
ID[28:0]	ID[28:0] ID[28:18]	Message Identifier 29-bit ("extended") identifier bits 11-bit ("standard") identifier bits
Msk[28:0]	0 1	Identifier Mask The corresponding bit in the message identifier is not used for acceptance filtering (don't care). The corresponding bit in the message identifier is used for acceptance filtering.
Xtd	0 1	Extended Identifier The 11-bit ("standard") identifier will be used for this message object. The 29-bit ("extended") identifier will be used for this message object.
MXtd	0 1	Mask Extended Identifier The extended identifier bit (IDE) has no effect on the acceptance filtering. The extended identifier bit (IDE) is used for acceptance filtering. Note: When 11-bit ("standard") Identifiers are used for a message object, the identifiers of received data frames are written into bits ID[28:18]. For acceptance filtering, only these bits together with mask bits Msk[28:18] are considered.
Dir	0 1	Message Direction Direction = receive: On TxRqst, a remote frame with the identifier of this message object is transmitted. On reception of a data frame with matching identifier, the message is stored in this message object. Direction = transmit: On TxRqst, a data frame is transmitted. On reception of a remote frame with matching identifier, the TxRqst bit of this message object is set (if RmtEn = one).
MDir	0 1	Mask Message Direction The message direction bit (Dir) has no effect on the acceptance filtering. The message direction bit (Dir) is used for acceptance filtering.
EOB	0 1	End of Block The message object is part of a FIFO Buffer block and is not the last message object of this FIFO Buffer block. The message object is a single message object or the last message object in a FIFO Buffer Block. Note: This bit is used to concatenate multiple message objects to build a FIFO Buffer. For single message objects (not belonging to a FIFO Buffer), this bit must always be set to one.
NewDat	0 1	New Data No new data has been written into the data bytes of this message object by the message handler since the last time when this flag was cleared by the CPU. The message handler or the CPU has written new data into the data bytes of this message object.
MsgLst	0 1	Message Lost (only valid for Message Objects with direction = receive) No message was lost since the last time when this bit was reset by the CPU. The message handler stored a new message into this message object when NewDat was still set, so the previous message has been overwritten.
RxIE	0 1	Receive Interrupt Enable IntPnd will not be triggered after the successful reception of a frame. IntPnd will be triggered after the successful reception of a frame.
TxIE	0 1	Transmit Interrupt Enable IntPnd will not be triggered after the successful transmission of a frame. IntPnd will be triggered after the successful transmission of a frame.
IntPnd	0 1	Interrupt Pending This message object is not the source of an interrupt. This message object is the source of an interrupt. The Interrupt Identifier in the Interrupt Register will point to this message object if there is no other interrupt source with higher priority.

Table 20-2. Message Object Field Descriptions (continued)

Name	Value	Description
RmtEn	0 1	Remote Enable At the reception of a remote frame, TxRqst is not changed. At the reception of a remote frame, TxRqst is set. Note: See Section 20.11.8 for details on the setup of RmtEn and UMask for remote frames.
TxRqst	0 1	Transmit Request This message object is not waiting for a transmission. The transmission of this message object is requested and is not yet done.
DLC[3:0]	0 1	Data length code Data frame has 0-8 data bits. Data frame has 8 data bytes. Note: The data length code of a message object must be defined to the same value as in the corresponding objects with the same identifier at other nodes. When the message handler stores a data frame, it will write the DLC to the value given by the received message.
Data 0 Data 1 Data 2 Data 3 Data 4 Data 5 Data 6 Data 7		1st data byte of a CAN data frame 2nd data byte of a CAN data frame 3rd data byte of a CAN data frame 4th data byte of a CAN data frame 5th data byte of a CAN data frame 6th data byte of a CAN data frame 7th data byte of a CAN data frame 8th data byte of a CAN data frame Note: Byte Data 0 is the first data byte shifted into the shift register of the CAN Core during a reception, byte Data 7 is the last. When the message handler stores a data frame, it will write all the eight data bytes into a message object. If the data length code is less than 8, the remaining bytes of the message object may be overwritten by undefined values.

20.14.2 Addressing Message Objects in RAM

The starting location of a particular message object in RAM is:

Message RAM base address + (message object number) * 0x20.

This means that Message Object 1 starts at offset 0x0020; Message Object 2 starts at offset 0x0040, etc.

NOTE: '0' is not a valid message object number. At address 0x0000, the last message object (32) (with the lowest priority) is located. Writing to the address of an unimplemented message object may overwrite an implemented message object.

Message Object number 1 has the highest priority.

Table 20-3. Message RAM Addressing in Debug Mode

Message Object Number	Offset From Base Address	Word Number	Debug Mode ⁽¹⁾
last implemented (here:32)	0x0000	1	Parity
	0x0004	2	MXtd,MDir,Mask
	0x0008	3	Xtd,Dir,ID
	0x000C	4	Ctrl
	0x0010	5	Data Bytes 3-0
	0x0014	6	Data Bytes 7-4

⁽¹⁾ See [Section 20.14.3](#).

Table 20-3. Message RAM Addressing in Debug Mode (continued)

Message Object Number	Offset From Base Address	Word Number	Debug Mode ⁽¹⁾
1	0x0020	1	Parity
	0x0024	2	MXtd,MDir,Mask
	0x0028	3	Xtd,Dir,ID
	0x002C	4	Ctrl
	0x0030	5	Data Bytes 3-0
	0x0034	6	Data Bytes 7-4
2	0x0040	1	Parity
	0x0044	2	MXtd,MDir,Mask
	0x0048	3	Xtd,Dir,ID
	0x004C	4	Ctrl
	0x0050	5	Data Bytes 3-0
	0x0054	6	Data Bytes 7-4
...
31	0x03E0	1	Parity
	0x03E4	2	MXtd,MDir,Mask
	0x03E8	3	Xtd,Dir,ID
	0x03EC	4	Ctrl
	0x03F0	5	Data Bytes 3-0
	0x03F4	6	Data Bytes 7-4

20.14.3 Message RAM Representation in Debug Mode

In debug mode, the Message RAM will be memory mapped. This allows the external debug unit to access the Message RAM.

NOTE: During debug mode, the Message RAM cannot be accessed via the IFx register sets.

Figure 20-17. Message RAM Representation in Debug Mode

31/ 15	30/ 14	29/ 13	28/ 12	27/ 11	26/ 10	25/ 9	24/ 8	23/ 7	22/ 6	21/ 5	20/ 4	19/ 3	18/ 2	17/ 1	16/ 0						
MsgAddr + 0x00																					
Reserved										Parity[4:0]											
MsgAddr + 0x04																					
MXtd MDir Rsvd Msk[28:16] Msk[15:0]																					
MsgAddr + 0x08																					
Rsvd Xtd Dir ID[28:16] ID[15:0]																					
MsgAddr + 0x0C																					
Reserved Rsvd MsgLs t Rsvd UMask TxIE RxIE RmtEn Rsvd EOB Reserved DLC[3:0]																					
MsgAddr + 0x10																					
Data 3 Data 2 Data 1 Data 0																					
MsgAddr + 0x14																					
Data 7 Data 6 Data 5 Data 4																					

20.15 Registers

20.15.1 CAN Base Addresses

Table 20-4. CAN Base Addresses Table

Device Registers	Register Name	Start Address	End Address
CanaRegs	CAN_REGS	0x0004_8000	0x0004_87FF
CanbRegs	CAN_REGS	0x0004_A000	0x0004_A7FF

20.15.2 CAN_REGS Registers

Table 20-5 lists the memory-mapped registers for the CAN_REGS. All register offset addresses not listed in **Table 20-5** should be considered as reserved locations and the register contents should not be modified.

Table 20-5. CAN_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	CAN_CTL	CAN Control Register	Section 20.15.2.1	EALLOW
4h	CAN_ES	Error and Status Register	Section 20.15.2.2	
8h	CAN_ERRC	Error Counter Register	Section 20.15.2.3	
Ch	CAN_BTR	Bit Timing Register	Section 20.15.2.4	
10h	CAN_INT	Interrupt Register	Section 20.15.2.5	
14h	CAN_TEST	Test Register	Section 20.15.2.6	
1Ch	CAN_PERR	CAN Parity Error Code Register	Section 20.15.2.7	
20h	CAN_REL	CAN Core Release Register	Section 20.15.2.8	
40h	CAN_RAM_INIT	CAN RAM Initialization Register	Section 20.15.2.9	
50h	CAN_GLB_INT_EN	CAN Global Interrupt Enable Register	Section 20.15.2.10	
54h	CAN_GLB_INT_FLG	CAN Global Interrupt Flag Register	Section 20.15.2.11	
58h	CAN_GLB_INT_CLR	CAN Global Interrupt Clear Register	Section 20.15.2.12	
80h	CAN_ABOTR	Auto-Bus-On Time Register	Section 20.15.2.13	
84h	CAN_TXRQ_X	CAN Transmission Request X Register	Section 20.15.2.14	
88h	CAN_TXRQ_21	CAN Transmission Request 2_1 Register	Section 20.15.2.15	
98h	CAN_NDAT_X	CAN New Data X Register	Section 20.15.2.16	
9Ch	CAN_NDAT_21	CAN New Data 2_1 Register	Section 20.15.2.17	
ACh	CAN_IPEN_X	CAN Interrupt Pending X Register	Section 20.15.2.18	
B0h	CAN_IPEN_21	CAN Interrupt Pending 2_1 Register	Section 20.15.2.19	
C0h	CAN_MVAL_X	CAN Message Valid X Register	Section 20.15.2.20	
C4h	CAN_MVAL_21	CAN Message Valid 2_1 Register	Section 20.15.2.21	
D8h	CAN_IP_MUX21	CAN Interrupt Multiplexer 2_1 Register	Section 20.15.2.22	
100h	CAN_IF1CMD	IF1 Command Register	Section 20.15.2.23	
104h	CAN_IF1MSK	IF1 Mask Register	Section 20.15.2.24	
108h	CAN_IF1ARB	IF1 Arbitration Register	Section 20.15.2.25	

Table 20-5. CAN_REGS REGISTERS (continued)

Offset	Acronym	Register Name	Section	Write Protection
10Ch	CAN_IF1MCTL	IF1 Message Control Register	Section 20.15.2.26	
110h	CAN_IF1DATA	IF1 Data A Register	Section 20.15.2.27	
114h	CAN_IF1DATB	IF1 Data B Register	Section 20.15.2.28	
120h	CAN_IF2CMD	IF2 Command Register	Section 20.15.2.29	
124h	CAN_IF2MSK	IF2 Mask Register	Section 20.15.2.30	
128h	CAN_IF2ARB	IF2 Arbitration Register	Section 20.15.2.31	
12Ch	CAN_IF2MCTL	IF2 Message Control Register	Section 20.15.2.32	
130h	CAN_IF2DATA	IF2 Data A Register	Section 20.15.2.33	
134h	CAN_IF2DATB	IF2 Data B Register	Section 20.15.2.34	
140h	CAN_IF3OBS	IF3 Observation Register	Section 20.15.2.35	
144h	CAN_IF3MSK	IF3 Mask Register	Section 20.15.2.36	
148h	CAN_IF3ARB	IF3 Arbitration Register	Section 20.15.2.37	
14Ch	CAN_IF3MCTL	IF3 Message Control Register	Section 20.15.2.38	
150h	CAN_IF3DATA	IF3 Data A Register	Section 20.15.2.39	
154h	CAN_IF3DATB	IF3 Data B Register	Section 20.15.2.40	
160h	CAN_IF3UPD	IF3 Update Enable Register	Section 20.15.2.41	

20.15.2.1 CAN_CTL Register (offset = 0h) [reset = 1401h]

CAN_CTL is shown in [Figure 20-18](#) and described in [Table 20-6](#).

CAN Control Register

Figure 20-18. CAN_CTL Register

31	30	29	28	27	26	25	24
RESERVED					WUBA	PDR	
R-0h					R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
RESERVED			RESERVED	RESERVED	RESERVED	IE1	INITDBG
R-0h			R-0h	R-0h	R-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
SWR	RESERVED	PMD				ABO	IDS
R/W-0h	R-0h	R/W-5h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
Test	CCE	DAR	RESERVED	EIE	SIE	IE0	Init
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-6. CAN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	WUBA	R/W	0h	Automatic wake up on bus activity Enable Bit: This bit is used to enable/disable Automatic wake up on bus activity, when in local power down mode. 0 No detection of a dominant CAN bus level while in local power down mode. 1 Detection of a dominant CAN bus level while in local power down mode is enabled. On occurrence of a dominant CAN bus level, the wake up
24	PDR	R/W	0h	Power Down Mode Request Bit: This bit is used to put the CAN module in local power down mode. 0 No application request for local low power down mode. If the application has cleared this bit while CAN is in power down mode, the INIT bit has to be cleared as well. 1 Power down mode has been requested by application. The CAN module will acknowledge this mode by setting the PDA bit in Error and Status Register. The local clocks will be turned off by CAN internal logic.
23-21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	IE1	R/W	0h	Interrupt line 1 Enable Bit: This bit is used to enable/disable interrupt line 1 (CANn_INT1) 0 Disabled. 1 Enabled.

Table 20-6. CAN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	INITDBG	R	0h	Debug Mode Status Bit: This bit indicates the internal init state for a debug access 0 Not in debug mode, or debug mode requested but not entered. 1 Debug mode requested and internally entered the CAN is ready for debug accesses.
15	SWR	R/W	0h	Software Reset Enable Bit: This bit activates the software reset. 0 Normal Operation. 1 Module is forced to reset state. This bit will get cleared automatically one clock cycle after execution of software reset. Note: To execute software reset, the following procedure is necessary: 1. Set INIT bit to shut down CAN communication. 2. Set SWR bit. This bit is EALLOW protected. Note: This bit is write Protected by Init bit
14	RESERVED	R	0h	Reserved
13-10	PMD	R/W	5h	Parity on/off - 0101 Parity function disabled xxxx Parity function enabled
9	ABO	R/W	0h	Auto-Bus-On Enable - 0 The Auto-Bus-On feature is disabled 1 The Auto-Bus-On feature is enabled
8	IDS	R/W	0h	Interruption Debug Support Enable - 0 When Debug mode is requested, CAN will wait for a started transmission or reception to be completed before entering Debug mode 1 When Debug mode is requested, CAN will interrupt any transmission or reception, and enter Debug mode immediately.
7	Test	R/W	0h	Test Mode Enable - Normal Operation Test Mode
6	CCE	R/W	0h	Configuration Change Enable - 0 The CPU has no write access to the configuration registers. 1 The CPU has write access to the configuration registers (when Init bit is set).
5	DAR	R/W	0h	Disable Automatic Retransmission - 0 Automatic Retransmission of not successful messages enabled. 1 Automatic Retransmission disabled.
4	RESERVED	R	0h	Reserved
3	EIE	R/W	0h	Error Interrupt Enable Disabled - 0 PER, BOff and EWarn bits can not generate an interrupt. 1 Enabled- PER, BOff and EWarn bits can generate an interrupt at CAN0INT line and affect the Interrupt Register.
2	SIE	R/W	0h	Status Change Interrupt Enable Disabled - 0 WakeUpPnd, RxOk, TxOk and LEC bits can not generate an interrupt. 1 Enabled - WakeUpPnd, RxOk, TxOk and LEC can generate an interrupt at CAN0INT line and affect the Interrupt Register.
1	IE0	R/W	0h	Interrupt line 0 Enable Disabled - 0 Module Interrupt CAN0INT is always low. 1 Enabled - Interrupts will assert line CAN0INT to one line remains active until pending interrupts are processed.
0	Init	R/W	1h	Initialization Normal Operation Initialization mode is entered

20.15.2.2 CAN_ES Register (offset = 4h) [reset = 3h]

CAN_ES is shown in [Figure 20-19](#) and described in [Table 20-7](#).

Error and Status Register

Figure 20-19. CAN_ES Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					PDA	WakeUpPnd	PER
R-0h							
7	6	5	4	3	2	1	0
BOff	EWarn	EPass	RxOk	TxOk		LEC	
R-0h	R-0h	R-0h	R-0h	R-0h		R-3h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-7. CAN_ES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	PDA	R	0h	Local power down mode acknowledge: 0 CAN is not in local power down mode. 1 Application request for setting CAN to local power down mode was successful. CAN is in local power down mode.
9	WakeUpPnd	R	0h	Wakeup pending: This bit can be used by the CPU to identify the CAN as the source to wake up the system. The bit will be reset after the CPU reads the register. 0 No Wake Up is requested by CAN. 1 CAN has initiated a wake up of the system due to dominant CAN bus while module power down.
8	PER	R	0h	Parity/double bit Error Detected: This bit will be reset after the CPU reads the register. 0 No parity/double bit error has been detected since last read access. 1 The parity check/SECDED mechanism has detected a parity/double bit error in the Message RAM.
7	BOff	R	0h	Bus-off Status Bit: 0 The CAN module is not Bus-Off state. 1 The CAN module is in Bus-Off state.
6	EWarn	R	0h	Warning State Bit: 0 Both error counters are below the error warning limit of 96. 1 At least one of the error counters has reached the error warning limit of 96.
5	EPass	R	0h	Error Passive State - 0 On CAN Bus error, the CAN could send active error frames. 1 The CAN Core is in the error passive state as defined in the CAN Specification.

Table 20-7. CAN_ES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RxOk	R	0h	<p>Reception status Bit: This bit indicates the status of reception. The bit will be reset after the CPU reads the register.</p> <p>0 No message has been successfully received since the last time when this bit was read by the CPU. This bit is never reset by CAN internal events.</p> <p>1 A message has been successfully received since the last time when this bit was reset by a read access of the CPU.</p>
3	TxOk	R	0h	<p>Transmission status Bit: This bit indicates the status of transmission. The bit will be reset after the CPU reads the register.</p> <p>0 No message has been successfully transmitted since the last time when this bit was read by the CPU. This bit is never reset by CAN internal events.</p> <p>1 A message has been successfully transmitted (error free and acknowledged by at least one other node) since the last time when this bit was cleared by a read access of the CPU.</p>
2-0	LEC	R	3h	<p>Last Error Code</p> <p>The LEC field indicates the type of the last error on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. This field will be reset to '7' whenever the CPU reads the register.</p> <p>0 No Error</p> <p>1 Stuff Error: More than five equal bits in a row have been detected in a part of a received message where this is not allowed.</p> <p>2 Form Error: A fixed format part of a received frame has the wrong format.</p> <p>3 Ack Error: The message this CAN Core transmitted was not acknowledged by another node.</p> <p>4 Bit1 Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant.</p> <p>5 Bit0 Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (logical value '0'), but the monitored bus level was recessive. During Bus-Off recovery, this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus-Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).</p> <p>6 CRC Error: In a received message, the CRC check sum was incorrect. (CRC received for an incoming message does not match the calculated CRC for the received data).</p> <p>7 No CAN bus event was detected since the last time when CPU has read the Error and Status Register. Any read access to the Error and Status Register re-initializes the LEC to value '7'.</p>

20.15.2.3 CAN_ERRC Register (offset = 8h) [reset = 0h]

CAN_ERRC is shown in [Figure 20-20](#) and described in [Table 20-8](#).

Error Counter Register

Figure 20-20. CAN_ERRC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP					REC						TEC				
R-0h					R-0h						R-0h				

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

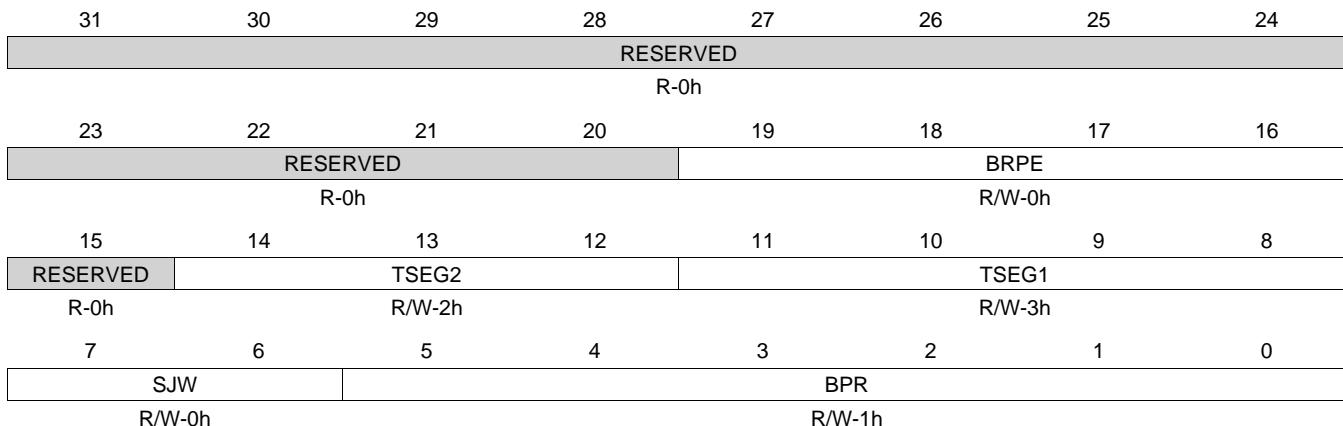
Table 20-8. CAN_ERRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	RP	R	0h	Receive Error Passive- 0 The Receive Error Counter is below the error passive level. 1 The Receive Error Counter has reached the error passive level as defined in the CAN Specification.
14-8	REC	R	0h	Receive Error Counter: Actual state of the Receive Error Counter. (values from 0 to 127).
7-0	TEC	R	0h	Transmit Error Counter - Actual state of the Transmit Error Counter. (values from 0 to 255).

20.15.2.4 CAN_BTR Register (offset = Ch) [reset = 2301h]

CAN_BTR is shown in [Figure 20-21](#) and described in [Table 20-9](#).

Bit Timing Register

Figure 20-21. CAN_BTR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-9. CAN_BTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	BRPE	R/W	0h	Baud Rate Prescaler Extension- Valid programmed values are 0 to 15. By programming BRPE the Baud Rate Prescaler can be extended to values up to 1024. Note: This bit is Write Protected by CCE bit.
15	RESERVED	R	0h	Reserved
14-12	TSEG2	R/W	2h	Time segment after the sample point Valid programmed values are 0 to 7. The actual TSeg2 value which is interpreted for the Bit Timing will be the programmed TSeg2 value + 1. Note: This bit is Write Protected by CCE bit.
11-8	TSEG1	R/W	3h	Time segment before the sample point Valid programmed values are 1 to 15. The actual TSeg1 value interpreted for the Bit Timing will be the programmed TSeg1 value + 1. Note: This bit is Write Protected by CCE bit.
7-6	SJW	R/W	0h	Synchronization Jump Width Valid programmed values are 0 to 3. The actual SJW value interpreted for the Synchronization will be the programmed SJW value + 1. Note: This bit is Write Protected by CCE bit.
5-0	BPR	R/W	1h	Baud Rate Prescaler- Value by which the CAN_CLK frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid programmed values are 0 to 63. The actual BRP value interpreted for the Bit Timing will be the programmed BRP value + 1. Note: This bit is Write Protected by CCE bit.

20.15.2.5 CAN_INT Register (offset = 10h) [reset = 0h]

CAN_INT is shown in [Figure 20-22](#) and described in [Table 20-10](#).

Interrupt Register

Figure 20-22. CAN_INT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										INT1ID										INT0ID											
R-0h										R-0h										R-0h											

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

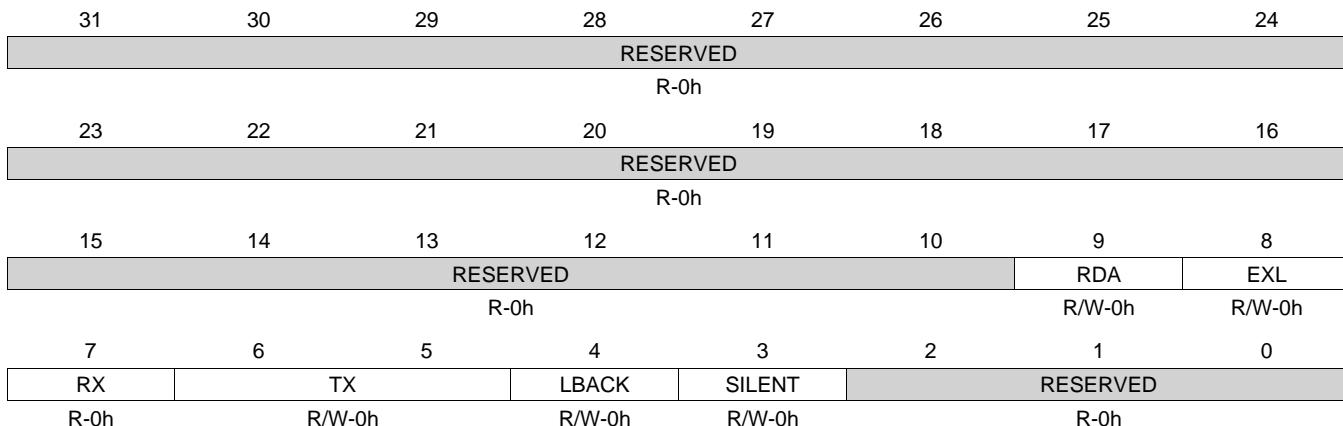
Table 20-10. CAN_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	INT1ID	R	0h	<p>Interrupt Identifier 1: The number here indicates the source of the interrupt.</p> <p>0x00 No interrupt is pending.</p> <p>0x01-0x20 Number of mailbox (mailbox) which caused the interrupt.</p> <p>0x21-0xFF Unused.</p> <p>If several interrupts are pending, the CAN Interrupt Register will point to the pending interrupt with the highest priority.</p> <p>The CANn_INT1 interrupt line remains active until INT0ID reaches value 0 (the cause of the interrupt is reset) or until IE0 is cleared.</p> <p>A message interrupt is cleared by clearing the mailbox's IntPnd bit.</p> <p>Among the message interrupts, the mailbox's interrupt priority decreases with increasing message number.</p>
15-0	INT0ID	R	0h	<p>Interrupt Identifier (the number here indicates the source of the interrupt)</p> <p>0x0000 No interrupt is pending</p> <p>0x0001- Number of message object which caused the interrupt.</p> <p>0x0080 0x0081- Unused</p> <p>0x7FFF 0x8000 Error and Status Register value is not 0x07.</p> <p>0x8001- Unused If several interrupts are pending, the CAN Interrupt Register will point to the pending 0xFFFF interrupt with the highest priority.</p> <p>The CAN0INT interrupt line remains active until Int0ID reaches value 0 (the cause of the interrupt is reset) or until IE0 is cleared. The Status Interrupt has the highest priority. Among the message interrupts, the message object's interrupt priority decreases with increasing message number.</p>

20.15.2.6 CAN_TEST Register (offset = 14h) [reset = 0h]

CAN_TEST is shown in [Figure 20-23](#) and described in [Table 20-11](#).

Test Register

Figure 20-23. CAN_TEST Register

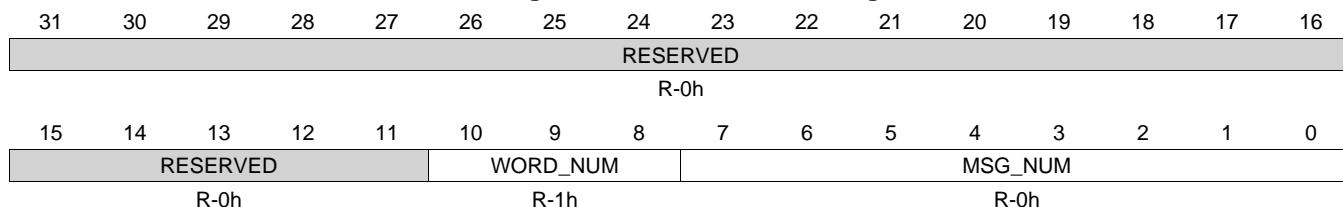
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-11. CAN_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	RDA	R/W	0h	RAM Direct Access Enable: 0 Normal Operation. 1 Direct access to the RAM is enabled while in Test Mode.
8	EXL	R/W	0h	External Loop Back Mode: 0 Disabled. 1 Enabled.
7	RX	R	0h	Monitors the actual value of the CANRX pin: 0 The CAN bus is dominant. 1 The CAN bus is recessive.
6-5	TX	R/W	0h	Control of CANTX pin: 00 Normal operation, CANTX is controlled by the CAN Core. 01 Sample Point can be monitored at CANTX pin. 10 CANTX pin drives a dominant value. 11 CANTX pin drives a recessive value.
4	LBACK	R/W	0h	Loop Back Mode: 0 Disabled. 1 Enabled.
3	SILENT	R/W	0h	Silent Mode: 0 Disabled. 1 Enabled.
2-0	RESERVED	R	0h	Reserved

20.15.2.7 CAN_PERR Register (offset = 1Ch) [reset = 100h]CAN_PERR is shown in [Figure 20-24](#) and described in [Table 20-12](#).

CAN Parity Error Code Register

Figure 20-24. CAN_PERR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-12. CAN_PERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	WORD_NUM	R	1h	0x01-0x05 Word number where parity error has been detected. RDA word number (1 to 5) of the mailbox (according to the Message RAM representation in RDA mode, see section 1.18.5). For the SECDED implementation the Word Number is 'Rsvd' and it will read always as 0x0.
7-0	MSG_NUM	R	0h	0x01-0x21 Mailbox number where parity/double bit error has been detected

20.15.2.8 CAN_REL Register (offset = 20h) [reset = A3170504h]

CAN_REL is shown in [Figure 20-25](#) and described in [Table 20-13](#).

CAN Core Release Register

Figure 20-25. CAN_REL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
R-Ah				R-3h				R-1h				R-7h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON								DAY							
R-5h								R-4h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-13. CAN_REL Register Field Descriptions

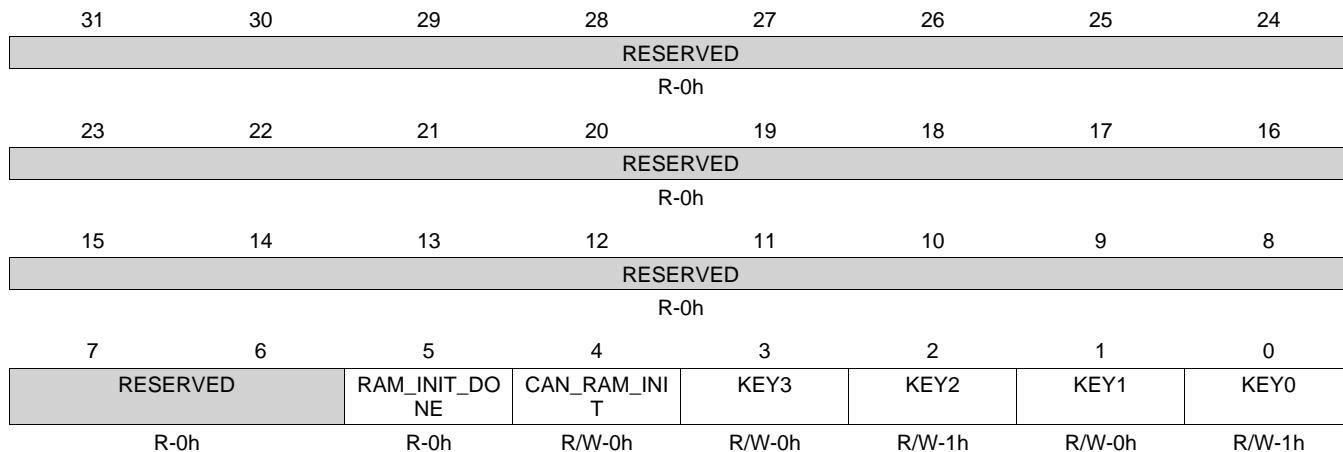
Bit	Field	Type	Reset	Description
31-28	REL	R	Ah	Core Release One digit, BCD-coded.
27-24	STEP	R	3h	Step of Core Release One digit, BCD-coded.
23-20	SUBSTEP	R	1h	Substep of Core Release One digit, BCD-coded.
19-16	YEAR	R	7h	Design Time Stamp, Year One-digit BCD-coded year value from the CAN synthesis time stamp. This constant value is for TI internal use only.
15-8	MON	R	5h	Design Time Stamp, Month Two-digit BCD-coded month value from the CAN synthesis time stamp. This constant value is for TI internal use only.
7-0	DAY	R	4h	Design Time Stamp, Day Two-digit BCD-coded day value from the CAN synthesis time stamp. This constant value is for TI internal use only.

20.15.2.9 CAN_RAM_INIT Register (offset = 40h) [reset = 5h]

CAN_RAM_INIT is shown in [Figure 20-26](#) and described in [Table 20-14](#).

CAN RAM Initialization Register

Figure 20-26. CAN_RAM_INIT Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

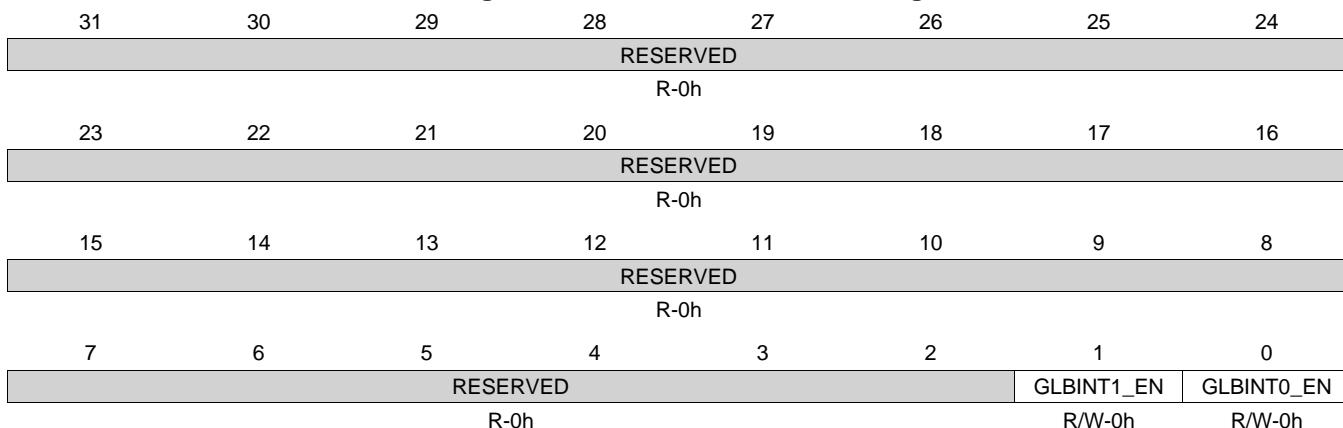
Table 20-14. CAN_RAM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	RAM_INIT_DONE	R	0h	CAN Mailbox RAM initialization status: 0 Read: Initialization is on-going or initialization not initiated. 1 Read: Initialization complete
4	CAN_RAM_INIT	R/W	0h	Initiate CAN Mailbox RAM initialization: 0 Read: Initialization complete or initialization not initiated. Write: No action 1 Read: Initialization is on-going Write: Initiate CAN Mailbox RAM initialization. After initialization, this bit will be automatically cleared to 0.
3	KEY3	R/W	0h	See Key 0
2	KEY2	R/W	1h	See Key 0
1	KEY1	R/W	0h	See Key 0
0	KEY0	R/W	1h	KEY3-KEY0 should be 1010 for any write to this register to be valid. These bits will be restored to their reset state after the CAN RAM initialization is complete.

20.15.2.10 CAN_GLB_INT_EN Register (offset = 50h) [reset = 0h]

CAN_GLB_INT_EN is shown in [Figure 20-27](#) and described in [Table 20-15](#).

CAN Global Interrupt Enable Register

Figure 20-27. CAN_GLB_INT_EN Register

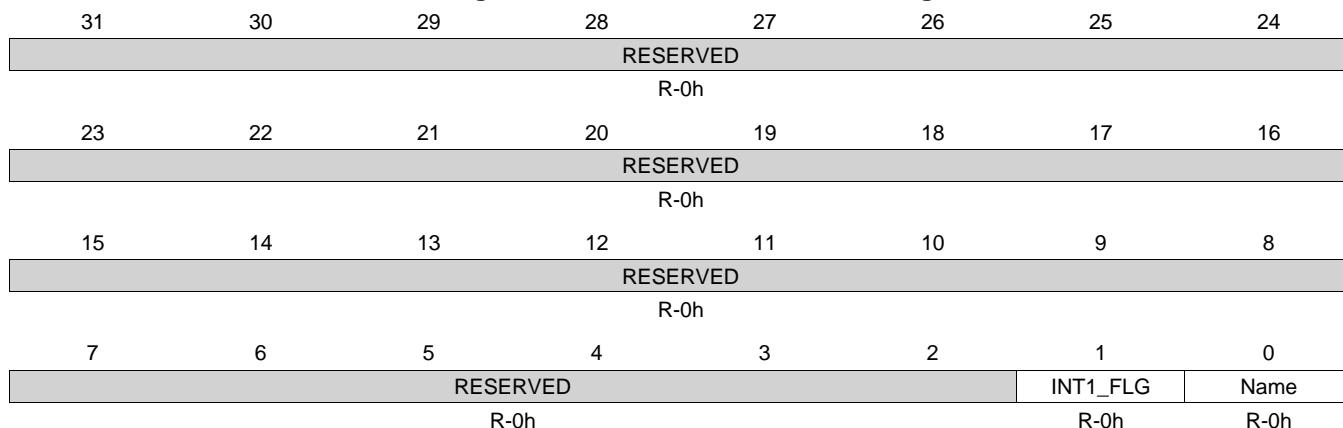
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-15. CAN_GLB_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	GLBINT1_EN	R/W	0h	Global Interrupt Enable for CAN INT1 0 = CAN INT1 does not generate interrupt to PIE 1= CAN INT1 generates interrupt to PIE if interrupt condition occurs
0	GLBINT0_EN	R/W	0h	Global Interrupt Enable for CAN INT0 0 = CAN INT0 does not generate interrupt to PIE 1= CAN INT0 generates interrupt to PIE if interrupt condition occurs

20.15.2.11 CAN_GLB_INT_FLG Register (offset = 54h) [reset = 0h]CAN_GLB_INT_FLG is shown in [Figure 20-28](#) and described in [Table 20-16](#).

CAN Global Interrupt Flag Register

Figure 20-28. CAN_GLB_INT_FLG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

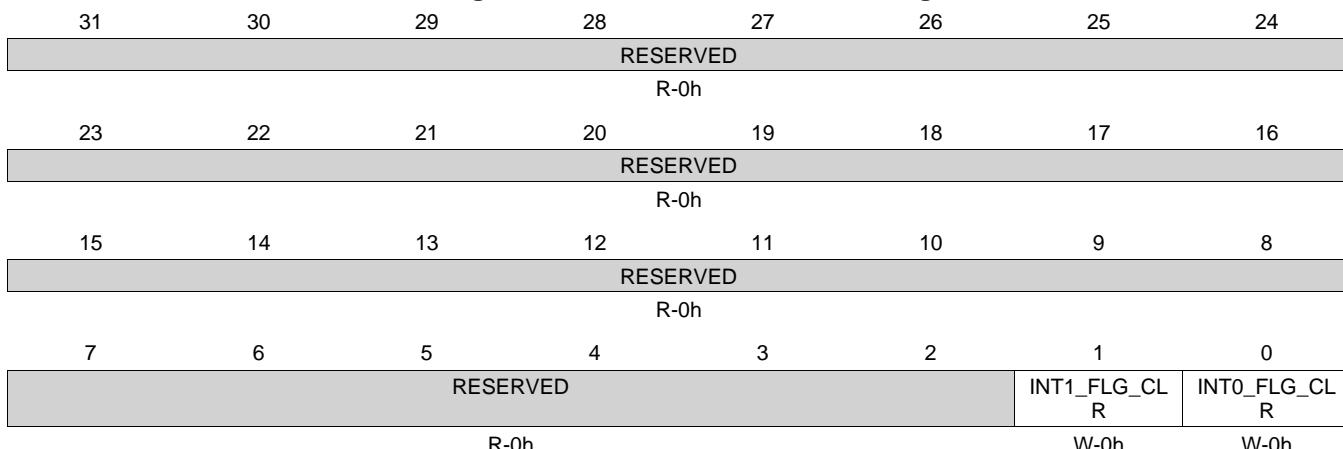
Table 20-16. CAN_GLB_INT_FLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	INT1_FLG	R	0h	Global Interrupt Flag for CAN INT1 0 = No interrupt generated 1= Interrupt is generated due to CAN INT1 (refer to CAN Interrupt Status Register for the condition)
0	Name	R	0h	Global Interrupt Flag for CAN INT0 0 = No interrupt generated 1= Interrupt is generated due to CAN INT0 (refer to CAN Interrupt Status Register for the condition)

20.15.2.12 CAN_GLB_INT_CLR Register (offset = 58h) [reset = 0h]

CAN_GLB_INT_CLR is shown in [Figure 20-29](#) and described in [Table 20-17](#).

CAN Global Interrupt Clear Register

Figure 20-29. CAN_GLB_INT_CLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-17. CAN_GLB_INT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	INT1_FLG_CLR	W	0h	Global Interrupt flag clear for CAN INT1 0 = No effect 1= Write '1' to clear the corresponding bit of the Global Interrupt Flag Register
0	INT0_FLG_CLR	W	0h	Global Interrupt flag clear for CAN INT0 0 = No effect 1= Write '1' to clear the corresponding bit of the Global Interrupt Flag Register

20.15.2.13 CAN_ABOTR Register (offset = 80h) [reset = 0h]

CAN_ABOTR is shown in [Figure 20-30](#) and described in [Table 20-18](#).

Auto-Bus-On Time Register

Figure 20-30. CAN_ABOTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABO_Time																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

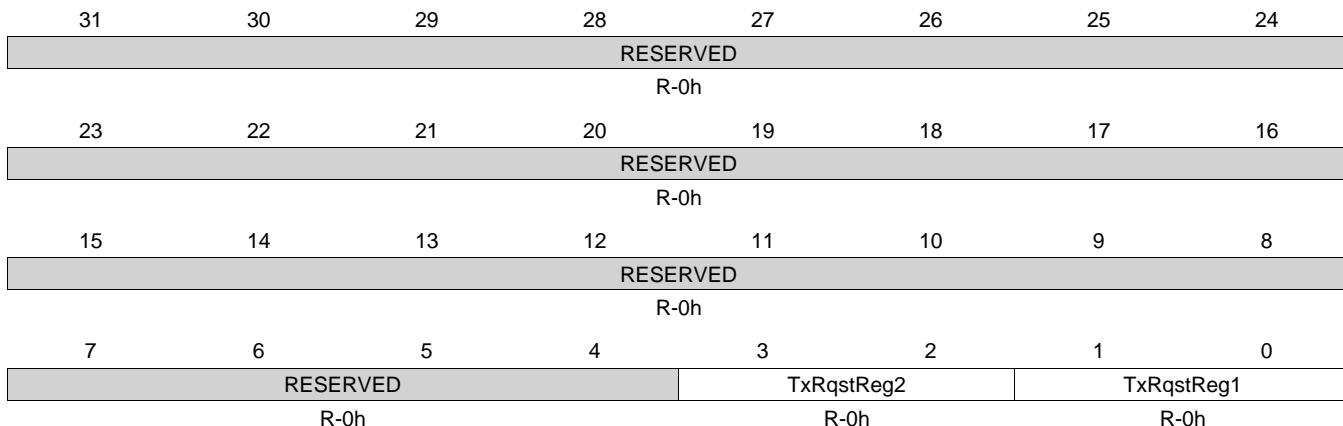
Table 20-18. CAN_ABOTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ABO_Time	R/W	0h	<p>Auto-Bus-On Timer</p> <p>Number of VBUS clock cycles before a Bus-Off recovery sequence is started by clearing the Init bit.</p> <p>This function has to be enabled by setting bit ABO in CAN Control Register.</p> <p>The Auto-Bus-On timer is realized by a 32-bit counter which starts to count down to zero when the module goes Bus-Off. The counter will be reloaded with the preload value of the ABO Time register after this phase.</p> <p>NOTE: On write access to the CAN Control register while Auto-Bus-On timer is running, the Auto-Bus-On procedure will be aborted.</p> <p>NOTE: During Debug mode, running Auto-Bus-On timer will be paused.</p>

20.15.2.14 CAN_TXRQ_X Register (offset = 84h) [reset = 0h]

CAN_TXRQ_X is shown in [Figure 20-31](#) and described in [Table 20-19](#).

CAN Transmission Request X Register

Figure 20-31. CAN_TXRQ_X Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-19. CAN_TXRQ_X Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TxRqstReg2	R	0h	Transmit Request Register 2 flag: Bit 2 represents byte 2 of CAN_TXRQ_21. If one or more bits in that byte are set, then bit 2 will be set. Bit 3 represents byte 3 of CAN_TXRQ_21 Register. If one or more bits in that byte are set, then bit 3 will be set.
1-0	TxRqstReg1	R	0h	Transmit Request Register 1 flag: With these bits, the CPU can detect if one or more bits in the CAN Transmission Request 2_1 Register (CAN_TXRQ_21) is set. Each register bit represents a group of eight mailboxes. If at least one of the TxRqst bits of these message objects are set, the corresponding bit in the Transmission Request X Register will be set. Bit 0 represents byte 0 of CAN_TXRQ_21 Register. If one or more bits in that byte are set, then bit 0 will be set. Bit 1 represents byte 1 of CAN_TXRQ_21 Register. If one or more bits in that byte are set, then bit 1 will be set.

20.15.2.15 CAN_TXRQ_21 Register (offset = 88h) [reset = 0h]CAN_TXRQ_21 is shown in [Figure 20-32](#) and described in [Table 20-20](#).

CAN Transmission Request 2_1 Register

Figure 20-32. CAN_TXRQ_21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxRqst																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

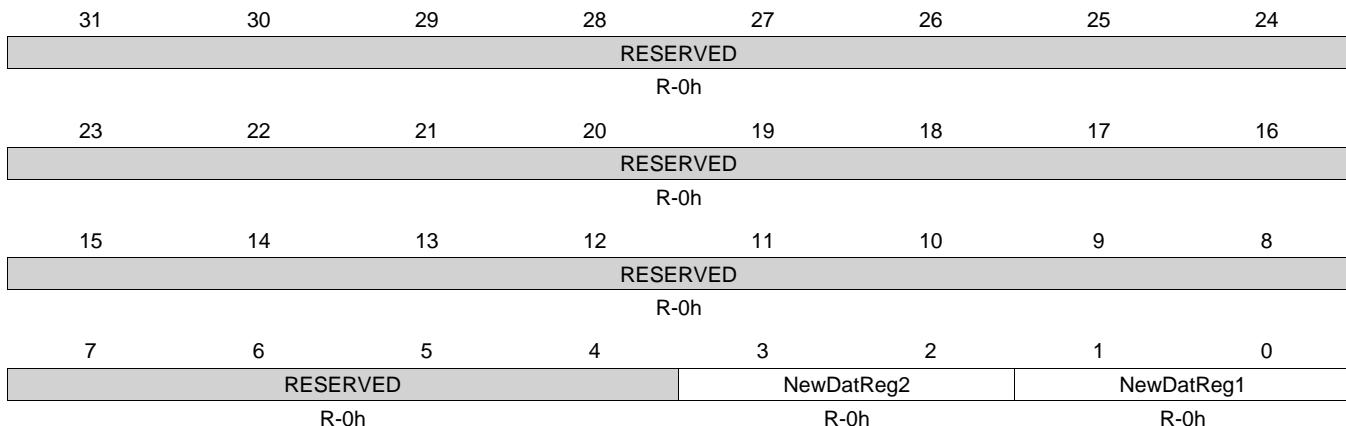
Table 20-20. CAN_TXRQ_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TxRqst	R	0h	Transmission Request Bits (for all message objects) 0 No transmission has been requested for this message object. 1 The transmission of this message object is requested and is not yet done.

20.15.2.16 CAN_NDAT_X Register (offset = 98h) [reset = 0h]

CAN_NDAT_X is shown in [Figure 20-33](#) and described in [Table 20-21](#).

CAN New Data X Register

Figure 20-33. CAN_NDAT_X Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-21. CAN_NDAT_X Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	NewDatReg2	R	0h	<p>New Data Register 2 flag: Bit 2 represents byte 2 of CAN_NDAT _21 Register. If one or more bits in that byte are set, then bit 2 will be set. Bit 3 represents byte 3 of CAN_NDAT _21 Register. If one or more bits in that byte are set, then bit 3 will be set.</p>
1-0	NewDatReg1	R	0h	<p>New Data Register 1 flag: With these bits, the CPU can detect if one or more bits in the CAN New Data 2_1 Register (CAN_NDAT _21) is set. Each register bit represents a group of eight mailboxes. If at least one of the NewDat bits of these mailboxes are set, the corresponding bit in the CAN New Data X Register will be set. Bit 0 represents byte 0 of CAN_NDAT _21 Register. If one or more bits in that byte are set, then bit 0 will be set. Bit 1 represents byte 1 of CAN_NDAT _21 Register. If one or more bits in that byte are set, then bit 1 will be set.</p>

20.15.2.17 CAN_NDAT_21 Register (offset = 9Ch) [reset = 0h]CAN_NDAT_21 is shown in [Figure 20-34](#) and described in [Table 20-22](#).

CAN New Data 2_1 Register

Figure 20-34. CAN_NDAT_21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NewDat																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

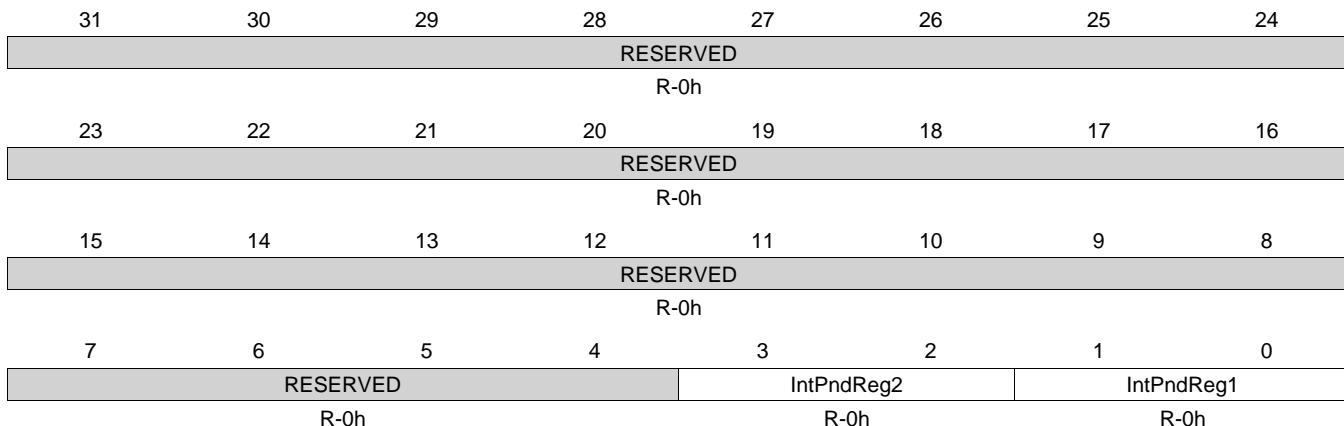
Table 20-22. CAN_NDAT_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NewDat	R	0h	<p>New Data Bits (for all message objects)</p> <p>0 No new data has been written into the data portion of this message object by the message handler since the last time when this flag was cleared by the CPU.</p> <p>1 The message handler or the CPU has written new data into the data portion of this message object.</p>

20.15.2.18 CAN_IPEN_X Register (offset = ACh) [reset = 0h]

CAN_IPEN_X is shown in [Figure 20-35](#) and described in [Table 20-23](#).

CAN Interrupt Pending X Register

Figure 20-35. CAN_IPEN_X Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-23. CAN_IPEN_X Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	IntPndReg2	R	0h	Interrupt Pending Register 2 flag: Bit 2 represents byte 2 of CAN_IPEN_21 Register. If one or more bits in that byte are set, then bit 2 will be set. Bit 3 represents byte 3 of CAN_IPEN_21 Register. If one or more bits in that byte are set, then bit 3 will be set.
1-0	IntPndReg1	R	0h	Interrupt Pending Register 1 flag: With these bits, the CPU can detect if one or more bits in the CAN Interrupt Pending 2_1 Register (CAN_IPEN_21) is set. Each register bit represents a group of eight mailboxes. If at least one of the IntPnd bits of these mailboxes are set, the corresponding bit in the CAN Interrupt Pending X Register will be set. Bit 0 represents byte 0 of CAN_IPEN_21 Register. If one or more bits in that byte are set, then bit 0 will be set. Bit 1 represents byte 1 of CAN_IPEN_21 Register. If one or more bits in that byte are set, then bit 1 will be set.

20.15.2.19 CAN_IPEN_21 Register (offset = B0h) [reset = 0h]

CAN_IPEN_21 is shown in [Figure 20-36](#) and described in [Table 20-24](#).

CAN Interrupt Pending 2_1 Register

Figure 20-36. CAN_IPEN_21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IntPnd																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

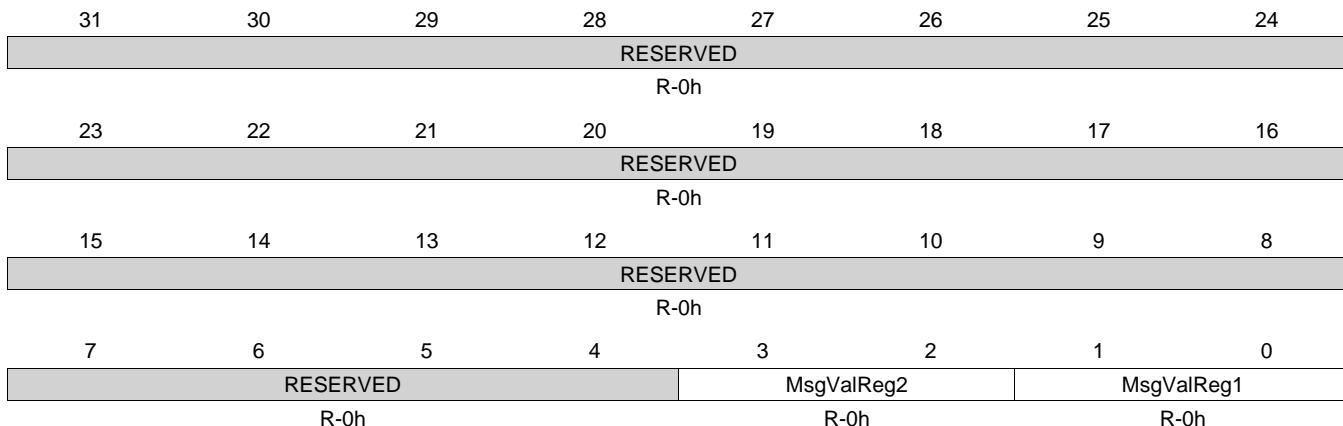
Table 20-24. CAN_IPEN_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IntPnd	R	0h	<p>Interrupt Pending bits: This register contains the bits that indicate the pending interrupts in each one of the 32 mailboxes.</p> <p>0 This mailbox is not the source of an interrupt.</p> <p>1 This mailbox is the source of an interrupt.</p>

20.15.2.20 CAN_MVAL_X Register (offset = C0h) [reset = 0h]

CAN_MVAL_X is shown in [Figure 20-37](#) and described in [Table 20-25](#).

CAN Message Valid X Register

Figure 20-37. CAN_MVAL_X Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-25. CAN_MVAL_X Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	MsgValReg2	R	0h	Message Valid Register 2 flag: Bit 2 represents byte 2 of CAN_MVAL_21 Register. If one or more bits in that byte are set, then bit 2 will be set. Bit 3 represents byte 3 of CAN_MVAL_21 Register. If one or more bits in that byte are set, then bit 3 will be set.
1-0	MsgValReg1	R	0h	Message Valid Register 1 flag: With these bits, the CPU can detect if one or more bits in the CAN Message Valid 2_1 Register (CAN_MVAL_21) is set. Each register bit represents a group of eight mailboxes. If at least one of the MsgVal bits of these mailboxes are set, the corresponding bit in the CAN Message Valid X Register will be set. Bit 0 represents byte 0 of CAN_MVAL_21 Register. If one or more bits in that byte are set, then bit 0 will be set. Bit 1 represents byte 1 of CAN_MVAL_21 Register. If one or more bits in that byte are set, then bit 1 will be set.

20.15.2.21 CAN_MVAL_21 Register (offset = C4h) [reset = 0h]CAN_MVAL_21 is shown in [Figure 20-38](#) and described in [Table 20-26](#).

CAN Message Valid 2_1 Register

Figure 20-38. CAN_MVAL_21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MsgValReg																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-26. CAN_MVAL_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MsgValReg	R	0h	Message Valid Bits (for all message objects) 0 This message object is ignored by the message handler. 1 This message object is configured and will be considered by the message handler.

20.15.2.22 CAN_IP_MUX21 Register (offset = D8h) [reset = 0h]

CAN_IP_MUX21 is shown in [Figure 20-39](#) and described in [Table 20-27](#).

CAN Interrupt Multiplexer 2_1 Register

Figure 20-39. CAN_IP_MUX21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IntMux																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-27. CAN_IP_MUX21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IntMux	R	0h	Interrupt Mux bits: The IntMux flag determines for each mailbox, which of the two interrupt lines (CANn_INT0 or CANn_INT1) will be asserted when the IntPnd of this mailbox is set. 0 CANn_INT0 line is active if corresponding IntPnd flag is one. 1 CANn_INT1 line is active if corresponding IntPnd flag is one.

20.15.2.23 CAN_IF1CMD Register (offset = 100h) [reset = 1h]

CAN_IF1CMD is shown in [Figure 20-40](#) and described in [Table 20-28](#).

IF1 Command Register

Figure 20-40. CAN_IF1CMD Register

31	30	29	28	27	26	25	24	
RESERVED								
R-0h								
23	22	21	20	19	18	17	16	
DIR	Mask	Arb	Control	ClrlntPnd	TXRQST	DATA_A	DATA_B	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8	
Busy	RESERVED		RESERVED					
R-0h	R-0h			R-0h				
7	6	5	4	3	2	1	0	
MSG_NUM								
R/W-1h								

LEGEND: R/W = Read/Write; R = Read only; W1toCI = Write 1 to clear bit; -n = value after reset

Table 20-28. CAN_IF1CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	DIR	R/W	0h	<p>Write/Read</p> <p>0 Direction = Read: Transfer direction is from the message object addressed by Message Number (Bits [7:0]) to the IF1/IF2 Register set.</p> <p>1 Direction = Write: Transfer direction is from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]).</p> <p>Note: This bit is write protected by Busy bit.</p>
22	Mask	R/W	0h	<p>Access Mask Bits</p> <p>0 Mask bits will not be changed</p> <p>1 Direction = Read: The Mask bits (Identifier Mask + MDir + MXtd) will be transferred from the message object addressed by Message Number (Bits [7:0]) to the IF1/IF2 Register set.</p> <p>Direction = Write: The Mask bits (Identifier Mask + MDir + MXtd) will be transferred from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]).</p> <p>Note: This bit is write protected by Busy bit.</p>
21	Arb	R/W	0h	<p>Access Arbitration Bits</p> <p>0 Arbitration bits will not be changed</p> <p>1 Direction = Read: The Arbitration bits (Identifier + Dir + Xtd + MsgVal) will be transferred from the message object addressed by Message Number (Bits [7:0]) to the corresponding IF1/IF2 Register set.</p> <p>Direction = Write: The Arbitration bits (Identifier + Dir + Xtd + MsgVal) will be transferred from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]).</p> <p>Note: This bit is write protected by Busy bit.</p>

Table 20-28. CAN_IF1CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	Control	R/W	0h	<p>Access Control Bits 0 Control bits will not be changed 1 Direction = Read: The Message Control bits will be transferred from the message object addressed by Message Number (Bits [7:0]) to the IF1/IF2 Register set. Direction = Write: The Message Control bits will be transferred from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]). If the TxRqst/NewDat bit in this register (Bit [18]) is set, the TxRqst/ NewDat bit in the IF1/IF2 Message Control Register will be ignored. Note: This bit is write protected by Busy bit.</p>
19	ClrIntPnd	R/W	0h	<p>Clear Interrupt Pending Bit 0 IntPnd bit will not be changed 1 Direction = Read: Clears IntPnd bit in the message object. Direction = Write: This bit is ignored. Copying of IntPnd flag from IF1/IF2 registers to Message RAM can only be controlled by the Control flag (Bit [20]). Note: This bit is write protected by Busy bit.</p>
18	TXRQST	R/W	0h	<p>Access Transmission Request Bit 0 Direction = Read: NewDat bit will not be changed. Direction = Write: TxRqst/NewDat bit will be handled according to the Control bit. 1 Direction = Read: Clears NewDat bit in the message object. Direction = Write: Sets TxRqst/NewDat in message object. Note: If a CAN transmission is requested by setting TxRqst/NewDat in this register, the TxRqst/NewDat bits in the message object will be set to one independent of the values in IF1/IF2 Message Control Register. Note: A read access to a message object can be combined with the reset of the control bits IntPnd and NewDat. The values of these bits transferred to the IF1/IF2 Message Control Register always reflect the status before resetting them. Note: This bit is write protected by Busy bit.</p>
17	DATA_A	R/W	0h	<p>Access Data Bytes 0-3 0 Data Bytes 0-3 will not be changed. 1 Direction = Read: The Data Bytes 0-3 will be transferred from the message object addressed by the Message Number (Bits [7:0]) to the corresponding IF1/IF2 Register set. Direction = Write: The Data Bytes 0-3 will be transferred from the IF1/IF2 Register set to the message object addressed by the Message Number (Bits [7:0]). Note: The duration of the message transfer is independent of the number of bytes to be transferred. Note: This bit is write protected by Busy bit.</p>
16	DATA_B	R/W	0h	<p>Access Data Bytes 4-7 0 Data Bytes 4-7 will not be changed. 1 Direction = Read: The Data Bytes 4-7 will be transferred from the message object addressed by Message Number (Bits [7:0]) to the corresponding IF1/IF2 Register set. Direction = Write: The Data Bytes 4-7 will be transferred from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]). Note: The duration of the message transfer is independent of the number of bytes to be transferred. Note: This bit is write protected by Busy bit.</p>

Table 20-28. CAN_IF1CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	Busy	R	0h	Busy Flag 0 No transfer between IF1/IF2 Register Set and Message RAM is in progress. 1 Transfer between IF1/IF2 Register Set and Message RAM is in progress. This bit is set to one after the message number has been written to bits [7:0]. IF1/IF2 Register Set will be write protected. The bit is cleared after read/write action has been finished.
14	RESERVED	R	0h	Reserved
13-8	RESERVED	R	0h	Reserved
7-0	MSG_NUM	R/W	1h	Number of message object in Message RAM which is used for data transfer 0x00 Invalid message number 0x01-0x80 Valid message numbers 0x81-0xFF Invalid message numbers Note: This bit is write protected by Busy bit.

20.15.2.24 CAN_IF1MSK Register (offset = 104h) [reset = FFFFFFFFh]

CAN_IF1MSK is shown in [Figure 20-41](#) and described in [Table 20-29](#).

IF1 Mask Register

Figure 20-41. CAN_IF1MSK Register

31	30	29	28	27	26	25	24
MXtd	MDir	RESERVED			Msk		
R/W-1h	R/W-1h	R-1h			R/W-1FFFFFFFh		
23	22	21	20	19	18	17	16
				Msk			
				R/W-1FFFFFFFh			
15	14	13	12	11	10	9	8
				Msk			
				R/W-1FFFFFFFh			
7	6	5	4	3	2	1	0
				Msk			
				R/W-1FFFFFFFh			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-29. CAN_IF1MSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MXtd	R/W	1h	<p>Mask Extended Identifier</p> <p>0 The extended identifier bit (IDE) has no effect on the acceptance filtering.</p> <p>1 The extended identifier bit (IDE) is used for acceptance filtering. When 11-bit ("standard") identifiers are used for a message object, the identifiers of received data frames are written into bits ID[28:18]. For acceptance filtering, only these bits together with mask bits Msk[28:18] are considered.</p> <p>Note: This bit is write protected by Busy bit.</p>
30	MDir	R/W	1h	<p>Mask Message Direction</p> <p>0 The message direction bit (Dir) has no effect on the acceptance filtering.</p> <p>1 The message direction bit (Dir) is used for acceptance filtering.</p> <p>Note: This bit is write protected by Busy bit.</p>
29	RESERVED	R	1h	Reserved
28-0	Msk	R/W	1FFFFFFFh	<p>Identifier Mask-</p> <p>0 The corresponding bit in the identifier of the message object is not used for acceptance filtering (don't care).</p> <p>1 The corresponding bit in the identifier of the message object is used for acceptance filtering.</p> <p>Note: This bit is write protected by Busy bit.</p>

20.15.2.25 CAN_IF1ARB Register (offset = 108h) [reset = 0h]

CAN_IF1ARB is shown in [Figure 20-42](#) and described in [Table 20-30](#).

IF1 Arbitration Register

Figure 20-42. CAN_IF1ARB Register

31	30	29	28	27	26	25	24
MsgVal	Xtd	Dir			ID		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		
23	22	21	20	19	18	17	16
				ID			
				R/W-0h			
15	14	13	12	11	10	9	8
				ID			
				R/W-0h			
7	6	5	4	3	2	1	0
				ID			
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-30. CAN_IF1ARB Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MsgVal	R/W	0h	<p>Message Valid</p> <p>0 The message object is ignored by the message handler.</p> <p>1 The message object is to be used by the message handler.</p> <p>The CPU should reset the MsgVal bit of all unused Messages Objects during the initialization before it resets bit Init in the CAN Control Register. This bit must also be reset before the identifier ID[28:0], the control bits Xtd, Dir or DLC[3:0] are modified, or if the messages object is no longer required.</p> <p>Note: This bit is write protected by Busy bit.</p>
30	Xtd	R/W	0h	<p>Extended Identifier</p> <p>0 The 11-bit ("standard") Identifier is used for this message object.</p> <p>1 The 29-bit ("extended") Identifier is used for this message object.</p> <p>Note: This bit is write protected by Busy bit.</p>
29	Dir	R/W	0h	<p>Message Direction</p> <p>0 Direction = receive: On TxRqst, a remote frame with the identifier of this message object is transmitted. On reception of a data frame with matching identifier, that message is stored in this message object.</p> <p>1 Direction = transmit: On TxRqst, the respective message object is transmitted as a data frame. On reception of a remote frame with matching identifier, the TxRqst bit of this message object is set (if RmtEn = one).</p> <p>Note: This bit is write protected by Busy bit.</p>
28-0	ID	R/W	0h	<p>Message Identifier</p> <p>ID[28:0] 29-bit Identifier ("Extended Frame")</p> <p>ID[28:18] 11-bit Identifier ("Standard Frame")</p> <p>Note: This bit is write protected by Busy bit.</p>

20.15.2.26 CAN_IF1MCTL Register (offset = 10Ch) [reset = 0h]

CAN_IF1MCTL is shown in [Figure 20-43](#) and described in [Table 20-31](#).

IF1 Message Control Register

Figure 20-43. CAN_IF1MCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
NewDat	MsgLst	IntPnd	UMask	TxIE	RxE	RmtEn	TxRqst
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EoB	RESERVED				DLC		
R/W-0h	R-0h				R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-31. CAN_IF1MCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NewDat	R/W	0h	<p>New Data</p> <p>0 No new data has been written into the data portion of this message object by the message handler since the last time when this flag was cleared by the CPU.</p> <p>1 The message handler or the CPU has written new data into the data portion of this message object.</p> <p>Note: This bit is write protected by Busy bit.</p>
14	MsgLst	R/W	0h	<p>Message Lost (only valid for message objects with direction = receive)</p> <p>0 No message lost since the last time when this bit was reset by the CPU.</p> <p>1 The message handler stored a new message into this object when NewDat was still set, so the previous message has been overwritten.</p> <p>Note: This bit is write protected by Busy bit.</p>
13	IntPnd	R/W	0h	<p>Interrupt Pending</p> <p>0 This message object is not the source of an interrupt.</p> <p>1 This message object is the source of an interrupt. The Interrupt Identifier in the Interrupt Register will point to this message object if there is no other interrupt source with higher priority.</p> <p>Note: This bit is write protected by Busy bit.</p>
12	UMask	R/W	0h	<p>Use Acceptance Mask</p> <p>0 Mask ignored</p> <p>1 Use Mask (Msk[28:0], MXtd, and MDir) for acceptance filtering</p> <p>If the UMask bit is set to one, the message object's mask bits have to be programmed during initialization of the message object before MsgVal is set to one.</p> <p>Note: This bit is write protected by Busy bit.</p>

Table 20-31. CAN_IF1MCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TxIE	R/W	0h	<p>Transmit Interrupt Enable</p> <p>0 IntPnd will not be triggered after the successful transmission of a frame.</p> <p>1 IntPnd will be triggered after the successful transmission of a frame.</p> <p>Note: This bit is write protected by Busy bit.</p>
10	RxE	R/W	0h	<p>Receive Interrupt Enable</p> <p>0 IntPnd will not be triggered after the successful reception of a frame.</p> <p>1 IntPnd will be triggered after the successful reception of a frame.</p> <p>Note: This bit is write protected by Busy bit.</p>
9	RmtEn	R/W	0h	<p>Remote Enable</p> <p>0 At the reception of a remote frame, TxRqst is not changed.</p> <p>1 At the reception of a remote frame, TxRqst is set.</p> <p>Note: This bit is write protected by Busy bit.</p>
8	TxRqst	R/W	0h	<p>Transmit Request</p> <p>0 This message object is not waiting for a transmission.</p> <p>1 The transmission of this message object is requested and is not yet done.</p> <p>Note: This bit is write protected by Busy bit.</p>
7	EoB	R/W	0h	<p>End of Block</p> <p>0 The message object is part of a FIFO Buffer block and is not the last message object of the FIFO Buffer block.</p> <p>1 The message object is a single message object or the last message object in a FIFO Buffer Block.</p> <p>Note: This bit is used to concatenate multiple message objects to build a FIFO Buffer. For single message objects (not belonging to a FIFO Buffer), this bit must always be set to one.</p> <p>Note: This bit is write protected by Busy bit.</p>
6-4	RESERVED	R	0h	Reserved
3-0	DLC	R/W	0h	<p>Data length code</p> <p>0-8 Data frame has 0-8 data bits.</p> <p>9-15 data frame has 8 data bytes.</p> <p>Note: The data length code of a message object must be defined the same as in all the corresponding objects with the same identifier at other nodes. When the message handler stores a data frame, it will write the DLC to the value given by the received message.</p> <p>Note: This bit is write protected by Busy bit.</p>

20.15.2.27 CAN_IF1DATA Register (offset = 110h) [reset = 0h]

CAN_IF1DATA is shown in [Figure 20-44](#) and described in [Table 20-32](#).

IF1 Data A Register

Figure 20-44. CAN_IF1DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data_3								Data_2								Data_1								Data_0							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-32. CAN_IF1DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Data_3	R/W	0h	Data Byte 3
23-16	Data_2	R/W	0h	Data Byte 2
15-8	Data_1	R/W	0h	Data Byte 1
7-0	Data_0	R/W	0h	Data Byte 0 Note: All bits in this register are write protected by Busy bit.

20.15.2.28 CAN_IF1DATB Register (offset = 114h) [reset = 0h]

CAN_IF1DATB is shown in [Figure 20-45](#) and described in [Table 20-33](#).

IF1 Data B Register

Figure 20-45. CAN_IF1DATB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data_7								Data_6								Data_5								Data_4							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-33. CAN_IF1DATB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Data_7	R/W	0h	Data Byte 7
23-16	Data_6	R/W	0h	Data Byte 6
15-8	Data_5	R/W	0h	Data Byte 5
7-0	Data_4	R/W	0h	Data Byte 4 Note: All bits in this register are write protected by Busy bit.

20.15.2.29 CAN_IF2CMD Register (offset = 120h) [reset = 1h]

CAN_IF2CMD is shown in [Figure 20-46](#) and described in [Table 20-34](#).

IF2 Command Register

Figure 20-46. CAN_IF2CMD Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
DIR	Mask	Arb	Control	ClrIntPnd	TxRqst	DATA_A	DATA_B
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
Busy	RESERVED	RESERVED					
R-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
MSG_NUM							
R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-34. CAN_IF2CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	DIR	R/W	0h	<p>Write/Read</p> <p>0 Direction = Read: Transfer direction is from the message object addressed by Message Number (Bits [7:0]) to the IF1/IF2 Register set.</p> <p>1 Direction = Write: Transfer direction is from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]).</p> <p>Note: This bit is write protected by Busy bit.</p>
22	Mask	R/W	0h	<p>Access Mask Bits</p> <p>0 Mask bits will not be changed</p> <p>1 Direction = Read: The Mask bits (Identifier Mask + MDir + MXtd) will be transferred from the message object addressed by Message Number (Bits [7:0]) to the IF1/IF2 Register set.</p> <p>Direction = Write: The Mask bits (Identifier Mask + MDir + MXtd) will be transferred from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]).</p> <p>Note: This bit is write protected by Busy bit.</p>
21	Arb	R/W	0h	<p>Access Arbitration Bits</p> <p>0 Arbitration bits will not be changed</p> <p>1 Direction = Read: The Arbitration bits (Identifier + Dir + Xtd + MsgVal) will be transferred from the message object addressed by Message Number (Bits [7:0]) to the corresponding IF1/IF2 Register set.</p> <p>Direction = Write: The Arbitration bits (Identifier + Dir + Xtd + MsgVal) will be transferred from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]).</p> <p>Note: This bit is write protected by Busy bit.</p>

Table 20-34. CAN_IF2CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	Control	R/W	0h	<p>Access Control Bits 0 Control bits will not be changed 1 Direction = Read: The Message Control bits will be transferred from the message object addressed by Message Number (Bits [7:0]) to the IF1/IF2 Register set. Direction = Write: The Message Control bits will be transferred from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]). If the TxRqst/NewDat bit in this register (Bit [18]) is set, the TxRqst/ NewDat bit in the IF1/IF2 Message Control Register will be ignored. Note: This bit is write protected by Busy bit.</p>
19	ClrIntPnd	R/W	0h	<p>Clear Interrupt Pending Bit 0 IntPnd bit will not be changed 1 Direction = Read: Clears IntPnd bit in the message object. Direction = Write: This bit is ignored. Copying of IntPnd flag from IF1/IF2 registers to Message RAM can only be controlled by the Control flag (Bit [20]). Note: This bit is write protected by Busy bit.</p>
18	TxRqst	R/W	0h	<p>Access Transmission Request Bit 0 Direction = Read: NewDat bit will not be changed. Direction = Write: TxRqst/NewDat bit will be handled according to the Control bit. 1 Direction = Read: Clears NewDat bit in the message object. Direction = Write: Sets TxRqst/NewDat in message object. Note: If a CAN transmission is requested by setting TxRqst/NewDat in this register, the TxRqst/NewDat bits in the message object will be set to one independent of the values in IF1/IF2 Message Control Register. Note: A read access to a message object can be combined with the reset of the control bits IntPnd and NewDat. The values of these bits transferred to the IF1/IF2 Message Control Register always reflect the status before resetting them. Note: This bit is write protected by Busy bit.</p>
17	DATA_A	R/W	0h	<p>Access Data Bytes 0-3 0 Data Bytes 0-3 will not be changed. 1 Direction = Read: The Data Bytes 0-3 will be transferred from the message object addressed by the Message Number (Bits [7:0]) to the corresponding IF1/IF2 Register set. Direction = Write: The Data Bytes 0-3 will be transferred from the IF1/IF2 Register set to the message object addressed by the Message Number (Bits [7:0]). Note: The duration of the message transfer is independent of the number of bytes to be transferred. Note: This bit is write protected by Busy bit.</p>
16	DATA_B	R/W	0h	<p>Access Data Bytes 4-7 0 Data Bytes 4-7 will not be changed. 1 Direction = Read: The Data Bytes 4-7 will be transferred from the message object addressed by Message Number (Bits [7:0]) to the corresponding IF1/IF2 Register set. Direction = Write: The Data Bytes 4-7 will be transferred from the IF1/IF2 Register set to the message object addressed by Message Number (Bits [7:0]). Note: The duration of the message transfer is independent of the number of bytes to be transferred. Note: This bit is write protected by Busy bit.</p>

Table 20-34. CAN_IF2CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	Busy	R	0h	Busy Flag 0 No transfer between IF1/IF2 Register Set and Message RAM is in progress. 1 Transfer between IF1/IF2 Register Set and Message RAM is in progress. This bit is set to one after the message number has been written to bits [7:0]. IF1/IF2 Register Set will be write protected. The bit is cleared after read/write action has been finished.
14	RESERVED	R	0h	Reserved
13-8	RESERVED	R	0h	Reserved
7-0	MSG_NUM	R/W	1h	Number of message object in Message RAM which is used for data transfer 0x00 Invalid message number 0x01-0x80 Valid message numbers 0x81-0xFF Invalid message numbers

20.15.2.30 CAN_IF2MSK Register (offset = 124h) [reset = FFFFFFFFh]

CAN_IF2MSK is shown in [Figure 20-47](#) and described in [Table 20-35](#).

IF2 Mask Register

Figure 20-47. CAN_IF2MSK Register

31	30	29	28	27	26	25	24
MXtd	MDir	RESERVED			Msk		
R/W-1h	R/W-1h	R-1h			R/W-1FFFFFFFh		
23	22	21	20	19	18	17	16
				Msk			
				R/W-1FFFFFFFh			
15	14	13	12	11	10	9	8
				Msk			
				R/W-1FFFFFFFh			
7	6	5	4	3	2	1	0
				Msk			
				R/W-1FFFFFFFh			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-35. CAN_IF2MSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MXtd	R/W	1h	<p>Mask Extended Identifier</p> <p>0 The extended identifier bit (IDE) has no effect on the acceptance filtering.</p> <p>1 The extended identifier bit (IDE) is used for acceptance filtering. When 11-bit ("standard") identifiers are used for a message object, the identifiers of received data frames are written into bits ID[28:18]. For acceptance filtering, only these bits together with mask bits Msk[28:18] are considered.</p> <p>Note: This bit is write protected by Busy bit.</p>
30	MDir	R/W	1h	<p>Mask Message Direction</p> <p>0 The message direction bit (Dir) has no effect on the acceptance filtering.</p> <p>1 The message direction bit (Dir) is used for acceptance filtering.</p> <p>Note: This bit is write protected by Busy bit.</p>
29	RESERVED	R	1h	Reserved
28-0	Msk	R/W	1FFFFFFFh	<p>Identifier Mask-</p> <p>0 The corresponding bit in the identifier of the message object is not used for acceptance filtering (don't care).</p> <p>1 The corresponding bit in the identifier of the message object is used for acceptance filtering.</p> <p>Note: This bit is write protected by Busy bit.</p>

20.15.2.31 CAN_IF2ARB Register (offset = 128h) [reset = 0h]

CAN_IF2ARB is shown in [Figure 20-48](#) and described in [Table 20-36](#).

IF2 Arbitration Register

Figure 20-48. CAN_IF2ARB Register

31	30	29	28	27	26	25	24
MsgVal	Xtd	Dir			ID		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		
23	22	21	20	19	18	17	16
				ID			
				R/W-0h			
15	14	13	12	11	10	9	8
				ID			
				R/W-0h			
7	6	5	4	3	2	1	0
				ID			
				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-36. CAN_IF2ARB Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MsgVal	R/W	0h	<p>Message Valid</p> <p>0 The message object is ignored by the message handler.</p> <p>1 The message object is to be used by the message handler.</p> <p>The CPU should reset the MsgVal bit of all unused Messages Objects during the initialization before it resets bit Init in the CAN Control Register. This bit must also be reset before the identifier ID[28:0], the control bits Xtd, Dir or DLC[3:0] are modified, or if the messages object is no longer required.</p> <p>Note: This bit is write protected by Busy bit.</p>
30	Xtd	R/W	0h	<p>Extended Identifier</p> <p>0 The 11-bit ("standard") Identifier is used for this message object.</p> <p>1 The 29-bit ("extended") Identifier is used for this message object.</p> <p>Note: This bit is write protected by Busy bit.</p>
29	Dir	R/W	0h	<p>Message Direction</p> <p>0 Direction = receive: On TxRqst, a remote frame with the identifier of this message object is transmitted. On reception of a data frame with matching identifier, that message is stored in this message object.</p> <p>1 Direction = transmit: On TxRqst, the respective message object is transmitted as a data frame. On reception of a remote frame with matching identifier, the TxRqst bit of this message object is set (if RmtEn = one).</p> <p>Note: This bit is write protected by Busy bit.</p>
28-0	ID	R/W	0h	<p>Message Identifier</p> <p>ID[28:0] 29-bit Identifier ("Extended Frame")</p> <p>ID[28:18] 11-bit Identifier ("Standard Frame")</p> <p>Note: This bit is write protected by Busy bit.</p>

20.15.2.32 CAN_IF2MCTL Register (offset = 12Ch) [reset = 0h]

CAN_IF2MCTL is shown in [Figure 20-49](#) and described in [Table 20-37](#).

IF2 Message Control Register

Figure 20-49. CAN_IF2MCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
NewDat	MsgLst	IntPnd	UMask	TxIE	RxE	RmtEn	TxRqst
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EoB	RESERVED				DLC		
R/W-0h	R-0h				R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-37. CAN_IF2MCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NewDat	R/W	0h	<p>New Data</p> <p>0 No new data has been written into the data portion of this message object by the message handler since the last time when this flag was cleared by the CPU.</p> <p>1 The message handler or the CPU has written new data into the data portion of this message object.</p> <p>Note: This bit is write protected by Busy bit.</p>
14	MsgLst	R/W	0h	<p>Message Lost (only valid for message objects with direction = receive)</p> <p>0 No message lost since the last time when this bit was reset by the CPU.</p> <p>1 The message handler stored a new message into this object when NewDat was still set, so the previous message has been overwritten.</p> <p>Note: This bit is write protected by Busy bit.</p>
13	IntPnd	R/W	0h	<p>Interrupt Pending</p> <p>0 This message object is not the source of an interrupt.</p> <p>1 This message object is the source of an interrupt. The Interrupt Identifier in the Interrupt Register will point to this message object if there is no other interrupt source with higher priority.</p> <p>Note: This bit is write protected by Busy bit.</p>
12	UMask	R/W	0h	<p>Use Acceptance Mask</p> <p>0 Mask ignored</p> <p>1 Use Mask (Msk[28:0], MXtd, and MDir) for acceptance filtering</p> <p>If the UMask bit is set to one, the message object's mask bits have to be programmed during initialization of the message object before MsgVal is set to one.</p> <p>Note: This bit is write protected by Busy bit.</p>

Table 20-37. CAN_IF2MCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TxIE	R/W	0h	<p>Transmit Interrupt Enable</p> <p>0 IntPnd will not be triggered after the successful transmission of a frame.</p> <p>1 IntPnd will be triggered after the successful transmission of a frame.</p> <p>Note: This bit is write protected by Busy bit.</p>
10	RxE	R/W	0h	<p>Receive Interrupt Enable</p> <p>0 IntPnd will not be triggered after the successful reception of a frame.</p> <p>1 IntPnd will be triggered after the successful reception of a frame.</p> <p>Note: This bit is write protected by Busy bit.</p>
9	RmtEn	R/W	0h	<p>Remote Enable</p> <p>0 At the reception of a remote frame, TxRqst is not changed.</p> <p>1 At the reception of a remote frame, TxRqst is set.</p> <p>Note: This bit is write protected by Busy bit.</p>
8	TxRqst	R/W	0h	<p>Transmit Request</p> <p>0 This message object is not waiting for a transmission.</p> <p>1 The transmission of this message object is requested and is not yet done.</p> <p>Note: This bit is write protected by Busy bit.</p>
7	EoB	R/W	0h	<p>End of Block</p> <p>0 The message object is part of a FIFO Buffer block and is not the last message object of the FIFO Buffer block.</p> <p>1 The message object is a single message object or the last message object in a FIFO Buffer Block.</p> <p>Note: This bit is used to concatenate multiple message objects to build a FIFO Buffer. For single message objects (not belonging to a FIFO Buffer), this bit must always be set to one.</p> <p>Note: This bit is write protected by Busy bit.</p>
6-4	RESERVED	R	0h	Reserved
3-0	DLC	R/W	0h	<p>Data length code</p> <p>0-8 Data frame has 0-8 data bits.</p> <p>9-15 data frame has 8 data bytes.</p> <p>Note: The data length code of a message object must be defined the same as in all the corresponding objects with the same identifier at other nodes. When the message handler stores a data frame, it will write the DLC to the value given by the received message.</p> <p>Note: This bit is write protected by Busy bit.</p>

20.15.2.33 CAN_IF2DATA Register (offset = 130h) [reset = 0h]CAN_IF2DATA is shown in [Figure 20-50](#) and described in [Table 20-38](#).

IF2 Data A Register

Figure 20-50. CAN_IF2DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data_3								Data_2								Data_1								Data_0							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-38. CAN_IF2DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Data_3	R/W	0h	Data Byte 3
23-16	Data_2	R/W	0h	Data Byte 2
15-8	Data_1	R/W	0h	Data Byte 1
7-0	Data_0	R/W	0h	Data Byte 0 Note: All bits in this register are write protected by Busy bit.

20.15.2.34 CAN_IF2DATB Register (offset = 134h) [reset = 0h]

CAN_IF2DATB is shown in [Figure 20-51](#) and described in [Table 20-39](#).

IF2 Data B Register

Figure 20-51. CAN_IF2DATB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data_7								Data_6								Data_5								Data_4							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-39. CAN_IF2DATB Register Field Descriptions

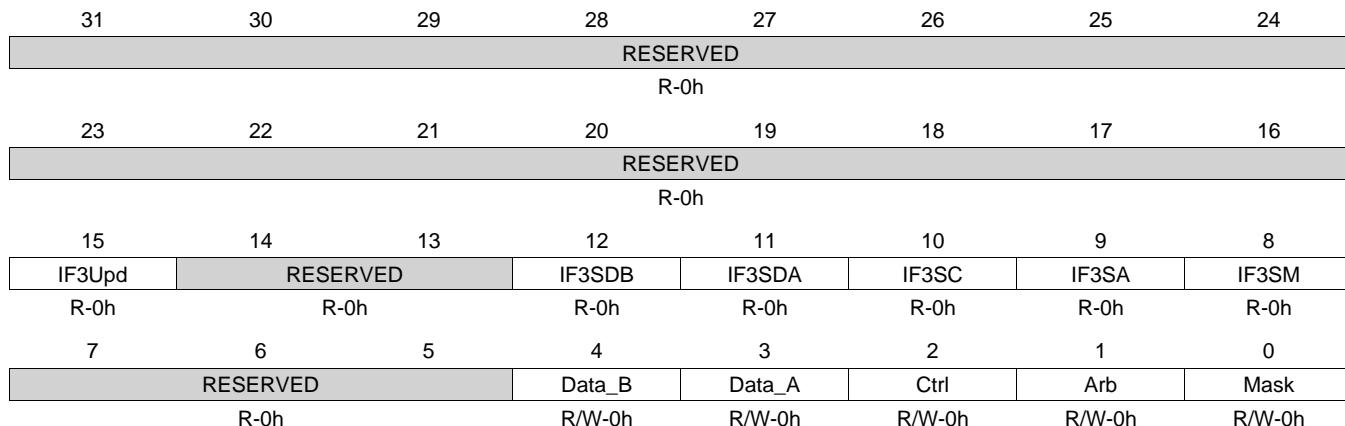
Bit	Field	Type	Reset	Description
31-24	Data_7	R/W	0h	Data Byte 7
23-16	Data_6	R/W	0h	Data Byte 6
15-8	Data_5	R/W	0h	Data Byte 5
7-0	Data_4	R/W	0h	Data Byte 4 Note: All bits in this register are write protected by Busy bit.

20.15.2.35 CAN_IF3OBS Register (offset = 140h) [reset = 0h]

CAN_IF3OBS is shown in [Figure 20-52](#) and described in [Table 20-40](#).

IF3 Observation Register

Figure 20-52. CAN_IF3OBS Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-40. CAN_IF3OBS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	IF3Upd	R	0h	IF3 Update Data 0 No new data has been loaded since last IF3 read. 1 New data has been loaded since last IF3 read.
14-13	RESERVED	R	0h	Reserved
12	IF3SDB	R	0h	IF3 Status of Data B read access 0 All Data B bytes are already read out, or are not marked to be read. 1 Data B section has still data to be read out.
11	IF3SDA	R	0h	IF3 Status of Data A read access 0 All Data A bytes are already read out, or are not marked to be read. 1 Data A section has still data to be read out.
10	IF3SC	R	0h	IF3 Status of Control bits read access 0 All Control section bytes are already read out, or are not marked to be read. 1 Control section has still data to be read out.
9	IF3SA	R	0h	IF3 Status of Arbitration data read access 0 All Arbitration data bytes are already read out, or are not marked to be read. 1 Arbitration section has still data to be read out.
8	IF3SM	R	0h	IF3 Status of Mask data read access 0 All Mask data bytes are already read out, or are not marked to be read. 1 Mask section has still data to be read out.
7-5	RESERVED	R	0h	Reserved

Table 20-40. CAN_IF3OBS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	Data_B	R/W	0h	Data B read observation 0 Data B section has not to be read. 1 Data B section has to be read to enable next IF3 update.
3	Data_A	R/W	0h	Data A read observation 0 Data A section has not to be read. 1 Data A section has to be read to enable next IF3 update.
2	Ctrl	R/W	0h	Ctrl read observation 0 Ctrl section has not to be read. 1 Ctrl section has to be read to enable next IF3 update.
1	Arb	R/W	0h	Arbitration data read observation 0 Arbitration data has not to be read. 1 Arbitration data has to be read to enable next IF3 update.
0	Mask	R/W	0h	Mask data read observation 0 Mask data has not to be read. 1 Mask data has to be read to enable next IF3 update.

20.15.2.36 CAN_IF3MSK Register (offset = 144h) [reset = FFFFFFFFh]

CAN_IF3MSK is shown in [Figure 20-53](#) and described in [Table 20-41](#).

IF3 Mask Register

Figure 20-53. CAN_IF3MSK Register

31	30	29	28	27	26	25	24
MXtd	MDir	RESERVED			Msk		
R-1h	R-1h	R-1h			R-1FFFFFFFh		
23	22	21	20	19	18	17	16
				Msk			
				R-1FFFFFFFh			
15	14	13	12	11	10	9	8
				Msk			
				R-1FFFFFFFh			
7	6	5	4	3	2	1	0
				Msk			
				R-1FFFFFFFh			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-41. CAN_IF3MSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MXtd	R	1h	Mask Extended Identifier 0 The extended identifier bit (IDE) has no effect on the acceptance filtering. 1 The extended identifier bit (IDE) is used for acceptance filtering. Note: When 11-bit ("standard") identifiers are used for a message object, the identifiers of received data frames are written into bits ID[28:18]. For acceptance filtering, only these bits together with mask bits Msk[28:18] are considered.
30	MDir	R	1h	Mask Message Direction 0 The message direction bit (Dir) has no effect on the acceptance filtering. 1 The message direction bit (Dir) is used for acceptance filtering.
29	RESERVED	R	1h	Reserved
28-0	Msk	R	1FFFFFFFh	Identifier Mask Identifier Mask 0 The corresponding bit in the identifier of the message object is not used for acceptance filtering (don't care). 1 The corresponding bit in the identifier of the message object is used for acceptance filtering. Identifier Mask

20.15.2.37 CAN_IF3ARB Register (offset = 148h) [reset = 0h]

CAN_IF3ARB is shown in [Figure 20-54](#) and described in [Table 20-42](#).

IF3 Arbitration Register

Figure 20-54. CAN_IF3ARB Register

31	30	29	28	27	26	25	24
MsgVal	Xtd	Dir			ID		
R-0h	R-0h	R-0h			R-0h		
23	22	21	20	19	18	17	16
				ID			
				R-0h			
15	14	13	12	11	10	9	8
				ID			
				R-0h			
7	6	5	4	3	2	1	0
				ID			
				R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-42. CAN_IF3ARB Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MsgVal	R	0h	Message Valid 0 The message object is ignored by the message handler. 1 The message object is to be used by the message handler. The CPU should reset the MsgVal bit of all unused Messages Objects during the initialization before it resets bit Init in the CAN Control Register. This bit must also be reset before the identifier ID[28:0], the control bits Xtd, Dir or DLC[3:0] are modified, or if the messages object is no longer required.
30	Xtd	R	0h	Extended Identifier 0 The 11-bit ("standard") Identifier is used for this message object. 1 The 29-bit ("extended") Identifier is used for this message object.
29	Dir	R	0h	Message Direction 0 Direction = receive: On TxRqst, a remote frame with the identifier of this message object is transmitted. On reception of a data frame with matching identifier, that message is stored in this message object. 1 Direction = transmit: On TxRqst, the respective message object is transmitted as a data frame. On reception of a remote frame with matching identifier, the TxRqst bit of this message object is set (if RmtEn = one).
28-0	ID	R	0h	Message Identifier ID[28:0] 29-bit Identifier ("Extended Frame") ID[28:18] 11-bit Identifier ("Standard Frame")

20.15.2.38 CAN_IF3MCTL Register (offset = 14Ch) [reset = 0h]

CAN_IF3MCTL is shown in [Figure 20-55](#) and described in [Table 20-43](#).

IF3 Message Control Register

Figure 20-55. CAN_IF3MCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
NewDat	MsgLst	IntPnd	UMask	TxIE	RxE	RmtEn	TxRqst
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
EoB	RESERVED			DLC			
R-0h	R-0h			R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-43. CAN_IF3MCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NewDat	R	0h	<p>New Data</p> <p>0 No new data has been written into the data portion of this message object by the message handler since the last time when this flag was cleared by the CPU.</p> <p>1 The message handler or the CPU has written new data into the data portion of this message object.</p>
14	MsgLst	R	0h	<p>Message Lost (only valid for message objects with direction = receive)</p> <p>0 No message lost since the last time when this bit was reset by the CPU.</p> <p>1 The message handler stored a new message into this object when NewDat was still set, so the previous message has been overwritten.</p>
13	IntPnd	R	0h	<p>Interrupt Pending</p> <p>0 This message object is not the source of an interrupt.</p> <p>1 This message object is the source of an interrupt. The Interrupt Identifier in the Interrupt Register will point to this message object if there is no other interrupt source with higher priority.</p>
12	UMask	R	0h	<p>Use Acceptance Mask</p> <p>0 Mask ignored</p> <p>1 Use Mask (Msk[28:0], MXtd, and MDir) for acceptance filtering</p> <p>If the UMask bit is set to one, the message object's mask bits have to be programmed during initialization of the message object before MsgVal is set to one.</p>
11	TxIE	R	0h	<p>Transmit Interrupt Enable</p> <p>0 IntPnd will not be triggered after the successful transmission of a frame.</p> <p>1 IntPnd will be triggered after the successful transmission of a frame.</p>
10	RxE	R	0h	<p>Receive Interrupt Enable</p> <p>0 IntPnd will not be triggered after the successful reception of a frame.</p> <p>1 IntPnd will be triggered after the successful reception of a frame.</p>

Table 20-43. CAN_IF3MCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RmtEn	R	0h	Remote Enable 0 At the reception of a remote frame, TxRqst is not changed. 1 At the reception of a remote frame, TxRqst is set.
8	TxRqst	R	0h	Transmit Request 0 This message object is not waiting for a transmission. 1 The transmission of this message object is requested and is not yet done.
7	EoB	R	0h	End of Block 0 The message object is part of a FIFO Buffer block and is not the last message object of the FIFO Buffer block. 1 The message object is a single message object or the last message object in a FIFO Buffer Block. Note: This bit is used to concatenate multiple message objects to build a FIFO Buffer. For single message objects (not belonging to a FIFO Buffer), this bit must always be set to one.
6-4	RESERVED	R	0h	Reserved
3-0	DLC	R	0h	Data length code 0-8 Data frame has 0-8 data bits. 9-15 data frame has 8 data bytes. Note: The data length code of a message object must be defined the same as in all the corresponding objects with the same identifier at other nodes. When the message handler stores a data frame, it will write the DLC to the value given by the received message.

20.15.2.39 CAN_IF3DATA Register (offset = 150h) [reset = 0h]

CAN_IF3DATA is shown in [Figure 20-56](#) and described in [Table 20-44](#).

IF3 Data A Register

Figure 20-56. CAN_IF3DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data_3								Data_2								Data_1								Data_0							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-44. CAN_IF3DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Data_3	R	0h	Data Byte 3
23-16	Data_2	R	0h	Data Byte 2
15-8	Data_1	R	0h	Data Byte 1
7-0	Data_0	R	0h	Data Byte 0

20.15.2.40 CAN_IF3DATB Register (offset = 154h) [reset = 0h]

CAN_IF3DATB is shown in [Figure 20-57](#) and described in [Table 20-45](#).

IF3 Data B Register

Figure 20-57. CAN_IF3DATB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data_7								Data_6								Data_5								Data_4							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-45. CAN_IF3DATB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Data_7	R	0h	Data Byte 7
23-16	Data_6	R	0h	Data Byte 6
15-8	Data_5	R	0h	Data Byte 5
7-0	Data_4	R	0h	Data Byte 4

20.15.2.41 CAN_IF3UPD Register (offset = 160h) [reset = 0h]

CAN_IF3UPD is shown in [Figure 20-58](#) and described in [Table 20-46](#).

IF3 Update Enable Register

Figure 20-58. CAN_IF3UPD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF3UpdEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 20-46. CAN_IF3UPD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IF3UpdEn	R/W	0h	IF3 Update Enabled (for all message objects) 0 Automatic IF3 update is disabled for this message object. 1 Automatic IF3 update is enabled for this message object. A message object is scheduled to be copied to IF3 register set, if NewDat flag of the message object is active.

Universal Serial Bus (USB) Controller

This chapter discusses the features and functions of the universal serial bus (USB) controller.

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21.4 Initialization and Configuration	2186
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21.1 Introduction

The USB controller operates as a full-speed function controller during point-to-point communications with the USB host. The controller complies with the USB 2.0 standard, which includes SUSPEND and RESUME signaling. It has thirty-two endpoints, sixteen for IN transactions and sixteen for OUT transactions. One IN and one OUT endpoint are fixed-function endpoints used for control transfers; the others are defined by firmware. A dynamically sizeable FIFO supports queuing multiple packets. DMA access to the FIFO allows data transfer with minimal interference to system software. Software-controlled connect and disconnect allow flexibility during USB device startup.

21.2 Features

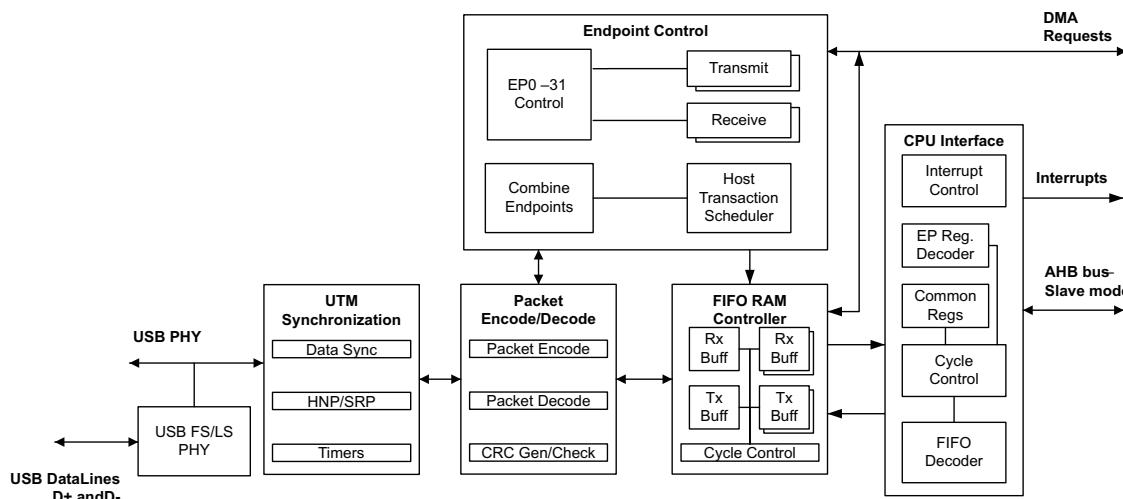
The USB module has the following features:

- Complies with USB-IF certification standards
- USB 2.0 full-speed (12 Mbps) operation in host and device modes as well as low-speed (1.5 Mbps) operation in host mode
- Integrated PHY
- Four transfer types: Control, Interrupt, Bulk, and Isochronous
- Thirty-two endpoints
 - One dedicated control IN endpoint and one dedicated control OUT endpoint
 - Fifteen configurable IN endpoints and fifteen configurable OUT endpoints
- Four KB dedicated endpoint memory: one endpoint may be defined for double-buffered 1023-byte isochronous packet size
- Efficient transfers using direct memory access controller (DMA)
 - Separate channels for transmit and receive for up to three IN endpoints and three OUT endpoints
 - Channel requests asserted when FIFO contains the required amount of data

21.2.1 Block Diagram

The USB block diagram is shown in the figure below.

Figure 21-1. USB Block Diagram



21.2.2 Signal Description

The USB controller requires a total of three signals (D+, D-, and VBus) to operate in device mode and two signals (D+, D-) to operate in embedded host mode. Because of the differential signaling needed for USB, the pins D+ and D- have special buffers to support USB. As such, their position on the chip is not user-selectable. These pins at reset are, by default, GPIOs. They must be configured before being used as USB function pins. Bits 10 and 11 in the GPIO B Analog Mode Select register (GPBAMSEL) should be set to choose the USB function. The signals USB bus voltage (VBus), External power enable (EPEN), and Power fault (PFLT) are not hardwired to any pin and some applications will require they be implemented in software via a GPIO. Software that implements these signals is available in the USB software library.

21.2.3 VBus Recommendations

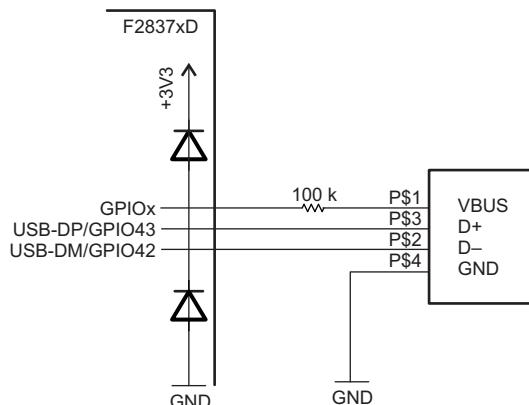
Most applications do not have a need to monitor VBus, and because of this, a dedicated VBus monitoring pin was not included on this processor. If you are designing a bus-powered device application or an embedded host application, you do NOT need to monitor VBus. If you are designing a self-powered device, you will however, need to actively monitor the state of the VBus pin in order to ensure compliance with the USB specification. In Section 7.1.5 and Section 7.2.1 of the USB Specification Revision 2.0™ it is stated respectively that:

- "The voltage source on the [speed identification] pull-up resistor must be derived from or controlled by the power supplied on the USB cable such that when VBUS is removed, the pull-up resistor does not supply current on the data line to which it is attached."
- When VBUS is removed, the device must remove power from the D+/D- pull-up resistor within 10 seconds.
- Later in the timing tables (Section 7.3.2) of the USB Specification 2.0 it is also stated that the D+/D- pull-up resistor should be applied within 100ms of VBus reaching a valid level."

Meeting the above specification is very easy because of the slow timing requirements. In this chapter we will discuss the hardware part of the VBus monitoring solution. The corresponding software will be discussed briefly, but for examples and an explanation the user should consult the USB software guide.

The pins of this microprocessor are NOT 5V tolerant, and because of this the VBus signal cannot be directly connected to a pin. Directly connecting 5V to a pin of the microcontroller WILL destroy the pin and possibly more of the chip. The most cost effective way of making any pin capable of reading a 5V input is to use a series resistance in conjunction with the ESD diode clamps already present inside the device on every pin. We recommend the use of a 100k series resistance between the VBus signal and the pin chosen to monitor it. A diagram of this setup is shown below.

Figure 21-2. USB Scheme



In the above diagram, if VBus is above or below 3.3V and 0V respectively, one of the ESD clamp diodes will be forward-biased, allowing current to flow through the 100K resistor. The purpose of the diode clamps is to protect the pins of the microcontroller from very short overvoltage spikes of a high magnitude. They do this by clamping the voltage excursion to one of the supply rails. We are effectively asking the ESD clamps to do the same thing they were designed to do, but instead of a short high magnitude pulse, we are giving them a long low magnitude static value via the 100k resistor.

Any pin that has digital input/output functionality could potentially be used to monitor VBus, but the use of an interrupt capable GPIO is recommended. A pin that does not have external interrupt capability may also be used, but the input state of the pin must be polled periodically by the application software to ensure appropriate action is taken whenever VBus is applied or removed. If an interrupt capable GPIO is chosen, it should be configured to generate an interrupt on both the rising and falling edge. More information on external interrupts can be found in the *System Control and Interrupts* chapter. Example code that implements VBus monitoring using external interrupts and takes the appropriate actions is documented in the USB Software Guide and can be found in the associated USB software package.

21.3 Functional Description

The USB controller can be configured to act as either a dedicated host or device. However, when the USB controller is acting as a self-powered device, a GPIO input or analog comparator input must be connected to VBUS and configured to generate an interrupt when the VBUS level drops. This interrupt is used to disable the pullup resistor on the USB0DP signal.

Note: When USB is used in the system, the minimum system frequency is 20 MHz.

21.3.1 Operation as a Device

This section describes how the USB controller performs when it is being used as a USB device. IN endpoints, OUT endpoints, entry into and exit from SUSPEND mode, and recognition of start of frame (SOF) are all described.

When in device mode, IN transactions are controlled by the endpoint transmit interface and uses the transmit endpoint registers for the given endpoint. OUT transactions are handled with the endpoints receive interface and uses the receive endpoint registers for the given endpoint. When configuring the size of the FIFOs for endpoints, take into account the maximum packet size for an endpoint.

- Bulk. Bulk endpoints should be the size of the maximum packet (up to 64 bytes) or twice the maximum packet size if double buffering is used (described further in the following section).
- Interrupt. Interrupt endpoints should be the size of the maximum packet (up to 64 bytes) or twice the maximum packet size if double buffering is used.
- Isochronous. Isochronous endpoints are more flexible and can be up to 1023 bytes.
- Control. It is also possible to specify a separate control endpoint for a USB device. However, in most cases the USB device should use the dedicated control endpoint on the USB controller's endpoint 0.

21.3.1.1 Control and Configurable Endpoints

When operating as a device, the USB controller provides two dedicated control endpoints (IN and OUT) and six configurable endpoints (three IN and three OUT) that can be used for communications with a host controller. The endpoint number and direction associated with an endpoint is directly related to its register designation. For example, when the Host is transmitting to endpoint 1, all configuration and data is in the endpoint 1 transmit register interface. Endpoint 0 is a dedicated control endpoint used for all control transactions to endpoint 0 during enumeration or when any other control requests are made to endpoint 0. Endpoint 0 uses the first 64 bytes of the USB controller's FIFO RAM as a shared memory for both IN and OUT transactions. The remaining six endpoints can be configured as control, bulk, interrupt, or isochronous endpoints. They should be treated as three configurable IN and three configurable OUT endpoints. The endpoint pairs are not required to have the same type for their IN and OUT endpoint configuration. For example, the OUT portion of an endpoint pair could be a bulk endpoint, while the IN portion of that endpoint pair could be an interrupt endpoint. The address and size of the FIFOs attached to each endpoint can be modified to fit the application's needs.

21.3.1.1.1 IN Transactions as a Device

When operating as a USB device, data for IN transactions is handled through the FIFOs attached to the transmit endpoints. The sizes of the FIFOs for the three configurable IN endpoints are determined by the USB Transmit FIFO Start Address (USBTXFIFOADD) register. The maximum size of a data packet that may be placed in a transmit endpoint's FIFO for transmission is programmable and is determined by the value written to the USB Maximum Transmit Data Endpoint n (USBTXMAXPn) register for that endpoint. The endpoint's FIFO can also be configured to use double-packet or single-packet buffering. When double-packet buffering is enabled, two data packets can be buffered in the FIFO, which also requires that the FIFO is at least two packets in size. When double-packet buffering is disabled, only one packet can be buffered, even if the packet size is less than half the FIFO size.

Note: The maximum packet size set for any endpoint must not exceed the FIFO size. The USBTXMAXPn register should not be written to while data is in the FIFO as unexpected results may occur.

Single-Packet Buffering

If the size of the transmit endpoint's FIFO is less than twice the maximum packet size for this endpoint (as set in the USB Transmit Dynamic FIFO Sizing (USBTXFIFOSZ) register), only one packet can be buffered in the FIFO and single-packet buffering is required. When each packet is completely loaded into the transmit FIFO, the TXRDY bit in the USB Transmit Control and Status Endpoint n Low (USBTXCSR_n) register must be set. If the AUTOSET bit in the USB Transmit Control and Status Endpoint n High (USBTXCSR_{Hn}) register is set, the TXRDY bit is automatically set when a maximum-sized packet is loaded into the FIFO. For packet sizes less than the maximum, the TXRDY bit must be set manually. When the TXRDY bit is set, either manually or automatically, the packet is ready to be sent. When the packet has been successfully sent, both TXRDY and FIFONE are cleared, and the appropriate transmit endpoint interrupt signaled. At this point, the next packet can be loaded into the FIFO.

Double-Packet Buffering

If the size of the transmit endpoint's FIFO is at least twice the maximum packet size for this endpoint, two packets can be buffered in the FIFO and double-packet buffering is allowed. As each packet is loaded into the transmit FIFO, the TXRDY bit in the USBTXCSR_n register must be set. If the AUTOSET bit in the USBTXCSR_{Hn} register is set, the TXRDY bit is automatically set when a maximum-sized packet is loaded into the FIFO. For packet sizes less than the maximum, TXRDY must be set manually. When the TXRDY bit is set, either manually or automatically, the packet is ready to be sent. After the first packet is loaded, TXRDY is immediately cleared and an interrupt is generated. A second packet can now be loaded into the transmit FIFO and TXRDY set again (either manually or automatically if the packet is the maximum size). At this point, both packets are ready to be sent. After each packet has been successfully sent, TXRDY is automatically cleared and the appropriate transmit endpoint interrupt signaled to indicate that another packet can now be loaded into the transmit FIFO. The state of the FIFONE bit in the USBTXCSR_n register at this point indicates how many packets may be loaded. If the FIFONE bit is set, then another packet is in the FIFO and only one more packet can be loaded. If the FIFONE bit is clear, then no packets are in the FIFO and two more packets can be loaded.

Note: Double-packet buffering is disabled if an endpoint's corresponding EPn bit is set in the USB Transmit Double Packet Buffer Disable (USBTXDPKTBUFDIS) register. This bit is set by default, so it must be cleared to enable double-packet buffering.

21.3.1.1.2 Out Transactions as a Device

When in device mode, OUT transactions are handled through the USB controller receive FIFOs. The sizes of the receive FIFOs for the three configurable OUT endpoints are determined by the USB Receive FIFO Start Address (USBRXFIFOADD) register. The maximum amount of data received by an endpoint in any packet is determined by the value written to the USB Maximum Receive Data Endpoint n (USBRXMAXPn) register for that endpoint. When double-packet buffering is enabled, two data packets can be buffered in the FIFO. When double-packet buffering is disabled, only one packet can be buffered even if the packet is less than half the FIFO size.

Note: In all cases, the maximum packet size must not exceed the FIFO size.

Single-Packet Buffering

If the size of the receive endpoint FIFO is less than twice the maximum packet size for an endpoint, only one data packet can be buffered in the FIFO and single-packet buffering is required. When a packet is received and placed in the receive FIFO, the RXRDY and FULL bits in the USB Receive Control and Status Endpoint n Low (USBRXCSR[n]) register are set and the appropriate receive endpoint is signaled, indicating that a packet can now be unloaded from the FIFO. After the packet has been unloaded, the RXRDY bit must be cleared in order to allow further packets to be received. This action also generates the acknowledge signaling to the Host controller. If the AUTOCL bit in the USB Receive Control and Status Endpoint n High (USBRXCSR[n]) register is set and a maximum-sized packet is unloaded from the FIFO, the RXRDY and FULL bits are cleared automatically. For packet sizes less than the maximum, RXRDY must be cleared manually.

Double-Packet Buffering

If the size of the receive endpoint FIFO is at least twice the maximum packet size for the endpoint, two data packets can be buffered and double-packet buffering can be used. When the first packet is received and loaded into the receive FIFO, the RXRDY bit in the USBRXCSR[n] register is set and the appropriate receive endpoint interrupt is signaled to indicate that a packet can now be unloaded from the FIFO.

Note: The FULL bit in USBRXCSR[n] is not set when the first packet is received. It is only set if a second packet is received and loaded into the receive FIFO.

After each packet has been unloaded, the RXRDY bit must be cleared to allow further packets to be received. If the AUTOCL bit in the USBRXCSR[n] register is set and a maximum-sized packet is unloaded from the FIFO, the RXRDY bit is cleared automatically. For packet sizes less than the maximum, RXRDY must be cleared manually. If the FULL bit is set when RXRDY is cleared, the USB controller first clears the FULL bit, then sets RXRDY again to indicate that there is another packet waiting in the FIFO to be unloaded.

Note: Double-packet buffering is disabled if an endpoint's corresponding EPn bit is set in the USB Receive Double Packet Buffer Disable (USBRXDPKTBUFDIS) register. This bit is set by default, so it must be cleared to enable double-packet buffering.

21.3.1.1.3 Scheduling

The device has no control over the scheduling of transactions as scheduling is determined by the Host controller. The USB controller can set up a transaction at any time. The USB controller waits for the request from the Host controller and generates an interrupt when the transaction is complete or if it was terminated due to some error. If the Host controller makes a request and the device controller is not ready, the USB controller sends a busy response (NAK) to all requests until it is ready.

21.3.1.1.4 Additional Actions

The USB controller responds automatically to certain conditions on the USB bus or actions by the Host controller such as when the USB controller automatically stalls a control transfer or unexpected zero length OUT data packets.

Stalled Control Transfer

The USB controller automatically issues a STALL handshake to a control transfer under the following conditions:

1. The Host sends more data during an OUT data phase of a control transfer than was specified in the device request during the SETUP phase. This condition is detected by the USB controller when the Host sends an OUT token (instead of an IN token) after the last OUT packet has been unloaded and the DATAEND bit in the USB Control and Status Endpoint 0 Low (USBCSRL0) register has been set.
2. The Host requests more data during an IN data phase of a control transfer than was specified in the device request during the SETUP phase. This condition is detected by the USB controller when the Host sends an IN token (instead of an OUT token) after the CPU has cleared TXRDY and set DATAEND in response to the ACK issued by the Host to what should have been the last packet.
3. The Host sends more than USBRXMAXPn bytes of data with an OUT data token.
4. The Host sends more than a zero length data packet for the OUT STATUS phase.

Zero Length OUT Data Packets

A zero-length OUT data packet is used to indicate the end of a control transfer. In normal operation, such packets should only be received after the entire length of the device request has been transferred.

However, if the Host sends a zero-length OUT data packet before the entire length of device request has been transferred, it is signaling the premature end of the transfer. In this case, the USB controller automatically flushes any IN token ready for the data phase from the FIFO and sets the DATAEND bit in the USBCSRL0 register.

Setting the Device Address

When a Host is attempting to enumerate the USB device, it requests that the device change its address from zero to some other value. The address is changed by writing the value that the Host requested to the USB Device Functional Address (USBFADDR) register. However, care should be taken when writing to USBFADDR to avoid changing the address before the transaction is complete. This register should only be set after the SET_ADDRESS command is complete. Like all control transactions, the transaction is only complete after the device has left the STATUS phase. In the case of a SET_ADDRESS command, the transaction is completed by responding to the IN request from the Host with a zero-byte packet. Once the device has responded to the IN request, the USBFADDR register should be programmed to the new value as soon as possible to avoid missing any new commands sent to the new address.

Note: If the USBFADDR register is set to the new value as soon as the device receives the OUT transaction with the SET_ADDRESS command in the packet, it changes the address during the control transfer. In this case, the device does not receive the IN request that allows the USB transaction to exit the STATUS phase of the control transfer because it is sent to the old address. As a result, the Host does not get a response to the IN request, and the Host fails to enumerate the device.

21.3.1.1.5 Device Mode Suspend

When no activity has occurred on the USB bus for 3 ms, the USB controller automatically enters SUSPEND mode. If the SUSPEND interrupt has been enabled in the USB Interrupt Enable (USBIE) register, an interrupt is generated at this time. When in SUSPEND mode, the PHY also goes into SUSPEND mode. When RESUME signaling is detected, the USB controller exits SUSPEND mode and takes the PHY out of SUSPEND. If the RESUME interrupt is enabled, an interrupt is generated. The USB controller can also be forced to exit SUSPEND mode by setting the RESUME bit in the USB Power (USBPOWER) register. When this bit is set, the USB controller exits SUSPEND mode and drives RESUME signaling onto the bus. The RESUME bit must be cleared after 10 ms (a maximum of 15 ms) to end RESUME signaling. To meet USB power requirements, the controller can be put into Deep Sleep mode which keeps the controller in a static state.

21.3.1.1.6 Start of Frame

When the USB controller is operating in device mode, it receives a Start-Of-Frame (SOF) packet from the Host once every millisecond. When the SOF packet is received, the 11-bit frame number contained in the packet is written into the USB Frame Value (USBFRAME) register, and an SOF interrupt is also signaled and can be handled by the application. Once the USB controller has started to receive SOF packets, it expects one every millisecond. If no SOF packet is received after 1.00358 ms, the packet is assumed to have been lost, and the USBFRAME register is not updated. The USB controller continues and resynchronizes these pulses to the received SOF packets when these packets are successfully received again.

21.3.1.1.7 USB Reset

When the USB controller is in device mode and a RESET condition is detected on the USB bus, the USB controller automatically performs the following actions:

- Clears the USBFADDR register
- Clears the USB Endpoint Index (USBEPIX) register
- Flushes all endpoint FIFOs
- Clears all control/status registers
- Enables all endpoint interrupts

- Generates a RESET interrupt

21.3.1.1.8 Connect/Disconnect

The USB controller connection to the USB bus is handled by software. The USB PHY can be switched between normal mode and non-driving mode by setting or clearing the SOFTCONN bit of the USBPOWER register. When the SOFTCONN bit is set, the PHY is placed in its normal mode, and the USB0DP/USB0DM lines of the USB bus are enabled. At the same time, the USB controller is placed into a state, in which it does not respond to any USB signaling except a USB RESET. When the SOFTCONN bit is cleared, the PHY is put into non-driving mode, USB0DP and USB0DM are tristated, and the USB controller appears to other devices on the USB bus as if it has been disconnected. The non-driving mode is the default so the USB controller appears disconnected until the SOFTCONN bit has been set. The application software can then choose when to set the PHY into its normal mode. Systems with a lengthy initialization procedure may use this to ensure that initialization is complete, and the system is ready to perform enumeration before connecting to the USB bus. Once the SOFTCONN bit has been set, the USB controller can be disconnected by clearing this bit.

Note: The USB controller does not generate an interrupt when the device is connected to the Host. However, an interrupt is generated when the Host terminates a session.

21.3.2 Operation as a Host

When the USB controller is operating in Host mode, it can either be used for point-to-point communications with another USB device or, when attached to a hub, for communication with multiple devices. Full-speed and low-speed USB devices are supported, both for point-to-point communication and for operation through a hub. The USB controller automatically carries out the necessary transaction translation needed to allow a low-speed or full-speed device to be used with a USB 2.0 hub. Control, bulk, isochronous, and interrupt transactions are supported. This section describes the USB controller's actions when it is being used as a USB Host. Configuration of IN endpoints, OUT endpoints, entry into and exit from SUSPEND mode, and RESET are all described.

When in Host mode, IN transactions are controlled by an endpoint's receive interface. All IN transactions use the receive endpoint registers and all OUT endpoints use the transmit endpoint registers for a given endpoint. As in device mode, the FIFOs for endpoints should take into account the maximum packet size for an endpoint.

- Bulk. Bulk endpoints should be the size of the maximum packet (up to 64 bytes) or twice the maximum packet size if double buffering is used (described further in the following section).
- Interrupt. Interrupt endpoints should be the size of the maximum packet (up to 64 bytes) or twice the maximum packet size if double buffering is used.
- Isochronous. Isochronous endpoints are more flexible and can be up to 1023 bytes.
- Control. It is also possible to specify a separate control endpoint to communicate with a device. However, in most cases the USB controller should use the dedicated control endpoint to communicate with a device's endpoint 0.

21.3.2.1 Endpoint Registers

The endpoint registers are used to control the USB endpoint interfaces which communicate with device(s) that are connected. The endpoints consist of a dedicated control IN endpoint, a dedicated control OUT endpoint, 3 configurable OUT endpoints, and 3 configurable IN endpoints.

The dedicated control interface can only be used for control transactions to endpoint 0 of devices. These control transactions are used during enumeration or other control functions that communicate using endpoint 0 of devices. This control endpoint shares the first 64 bytes of the USB controller's FIFO RAM for IN and OUT transactions. The remaining IN and OUT interfaces can be configured to communicate with control, bulk, interrupt, or isochronous device endpoints.

These USB interfaces can be used to simultaneously schedule as many as 3 independent OUT and 3 independent IN transactions to any endpoints on any device. The IN and OUT controls are paired in three sets of registers. However, they can be configured to communicate with different types of endpoints and different endpoints on devices. For example, the first pair of endpoint controls can be split so that the OUT portion is communicating with a device's bulk OUT endpoint 1, while the IN portion is communicating with a device's interrupt IN endpoint 2.

Before accessing any device, whether for point-to-point communications or for communications via a hub, the relevant USB Receive Functional Address Endpoint n (USBRXFUNCADDRn) or USB Transmit Functional Address Endpoint n (USBTXFUNCADDRn) registers must be set for each receive or transmit endpoint to record the address of the device being accessed.

The USB controller also supports connections to devices through a USB hub by providing a register that specifies the hub address and port of each USB transfer. The FIFO address and size are customizable and can be specified for each USB IN and OUT transfer. Customization includes allowing one FIFO per transaction, sharing a FIFO across transactions, and allowing for double-buffered FIFOs.

21.3.2.2 IN Transactions as a Host

IN transactions are handled in a similar manner to the way in which OUT transactions are handled when the USB controller is in device mode except that the transaction first must be initiated by setting the REQPKT bit in the USBCSRL0 register, indicating to the transaction scheduler that there is an active transaction on this endpoint. The transaction scheduler then sends an IN token to the target device. When the packet is received and placed in the receive FIFO, the RXRDY bit in the USBCSRL0 register is set, and the appropriate receive endpoint interrupt is signaled to indicate that a packet can now be unloaded from the FIFO.

When the packet has been unloaded, RXRDY must be cleared. The AUTOCL bit in the USBRXCSR_n register can be used to have RXRDY automatically cleared when a maximum-sized packet has been unloaded from the FIFO. The AUTORQ bit in USBRXCSR_n causes the REQPKT bit to be automatically set when the RXRDY bit is cleared. The AUTOCL and AUTORQ bits can be used with DMA accesses to perform complete bulk transfers without main processor intervention. When the RXRDY bit is cleared, the controller sends an acknowledge to the device. When there is a known number of packets to be transferred, the USB Request Packet Count in Block Transfer Endpoint n (USBRQPKTCOUNT_n) register associated with the endpoint should be configured to the number of packets to be transferred. The USB controller decrements the value in the USBRQPKTCOUNT_n register following each request. When the USBRQPKTCOUNT_n value decrements to 0, the AUTORQ bit is cleared to prevent any further transactions being attempted. For cases where the size of the transfer is unknown, USBRQPKTCOUNT_n should be cleared. AUTORQ then remains set until cleared by the reception of a short packet (that is, less than the MAXLOAD value in the USBRXMAXP_n register) such as may occur at the end of a bulk transfer.

If the device responds to a bulk or interrupt IN token with a NAK, the USB Host controller keeps retrying the transaction until any NAK Limit that has been set has been reached. If the target device responds with a STALL, however, the USB Host controller does not retry the transaction but sets the STALLED bit in the USBCSRL0 register. If the target device does not respond to the IN token within the required time, or the packet contained a CRC or bit-stuff error, the USB Host controller retries the transaction. If after three attempts the target device has still not responded, the USB Host controller clears the REQPKT bit and sets the ERROR bit in the USBCSRL0 register.

21.3.2.3 OUT Transactions as a Host

OUT transactions are handled in a similar manner to the way in which IN transactions are handled when the USB controller is in device mode. The TXRDY bit in the USBTXCSR_n register must be set as each packet is loaded into the transmit FIFO. Again, setting the AUTOSET bit in the USBTXCSR_n register automatically sets TXRDY when a maximum-sized packet has been loaded into the FIFO. Furthermore, AUTOSET can be used with the DMA controller to perform complete bulk transfers without software intervention.

If the target device responds to the OUT token with a NAK, the USB Host controller keeps retrying the transaction until the NAK Limit that has been set has been reached. However, if the target device responds with a STALL, the USB controller does not retry the transaction but interrupts the main processor by setting the STALLED bit in the USBTXCSR_n register. If the target device does not respond to the OUT token within the required time, or the packet contained a CRC or bit-stuff error, the USB Host controller retries the transaction. If after three attempts the target device has still not responded, the USB controller flushes the FIFO and sets the ERROR bit in the USBTXCSR_n register.

21.3.2.4 Transaction Scheduling

Scheduling of transactions is handled automatically by the USB Host controller. The Host controller allows configuration of the endpoint communication scheduling based on the type of endpoint transaction. Interrupt transactions can be scheduled to occur in the range of every frame to every 255 frames in 1 frame increments. Bulk endpoints do not allow scheduling parameters, but do allow for a NAK timeout in the event an endpoint on a device is not responding. Isochronous endpoints can be scheduled from every frame to every 216 frames, in powers of 2.

The USB controller maintains a frame counter. If the target device is a full-speed device, the USB controller automatically sends an SOF packet at the start of each frame and increments the frame counter. If the target device is a low-speed device, a K state is transmitted on the bus to act as a keep-alive to stop the low-speed device from going into SUSPEND mode.

After the SOF packet has been transmitted, the USB Host controller cycles through all the configured endpoints looking for active transactions. An active transaction is defined as a receive endpoint for which the REQPKT bit is set or a transmit endpoint for which the TXRDY bit and/or the FIFONE bit is set.

An isochronous or interrupt transaction is started if the transaction is found on the first scheduler cycle of a frame and if the interval counter for that endpoint has counted down to zero. As a result, only one interrupt or isochronous transaction occurs per endpoint every n frames, where n is the interval set via the USB Host Transmit Interval Endpoint n (USBTXINTERVAL[n]) or USB Host Receive Interval Endpoint n (USBRXINTERVAL[n]) register for that endpoint.

An active bulk transaction starts immediately, provided sufficient time is left in the frame to complete the transaction before the next SOF packet is due. If the transaction must be retried (for example, because a NAK was received or the target device did not respond), then the transaction is not retried until the transaction scheduler has first checked all the other endpoints for active transactions. This process ensures that an endpoint that is sending a lot of NAKs does not block other transactions on the bus. The controller also allows the user to specify a limit to the length of time for NAKs to be received from a target device before the endpoint times out.

21.3.2.5 USB Hubs

The following setup requirements apply to the USB Host controller only if it is used with a USB hub. When a full- or low-speed device is connected to the USB controller via a USB 2.0 hub, details of the hub address and the hub port also must be recorded in the corresponding USB Receive Hub Address Endpoint n (USBRXHUBADDRn) and USB Receive Hub Port Endpoint n (USBRXHUBPORTn) or the USB Transmit Hub Address Endpoint n (USBTXHUBADDRn) and USB Transmit Hub Port Endpoint n (USBTXHUBPORTn) registers. In addition, the speed at which the device operates (full or low) must be recorded in the USB Type Endpoint 0 (USBTYPE0) (endpoint 0), USB Host Configure Transmit Type Endpoint n (USBTXTYPEEn), or USB Host Configure Receive Type Endpoint n (USBRXTYPEEn) registers for each endpoint that is accessed by the device.

For hub communications, the settings in these registers record the current allocation of the endpoints to the attached USB devices. To maximize the number of devices supported, the USB Host controller allows this allocation to be changed dynamically by simply updating the address and speed information recorded in these registers. Any changes in the allocation of endpoints to device functions must be made following the completion of any on-going transactions on the endpoints affected.

21.3.2.6 Babble

The USB Host controller does not start a transaction until the bus has been inactive for at least the minimum inter-packet delay. The controller also does not start a transaction unless it can be finished before the end of the frame. If the bus is still active at the end of a frame, then the USB Host controller assumes that the target device to which it is connected has malfunctioned, and the USB controller suspends all transactions and generates a babble interrupt.

21.3.2.7 Host SUSPEND

If the SUSPEND bit in the USBPOWER register is set, the USB Host controller completes the current transaction then stops the transaction scheduler and frame counter. No further transactions are started and no SOF packets are generated.

To exit SUSPEND mode, set the RESUME bit and clear the SUSPEND bit. While the RESUME bit is set, the USB Host controller generates RESUME signaling on the bus. After 20 ms, the RESUME bit must be cleared, at which point the frame counter and transaction scheduler start. The Host supports the detection of a remote wake-up.

21.3.2.8 USB RESET

If the RESET bit in the USBPOWER register is set, the USB Host controller generates USB RESET signaling on the bus. The RESET bit must be set for at least 20 ms to ensure correct resetting of the target device. After the CPU has cleared the bit, the USB Host controller starts its frame counter and transaction scheduler.

21.3.2.9 Connect/Disconnect

A session is started by setting the SESSION bit in the USB device Control (USBDEVCTL) register, enabling the USB controller to wait for a device to be connected. When a device is detected, a connect interrupt is generated. The speed of the device that has been connected can be determined by reading the USBDEVCTL register where the FSDEV bit is set for a full-speed device, and the LSDEV bit is set for a low-speed device. The USB controller must generate a RESET to the device, and then the USB Host controller can begin device enumeration. If the device is disconnected while a session is in progress, a disconnect interrupt is generated.

21.3.3 DMA Operation

The USB peripheral provides an interface connected to the DMA controller with separate channels for 3 transmit endpoints and 3 receive endpoints. The DMA operation of the USB is enabled through the USBTXCSR n and USBRXCSR n registers, for the TX and RX channels respectively. When DMA operation is enabled, the USB asserts a DMA request on the enabled receive or transmit channel when the associated FIFO can transfer data. When either FIFO can transfer data, the request for that channel is asserted. The size of the DMA transfer must be restricted to whole multiples of the size of the USB FIFO. Both read and write transfers of the USB FIFOs using DMA must be configured in this manner. For example, if the USB endpoint is configured with a FIFO size of 64 bytes, the DMA channel can be used to transfer 64 bytes to or from the endpoint FIFO. If the number of bytes to transfer is less than 64, then a programmed I/O method must be used to copy the data to or from the FIFO.

If the DMAMOD bit in the USBTXCSR n /USBRXCSR n register is clear, an interrupt is generated after every packet is transferred, but the DMA continues transferring data. If the DMAMOD bit is set, an interrupt is generated only when the entire DMA transfer is complete. The interrupt occurs on the USB interrupt vector. Therefore, if interrupts are used for USB operation and the DMA is enabled, the USB interrupt handler must be designed to handle the DMA completion interrupt.

Care must be taken when using the DMA to unload the receive FIFO as data is read from the receive FIFO in 4 byte chunks regardless of value of the MAXLOAD field in the USBRXCSR n register. The RXRDY bit is cleared as follows.

To enable DMA operation for the endpoint receive channel, the DMAEN bit of the USBRXCSR $[n]$ register should be set. To enable DMA operation for the endpoint transmit channel, the DMAEN bit of the USBTXCSR $[n]$ register must be set.

See the Direct Memory Access (DMA)" Users Guide for more details about programming the DMA controller.

21.3.4 Address/Data Bus Bridge

The USB controller on this device is the same controller that is on the Stellaris devices. This controller was originally designed to connect to an ARM AHB bus, but has been modified in order to function with the C28x device's bus architecture. The modifications made are largely invisible to the user application, but there are some things to note.

- The USB memory space is 8 bits wide, while the C28x memory space is 16 bits wide.
- 32 and 16 bit accesses (r/w) are completely transparent to the user application code, no changes need be made.
- The C28x core only supports 8 bit accesses through a byte intrinsic type. This can be used to perform 8 bit reads or writes to the USB controller.
 - int &__byte(int *array, unsigned int byte_index);
 - *array = ptr to address to access, byte_index = always 0 (for USB)
See [Table 21-1](#) for example.
 - See the [TMS320C28x Optimizing C/C++ Compiler User's Guide \(SPRU514\)](#) and the [TMS320C28x Assembly Language Tools User's Guide \(SPRU513\)](#)
- Because of the bridge, the memory view of the USB controller memory space in CCS isn't a 1:1 representation of what is in the controller
 - When the view mode is
 - 32 bit or 16 bit, even address are effectively duplicated, ignore odd addresses.
 - 8 bit, Even addresses from within the controller are duplicated into odd address in the view window; odd addresses from within the controller are not displayed.
See [Table 21-2](#) for example.

Table 21-1. USB Memory Access From Software

USB Controller Memory			C28x 8 Bit	
Address	Reg. Name	Data	Access	Data
0x00	FADDR	0x00	__byte((int *)0x00,0)	0x0000
0x01	POWER	0x11	__byte((int *)0x01,0)	0x0011
0x02	TXIS (LSB)	0x22	__byte((int *)0x02,0)	0x0022
0x03	TXIS (MSB)	0x33	__byte((int *)0x03,0)	0x0033
0x04	RXIS (LSB)	0x44	__byte((int *)0x04,0)	0x0044
0x05	RXIS (MSB)	0x55	__byte((int *)0x05,0)	0x0055
0x06	TXIE (LSB)	0x66	__byte((int *)0x06,0)	0x0066
0x07	TXIE (MSB)	0x77	__byte((int *)0x07,0)	0x0077
0x08	RXIE (LSB)	0x88	__byte((int *)0x08,0)	0x0088
0x09	RXIE (MSB)	0x99	__byte((int *)0x09,0)	0x0099
0x0A	USBIS	0xAA	__byte((int *)0xA0,0)	0x00AA
0x0B	USBIE	0xBB	__byte((int *)0xB0,0)	0x00BB
0x0C	FRAME (LSB)	0xCC	__byte((int *)0xC0,0)	0x00CC
0x0D	FRAME (MSB)	0xDD	__byte((int *)0xD0,0)	0x00DD
0x0E	EPIIDX	0xEE	__byte((int *)0xE0,0)	0x00EE
0x0F	TEST	0xFF	__byte((int *)0xF0,0)	0x00FF
C28x 16 Bit			C28x 32 Bit	
Access	Data		Access	Data
(*((short *)(0x00)))	0x1100		(*((long *)(0x00)))	0x33221100
(*((short *)(0x01)))	0x1100		(*((long *)(0x01)))	0x33221100
(*((short *)(0x02)))	0x3322		(*((long *)(0x02)))	0x33221100

Table 21-1. USB Memory Access From Software (continued)

USB Controller Memory			C28x 8 Bit	
(*((short *)(0x03)))	0x3322		(*((long *)(0x03)))	0x33221100
(*((short *)(0x04)))	0x5544		(*((long *)(0x04)))	0x77665544
(*((short *)(0x05)))	0x5544		(*((long *)(0x05)))	0x77665544
(*((short *)(0x06)))	0x7766		(*((long *)(0x06)))	0x77665544
(*((short *)(0x07)))	0x7766		(*((long *)(0x07)))	0x77665544
(*((short *)(0x08)))	0x9988		(*((long *)(0x08)))	0xBBAA9988
(*((short *)(0x09)))	0x9988		(*((long *)(0x09)))	0xBBAA9988
(*((short *)(0x0A)))	0xBBAA		(*((long *)(0x0A)))	0xBBAA9988
(*((short *)(0x0B)))	0xBBAA		(*((long *)(0x0B)))	0xBBAA9988
(*((short *)(0x0C)))	0xDDCC		(*((long *)(0x0C)))	0xFFEEDDCC
(*((short *)(0x0D)))	0xDDCC		(*((long *)(0x0D)))	0xFFEEDDCC
(*((short *)(0x0E)))	0xFFEE		(*((long *)(0x0E)))	0xFFEEDDCC
(*((short *)(0x0F)))	0xFFEE		(*((long *)(0x0F)))	0xFFEEDDCC

Table 21-2. USB Memory Access From CCS

CCS 8 Bit		CCS 16 Bit		CCS 32 Bit	
Address	Displayed Data	Address	Displayed Data	Address	Displayed Data
0x00	0x00	0x00	0x1100	0x00	0x11001100
0x01	0x00	0x01	0x1100	0x02	0x33223322
0x02	0x22	0x02	0x3322	0x04	0x55445544
0x03	0x22	0x03	0x3322	0x06	0x77667766
0x04	0x44	0x04	0x5544	0x08	0x99889988
0x05	0x44	0x05	0x5544	0x0A	0xBBAAABBAA
0x06	0x66	0x06	0x7766	0x0C	0xDDCCDDCC
0x07	0x66	0x07	0x7766	0x0E	0xFFEEFFEE
0x08	0x88	0x08	0x9988		
0x09	0x88	0x09	0x9988		
0x0A	0xAA	0x0A	0xBBAA		
0x0B	0xAA	0x0B	0xBBAA		
0x0C	0xCC	0x0C	0xDDCC		
0x0D	0xCC	0x0D	0xDDCC		
0x0E	0xEE	0x0E	0xFFEE		
0x0F	0xEE	0x0F	0xFFEE		

21.4 Initialization and Configuration

To use the USB Controller, the clock for the USB controller must first be configured. USBCLK is driven via the second PLL within the chip. The PLL should be configured to operate at 60MHz via the PLL2CTL, PLL2MULT, PLL2STS registers. After the PLL is enabled and locked, the controller can be clocked by enabling the peripheral in the PCLKCR3 register. In addition to the clock, the USB PHY must be enabled. Configure the USBIOPEN field in the GPACTRL2 register to enable USB functionality on the designated pins. After the clock has been enabled and the USB PHY turned on the USB peripheral is ready for operation and the associated software initialization routines may be called.

21.4.1 Pin Configuration

In order to give the user more flexibility, the signals External Power Enable (EPEN) and Power Fault (PFLT) were not implemented in hardware. Instead, it is left up to the user to implement these signals in software. Examples of how to implement these signals in software can be found in the f2806x USB Software Guide.

When using the device controller portion of the USB controller in a system that also provides Host functionality, the power to VBUS must be disabled to allow the external Host controller to supply power. Usually, the EPEN signal is used to control the external regulator and should be negated to avoid having two devices driving the VBUS power pin on the USB connector.

When the USB controller is acting as a Host, it is in control of two signals that are attached to an external voltage supply that provides power to VBUS. The Host controller uses the EPEN signal to enable or disable power to the VBUS pin on the USB connector. An input pin, PFLT, provides feedback when there has been a power fault on VBUS. The PFLT signal can be configured to either automatically negate the EPEN signal to disable power, and/or it can generate an interrupt to the interrupt controller to allow software to handle the power fault condition. The polarity and actions related to both EPEN and PFLT are fully configurable in the USB controller. The controller also provides interrupts on device insertion and removal to allow the Host controller code to respond to these external events.

21.4.2 Endpoint Configuration

To start communication in Host or device mode, the endpoint registers must first be configured. In Host mode, this configuration establishes a connection between an endpoint register and an endpoint on a device. In device mode, an endpoint must be configured before enumerating to the Host controller.

In both cases, the endpoint 0 configuration is limited because it is a fixed-function, fixed-FIFO-size endpoint. In device and Host modes, the endpoint requires little setup but does require a software-based state machine to progress through the setup, data, and status phases of a standard control transaction. In device mode, the configuration of the remaining endpoints is done once before enumerating and then only changed if an alternate configuration is selected by the Host controller. In Host mode, the endpoints must be configured to operate as control, bulk, interrupt or isochronous mode. Once the type of endpoint is configured, a FIFO area must be assigned to each endpoint. In the case of bulk, control and interrupt endpoints, each has a maximum of 64 bytes per transaction. Isochronous endpoints can have packets with up to 1023 bytes per packet. In either mode, the maximum packet size for the given endpoint must be set prior to sending or receiving data.

Configuring each endpoint's FIFO involves reserving a portion of the overall USB FIFO RAM to each endpoint. The total FIFO RAM available is 4 Kbytes with the first 64 bytes reserved for endpoint 0. The endpoint's FIFO must be at least as large as the maximum packet size. The FIFO can also be configured as a double-buffered FIFO so that interrupts occur at the end of each packet and allow filling the other half of the FIFO.

If operating as a device, the USB device controller's soft connect must be enabled when the device is ready to start communications, indicating to the host controller that the device is ready to start the enumeration process. If operating as a Host controller, the device soft connect must be disabled and power must be provided to VBUS via the USB0EPEN signal.

21.5 Register Map

Table 21-3 lists the registers. All addresses given are relative to the USB base address of 0x4000. Note that the USB controller clock must be enabled before the registers can be programmed (see the *System Control* chapter).

Table 21-3. Universal Serial Bus (USB) Controller Register Map

Offset	Name	Type	Reset	Description	Location
0x000	USBFADDR ⁽¹⁾	R/W	0x00	USB Device Functional Address	Section 21.6.1
0x001	USBPOWER ⁽¹⁾⁽²⁾	R/W	0x20	USB Power	Section 21.6.2
0x002	USBTXIS ⁽¹⁾⁽²⁾	RO	0x0000	USB Transmit Interrupt Status	Section 21.6.3

Table 21-3. Universal Serial Bus (USB) Controller Register Map (continued)

Offset	Name	Type	Reset	Description	Location
0x004	USBRXIS ⁽¹⁾⁽²⁾	RO	0x0000	USB Receive Interrupt Status	Section 21.6.4
0x006	USBTXIE ⁽¹⁾⁽²⁾	R/W	0xFFFF	USB Transmit Interrupt Enable	Section 21.6.5
0x008	USBRXIE ⁽¹⁾⁽²⁾	R/W	0xFFFE	USB Receive Interrupt Enable	Section 21.6.6
0x00A	USBIS ⁽¹⁾⁽²⁾	RO	0x00	USB General Interrupt Status	Section 21.6.7
0x00B	USBIE ⁽¹⁾⁽²⁾	R/W	0x06	USB Interrupt Enable	Section 21.6.8
0x00C	USBFRAME ⁽¹⁾⁽²⁾	RO	0x0000	USB Frame Value	Section 21.6.9
0x00E	USBEPIDX ⁽¹⁾⁽²⁾	R/W	0x00	USB Endpoint Index	Section 21.6.10
0x00F	USBTEST ⁽¹⁾⁽²⁾	R/W	0x00	USB Test Mode	Section 21.6.11
0x020	USBFIFO0 ⁽¹⁾⁽²⁾	R/W	0x0000.0000	USB FIFO Endpoint 0	Section 21.6.12
0x024	USBFIFO1 ⁽¹⁾⁽²⁾	R/W	0x0000.0000	USB FIFO Endpoint 1	Section 21.6.12
0x028	USBFIFO2 ⁽¹⁾⁽²⁾	R/W	0x0000.0000	USB FIFO Endpoint 2	Section 21.6.12
0x02C	USBFIFO3 ⁽¹⁾⁽²⁾	R/W	0x0000.0000	USB FIFO Endpoint 3	Section 21.6.12
0x060	USBDEVCTL ⁽²⁾	R/W	0x80	USB Device Control	Section 21.6.13
0x062	USBTXFIFOSZ ⁽¹⁾⁽²⁾	R/W	0x00	USB Transmit Dynamic FIFO Sizing	Section 21.6.14
0x063	USBRXFIFOSZ ⁽¹⁾⁽²⁾	R/W	0x00	USB Receive Dynamic FIFO Sizing	Section 21.6.15
0x064	USBTXFIFOADD ⁽¹⁾⁽²⁾	R/W	0x0000	USB Transmit FIFO Start Address	Section 21.6.16
0x066	USBRXFIFOADD ⁽¹⁾⁽²⁾	R/W	0x0000	USB Receive FIFO Start Address	Section 21.6.17
0x07A	USBCONTIM ⁽¹⁾⁽²⁾	R/W	0x5C	USB Connect Timing	Section 21.6.18
0x07D	USBFSEOF ⁽¹⁾⁽²⁾	R/W	0x77	USB Full-Speed Last Transaction to End of Frame Timing	Section 21.6.19
0x07E	USBLSEOF ⁽¹⁾⁽²⁾	R/W	0x72	USB Low-Speed Last Transaction to End of Frame Timing	Section 21.6.20
0x080	USBTXFUNCADDR0 ⁽²⁾	R/W	0x00	USB Transmit Functional Address Endpoint 0	Section 21.6.21
0x082	USBTXHUBADDR0 ⁽²⁾	R/W	0x00	USB Transmit Hub Address Endpoint 0	Section 21.6.22
0x083	USBTXHUBPORT0 ⁽²⁾	R/W	0x00	USB Transmit Hub Port Endpoint 0	Section 21.6.23
0x088	USBTXFUNCADDR1 ⁽²⁾	R/W	0x00	USB Transmit Functional Address Endpoint 1	Section 21.6.21
0x08A	USBTXHUBADDR1 ⁽²⁾	R/W	0x00	USB Transmit Hub Address Endpoint 1	Section 21.6.22
0x08B	USBTXHUBPORT1 ⁽²⁾	R/W	0x00	USB Transmit Hub Port Endpoint 1	Section 21.6.23
0x08C	USBRXFUNCADDR1 ⁽²⁾	R/W	0x00	USB Receive Functional Address Endpoint 1	Section 21.6.24
0x08E	USBRXHUBADDR1 ⁽²⁾	R/W	0x00	USB Receive Hub Address Endpoint 1	Section 21.6.25
0x08F	USBRXHUBPORT1 ⁽²⁾	R/W	0x00	USB Receive Hub Port Endpoint 1	Section 21.6.26
0x090	USBTXFUNCADDR2 ⁽²⁾	R/W	0x00	USB Transmit Functional Address Endpoint 2	Section 21.6.21

Table 21-3. Universal Serial Bus (USB) Controller Register Map (continued)

Offset	Name	Type	Reset	Description	Location
0x092	USBTXHUBADDR2 ⁽²⁾	R/W	0x00	USB Transmit Hub Address Endpoint 2	Section 21.6.22
0x093	USBTXHUBPORT2 ⁽²⁾	R/W	0x00	USB Transmit Hub Port Endpoint 2	Section 21.6.23
0x094	USBRXFUNCADDR2 ⁽²⁾	R/W	0x00	USB Receive Functional Address Endpoint 2	Section 21.6.24
0x096	USBRXHUBADDR2 ⁽²⁾	R/W	0x00	USB Receive Hub Address Endpoint 2	Section 21.6.25
0x097	USBRXHUBPORT2 ⁽²⁾	R/W	0x00	USB Receive Hub Port Endpoint 2	Section 21.6.26
0x098	USBTXFUNCADDR3 ⁽²⁾	R/W	0x00	USB Transmit Functional Address Endpoint 3	Section 21.6.21
0x09A	USBTXHUBADDR3 ⁽²⁾	R/W	0x00	USB Transmit Hub Address Endpoint 3	Section 21.6.22
0x09B	USBTXHUBPORT3 ⁽²⁾	R/W	0x00	USB Transmit Hub Port Endpoint 3	Section 21.6.23
0x09C	USBRXFUNCADDR3 ⁽²⁾	R/W	0x00	USB Receive Functional Address Endpoint 3	Section 21.6.24
0x09E	USBRXHUBADDR3 ⁽²⁾	R/W	0x00	USB Receive Hub Address Endpoint 3	Section 21.6.25
0x09F	USBRXHUBPORT3 ⁽²⁾	R/W	0x00	USB Receive Hub Port Endpoint 3	Section 21.6.26
0x102	USBCSRL0 ⁽¹⁾⁽²⁾	W1C	0x00	USB Control and Status Endpoint 0 Low	Section 21.6.28
0x103	USBCSRH0 ⁽¹⁾⁽²⁾	W1C	0x00	USB Control and Status Endpoint 0 High	Section 21.6.29
0x108	USBCOUNT0 ⁽¹⁾⁽²⁾	R/o	0x00	USB Receive Byte Count Endpoint 0	Section 21.6.30
0x10A	USBTYPE0 ⁽²⁾	R/W	0x00	USB Type Endpoint 0	Section 21.6.31
0x10B	USBNAKLMT ⁽²⁾	R/W	0x00	USB NAK Limit	Section 21.6.32
0x110	USBTXMAXP1 ⁽¹⁾⁽²⁾	R/W	0x0000	USB Maximum Transmit Data Endpoint 1	Section 21.6.27
0x112	USBTXCSR1 ⁽¹⁾⁽²⁾	R/W	0x00	USB Transmit Control and Status Endpoint 1 Low	Section 21.6.33
0x113	USBTXCSR1 ⁽¹⁾⁽²⁾	R/W	0x00	USB Transmit Control and Status Endpoint 1 High	Section 21.6.34
0x114	USBRXMAXP1 ⁽¹⁾⁽²⁾	R/W	0x0000	USB Maximum Receive Data Endpoint 1	Section 21.6.35
0x116	USBRXCSR1 ⁽¹⁾⁽²⁾	R/W	0x00	USB Receive Control and Status Endpoint 1 Low	Section 21.6.36
0x117	USBRXCSR1 ⁽¹⁾⁽²⁾	R/W	0x00	USB Receive Control and Status Endpoint 1 High	Section 21.6.37
0x118	USBRXCOUNT1 ⁽¹⁾⁽²⁾	RO	0x0000	USB Receive Byte Count Endpoint 1	Section 21.6.38
0x11A	USBTXTYPE1 ⁽²⁾	R/W	0x00	USB Host Transmit Configure Type Endpoint 1	Section 21.6.39

Table 21-3. Universal Serial Bus (USB) Controller Register Map (continued)

Offset	Name	Type	Reset	Description	Location
0x11B	USBTXINTERVAL1 ⁽²⁾	R/W	0x00	USB Host Transmit Interval Endpoint 1	Section 21.6.40
0x11C	USBRXTYPE1 ⁽²⁾	R/W	0x00	USB Host Configure Receive Type Endpoint 1	Section 21.6.41
0x11D	USBRXINTERVAL1 ⁽²⁾	R/W	0x00	USB Host Receive Polling Interval Endpoint 1	Section 21.6.42
0x120	USBTXMAXP2 ⁽¹⁾⁽²⁾	R/W	0x0000	USB Maximum Transmit Data Endpoint 2	Section 21.6.27
0x122	USBTXCSRL2 ⁽¹⁾⁽²⁾	R/W	0x00	USB Transmit Control and Status Endpoint 2 Low	Section 21.6.33
0x123	USBTXCSRH2 ⁽¹⁾⁽²⁾	R/W	0x00	USB Transmit Control and Status Endpoint 2 High	Section 21.6.34
0x124	USBRXMAXP2 ⁽¹⁾⁽²⁾	R/W	0x0000	USB Maximum Receive Data Endpoint 2	Section 21.6.35
0x126	USBRXCSRL2 ⁽¹⁾⁽²⁾	R/W	0x00	USB Receive Control and Status Endpoint 2 Low	Section 21.6.36
0x127	USBRXCSRH2 ⁽¹⁾⁽²⁾	R/W	0x00	USB Receive Control and Status Endpoint 2 High	Section 21.6.37
0x128	USBRXCOUNT2 ⁽¹⁾⁽²⁾	RO	0x0000	USB Receive Byte Count Endpoint 2	Section 21.6.38
0x12A	USBTXTYPE2 ⁽²⁾	R/W	0x00	USB Host Transmit Configure Type Endpoint 2	Section 21.6.39
0x12B	USBTXINTERVAL2 ⁽²⁾	R/W	0x00	USB Host Transmit Interval Endpoint 2	Section 21.6.40
0x12C	USBRXTYPE2 ⁽²⁾	R/W	0x00	USB Host Configure Receive Type Endpoint 2	Section 21.6.41
0x12D	USBRXINTERVAL2 ⁽²⁾	R/W	0x00	USB Host Receive Polling Interval Endpoint 2	Section 21.6.42
0x130	USBTXMAXP3 ⁽¹⁾⁽²⁾	R/W	0x0000	USB Maximum Transmit Data Endpoint 3	Section 21.6.27
0x132	USBTXCSRL3 ⁽¹⁾⁽²⁾	R/W	0x00	USB Transmit Control and Status Endpoint 3 Low	Section 21.6.33
0x133	USBTXCSRH3 ⁽¹⁾⁽²⁾	R/W	0x00	USB Transmit Control and Status Endpoint 3 High <small>Section 21.6.34</small>	Section 21.6.34
0x134	USBRXMAXP3 ⁽¹⁾⁽²⁾	R/W	0x0000	USB Maximum Receive Data Endpoint 3	Section 21.6.35
0x136	USBRXCSRL3 ⁽¹⁾⁽²⁾	R/W	0x00	USB Receive Control and Status Endpoint 3 Low	Section 21.6.33
0x137	USBRXCSRH3 ⁽¹⁾⁽²⁾	R/W	0x00	USB Receive Control and Status Endpoint 3 High	Section 21.6.36
0x138	USBRXCOUNT3 ⁽¹⁾⁽²⁾	RO	0x0000	USB Receive Byte Count Endpoint 3	Section 21.6.38

Table 21-3. Universal Serial Bus (USB) Controller Register Map (continued)

Offset	Name	Type	Reset	Description	Location
0x13A	USBTXTYPE3 ⁽²⁾	R/W	0x00	USB Host Transmit Configure Type Endpoint 3	Section 21.6.39
0x13B	USBTXINTERVAL3 ⁽²⁾	R/W	0x00	USB Host Transmit Interval Endpoint 3	Section 21.6.40
0x13C	USRXTYPE3 ⁽²⁾	R/W	0x00	USB Host Configure Receive Type Endpoint 3	Section 21.6.41
0x13D	USRXINTERVAL3 ⁽²⁾	R/W	0x00	USB Host Receive Polling Interval Endpoint 3	Section 21.6.42
0x304	USRQPKTCOUNT1 ⁽²⁾	R/W	0x0000 1	USB Request Packet Count in Block Transfer Endpoint 1	Section 21.6.43
0x308	USRQPKTCOUNT2 ⁽²⁾	R/W	0x0000	USB Request Packet Count in Block Transfer Endpoint 2	Section 21.6.43
0x30C	USRQPKTCOUNT3 ⁽²⁾	R/W	0x0000	USB Request Packet Count in Block Transfer Endpoint 3	Section 21.6.43
0x340	USBRXDPKTBUFDIS ⁽¹⁾⁽²⁾	R/W	0x0000	USB Receive Double Packet Buffer Disable	Section 21.6.44
0x342	USBTXDPKTBUFDIS ⁽¹⁾⁽²⁾	R/W	0x0000	USB Transmit Double Packet Buffer Disable	Section 21.6.45
0x400	USBEPC ⁽¹⁾⁽²⁾	R/W	0x0000.0000	USB External Power Control	Section 21.6.46
0x404	USBEPCRIS ⁽¹⁾⁽²⁾	RO	0x0000.0000	USB External Power Control Raw Interrupt Status	Section 21.6.47
0x408	USBEPCIM ⁽²⁾⁽¹⁾	R/W	0x0000.0000	USB External Power Control Interrupt Mask	Section 21.6.48
0x40C	USBEPCISC ⁽¹⁾⁽²⁾	R/W	0x0000.0000	USB External Power Control Interrupt Status and Clear	Section 21.6.49
0x410	USBDRRIS ⁽¹⁾⁽²⁾	RO	0x0000.0000	USB Device RESUME Raw Interrupt Status	Section 21.6.50
0x414	USBDRIM ⁽¹⁾⁽²⁾	R/W	0x0000.0000	USB Device RESUME Interrupt Mask	Section 21.6.51
0x418	USBDRISC ⁽¹⁾⁽²⁾	W1C	0x0000.0000	USB Device RESUME Interrupt Status and Clear	Section 21.6.52
0x41C	USBGPCS ⁽¹⁾⁽²⁾	R/W	0x0000.0000	USB General-Purpose Control and Status	Section 21.6.53
0x450	USBDMASEL ⁽¹⁾⁽²⁾	R/W	0x0033.2211	USB DMA Select	Section 21.6.54

- (1) This register is used in Device mode. Some registers are used for both Host and Device mode and may have different bit definitions depending on the mode.
- (2) This register is used in Host mode. Some registers are used for both Host and Device mode and may have different bit definitions depending on the mode. The USB controller is in Device mode upon reset, so the reset values shown for these registers apply to the Device mode definition.

21.6 Register Descriptions

21.6.1 USB Device Functional Address Register (USBFADDR), offset 0x000

The USB function address 8-bit register (USBFADDR) contains the 7-bit address of the device part of the transaction.

When the USB controller is being used in device mode (the HOST bit in the USBDEVCTL register is clear), this register must be written with the address received through a SET_ADDRESS command, which is then used for decoding the function address in subsequent token packets.

Mode(s): Device

For special considerations when writing this register, see the *Setting the Device Address* in [Section 21.3.1.1.4](#).

USBFADDR is shown in [Figure 21-3](#) and described in [Table 21-4](#).

Figure 21-3. Function Address Register (USBFADDR)

7	6	0
Reserved		FUNCADDR
R-0		R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-4. Function Address Register (USBFADDR) Field Descriptions

Bit	Field	Value	Description
7	Reserved	0	Reserved
6-0	FUNCADDR	0-7Fh	Function Address of Device as received through SET_ADDRESS.

21.6.2 USB Power Management Register (USBPOWER), offset 0x001

The power management 8-bit register (USBPOWER) is used for controlling SUSPEND and RESUME signaling, and some basic operational aspects of the USB controller.

Mode(s): Host Device

USBPOWER in Host Mode is shown in [Figure 21-4](#) and described in [Table 21-5](#).

Figure 21-4. Power Management Register (USBPOWER) in Host Mode

7	4	3	2	1	0
Reserved		RESET	RESUME	SUSPEND	PWRDNPHY

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-5. Power Management Register (USBPOWER) in Host Mode Field Descriptions

Bit	Field	Value	Description
7-4	Reserved	0	Reserved
3	RESET	0 1	RESET signaling. Ends RESET signaling on the bus. Enables RESET signaling on the bus.
2	RESUME	0 1	RESUME signaling. The bit should be cleared by software 20 ms after being set. Ends RESUME signaling on the bus. Enables RESUME signaling when the Device is in SUSPEND mode.
1	SUSPEND	0 1	SUSPEND mode No effect Enables SUSPEND mode.
0	PWRDNPHY	0 1	Power Down PHY No effect Powers down the internal USB PHY.

USBPOWER in Device Mode is shown in [Figure 21-5](#) and described in [Table 21-6](#).

Figure 21-5. Power Management Register (USBPOWER) in Device Mode

7	6	5	4	3	2	1	0
ISOUPDATE	SOFTCONN	Reserved	R-0	RESET	RESUME	SUSPEND	PWRDNPHY

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-6. Power Management Register (USBPOWER) in Device Mode Field Descriptions

Bit	Field	Value	Description
7	ISOUPDATE	0 1	Isochronous Update No effect The USB controller waits for an SOF token from the time the TXRDY bit is set in the USBTXCSRLn register before sending the packet. If an IN token is received before an SOF token, then a zero-length data packet is sent.
6	SOFTCONN	0 1	Soft Connect/Disconnect The USB D+/D- lines are tri-stated. The USB D+/D- lines are enabled.
5-4	Reserved	0	Reserved

Table 21-6. Power Management Register (USBPOWER) in Device Mode Field Descriptions (continued)

Bit	Field	Value	Description
3	RESET	0	RESET signaling Ends RESET signaling on the bus.
		1	Enables RESET signaling on the bus.
2	RESUME	0	RESUME signaling. The bit should be cleared by software 10 ms (a maximum of 15 ms) after being set. Ends RESUME signaling on the bus.
		1	Enables RESUME signaling when the Device is in SUSPEND mode.
1	SUSPEND	0	SUSPEND mode. This bit is cleared when software reads the interrupt register or sets the RESUME bit above.
		1	The USB controller is in SUSPEND mode.
0	PWRDNPHY	0	Power Down PHY No effect
		1	Powers down the internal USB PHY.

21.6.3 USB Transmit Interrupt Status Register (USBTXIS), offset 0x002

NOTE: Use caution when reading this register. Performing a read may change bit status.

The USB transmit interrupt status 16-bit read-only register (USBTXIS) indicates which interrupts are currently active for endpoint 0 and the transmit endpoints 1–3. The meaning of the EPn bits in this register is based on the mode of the device. The EP1 through EP3 bits always indicate that the USB controller is sending data; however, in Host mode, the bits refer to OUT endpoints; while in Device mode, the bits refer to IN endpoints. The EP0 bit is special in Host and Device modes and indicates that either a control IN or control OUT endpoint has generated an interrupt.

Mode(s): Host Device

USBTXIS is shown in [Figure 21-6](#) and described in [Table 21-7](#).

Figure 21-6. USB Transmit Interrupt Status Register (USBTXIS)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Reserved										EP3	EP2	EP1	EP0
			R-0							R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset sho

Table 21-7. USB Transmit Interrupt Status Register (USBTXIS) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved		Reserved
3	EP3	0	TX Endpoint 3 Interrupt No interrupt
		1	The Endpoint 3 transmit interrupt is asserted.
2	EP2	0	TX Endpoint 2 Interrupt No interrupt
		1	The Endpoint 2 transmit interrupt is asserted.
1	EP1	0	TX Endpoint 1 Interrupt No interrupt
		1	The Endpoint 1 transmit interrupt is asserted.
0	EP0	0	TX and RX Endpoint 0 Interrupt No interrupt
		1	The Endpoint 0 transmit and receive interrupt is asserted.

21.6.4 USB Receive Interrupt Status Register (USBRXIS), offset 0x004

NOTE: Use caution when reading this register. Performing a read may change bit status.

The USB receive interrupt status 16-bit read-only register (USBRXIS) indicates which interrupts are currently active for receive endpoints 1–3.

Note: Bits relating to endpoints that have not been configured always return 0. All active interrupts are cleared when this register is read.

Mode(s): Host Device

USBRXIS is shown in [Figure 21-7](#) and described in [Table 21-8](#).

Figure 21-7. USB Receive Interrupt Status Register (USBRXIS)

15	Reserved	4	3	2	1	0
	R-0	R-0	R-0	R-0	R-0	Rsvd

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-8. USB Receive Interrupt Status Register (USBRXIS) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved		Reserved
3	EP3	0	RX Endpoint 3 Interrupt No interrupt
		1	The Endpoint 3 receive interrupt is asserted.
2	EP2	0	RX Endpoint 2 Interrupt No interrupt
		1	The Endpoint 2 receive interrupt is asserted.
1	EP1	0	RX Endpoint 1 Interrupt No interrupt
		1	The Endpoint 1 receive interrupt is asserted.
0	Reserved	0	Reserved

21.6.5 USB Transmit Interrupt Enable Register (USBTXIE), offset 0x006

The USB transmit interrupt enable 16-bit register (USBTXIE) provides interrupt enable bits for the interrupts in the USBTXIS register. When a bit is set, the USB interrupt is asserted to the interrupt controller when the corresponding interrupt bit in the USBTXIS register is set. When a bit is cleared, the interrupt in the USBTXIS register is still set but the USB interrupt to the interrupt controller is not asserted. On reset, all interrupts are enabled.

Mode(s): Host Device

USBTXIS is shown in [Figure 21-8](#) and described in [Table 21-9](#).

Figure 21-8. USB Transmit Interrupt Status Enable Register (USBTXIE)

15	4	3	2	1	0
Reserved	EP3	EP2	EP1	EP0	
R-0	R/W-1	R/W-1	R/W-1	R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-9. USB Transmit Interrupt Status Register (USBTXIE) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved		Reserved
		0	TX Endpoint 3 Interrupt Enable The EP3 transmit interrupt is suppressed and not sent to the interrupt controller.
3	EP3	1	An interrupt is sent to the interrupt controller when the EP3 bit in the USBTXIS register is set.
		0	TX Endpoint 2 Interrupt Enable The EP2 transmit interrupt is suppressed and not sent to the interrupt controller.
2	EP2	1	An interrupt is sent to the interrupt controller when the EP2 bit in the USBTXIS register is set.
		0	TX Endpoint 1 Interrupt Enable The EP1 transmit interrupt is suppressed and not sent to the interrupt controller.
1	EP1	1	An interrupt is sent to the interrupt controller when the EP1 bit in the USBTXIS register is set.
		0	TX and RX Endpoint 0 Interrupt Enable The EP0 transmit and receive interrupt is suppressed and not sent to the interrupt controller.
0	EP0	1	An interrupt is sent to the interrupt controller when the EP0 bit in the USBTXIS register is set.

21.6.6 USB Receive Interrupt Enable Register (USBRXIE), offset 0x008

The USB receive interrupt enable 16-bit register (USBRXIE) provides interrupt enable bits for the interrupts in the USBRXIS register. When a bit is set, the USB interrupt is asserted to the interrupt controller when the corresponding interrupt bit in the USBRXIS register is set. When a bit is cleared, the interrupt in the USBRXIS register is still set but the USB interrupt to the interrupt controller is not asserted. On reset, all interrupts are enabled.

Mode(s): Host Device

USBRXIE is shown in [Figure 21-8](#) and described in [Table 21-9](#).

Figure 21-9. USB Receive Interrupt Enable Register (USBRXIE)

15	4	3	2	1	0
Reserved	EP3	EP2	EP1	Rsvd	
R-0	R/W-1	R/W-1	R/W-1	R-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-10. USB Receive Interrupt Register (USBRXIE) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved		Reserved
3	EP3	0	RX Endpoint 3 Interrupt Enable The EP3 receive interrupt is suppressed and not sent to the interrupt controller.
		1	An interrupt is sent to the interrupt controller when the EP3 bit in the USBRXIS register is set.
2	EP2	0	RX Endpoint 2 Interrupt Enable The EP2 receive interrupt is suppressed and not sent to the interrupt controller.
		1	An interrupt is sent to the interrupt controller when the EP2 bit in the USBRXIS register is set.
1	EP1	0	RX Endpoint 1 Interrupt Enable The EP1 receive interrupt is suppressed and not sent to the interrupt controller.
		1	An interrupt is sent to the interrupt controller when the EP1 bit in the USBRXIS register is set.
0	Reserved	0	Reserved

21.6.7 USB General Interrupt Status Register (USBIS), offset 0x00A

NOTE: Use caution when reading this register. Performing a read may change bit status.

The USB general interrupt status 8-bit read-only register (USBIS) indicates which USB interrupts are currently active. All active interrupts are cleared when this register is read.

Mode(s): Host Device

USBIS in Host Mode is shown in [Figure 21-10](#) and described in [Table 21-11](#).

Figure 21-10. USB General Interrupt Status Register (USBIS) in Host Mode

7	6	5	4	3	2	1	0
VBUSERR	SESREQ	DISCON	CONN	SOF	BABBLE	RESUME	Reserved
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-11. USB General Interrupt Status Register (USBIS) in Host Mode Field Descriptions

Bit	Field	Value	Description
7	VBUSERR	0	VBUS Error
		1	No interrupt
			VBUS has dropped below the VBUS Valid threshold during a session.
6	SESREQ	0	Session Request
		1	No interrupt
			SESSION REQUEST signaling has been detected.
5	DISCON	0	Session Disconnect
		1	No interrupt
			A Device disconnect has been detected.
4	CONN	0	Session Connect
		1	No interrupt
			A Device connection has been detected.
3	SOF	0	Start of Frame
		1	No interrupt
			A new frame has started.
2	BABBLE	0	Babble Detected
		1	No interrupt
			Babble has been detected. This interrupt is active only after the first SOF has been sent.
1	RESUME	0	RESUME Signaling Detected. This interrupt can only be used if the USB controller's system clock is enabled. If the user disables the clock programming, the USBDRRIS, USBDRIM, and USBDRISC registers should be used.
		1	No effect
			RESUME signaling has been detected on the bus while the USB controller is in SUSPEND mode.
0	Reserved	0	Reserved

USBIS in Device Mode is shown in [Figure 21-11](#) and described in [Table 21-12](#).

Figure 21-11. USB General Interrupt Status Register (USBIS) in Device Mode

7	6	5	4	3	2	1	0
Reserved	DISCON	Reserved	SOF	RESET	RESUME	SUSPEND	
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-12. USB General Interrupt Status Register (USBIS) in Device Mode Field Descriptions

Bit	Field	Value	Description
7-6	Reserved	0	Reserved
5	DISCON	0	Session Disconnect
		1	No interrupt
		1	The device has been disconnected from the host.
4	Reserved	0	Reserved
3	SOF	0	Start of frame
		0	No interrupt
		1	A new frame has started.
2	RESET	0	RESET Signaling Detected
		1	No interrupt
		1	RESET signaling has been detected on the bus.
1	RESUME	0	RESUME Signaling Detected. This interrupt can only be used if the USB controller's system clock is enabled. If the user disables the clock programming, the USBDRRIS, USBDRIM, and USBDRISC registers should be used.
		0	No interrupt
		1	RESUME signaling has been detected on the bus while the USB controller is in SUSPEND mode.
0	SUSPEND	0	SUSPEND Signaling Detected
		0	No interrupt
		1	SUSPEND signaling has been detected on the bus.

21.6.8 USB Interrupt Enable Register (USBIE), offset 0x00B

NOTE: Use caution when reading this register. Performing a read may change bit status.

The USB interrupt enable 8-bit register (USBIE) provides interrupt enable bits for each of the interrupts in USBIS. At reset interrupts 1 and 2 are enabled in device mode.

Mode(s): Host Device

USBIE in Host Mode is shown in [Figure 21-12](#) and described in [Table 21-13](#).

Figure 21-12. USB Interrupt Enable Register (USBIE) in Host Mode

7	6	5	4	3	2	1	0
VBUSERR	SESREQ	DISCON	CONN	SOF	BABBLE	RESUME	Reserved
R-W	R-W	R-W	R-W	R-W	R-W	R-W	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-13. USB Interrupt Enable Register (USBIE) in Host Mode Field Descriptions

Bit	Field	Value	Description
7	VBUSERR	0	Enable VBUS Error Interrupt
		1	The VBUSERR interrupt is suppressed and not sent to the interrupt controller. An interrupt is sent to the interrupt controller when the VBUSERR bit in the USBIS register is set.
6	SESREQ	0	Enable Session Request
		1	The SESREQ interrupt is suppressed and not sent to the interrupt controller. An interrupt is sent to the interrupt controller when the SESREQ bit in the USBIS register is set.
5	DISCON	0	Enable Disconnect Interrupt
		1	The DISCON interrupt is suppressed and not sent to the interrupt controller. An interrupt is sent to the interrupt controller when the DISCON bit in the USBIS register is set.
4	CONN	0	Enable Connect Interrupt
		1	The CONN interrupt is suppressed and not sent to the interrupt controller. An interrupt is sent to the interrupt controller when the CONN bit in the USBIS register is set.
3	SOF	0	Start of Frame
		1	The SOF interrupt is suppressed and not sent to the interrupt controller. An interrupt is sent to the interrupt controller when the SOF bit in the USBIS register is set.
2	BABBLE	0	Babble Detected
		1	The BABBLE interrupt is suppressed and not sent to the interrupt controller. An interrupt is sent to the interrupt controller when the BABBLE bit in the USBIS register is set.
1	RESUME	0	RESUME Signaling Detected. This interrupt can only be used if the USB controller's system clock is enabled. If the user disables the clock programming, the USBDRRIS, USBDRIM, and USBDRISC registers should be used.
		1	The RESUME interrupt is suppressed and not sent to the interrupt controller. An interrupt is sent to the interrupt controller when the RESUME bit in the USBIS register is set.
0	Reserved	0	Reserved

USBIE in Device Mode is shown in [Figure 21-11](#) and described in [Table 21-12](#).

Figure 21-13. USB Interrupt Enable Register (USBIE) in Device Mode

7	6	5	4	3	2	1	0
Reserved	DISCON	Reserved	SOF	RESET	RESUME	SUSPEND	
R-0	R/W-0	R-0	R/W-0	R/W-1	RW-1	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-14. USB Interrupt Enable Register (USBIE) in Device Mode Field Descriptions

Bit	Field	Value	Description
7-6	Reserved	0	Reserved
5	DISCON	0	Enable Disconnect Interrupt
		1	The DISCON interrupt is suppressed and not sent to the interrupt controller.
		1	An interrupt is sent to the interrupt controller when the DISCON bit in the USBIS register is set.
4	Reserved	0	Reserved
3	SOF	0	Start of frame
		0	The SOF interrupt is suppressed and not sent to the interrupt controller.
		1	An interrupt is sent to the interrupt controller when the SOF bit in the USBIS register is set.
2	RESET	0	RESET Signaling Detected
		0	The RESET interrupt is suppressed and not sent to the interrupt controller.
		1	An interrupt is sent to the interrupt controller when the RESET bit in the USBIS register is set.
1	RESUME	0	RESUME Signaling Detected. This interrupt can only be used if the USB controller's system clock is enabled. If the user disables the clock programming, the USBDRRIS, USBDRIM, and USBDRISC registers should be used.
		0	The RESUME interrupt is suppressed and not sent to the interrupt controller.
		1	An interrupt is sent to the interrupt controller when the RESUME bit in the USBIS register is set.
0	SUSPEND	0	SUSPEND Signaling Detected
		0	The SUSPEND interrupt is suppressed and not sent to the interrupt controller.
		1	An interrupt is sent to the interrupt controller when the DISCON bit in the USBIS register is set.

21.6.9 USB Frame Value Register (USBFRAME), offset 0x00C

The frame number 16-bit read-only register (USBFRAME) holds the last received frame number.

Mode(s): Host Device

USBFRAME is shown in [Figure 21-14](#) and described in [Table 21-15](#).

Figure 21-14. Frame Number Register (FRAME)

15	11	10	0
Reserved			FRAME
R-0			R-0

LEGEND: R = Read only; -n = value after reset

Table 21-15. Frame Number Register (FRAME) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	FRAME	0-7FFh	Last received frame number

21.6.10 USB Endpoint Index Register (USBEPIDX), offset 0x00E

Each endpoint buffer can be accessed by configuring a FIFO size and starting address. The endpoint index 16-bit register (USBEPIDX) is used with the USBTXFIFOSZ, USBRXFIFOSZ, USBTXFIFOADD, and USBRXFIFOADD registers.

Mode(s): Host Device

USBEPIDX is shown in [Figure 21-15](#) and described in [Table 21-16](#).

Figure 21-15. USB Endpoint Index Register (USBEPIDX)

7	4	3	0
Reserved			EPIIDX
R-0			R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-16. USB Endpoint Index Register (USBEPIDX) Field Descriptions

Bit	Field	Value	Description
7-4	Reserved	0	Reserved
3-0	EPIIDX	0-4h	Endpoint Index. This bit field configures which endpoint is accessed when reading or writing to one of the USB controller's indexed registers. A value of 0x0 corresponds to Endpoint 0 and a value of 0xF corresponds to Endpoint 15.

21.6.11 USB Test Mode Register (USBTEST), offset 0x00F

The USB test mode 8-bit register (USBTEST) is primarily used to put the USB controller into one of the four test modes for operation described in the USB Specification 2.0 , in response to a SET FEATURE: USBTESTMODE command. This register is not used in normal operation.

Note: Only one of these bits should be set at any time.

Mode(s): Host Device

USBTEST in Host Mode is shown in [Figure 21-16](#) and described in [Table 21-17](#).

Figure 21-16. USB Test Mode Register (USBTEST) in Host Mode

7	6	5	4	0
FORCEH	FIFOACC	FORCEFS		Reserved
R/W-0	R/W1S-0	R/W-0		R-0

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 21-17. USB Test Mode Register (USBTEST) in Host Mode Field Descriptions

Bit	Field	Value	Description
7	FORCEH	0	Force Host Mode. While in this mode, status of the bus connection may be read using the DEV bit of the USBDEVCTL register. The operating speed is determined from the FORCEFS bit.
		1	No effect
6	FIFOACC	0	Forces the USB controller to enter Host mode when the SESSION bit is set, regardless of whether the USB controller is connected to any peripheral. The state of the USBD0P and USBD0M signals is ignored. The USB controller then remains in Host mode until the SESSION bit is cleared, even if a Device is disconnected. If the FORCEH bit remains set, the USB controller re-enters Host mode the next time the SESSION bit is set.
		1	Transfers the packet in the endpoint 0 transmit FIFO to the endpoint 0 receive FIFO.
5	FORCEFS	0	Force Full-Speed Mode
		1	The USB controller operates at Low Speed.
4-0	Reserved	0	Forces the USB controller into Full-Speed mode upon receiving a USB RESET.

USBTEST in Device Mode is shown in [Figure 21-17](#) and described in [Table 21-18](#).

Figure 21-17. USB Test Mode Register (USBTEST) in Device Mode

7	6	5	4	0
Reserved	FIFOACC	FORCEFS		Reserved
R-0	R/W1S-0	R/W-0		R-0

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 21-18. USB Test Mode Register (USBTEST) in Device Mode Field Descriptions

Bit	Field	Value	Description
7	Reserved		Force Host Mode. While in this mode, status of the bus connection may be read using the DEV bit of the USBDEVCTL register. The operating speed is determined from the FORCEFS bit.
6	FIFOACC	0	FIFO Access
		1	No effect
		1	Transfers the packet in the endpoint 0 transmit FIFO to the endpoint 0 receive FIFO.

Table 21-18. USB Test Mode Register (USBTEST) in Device Mode Field Descriptions (continued)

Bit	Field	Value	Description
5	FORCEFS	0	Force Full-Speed Mode The USB controller operates at Low Speed.
		1	Forces the USB controller into Full-Speed mode upon receiving a USB RESET.
4-0	Reserved	0	Reserved

21.6.12 USB FIFO Endpoint n Register (USBFIFO[0]-USBFIFO[3])

NOTE: Use caution when reading these registers. Performing a read may change bit status.

The USB FIFO endpoint n 32-bit registers (USBFIFO[n]) provide an address for CPU access to the FIFOs for each endpoint. Writing to these addresses loads data into the Transmit FIFO for the corresponding endpoint. Reading from these addresses unloads data from the Receive FIFO for the corresponding endpoint.

Transfers to and from FIFOs can be 8-bit, 16-bit or 32-bit as required, and any combination of accesses is allowed provided the data accessed is contiguous. All transfers associated with one packet must be of the same width so that the data is consistently byte-, halfword- or word-aligned. However, the last transfer may contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

Depending on the size of the FIFO and the expected maximum packet size, the FIFOs support either single-packet or double-packet buffering (see *Single-Packet Buffering* in [Section 21.3.1.1.2](#)). Burst writing of multiple packets is not supported as flags must be set after each packet is written.

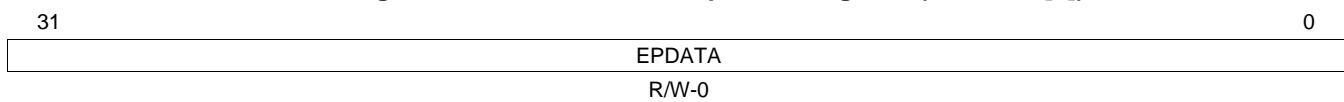
Following a STALL response or a transmit error on endpoint 1–3, the associated FIFO is completely flushed.

For the specific offset for each FIFO register see [Table 21-3](#).

Mode(s): Host Device

USBFIFO0-3 are shown in [Figure 21-18](#) and described in [Table 21-19](#).

Figure 21-18. USB FIFO Endpoint n Register (USBFIFO[n])



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-19. USB FIFO Endpoint n Register (USBFIFO[n]) Field Descriptions

Bit	Field	Reset	Description
31-0	EPDATA	0x0000.0000	Endpoint Data. Writing to this register loads the data into the Transmit FIFO and reading unloads data from the Receive FIFO.

21.6.13 USB Device Control Register (USBDEVCTL), offset 0x060

The USB device control 8-bit register (USBDEVCTL) is used for controlling and monitoring the USB VBUS line. If the PHY is suspended, no PHY clock is received and the VBUS is not sampled. In addition, in Host mode, USBDEVCTL provides the status information for the current operating mode (Host or Device) of the USB controller. If the USB controller is in Host mode, this register also indicates if a full- or low-speed Device has been connected.

Mode(s): Host Device

USBDEVCTL is shown in [Figure 21-19](#) and described in [Table 21-20](#).

Figure 21-19. USB Device Control Register (USBDEVCTL)

7	6	5	4	3	2	1	0
DEV	FSDEV	LSDEV		VBUS	HOSTMODE	HOSTREQ	SESSION
R-1	R-0	R-0		R-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-20. USB Device Control Register (USBDEVCTL) Field Descriptions

Bit	Field	Value	Description
7	DEV	0 1	Device mode The USB controller is operating on the OTG A side of the cable. The USB controller is operating on the OTG B side of the cable. Only valid while a session is in progress.
6	FSDEV	0 1	Full-Speed Device Detected A full-speed Device has not been detected on the port. A full-speed Device has been detected on the port.
5	LSDEV	0 1	Low-Speed Device Detected A low-speed Device has not been detected on the port. A low-speed Device has been detected on the port.
4-3	VBUS	0-3h 0 1h 2h 3h	These read-only bits encode the current VBus level as follows: 0 Below Session End. VBUS is detected as under 0.5 V. 1h Above Session End, below AValid. VBUS is detected as above 0.5 V and under 1.5 V. 2h Above AValid, below VBusValid. VBUS is detected as above 1.5 V and below 4.75 V. 3h Above VBusValid. VBUS is detected as above 4.75 V.
2	HOSTMODE	0 1	This read-only bit is set when the USB controller is acting as a Host. The USB controller is acting as a Device. The USB controller is acting as a Host. Only valid while a session is in progress.
1	HOSTREQ	0 1	When set, the USB controller will initiate the Host Negotiation when Suspend mode is entered. It is cleared when Host Negotiation is completed. No effect Initiates the Host Negotiation when SUSPENDmode is entered.

Table 21-20. USB Device Control Register (USBDEVCTL) Field Descriptions (continued)

Bit	Field	Value	Description
0	SESSION		<p>Session Start/End When operating as a Host:</p> <p>0 When cleared by software, this bit ends a session.</p> <p>1 When set by software, this bit starts a session.</p> <p>When operating as a Device:</p> <p>0 The USB controller has ended a session. When the USB controller is in SUSPEND mode, this bit may be cleared by software to perform a software disconnect.</p> <p>1 The USB controller has started a session. When set by software, the Session Request Protocol is initiated.</p> <p>Clearing this bit when the USB controller is not suspended results in undefined behavior.</p>

21.6.14 USB Transmit Dynamic FIFO Sizing Register (USBTXFIFOSZ), offset 0x062

The USB transmit dynamic FIFO sizing 8-bit register (USBTXFIFOSZ) allows the selected TX endpoint FIFOs to be dynamically sized. USBEPIIDX is used to configure each transmit endpoint's FIFO size.

Mode(s): Host Device

USBTXFIFOSZ is shown in [Figure 21-20](#) and described in [Table 21-21](#).

Figure 21-20. USB Transmit Dynamic FIFO Sizing Register (USBTXFIFOSZ)

7	5	4	3	0
Reserved		DPB		SZ
R-0		R/W-0		R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-21. USB Transmit Dynamic FIFO Sizing Register (USBTXFIFOSZ) Field Descriptions

Bit	Field	Value	Description
7-5	Reserved	0	Reserved
4	DPB	0	Double Packet Buffering Support Single packet buffering is supported.
3-0	SZ	1	Double packet buffering is enabled.
			Maximum packet size to be allowed. If DPB = 0, the FIFO also is this size; if DPB = 1, the FIFO is twice this size. Packet size in bytes:
		0h	8
		1h	16
		2h	32
		3h	64
		4h	128
		5h	256
		6h	512
		7h	1024
		8h	2048
		9-Fh	Reserved

21.6.15 USB Receive Dynamic FIFO Sizing Register (USBRXFIFOSZ), offset 0x063

The USB receive dynamic FIFO sizing 8-bit register (USBRXFIFOSZ) allows the selected RX endpoint FIFOs to be dynamically sized.

Mode(s): Host Device

USBRXFIFOSZ is shown in [Figure 21-21](#) and described in [Table 21-22](#).

Figure 21-21. USB Receive Dynamic FIFO Sizing Register (USBRXFIFOSZ)

7	5	4	3	0
Reserved		DPB		SZ

R-0 R/W-0 R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-22. USB Receive Dynamic FIFO Sizing Register (USBRXFIFOSZ) Field Descriptions

Bit	Field	Value	Description
7-5	Reserved	0	Reserved
4	DPB	0	Double Packet Buffering Support Single packet buffering is supported.
		1	Double packet buffering is enabled.
3-0	SZ		Maximum packet size to be allowed. If DPB = 0, the FIFO also is this size; if DPB = 1, the FIFO is twice this size. Packet size in bytes: 0h 8 1h 16 2h 32 3h 64 4h 128 5h 256 6h 512 7h 1024 8h 2048 9-Fh Reserved

21.6.16 USB Transmit FIFO Start Address Register (USBTXFIFOADD), offset 0x064

The USB transmit FIFO start address 16-bit register (USBTXFIFOADD) controls the start address of the selected transmit endpoint FIFOs.

Mode(s): Host Device

USBTXFIFOADDR is shown in [Figure 21-22](#) and described in [Table 21-23](#).

Figure 21-22. USB Transmit FIFO Start Address Register (USBTXFIFOADDR)]

15	9	8	0
Reserved			ADDR
R-0			R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-23. USB Transmit FIFO Start Address Register (USBTXFIFOADDR) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	ADDR	0h 1h 2h 3h 4h 5h 6h 7h 8h .. 1FFh	Start Address of the endpoint FIFO in units of 8 bytes. 0 8 16 24 32 40 48 56 64 .. 4095

21.6.17 USB Receive FIFO Start Address Register (USBRXFIFOADD), offset 0x066

The USB receive FIFO start address 16-bit register (USBRXFIFOADD) controls the start address of the selected receive endpoint FIFOs.

Mode(s): Host Device

USBRXFIFOADDR is shown in [Figure 21-23](#) and described in [Table 21-24](#).

Figure 21-23. USB Receive FIFO Start Address Register (USBRXFIFOADDR)

15	9	8	0
Reserved			ADDR
R-0			R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-24. USB Receive FIFO Start Address Register (USBRXFIFOADDR) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	ADDR	0h 0 1h 8 2h 16 3h 24 4h 32 5h 40 6h 48 7h 56 8h 64 1FFh 4095	Start Address of the endpoint FIFO in units of 8 bytes.

21.6.18 USB Connect Timing Register (USBCONTIM), offset 0x07A

The USB connect timing 8-bit configuration register (USBCONTIM) specifies connection and negotiation delays.

Mode(s): Host Device

USBCONTIM is shown in [Figure 21-24](#) and described in [Table 21-25](#).

Figure 21-24. USB Connect Timing Register (USBCONTIM)

7	4	3	0
WTCON			WTID
R/W-1			R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-25. USB Connect Timing Register (USBCONTIM) Field Descriptions

Bit	Field	Value	Description
7-4	WTCON	5h	The connect wait field configures the wait required to allow for the user's connect/disconnect filter, in units of 533.3 ns. The default corresponds to 2.667 μ s.
3-0	WTID	Ch	The wait ID field configures the delay required from the enable of the ID detection to when the ID value is valid, in units of 4.369 ms. The default corresponds to 52.43 ms.

21.6.19 USB Full-Speed Last Transaction to End of Frame Timing Register (USBFSEOF), offset 0x07D

USB full-speed last transaction to end of frame timing 8-bit configuration register (USBFSEOF) specifies the minimum time gap allowed between the start of the last transaction and the EOF for full-speed transactions.

Mode(s): Host Device

USBFSEOF is shown in [Figure 21-25](#) and described in [Table 21-26](#).

Figure 21-25. USB Full-Speed Last Transaction to End of Frame Timing Register (USBFSEOF)

7	FSEOFG	0
R/W-0x77		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-26. USB Full-Speed Last Transaction to End of Frame Timing Register (USBFSEOF) Field Descriptions

Bit	Field	Reset	Description
7-0	FSEOFG	77h	The full-speed end-of-frame gap field is used during full-speed transactions to configure the gap between the last transaction and the End-of-Frame (EOF), in units of 533.3 ns. The default corresponds to 63.46 µs.

21.6.20 USB Low-Speed Last Transaction to End of Frame Timing Register (USBLSEOF), offset 0x07E

The USB low-speed last transaction to end of frame timing 8-bit configuration register (USBLSEOF) specifies the minimum time gap that is to be allowed between the start of the last transaction and the EOF for low-speed transactions.

Mode(s): Host Device

USBLSEOF is shown in [Figure 21-26](#) and described in [Table 21-27](#).

Figure 21-26. USB Low-Speed Last Transaction to End of Frame Timing Register (USBLSEOF)

7	LSEOFG	0
R/W-0x72		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-27. USB Low-Speed Last Transaction to End of Frame Timing Register (USBLSEOF) Field Descriptions

Bit	Field	Reset	Description
7-0	LSEOFG	72h	The low-speed end-of-frame gap field is used during low-speed transactions to set the gap between the last transaction and the End-of-Frame (EOF), in units of 1.067 µs. The default corresponds to 121.6 µs.

21.6.21 USB Transmit Functional Address Endpoint n Registers (USBTXFUNCADDR[0]-USBTXFUNCADDR[3])

The transmit functional address endpoint n 8-bit registers (USBTXFUNCADDR[n]) record the address of the target function to be accessed through the associated endpoint (EP n). USBTXFUNCADDR x must be defined for each transmit endpoint that is used.

Note: USBTXFUNCADDR0 is used for both receive and transmit for endpoint 0.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBTXFUNCADDR[n] registers are shown in [Figure 21-27](#) and described in [Table 21-28](#).

Figure 21-27. USB Transmit Functional Address Endpoint n Registers (USBTXFUNCADDR[n])

7	6	0
Reserved		ADDR
R-0		R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-28. USB Transmit Functional Address Endpoint n Registers (USBTXFUNCADDR[n]) Field Descriptions

Bit	Field	Value	Description
7	Reserved	0	Reserved
6-0	ADDR	0	Device Address specifies the USB bus address for the target Device.

21.6.22 USB Transmit Hub Address Endpoint n Registers (USBTXHUBADDR[0]-USBTXHUBADDR[3])

The transmit hub address endpoint n 8-bit read/write registers (USBTXHUBADDR[n]), like USBTXHUBPORT[n], must be written only when a USB device is connected to transmit endpoint EP n via a USB 2.0 hub. This register records the address of the USB 2.0 hub through which the target associated with the endpoint is accessed.

Note: USBTXHUBADDR0 is used for both receive and transmit for endpoint 0.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBTXHUBADDR[n] registers are shown in [Figure 21-27](#) and described in [Table 21-28](#).

Figure 21-28. USB Transmit Hub Address Endpoint n Registers (USBTXHUBADDR[n])

7	6	0
Reserved		ADDR
R-0		R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-29. USB Transmit Hub Address Endpoint n Registers(USBTXHUBADDR[n]) Field Descriptions

Bit	Field	Value	Description
7	Reserved	0	Reserved
6-0	ADDR	0	Device Address specifies the USB bus address for the target Device.

21.6.23 USB Transmit Hub Port Endpoint n Registers (USBTXHUBPORT[0]-USBTXHUBPORT[3])

The transmit hub port endpoint n 8-bit read/write registers (USBTXHUBPORT[n]), like USBTXHUBADDR[n], must be written only when a full- or low-speed Device is connected to transmit endpoint EP n via a USB 2.0 hub. This register records the port of the USB 2.0 hub through which the target associated with the endpoint is accessed.

Note: USBTXHUBPORT0 is used for both receive and transmit for endpoint 0.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBTXHUBPORT n registers are shown in [Figure 21-29](#) and described in [Table 21-30](#).

Figure 21-29. USB Transmit Hub Port Endpoint n Registers (USBTXHUBPORT[n])

7	6	0
Reserved		PORt
R-0		R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

**Table 21-30. USB Transmit Hub Port Endpoint n Registers(USBTXHUBPORT[n])
Field Descriptions**

Bit	Field	Value	Description
7	Reserved	0	Reserved
6-0	PORT	0	Hub Port specifies the USB hub port number.

21.6.24 USB Receive Functional Address Endpoint n Registers (USBRXFUNCADDR[1]-USBRXFUNCADDR[3])

The receive functional address endpoint n 8-bit read/write registers (USBRXFUNCADDR[n]) record the address of the target function to be accessed through the associated endpoint (EP n). USBRХFUNCADDR x must be defined for each receive endpoint that is used.

Note: USBTXFUNCADDR0 is used for both receive and transmit for endpoint 0.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBRХFUNCADDR[n] registers are shown in [Figure 21-30](#) and described in [Table 21-31](#).

Figure 21-30. USB Receive Functional Address Endpoint n Registers (USBFIFO[n])

7	6	0
Reserved		ADDR
R-0		R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-31. USB Recieve Functional Address Endpoint n Registers(USBFIFO[n]) Field Descriptions

Bit	Field	Value	Description
7	Reserved	0	Reserved
6-0	ADDR	0	Device Address specifies the USB bus address for the target Device.

21.6.25 USB Receive Hub Address Endpoint n Registers (USBRXHUBADDR[1]-USBRXHUBADDR[3])

The receive hub address endpoint n 8-bit read/write registers (USBRXHUBADDR[n]), like [n], must be written only when a full- or low-speed Device is connected to receive endpoint EP n via a USB 2.0 hub. Each register records the address of the USB 2.0 hub through which the target associated with the endpoint is accessed.

Note: USBTXHUBADDR0 is used for both receive and transmit for endpoint 0.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBRXHUBADDR[n] registers are shown in [Figure 21-31](#) and described in [Table 21-32](#).

Figure 21-31. USB Receive Hub Address Endpoint n Registers (USBRXHUBADDR[n])

7	6	0
MULTTRAN		ADDR
R/w-0		R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-32. USB Receive Hub Address Endpoint n Registers(USBRXHUBADDR[n]) Field Descriptions

Bit	Field	Value	Description
7	MULTTRAN	0	Multiple Translators
			Clear to indicate that the hub has a single transaction translator.
			Set to indicate that the hub has multiple transaction translators.
6-0	ADDR	0	Device Address specifies the USB bus address for the target Device.

21.6.26 USB Receive Hub Port Endpoint n Registers (USBRXHUBPORT[1]-USBRXHUBPORT[3])

The receive hub port endpoint n 8-bit read/write registers (USBRXHUBPORT[n]), like USBRXHUBADDR[n], must be written only when a full- or low-speed device is connected to receive endpoint EP n via a USB 2.0 hub. Each register records the port of the USB 2.0 hub through which the target associated with the endpoint is accessed.

Note: USBTXHUBPORT0 is used for both receive and transmit for endpoint 0.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBRXHUBPORT n registers are shown in [Figure 21-32](#) and described in [Table 21-33](#).

Figure 21-32. USB Transmit Hub Port Endpoint n Registers (USBRXHUBPORT[n])

7	6	0
Reserved		PORt
R-0		R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-33. USB Transmit Hub Port Endpoint n Registers(USBRXHUBPORT[n]) Field Descriptions

Bit	Field	Value	Description
7	Reserved	0	Reserved
6-0	PORT	0	Hub Port specifies the USB hub port number.

21.6.27 USB Maximum Transmit Data Endpoint n Registers (USBTXMAXP[1]-USBTXMAXP[3])

The USB maximum transmit data endpoint n 16-bit registers (USBTXMAXP[n]) define the maximum amount of data that can be transferred through the selected transmit endpoint in a single operation.

Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the *USB Specification* on packet sizes for bulk, interrupt and isochronous transfers in full-speed operation.

The total amount of data represented by the value written to this register must not exceed the FIFO size for the transmit endpoint, and must not exceed half the FIFO size if double-buffering is required.

If this register is changed after packets have been sent from the endpoint, the transmit endpoint FIFO must be completely flushed (using the FLUSH bit in USBTXCSRLn) after writing the new value to this register.

Note: USBTXMAXP[n] must be set to an even number of bytes for proper interrupt generation in DMA Basic Mode.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host Device

The USBTXMAXP[n] registers are shown in [Figure 21-33](#) and described in [Table 21-34](#).

Figure 21-33. USB Maximum Transmit Data Endpoint n Registers (USBTXMAXP[n])

15	11	10	0
Reserved		MAXLOAD	
R-0		R/W-000	

LEGEND: R/W = Read/Write; R = Read only; - n = value after reset

Table 21-34. USB Maximum Transmit Data Endpoint n Registers(USBTXMAXP[n]) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	MAXLOAD		Maximum Payload specifies the maximum payload in bytes per transaction.

21.6.28 USB Control and Status Endpoint 0 Low Register (USBCSRL0), offset 0x102

The USB control and status endpoint 0 low 8-bit register (USBCSRL0) provides control and status bits for endpoint 0.

Mode(s): Host Device

USBCSRL0 in Host mode is shown in Figure 21-34 and described in Table 21-35.

Figure 21-34. USB Control and Status Endpoint 0 Low Register (USBCSRL0) in Host Mode

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-35. USB Control and Status Endpoint 0 Low Register(USBCSRL0) in Host Mode Field Descriptions

Bit	Field	Value	Description
7	NAKTO	0	NAK Timeout. Software must clear this bit to allow the endpoint to continue.
		1	No timeout
		1	Indicates that endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the USBNAKLMT register.
6	STATUS	0	Status Packet. Setting this bit ensures that the DT bit is set in the USBCSRH0 register so that a DATA1 packet is used for the STATUS stage transaction.
		0	No transaction
		1	Initiates a STATUS stage transaction. This bit must be set at the same time as the TXRDY or REQPKT bit is set. This bit is automatically cleared when the STATUS stage is over.
5	REQPKT	0	Request Packet. This bit is cleared when the RXRDY bit is set.
		0	No request
		1	Requests an IN transaction.
4	ERROR	0	Error. Software must clear this bit.
		0	No error
		1	Three attempts have been made to perform a transaction with no response from the peripheral. The EP0 bit in the USBTXIS register is also set in this situation.
3	SETUP	0	Setup Packet. Setting this bit always clears the DT bit in the USBCSRH0 register to send a DATA0 packet.
		0	Sends an OUT token.
		1	Sends a SETUP token instead of an OUT token for the transaction. This bit should be set at the same time as the TXRDY bit is set.
2	STALLED	0	Endpoint Stalled. Software must clear this bit.
		0	No handshake has been received.
		1	A STALL handshake has been received.
1	TXRDY	0	Transmit Packet Ready. If both the TXRDY and SETUP bits are set, a setup packet is sent. If just TXRDY is set, an OUT packet is sent.
		0	No transmit packet is ready.
		1	Software sets this bit after loading a data packet into the TX FIFO. The EP0 bit in the USBTXIS register is also set in this situation.
0	RXRDY	0	Receive Packet Ready. Software must clear this bit after the packet has been read from the FIFO to acknowledge that the data has been read from the FIFO.
		0	No receive packet has been received.
		1	Indicates that a data packet has been received in the RX FIFO. The EP0 bit in the USBTXIS register is also set in this situation.

USBCSRL0 in Device mode is shown in [Figure 21-35](#) and described in [Table 21-36](#).

Figure 21-35. USB Control and Status Endpoint 0 Low Register (USBCSRL0) in Device Mode

7	6	5	4	3	2	1	0
SETENDC	RXRDYC	STALL	SETEND	DATAEND	STALLED	TXRDY	RXRDY
W1C-0	W1C-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-36. USB Control and Status Endpoint 0 Low Register (USBCSRL0) in Device Mode Field Descriptions

Bit	Field	Value	Description
7	SETENDC	0	Setup End Clear
		1	No effect
		1	Writing a 1 to this bit clears the SETEND bit.
6	RXRDYC	0	RXRDY Clear
		1	No effect
		1	Writing a 1 to this bit clears the RXRDY bit.
5	STALL	0	Send Stall.
		1	No effect
		1	Terminates the current transaction and transmits the STALL handshake. This bit is cleared automatically after the STALL handshake is transmitted.
4	SETEND	0	Setup end. A control transaction has not ended or ended after the DATAEND bit was set.
		1	A control transaction has ended before the DATAEND bit has been set. The EP0 bit in the USBTXIS register is also set in this situation. This bit is cleared by writing a 1 to the SETENDC bit.
		1	
3	DATAEND	0	Data end. No effect
		1	Set this bit in the following situations: <ul style="list-style-type: none">• When setting TXRDY for the last data packet• When clearing RXRDY after unloading the last data packet• When setting TXRDY for a zero-length data packet This bit is cleared automatically.
		1	
2	STALLED	0	Endpoint Stalled. Software must clear this bit. A STALL handshake has not been transmitted.
		1	A STALL handshake has been transmitted.
		1	
1	TXRDY	0	Transmit Packet Ready. If both the TXRDY and SETUP bits are set, a setup packet is sent. If just TXRDY is set, an OUT packet is sent. No transmit packet is ready.
		1	Software sets this bit after loading an IN data packet into the TX FIFO. The EP0 bit in the USBTXIS register is also set in this situation.
		1	
0	RXRDY	0	Receive Packet Ready. No receive packet has been received.
		1	A data packet has been received. The EP0 bit in the USBTXIS register is also set in this situation. This bit is cleared by writing a 1 to the RXRDYC bit.
		1	

21.6.29 USB Control and Status Endpoint 0 High Register (USBCSRH0), offset 0x103

The USB control and status endpoint 0 high 8-bit register (USBCSRH0) provides control and status bits for endpoint 0.

Mode(s): Host Device

USBCSRH0 in Host mode is shown in [Figure 21-36](#) and described in [Table 21-37](#).

Figure 21-36. USB Control and Status Endpoint 0 High Register (USBCSRH0) in Host Mode

7	3	2	1	0
	Reserved		DTWE	DT
	R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-37. USB Control and Status Endpoint 0 High Register (USBCSRH0) in Host Mode Field Descriptions

Bit	Field	Value	Description
7-3	Reserved	0	Reserved
2	DTWE	0	Data Toggle Write Enable. This bit is automatically cleared once the new value is written.
		1	The DT bit cannot be written.
1	DT		Enables the current state of the endpoint 0 data toggle to be written (see DT bit).
0	FLUSH		Data Toggle. When read, this bit indicates the current state of the endpoint 0 data toggle.
			If DTWE is set, this bit may be written with the required setting of the data toggle. If DTWE is Low, this bit cannot be written. Care should be taken when writing to this bit as it should only be changed to RESET USB endpoint 0.
		0	Flush FIFO. This bit is automatically cleared after the flush is performed.
		1	No effect
			Flushes the next packet to be transmitted/read from the endpoint 0 FIFO. The FIFO pointer is reset and the TXRDY/RXRDY bit is cleared.
			Note: This bit should only be set when TXRDY/RXRDY is set. At other times, it may cause data to be corrupted.

USBCSRH0 in Device mode is shown in [Figure 21-37](#) and described in [Table 21-38](#).

Figure 21-37. USB Control and Status Endpoint 0 High Register (USBCSRH0) in Device Mode

7	1	0
	Reserved	
	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-38. USB Control and Status Endpoint 0 High Register (USBCSRH0) in Device Mode Field Descriptions

Bit	Field	Value	Description
7-1	Reserved	0	Reserved
0	FLUSH	0	Flush FIFO. This bit is automatically cleared after the flush is performed.
		1	No effect
0			Flushes the next packet to be transmitted/read from the endpoint 0 FIFO. The FIFO pointer is reset and the TXRDY/RXRDY bit is cleared.
			Note: This bit should only be set when TXRDY/RXRDY is set. At other times, it may cause data to be corrupted.

21.6.30 USB Receive Byte Count Endpoint 0 Register (USBCOUNT0), offset 0x108

The USB receive byte count endpoint 0 8-bit read-only register (USBCOUNT0) indicates the number of received data bytes in the endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while the RXRDY bit is set.

Mode(s): Host Device

USBCOUNT0 is shown in [Figure 21-38](#) and described in [Table 21-28](#).

Figure 21-38. USB Receive Byte Count Endpoint 0 Register (USBCOUNT0)

7	6	0
Reserved	COUNT	
R-0		R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-39. USB Receive Byte Count Endpoint 0 Register (USBCOUNT0) Field Descriptions

Bit	Field	Value	Description
7	Reserved	0	Reserved
6-0	COUNT	0	FIFO Count. COUNT is a read-only value that indicates the number of received data bytes in the endpoint 0 FIFO.

21.6.31 USB Type Endpoint 0 Register (USBTYPE0), offset 0x10A

The USB type endpoint 0 8-bit register (USBTYPE0) must be written with the operating speed of the targeted Device being communicated with using endpoint 0.

Mode(s): Host

USBTYPE0 is shown in [Figure 21-39](#) and described in [Table 21-40](#).

Figure 21-39. USB Type Endpoint 0 Register (USBTYPE0)

7	6	5	0
SPEED		Reserved	
R/W-0		R-0	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-40. USB Type Endpoint 0 Register (USBTYPE0) Field Descriptions

Bit	Field	Value	Description
7-6	SPEED	0	Operating Speed specifies the operating speed of the target Device. If selected, the target is assumed to have the same connection speed as the USB controller.
		0-1h	Reserved
		2h	Full
		3h	Low
5-0	Reserved	0	Reserved

21.6.32 USB NAK Limit Register (USBNAKLMT), offset 0x10B

The USB NAK limit 8-bit read-only register (USBNAKLMT) sets the number of frames after which endpoint 0 should time out on receiving a stream of NAK responses. (Equivalent settings for other endpoints can be made through their USBTXINTERVAL[n] and USBRXINTERVAL[n] registers.)

The number of frames selected is $2(m-1)$ (where m is the value set in the register, with valid values of 2–16). If the Host receives NAK responses from the target for more frames than the number represented by the limit set in this register, the endpoint is halted.

Note: A value of 0 or 1 disables the NAK timeout function.

Mode(s): Host

USBNAKLMT is shown in [Figure 21-40](#) and described in [Table 21-41](#).

Figure 21-40. USB NAK Limit Register (USBNAKLMT)

7	5	4	0
Reserved			NAKLMT
R-0			R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-41. USB NAK Limit Register (USBNAKLMT) Field Descriptions

Bit	Field	Value	Description
7-5	Reserved	0	Reserved
4-0	NAKLMT	0	EP0 NAK Limit specifies the number of frames after receiving a stream of NAK responses.

21.6.33 USB Transmit Control and Status Endpoint n Low Register (USBTXCSRL[1]-USBTXCSRL[3])

The USB transmit control and status endpoint n low 8-bit registers (USBTXCSRL[n]) provide control and status bits for transfers through the currently selected transmit endpoint.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host Device

The USBTXCSRL[n] registers in Host Mode are shown in [Figure 21-41](#) and described in [Table 21-42](#).

Figure 21-41. USB Transmit Control and Status Endpoint n Low Register (USBTXCSRL[n]) in Host Mode

7	6	5	4	3	2	1	0
NAKTO	CLRD _T	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-42. USB Transmit Control and Status Endpoint n Low Register (USBTXCSRL[n]) in Host Mode Field Descriptions

Bit	Field	Value	Description
7	NAKTO	0	NAK Timeout. Software must clear this bit to allow the endpoint to continue.
		1	Bulk endpoints only: Indicates that the transmit endpoint is halted following the receipt of NAK responses for longer than the time set by the NAKLMT field in the USBTXINTERVAL[n] register.
6	CLRD _T	0	Clear DataToggle
		1	Writing a 1 to this bit clears the DT bit in the USBTXCSR _H [n] register.
5	STALLED	0	Endpoint Stalled. Software must clear this bit.
		1	A STALL handshake has not been received Indicates that a STALL handshake has been received. When this bit is set, any DMA request that is in progress is stopped, the FIFO is completely flushed, and the TXRDY bit is cleared.
4	SETUP	0	Setup Packet.
		1	No SETUP token is sent. Sends a SETUP token instead of an OUT token for the transaction. This bit should be set at the same time as the TXRDY bit is set. Note: Setting this bit also clears the DT bit in the USBTXCSR _H [n] register.
3	FLUSH	0	Flush FIFO. This bit can be set simultaneously with the TXRDY bit to abort the packet that is currently being loaded into the FIFO. Note that if the FIFO is double-buffered, FLUSH may have to be set twice to completely clear the FIFO.
		1	No effect Flushes the latest packet from the endpoint transmit FIFO. The FIFO pointer is reset and the TXRDY bit is cleared. The EPn bit in the USBTXIS register is also set in this situation. Note: This bit should only be set when the TXRDY bit is set. At other times, it may cause data to be corrupted.
2	ERROR	0	Error. Software must clear this bit.
		1	No error Three attempts have been made to send a packet and no handshake packet has been received. The TXRDY bit is cleared, the EPn bit in the USBTXIS register is set, and the FIFO is completely flushed in this situation. Note: This bit is valid only when the endpoint is operating in Bulk or Interrupt mode.
1	FIFONE	0	FIFO Not Empty
		1	The FIFO is empty At least one packet is in the transmit FIFO.

Table 21-42. USB Transmit Control and Status Endpoint n Low Register (USBTXCSRL[n])**in Host Mode Field Descriptions (continued)**

Bit	Field	Value	Description
0	TXRDY		Transmit Packet Ready. This bit is cleared automatically when a data packet has been transmitted. The EPn bit in the USBTXIS register is also set at this point. TXRDY is also automatically cleared prior to loading a second packet into a double-buffered FIFO.
		0	No transmit packet is ready.
		1	Software sets this bit after loading a data packet into the TX FIFO.

The USBTXCSRL[n] registers in Device Mode are shown in [Table 21-42](#) and described in [Figure 21-42](#).

Figure 21-42. USB Transmit Control and Status Endpoint n Low Register (USBTXCSRL[n]) in Device Mode

7	6	5	4	3	2	1	0
Reserved	CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-43. USB Transmit Control and Status Endpoint n Low Register (USBTXCSRL[n]) in Device Mode Field Descriptions

Bit	Field	Value	Description
7	Reserved	0	Reserved
6	CLRDT	0	Clear Data Toggle
		1	No effect
		1	Writing a 1 to this bit clears the DT bit in the USBTXCSR[n] register.
5	STALLED	0	Endpoint Stalled. Software must clear this bit.
		1	A STALL handshake has not been transmitted.
		1	A STALL handshake has been transmitted. The FIFO is flushed and the TXRDY bit is cleared.
4	STALL		Send Stall. Software clears this bit to terminate the STALL condition. Note: This bit has no effect in isochronous transfers.
		0	No effect
		1	Issues a STALL handshake to an IN token.
3	FLUSH		Flush FIFO. This bit may be set simultaneously with the TXRDY bit to abort the packet that is currently being loaded into the FIFO. Note that if the FIFO is double-buffered, FLUSH may have to be set twice to completely clear the FIFO. Note: This bit should only be set when the TXRDY bit is set. At other times, it may cause data to be corrupted.
		0	No effect
		1	Flushes the latest packet from the endpoint transmit FIFO. The FIFO pointer is reset and the TXRDY bit is cleared. The EPn bit in the USBTXIS register is also set in this situation. This bit is cleared automatically.
2	UNDRN	0	Underrun. Software must clear this bit.
		1	No underrun
		1	An IN token has been received when TXRDY is not set.
1	FIFONE	0	FIFO Not Empty
		1	The FIFO is empty.
		1	At least one packet is in the transmit FIFO.

Table 21-43. USB Transmit Control and Status Endpoint n Low Register (USBTXCSRL[n])**in Device Mode Field Descriptions (continued)**

Bit	Field	Value	Description
0	TXRDY	0	Transmit Packet Ready. This bit is cleared automatically when a data packet has been transmitted. The EPn bit in the USBTXIS register is also set at this point. TXRDY is also automatically cleared prior to loading a second packet into a double-buffered FIFO.

21.6.34 USB Transmit Control and Status Endpoint n High Register (USBTXCSRH[1]-USBTXCSRH[3])

The USB transmit control and status endpoint n high 8-bit registers (USBTXCSRH[n]) provide additional control for transfers through the currently selected transmit endpoint.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host Device

The USBTXCSRH[n] registers in Host Mode are shown in [Figure 21-43](#) and described in [Table 21-44](#).

Figure 21-43. USB Transmit Control and Status Endpoint n High Register (USBTXCSRH[n]) in Host Mode

7	6	5	4	3	2	1	0
AUTOSET	Reserved	MODE	DMAEN	FDT	DMAMOD	DTWE	DT
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-44. USB Transmit Control and Status Endpoint n High Register (USBTXCSRH[n]) in Host Mode Field Descriptions

Bit	Field	Value	Description
7	AUTOSET	0	Auto Set The TXRDY bit must be set manually.
		1	Enables the TXRDY bit to be automatically set when data of the maximum packet size (value in USBTXMAXP[n]) is loaded into the transmit FIFO. If a packet of less than the maximum packet size is loaded, then the TXRDY bit must be set manually.
6	Reserved	0	Reserved
5	MODE	0	Mode Note: This bit only has an effect when the same endpoint FIFO is used for both transmit and receive transactions.
		1	Enables the endpoint direction as RX. Enables the endpoint direction as TX.
4	DMAEN	0	DMA Request Enable Note: Three TX and three /RX endpoints can be connected to the DMA module. If this bit is set for a particular endpoint, the DMAATX, DMABTX, or DMACTX field in the USB DMA Select (USBDMASEL) register must be programmed correspondingly.
		1	Disables the DMA request for the transmit endpoint. Enables the DMA request for the transmit endpoint.
3	FDT	0	Force Data Toggle No effect
		1	Forces the endpoint DT bit to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This bit can be used by interrupt transmit endpoints that are used to communicate rate feedback for isochronous endpoints. Note: This bit should only be set when the TXRDY bit is set. At other times, it may cause data to be corrupted.
2	DMAMOD	0	DMA Request Mode Note: This bit must not be cleared either before or in the same cycle as the above DMAEN bit is cleared. An interrupt is generated after every DMA packet transfer.
		1	An interrupt is generated only after the entire DMA transfer is complete. Note: This bit is valid only when the endpoint is operating in Bulk or Interrupt mode.
1	DTWE	0	Data Toggle Write Enable. This bit is automatically cleared once the new value is written. The DT bit cannot be written.
		1	Enables the current state of the transmit endpoint data to be written (see DT bit).

Table 21-44. USB Transmit Control and Status Endpoint n High Register (USBTXCSR[n])
in Host Mode Field Descriptions (continued)

Bit	Field	Value	Description
0	DT		Data Toggle. When read, this bit indicates the current state of the transmit endpoint data toggle. If DTWE is High, this bit can be written with the required setting of the data toggle. If DTWE is Low, any value written to this bit is ignored. Care should be taken when writing to this bit as it should only be changed to RESET the transmit endpoint.

The USBTXCSR[n] registers in Device Mode are shown in [Figure 21-44](#) and described in [Table 21-45](#).

Figure 21-44. USB Transmit Control and Status Endpoint n High Register (USBTXCSR[n]) in Device Mode

7	6	5	4	3	2	1	0
AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		Reserved

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-45. USB Transmit Control and Status Endpoint n High Register (USBTXCSR[n]) in Device Mode Field Descriptions

Bit	Field	Value	Description
7	AUTOSET	0	Auto Set The TXRDY bit must be set manually.
		1	Enables the TXRDY bit to be automatically set when data of the maximum packet size (value in USBTXMAXP[n]) is loaded into the transmit FIFO. If a packet of less than the maximum packet size is loaded, then the TXRDY bit must be set manually.
6	ISO	0	Isochronous Transfers Enables the transmit endpoint for bulk or interrupt transfers.
		1	Enables the transmit endpoint for isochronous transfers.
5	MODE	0	Mode Note: This bit only has an effect when the same endpoint FIFO is used for both transmit and receive transactions.
		1	Enables the endpoint direction as RX. Enables the endpoint direction as TX.
4	DMAEN	0	DMA Request Enable Note: Three TX and three RX endpoints can be connected to the DMA module. If this bit is set for a particular endpoint, the DMAATX, DMABTX, or DMACTX field in the USB DMA Select (USBDMASEL) register must be programmed correspondingly.
		1	Disables the DMA request for the transmit endpoint. Enables the DMA request for the transmit endpoint.
3	FDT	0	Force Data Toggle No effect
		1	Forces the endpoint DT bit to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This bit can be used by interrupt transmit endpoints that are used to communicate rate feedback for isochronous endpoints.
2	DMAMOD	0	DMA Request Mode Note: This bit must not be cleared either before or in the same cycle as the above DMAEN bit is cleared. An interrupt is generated after every DMA packet transfer.
		1	An interrupt is generated only after the entire DMA transfer is complete.
0	Reserved	0	Reserved

21.6.35 USB Maximum Receive Data Endpoint n Registers (USBRXMAXP[1]-USBRXMAXP[3])

The USB maximum receive data endpoint n 16-bit registers (USBRXMAXP[n]) define the maximum amount of data that can be transferred through the selected receive endpoint in a single operation.

Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the *USB Specification* on packet sizes for bulk, interrupt and isochronous transfers in full-speed operation.

The total amount of data represented by the value written to this register must not exceed the FIFO size for the transmit endpoint, and must not exceed half the FIFO size if double-buffering is required.

Note: USBRXMAXP[n] must be set to an even number of bytes for proper interrupt generation in DMA Basic Mode.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host Device

The USBRXMAXP[n] registers are shown in [Figure 21-45](#) and described in [Table 21-46](#).

Figure 21-45. USB Maximum Receive Data Endpoint n Registers (USBRXMAXP[n])

15	11	10	0
Reserved			MAXLOAD
R-0			R/W-000

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-46. USB Maximum Receive Data Endpoint n Registers (USBTXMAXP[n]) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	MAXLOAD		Maximum Payload specifies the maximum payload in bytes per transaction.

21.6.36 USB Receive Control and Status Endpoint n Low Register (USBRXCSRL[1]-USBRXCSRL[3])

The USB receive control and status endpoint n low 8-bit register (USBCSRL[n]) provides control and status bits for transfers through the currently selected receive endpoint.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host Device

The USBCSRL[n] registers in Host mode are shown in [Figure 21-46](#) and described in [Table 21-47](#).

Figure 21-46. USB Receive Control and Status Endpoint n Low Register (USBCSRL[n]) in Host Mode

7	6	5	4	3	2	1	0
CLRD _T	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
W1C-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-47. USB Control and Status Endpoint n Low Register(USBCSRL[n]) in Host Mode Field Descriptions

Bit	Field	Value	Description
7	NAKTO	0	Clear Data Toggle. No effect
		1	Writing a 1 to this bit clears the DT bit in the USBRXCSR _H [n] register.
6	STALLED	0	Endpoint Stalled. Software must clear this bit. No handshake has been received.
		1	A STALL handshake has been received. The EP n bit in the USBRXIS register is also set.
5	REQPKT	0	Request Packet. This bit is cleared when the RXRDY bit is set. No request
		1	Requests an IN transaction.
4	FLUSH	0	Flush FIFO. If the FIFO is double-buffered, FLUSH may have to be set twice to completely clear the FIFO. Note: This bit should only be set when the RXRDY bit is set. At other times, it may cause data to be corrupted.
		1	Flushes the next packet to be read from the endpoint receive FIFO. The FIFO pointer is reset and the RXRDY bit is cleared.
3	DATAERR / NAKTO	0	Data Error / NAK Timeout Normal operation
		1	Isochronous endpoints only: Indicates that RXRDY is set and the data packet has a CRC or bit-stuff error. This bit is cleared when RXRDY is cleared. Bulk endpoints only: Indicates that the receive endpoint is halted following the receipt of NAK responses for longer than the time set by the NAKLMT field in the USBRXINTERVAL[n] register. Software must clear this bit to allow the endpoint to continue.
2	ERROR	0	Error. Software must clear this bit. Note: This bit is only valid when the receive endpoint is operating in Bulk or Interrupt mode. In Isochronous mode, it always returns zero. No error
		1	Three attempts have been made to receive a packet and no data packet has been received. The EP n bit in the USBRXIS register is set in this situation.
1	FULL	0	FIFO Full The receive FIFO is not full.
		1	No more packets can be loaded into the receive FIFO.

Table 21-47. USB Control and Status Endpoint n Low Register(USBCSRL[n])**in Host Mode Field Descriptions (continued)**

Bit	Field	Value	Description
0	RXRDY		Receive Packet Ready. If the AUTOCLR bit in the USBRXCSR[n] register is set, then this bit is automatically cleared when a packet of USBRXMAXP[n] bytes has been unloaded from the receive FIFO. If the AUTOCLR bit is clear, or if packets of less than the maximum packet size are unloaded, then software must clear this bit manually when the packet has been unloaded from the receive FIFO.
		0	No data packet has been received.
		1	Indicates that a data packet has been received. The EPn bit in the USBTXIS register is also set in this situation.

USBCSRL0 in Device mode is shown in [Figure 21-47](#) and described in [Table 21-48](#).

**Figure 21-47. USB Control and Status Endpoint n Low Register (USBCSRL[n])
in Device Mode**

7	6	5	4	3	2	1	0
CLRD _T	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
W1C-0	W1C-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; -n = value after reset

**Table 21-48. USB Control and Status Endpoint 0 Low Register(USBCSRL[n])
in Device Mode Field Descriptions**

Bit	Field	Value	Description
7	CLRD _T		Clear Data Toggle
		0	No effect
		1	Writing a 1 to this bit clears the DT bit in the USBRXCSR[n] register.
6	STALLED		Endpoint Stalled. Software must clear this bit.
		0	A STALL handshake has been transmitted.
		1	A STALL handshake has been transmitted.
5	STALL		Send Stall. Software must clear this bit to terminate the STALL condition. Note: This bit has no effect where the endpoint is being used for isochronous transfers.
		0	No effect
		1	Issues a STALL handshake.
4	FLUSH		Flush FIFO. The CPU writes a 1 to this bit to flush the next packet to be read from the endpoint receive FIFO. The FIFO pointer is reset and the RXRDY bit is cleared. Note that if the FIFO is double-buffered, FLUSH may have to be set twice to completely clear the FIFO.
		0	No effect
		1	Flushes the next packet from the endpoint receive FIFO. The FIFO pointer is reset and the RXRDY bit is cleared. Note: This bit should only be set when the RXRDY bit is set. At other times, it may cause data to be corrupted.
3	DATAEND		Data error. This bit is cleared when RXRDY is cleared. Note: This bit is only valid when the endpoint is operating in Isochronous mode. In Bulk mode, it always returns zero.
		0	Normal operation
		1	Indicates that RXRDY is set and the data packet has a CRC or bit-stuff error. This bit is cleared automatically.
2	OVER		Overrun. Software must clear this bit. Note: This bit is only valid when the endpoint is operating in Isochronous mode. In Bulk mode, it always returns zero.
		0	No overrun error
		1	Indicates an OUT packet cannot be loaded into the receive FIFO.

Table 21-48. USB Control and Status Endpoint 0 Low Register(USBCSRL[n])
in Device Mode Field Descriptions (continued)

Bit	Field	Value	Description
1	FULL	0	FIFO Full The receive FIFO is not full.
		1	No more packets can be loaded into the receive FIFO.
0	RXRDY	0	Receive Packet Ready. If the AUTOCLR bit in the USBRXCSR[n] register is set, then this bit is automatically cleared when a packet of USBRXMAXP[n] bytes has been unloaded from the receive FIFO. If the AUTOCLR bit is clear, or if packets of less than the maximum packet size are unloaded, then software must clear this bit manually when the packet has been unloaded from the receive FIFO.
		1	No data packet has been received. A data packet has been received. The EPn bit in the USBTXIS register is also set in this situation. This bit is cleared by writing a 1 to the RXRDYC bit.

21.6.37 USB Receive Control and Status Endpoint n High Register (USBRXCSR[n]-USBRXCSR[n][3])

The USB receive control and status endpoint n high 8-bit register (USBCSRL[n]) provides additional control and status bits for transfers through the currently selected receive endpoint.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host Device

The USBCSRH[n] registers in OTG A/Host mode are shown in [Figure 21-48](#) and described in [Table 21-49](#).

Figure 21-48. USB Receive Control and Status Endpoint n High Register (USBCSRH[n]) in Host Mode

7	6	5	4	3	2	1	0
AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	Reserved
W1C-0	R/W-0	R/W-0	R-0	R/W-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-49. USB Control and Status Endpoint n High Register (USBCSRH[n]) in Host Mode Field Descriptions

Bit	Field	Value	Description
7	AUTOCL	0	Auto Clear
		1	No effect
			Enables the RXRDY bit to be automatically cleared when a packet of USBRXMAXP[n] bytes has been unloaded from the receive FIFO. When packets of less than the maximum packet size are unloaded, RXRDY must be cleared manually. Care must be taken when using DMA to unload the receive FIFO as data is read from the receive FIFO in 4-byte chunks regardless of the value of the MAXLOAD field in the USBRXMAXP[n] register, see Section 21.3.3 .
6	AUTORQ	0	Auto Request Note: This bit is automatically cleared when a short packet is received.
		1	No effect
			Enables the REQPKT bit to be automatically set when the RXRDY bit is cleared.
5	DMAEN	0	DMA Request Enable Note: Three TX and three RX endpoints can be connected to the DMA module. If this bit is set for a particular endpoint, the DMAARX, DMABRX, or DMACRX field in the USB DMA Select (USBDMASEL) register must be programmed correspondingly.
		1	Disables the DMA request for the receive endpoint.
			Enables the DMA request for the receive endpoint.
4	PIDERR	0	PID Error. This bit is ignored in bulk or interrupt transactions.
		1	No error
			Indicates a PID error in the received packet of an isochronous transaction.
3	DMAMOD	0	DMAMOD Note: This bit must not be cleared either before or in the same cycle as the above DMAEN bit is cleared.
		1	An interrupt is generated after every DMA packet transfer.
			An interrupt is generated only after the entire DMA transfer is complete.
2	DTWE	0	Data Toggle Write Enable. This bit is automatically cleared once the new value is written.
		1	The DT bit cannot be written.
			Enables the current state of the receive endpoint data to be written (see DT bit).
1	DT		Data Toggle. When read, this bit indicates the current state of the receive data toggle. If DTWE is High, this bit may be written with the required setting of the data toggle. If DTWE is Low, any value written to this bit is ignored. Care should be taken when writing to this bit as it should only be changed to RESET the receive endpoint.
0	Reserved	0	Reserved

The USBCSRH[*n*] registers in Device mode are shown in [Figure 21-49](#) and described in [Table 21-50](#).

Figure 21-49. USB Control and Status Endpoint *n* High Register (USBCSRH[*n*]) in Device Mode

7	6	5	4	3	2	0
AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD		Reserved
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 21-50. USB Control and Status Endpoint 0 High Register(USBCSRH[*n*]) in Device Mode Field Descriptions

Bit	Field	Value	Description
7	AUTOCL	0	Auto Clear
		1	No effect
		1	Enables the RXRDY bit to be automatically cleared when a packet of USBRXMAXP[<i>n</i>] bytes has been unloaded from the receive FIFO. When packets of less than the maximum packet size are unloaded, RXRDY must be cleared manually. Care must be taken when using DMA to unload the receive FIFO as data is read from the receive FIFO in 4-byte chunks regardless of the value of the MAXLOAD field in the USBRXMAXP[<i>n</i>] register, see Section 21.3.3 .
6	ISO	0	Isochronous Transfers
		1	Enables the receive endpoint for isochronous transfers.
		1	Enables the receive endpoint for bulk/interrupt transfers.
5	DMAEN	0	DMA Request Enable
		1	Note: Three TX and three RX endpoints can be connected to the DMA module. If this bit is set for a particular endpoint, the DMAARX, DMABRX, or DMACRX field in the USB DMA Select (USBDMASEL) register must be programmed correspondingly.
		0	Disables the DMA request for the receive endpoint.
		1	Enables the DMA request for the receive endpoint.
4	DISNYET/PI DERR	0	Disable NYET / PID Error
		1	For bulk or interrupt transactions: Disables the sending of NYET handshakes. When this bit is set, all successfully received packets are acknowledged, including at the point at which the FIFO becomes full. For isochronous transactions: Indicates a PID error in the received packet.
3	DMAMOD	0	DMA Request Mode
		1	Note: This bit must not be cleared either before or in the same cycle as the above DMAEN bit is cleared.
		0	An interrupt is generated after every DMA packet transfer.
		1	An interrupt is generated only after the entire DMA transfer is complete.
0	Reserved	0	Reserved

21.6.38 USB Receive Byte Count Endpoint n Registers (USBRXCOUNT[1]-USBRXCOUNT[3])

The USB receive byte count endpoint n 16-bit read-only registers hold the number of data bytes in the packet currently in line to be read from the receive FIFO. If the packet is transmitted as multiple bulk packets, the number given is for the combined packet.

Note: The value returned changes as the FIFO is unloaded and is only valid while the RXRDY bit in the USBRXCSR n register is set.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host Device

The USBRXCOUNT[n] registers are shown in [Figure 21-50](#) and described in [Table 21-51](#).

Figure 21-50. USB Maximum Receive Data Endpoint n Registers (USBRXCOUNT[n])

15	13	12	0
Reserved		COUNT	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-51. USB Maximum Receive Data Endpoint n Registers (USBRXCOUNT[n]) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	COUNT		Receive Packet Count indicates the number of bytes in the receive packet.

21.6.39 USB Host Transmit Configure Type Endpoint n Register (USBTXTYPE[1]-USBTXTYPE[3])

The USB host transmit configure type endpoint n 8-bit registers (USBTXTYPE[n]) must be written with the endpoint number to be targeted by the endpoint, the transaction protocol to use for the currently selected transmit endpoint, and its operating speed.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBXTYPE[n] registers are shown in [Figure 21-51](#) and described in [Table 21-52](#).

Figure 21-51. USB Host Transmit Configure Type Endpoint n Register (USBTXTYPE[n])

7	6	5	4	3	0
SPEED		PROTO		TEP	
R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-52. USB Host Transmit Configure Type Endpoint n Register(USBTXTYPE[n]) Field Descriptions

Bit	Field	Value	Description
7-6	SPEED	0h 1h 2h 3h	Operating Speed. This bit field specifies the operating speed of the target Device: Default. The target is assumed to be using the same connection speed as the USB controller. Reserved Full Low
5-4	PROTO	0h 1h 2h 3h	Protocol. Software must configure this bit field to select the required protocol for the transmit endpoint: Control Isochronous Bulk Interrupt
3-0	TEP	0	Target Endpoint Number. Software must configure this value to the endpoint number contained in the transmit endpoint descriptor returned to the USB controller during Device enumeration.

21.6.40 USB Host Transmit Interval Endpoint n Register (USBTXINTERVAL[1]USBTXINTERVAL[3])

The USB host transmit interval endpoint n 8-bit registers (USBTXINTERVAL[n]), for interrupt and isochronous transfers, define the polling interval for the currently selected transmit endpoint. For bulk endpoints, this register defines the number of frames after which the endpoint should time out on receiving a stream of NAK responses.

The USBTXINTERVAL[n] registers values define a number of frames, as follows:

Table 21-53. USBTXINTERVAL[n] Frame Numbers

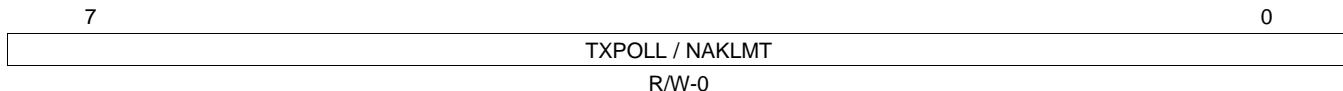
Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low-speed or Full-speed	0x01-0xFF	The polling interval is m frames.
Isochronous	Full-speed	0x01-0x10	The polling interval is $2^{(m-1)}$ frames.
Bulk	Full-speed	0x02-0x10	The NAK Limit is $2^{(m-1)}$ frames. A value of 0 or 1 disables the NAK timeout function.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBTXINTERVAL[n] registers are shown in [Figure 21-51](#) and described in [Table 21-52](#).

Figure 21-52. USB Host Transmit Interval Endpoint n Register (USBTXINTERVAL[n])



LEGEND: R/W = Read/Write; - n = value after reset

Table 21-54. USB Host Transmit Interval Endpoint n Register(USBTXINTERVAL[n]) Field Descriptions

Bit	Field	Value	Description
7-0	TXPOLL / NAKLMT	0	TX Polling / NAK Limit The polling interval for interrupt/isochronous transfers; the NAK limit for bulk transfers. See Table 21-53 for valid entries; other values are reserved.

21.6.41 USB Host Configure Receive Type Endpoint n Register (USBRXTYPE[1]-USBRXTYPE[3])

The USB host configure receive type endpoint n 8-bit registers (USBRXTYPE[n]) must be written with the endpoint number to be targeted by the endpoint, the transaction protocol to use for the currently selected receive endpoint, and its operating speed.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBRXTYPE[n] registers are shown in [Figure 21-53](#) and described in [Table 21-55](#).

Figure 21-53. USB Host Configure Receive Type Endpoint n Register (USBRXTYPE[n])

7	6	5	4	3	0
SPEED		PROTO		TEP	
R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; - n = value after reset

Table 21-55. USB Host Configure Receive Type Endpoint n Register(USBRXTYPE[n]) Field Descriptions

Bit	Field	Value	Description
7-6	SPEED	0h 1h 2h 3h	Operating Speed. This bit field specifies the operating speed of the target Device: Default. The target is assumed to be using the same connection speed as the USB controller. Reserved Full Low
5-4	PROTO	0h 1h 2h 3h	Protocol. Software must configure this bit field to select the required protocol for the receive endpoint: Control Isochronous Bulk Interrupt
3-0	TEP	0	Target Endpoint Number. Software must configure this value to the endpoint number contained in the transmit endpoint descriptor returned to the USB controller during Device enumeration.

21.6.42 USB Host Receive Polling Interval Endpoint n Register (USBRXINTERVAL[1]-USBRXINTERVAL[3])

The USB host receive polling interval endpoint n 8-bit registers (USBRXINTERVAL[n]), for interrupt and isochronous transfers, define the polling interval for the currently selected transmit endpoint. For bulk endpoints, this register defines the number of frames after which the endpoint should time out on receiving a stream of NAK responses.

The USBRXINTERVAL[n] registers values define a number of frames, as follows:

Table 21-56. USBRXINTERVAL[n] Frame Numbers

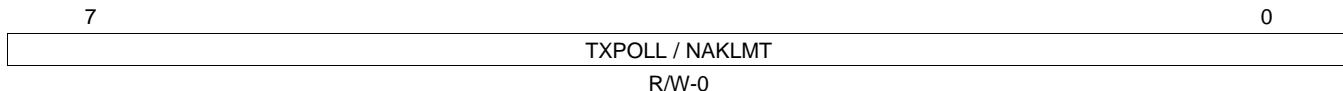
Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low-speed or Full-speed	0x01-0xFF	The polling interval is m frames.
Isochronous	Full-speed	0x01-0x10	The polling interval is $2^{(m-1)}$ frames.
Bulk	Full-speed	0x02-0x10	The NAK Limit is $2^{(m-1)}$ frames. A value of 0 or 1 disables the NAK timeout function.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBRXINTERVAL[n] registers are shown in [Figure 21-51](#) and described in [Table 21-52](#).

Figure 21-54. USB Host Receive Polling Interval Endpoint n Register (USBRXINTERVAL[n])



LEGEND: R/W = Read/Write; - n = value after reset

Table 21-57. USB Host Receive Polling Interval Endpoint n Register(USBRXINTERVAL[n]) Field Descriptions

Bit	Field	Value	Description
7-0	TXPOLL / NAKLMT	0	TX Polling / NAK Limit The polling interval for interrupt/isochronous transfers; the NAK limit for bulk transfers. See Table 21-56 for valid entries; other values are reserved.

21.6.43 USB Request Packet Count in Block Transfer Endpoint n Registers (USBRQPKTCOUNT[1]-USBRQPKTCOUNT[3])

The USB receive packet count in block transfer endpoint n 16-bit read/writer registers are used in Host mode to specify the number of packets that are to be transferred in a block transfer of one or more bulk packets to receive endpoint n . The USB controller uses the value recorded in this register to determine the number of requests to issue where the AUTORQ bit in the USBRXCSR[n] register has been set. For more information about IN transactions as a host, see [Section 21.3.2.2](#).

Note: Multiple packets combined into a single bulk packet within the FIFO count as one packet.

For the specific offset for each register see [Table 21-3](#).

Mode(s): Host

The USBRQPKTCOUNT[n] registers are shown in [Figure 21-55](#) and described in [Table 21-58](#).

**Figure 21-55. USB Request Packet Count in Block Transfer Endpoint n Registers
(USBRQPKTCOUNT[n])**

15	13	12	0
Reserved		COUNT	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 21-58. USB Request Packet Count in Block Transfer Endpoint n Registers
(USBRQPKTCOUNT[n]) Field Descriptions**

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	COUNT		Block Transfer Packet Count sets the number of packets of the size defined by the MAXLOAD bit field that are to be transferred in a block transfer. Note: This is only used in Host mode when AUTORQ is set. The bit has no effect in Device mode or when AUTORQ is not set.

21.6.44 USB Receive Double Packet Buffer Disable Register (USBRXDPKTBUFDIS), offset 0x340

The USB receive double packet buffer disable 16-bit register (USBTXIE) indicates which of the receive endpoints have disabled the double-packet buffer functionality (see *Double-Packet Buffering* in Section 21.3.1.1.1).

Mode(s): Host Device

USBRXDPKTBUFDIS is shown in Figure 21-56 and described in Table 21-59.

Figure 21-56. USB Receive Double Packet Buffer Disable Register (USBRXDPKTBUFDIS)

15	Reserved	4	3	2	1	0
	R-0			R/W-1	R/W-1	R/W-1 R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-59. USB Receive Double Packet Buffer Disable Register (USBRXDPKTBUFDIS) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved		Reserved
3	EP3	0 1	EP3 RX Double-Packet Buffer Disable Disables double-packet buffering. Enables double-packet buffering.
2	EP2	0 1	EP2 RX Double-Packet Buffer Disable Disables double-packet buffering. Enables double-packet buffering.
1	EP1	0 1	EP1 RX Double-Packet Buffer Disable Disables double-packet buffering. Enables double-packet buffering.
0	Reserved	0	Reserved

21.6.45 USB Transmit Double Packet Buffer Disable Register (USBTXDPKTBUFDIS), offset 0x342

The USB transmit double packet buffer disable 16-bit register (USBTXIE) indicates which of the transmit endpoints have disabled the double-packet buffer functionality (see *Double-Packet Buffering* in Section 21.3.1.1.1).

Mode(s): Host Device

USBTXDPKTBUFDIS is shown in [Figure 21-57](#) and described in [Table 21-60](#).

Figure 21-57. USB Transmit Double Packet Buffer Disable Register (USBTXDPKTBUFDIS)

15	4	3	2	1	0
Reserved	EP3	EP2	EP1	Rsvd	
R-0	R/W-1	R/W-1	R/W-1	R-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 21-60. USB Transmit Double Packet Buffer Disable Register (USBTXDPKTBUFDIS)
Field Descriptions**

Bit	Field	Value	Description
15-4	Reserved		Reserved
3	EP3	0	EP3 RX Double-Packet Buffer Disable Disables double-packet buffering.
		1	Enables double-packet buffering.
2	EP2	0	EP2 RX Double-Packet Buffer Disable Disables double-packet buffering.
		1	Enables double-packet buffering.
1	EP1	0	EP1 RX Double-Packet Buffer Disable Disables double-packet buffering.
		1	Enables double-packet buffering.
0	Reserved	0	Reserved

21.6.46 USB External Power Control Register (USBEPC), offset 0x400

The USB external power control 32-bit register (USBEPC) specifies the function of the two-pin external power interface (USB0EPEN and USB0PFLT). The assertion of the power fault input may generate an automatic action, as controlled by the hardware configuration registers. The automatic action is necessary because the fault condition may require a response faster than one provided by firmware.

Mode(s): Host Device

USBEPC is shown in [Figure 21-58](#) and described in [Table 21-61](#).

Figure 21-58. USB External Power Control Register (USBEPC)

31	Reserved							16
R-0								
15	Reserved				10	9	8	
R-0								
7	6	5	4	3	2	1	0	
Reserved	PFLTAEN	PFLTSEN	PFLTEN	Reserved	EPENDE	EPEN		
R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0		

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-61. USB External Power Control Register (USBEPC) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-8	PFLTACT	0h 1h 2h 3h	Power Fault Action. This bit field specifies how the USB0EPEN signal is changed when detecting a USB power fault. Unchanged. USB0EPEN is controlled by the combination of the EPEN and EPENDE bits. Tristate. USB0EPEN is undriven (tristate). Low. USB0EPEN is driven Low. High. USB0EPEN is driven High.
7	Reserved	0	Reserved
6	PFLTAEN	0 1	Power Fault Action Enable. This bit specifies whether a USB power fault triggers any automatic corrective action regarding the driven state of the USB0EPEN signal. Disabled. USB0EPEN is controlled by the combination of the EPEN and EPENDE bits. Enabled. The USB0EPEN output is automatically changed to the state specified by the PFLTACT field.
5	PFLTSEN	0 1	Power Fault Sense. This bit specifies the logical sense of the USB0PFLT input signal that indicates an error condition. The complementary state is the inactive state. 0 Low Fault. If USB0PFLT is driven Low, the power fault is signaled internally (if enabled by the PFLTEN bit). 1 High Fault. If USB0PFLT is driven High, the power fault is signaled internally (if enabled by the PFLTEN bit).
4	PFLTEN	0 1	Power Fault Input Enable. This bit specifies whether the USB0PFLT input signal is used in internal logic. 0 Not Used. The USB0PFLT signal is ignored. 1 Used. The USB0PFLT signal is used internally
3	Reserved	0	Reserved

Table 21-61. USB External Power Control Register (USBEPC) Field Descriptions (continued)

Bit	Field	Value	Description
2	EPENDE		<p>EPEN Drive Enable. This bit specifies whether the USB0EPEN signal is driven or undriven (tristate). When driven, the signal value is specified by the EPEN field. When not driven, the EPEN field is ignored and the USB0EPEN signal is placed in a high-impedance state.</p> <p>The USB0EPEN signal is undriven at reset because the sense of the external power supply enable is unknown. By adding the high-impedance state, system designers can bias the power supply enable to the disabled state using a large resistor (100 kΩ) and later configure and drive the output signal to enable the power supply.</p> <p>0 Not Driven. The USB0EPEN signal is high impedance.</p> <p>1 Driven. The USB0EPEN signal is driven to the logical value specified by the value of the EPEN field.</p>
1-0	EPEN	0h 1h 2h 3h	<p>External Power Supply Enable Configuration. This bit field specifies and controls the logical value driven on the USB0EPEN signal.</p> <p>0h Power Enable Active Low. The USB0EPEN signal is driven Low if the EPENDE bit is set.</p> <p>1h Power Enable Active High. The USB0EPEN signal is driven High if the EPENDE bit is set.</p> <p>2h Power Enable High if VBUS Low. The USB0EPEN signal is driven High when the A device is not recognized.</p> <p>3h Power Enable High if VBUS High. The USB0EPEN signal is driven High when the A device is recognized.</p>

21.6.47 USB External Power Control Raw Interrupt Status Register (USBEPCRIS), offset 0x404

The USB external power control raw interrupt status 32-bit register (USBEPCRIS) specifies the unmasked interrupt status of the two-pin external power interface.

Mode(s): Host Device

USBEPCRIS is shown in [Figure 21-59](#) and described in [Table 21-62](#).

Figure 21-59. USB External Power Control Raw Interrupt Status Register (USBEPCRIS)

31	1	0
Reserved	R-0	PF

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-62. USB External Power Control Raw Interrupt Status Register (USBEPCRIS) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	PF	0	USB Power Fault Interrupt Status. This bit is cleared by writing a 1 to the PF bit in the USBEPCISC register.
		1	A Power Fault status has been detected.
		1	An interrupt has not occurred.

21.6.48 USB External Power Control Interrupt Mask Register (USBEPCIM), offset 0x408

The USB external power control interrupt mask 32-bit register (USBEPCIM) specifies the interrupt mask of the two-pin external power interface.

Mode(s): Host Device

USBEPCIM is shown in [Figure 21-59](#) and described in [Table 21-62](#).

Figure 21-60. USB External Power Control Interrupt Mask Register (USBEPCIM)

31	1	0
Reserved		PF
R-0		R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-63. USB External Power Control Interrupt Mask Register (USBEPCIM) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	PF	0	USB Power Fault Interrupt Mask. The raw interrupt signal from a detected power fault is sent to the interrupt controller.
		1	A detected power fault does not affect the interrupt status.

21.6.49 USB External Power Control Interrupt Status and Clear Register (USBEPCISC), offset 0x40C

The USB external power control interrupt status and clear 32-bit register (USBEPCISC) specifies the unmasked interrupt status of the two-pin external power interface.

Mode(s): Host Device

USBEPCISC is shown in [Figure 21-61](#) and described in [Table 21-64](#).

Figure 21-61. USB External Power Control Interrupt Status and Clear Register (USBEPCISC)

31	Reserved	R-0	1	0
			PF	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-64. USB External Power Control Interrupt Status and Clear Register (USBEPCISC) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. Reset is 0x0000.000.
0	PF	0	USB Power Fault Interrupt Status and Clear. This bit is cleared by writing a 1. Clearing this bit also clears the PF bit in the USBEPCISC register.
		0	The PF bits in the USBEPCRIS and USBEPCIM registers are set, providing an interrupt to the interrupt controller.
		1	No interrupt has occurred or the interrupt is masked.

21.6.50 USB Device RESUME Raw Interrupt Status Register (USBDRRIS), offset 0x410

The USB device RESUME raw interrupt status register (USBDRRIS) is the raw interrupt status register. On a read, this register gives the current raw status value of the corresponding interrupt prior to masking. A write has no effect.

Mode(s): Host Device

USBDRRIS is shown in [Figure 21-62](#) and described in [Table 21-65](#).

Figure 21-62. USB Device RESUME Raw Interrupt Status Register (USBDRRIS)

31	Reserved	1	0
	R-0		RESUME R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-65. USB Device RESUME Raw Interrupt Status Register (USBDRRIS) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. Reset is 0x0000.000.
0	PF	0	RESUME Interrupt Status This bit is cleared by writing a 1 to the RESUME bit in the USBDRISC register. 1 A RESUME status has been detected. 0 An interrupt has not occurred.

21.6.51 USB Device RESUME Raw Interrupt Mask Register (USBDRIM), offset 0x414

The USB device RESUME raw interrupt status register (USBDRIM) is the masked interrupt status register. On a read, this register gives the current masked status value of the corresponding interrupt. A write has no effect.

Mode(s): Host Device

USBDRIM is shown in [Figure 21-63](#) and described in [Table 21-66](#).

Figure 21-63. USB Device RESUME Raw Interrupt Status Register (USBDRRIS)

31	Reserved	1	0
	R-0		RESUME R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-66. USB Device RESUME Raw Interrupt Status Register (USBDRRIS) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. Reset is 0x0000.000.
0	PF	0	RESUME Interrupt Mask The raw interrupt signal from a detected RESUME is sent to the interrupt controller. This bit should only be set when a SUSPEND has been detected (the SUSPEND bit in the USBIS register is set).
		1	A detected RESUME does not affect the interrupt status.

21.6.52 USB Device RESUME Interrupt Status and Clear Register (USBDRISC), offset 0x418

The USB device RESUME interrupt status and clear register (USBDRRIS) is the raw interrupt clear register. On a write of 1, the corresponding interrupt is cleared. A write of 0 has no effect.

Mode(s): Host Device

USBDRISC is shown in [Figure 21-64](#) and described in [Table 21-67](#).

Figure 21-64. USB Device RESUME Interrupt Status and Clear Register (USBDRISC)

31	Reserved	1	0
	R-0		R/W1C

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 21-67. USB Device RESUME Interrupt Status and Clear Register (USBDRISC)
Field Descriptions**

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. Reset is 0x0000.000.
0	RESUME	0	RESUME Interrupt Status and Clear. This bit is cleared by writing a 1. Clearing this bit also clears the RESUME bit in the USBDRCRIS register.
		0	The RESUME bits in the USBDRRIS and USBDRCIM registers are set, providing an interrupt to the interrupt controller.
		1	No interrupt has occurred or the interrupt is masked.

21.6.53 USB General-Purpose Control and Status Register (USBGPCS), offset 0x41C

The USB general-purpose control and status register (USBGPCS) provides the state of the internal ID signal.

When the USB controller is used as either a dedicated Host or Device, the DEVMODOTG and DEVMOD bits in the USB General-Purpose Control and Status (USBGPCS) register should be used to connect the ID inputs to fixed levels internally. For proper self-powered Device operation, the VBUS value must be monitored to assure that if the Host removes VBUS, the self-powered Device disables the D+/D- pull-up resistors. This function can be accomplished by connecting a standard GPIO to VBUS.

Mode(s): Host Device

USBGPCS is shown in [Figure 21-65](#) and described in [Table 21-68](#).

Figure 21-65. USB General-Purpose Control and Status Register (USBGPCS)

31	2	1	0
Reserved	R-0	DEVMODOTG	DEVMOD

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-68. USB General-Purpose Control and Status Register (USBGPCS) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved. Reset is 0x0000.000.
1	DEVMODOTG	0	Enable Device Mode. This bit enables the DEVMOD bit to control the state of the internal ID signal in OTG mode.
		1	The mode is specified by the state of the internal ID signal.
0	DEVMOD	0	This bit enables the DEVMOD bit to control the internal ID signal.
		1	Device Mode This bit specifies the state of the internal ID signal in Host mode and in OTG mode when the DEVMODOTG bit is set. In Device mode this bit is ignored (assumed set).
		0	Host mode
		1	Device mode

21.6.54 USB DMA Select Register (USBDMASEL), offset 0x450

The USB DMA select 32-bit register (USBDMASEL) specifies whether the unmasked interrupt status of the ID value is valid.

Mode(s): Host Device

USBDMASEL is shown in [Figure 21-66](#) and described in [Table 21-69](#).

Figure 21-66. USB DMA Select Register (USBDMASEL)

31	24	23	20	19	16
Reserved		DMACTX		DMACRX	
R/0		R/W-0		R/W-0	
15	12	11	8	7	4
DMABTX		DMABRX		DMAATX	DMAARX
R/W-0		R/W-0		R/W-0	R/W-0
					0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21-69. USB DMA Select Register (USBDMASEL) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved. Reset is 0x0000.000.
23-20	DMACTX	0h	DMA C TX Select specifies the TX mapping of the third USB endpoint on DMA channel 5 (primary assignment).
		1h	Reserved
		2h	Endpoint 1 TX
		3h	Endpoint 2 TX
			Endpoint 3 TX
19-16	DMACRX	0h	DMA C RX Select specifies the RX and TX mapping of the third USB endpoint on DMA channel 4 (primary assignment).
		1h	Reserved
		2h	Endpoint 1 RX
		3h	Endpoint 2 RX
			Endpoint 3 RX
15-12	DMABTX	0h	DMA B TX Select specifies the TX mapping of the second USB endpoint on DMA channel 3 (primary assignment).
		1h	Reserved
		2h	Endpoint 1 TX
		3h	Endpoint 2 TX
			Endpoint 3 TX
11-8	DMABRX	0h	DMA B RX Select Specifies the RX mapping of the second USB endpoint on DMA channel 2 (primary assignment).
		1h	Reserved
		2h	Endpoint 1 RX
		3h	Endpoint 2 RX
			Endpoint 3 RX
7-4	DMAATX	0h	DMA A TX Select specifies the TX mapping of the first USB endpoint on DMA channel 1 (primary assignment).
		1h	Reserved
		2h	Endpoint 1 TX
		3h	Endpoint 2 TX
			Endpoint 3 TX

Table 21-69. USB DMA Select Register (USBDMASEL) Field Descriptions (continued)

Bit	Field	Value	Description
3-0	DMAARX		DMA A RX Select specifies the RX mapping of the first USB endpoint on DMA channel 0 (primary assignment).
		0h	Reserved
		1h	Endpoint 1 RX
		2h	Endpoint 2 RX
		3h	Endpoint 3 RX

Universal Parallel Port (uPP)

This chapter discusses the features and functions of the Universal Parallel Port module.

Topic	Page
22.1 Introduction	2258
22.2 Functional Description	2259
22.3 IO Interface and System Requirements	2262
22.4 Registers	2272

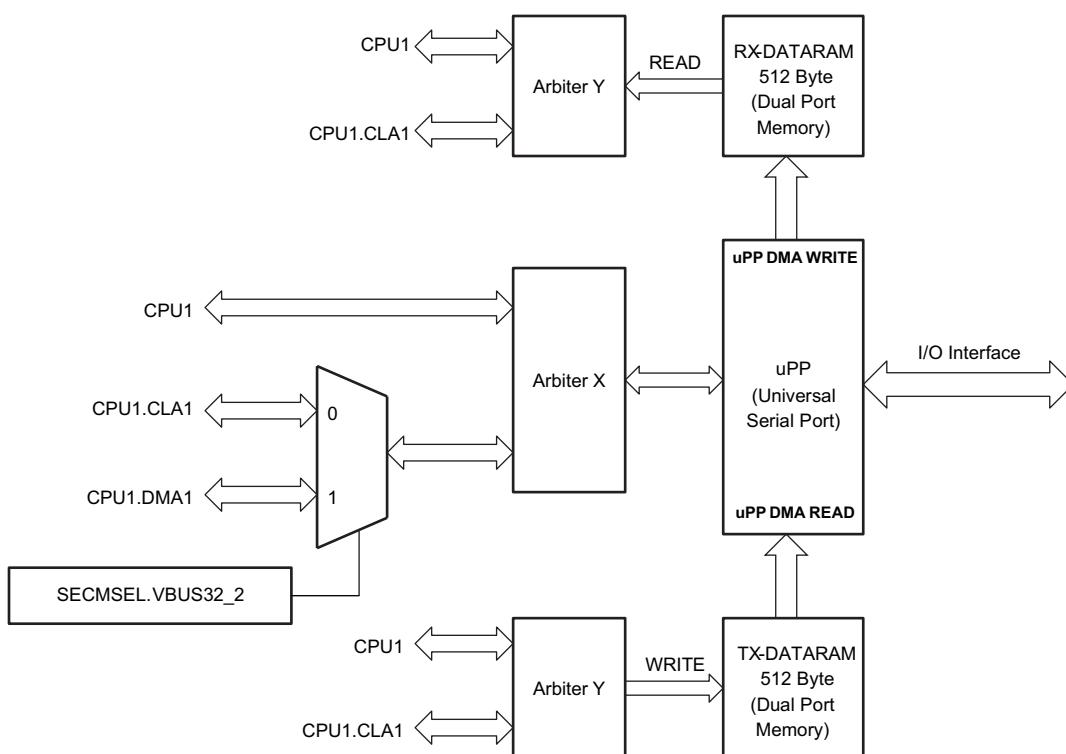
22.1 Introduction

The Universal parallel port (uPP) peripheral is a high-speed parallel interface with dedicated data lines and minimal control signals. It is designed to interface cleanly with high-speed analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) with 8-bit data width. It can also be interconnected with field-programmable gate arrays (FPGAs) or other uPP devices to achieve high-speed digital data transfer. It can operate in receive mode or transmit mode (simplex mode).

This peripheral includes an internal DMA controller to maximize throughput and minimize CPU overhead during high-speed data transmission. All UPP transactions uses internal DMA to feed data to or retrieve data from the I/O channels. Even though there is only one I/O channel, DMA controller includes two DMA channels to supports data interleave mode, in which all DMA resources service a single I/O channel.

On this device, uPP is dedicated resource for CPU1 subsystem and CPU1, CPU1.CLA1 and CPU1.DMA1 have access to this module. There are two dedicated DATA RAMs (also known as MSG RAMs), each of 512B, tightly coupled with uPP module (one for each, TX and RX). These DATA RAMs are used to store bulk of data to avoid frequent interruption to CPU. Only CPU1 and CPU1.CLA1 has access to these DATA RAMs. [Figure 22-1](#) shows the integration of uPP on this device.

Figure 22-1. uPP Integration



NOTE: In some other TI devices uPP IP is also called the Radio Peripheral Interface (RPI) module.

22.1.1 Features Supported

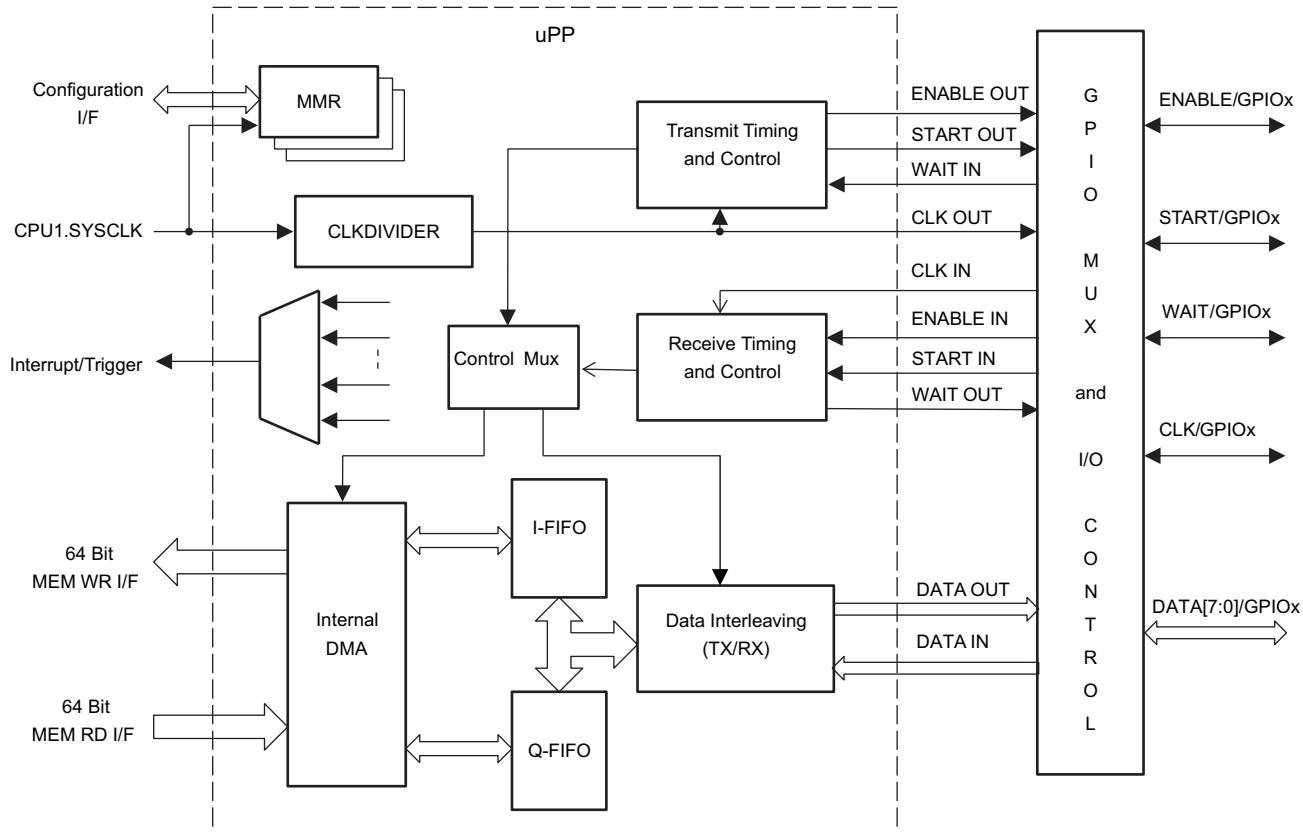
- Supports mainstream high-speed data converters with parallel conversion interface.
- Supports mainstream high-speed streaming interface with frame START indication.
- Supports mainstream high-speed streaming interface with data ENABLE indication.
- Supports mainstream high-speed streaming interface with synchronization WAIT signal.
- Supports SDR (single-data-rate) or DDR (double-data-rate, interleaved) interface.
- Supports multiplexing of interleaved data in SDR transmit case.
- Supports de-multiplexing and multiplexing of interleaved data in DDR case.

- Supports I/O interface clock frequency up to 50MHz for SDR case, and 25MHz for DDR.
- Supports single-channel 8-bit input receive or output transmit mode.
- Max throughput is 50MB/s for pure read or pure write.
- Available as a DSP to FPGA general purpose streaming interface.

22.2 Functional Description

22.2.1 Functional Block Diagram

Figure 22-2. Functional Block Diagram



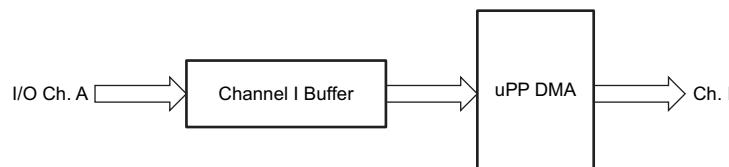
The uPP IP supports internal FIFO to store the data to and from IOs. To alleviate the load of data transfer from system memory to and from the uPP FIFOs, the IP supports internal DMA. The internal DMA has two channels: channel I and channel Q.

22.2.2 Data Flow

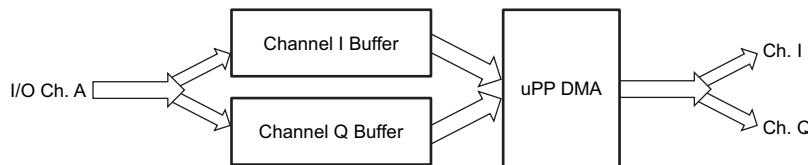
The following naming conventions are followed regarding channel numbering:

- It has only one I/O channel and that has been labeled as “channel A”
- DMA channel are labeled as “channel I and channel Q”.

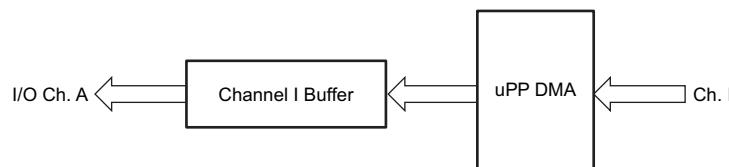
Figure 22-3 explains the data flow for receive in SDR mode and DDR non-demux mode. In this case, only one DMA channel (channel I) get used.

Figure 22-3. RX in SDR or DDR (non-demux) Mode

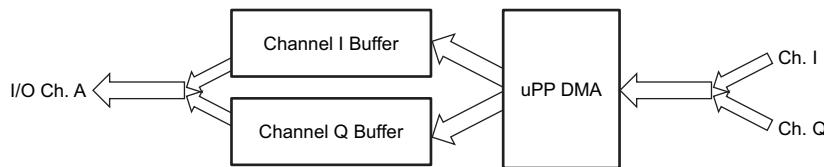
[Figure 22-4](#) explains the data flow for receive in DDR demux mode. In this case, both DMA channels (channel I and channel Q) are used.

Figure 22-4. RX in DDR (demux) Mode

[Figure 22-5](#) explains the data flow for transmit in SDR non-interleave or DDR non-demux mode. In this case, only one DMA channel (channel I) get used.

Figure 22-5. TX in SDR (non-interleave) or DDR (non-demux) Mode

[Figure 22-6](#) explains the data flow for transmit in SDR interleave or DDR demux mode. In this case, both DMA channels (channel I and channel Q) are used.

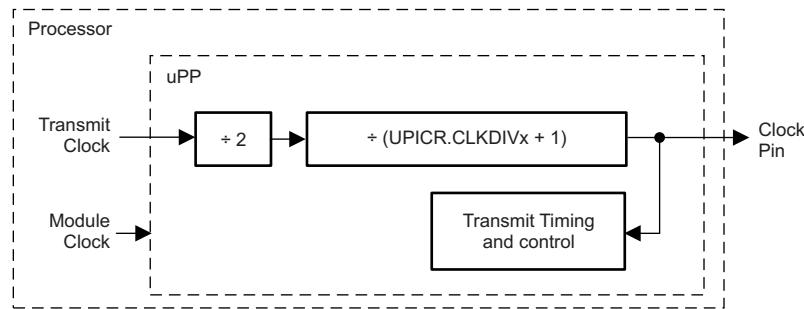
Figure 22-6. TX in SDR (interleave) or DDR (demux) Mode

22.2.3 Clock Generation and Control

The uPP peripheral uses three different clocks:

- A module clock that controls its internal logic and CPU interface. This is driven by CPU1.SYSCLK.
- A transmit clock (internally divided clock from the module clock) that runs the interface channel and drives the CLK pin out in transmit mode.
- A receive clock (input via CLK pin) that runs the interface channel in receive mode.

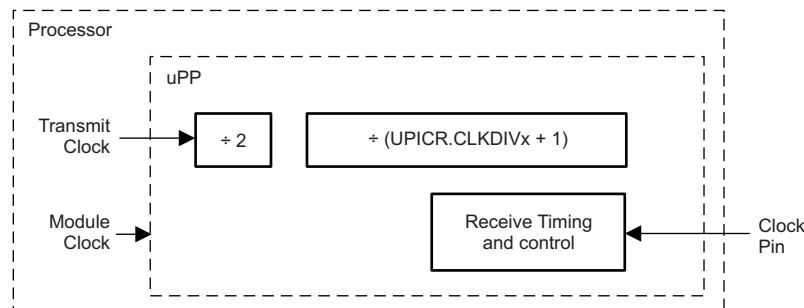
[Figure 22-7](#) shows the output clock generation system in transmit mode.

Figure 22-7. IO Output Clock Generation for TX Mode


$$\text{Output Clock} = \text{Module Clock} / (2 \times (\text{CLKDIVn} + 1))$$

The fixed divisor restricts the maximum speed of the I/O clock to 1/2 the device CPU clock speed. For DDR mode operation, the CLK output freq must be one eighth (1/8) or less of module clock.

For receive mode, channel requires an external clock to drive its CLK pin. The incoming clock is not divided, and its maximum allowed speed is one fourth (1/4) the module clock speed for SDR mode and one eighth (1/8) the module clock speed for DDR mode. [Figure 22-8](#) shows the clock generation system for a channel configured in receive mode.

Figure 22-8. IO Input clock for RX Mode


22.3 IO Interface and System Requirements

The uPP module provides interfacing logic to external streaming data, both inbound and outbound flow of data are supported. The interface protocol is a simple streaming interface. It is build on top of the existing high-speed data converters, and captures most of the high-speed data converters protocol.

The input receive mode and output transmit mode protocol are symmetrical, and source synchronous, that is, clock is supplied by the transmitter and the same clock is used to receive the data.

Table 22-1 describes the functionality of all the input/output (IO) signals of uPP module.

Table 22-1. uPP Signal Description

Signal	Description
CLK	<ul style="list-style-type: none"> Transmit or receive clock Input in receive mode Output in transmit mode (Clock divider programmable)
START	<ul style="list-style-type: none"> Input in receive mode Output in transmit mode Polarity programmable Indicates first data word of each line (frame) This is optional signal and if this feature is not used, external receiver can ignore this signal.
ENABLE	<ul style="list-style-type: none"> Input when in receive mode Output in transmit mode Polarity programmable Indicates data received is valid, or data transmitted is valid Can be programmed to be ignored in receive mode but in transmit mode always drive active in sync with valid data.
WAIT	<ul style="list-style-type: none"> Input in transmit mode Output in receive mode but always drive inactive by uPP in this case Polarity programmable In transmit mode when active, indicates that target is not ready to receive data. uPP will stop transmitting data at next clock cycle right after Wait signal is sampled as active. uPP module can be programmed to ignore this in transmit mode. <p>NOTE: The WAIT needs to be asserted for one full cycle of IO clock by external device.</p>
DATA[7:0]	<ul style="list-style-type: none"> 8-bit inputs in receive mode 8-bit output in transmit mode

22.3.1 Pin Multiplexing

Extensive pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. To determine how pin multiplexing affects the uPP peripheral, see the device-specific data manual.

22.3.2 Internal DMA Controller Description

The uPP peripheral includes an internal DMA controller separate from any device-level DMA, such as CPU1.DMA1/CPU2.DMA1. The internal DMA controller consists of two DMA channels, channel I and channel Q, which moves data to and from the uPP peripheral interface (I/O) channels in all operating modes. This section describes how to program the internal DMA channels.

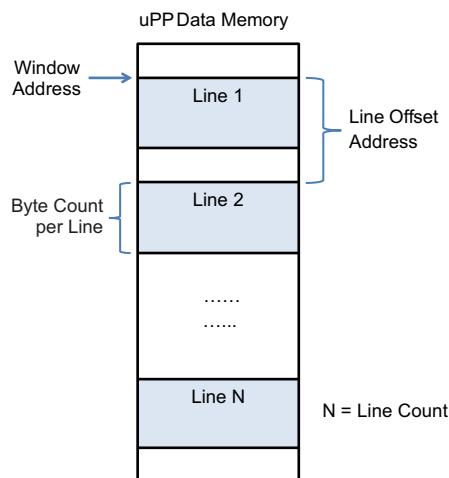
22.3.2.1 DMA Programming Concepts

The uPP internal DMA controller uses a simplified programming model similar to 2D transfers performed by any other DMA at system level. Each DMA channel may be configured with four parameters: window address, byte count, line count, and line offset address.

- Window Address (CHxDESC0.ADDR) - The location in uPP data memory of the first byte in the data buffer. When the uPP operates in receive mode, the DMA channel begins writing to this address as it takes incoming data from the uPP I/O channel. When the uPP operates in transmit mode, the DMA channel begins reading from this address and pass the data to the uPP I/O channel. The window address must be aligned to a 64-bit boundary (that is, the three LSBs must equal 0). Non-aligned addresses are automatically adjusted to a properly aligned value when written to configuration register.
- Byte Count (CHxDESC1.BCNT) - The number of bytes per line. The byte count must be an even number.
- Line Count (UPxDESC1.LCNT) - The number of lines per window. The total number of bytes transferred equals $B \times L$, where B is the byte count per line and L is the line count.
- Line Offset Address (CHxDESC2.LOFFSET) - The offset address between the first byte in successive Lines. The line offset address cannot exceed 65528 (FFF8h) bytes, and must be aligned to a 64-bit boundary in memory (that is, the three LSBs must equal 0).

Figure 22-9 shows a typical DMA window defined by these parameters.

Figure 22-9. Structure of DMA Window and Lines in Memory



Certain values of the line offset address have special implications on the structure of the data buffer:

- Line Offset Address = Byte Count : Data buffer is a contiguous block in memory with size equal to (Line Count) x (Byte Count).
- Line Offset Address = 0 : Data buffer consists of a single line, with total size equal to Byte Count. If the I/O channel is configured in transmit mode, this line is transmitted (Line Count) consecutive times before the DMA transfer completes. If the I/O channel is configured in receive mode, the buffer is repeatedly written and overwritten by incoming data.

To program a DMA transfer, write the appropriate fields in the DMA channel descriptor registers for DMA Channel I or for DMA Channel Q. If the associated I/O channel is initialized and idle, the DMA transfer and I/O transaction begins immediately. [Section 22.3.10](#) describes a step-by-step process for configuring the I/O channel and DMA channels to start a uPP transfer.

Each DMA channel allows a second descriptor to be queued while the previously programmed DMA transfer is still running. The PEND status bit in channel status register reports whether a new set of DMA parameters may be written to the DMA descriptor registers. Each DMA channel can have at most one active transfer and one queued transfer. This allows each I/O channel to perform uninterrupted, consecutive transactions across DMA transfer boundaries.

This DMA controller does not support automatically reloading DMA transfer descriptors. Each successive descriptor set must be explicitly written to the configuration registers by software. All uPP interrupt events originate in the internal DMA controller. [Section 22.3.6](#) lists and explains all uPP interrupt events.

The internal DMA controller always writes data in bursts of 64 bytes. However, DMA read operations have configurable burst size, which may be set per channel using the RDSIZEI and RDSIZEQ bits in the uPP threshold configuration register. A DMA channel waits until the specified number of bytes leaves its internal buffer before performing another burst read from memory.

Note that the TXSIZEA bit in threshold configuration register is not DMA parameters; instead, it controls transmit thresholds for the uPP interface channel.

22.3.2.2 Data Interleave Mode

The data interleave mode is a special configuration that maps both DMA channels to a single interface I/O channel. There are two variants on data interleave mode, each with special conditions:

- Single Data Rate (SDR) Interleave
 - Single Data Rate (DRA = 0)
 - Transmit Only (MODE = 1)
 - SDR Transmit interleave enabled (SDRTXILA = 1)
- Double Data Rate (DDR) Interleave
 - Double Data Rate (DRA = 1)
 - Transmit or Receive (MODE = 0/1)
 - SDR Transmit interleave disabled (SDRTXILA = 0)
 - DDR interleave enabled (DEMUXA = 1)

In data interleave mode, I/O channel is associated with two data buffers, each serviced by its own DMA channel (I and Q). In SDR interleave mode, the START signal is used as a buffer selection line: START = 1 indicates that the current word comes from DMA Channel I; START = 0 indicates that the current word comes from DMA Channel Q. In DDR Interleave mode, the data buffers alternate every word beginning with Channel I: Channel I Word 0, Channel Q Word 0, Channel I Word 1, Channel Q Word 1, and so forth. [Section 22.3.10](#) shows signal diagrams for both data interleave modes.

22.3.3 Protocol Description

The uPP peripheral on this device has one I/O channel with 8 data lines, which can be configured to run in transmit or receive mode. A channel may also be configured to ignore certain control signals using the uPP interface configuration register. By default it uses all four control signals, unless otherwise configured.

22.3.3.1 DATA[7:0] Signals

DATA[7:0] comprise the channel's entire data bus. In transmit mode, these pins are outputs that transmit data supplied by the channel's associated DMA channel. While the channel is idle, their behavior depends on the TRISENA bit in IFCFG register. These pins can be configured to drive an idle value (TRISENA = 0, VALA field in the uPP interface idle value register (IFIVAL)) or be in a high-impedance state while idle (TRISENA = 1). In receive mode, these pins are inputs that provide data to the channel's associated DMA channel.

22.3.3.2 START Signal

The uPP transmitter asserts the START signal when it transfers the first word of a data line. A line is defined in terms of the channel's associated DMA channel; for more on DMA programming concepts, see [Section 22.3.2](#). The START signal is active-high by default, but its polarity is controlled by the STARTPOLA bit in IFCFG register.

In transmit mode, START is an output signal and is always driven; in receive mode, START is an input signal and may be disabled using the STARTA bit in IFCFG register. When the channel is configured in transmit mode with data interleave enabled (SDRTXILA = 1 in CHCTL register), the START signal function changes completely. The START signal now asserts on every data word that is provided by DMA Channel I. For this alternative behavior, see [Section 22.3.3.6](#).

22.3.3.3 ENABLE

The uPP transmitter asserts the ENABLE signal when it transfers a valid data word. The ENABLE signal is active-high by default, but its polarity is controlled by the ENAPOLA bit in IFCFG register. In transmit mode, ENABLE is an output signal and is always driven; in receive mode, ENABLE is an input signal and may be disabled using the ENAA bit in IFCFG register.

22.3.3.4 WAIT Signal

The WAIT signal allows the receiver to request a temporary halt in data transmission. When the receiver asserts WAIT, the transmitter responds by stopping transmission (starting with the next word) until WAIT is released. The receiver ignores all incoming data until WAIT is released. Once WAIT is released, the transmitter can resume transmission on the next word. [Section 22.3.3](#) shows WAIT signal timing. The WAIT signal is active-high by default, but its polarity is controlled by the WAITPOLA bit in IFCFG register. In transmit mode, WAIT is an input signal and may be disabled using the WAITA bit in IFCFG register; in receive mode, WAIT is an output signal and always driven inactive by uPP.

22.3.3.5 CLOCK Signal

The uPP transmitter drives the CLOCK signal to align all other uPP signals. By default, other signals align on the rising edge of CLOCK, but its polarity is controlled by the CLKINVA bit in IFCFG register. The active edge(s) of CLOCK should always slightly precede transitions of other uPP signals. In transmit mode, CLOCK is an output signal; in receive mode, CLOCK is an input signal. For more information on clock generation and allowed frequencies, see [Section 22.3.2](#).

22.3.3.6 Signal Timing Diagrams

In the following diagrams, signals are marked (I) to indicate that they are inputs to the uPP peripheral and (o) to indicate that they are outputs from the uPP peripheral. Data words from a single DMA channel are designated Dx, while data words that must come from a specific DMA channel are designated Ix or Qx to indicate DMA Channel I or Q, respectively. For more information on DMA channels and data interleave mode, see [Section 22.3.2](#).

All signal diagrams are drawn with signal polarities in their default states. All signals except DATA are independently configurable in the uPP interface configuration register (IFCFG).

Figure 22-10. uPP Receive in SDR Mode

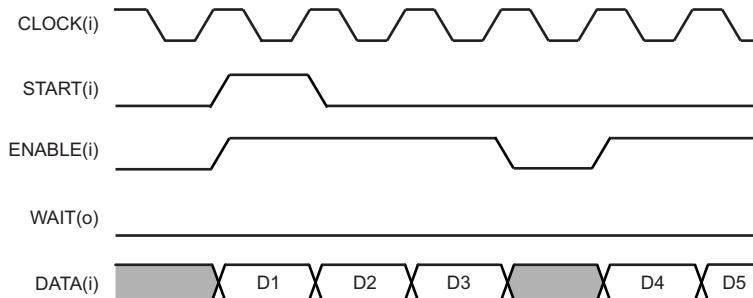
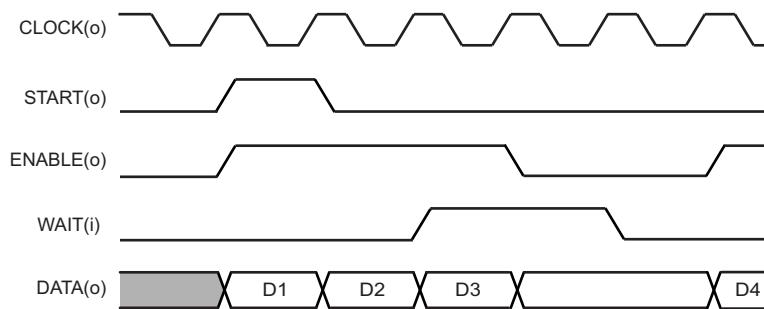
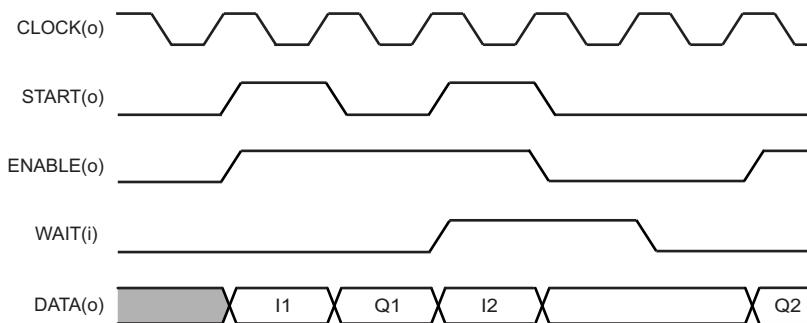
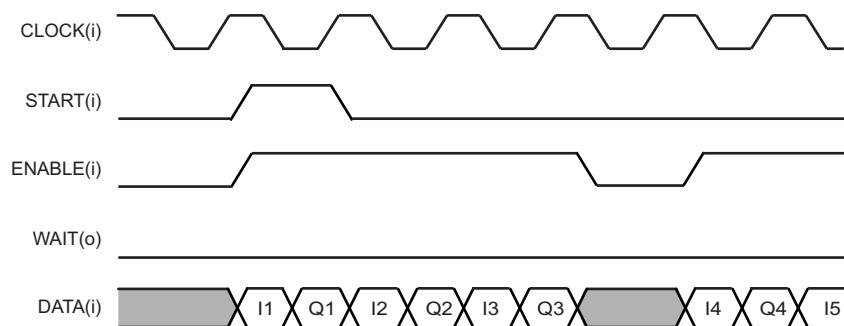
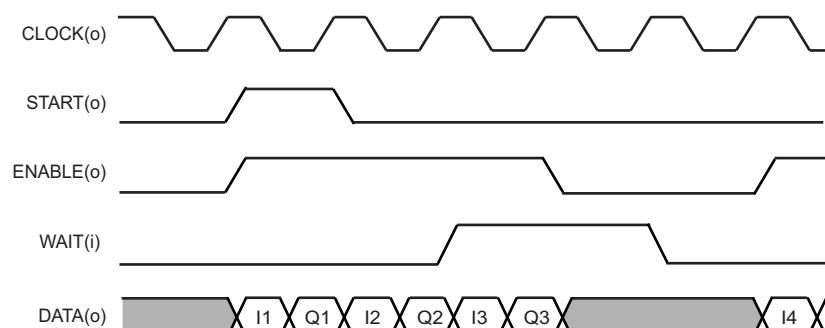


Figure 22-11. uPP Transmit in SDR Mode**Figure 22-12. uPP Transmit in SDR Mode – Interleaving****Figure 22-13. uPP Receive DDR Case****Figure 22-14. uPP Transmit DDR Case**

NOTE: START asserts on every data word from DMA Channel I in interleaving mode.

22.3.4 Data Format

On this device, uPP only support 8-bit interface hence no data packing is performed. User in this case, will have to make appropriate connection externally, if needed. For example, if a 4-bit ADC is used, then the user would have to tie the upper 4-bit of the uPP data inputs to '0' or '1' as needed. If external FPGA is connected, then the user would have to make sure that 8-bit data (or appropriate tieoffs) is driven out from the FPGA. By default uPP supports little endian data format but to support the data format of one of the TI device (CC1260), a configuration bit is provided to select 16bit big endian mode also.

Figure 22-15 and Figure 22-16 describe how data goes out and comes in based on these modes.

Figure 22-15. uPP Tx Data Pattern in Non-Interleaved Mode

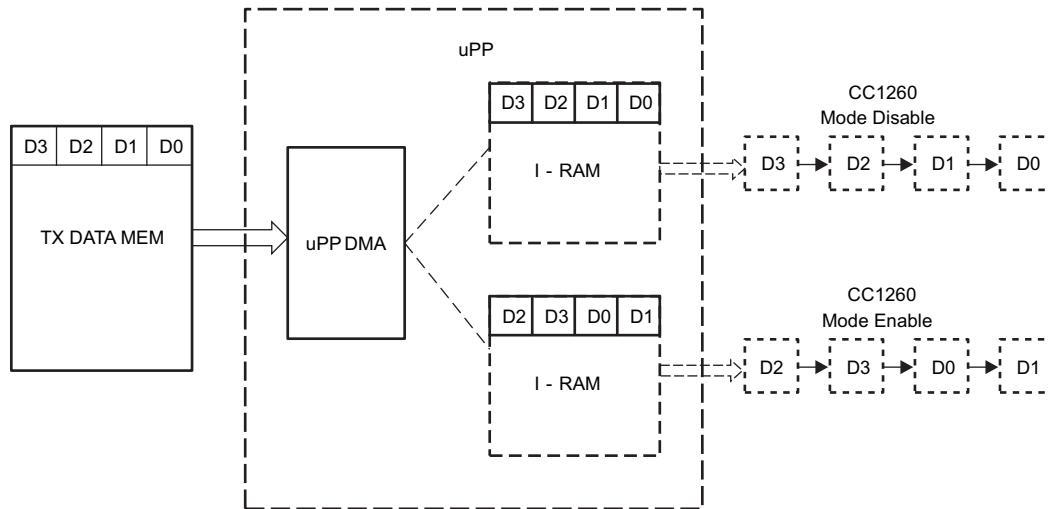
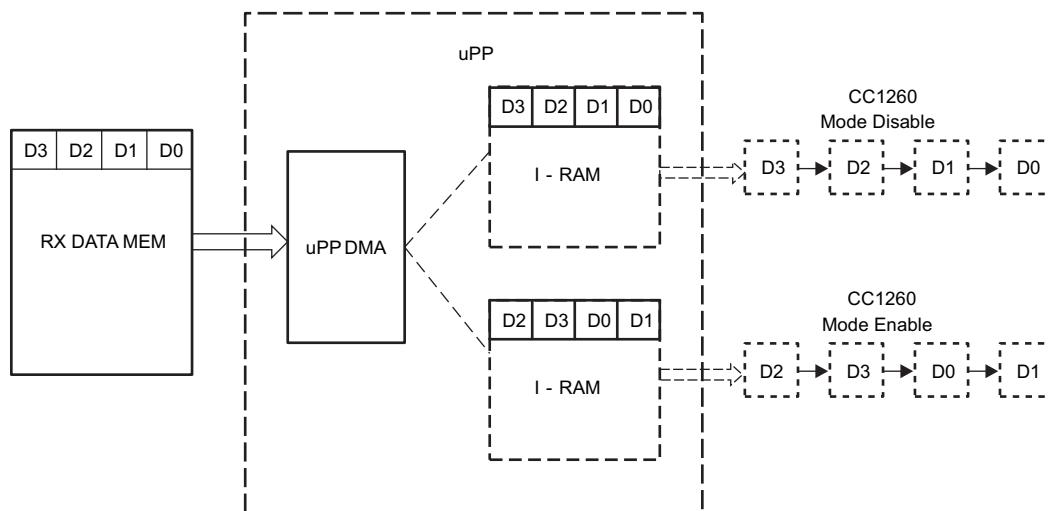


Figure 22-16. uPP Rx Data Pattern in Non-Interleaved Mode



22.3.5 Reset Considerations

22.3.5.1 Software Reset

Software reset clears the uPP internal state machines but does not reset the contents of the uPP registers. The following procedure performs a software reset on the uPP peripheral:

1. Write the PEREN bit in the uPP PERCTL register to 0 (disables the uPP).
2. Poll the DMAST bit in uPP PERCTL register for activity; wait until DMA controller is inactive and idle.
3. Write the SOFTRST bit in uPP PERCTL register to 1 (places uPP in software reset).

-
4. Write the SOFTRST bit in uPP PERCTL register to 0 to (brings uPP out of software reset).

NOTE: In receive mode, uPP IO input clock must be running to have effect of soft reset.

22.3.5.2 Hardware Reset

When the processor XRSn (or CPU1.SYSRSn) pin is asserted, the entire processor is reset and is held in the reset state until the RESET pin is released. As part of a device reset, the uPP state machines are reset, and the uPP registers are forced to their default states. For default states, see the register section.

NOTE: There is no SW method to apply a hard reset to the UPP module on this device.

22.3.6 Interrupt Support

The uPP peripheral generates multiple interrupt events, all tied to internal DMA Channels I and Q. The uPP peripheral automatically combines all interrupt events into a single chip-level interrupt driven to CPU1 and CPU1.CLA1. Individual events may be enabled using the uPP interrupt enable set register (INTENSET) and disabled using the uPP interrupt enable clear register (INTENCLR). Only enabled events generate interrupts and assert bits in the enabled interrupt status register (ENINTST). Disabled events do not generate interrupts but do assert bits in the raw interrupt status register (RAWINTST). An interrupt service routine (ISR) may be assigned to handle uPP CPU-level interrupts using the interrupt controller module. If uPP events occur in close proximity to one another, a single CPU interrupt (and a single call to the ISR) may represent multiple interrupt events. Thus, the uPP ISR must meet certain structural requirements:

- The ISR must be able to handle multiple events before returning
- The ISR must handle any subsequent events that occur after it is called but before it returns

Like CPU ISR, CLA tasks can be assigned based on these interrupt events.

22.3.6.1 End of Line (EOL) Event

This event occurs each time when DMA channel reaches the end of a line in the data window. Note that if the associated uPP interface channel is operating in transmit mode, this event may occur before the line's final bytes are actually transmitted over the data pins.

For small line size and fast data transfer, it is possible to "miss" EOL events if they occur faster than the user's code can handle them. This does not hinder uPP operation; the uPP peripheral continue processing data uninterrupted until the EOW event or some error condition is encountered.

22.3.6.2 End of Window (EOW) Event

This event occurs when the DMA channel reaches the end of its current data window. Note that if the associated uPP interface channel is operating in transmit mode, this event may occur shortly before the window's final bytes are actually transmitted over the data pins.

When an EOW event occurs, the DMA channel automatically begins the next DMA transfer if one has been pre-programmed into the channel descriptor registers. If no new transfer is preprogrammed, the DMA channel becomes idle. For small window size and fast data transfer, code overhead may make it impossible to maintain a constant flow of data through the uPP interface channel. This problem can be solved by increasing the DMA window size or decreasing the peripheral clock speed.

22.3.6.3 Underrun or Overflow (UOR) Event

This event occurs when the DMA channel fails to keep up with incoming or outgoing data on its associated interface channel. Typically, this error indicates that background system activity has interfered with normal operation of the peripheral. It does not occur simply when a channel is allowed to idle. After encountering this error, the uPP peripheral should be reset when this event occurs.

This error should primarily occur when operating the uPP at high speed with significant system loading. To avoid this error, run the uPP at slower speeds or reduce background activity, such as non-uPP peripheral or DMA transactions. Additional tuning tips are given in [Section 22.3.10.1](#).

22.3.6.4 DMA Programming Error (DPE) Event

This event occurs when the DMA channel descriptors are programmed while its PEND bit in the uPP DMA channel status register is set to 1. A channel's descriptors should only be programmed while the channel's PEND bit is cleared to 0.

22.3.7 Emulation Considerations

The uPP peripheral stops running if any of three conditions are met:

- Peripheral Disable - EN bit in the uPP peripheral control register (PERCTL) is 0.
- Clock Stop – Clock to uPP is disabled using PCLKCR.
- Emulation Suspend - JTAG emulator halts chip while FREE = 0 and SOFT = 1 in uPP PERCTL register.

For other settings of FREE and SOFT, the uPP peripheral continues running during emulation halt. When the uPP encounters a stop condition, it completes the current DMA burst transaction (if one is active) before stopping.

I/O channel, configured in transmit mode, immediately places its pins in a high-impedance state and preserves the state of its internal state machines. Unless some reset event occurs (see [Section 22.3.5](#)), the channel can resume where it left off when the stop condition is cleared. I/O channel configured in receive mode only captures one additional data word. Further incoming data words are ignored as long as the stop condition persists.

22.3.8 Transmit and Receive FIFOs

Each of the uPP peripheral I/O channels has a 512-byte FIFO. In receive mode, the FIFO is divided into eight 64-byte blocks. In transmit mode, the FIFO is divided into blocks that can be set to 64, 128, or 256 bytes, configured by the TXSIZEA field in the uPP threshold configuration register (THCFG).

Transmission will not begin until the channel has loaded enough data to fill at least one full FIFO block. The internal DMA channels may also be configured to use a read threshold of 64, 128, or 256 bytes using the RDSIZEI or RDSIZEQ field in uPP THCFG register. The DMA write threshold is fixed at 64 bytes.

22.3.9 Transmit and Receive Data (MSG) RAM

On this device, uPP internal DMA doesn't have access to system memories. Instead, there are two dedicated DATA RAMs (also called as MSGRAM) that have been provided: one for each RX and TX; each of these DATA RAMs are 512B. Since C28 CPU/CLA operates in 16-bit addressing mode, whereas, uPP internal DMA operates in byte addressing mode, the addresses for these RAMs are different for different views.

[Table 22-2](#) describes the addresses for these RAMs for two different views.

Table 22-2. CPU/CLA/uPP-DMA Address Map

Data (MSG)RAM	CPU/CLA Address		uPP DMA (programming) Address	
	Start Address	End Address	Start Address	End Address
TX DATA RAM	0x6C00	0x6CFF	0x6C00	0x6dff
RX DATA RAM	0x6E00	0x6EFF	0x7000	0x71ff

[Table 22-3](#) describes the different access type for both the DATA(MSG) RAMs.

Table 22-3. CPU/CLA/uPP-DMA Address Map

Master/Data RAM	TX DATA(MSG) RAM		RX DATA(MSG) RAM	
	Read	Write	Read	Write
CPU1	Yes	Yes	Yes	Yes (Debug Mode Only)
CPU1.CLA1	Yes	Yes	Yes	No
uPP-DMA	Yes	No	No	Yes

NOTE: The message RAMs clocks are gated off when uPP clock is gated by the PCLKCR configuration. Thus, the message RAMs are not accessible by CPU/CLA when RPI clock is disabled by CPU.

22.3.10 Initialization and Operation

This section provides step-by-step instructions for initializing and running the uPP peripheral in various modes. These instructions are given assuming that the device has just come out of a power-on reset (POR) state.

1. Apply the appropriate pin multiplexing settings. For more information, see the device-specific data manual, and (or) pin multiplexing utility.
2. Enable the clocks to the uPP peripheral. For more information, see the **clock control section of this document (???)**.
3. Wait for few (~32) device clock cycles, and then clear the “Soft Reset” bit to 0 to bring the module out of reset.
4. Program the following uPP configuration registers: CHCTL, IFCFG, IFIVAL, THCFG.
 - (a) uPP Channel Control Register (data format, SDR/DDR, TX/RX, single/dual channel, interleave, demux)
 - (b) uPP Interface configuration Register (IO signal enable, polarity, clock divisor)
 - (c) uPP Interface idle value register (to drive value in idle mode for Tx)
 - (d) uPP Threshold configuration register (TX Size, DMA read burst size)
5. Program the uPP interrupt enable set register to interrupt generation for the desired events. Register an interrupt service routine (ISR) if desired; otherwise, polling is required.
6. Set the “PerEn” bit in the uPP peripheral control register (PCR) to 1 to turn on the uPP peripheral.
7. Allocate or initialize data buffers for use with uPP.
8. Program the DMA channels with their first transfers using the uPP DMA channel descriptor register0, 1 and 2 (byte count, line count, line offset).
9. Once the DMA descriptors are written, the module will start to receive and transmit data, and perform DMA transfers. Below is a simple description of how the DMA works.
10. Watch for interrupt events. Reprogram the DMA as necessary. (check that the PEND bit in the uPP DMA channel status is ‘0’).
 - (a) If polling, check uPP Interrupt enabled status register. Reading a bit as 1 indicates the corresponding event has occurred. Write the corresponding bit with 1 to clear.
 - (b) If using ISR, check ENINTST inside your ISR

Once the channel is started, the initial latency between the time when the first data is received or transmitted on the pin, and the time when the first DMA burst is transferred on the CBA bus, is unpredictable. This initial latency is determined by several factors:

- Clock ratio between system clock and uPP clock
- Various threshold values being programmed
- Chip-level traffic activities level

However, once the data is moving, all subsequent data movement is continuous (streaming). If such data movement cannot be maintained, then DMA under-run or over-flow situation may occur.

22.3.10.1 System Tuning Tips

The uPP peripheral can operate at high speed and transfer data at a very high rate. When operating the uPP near its upper limits, tuning certain parameters can help decrease the incidence of errors and the software overhead incurred servicing uPP data. Table 22-4 lists several parameters that can be useful in system tuning. A parameter is defined as a “coarse” adjustment, if changing the parameter directly alters the peripheral throughput. A “fine” adjustment does not change the peripheral throughput, but it does affect general system performance.

Table 22-4. uPP Parameters Useful for System Tuning

Parameter	Register	Register Field	Edge Value	Safe Value	Description
Data Rate	CHCTL	DRA	1	0	Double data rate increases data transfer by a factor of 2 and greatly increases system loading for the same clock divisor. This is a coarse adjustment and is probably fixed due to design constraints.
Clock Division	IFCFG	CLKDIVA	0	1+	Increasing clock division is the most straight-forward way to decrease system loading. This is a coarse adjustment; the difference between CLKDIVx = 0 and 1 is the same (in terms of data rate) as the difference between single and double data rate.
DMA Read Burst Size	THCFG	RDSIZEQ RDSIZEI	0	3h	Increasing the DMA read threshold decreases system loading by generating fewer, larger DMA events. This is a fine adjustment.
DMA Line Size, Count	CHxDESC 1	LCNT BCNT	0		⁽¹⁾ Condensing uPP transfers into fewer, larger lines generates fewer end-of-line interrupts and, thus, invokes fewer ISR calls. This is a fine adjustment.
Total Transfer Size	CHxDESC 1	LCNT BCNT	⁽¹⁾	⁽¹⁾	Performing many small uPP transfers can require excessive software overhead (programming DMA descriptors, handling interrupts, and so forth) at high data rates. This is a fine adjustment.

⁽¹⁾ (1) These values vary per application. One example could be a 16-KB transfer. The same total data could be transferred as 16 1-KB lines or 2 8-KB lines.

22.4 Registers

22.4.1 UPP Base Addresses

Table 22-5. UPP Base Address Table

Device Registers	Register Name	Start Address	End Address
UppRegs ⁽¹⁾	UPP_REGS	0x0000_6200	0x0000_62FF

⁽¹⁾ Only available on CPU1.

22.4.2 UPP_REGS Registers

Table 22-6 lists the memory-mapped registers for the UPP_REGS. All register offset addresses not listed in **Table 22-6** should be considered as reserved locations and the register contents should not be modified.

Table 22-6. UPP_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	PID	Peripheral ID Register	Section 22.4.2.1	
2h	PERCTL	Peripheral Control Register	Section 22.4.2.2	
8h	CHCTL	General Control Register	Section 22.4.2.3	
Ah	IFCFG	Interface Configuration Register	Section 22.4.2.4	
Ch	IFIVAL	Interface Idle Value Register	Section 22.4.2.5	
Eh	THCFG	Threshold Configuration Register	Section 22.4.2.6	
10h	RAWINTST	Raw Interrupt Status Register	Section 22.4.2.7	
12h	ENINTST	Enable Interrupt Status Register	Section 22.4.2.8	
14h	INTENSET	Interrupt Enable Set Register	Section 22.4.2.9	
16h	INTENCLR	Interrupt Enable Clear Register	Section 22.4.2.10	
20h	CHIDESC0	DMA Channel I Descriptor 0 Register	Section 22.4.2.11	
22h	CHIDESC1	DMA Channel I Descriptor 1 Register	Section 22.4.2.12	
24h	CHIDESC2	DMA Channel I Descriptor 2 Register	Section 22.4.2.13	
28h	CHIST0	DMA Channel I Status 0 Register	Section 22.4.2.14	
2Ah	CHIST1	DMA Channel I Status 1 Register	Section 22.4.2.15	
2Ch	CHIST2	DMA Channel I Status 2 Register	Section 22.4.2.16	
30h	CHQDESC0	DMA Channel Q Descriptor 0 Register	Section 22.4.2.17	
32h	CHQDESC1	DMA Channel Q Descriptor 1 Register	Section 22.4.2.18	
34h	CHQDESC2	DMA Channel Q Descriptor 2 Register	Section 22.4.2.19	
38h	CHQST0	DMA Channel Q Status 0 Register	Section 22.4.2.20	
3Ah	CHQST1	DMA Channel Q Status 1 Register	Section 22.4.2.21	
3Ch	CHQST2	DMA Channel Q Status 2 Register	Section 22.4.2.22	
40h	GINTEN	Global Peripheral Interrupt Enable Register	Section 22.4.2.23	
42h	GINTFLG	Global Peripheral Interrupt Flag Register	Section 22.4.2.24	
44h	GINTCLR	Global Peripheral Interrupt Clear Register	Section 22.4.2.25	
46h	DLYCTL	IO clock data skew control Register	Section 22.4.2.26	

22.4.2.1 PID Register (offset = 0h) [reset = 44231100h]

PID is shown in [Figure 22-17](#) and described in [Table 22-7](#).

Peripheral ID Register

Figure 22-17. PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVID																															
R-44231100h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-7. PID Register Field Descriptions

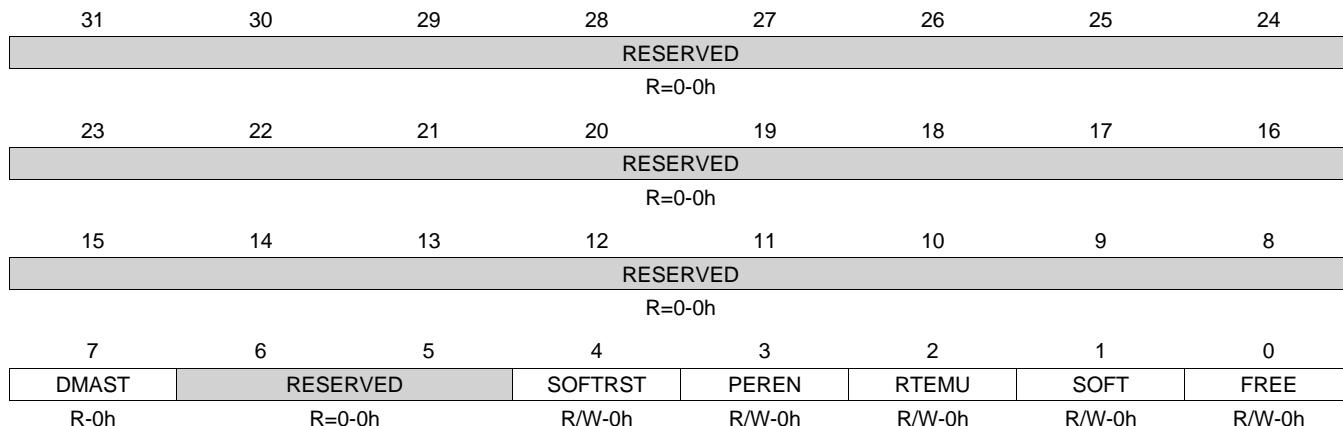
Bit	Field	Type	Reset	Description
31-0	REVID	R	44231100h	Module revision id.

22.4.2.2 PERCTL Register (offset = 2h) [reset = 0h]

PERCTL is shown in [Figure 22-18](#) and described in [Table 22-8](#).

Peripheral Control Register

Figure 22-18. PERCTL Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-8. PERCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R=0	0h	Reserved
7	DMAST	R	0h	DMA state machine status. 0: Idle 1: DMA Burst transaction is active.
6-5	RESERVED	R=0	0h	Reserved
4	SOFTRST	R/W	0h	This bit reset all the state machines and certain memory elements inside the RPI module immediately. Software can write this bit to '1', and later write '0' to bring the RPI module out of reset. Note that MMR are NOT reset, except for Interrupt-Raw-Status Register. This reset can be used to recover the RPI from an error condition. To make sure that a graceful or fail-safe reset is performed, software can first disable the "PerEn" bit, then poll the DMAStatus bit to make sure that all pending VBUSP DMA burst are completed, then perform a software reset. 0: De-assert the reset (out of reset). 1: Assert the reset (in to reset).
3	PEREN	R/W	0h	This bit can be used to disable or suspend the RPI module. When this bit is programmed to be disabled, the RPI will be stopped (suspended) after all current DMA activity are completed. 0: Disable/Suspend the uPP module. 1: Enable/Resume the uPP module.
2	RTEMU	R/W	0h	0: Real Time emulation is disable. Module gets suspended when CPU is suspended. 1: Real Time emulation is enable.
1	SOFT	R/W	0h	0: Hard Stop. 1: Soft Stop.
0	FREE	R/W	0h	0: Software controlled. 1: Free Running.

22.4.2.3 CHCTL Register (offset = 8h) [reset = 0h]

CHCTL is shown in [Figure 22-19](#) and described in [Table 22-9](#).

General Control Register

Figure 22-19. CHCTL Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R=0-0h	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED							DRA
R/W-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	DEMUXA	SDRTXILA	RESERVED	RESERVED	RESERVED	RESERVED	MODE
R/W-0h	R/W-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-9. CHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R=0	0h	Reserved
30-17	RESERVED	R/W	0h	Reserved
16	DRA	R/W	0h	Data rate control. 0: Single Data Rate (SDR). 1: Double Data Rate (DDR).
15-5	RESERVED	R/W	0h	Reserved
4	DEMUXA	R/W	0h	DDR de-multiplexing mode (This bit is only valid for DDR mode): 0: De-multiplexing is disable. 1: De-multiplexing is Enable (split data into 2 DMA channels).
3	SDRTXILA	R/W	0h	Tx SDR interleave mode (This bit is only valid for SDR mode): 0: Interleaving is disable. 1: Interleaving is Enable (split data into 2 DMA channels).
2	RESERVED	R/W	0h	Reserved
1-0	MODE	R/W	0h	Operating mode: 00: Pure input receive mode. 01: Pure output transmit mode. 10: Reserved. 11: Reserved.

22.4.2.4 IFCFG Register (offset = Ah) [reset = 0h]

IFCFG is shown in [Figure 22-20](#) and described in [Table 22-10](#).

Interface Configuration Register

Figure 22-20. IFCFG Register

31	30	29	28	27	26	25	24
RESERVED		RESERVED					
R=0-0h		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		RESERVED					
R=0-0h		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		TRISENA	CLKINVA	CLKDIVA			
R=0-0h		R/W-0h	R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		WAITA	ENAA	STARTA	WAITPOLA	ENAPOLA	STARTPOLA
R=0-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-10. IFCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R=0	0h	Reserved
29-24	RESERVED	R/W	0h	Reserved
23-22	RESERVED	R=0	0h	Reserved
21-16	RESERVED	R/W	0h	Reserved
15-14	RESERVED	R=0	0h	Reserved
13	TRISENA	R/W	0h	Transmit mode output tri-state control: 0: Disable. RPI will not tri-state during idle time and will drive values from the Interface Idle Value Register. 1: Enable. RPI will tri-state during idle time. Idle time is the time before and between Window transfers.
12	CLKINVA	R/W	0h	Clock inversion: 0: Clock is not inverted 1: Clock is inverted When in Rx mode, the clock will be treated as inverted if enabled. When in Tx mode, the clock will be inverted before going out of the pin.
11-8	CLKDIVA	R/W	0h	Clock divider for transmit mode: $TX_IOCLK = CHIP_CLK / 2(N+1)$ Where 'N' is the value programmed into this field.
7-6	RESERVED	R=0	0h	Reserved
5	WAITA	R/W	0h	Enable Usage of WAIT signal: 0: Disable (Tx: ignore wait) 1: Enable (Tx: honor wait) This bit is only valid for transmit mode, receive mode always drive WAIT signal inactive (except for stop_run situation).

Table 22-10. IFCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ENAA	R/W	0h	Enable Usage of ENABLE (WRITE) signal: 0: Disable (Rx: ignore enable) 1: Enable (Rx: honor enable) This bit is only valid for receive mode, transmit mode always drive ENABLE signal active.
3	STARTA	R/W	0h	Enable Usage of START (SELECT) signal: 0: Disable (Rx: ignore start) 1: Enable (Rx: honor start) This bit is only valid for receive mode, transmit mode always drive START signal active.
2	WAITPOLA	R/W	0h	Polarity of WAIT signal: 0: Active High. 1: Active Low.
1	ENAPOLA	R/W	0h	Polarity of ENABLE(WRITE) signal: 0: Active High. 1: Active Low.
0	STARTPOLA	R/W	0h	Polarity of START(SELECT) signal: 0: Active High. 1: Active Low.

22.4.2.5 IFIVAL Register (offset = Ch) [reset = 0h]IFIVAL is shown in [Figure 22-21](#) and described in [Table 22-11](#).

Interface Idle Value Register

Figure 22-21. IFIVAL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VALA							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-11. IFIVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	Reserved
15-9	RESERVED	R/W	0h	Reserved
8-0	VALA	R/W	0h	When in transmit mode, this field holds the value that will be driven out when the channel is idle. This includes both situations when TRISEN field of the RPI Interface Configuration Register is enabled, and when wait-state is inserted by the external receiver (WAIT asserted).

22.4.2.6 THCFG Register (offset = Eh) [reset = 0h]

THCFG is shown in [Figure 22-22](#) and described in [Table 22-12](#).

Threshold Configuration Register

Figure 22-22. THCFG Register

31	30	29	28	27	26	25	24
RESERVED						RESERVED	
R=0-0h						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						TXSIZEA	
R=0-0h						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						RDSIZEQ	
R=0-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						RDSIZEI	
R=0-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-12. THCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R=0	0h	Reserved
25-24	RESERVED	R/W	0h	Reserved
23-18	RESERVED	R=0	0h	Reserved
17-16	TXSIZEA	R/W	0h	I/O Transmit Threshold: 00: 64 Byte 01: 128 Byte 10: Reserved 11: 256 Byte The uPP will hold off transmitting until this threshold is reach in the transmit buffer. The following programming limitation applies: If TX_SIZE = 64B, there is no programming limitation. If TX_SIZE = 128B, descriptor Byte-Count must > 64B. If TX_SIZE = 256B, descriptor Byte-Count must > 192B
15-10	RESERVED	R=0	0h	Reserved
9-8	RDSIZEQ	R/W	0h	DMA Read Threshold for DMA Channel Q: 00: 64 Byte 01: 128 Byte 10: Reserved 11: 256 Byte DMA read burst is based on this value (same as FIFO block size). Note: DMA Write Threshold (write burst) is fixed at 64B.
7-2	RESERVED	R=0	0h	Reserved

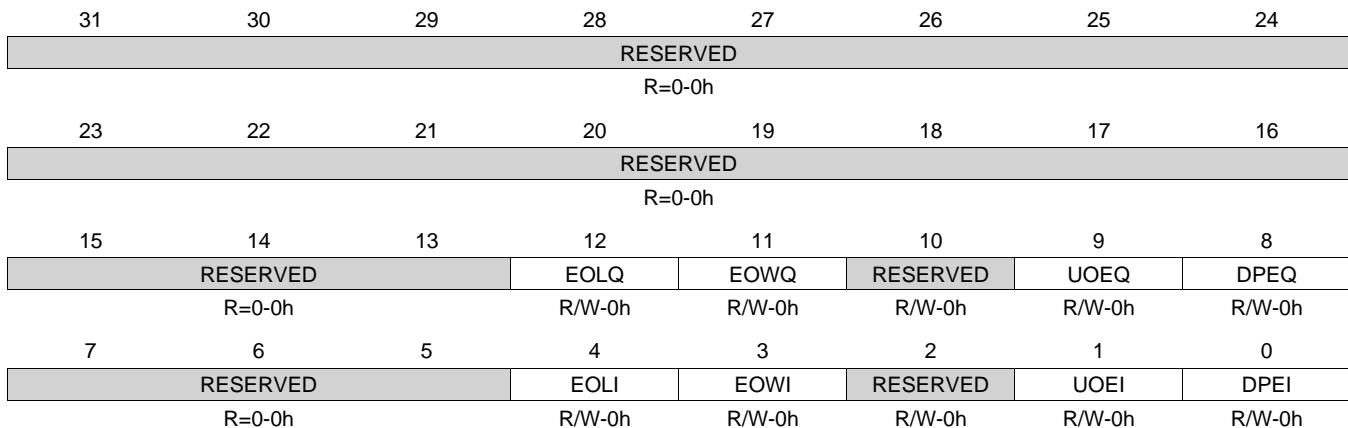
Table 22-12. THCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	RDSIZEI	R/W	0h	DMA Read Threshold for DMA Channel I: 00: 64 Byte 01: 128 Byte 10: Reserved 11: 256 Byte DMA read burst is based on this value (same as FIFO block size). Note: DMA Write Threshold (write burst) is fixed at 64B.

22.4.2.7 RAWINTST Register (offset = 10h) [reset = 0h]

RAWINTST is shown in [Figure 22-23](#) and described in [Table 22-13](#).

Raw Interrupt Status Register

Figure 22-23. RAWINTST Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-13. RAWINTST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R=0	0h	Reserved
12	EOLQ	R/W	0h	Interrupt raw status for end-of-line condition: 0: No event. 1: End Of Line event happened.
11	EOWQ	R/W	0h	Interrupt raw status for end-of-line condition: 0: No event. 1: End Of Window event happened.
10	RESERVED	R/W	0h	Reserved
9	UOEQ	R/W	0h	Interrupt raw status for DMA under-run or over-run : 0: No event. 1: Under-run/Over-run event happened. Over-run in receiving or Under-Run in transmitting.
8	DPEQ	R/W	0h	Interrupt raw status for DMA programming error: 0: No event. 1: DMA programming error (Writing of DMA descriptors while PENDING bit is active) occurred.
7-5	RESERVED	R=0	0h	Reserved
4	EOLI	R/W	0h	Interrupt raw status for end-of-line condition: 0: No event. 1: End Of Line event happened.
3	EOWI	R/W	0h	Interrupt raw status for end-of-line condition: 0: No event. 1: End Of Window event happened.
2	RESERVED	R/W	0h	Reserved

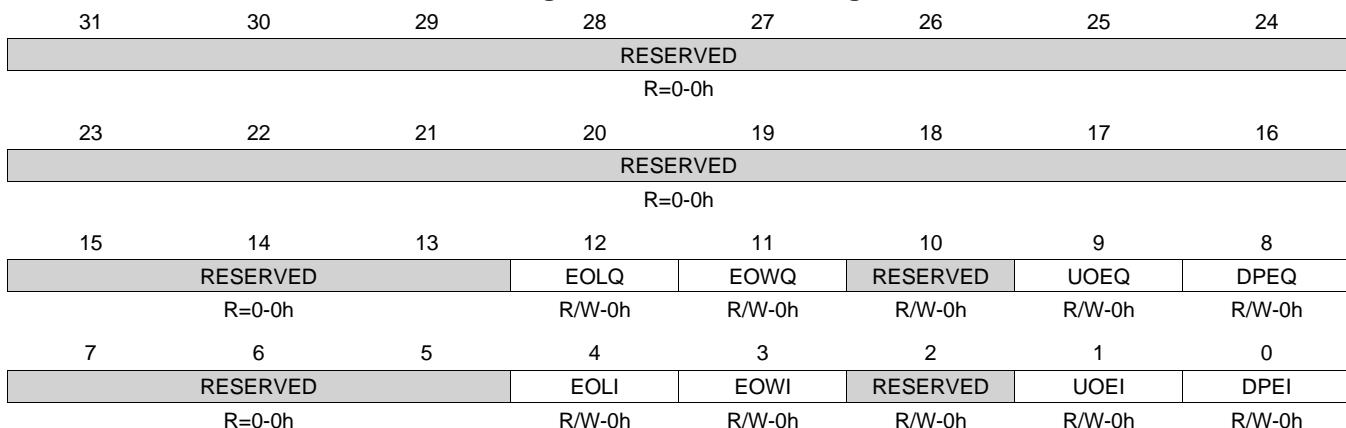
Table 22-13. RAWINTST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UOEI	R/W	0h	Interrupt raw status for DMA under-run or over-run : 0: No event. 1: Under-run/Over-run event happened. Over-run in receiving or Under-Run in transmitting.
0	DPEI	R/W	0h	Interrupt raw status for DMA programming error: 0: No event. 1: DMA programming error (Writing of DMA descriptors while PENDING bit is active) occurred.

22.4.2.8 ENINTST Register (offset = 12h) [reset = 0h]

ENINTST is shown in [Figure 22-24](#) and described in [Table 22-14](#).

Enable Interrupt Status Register

Figure 22-24. ENINTST Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-14. ENINTST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R=0	0h	Reserved
12	EOLQ	R/W	0h	Interrupt enable status for end-of-line condition: 0: No event. 1: End Of Line event happened.
11	EOWQ	R/W	0h	Interrupt enable status for end-of-line condition: 0: No event. 1: End Of Window event happened.
10	RESERVED	R/W	0h	Reserved
9	UOEQ	R/W	0h	Interrupt enable status for DMA under-run or over-run : 0: No event. 1: Under-run/Over-run event happened. Over-run in receiving or Under-Run in transmitting.
8	DPEQ	R/W	0h	Interrupt enable status for DMA programming error: 0: No event. 1: DMA programming error (Writing of DMA descriptors while PENDING bit is active) occurred.
7-5	RESERVED	R=0	0h	Reserved
4	EOLI	R/W	0h	Interrupt enable status for end-of-line condition: 0: No event. 1: End Of Line event happened.
3	EOWI	R/W	0h	Interrupt enable status for end-of-line condition: 0: No event. 1: End Of Window event happened.
2	RESERVED	R/W	0h	Reserved

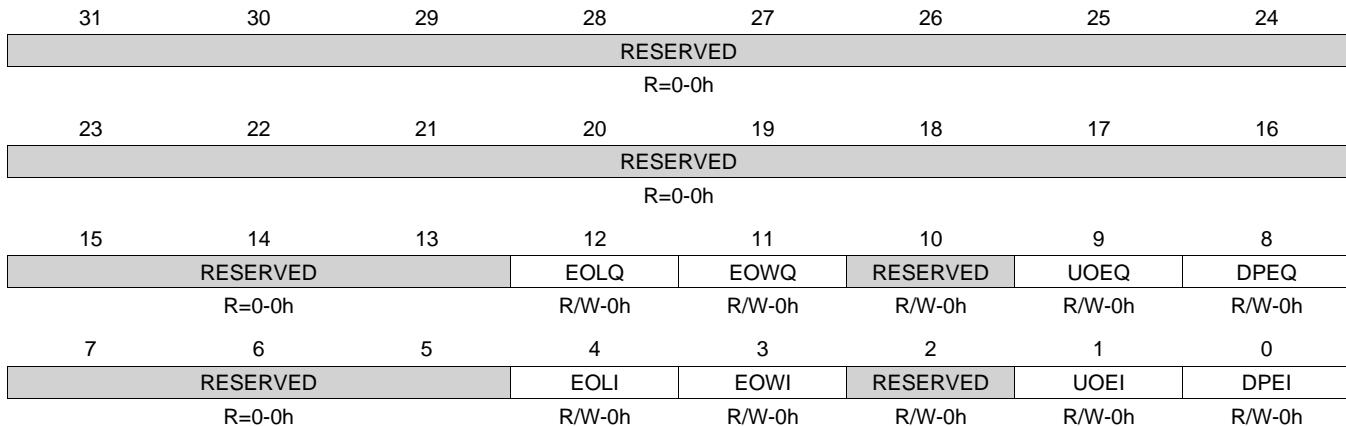
Table 22-14. ENINTST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UOEI	R/W	0h	Interrupt enable status for DMA under-run or over-run : 0: No event. 1: Under-run/Over-run event happened. Over-run in receiving or Under-Run in transmitting.
0	DPEI	R/W	0h	Interrupt enable status for DMA programming error: 0: No event. 1: DMA programming error (Writing of DMA descriptors while PENDING bit is active) occurred.

22.4.2.9 INTENSET Register (offset = 14h) [reset = 0h]

INTENSET is shown in [Figure 22-25](#) and described in [Table 22-15](#).

Interrupt Enable Set Register

Figure 22-25. INTENSET Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-15. INTENSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R=0	0h	Reserved
12	EOLQ	R/W	0h	Interrupt enable for end-of-line condition: 0: Interrupt is disable. 1: Interrupt is enable.
11	EOWQ	R/W	0h	Interrupt enable for end-of-line condition: 0: Interrupt is disable. 1: Interrupt is enable.
10	RESERVED	R/W	0h	Reserved
9	UOEQ	R/W	0h	Interrupt enable for DMA under-run or over-run : 0: Interrupt is disable. 1: Interrupt is enable.
8	DPEQ	R/W	0h	Interrupt enable for DMA programming error: 0: Interrupt is disable. 1: Interrupt is enable.
7-5	RESERVED	R=0	0h	Reserved
4	EOLI	R/W	0h	Interrupt enable for end-of-line condition: 0: Interrupt is disable. 1: Interrupt is enable.
3	EOWI	R/W	0h	Interrupt enable for end-of-line condition: 0: Interrupt is disable. 1: Interrupt is enable.
2	RESERVED	R/W	0h	Reserved
1	UOEI	R/W	0h	Interrupt enable for DMA under-run or over-run : 0: Interrupt is disable. 1: Interrupt is enable. Over-run in receiving or Under-Run in transmitting.

Table 22-15. INTENSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPEI	R/W	0h	Interrupt enable for DMA programming error: 0: Interrupt is disable. 1: Interrupt is enable.

22.4.2.10 INTENCLR Register (offset = 16h) [reset = 0h]

INTENCLR is shown in [Figure 22-26](#) and described in [Table 22-16](#).

Interrupt Enable Clear Register

Figure 22-26. INTENCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED			EOLQ	EOWQ	RESERVED	UOEQ	DPEQ
R=0-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			EOLI	EOWI	RESERVED	UOEI	DPEI
R=0-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-16. INTENCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R=0	0h	Reserved
12	EOLQ	R/W	0h	Interrupt clear for end-of-line condition: 0: No action. 1: Interrupt status gets clear.
11	EOWQ	R/W	0h	Interrupt clear for end-of-line condition: 0: No action. 1: Interrupt status gets clear.
10	RESERVED	R/W	0h	Reserved
9	UOEQ	R/W	0h	Interrupt clear for DMA under-run or over-run : 0: No action. 1: Interrupt status gets clear.
8	DPEQ	R/W	0h	Interrupt clear for DMA programming error: 0: No action. 1: Interrupt status gets clear.
7-5	RESERVED	R=0	0h	Reserved
4	EOLI	R/W	0h	Interrupt clear for end-of-line condition: 0: No action. 1: Interrupt status gets clear.
3	EOWI	R/W	0h	Interrupt clear for end-of-line condition: 0: No action. 1: Interrupt status gets clear.
2	RESERVED	R/W	0h	Reserved
1	UOEI	R/W	0h	Interrupt clear for DMA under-run or over-run : 0: No action. 1: Interrupt status gets clear. Over-run in receiving or Under-Run in transmitting.

Table 22-16. INTENCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPEI	R/W	0h	Interrupt clear for DMA programming error: 0: No action. 1: Interrupt status gets clear.

22.4.2.11 CHIDESC0 Register (offset = 20h) [reset = 0h]

CHIDESC0 is shown in [Figure 22-27](#) and described in [Table 22-17](#).

DMA Channel I Descriptor 0 Register

Figure 22-27. CHIDESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-17. CHIDESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	Starting address of the DMA Channel I transfer. It must be 64bit aligned.

22.4.2.12 CHIDESC1 Register (offset = 22h) [reset = 0h]CHIDESC1 is shown in [Figure 22-28](#) and described in [Table 22-18](#).

DMA Channel I Descriptor 1 Register

Figure 22-28. CHIDESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCNT															BCNT																
R/W-0h															R/W-0h																

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-18. CHIDESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	LCNT	R/W	0h	Number of lines in a window for DMA Channel I transfer(number of packets in CPPI 4.1 terminology): 0: Line count of 0 (invalid programming) 1: Line count of 1 So on...
15-0	BCNT	R/W	0h	Number of bytes in a line for DMA Channel I transfer(number of bytes in a packet in CPPI 4.1 terminology): 0: Byte count of 0 (invalid programming) 1: Byte count of 1 So on...

22.4.2.13 CHIDESC2 Register (offset = 24h) [reset = 0h]

CHIDESC2 is shown in [Figure 22-29](#) and described in [Table 22-19](#).

DMA Channel I Descriptor 2 Register

Figure 22-29. CHIDESC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LOFFSET															

R=0-0h

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-19. CHIDESC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-0	LOFFSET	R/W	0h	Offset from the current line starting address to the next line starting address for DMA Channel I transfers. It must be 64bit aligned.

22.4.2.14 CHIST0 Register (offset = 28h) [reset = 0h]

CHIST0 is shown in [Figure 22-30](#) and described in [Table 22-20](#).

DMA Channel I Status 0 Register

Figure 22-30. CHIST0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

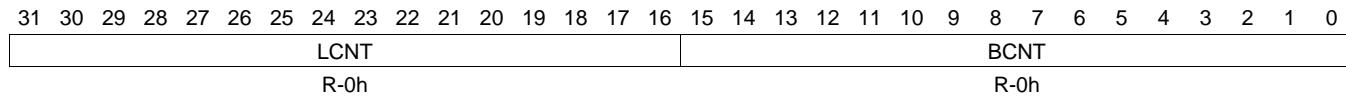
Table 22-20. CHIST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R	0h	Current address of the DMA transfer.

22.4.2.15 CHIST1 Register (offset = 2Ah) [reset = 0h]

CHIST1 is shown in [Figure 22-31](#) and described in [Table 22-21](#).

DMA Channel 1 Status 1 Register

Figure 22-31. CHIST1 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-21. CHIST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	LCNT	R	0h	Current line number.
15-0	BCNT	R	0h	Current byte number.

22.4.2.16 CHIST2 Register (offset = 2Ch) [reset = 0h]

CHIST2 is shown in [Figure 22-32](#) and described in [Table 22-22](#).

DMA Channel I Status 2 Register

Figure 22-32. CHIST2 Register

31	30	29	28	27	26	25	24
RESERVED							
R=0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R=0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R=0-0h							
7	6	5	4	3	2	1	0
WM				RESERVED		PEND	ACT
R-0h				R=0-0h		R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-22. CHIST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R=0	0h	Reserved
7-4	WM	R	0h	Watermark for FIFO block count for DMA Channel I transfer. For RX, this is a recording of the maximum FIFO Block Occupancy ever reached for a continuous transaction. For TX, this is a simple capture of the FIFO Block Emptiness count every clock.
3-2	RESERVED	R=0	0h	Reserved
1	PEND	R	0h	Status of DMA: 0: OK to write a new set of DMA descriptor. 1: Writing of new DMA descriptor is disallowed/ignored.
0	ACT	R	0h	Status of DMA descriptor.t: 0: Descriptor is currently idle. 1: Descriptor is currently active (transferring data). "PENDING" bit is used for descriptor programming allowance, while "ACTIVE" is used for indicating if a descriptor is being in use or not. Software should not use these bit to indicate "end-of-window" transfer condition (use the EOW status/interrupt instead). For RX mode, this bit reflects if any of the 2 pending descriptors on the CBA clock domain is currently running. For TX mode, this bit reflects if any of the 2 pending descriptors on the RPI clock domain is currently running. A proper way to monitor this signal (after loading a descriptor) is to first wait for this ACTIVE signal to go active, then wait for this signal to go inactive. The deassertion of the ACTIVE signal indicates that the descriptor is completed. Another side note is that the "DMA_STATUS" of PCR is a low-level monitoring signal for DMA VBUSP bus activity, while the PENDING, ACTIVE are higher-lever monitoring for descriptor status.

22.4.2.17 CHQDESC0 Register (offset = 30h) [reset = 0h]

CHQDESC0 is shown in [Figure 22-33](#) and described in [Table 22-23](#).

DMA Channel Q Descriptor 0 Register

Figure 22-33. CHQDESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-23. CHQDESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	Starting address of the DMA Channel Q transfer. This must be 64bit aligned.

22.4.2.18 CHQDESC1 Register (offset = 32h) [reset = 0h]CHQDESC1 is shown in [Figure 22-34](#) and described in [Table 22-24](#).

DMA Channel Q Descriptor 1 Register

Figure 22-34. CHQDESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCNT																BCNT															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-24. CHQDESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	LCNT	R/W	0h	Number of lines in a window for DMA Channel Q transfer(number of packets in CPPI 4.1 terminology): 0: Line count of 0 (invalid programming) 1: Line count of 1 So on...
15-0	BCNT	R/W	0h	Number of bytes in a line for DMA Channel Q transfer(number of bytes in a packet in CPPI 4.1 terminology): 0: Byte count of 0 (invalid programming) 1: Byte count of 1 So on...

22.4.2.19 CHQDESC2 Register (offset = 34h) [reset = 0h]

CHQDESC2 is shown in [Figure 22-35](#) and described in [Table 22-25](#).

DMA Channel Q Descriptor 2 Register

Figure 22-35. CHQDESC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LOFFSET															

R=0-0h

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-25. CHQDESC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R=0	0h	Reserved
15-0	LOFFSET	R/W	0h	Offset from the current line starting address to the next line starting address for DMA Channel Q transfers. It must be 64bit aligned.

22.4.2.20 CHQST0 Register (offset = 38h) [reset = 0h]CHQST0 is shown in [Figure 22-36](#) and described in [Table 22-26](#).

DMA Channel Q Status 0 Register

Figure 22-36. CHQST0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-26. CHQST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R	0h	Current address of the DMA transfer.

22.4.2.21 CHQST1 Register (offset = 3Ah) [reset = 0h]

CHQST1 is shown in [Figure 22-37](#) and described in [Table 22-27](#).

DMA Channel Q Status 1 Register

Figure 22-37. CHQST1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCNT																BCNT															
R-0h																R-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-27. CHQST1 Register Field Descriptions

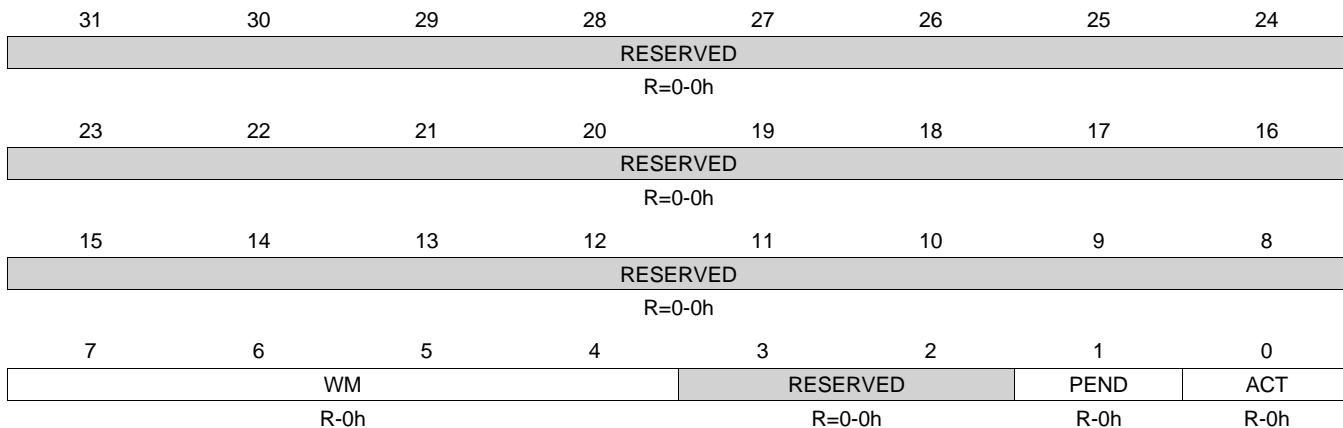
Bit	Field	Type	Reset	Description
31-16	LCNT	R	0h	Current line number.
15-0	BCNT	R	0h	Current byte number.

22.4.2.22 CHQST2 Register (offset = 3Ch) [reset = 0h]

CHQST2 is shown in [Figure 22-38](#) and described in [Table 22-28](#).

DMA Channel Q Status 2 Register

Figure 22-38. CHQST2 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

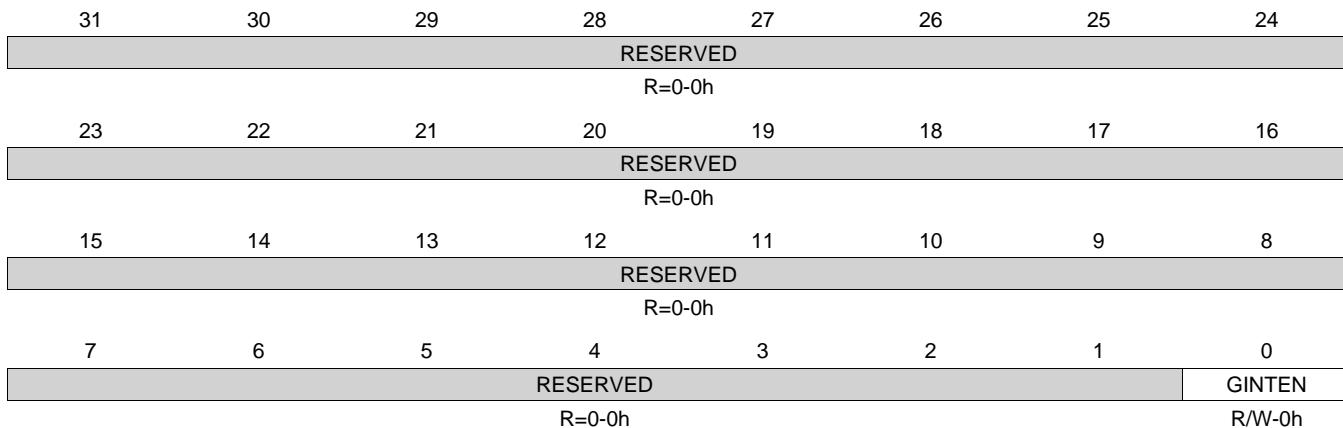
Table 22-28. CHQST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R=0	0h	Reserved
7-4	WM	R	0h	Watermark for FIFO block count for DMA Channel Q transfer. For RX, this is a recording of the maximum FIFO Block Occupancy ever reached for a continuous transaction. For TX, this is a simple capture of the FIFO Block Emptiness count every clock.
3-2	RESERVED	R=0	0h	Reserved
1	PEND	R	0h	Status of DMA: 0: OK to write a new set of DMA descriptor. 1: Writing of new DMA descriptor is disallowed/ignored.
0	ACT	R	0h	Status of DMA descriptor.t: 0: Descriptor is currently idle. 1: Descriptor is currently active (transferring data). "PENDING" bit is used for descriptor programming allowance, while "ACTIVE" is used for indicating if a descriptor is being in use or not. Software should not use these bit to indicate "end-of-window" transfer condition (use the EOW status/interrupt instead). For RX mode, this bit reflects if any of the 2 pending descriptors on the CBA clock domain is currently running. For TX mode, this bit reflects if any of the 2 pending descriptors on the RPI clock domain is currently running. A proper way to monitor this signal (after loading a descriptor) is to first wait for this ACTIVE signal to go active, then wait for this signal to go inactive. The deassertion of the ACTIVE signal indicates that the descriptor is completed. Another side note is that the "DMA_STATUS" of PCR is a low-level monitoring signal for DMA VBUSP bus activity, while the PENDING, ACTIVE are higher-lever monitoring for descriptor status.

22.4.2.23 GINTEN Register (offset = 40h) [reset = 0h]

GINTEN is shown in [Figure 22-39](#) and described in [Table 22-29](#).

Global Peripheral Interrupt Enable Register

Figure 22-39. GINTEN Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

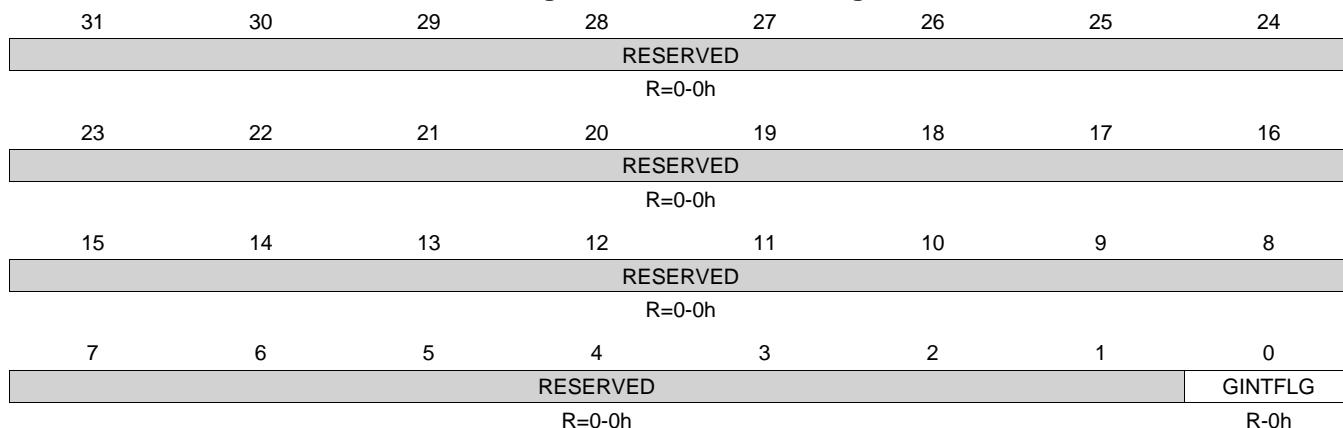
Table 22-29. GINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R=0	0h	Reserved
0	GINTEN	R/W	0h	0 = uPP does not generate interrupt. 1= uPP generates interrupt to if interrupt flag gets set.

22.4.2.24 GINTFLG Register (offset = 42h) [reset = 0h]

GINTFLG is shown in [Figure 22-40](#) and described in [Table 22-30](#).

Global Peripheral Interrupt Flag Register

Figure 22-40. GINTFLG Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

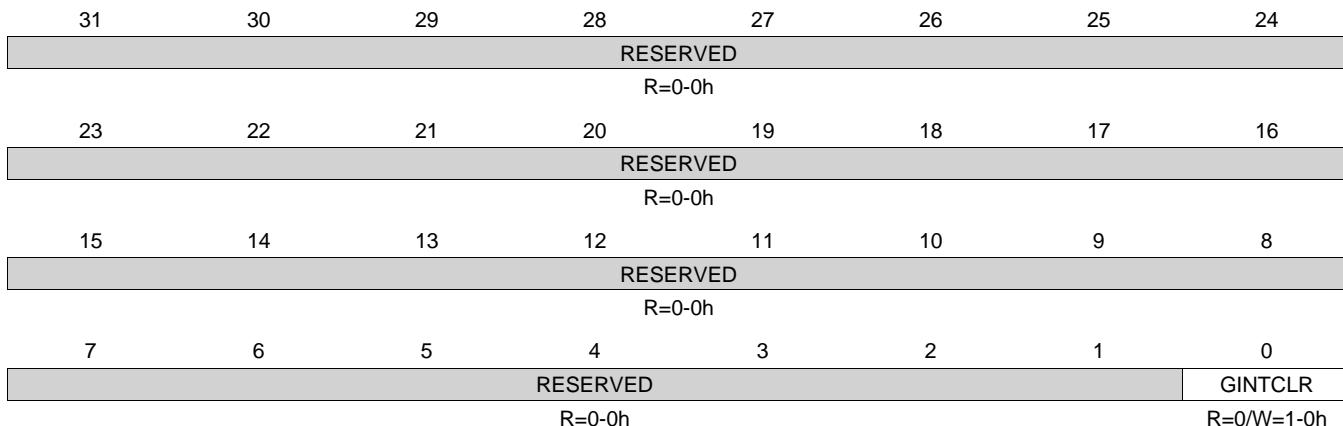
Table 22-30. GINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R=0	0h	Reserved
0	GINTFLG	R	0h	0: No interrupt has been generated. 1: Interrupt has been generated.

22.4.2.25 GINTCLR Register (offset = 44h) [reset = 0h]

GINTCLR is shown in [Figure 22-41](#) and described in [Table 22-31](#).

Global Peripheral Interrupt Clear Register

Figure 22-41. GINTCLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

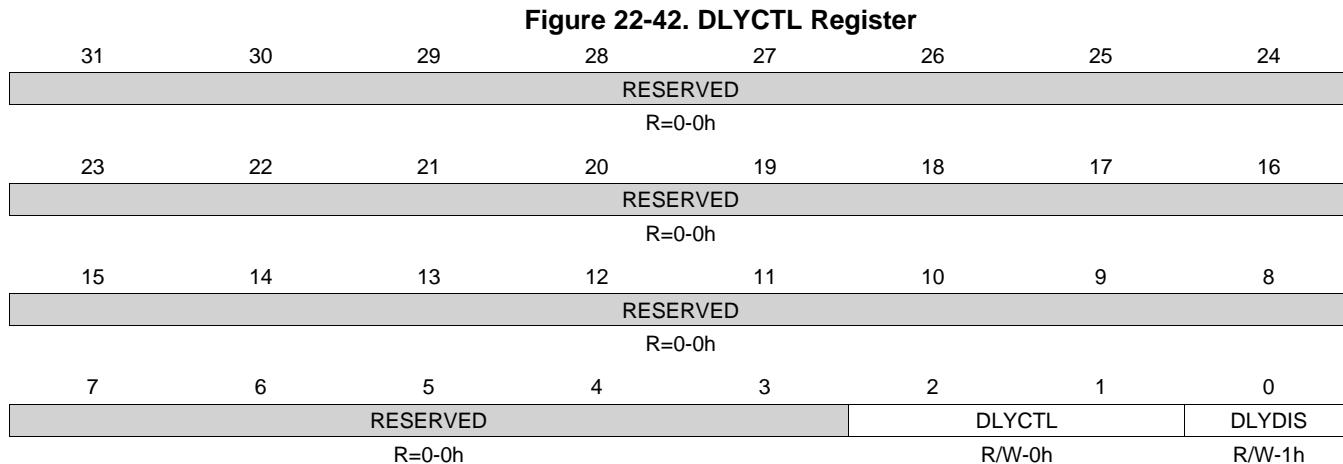
Table 22-31. GINTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R=0	0h	Reserved
0	GINTCLR	R=0/W=1	0h	Write '1' to this clears the flag in GINTFR. Read always returns '0'.

22.4.2.26 DLYCTL Register (offset = 46h) [reset = 1h]

DLYCTL is shown in [Figure 22-42](#) and described in [Table 22-32](#).

IO clock data skew control Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 22-32. DLYCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R=0	0h	Reserved
2-1	DLYCTL	R/W	0h	<p>Controls the delay on the input signals for uPP.</p> <p>00: Data and control pins have 4 cycle delay, clock pins have 2 cycle delay.</p> <p>01: Data and control pins have 6 cycle delay, clock pins have 2 cycle delay.</p> <p>10: Data and control pins have 9 cycle delay, clock pins have 2 cycle delay.</p> <p>11: Data and control pins have 14 cycle delay, clock pins have 2 cycle delay.</p>
0	DLYDIS	R/W	1h	<p>0: Delay on pins are controlled by setting in DLYCTL field.</p> <p>1: No extra delay on pins.</p>

External Memory Interface (EMIF)

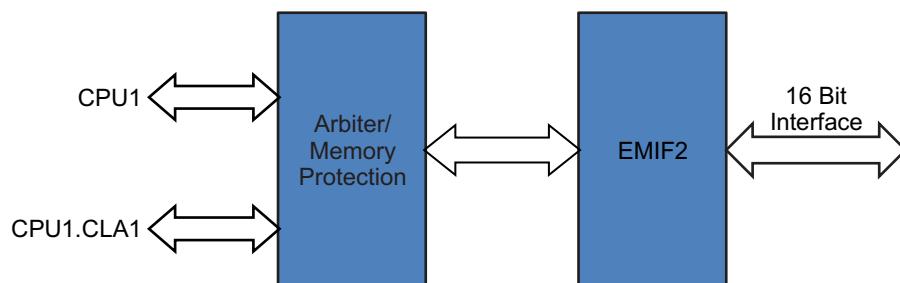
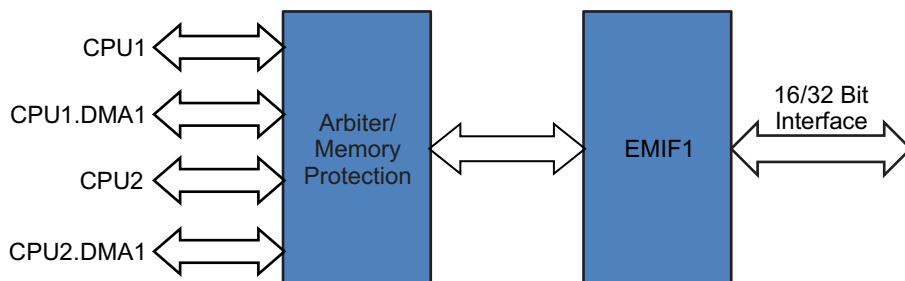
This chapter describes the external memory Interface (EMIF).

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23.3 Example Configuration	2342
23.4 Registers	2349

23.1 Introduction

The F2837Dx device supports dual-core architecture; in order to have a dedicated EMIF for each CPU subsystem, the device supports two EMIF modules — EMIF1 and EMIF2. Both modules are exactly the same with the same feature set, but have different address/data sizes. EMIF1 is shared between the CPU1 and CPU2 subsystem, whereas EMIF2 is dedicated to the CPU1 subsystem. [Figure 23-1](#) represents the two modules.

Figure 23-1. CPU1 and CPU2 Shared Subsystems



[Table 23-1](#) gives the configuration for two EMIF modules.

Table 23-1. Configuration for EMIF1 and EMIF2 Modules

	EMIF1	EMIF2
176 Pin Package	Yes	NA
337 Pin Package	Yes	Yes
Max Data Width	32	16
Max Address Width	22 (Some of the EMIF1 pins are muxed with each other. Please refer IO mux section for exact usage)	12
SDRAM CSx Support	1 (CS0)	1(CS0)
ASRAM CSx Support	3 (CS2/CS3/CS4)	1(CS2)

Subsequent sections in this chapter will provide the details on generic EMIF modules unless otherwise specified.

23.1.1 Purpose of the Peripheral

This EMIF memory controller is compliant with the JESD21-C SDR SDRAM memories utilizing a 32-bit/16-bit data bus. The purpose of this EMIF is to provide a means for the CPU to connect to a variety of external devices including:

- Single data rate (SDR) SDRAM

- Asynchronous devices including NOR Flash and SRAM

The most common use for the EMIF is to interface with both a flash device and an SDRAM device simultaneously. contains an example of operating the EMIF in this configuration.

23.1.2 Features

The EMIF includes many features to enhance the ease and flexibility of connecting to external SDR SDRAM and asynchronous devices.

23.1.2.1 Asynchronous Memory Support

EMIF supports asynchronous:

- SRAM memories
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects (EMIF_nCS[4:2]). Each chip select has the following individually programmable attributes:

- Data Bus Width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turn-around time
- Extended Wait Option with Programmable Timeout
- Select Strobe option

23.1.2.2 Synchronous DRAM Memory Support

The EMIF module supports 16-bit/32-bit SDRAM in addition to the asynchronous memories listed in [Section 23.1.2.1](#). It has a single SDRAM chip select (EMIF_nCS[0]). SDRAM configurations that are supported are:

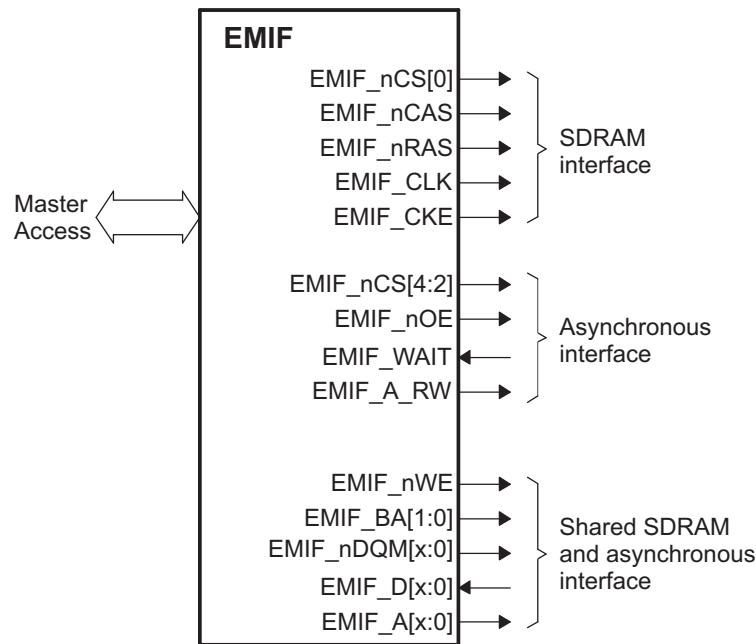
- One, Two and Four Bank SDRAM devices
- Devices with Eight, Nine, Ten, and Eleven Column Address
- CAS Latency of two or three clock cycles
- 16-bit/32-bit Data Bus Width
- 3.3V LVCMOS Interface

Additionally, the EMIF supports placing the SDRAM in Self-Refresh and Powerdown modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents; since the SDRAM will continue to refresh itself even without clocks from the microcontroller. Powerdown mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required.

Note that the EMIF module does not support Mobile SDRAM devices.

23.1.3 Functional Block Diagram

[Figure 23-2](#) illustrates the connections between the EMIF and its internal requesters, along with the external EMIF pins. [Section 23.2.2](#) contains a description of the entities internal to the SoC that can send requests to the EMIF, along with their prioritization. [Section 23.2.3](#) describes the EMIF external pins and summarizes their purpose when interfacing with SDRAM and asynchronous devices.

Figure 23-2. EMIF Functional Block Diagram

23.2 EMIF Module Architecture

This section provides details about the architecture and operation of the EMIF. Both, SDRAM and asynchronous Interface are covered, along with other system-related issues such as clock control.

23.2.1 EMIF Clock Control

The EMIF clock is output on the EMIF_CLK pin and should be used when interfacing to external SDRAM devices. The EMIF module gets the PLLSYSCLK clock domain as the input. The user can choose to run the EMIF at PLLSYSCLK/1 or PLLSYSCLK/2 clock frequency by configuring the EMIFxCLKDIV field in the PERCLKDIVSEL register in the Clock Control module.

23.2.2 EMIF Requests

Different sources within the SoC can make requests to the EMIF. These requests consist of accesses to SDRAM memory, asynchronous memory, and EMIF registers. The EMIF can process only one request at a time. Therefore a high performance crossbar switch exists within the SoC to provide prioritized requests from the different sources to the EMIF. The sources are:

- CPU1
- CPU1.DMA1
- CPU2
- CPU2.DMA1

If a request is submitted from two or more sources simultaneously, the crossbar switch will forward the highest priority request to the EMIF first. Upon completion of a request, the crossbar switch again evaluates the pending requests and forwards the highest priority pending request to the EMIF.

The crossbar switch only allows RD access from all the masters. But for WR access (or execute access in case of CPUx), the crossbar switch only allows access of masters from a CPU subsystem which grabs master ownership of EMIF based on the configuration in the EMIF1MSEL register in the Memory Controller module.

When the EMIF receives a request, it may or may not be immediately processed. In some cases, the EMIF will perform one or more auto refresh cycles before processing the request. For details on the EMIF's internal arbitration between performing requests and performing auto refresh cycles, see [Section 23.2.13](#).

23.2.3 EMIF Signal Descriptions

This section describes the function of each of the EMIF signals.

Table 23-2. EMIF Pins Used to Access Both SDRAM and Asynchronous Memories

Pins(s)	I/O	Description
EMIF_D[x:0]	I/O	EMIF data bus.
EMIF_A[x:0]	O	EMIF address bus. When interfacing to an SDRAM device, these pins are primarily used to provide the row and column address to the SDRAM. The mapping from the internal program address to the external values placed on these pins can be found in Table 23-14 . EMIF_A[10] is also used during the PRE command to select which banks to deactivate. When interfacing to an asynchronous device, these pins are used in conjunction with the EMIF_BA pins to form the address that is sent to the device. The mapping from the internal program address to the external values placed on these pins can be found in Section 23.2.6.1 .
EMIF_BA[1:0]	O	EMIF bank address. When interfacing to an SDRAM device, these pins are used to provide the bank address inputs to the SDRAM. The mapping from the internal program address to the external values placed on these pins can be found in Table 23-14 . When interfacing to an asynchronous device, these pins are used in conjunction with the EMIF_A pins to form the address that is sent to the device. The mapping from the internal program address to the external values placed on these pins can be found in Section 23.2.6.1 .

Table 23-2. EMIF Pins Used to Access Both SDRAM and Asynchronous Memories (continued)

Pins(s)	I/O	Description
EMIF_nDQM[x:0]	O	Active-low byte enables. When interfacing to SDRAM, these pins are connected to the DQM pins of the SDRAM to individually enable/disable each of the bytes in a data access. When interfacing to an asynchronous device, these pins are connected to byte enables. See Section 23.2.6 for details.
EMIF_nWE	O	Active-low write enable. When interfacing to SDRAM, this pin is connected to the nWE pin of the SDRAM and is used to send commands to the device. When interfacing to an asynchronous device, this pin provides a signal which is active-low during the strobe period of an asynchronous write access cycle.

Table 23-3. EMIF Pins Specific to SDRAM

Pin(s)	I/O	Description
EMIF_nCS[0]	O	Active-low chip enable pin for SDRAM devices. This pin is connected to the chip-select pin of the attached SDRAM device and is used for enabling/disabling commands. By default, the EMIF keeps this SDRAM chip select active, even if the EMIF is not interfaced with an SDRAM device. This pin is deactivated when accessing the asynchronous memory bank and is reactivated on completion of the asynchronous access.
EMIF_nRAS	O	Active-low row address strobe pin. This pin is connected to the nRAS pin of the attached SDRAM device and is used for sending commands to the device.
EMIF_nCAS	O	Active-low column address strobe pin. This pin is connected to the nCAS pin of the attached SDRAM device and is used for sending commands to the device.
EMIF_CKE	O	Clock enable pin. This pin is connected to the CKE pin of the attached SDRAM device and is used for issuing the SELF REFRESH command which places the device in self refresh mode. See Section 23.2.5.7 for details.
EMIF_CLK	O	SDRAM clock pin. This pin is connected to the CLK pin of the attached SDRAM device. See Section 23.2.1 for details on the clock signal.

Table 23-4. EMIF Pins Specific to Asynchronous Memory

Pin(s)	I/O	Description
EMIF_nCS[4:2]	O	Active-low chip enable pins for asynchronous devices. These pins are meant to be connected to the chip-select pins of the attached asynchronous device. These pins are active only during accesses to the asynchronous memory.
EMIF_nWAIT	I	Wait input with programmable polarity. A connected asynchronous device can extend the strobe period of an access cycle by asserting the EMIF_nWAIT input to the EMIF as described in Section 23.2.6.6 . To enable this functionality, the EW bit in the asynchronous 1 configuration register (CE2CFG) must be set to 1. In addition, the WP0 bit in CE2CFG must be configured to define the polarity of the EMIF_nWAIT pin.
EMIF_nOE	O	Active-low pin enable for asynchronous devices. This pin provides a signal which is active-low during the strobe period of an asynchronous read access cycle.
EMIF_RnW	O	EMIF asynchronous read/write control. This pin stays high during reads and stays low during writes (same duration as CS).

23.2.4 EMIF Signal Multiplexing Control

Several EMIF signals are multiplexed with other functions on this microcontroller. Please refer to the I/O Multiplexing Module chapter of the technical reference manual for more information on how to enable the output of these EMIF signals.

23.2.5 SDRAM Controller and Interface

The EMIF can gluelessly interface to most standard SDR SDRAM devices and supports such features as self refresh mode and prioritized refresh. In addition, it provides flexibility through programmable parameters such as the refresh rate, CAS latency, and many SDRAM timing parameters. The following sections include details on how to interface and properly configure the EMIF to perform read and write operations to externally connected SDR SDRAM devices. Also, provides a detailed example of interfacing the EMIF to a common SDRAM device.

23.2.5.1 SDRAM Commands

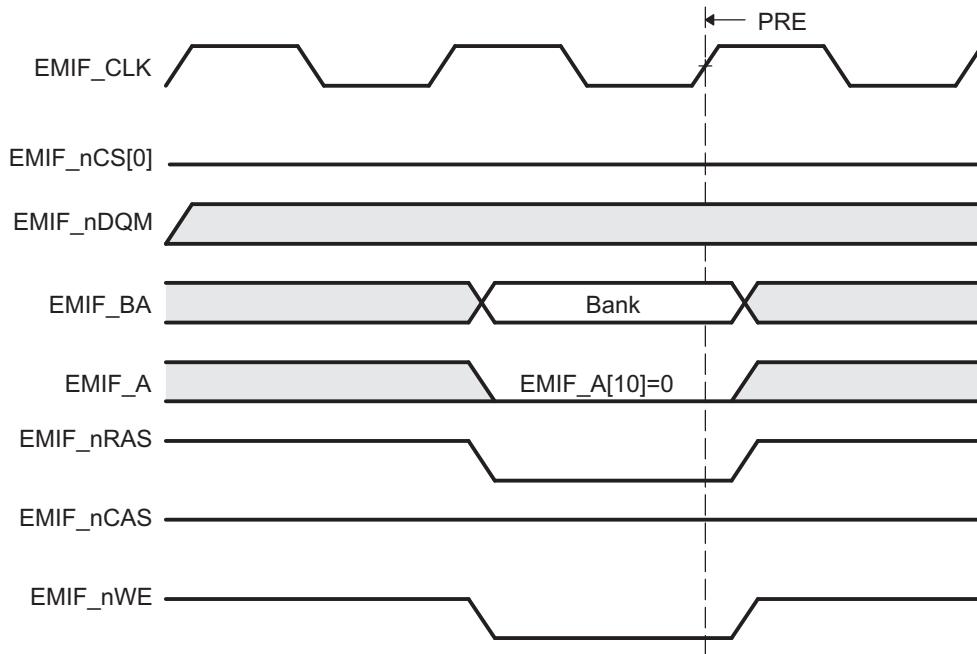
The EMIF supports the SDRAM commands described in [Table 23-5](#). [Table 23-6](#) shows the truth table for the SDRAM commands, and an example timing waveform of the PRE command is shown in [Figure 23-3](#). EMIF_A[10] is pulled low in this example to deactivate only the bank specified by the EMIF_BA pins.

Table 23-5. EMIF SDRAM Commands

Command	Function
PRE	Precharge. Depending on the value of EMIF_A[10], the PRE command either deactivates the open row in all banks (EMIF_A[10] = 1) or only the bank specified by the EMIF_BA[1:0] pins (EMIF_A[10] = 0).
ACTV	Activate. The ACTV command activates the selected row in a particular bank for the current access.
READ	Read. The READ command outputs the starting column address and signals the SDRAM to begin the burst read operation. Address EMIF_A[10] is always pulled low to avoid auto precharge. This allows for better bank interleaving performance.
WRT	Write. The WRT command outputs the starting column address and signals the SDRAM to begin the burst write operation. Address EMIF_A[10] is always pulled low to avoid auto precharge. This allows for better bank interleaving performance.
BT	Burst terminate. The BT command is used to truncate the current read or write burst request.
LMR	Load mode register. The LMR command sets the mode register of the attached SDRAM devices and is only issued during the SDRAM initialization sequence described in Section 23.2.5.4 .
REFR	Auto refresh. The REFR command signals the SDRAM to perform an auto refresh according to its internal address.
SLFR	Self refresh. The self refresh command places the SDRAM into self refresh mode, during which it provides its own clock signal and auto refresh cycles.
NOP	No operation. The NOP command is issued during all cycles in which one of the above commands is not issued.

Table 23-6. Truth Table for SDRAM Commands

SDRAM Pins:	CKE	nCS	nRAS	nCAS	nWE	BA[1:0]	A[12:11]	A[10]	A[9:0]
EMIF Pins:	EMIF_CKE	EMIF_nCS[0]	EMIF_nRAS	EMIF_nCAS	EMIF_nWE	EMIF_BA[1:0]	EMIF_A[12:11]	EMIF_A[10]	EMIF_A[9:0]
PRE	H	L	L	H	L	Bank/X	X	L/H	X
ACTV	H	L	L	H	H	Bank	Row	Row	Row
READ	H	L	H	L	H	Bank	Column	L	Column
WRT	H	L	H	L	L	Bank	Column	L	Column
BT	H	L	H	H	L	X	X	X	X
LMR	H	L	L	L	L	X	Mode	Mode	Mode
REFR	H	L	L	L	H	X	X	X	X
SLFR	L	L	L	L	H	X	X	X	X
NOP	H	L	H	H	H	X	X	X	X

Figure 23-3. Timing Waveform of SDRAM PRE Command

23.2.5.2 Interfacing to SDRAM

The EMIF supports a glueless interface to SDRAM devices with the following characteristics:

- Pre-charge bit is A[10]
- The number of column address bits is 8, 9, 10, or 11.
- The number of row address bits is 13, 14, 15, or 16.
- The number of internal banks is 1, 2, or 4.

[Figure 23-4](#) shows an interface between the EMIF and a $2M \times 16 \times 4$ bank SDRAM device, and [Figure 23-5](#) shows an interface between the EMIF and a $512K \times 16 \times 2$ bank SDRAM device. For devices supporting 16-bit interface, refer to [Table 23-7](#) for list of commonly-supported SDRAM devices and the required connections for the address pins.

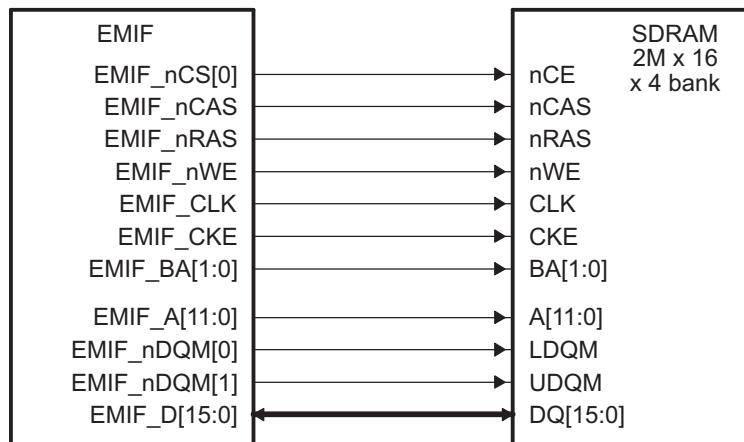
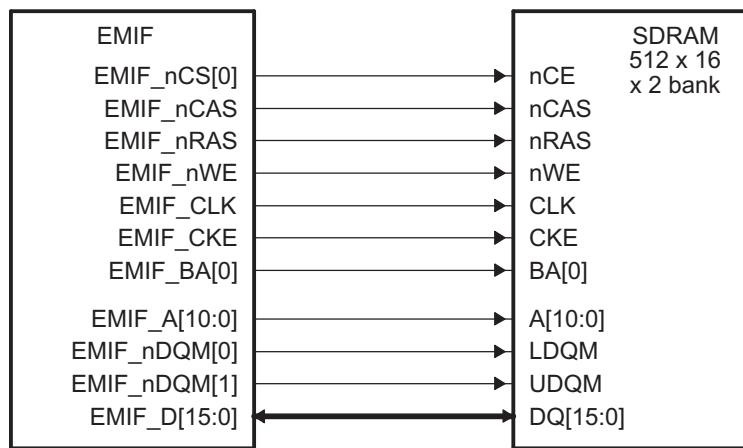
Figure 23-4. EMIF to $2M \times 16 \times 4$ bank SDRAM Interface

Figure 23-5. EMIF to 512K × 16 × 2 bank SDRAM Interface**Table 23-7. 16-bit EMIF Address Pin Connections**

SDRAM Size	Width	Banks	Device	Address Pins
16M bits	x16	2	SDRAM	A[10:0]
			EMIF	EMIF_A[10:0]
64M bits	x16	4	SDRAM	A[11:0]
			EMIF	EMIF_A[11:0]
128M bits	x16	4	SDRAM	A[11:0]
			EMIF	EMIF_A[11:0]
256M bits	x16	4	SDRAM	A[12:0]
			EMIF	EMIF_A[12:0]
512M bits	x16	4	SDRAM	A[12:0]
			EMIF	EMIF_A[12:0]

23.2.5.3 SDRAM Configuration Registers

The operation of the EMIF's SDRAM interface is controlled by programming the appropriate configuration registers. This section describes the purpose and function of each configuration register, but should be referred for a more detailed description of each register, including the default registers values and bit-field positions. The following tables list the four such configuration registers, along with a description of each of their programmable fields.

NOTE: Writing to any of the fields: NM, CL, IBANK, and PAGESIZE in the SDRAM configuration register (SDCR) causes the EMIF to abandon whatever it is currently doing and trigger the SDRAM initialization procedure described in [Section 23.2.5.4](#).

Table 23-8. Description of the SDRAM Configuration Register (SDCR)

Parameter	Description
SR	This bit controls entering and exiting of the Self-Refresh mode. The field should be written using a byte-write to the upper byte of SDCR to avoid triggering the SDRAM initialization sequence.
PD	This bit controls entering and exiting of the Power down mode. The field should be written using a byte-write to the upper byte of SDCR to avoid triggering the SDRAM initialization sequence. If both SR and PD bits are set, the EMIF will go into Self Refresh.
PDWR	Perform refreshes during Power Down. Writing a 1 to this bit will cause the EMIF to exit the power down state and issue an AUTO REFRESH command every time Refresh May level is set. The field should be written using a byte-write to the upper byte of SDCR to avoid triggering the SDRAM initialization sequence. This bit should be set along with PD when entering power-down mode.
NM	Narrow Mode. This bit defines the width of the data bus between the EMIF and the attached SDRAM device. When set to 1, the data bus is set to 16-bits. When set to 0, the data bus is set to 32-bits. This bit must always be set to 1.
CL	CAS latency. This field defines the number of clock cycles between when an SDRAM issues a READ command and when the first piece of data appears on the bus. The value in this field is sent to the attached SDRAM device via the LOAD MODE REGISTER command during the SDRAM initialization procedure as described in Section 23.2.5.4 . Only, values of 2h (CAS latency = 2) and 3h (CAS latency = 3) are supported and should be written to this field. A 1 must be simultaneously written to the BIT11_9LOCK bit field of SDCR in order to write to the CL bit field.
IBANK	Number of Internal SDRAM Banks. This field defines the number of banks inside the attached SDRAM devices in the following way: <ul style="list-style-type: none"> When IBANK = 0, 1 internal bank is used When IBANK = 1h, 2 internal banks are used When IBANK = 2h, 4 internal banks are used This field value affects the mapping of logical addresses to SDRAM row, column, and bank addresses. See Section 23.2.5.11 for details.
PAGESIZE	Page Size. This field defines the internal page size of the attached SDRAM devices in the following way: <ul style="list-style-type: none"> When PAGESIZE = 0, 256-word pages are used When PAGESIZE = 1h, 512-word pages are used When PAGESIZE = 2h, 1024-word pages are used When PAGESIZE = 3h, 2048-word pages are used This field value affects the mapping of logical addresses to SDRAM row, column, and bank addresses. See Section 23.2.5.11 for details.

Table 23-9. Description of the SDRAM Refresh Control Register (SDRCR)

Parameter	Description
RR	Refresh Rate. This field controls the rate at which attached SDRAM devices will be refreshed. The following equation can be used to determine the required value of RR for an SDRAM device: <ul style="list-style-type: none"> $RR = f_{EMIF_CLK} / (\text{Required SDRAM Refresh Rate})$ More information about the operation of the SDRAM refresh controller can be found in Section 23.2.5.6 .

Table 23-10. Description of the SDRAM Timing Register (SDTIMR)

Parameter	Description
T_RFC	SDRAM Timing Parameters. These fields configure the EMIF to comply with the AC timing requirements of the attached SDRAM devices. This allows the EMIF to avoid violating SDRAM timing constraints and to more efficiently schedule its operations. More details about each of these parameters can be found in the register description in . These parameters should be set to satisfy the corresponding timing requirements found in the SDRAM's datasheet.
T_RP	
T_RCD	
T_WR	
T_RAS	
T_RC	
T_RRD	

Table 23-11. Description of the SDRAM Self Refresh Exit Timing Register (SDSRETR)

Parameter	Description
T_XS	Self Refresh Exit Parameter. The T_XS field of this register informs the EMIF about the minimum number of EMIF_CLK cycles required between exiting Self Refresh and issuing any command. This parameter should be set to satisfy the t_{XSR} value for the attached SDRAM device.

23.2.5.4 SDRAM Auto-Initialization Sequence

The EMIF automatically performs an SDRAM initialization sequence, regardless of whether it is interfaced to an SDRAM device, when either of the following two events occur:

- The EMIF comes out of reset. No memory accesses to the SDRAM and Asynchronous interfaces are performed until this auto-initialization is complete.
- A write is performed to any of the three least significant bytes of the SDRAM configuration register (SDCR)

An SDRAM initialization sequence consists of the following steps:

1. If the initialization sequence is activated by a write to SDCR, and if any of the SDRAM banks are open, the EMIF issues a PRE command with EMIF_A[10] held high to indicate all banks. This is done so that the maximum ACTV to PRE timing for an SDRAM is not violated.
2. The EMIF drives EMIF_CKE high and begins continuously issuing NOP commands until eight SDRAM refresh intervals have elapsed. An SDRAM refresh interval is equal to the value of the RR field of SDRAM refresh control register (SDRCR), divided by the frequency of EMIF_CLK (RR/f_{EMIF_CLK}). This step is used to avoid violating the Power-up constraint of most SDRAM devices that requires 200 μ s (sometimes 100 μ s) between receiving stable Vdd and CLK and the issuing of a PRE command. Depending on the frequency of EMIF_CLK, this step may or may not be sufficient to avoid violating the SDRAM constraint. See [Section 23.2.5.5](#) for more information.
3. After the refresh intervals have elapsed, the EMIF issues a PRE command with EMIF_A[10] held high to indicate all banks.
4. The EMIF issues eight AUTO REFRESH commands.
5. The EMIF issues the LMR command with the EMIF_A[9:0] pins set as described in [Table 23-12](#).
6. Finally, the EMIF performs a refresh cycle, which consists of the following steps:
 - (a) Issuing a PRE command with EMIF_A[10] held high if any banks are open
 - (b) Issuing an REF command

Table 23-12. SDRAM LOAD MODE REGISTER Command

EMIF_A[9:7]	EMIF_A[6:4]	EMIF_A[3]	EMIF_A[2:0]
0 (Write bursts are of the programmed burst length in EMIF_A[2:0])	These bits control the CAS latency of the SDRAM and are set according to CL field in the SDRAM configuration register (SDCR) as follows: <ul style="list-style-type: none">• If CL = 2, EMIF_A[6:4] = 2h (CAS latency = 2)• If CL = 3, EMIF_A[6:4] = 3h (CAS latency = 3)	0 (Sequential Burst Type. Interleaved Burst Type not supported)	These bits control the burst length of the SDRAM and are set according to the NM field in the SDRAM configuration register (SDCR) as follows: <ul style="list-style-type: none">• If NM = 0, EMIF_A[2:0] = 2h (Burst Length = 4)• If NM = 1, EMIF_A[2:0] = 3h (Burst Length = 8)

23.2.5.5 SDRAM Configuration Procedure

There are two different SDRAM configuration procedures. Although EMIF automatically performs the SDRAM initialization sequence described in [Section 23.2.5.4](#) when coming out of reset, it is recommended to follow one of the procedures listed below before performing any EMIF memory requests. Procedure A should be followed if it is determined that the SDRAM Power-up constraint was not violated during the SDRAM Auto-Initialization Sequence detailed in [Section 23.2.5.4](#) on coming out of Reset. The SDRAM Power-up constraint specifies that 200 µs (sometimes 100 µs) should exist between receiving stable Vdd and CLK and the issuing of a PRE command. Procedure B should be followed if the SDRAM Power-up constraint was violated. The 200 µs (100 µs) SDRAM Power-up constraint will be violated if the frequency of EMIF_CLK is greater than 50 MHz (100 MHz for 100 µs SDRAM power-up constraint) during SDRAM Auto-Initialization Sequence. Procedure B should be followed if there is any doubt that the Power-up constraint was not met.

Procedure A — Following is the procedure to be followed if the SDRAM Power-up constraint was NOT violated:

1. Place the SDRAM into Self-Refresh Mode by setting the SR bit of SDCR to 1. A byte-write to the upper byte of SDCR should be used to avoid restarting the SDRAM Auto-Initialization Sequence described in [Section 23.2.5.4](#). The SDRAM should be placed into Self-Refresh mode when changing the frequency of EMIF_CLK to avoid incurring the 200 µs Power-up constraint again.
2. Configure the desired EMIF_CLK clock frequency. The frequency of the memory clock must meet the timing requirements in the SDRAM manufacturer's documentation and the timing limitations shown in the electrical specifications of the device datasheet.
3. Remove the SDRAM from Self-Refresh Mode by clearing the SR bit of SDCR to 0. A byte-write to the upper byte of SDCR should be used to avoid restarting the SDRAM Auto-Initialization Sequence described in [Section 23.2.5.4](#).
4. Program SDTIMR and SDSRETR to satisfy the timing requirements for the attached SDRAM device. The timing parameters should be taken from the SDRAM datasheet.
5. Program the RR field of SDRCR to match that of the attached device's refresh interval. See [Section 23.2.5.6.1](#) details on determining the appropriate value.
6. Program SDCR to match the characteristics of the attached SDRAM device. This will cause the auto-initialization sequence in [Section 23.2.5.4](#) to be re-run. This second initialization generally takes much less time due to the increased frequency of EMIF_CLK.

Procedure B — Following is the procedure to be followed if the SDRAM Power-up constraint was violated:

1. Configure the desired EMIF_CLK clock frequency. The frequency of the memory clock must meet the timing requirements in the SDRAM manufacturer's documentation and the timing limitations shown in the electrical specifications of the device datasheet.
2. Program SDTIMR and SDSRETR to satisfy the timing requirements for the attached SDRAM device. The timing parameters should be taken from the SDRAM datasheet.
3. Program the RR field of SDRCR such that the following equation is satisfied: $(RR \times 8)/(f_{EMIF_CLK}) > 200 \mu s$ (sometimes 100 µs). For example, an EMIF_CLK frequency of 100 MHz would require setting RR to 2501 (9C5h) or higher to meet a 200 µs constraint.

4. Program SDCR to match the characteristics of the attached SDRAM device. This will cause the auto-initialization sequence in [Section 23.2.5.4](#) to be re-run with the new value of RR.
5. Perform a read from the SDRAM to assure that step 5 of this procedure will occur after the initialization process has completed. Alternatively, wait for 200 μ s instead of performing a read.
6. Finally, program the RR field to match that of the attached device's refresh interval. See [Section 23.2.5.6.1](#) details on determining the appropriate value.

After following the above procedure, the EMIF is ready to perform accesses to the attached SDRAM device. See for an example of configuring the SDRAM interface.

23.2.5.6 EMIF Refresh Controller

An SDRAM device requires that each of its rows be refreshed at a minimum required rate. The EMIF can meet this constraint by performing auto refresh cycles at or above this required rate. An auto refresh cycle consists of issuing a PRE command to all banks of the SDRAM device followed by issuing a REFR command. To inform the EMIF of the required rate for performing auto refresh cycles, the RR field of the SDRAM refresh control register (SDRCR) must be programmed. The EMIF will use this value along with two internal counters to automatically perform auto refresh cycles at the required rate. The auto refresh cycles cannot be disabled, even if the EMIF is not interfaced with an SDRAM. The remainder of this section details the EMIF's refresh scheme and provides an example for determining the appropriate value to place in the RR field of SDRCR.

The two counters used to perform auto-refresh cycles are a 13-bit refresh interval counter and a 4-bit refresh backlog counter. At reset and upon writing to the RR field, the refresh interval counter is loaded with the value from RR field and begins decrementing, by one, each EMIF clock cycle. When the refresh interval counter reaches zero, the following actions occur:

- The refresh interval counter is reloaded with the value from the RR field and restarts decrementing.
- The 4-bit refresh backlog counter increments unless it has already reached its maximum value.

The refresh backlog counter records the number of auto refresh cycles that the EMIF currently has outstanding. This counter is decremented by one each time an auto refresh cycle is performed and incremented by one each time the refresh interval counter expires. The refresh backlog counter saturates at the values of 0000b and 1111b. The EMIF uses the refresh backlog counter to determine the urgency with which an auto refresh cycle should be performed. The four levels of urgency are described in [Table 23-13](#). This refresh scheme allows the required refreshes to be performed with minimal impact on access requests.

Table 23-13. Refresh Urgency Levels

Urgency Level	Refresh Backlog Counter Range	Action Taken
Refresh May	1-3	An auto-refresh cycle is performed only if the EMIF has no requests pending and none of the SDRAM banks are open.
Refresh Release	4-7	An auto-refresh cycle is performed if the EMIF has no requests pending, regardless of whether any SDRAM banks are open.
Refresh Need	8-11	An auto-refresh cycle is performed at the completion of the current access unless there are read requests pending.
Refresh Must	12-15	Multiple auto-refresh cycles are performed at the completion of the current access until the Refresh Release urgency level is reached. At that point, the EMIF can begin servicing any new read or write requests.

23.2.5.6.1 Determining the Appropriate Value for the RR Field

The value that should be programmed into the RR field of SDRCR can be calculated by using the frequency of the EMIF_CLK signal (f_{EMIF_CLK}) and the required refresh rate of the SDRAM ($f_{Refresh}$). The following formula can be used:

$$RR = f_{EMIF_CLK} / f_{Refresh}$$

The SDRAM datasheet often communicates the required SDRAM Refresh Rate in terms of the number of REFRESH commands required in a given time interval. The required SDRAM Refresh Rate in the formula above can therefore be calculated by dividing the number of required cycles per time interval (n_{cycles}) by the time interval given in the datasheet ($t_{Refresh\ Period}$):

$$f_{Refresh} = n_{cycles} / t_{Refresh\ Period}$$

Combining these formulas, the value that should be programmed into the RR field can be computed as:

$$RR = f_{EMIF_CLK} \times t_{Refresh\ Period} / n_{cycles}$$

The following example illustrates calculating the value of RR. Given that:

- $f_{EMIF_CLK} = 100$ MHz (frequency of the EMIF clock)
- $t_{Refresh\ Period} = 64$ ms (required refresh interval of the SDRAM)
- $n_{cycles} = 8192$ (number of cycles in a refresh interval for the SDRAM)

RR can be calculated as:

$$RR = 100\text{ MHz} \times 64\text{ ms} / 8192$$

$$RR = 781.25$$

$$RR = 782\text{ cycles} = 30Eh\text{ cycles}$$

23.2.5.7 Self-Refresh Mode

The EMIF can be programmed to enter the self-refresh state by setting the SR bit of SDCR to 1. This will cause the EMIF to issue the SLFR command after completing any outstanding SDRAM access requests and clearing the refresh backlog counter by performing one or more auto refresh cycles. This places the attached SDRAM device into self-refresh mode in which it consumes a minimal amount of power while performing its own refresh cycles. The SR bit should be set and cleared using a byte-write to the upper byte of the SDRAM configuration register (SDCR) to avoid triggering the SDRAM initialization sequence.

While in the self-refresh state, the EMIF continues to service asynchronous bank requests and register accesses as normal, with one caveat. The EMIF will not park the data bus following a read to asynchronous memory while in the self-refresh state. Instead, the EMIF tri-states the data bus. Therefore, it is not recommended to perform asynchronous read operations while the EMIF is in the self-refresh state, in order to prevent floating inputs on the data bus. More information about data bus parking can be found in [Section 23.2.7](#).

The EMIF will exit from the self-refresh state if either of the following events occur:

- The SR bit of SDCR is cleared to 0.
- An SDRAM accesses is requested.

The EMIF exits from the self-refresh state by driving EMIF_CKE high and performing an auto refresh cycle.

The attached SDRAM device should also be placed into Self-Refresh Mode when changing the frequency of EMIF_CLK. If the frequency of EMIF_CLK changes while the SDRAM is not in Self-Refresh Mode, Procedure B in [Section 23.2.5.5](#) should be followed to reinitialize the device.

23.2.5.8 Power Down Mode

To support low-power modes, the EMIF can be requested to issue a POWER DOWN command to the SDRAM by setting the PD bit in the SDRAM configuration register (SDCR). When this bit is set, the EMIF will continue normal operation until all outstanding memory access requests have been serviced and the SDRAM refresh backlog (if there is one) has been cleared. At this point the EMIF will enter the power-down state. Upon entering this state, the EMIF will issue a POWER DOWN command (same as a NOP command but driving EMIF_CKE low on the same cycle). The EMIF then maintains EMIF_CKE low until it exits the power-down state.

Since the EMIF services the refresh backlog before it enters the power-down state, all internal banks of the SDRAM are closed (precharged) prior to issuing the POWER DOWN command. Therefore, the EMIF only supports Precharge Power Down. The EMIF does not support Active Power Down, where internal banks of the SDRAM are open (active) before the POWER DOWN command is issued.

During the power-down state, the EMIF services the SDRAM, asynchronous memory, and register accesses as normal, returning to the power-down state upon completion.

The PDWR bit in SDCR indicates whether the EMIF should perform refreshes in power-down state. If the PDWR bit is set, the EMIF exits the power-down state every time the Refresh Must level is set, performs AUTO REFRESH commands to the SDRAM, and returns back to the power-down state. This evenly distributes the refreshes to the SDRAM in power-down state. If the PDWR bit is not set, the EMIF does not perform any refreshes to the SDRAM. Therefore, the data integrity of the SDRAM is not assured upon power down exit if the PDWR bit is not set.

If the PD bit is cleared while in the power-down state, the EMIF will come out of the power-down state.
The EMIF:

- Drives EMIF_CKE high.
- Enters its idle state.

23.2.5.9 SDRAM Read Operation

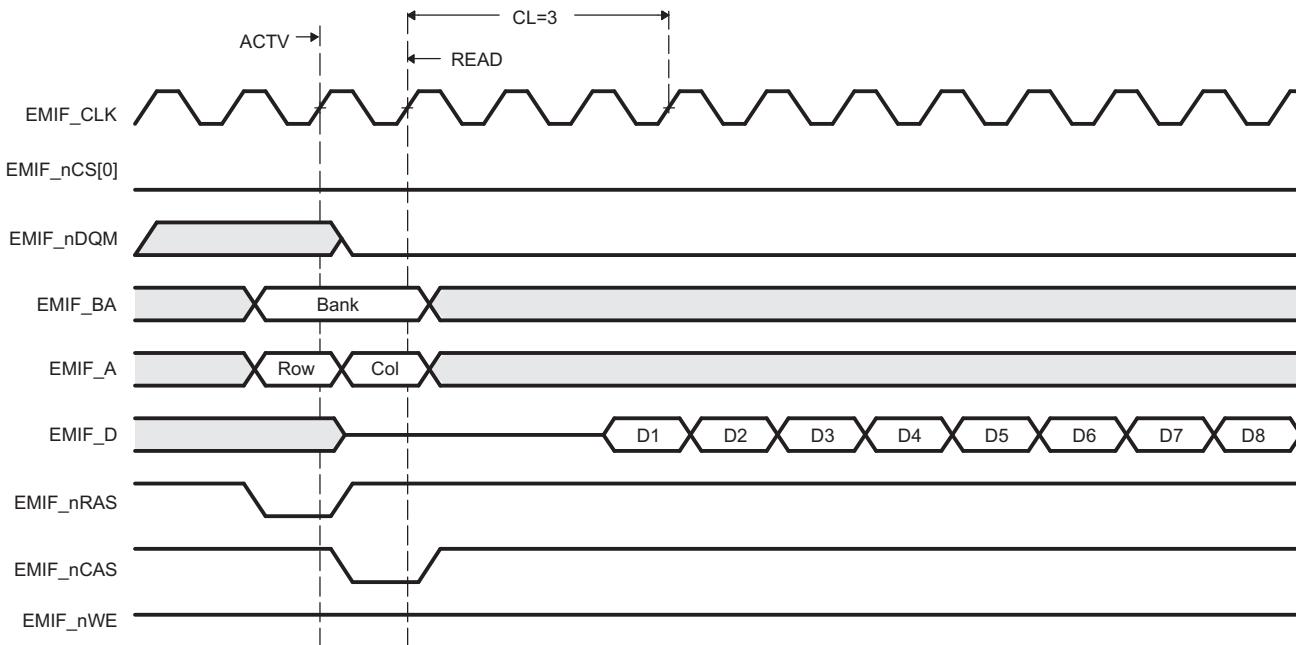
When the EMIF receives a read request to SDRAM from one of the requesters listed in [Section 23.2.2](#), it performs one or more read access cycles. A read access cycle begins with the issuing of the ACTV command to select the desired bank and row of the SDRAM device. After the row has been opened, the EMIF proceeds to issue a READ command while specifying the desired bank and column address. EMIF_A[10] is held low during the READ command to avoid auto-precharging. The READ command signals the SDRAM device to start bursting data from the specified address while the EMIF issues NOP commands. Following a READ command, the CL field of the SDRAM configuration register (SDCR) defines how many delay cycles will be present before the read data appears on the data bus. This is referred to as the CAS latency.

[Figure 23-6](#) shows the signal waveforms for a basic SDRAM read operation in which a burst of data is read from a single page. When the EMIF SDRAM interface is configured to 16 bit by setting the NM bit of the SDRAM configuration register (SDCR) to 1, a burst size of eight is used. [Figure 23-6](#) shows a burst size of eight.

The EMIF will truncate a series of bursting data if the remaining addresses of the burst are not required to complete the request. The EMIF can truncate the burst in three ways:

- By issuing another READ to the same page in the same bank.
- By issuing a PRE command in order to prepare for accessing a different page of the same bank.
- By issuing a BT command in order to prepare for accessing a page in a different bank.

Figure 23-6. Timing Waveform for Basic SDRAM Read Operation



Several other pins are also active during a read access. The EMIF_nDQM[1:0] pins are driven low during the READ commands and are kept low during the NOP commands that correspond to the burst request. The state of the other EMIF pins during each command can be found in [Table 23-6](#).

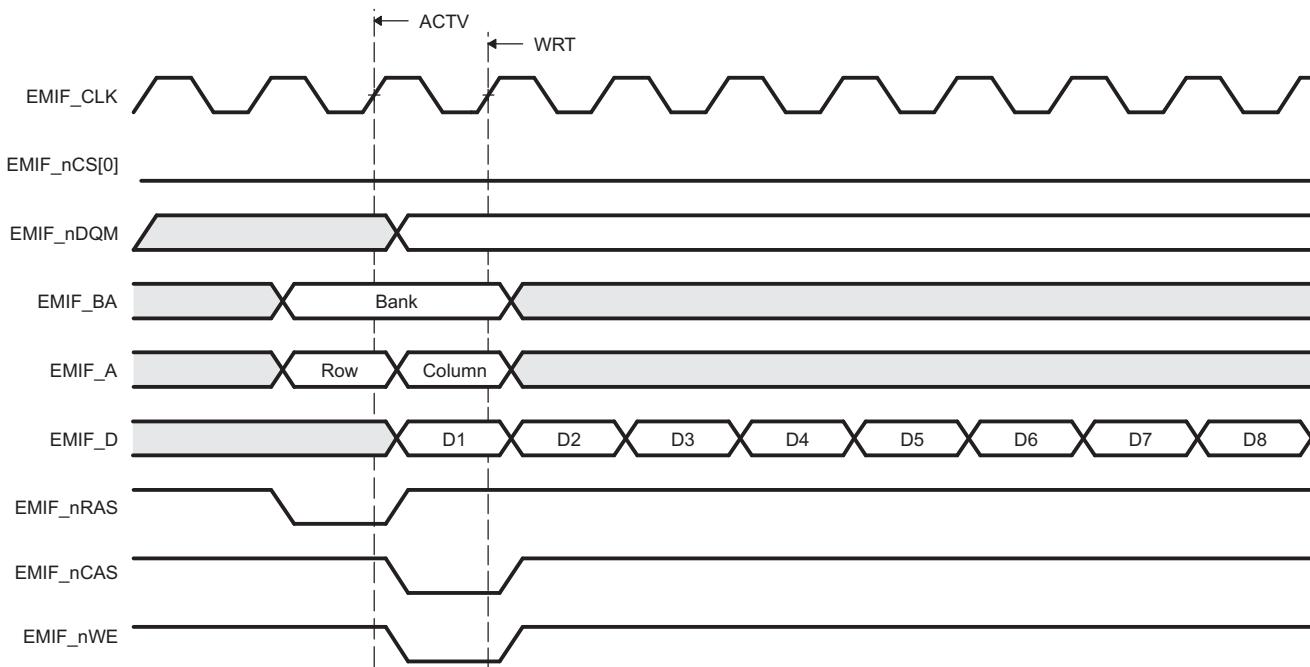
The EMIF schedules its commands based on the timing information that is provided to it in the SDRAM timing register (SDTIMR). The values for the timing parameters in this register should be chosen to satisfy the timing requirements listed in the SDRAM datasheet. The EMIF uses this timing information to avoid violating any timing constraints related to issuing commands. This is commonly accomplished by inserting NOP commands between various commands during an access. Refer to the register description of SDTIMR in for more details on the various timing parameters.

23.2.5.10 SDRAM Write Operations

When the EMIF receives a write request to SDRAM from one of the requesters listed in [Section 23.2.2](#), it performs one or more write-access cycles. A write-access cycle begins with the issuing of the ACTV command to select the desired bank and row of the SDRAM device. After the row has been opened, the EMIF proceeds to issue a WRT command while specifying the desired bank and column address. EMIF_A[10] is held low during the WRT command to avoid auto-precharging. The WRT command signals the SDRAM device to start writing a burst of data to the specified address while the EMIF issues NOP commands. The associated write data will be placed on the data bus in the cycle concurrent with the WRT command and with subsequent burst continuation NOP commands.

[Figure 23-7](#) shows the signal waveforms for a basic SDRAM write operation in which a burst of data is read from a single page. When the EMIF SDRAM interface is configured to 16-bit by setting the NM bit of the SDRAM configuration register (SDCR) to 1, a burst size of eight is used. [Figure 23-7](#) shows a burst size of eight.

Figure 23-7. Timing Waveform for Basic SDRAM Write Operation



The EMIF will truncate a series of bursting data if the remaining addresses of the burst are not part of the write request. The EMIF can truncate the burst in three ways:

- By issuing another WRT to the same page
- By issuing a PRE command in order to prepare for accessing a different page of the same bank
- By issuing a BT command in order to prepare for accessing a page in a different bank

Several other pins are also active during a write access. The EMIF_nDQM[1:0] pins are driven to select which bytes of the data word will be written to the SDRAM device. They are also used to mask out entire undesired data words during a burst access. The state of the other EMIF pins during each command can be found in [Table 23-6](#).

The EMIF schedules its commands based on the timing information that is provided to it in the SDRAM timing register (SDTIMR). The values for the timing parameters in this register should be chosen to satisfy the timing requirements listed in the SDRAM datasheet. The EMIF uses this timing information to avoid violating any timing constraints related to issuing commands. This is commonly accomplished by inserting NOP commands during various cycles of an access. Refer to the register description of SDTIMR for more details on the various timing parameters.

23.2.5.11 Mapping from Logical Address to EMIF Pins

When the EMIF receives an SDRAM access request, it must convert the address of the access into the appropriate signals to send to the SDRAM device. The details of this address mapping are shown in [Table 23-14](#) for 16-bit operation. Using the settings of the IBANK and PAGESIZE fields of the SDRAM configuration register (SDCR), the EMIF determines which bits of the logical address will be mapped to the SDRAM row, column, and bank addresses.

As the logical address is incremented by one halfword (16-bit operation), the column address is likewise incremented by one until a page boundary is reached. When the logical address increments across a page boundary, the EMIF moves into the same page in the next bank of the attached device by incrementing the bank address EMIF_BA and resetting the column address. The page in the previous bank is left open until it is necessary to close it. This method of traversal through the SDRAM banks helps maximize the number of open banks inside of the SDRAM and results in an efficient use of the device. There is no limitation on the number of banks that can be open at one time, but only one page within a bank can be open at a time.

The EMIF uses the EMIF_nDQM[1:0] pins during a WRT command to mask out selected bytes or entire words. The EMIF_nDQM[1:0] pins are always low during a READ command.

Table 23-14. Mapping from Logical Address to EMIF Pins for 16-bit SDRAM

IBANK	PAGESIZE	Logical Address													
		31:27	26	25	24	23	22	21:14	13	12	11	10	9	8:1	0
0	0	-												Col Address	EMIF_nDQM[0]
1	0	-												Col Address	EMIF_nDQM[0]
2	0	-												Col Address	EMIF_nDQM[0]
0	1	-												Column Address	EMIF_nDQM[0]
1	1	-												Column Address	EMIF_nDQM[0]
2	1	-												Column Address	EMIF_nDQM[0]
0	2	-												Column Address	EMIF_nDQM[0]
1	2	-												Column Address	EMIF_nDQM[0]
2	2	-												Column Address	EMIF_nDQM[0]
0	3	-												Column Address	EMIF_nDQM[0]
1	3	-												Column Address	EMIF_nDQM[0]
2	3	-												Column Address	EMIF_nDQM[0]

NOTE: The upper bit of the Row Address is used only when addressing 256-Mbit and 512-Mbit SDRAM memories.

23.2.6 Asynchronous Controller and Interface

The EMIF easily interfaces to a variety of asynchronous devices including NOR Flash and SRAM. It can be operated in two major modes (see [Table 23-15](#)):

- Normal Mode
- Select Strobe Mode

Table 23-15. Normal Mode vs. Select Strobe Mode

Mode	Function of EMIF_nDQM pins	Operation of EMIF_nCS[4:2]
Normal Mode	Byte enables	Active during the entire asynchronous access cycle
Select Strobe Mode	Byte enables	Active only during the strobe period of an access cycle

The first mode of operation is Normal Mode, in which the EMIF_nDQM pins of the EMIF function as byte enables. In this mode, the EMIF_nCS[4:2] pins behaves as typical chip select signals, remaining active for the duration of the asynchronous access. See [Section 23.2.6.1](#) for an example interface with multiple 8-bit devices.

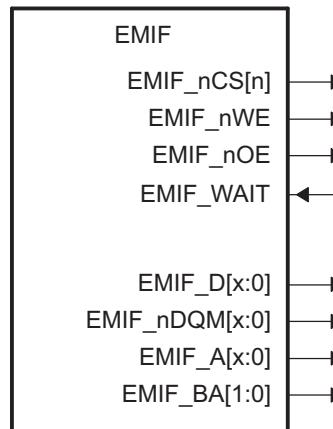
The second mode of operation is Select Strobe Mode, in which the EMIF_nCS[4:2] pins act as a strobe, active only during the strobe period of an access. In this mode, the EMIF_nDQM pins of the EMIF function as standard byte enables for reads and writes. A summary of the differences between the two modes of operation are shown in [Table 23-15](#). Refer to [Section 23.2.6.4](#) for the details of asynchronous operations in Normal Mode, and to [Section 23.2.6.5](#) for the details of asynchronous operations in Select Strobe Mode. The EMIF hardware defaults to Normal Mode, but can be manually switched to Select Strobe Mode by setting the SS bit in the asynchronous m ($m = 1, 2, 3$, or 4) configuration register (CEnCFG) ($n = 2, 3$, or 4). Throughout the chapter, m can hold the values 1, 2, 3 or 4; and n can hold the values 2, 3, or 4.

The EMIF also provides configurable cycle timing parameters and an Extended Wait Mode that allows the connected device to extend the strobe period of an access cycle. The following sections describe the features related to interfacing with external asynchronous devices.

23.2.6.1 Interfacing to Asynchronous Memory

[Figure 23-8](#) shows the EMIF's external pins used in interfacing with an asynchronous device. In EMIF_nCS[n], $n = 2, 3$, or 4 .

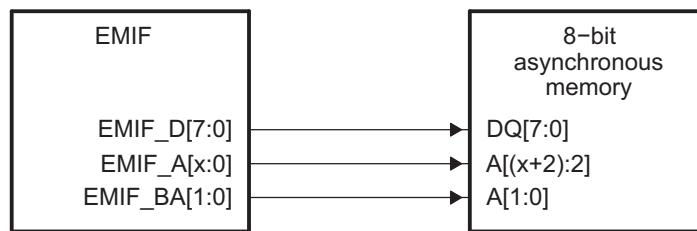
Figure 23-8. EMIF Asynchronous Interface



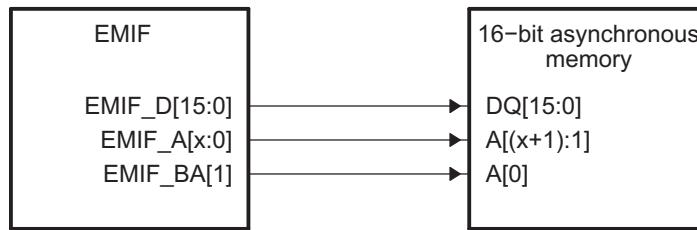
Of special note is the connection between the EMIF and the external device's address bus. The EMIF address pin EMIF_A[0] always provides the least significant bit of a 32-bit word address. Therefore, when interfacing to a 16-bit or 8-bit asynchronous device, the EMIF_BA[1] and EMIF_BA[0] pins provide the least-significant bits of the halfword or byte address, respectively. Additionally, when the EMIF interfaces to a 16-bit asynchronous device, the EMIF_BA[0] pin can serve as the upper address line EMIF_A[22]. Figure 23-9 and Figure 23-10 show the mapping between the EMIF and the connected device's data and address pins for various programmed data bus widths. The data bus width may be configured in the asynchronous n configuration register (CEnCFG).

Figure 23-10 shows a common interface between the EMIF and external asynchronous memory. Figure 23-10 shows an interface between the EMIF and an external memory with byte enables. The EMIF should be operated in either Normal Mode or Select Strobe Mode when using this interface, so that the EMIF_nDQM signals operate as byte enables.

Figure 23-9. EMIF to 8-bit/16-bit Memory Interface

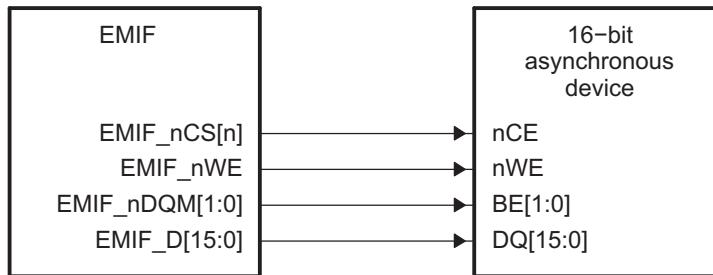


a) EMIF to 8-bit memory interface



b) EMIF to 16-bit memory interface

Figure 23-10. Common Asynchronous Interface



23.2.6.2 Accessing Larger Asynchronous Memories

If a device such as a large asynchronous flash needs to be attached to the EMIF, then GPIO pins may be used to control the flash device's upper address lines.

23.2.6.3 Configuring the EMIF for Asynchronous Accesses

The operation of the EMIF's asynchronous interface can be configured by programming the appropriate register fields. The reset value and bit position for each register field can be found in . The following tables list the register fields that can be programmed and describe the purpose of each field. These registers can be programmed prior to accessing the external memory, and the transfer following a write to these registers will use the new configuration.

Table 23-16. Description of the Asynchronous *m* Configuration Register (CE*n*CFG)

Parameter	Description
SS	Select Strobe mode. This bit selects the EMIF's mode of operation in the following way: <ul style="list-style-type: none"> • SS = 0 selects Normal Mode <ul style="list-style-type: none"> – EMIF_nDQM pins function as byte enables – EMIF_nCS[4:2] active for duration of access • SS = 1 selects Select Strobe Mode <ul style="list-style-type: none"> – EMIF_nDQM pins function as byte enables – EMIF_nCS[4:2] acts as a strobe.
EW	Extended Wait Mode enable. <ul style="list-style-type: none"> • EW = 0 disables Extended Wait Mode • EW = 1 enables Extended Wait Mode When set to 1, the EMIF enables its Extended Wait Mode in which the strobe width of an access cycle can be extended in response to the assertion of the EMIF_nWAIT pin. The WP <i>n</i> bit in the asynchronous wait cycle configuration register (AWCC) controls the polarity of EMIF_nWAIT pin. See Section 23.2.6.6 for more details on this mode of operation.
W_SETUP/R_SETUP	Read/Write setup widths. These fields define the number of EMIF clock cycles of setup time for the address pins (EMIF_A and EMIF_BA), byte enables (EMIF_nDQM), and asynchronous chip enable (EMIF_nCS[4:2]) before the read strobe pin (EMIF_nOE) or write strobe pin (EMIF_nWE) falls, minus one cycle. For writes, the W_SETUP field also defines the setup time for the data pins (EMIF_D). Refer to the datasheet of the external asynchronous device to determine the appropriate setting for this field.
W_STROBE/R_STROBE	Read/Write strobe widths. These fields define the number of EMIF clock cycles between the falling and rising of the read strobe pin (EMIF_nOE) or write strobe pin (EMIF_nWE), minus one cycle. If Extended Wait Mode is enabled by setting the EW field in the asynchronous <i>n</i> configuration register (CE <i>n</i> CFG), these fields must be set to a value greater than zero. Refer to the datasheet of the external asynchronous device to determine the appropriate setting for this field.
W_HOLD/R_HOLD	Read/Write hold widths. These fields define the number of EMIF clock cycles of hold time for the address pins (EMIF_A and EMIF_BA), byte enables (EMIF_nDQM), and asynchronous chip enable (EMIF_nCS[4:2]) after the read strobe pin (EMIF_nOE) or write strobe pin (EMIF_nWE) rises, minus one cycle. For writes, the W_HOLD field also defines the hold time for the data pins (EMIF_D). Refer to the datasheet of the external asynchronous device to determine the appropriate setting for this field.
TA	Minimum turnaround time. This field defines the minimum number of EMIF clock cycles between asynchronous reads and writes, minus one cycle. The purpose of this feature is to avoid contention on the bus. The value written to this field also determines the number of cycles that will be inserted between asynchronous accesses and SDRAM accesses. Refer to the datasheet of the external asynchronous device to determine the appropriate setting for this field.

Table 23-16. Description of the Asynchronous m Configuration Register (CE n CFG) (continued)

Parameter	Description
ASIZE	<p>Asynchronous Device Bus Width. This field determines the data bus width of the asynchronous interface in the following way:</p> <ul style="list-style-type: none"> • ASIZE = 0 selects an 8-bit bus • ASIZE = 1 selects a 16-bit bus • ASIZE = 2 selects a 32-bit bus <p>The configuration of ASIZE determines the function of the EMIF_A and EMIF_BA pins as described in Section 23.2.6.1. This field also determines the number of external accesses required to fulfill a request generated by one of the sources mentioned in Section 23.2.2. For example, a request for a 32-bit word would require four external access when ASIZE = 0. Refer to the datasheet of the external asynchronous device to determine the appropriate setting for this field.</p>

Table 23-17. Description of the Asynchronous Wait Cycle Configuration Register (AWCC)

Parameter	Description
WP n	<p>EM_WAIT Polarity.</p> <ul style="list-style-type: none"> • WPn = 0 selects active-low polarity • WPn = 1 selects active-high polarity <p>When set to 1, the EMIF will wait if the EMIF_nWAIT pin is high. When cleared to 0, the EMIF will wait if the EMIF_nWAIT pin is low. The EMIF must have the Extended Wait Mode enabled for the EMIF_nWAIT pin to affect the width of the strobe period.</p>
MAX_EXT_WAIT	<p>Maximum Extended Wait Cycles.</p> <p>This field configures the number of EMIF clock cycles the EMIF will wait for the EMIF_nWAIT pin to be deactivated during the strobe period of an access cycle. The maximum number of EMIF clock cycles it will wait is determined by the following formula:</p> $\text{Maximum Extended Wait Cycles} = (\text{MAX_EXT_WAIT} + 1) \times 16$ <p>If the EMIF_nWAIT pin is not deactivated within the time specified by this field, the EMIF resumes the access cycle, registering whatever data is on the bus and proceeding to the hold period of the access cycle. This situation is referred to as an Asynchronous Timeout. An Asynchronous Timeout generates an interrupt, if it has been enabled in the EMIF interrupt mask set register (INTMSKSET). Refer to Section 23.2.9.1 for more information about the EMIF interrupts.</p>

Table 23-18. Description of the EMIF Interrupt Mask Set Register (INTMSKSET)

Parameter	Description
WR_MASK_SET	Wait Rise Mask Set. Writing a 1 enables an interrupt to be generated when a rising edge on EMIF_nWAIT occurs while in NAND Flash Mode
AT_MASK_SET	Asynchronous Timeout Mask Set. Writing a 1 to this bit enables an interrupt to be generated when an Asynchronous Timeout occurs.

Table 23-19. Description of the EMIF Interrupt Mast Clear Register (INTMSKCLR)

Parameter	Description
WR_MASK_CLR	Wait Rise Mask Clear. Writing a 1 to this bit disables the interrupt, clearing the WR_MASK_SET bit in the EMIF interrupt mask set register (INTMSKSET).
AT_MASK_CLR	Asynchronous Timeout Mask Clear. Writing a 1 to this bit prevents an interrupt from being generated when an Asynchronous Timeout occurs.

23.2.6.4 Read and Write Operations in Normal Mode

Normal Mode is the asynchronous interface's default mode of operation. It is selected when the SS bit in the asynchronous *n* configuration register (CE*n*CFG) is cleared to 0. In this mode, the EMIF_nDQM pins operate as byte enables. [Section 23.2.6.4.1](#) and [Section 23.2.6.4.2](#) explain the details of read and write operations while in Normal Mode.

23.2.6.4.1 Asynchronous Read Operations (Normal Mode)

NOTE: During an entire asynchronous read operation, the EMIF_nWE pin is driven high.

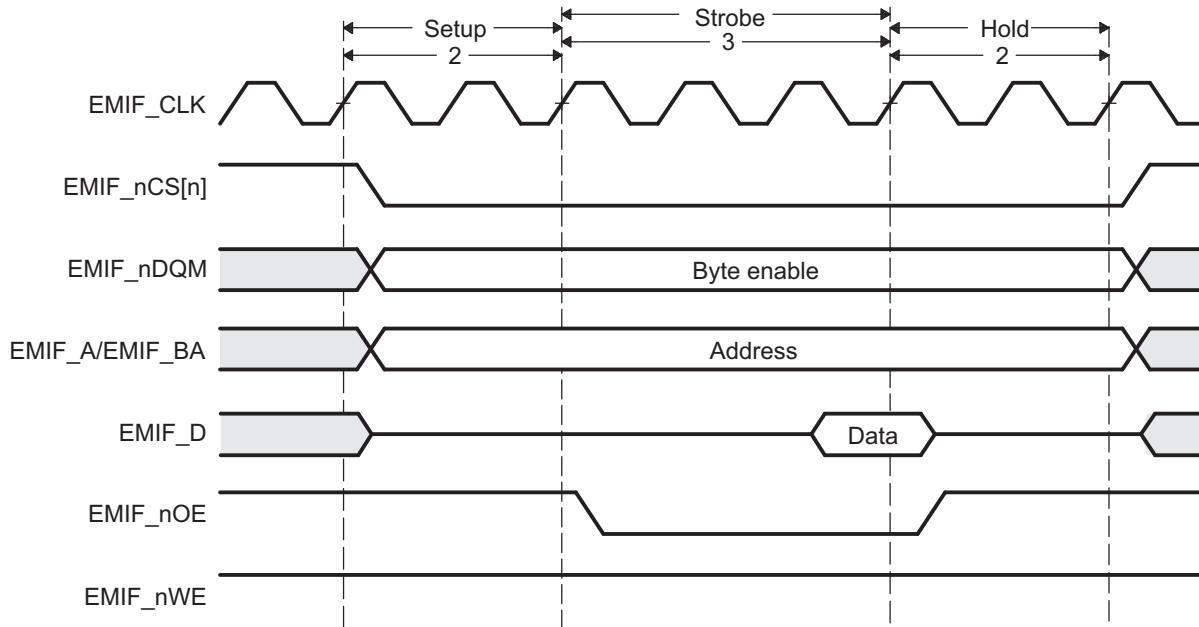
An asynchronous read is performed when any of the requesters mentioned in [Section 23.2.2](#) request a read from the attached asynchronous memory. After the request is received, a read operation is initiated once it becomes the EMIF's highest priority task, according to the priority scheme detailed in [Section 23.2.13](#). In the event that the read request cannot be serviced by a single access cycle to the external device, multiple access cycles will be performed by the EMIF until the entire request is fulfilled. The details of an asynchronous read operation in Normal Mode are described in [Table 23-20](#). Also, [Figure 23-11](#) shows an example timing diagram of a basic read operation.

Table 23-20. Asynchronous Read Operation in Normal Mode

Time Interval	Pin Activity in Normal Mode
Turn-around period	Once the read operation becomes the highest priority task for the EMIF, the EMIF waits for the programmed number of turn-around cycles before proceeding to the setup period of the operation. The number of wait cycles is taken directly from the TA field of the asynchronous <i>n</i> configuration register (CE <i>n</i> CFG). There are two exceptions to this rule: <ul style="list-style-type: none"> • If the current read operation was directly proceeded by another read operation, no turnaround cycles are inserted. • If the current read operation was directly proceeded by a write operation and the TA field has been cleared to 0, one turn-around cycle will be inserted. After the EMIF has waited for the turnaround cycles to complete, it again checks to make sure that the read operation is still its highest priority task. If so, the EMIF proceeds to the setup period of the operation. If it is no longer the highest priority task, the EMIF terminates the operation.

Table 23-20. Asynchronous Read Operation in Normal Mode (continued)

Time Interval	Pin Activity in Normal Mode
Start of the setup period	The following actions occur at the start of the setup period: <ul style="list-style-type: none"> The setup, strobe, and hold values are set according to the R_SETUP, R_STROBE, and R_HOLD values in CEnCFG. The address pins EMIF_A and EMIF_BA become valid and carry the values described in Section 23.2.6.1. EMIF_nCS[4:2] falls to enable the external device (if not already low from a previous operation)
Strobe period	The following actions occur during the strobe period of a read operation: <ol style="list-style-type: none"> 1. EMIF_nOE falls at the start of the strobe period 2. On the rising edge of the clock which is concurrent with the end of the strobe period: <ul style="list-style-type: none"> • EMIF_nOE rises • The data on the EMIF_D bus is sampled by the EMIF. <p>In Figure 23-11, EMIF_nWAIT is inactive. If EMIF_nWAIT is instead activated, the strobe period can be extended by the external device to give it more time to provide the data. Section 23.2.6.6 contains more details on using the EMIF_nWAIT pin.</p>
End of the hold period	At the end of the hold period: <ul style="list-style-type: none"> The address pins EMIF_A and EMIF_BA become invalid EMIF_nCS[4:2] rises (if no more operations are required to complete the current request) <p>EMIF may be required to issue additional read operations to a device with a small data bus width in order to complete an entire word access. In this case, the EMIF immediately re-enters the setup period to begin another operation without incurring the turn-round cycle delay. The setup, strobe, and hold values are not updated in this case. If the entire word access has been completed, the EMIF returns to its previous state unless another asynchronous request has been submitted and is currently the highest priority task. If this is the case, the EMIF instead enters directly into the turnaround period for the pending read or write operation.</p>

Figure 23-11. Timing Waveform of an Asynchronous Read Cycle in Normal Mode


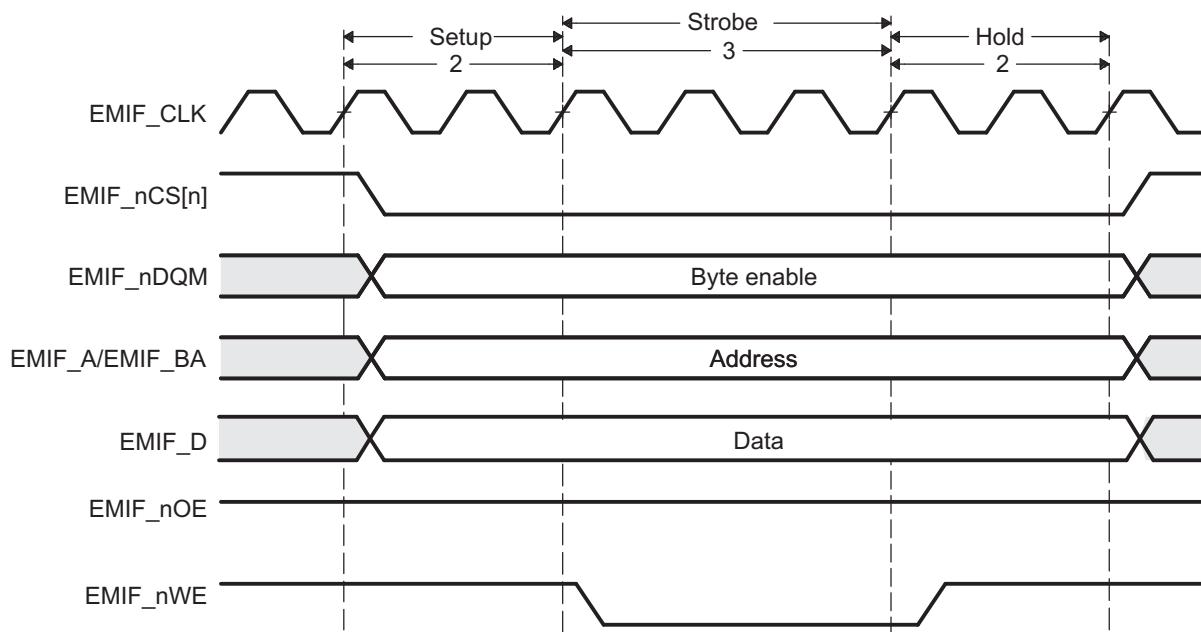
23.2.6.4.2 Asynchronous Write Operations (Normal Mode)

NOTE: During an entire asynchronous write operation, the EMIF_nOE pin is driven high.

An asynchronous write is performed when any of the requesters mentioned in [Section 23.2.2](#) request a write to memory in the asynchronous bank of the EMIF. After the request is received, a write operation is initiated once it becomes the EMIF's highest priority task, according to the priority scheme detailed in [Section 23.2.13](#). In the event that the write request cannot be serviced by a single access cycle to the external device, multiple access cycles will be performed by the EMIF until the entire request is fulfilled. The details of an asynchronous write operation in Normal Mode are described in [Table 23-21](#). Also, [Figure 23-12](#) shows an example timing diagram of a basic write operation.

Table 23-21. Asynchronous Write Operation in Normal Mode

Time Interval	Pin Activity in Normal Mode
Turnaround period	<p>Once the write operation becomes the highest priority task for the EMIF, the EMIF waits for the programmed number of turn-around cycles before proceeding to the setup period of the operation. The number of wait cycles is taken directly from the TA field of the asynchronous <i>n</i> configuration register (CE<i>n</i>CFG). There are two exceptions to this rule:</p> <ul style="list-style-type: none"> If the current write operation was directly proceeded by another write operation, no turn-around cycles are inserted. If the current write operation was directly proceeded by a read operation and the TA field has been cleared to 0, one turnaround cycle will be inserted. <p>After the EMIF has waited for the turn-around cycles to complete, it again checks to make sure that the write operation is still its highest priority task. If so, the EMIF proceeds to the setup period of the operation. If it is no longer the highest priority task, the EMIF terminates the operation.</p>
Start of the setup period	<p>The following actions occur at the start of the setup period:</p> <ul style="list-style-type: none"> The setup, strobe, and hold values are set according to the W_SETUP, W_STROBE, and W_HOLD values in CE<i>n</i>CFG. The address pins EMIF_A and EMIF_BA and the data pins EMIF_D become valid. The EMIF_A and EMIF_BA pins carry the values described in Section 23.2.6.1. EMIF_nCS[4:2] falls to enable the external device (if not already low from a previous operation).
Strobe period	<p>The following actions occur at the start of the strobe period of a write operation:</p> <ol style="list-style-type: none"> EMIF_nWE falls The EMIF_nDQM pins become valid as byte enables. <p>The following actions occur on the rising edge of the clock which is concurrent with the end of the strobe period:</p> <ol style="list-style-type: none"> EMIF_nWE rises The EMIF_nDQM pins deactivate <p>In Figure 23-12, EMIF_nWAIT is inactive. If EMIF_nWAIT is instead activated, the strobe period can be extended by the external device to give it more time to accept the data. Section 23.2.6.6 contains more details on using the EMIF_nWAIT pin.</p>
End of the hold period	<p>At the end of the hold period:</p> <ul style="list-style-type: none"> The address pins EMIF_A and EMIF_BA become invalid The data pins become invalid EMIF_nCS[n] (n = 2, 3, or 4) rises (if no more operations are required to complete the current request) <p>The EMIF may be required to issue additional write operations to a device with a small data bus width in order to complete an entire word access. In this case, the EMIF immediately re-enters the setup period to begin another operation without incurring the turnaround cycle delay. The setup, strobe, and hold values are not updated in this case. If the entire word access has been completed, the EMIF returns to its previous state unless another asynchronous request has been submitted and is currently the highest priority task. If this is the case, the EMIF instead enters directly into the turnaround period for the pending read or write operation.</p>

Figure 23-12. Timing Waveform of an Asynchronous Write Cycle in Normal Mode

23.2.6.5 Read and Write Operation in Select Strobe Mode

Select Strobe Mode is the EMIF's second mode of operation. It is selected when the SS bit of the asynchronous n configuration register (CE n CFG) is set to 1. In this mode, the EMIF_nDQM pins operate as byte enables and the EMIF_nCS[n] ($n = 2, 3$, or 4) pin is only active during the strobe period of an access cycle. [Section 23.2.6.4.1](#) and [Section 23.2.6.4.2](#) explain the details of read and write operations while in Select Strobe Mode.

23.2.6.5.1 Asynchronous Read Operations (Select Strobe Mode)

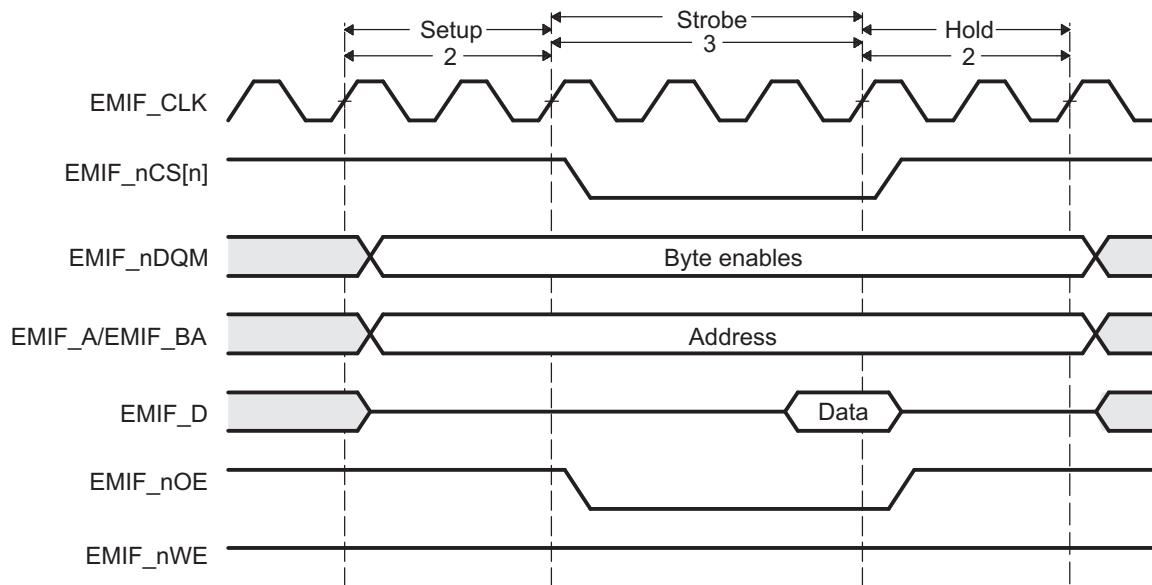
NOTE: During the entirety of an asynchronous read operation, the EMIF_nWE pin is driven high.

An asynchronous read is performed when any of the requesters mentioned in [Section 23.2.2](#) request a read from the attached asynchronous memory. After the request is received, a read operation is initiated once it becomes the EMIF's highest priority task, according to the priority scheme detailed in [Section 23.2.13](#). In the event that the read request cannot be serviced by a single access cycle to the external device, multiple access cycles will be performed by the EMIF until the entire request is fulfilled. The details of an asynchronous read operation in Select Strobe Mode are described in [Table 23-22](#). Also, [Figure 23-13](#) shows an example timing diagram of a basic read operation.

Table 23-22. Asynchronous Read Operation in Select Strobe Mode

Time Interval	Pin Activity in Select Strobe Mode
Turnaround period	Once the read operation becomes the highest priority task for the EMIF, the EMIF waits for the programmed number of turn-around cycles before proceeding to the setup period of the operation. The number of wait cycles is taken directly from the TA field of the asynchronous n configuration register (CE n CFG). There are two exceptions to this rule: <ul style="list-style-type: none"> If the current read operation was directly proceeded by another read operation, no turn-around cycles are inserted. If the current read operation was directly proceeded by a write operation and the TA field has been cleared to 0, one turn-around cycle will be inserted. After the EMIF has waited for the turn-around cycles to complete, it again checks to make sure that the read operation is still its highest priority task. If so, the EMIF proceeds to the setup period of the operation. If it is no longer the highest priority task, the EMIF terminates the operation.
Start of the setup period	The following actions occur at the start of the setup period: <ul style="list-style-type: none"> The setup, strobe, and hold values are set according to the R_SETUP, R_STROBE, and R_HOLD values in CEnCFG. The address pins EMIF_A and EMIF_BA become valid and carry the values described in Section 23.2.6.1. The EMIF_nDQM pins become valid as byte enables.
Strobe period	The following actions occur during the strobe period of a read operation: <ol style="list-style-type: none"> EMIF_nCS[n] ($n = 2, 3$, or 4) and EMIF_nOE fall at the start of the strobe period On the rising edge of the clock which is concurrent with the end of the strobe period: <ul style="list-style-type: none"> EMIF_nCS[n] ($n = 2, 3$, or 4) and EMIF_nOE rise The data on the EMIF_D bus is sampled by the EMIF. In Figure 23-13 , EMIF_nWAIT is inactive. If EMIF_nWAIT is instead activated, the strobe period can be extended by the external device to give it more time to provide the data. Section 23.2.6.6 contains more details on using the EMIF_nWAIT pin.
End of the hold period	At the end of the hold period: <ul style="list-style-type: none"> The address pins EMIF_A and EMIF_BA become invalid The EMIF_nDQM pins become invalid The EMIF may be required to issue additional read operations to a device with a small data bus width in order to complete an entire word access. In this case, the EMIF immediately re-enters the setup period to begin another operation without incurring the turnaround cycle delay. The setup, strobe, and hold values are not updated in this case. If the entire word access has been completed, the EMIF returns to its previous state unless another asynchronous request has been submitted and is currently the highest priority task. If this is the case, the EMIF instead enters directly into the turnaround period for the pending read or write operation.

Figure 23-13. Timing Waveform of an Asynchronous Read Cycle in Select Strobe Mode



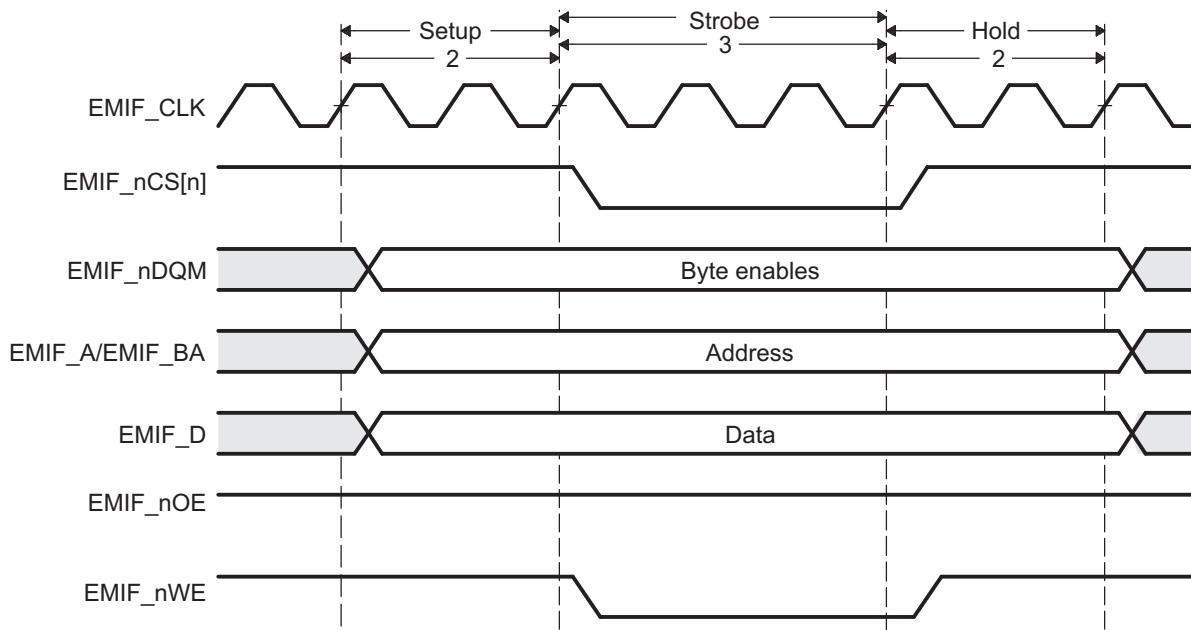
23.2.6.5.2 Asynchronous Write Operations (Select Strobe Mode)

NOTE: During the entirety of an asynchronous write operation, the EMIF_nOE pin is driven high.

An asynchronous write is performed when any of the requesters mentioned in [Section 23.2.2](#) request a write to memory in the asynchronous bank of the EMIF. After the request is received, a write operation is initiated once it becomes the EMIF's highest priority task, according to the priority scheme detailed in [Section 23.2.13](#). In the event that the write request cannot be serviced by a single access cycle to the external device, multiple access cycles will be performed by the EMIF until the entire request is fulfilled. The details of an asynchronous write operation in Select Strobe Mode are described in [Table 23-23](#). Also, [Figure 23-14](#) shows an example timing diagram of a basic write operation.

Table 23-23. Asynchronous Write Operation in Select Strobe Mode

Time Interval	Pin Activity in Select Strobe Mode
Turnaround period	<p>Once the write operation becomes the highest priority task for the EMIF, the EMIF waits for the programmed number of turnaround cycles before proceeding to the setup period of the operation. The number of wait cycles is taken directly from the TA field of the asynchronous n configuration register (CEnCFG). There are two exceptions to this rule:</p> <ul style="list-style-type: none"> If the current write operation was directly proceeded by another write operation, no turn-around cycles are inserted. If the current write operation was directly proceeded by a read operation and the TA field has been cleared to 0, one turnaround cycle will be inserted. <p>After the EMIF has waited for the turnaround cycles to complete, it again checks to make sure that the write operation is still its highest priority task. If so, the EMIF proceeds to the setup period of the operation. If it is no longer the highest priority task, the EMIF terminates the operation.</p>
Start of the setup period	<p>The following actions occur at the start of the setup period:</p> <ul style="list-style-type: none"> The setup, strobe, and hold values are set according to the W_SETUP, W_STROBE, and W_HOLD values in CEnCFG. The address pins EMIF_A and EMIF_BA and the data pins EMIF_D become valid. The EMIF_A and EMIF_BA pins carry the values described in Section 23.2.6.1. The EMIF_nDQM pins become active as byte enables.
Strobe period	<p>The following actions occur at the start of the strobe period of a write operation:</p> <ul style="list-style-type: none"> EMIF_nCS[n] ($n = 2, 3$, or 4) and EMIF_nWE fall <p>The following actions occur on the rising edge of the clock which is concurrent with the end of the strobe period:</p> <ul style="list-style-type: none"> EMIF_nCS[n] ($n = 2, 3$, or 4) and EMIF_nWE rise <p>In Figure 23-14, EMIF_nWAIT is inactive. If EMIF_nWAIT is instead activated, the strobe period can be extended by the external device to give it more time to accept the data. Section 23.2.6.6 contains more details on using the EMIF_nWAIT pin.</p>
End of the hold period	<p>At the end of the hold period:</p> <ul style="list-style-type: none"> The address pins EMIF_A and EMIF_BA become invalid The data pins become invalid The EMIF_nDQM pins become invalid <p>The EMIF may be required to issue additional write operations to a device with a small data bus width in order to complete an entire word access. In this case, the EMIF immediately re-enters the setup period to begin another operation without incurring the turnaround cycle delay. The setup, strobe, and hold values are not updated in this case. If the entire word access has been completed, the EMIF returns to its previous state unless another asynchronous request has been submitted and is currently the highest priority task. If this is the case, the EMIF instead enters directly into the turn-around period for the pending read or write operation.</p>

Figure 23-14. Timing Waveform of an Asynchronous Write Cycle in Select Strobe Mode

23.2.6.6 Extended Wait Mode and the EMIF_nWAIT Pin

The EMIF supports the Extend Wait Mode. This is a mode in which the external asynchronous device may assert control over the length of the strobe period. The Extended Wait Mode can be entered by setting the EW bit in the asynchronous n configuration register (CEnCFG) ($n = 2, 3$, or 4). When this bit is set, the EMIF monitors the EMIF_nWAIT pin to determine if the attached device wishes to extend the strobe period of the current access cycle beyond the programmed number of clock cycles.

When the EMIF detects that the EMIF_nWAIT pin has been asserted, it will begin inserting extra strobe cycles into the operation until the EMIF_nWAIT pin is deactivated by the external device. The EMIF will then return to the last cycle of the programmed strobe period and the operation will proceed as usual from this point. Please refer to the device data manual for details on the timing requirements of the EMIF_nWAIT signal.

The EMIF_nWAIT pin cannot be used to extend the strobe period indefinitely. The programmable MAX_EXT_WAIT field in the asynchronous wait cycle configuration register (AWCC) determines the maximum number of EMIF_CLK cycles the strobe period may be extended beyond the programmed length. When the counter expires, the EMIF proceeds to the hold period of the operation regardless of the state of the EMIF_nWAIT pin. The EMIF can also generate an interrupt upon expiration of this counter. See [Section 23.2.9.1](#) for details on enabling this interrupt.

For the EMIF to function properly in the Extended Wait mode, the WP n bit of AWCC must be programmed to match the polarity of the EMIF_nWAIT pin. In its reset state of 1, the EMIF will insert wait cycles when the EMIF_nWAIT pin is sampled high. When set to 0, the EMIF will insert wait cycles only when EMIF_nWAIT is sampled low. This programmability allows for a glueless connection to larger variety of asynchronous devices.

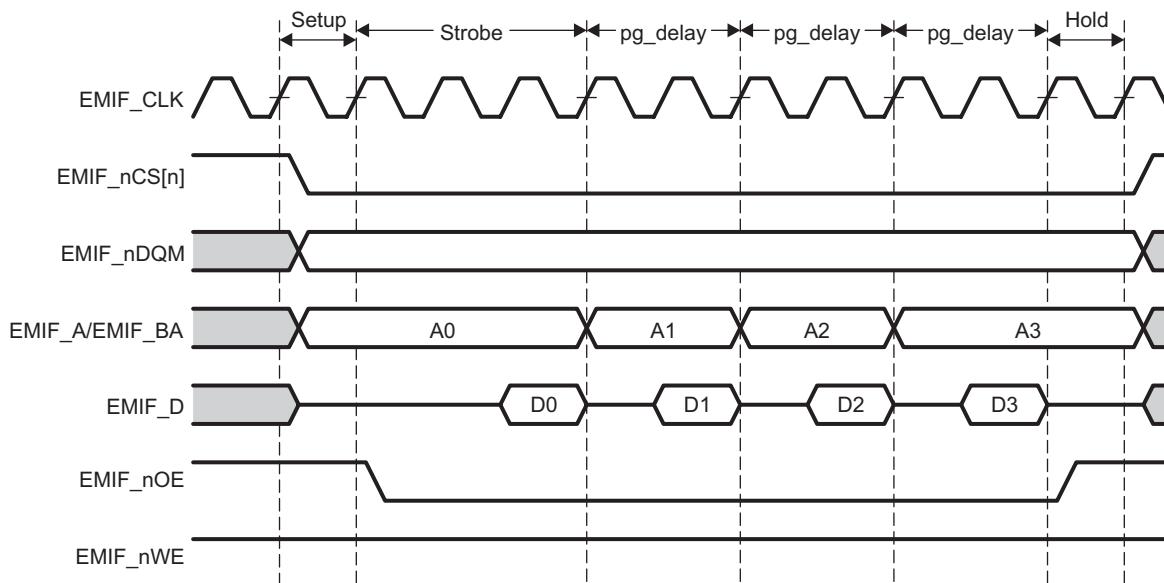
Finally, a restriction is placed on the strobe period timing parameters when operating in Extended Wait mode. Specifically, the sum of the W_SETUP and W_STROBE fields must be greater than 4, and the sum of the R_SETUP and R_STROBE fields must be greater than 4 for the EMIF to recognize the EMIF_nWAIT pin has been asserted. The W_SETUP, W_STROBE, R_SETUP, and R_STROBE fields are in CEnCFG.

23.2.6.7 NOR Flash Page Mode

EMIF supports Page mode reads for NOR Flash on its asynchronous memory chip selects. This mode can be enabled by writing a 1 to the CS_n_PG_MD_EN ($n = 2, 3$, or 4) field in the Page Mode Control register for the chip select in consideration. Whenever Page Mode for reads is enabled for a particular chip select, the page size for the device connected must also be programmed in the CS_n_PG_SIZE field of the Page Mode Control register. The address change to valid read data available timing must be programmed in the CS_n_PG_DEL field of the Page Control register. All other asynchronous memory timings must be programmed in the asynchronous configuration register (CE_nCFG). See [Figure 23-15](#) for read in asynchronous page mode.

NOTE: The Extended Wait mode and the Select Strobe mode must be disabled when using the asynchronous interface in Page mode.

Figure 23-15. Asynchronous Read in Page Mode



23.2.7 Data Bus Parking

The EMIF always drives the data bus to the previous write data value when it is idle. This feature is called data bus parking. Only when the EMIF issues a read command to the external memory does it stop driving the data bus. After the EMIF latches the last read data, it immediately parks the data bus again.

The one exception to this behavior occurs after performing an asynchronous read operation while the EMIF is in the self-refresh state. In this situation, the read operation is not followed by the EMIF parking the data bus. Instead, the EMIF tri-states the data bus. Therefore, it is not recommended to perform asynchronous read operations while the EMIF is in the self-refresh state, in order to prevent floating inputs on the data bus. External pull-ups, such as $10\text{k}\Omega$ resistors, should be placed on the 16 EMIF data bus pins (which do not have internal pull-ups) if it is required to perform reads in this situation. The precise resistor value should be chosen so that the worst case combined off-state leakage currents do not cause the voltage levels on the associated pins to drop below the high-level input voltage requirement.

For information about the self-refresh state, see [Section 23.2.5.7](#).

23.2.8 Reset and Initialization Considerations

The EMIF memory controller has two active-low reset signals, CHIP_RST_n and MOD_G_RST_n. Both these reset signals are driven by the device system reset signal. This device does not offer the flexibility to reset just the EMIF state machine without also resetting the EMIF controller's memory-mapped registers. As soon as the device system reset is released (driven High), the EMIF memory controller immediately begins its initialization sequence. Command and data stored in the EMIF memory controller FIFOs are lost. Refer the Architecture chapter of the technical reference manual (TRM) for more information on conditions that can cause a device system reset to be asserted.

When system reset is released, the EMIF automatically begins running the SDRAM initialization sequence described in [Section 23.2.5.4](#). Even though the initialization procedure is automatic, a special procedure, found in [Section 23.2.5](#) must still be followed.

23.2.9 Interrupt Support

The EMIF supports a single interrupt to the CPU. [Section 23.2.9.1](#) details the generation and internal masking of EMIF interrupts.

23.2.9.1 Interrupt Events

There are three conditions that may cause the EMIF to generate an interrupt to the CPU. These conditions are:

- A rising edge on the EMIF_nWAIT signal (wait rise interrupt)
- An asynchronous time out
- Usage of unsupported addressing mode (line trap interrupt)

The wait rise interrupt occurs when a rising edge is detected on EMIF_nWAIT signal. This interrupt generation is not affected by the WPn bit in the asynchronous wait cycle configuration register (AWCC). The asynchronous time out interrupt condition occurs when the attached asynchronous device fails to deassert the EMIF_nWAIT pin within the number of cycles defined by the MAX_EXT_WAIT bit in AWCC (this happens only in extended wait mode). EMIF supports only linear incrementing and cache line wrap addressing modes . If an access request for an unsupported addressing mode is received, the EMIF will set the LT bit in the EMIF interrupt raw register (INTRAW) and treat the request as a linear incrementing request.

Only when the interrupt is enabled by setting the appropriate bit (WR_MASK_SET/AT_MASK_SET/LT_MASK_SET) in the EMIF interrupt mask set register (INTMSKSET) to 1, will the interrupt be sent to the CPU. Once enabled, the interrupt may be disabled by writing a 1 to the corresponding bit in the EMIF interrupt mask clear register (INTMSKCLR). The bit fields in both the INTMSKSET and INTMSKCLR may be used to indicate whether the interrupt is enabled. When the interrupt is enabled, the corresponding bit field in both the INTMSKSET and INTMSKCLR will have a value of 1; when the interrupt is disabled, the corresponding bit field will have a value of 0.

The EMIF interrupt raw register (INTRAW) and the EMIF interrupt mask register (INTMSK) indicate the status of each interrupt. The appropriate bit (WR/AT/LT) in INTRAW is set when the interrupt condition occurs, whether or not the interrupt has been enabled. However, the appropriate bit (WR_MASKED/AT_MASKED/LT_MASKED) in INTMSK is set only when the interrupt condition occurs and the interrupt is enabled. Writing a 1 to the bit in INTRAW clears the INTRAW bit as well as the corresponding bit in INTMSK. [Table 23-24](#) contains a brief summary of the interrupt status and control bit fields. See for complete details on the register fields.

Table 23-24. Interrupt Monitor and Control Bit Fields

Register Name	Bit Name	Description
EMIF interrupt raw register (INTRAW)	WR	This bit is set when an rising edge on the EMIF_nWAIT signal occurs. Writing a 1 clears the WR bit as well as the WR_MASKED bit in INTMSK.
	AT	This bit is set when an asynchronous timeout occurs. Writing a 1 clears the AT bit as well as the AT_MASKED bit in INTMSK.
	LT	This bit is set when an unsupported addressing mode is used. Writing a 1 clears LT bit as well as the LT_MASKED bit in INTMSK.
EMIF interrupt mask register (INTMSK)	WR_MASKED	This bit is set only when a rising edge on the EMIF_nWAIT signal occurs and the interrupt has been enabled by writing a 1 to the WR_MASK_SET bit in INTMSKSET.
	AT_MASKED	This bit is set only when an asynchronous timeout occurs and the interrupt has been enabled by writing a 1 to the AT_MASK_SET bit in INTMSKSET.
	LT_MASKED	This bit is set only when line trap interrupt occurs and the interrupt has been enabled by writing a 1 to the LT_MASK_SET bit in INTMSKSET.
EMIF interrupt mask set register (INTMSKSET)	WR_MASK_SET	Writing a 1 to this bit enables the wait rise interrupt.
	AT_MASK_SET	Writing a 1 to this bit enables the asynchronous timeout interrupt.
	LT_MASK_SET	Writing a 1 to this bit enables the line trap interrupt.
EMIF interrupt mask clear register (INTMSKCLR)	WR_MASK_CLR	Writing a 1 to this bit disables the wait rise interrupt.
	AT_MASK_CLR	Writing a 1 to this bit disables the asynchronous timeout interrupt.
	LT_MASK_CLR	Writing a 1 to this bit disables the line trap interrupt.

23.2.10 DMA Event Support

EMIF memory controller is a DMA slave peripheral and therefore does not generate DMA events. Data read and write requests may be made directly, by masters and the DMA.

23.2.11 EMIF Signal Multiplexing

For details on EMIF signal multiplexing, see the I/O Multiplexing Module chapter of the technical reference manual.

23.2.12 Memory Map

For information describing the device memory-map, see your device-specific datasheet.

23.2.13 Priority and Arbitration

[Section 23.2.2](#) describes the external prioritization and arbitration among requests from different sources within the microcontroller. The result of this external arbitration is that only one request is presented to the EMIF at a time. Once the EMIF completes a request, the external arbiter then provides the EMIF with the next pending request.

Internally, the EMIF undertakes memory device transactions according to a strict priority scheme. The highest priority events are:

- A device reset.
- A write to any of the three least significant bytes of the SDRAM configuration register (SDCR).

Either of these events will cause the EMIF to immediately commence its initialization sequence as described in [Section 23.2.5.4](#).

Once the EMIF has completed its initialization sequence, it performs memory transactions according to the following priority scheme (highest priority listed first):

1. If the EMIF's backlog refresh counter is at the Refresh Must urgency level, the EMIF performs multiple SDRAM auto refresh cycles until the Refresh Release urgency level is reached.
2. If an SDRAM or asynchronous read has been requested, the EMIF performs a read operation.
3. If the EMIF's backlog refresh counter is at the Refresh Need urgency level, the EMIF performs an SDRAM auto refresh cycle.
4. If an SDRAM or asynchronous write has been requested, the EMIF performs a write operation.
5. If the EMIF's backlog refresh counter is at the Refresh May or Refresh Release urgency level, the EMIF performs an SDRAM auto refresh cycle.
6. If the value of the SR bit in SDCR has been set to 1, the EMIF will enter the self-refresh state as described in [Section 23.2.5.7](#).

After taking one of the actions listed above, the EMIF then returns to the top of the priority list to determine its next action.

Because the EMIF does not issue auto-refresh cycles when in the self-refresh state, the above priority scheme does not apply when in this state. See [Section 23.2.5.7](#) for details on the operation of the EMIF when in the self-refresh state.

23.2.14 System Considerations

This section describes various system considerations to keep in mind when operating the EMIF.

23.2.14.1 Asynchronous Request Times

In a system that interfaces to both SDRAM and asynchronous memory, the asynchronous requests must not take longer than the smaller of the following two values:

- t_{RAS} (typically 120 μ s) - to avoid violating the maximum time allowed between issuing an ACTV and PRE command to the SDRAM.
- $t_{\text{Refresh Rate}} \times 11$ (typically 15.7 μ s \times 11 = 172.7 μ s) - to avoid refresh violations on the SDRAM.

The length of an asynchronous request is controlled by multiple factors, the primary factor being the number of access cycles required to complete the request. For example, an asynchronous request for 4 bytes will require four access cycles using an 8-bit data bus and only two access cycle using a 16-bit data bus. The maximum request size that the EMIF can be sent is 16 words, therefore the maximum number of access cycles per memory request is 64 when the EMIF is configured with an 8-bit data bus. The length of the individual access cycles that make up the asynchronous request is determined by the programmed setup, strobe, hold, and turnaround values, but can also be extended with the assertion of the EMIF_nWAIT input signal up to a programmed maximum limit. It is up to the user to make sure that an entire asynchronous request does not exceed the timing values listed above when also interfacing to an SDRAM device. This can be done by limiting the asynchronous timing parameters.

23.2.14.2 Interface to External Peripheral or FIFO Memory

If EMIF is used to interface to an external peripheral or FIFO logic (e.g. UHPI), it is recommended to use the host CPU's Memory Protection Unit (MPU) to define this external memory range as a region that is either strongly-ordered or of device type.

23.2.14.3 Interface to External SDRAM

If EMIF is used to interface to an external SDRAM, it is recommended to burst as much as possible to normal memory to improve the interface bandwidth.

23.2.15 Power Management

Power dissipation from the EMIF memory controller may be managed by following methods:

- Self-refresh mode
- Power-down mode
- Gating input clocks to the module off

Gating input clocks off to the EMIF memory controller achieves higher power savings when compared to the power savings of self-refresh or power down mode. The input clock VCLK3 can be turned off through the use of the Global Clock Module (GCM). Before gating clocks off, the EMIF memory controller must place the SDR SDRAM memory in self-refresh mode. If the external memory requires a continuous clock, the VCLK3 clock domain must not be turned off because this may result in data corruption. See the following subsections for the proper procedures to follow when stopping the EMIF memory controller clocks.

23.2.15.1 Power Management Using Self-Refresh Mode

The EMIF can be placed into a self-refresh state in order to place the attached SDRAM devices into self-refresh mode, which consumes less power for most SDRAM devices. In this state, the attached SDRAM device uses an internal clock to perform its own auto refresh cycles. This maintains the validity of the data in the SDRAM without the need for any external commands. Refer to [Section 23.2.5.7](#) for more details on placing the EMIF into the self-refresh state.

23.2.15.2 Power Management Using Power Down Mode

In the power down mode, EMIF drives EMIF_CKE low to lower the power consumption. EMIF_CKE goes high when there is a need to send refresh (REFR) commands, after which EMIF_CKE is again driven low. EMIF_CKE remains low until any request arrives. Refer to [Section 23.2.5.8](#) for more details on placing EMIF in power down mode.

23.2.16 Emulation Considerations

EMIF memory controller remains fully functional during emulation halts in order to allow emulation access to external memory.

23.3 Example Configuration

This section presents an example of interfacing the EMIF to both an SDR SDRAM device and an asynchronous flash device.

23.3.1 Hardware Interface

[Figure 23-16](#) shows the hardware interface between the EMIF, a Samsung K4S641632H-TC(L)70 64Mb SDRAM device, and two SHARP LH28F800BJE-PTTL90 8Mb Flash memory. The connection between the EMIF and the SDRAM is straightforward, but the connection between the EMIF and the flash deserves a detailed look.

The address inputs for the flash are provided by three sources. The A[18:0] address inputs are provided by a combination of the EMIF_A and EMIF_BA pins according to [Section 23.2.6.1](#). RD/nBY signal from one flash is connected to EMIF_nWAIT pin of EMIF.

Finally, this example configuration connects the EMIF_nWE pin to the nWE input of the flash and operates the EMIF in Select Strobe Mode.

23.3.2 Software Configuration

The following sections describe how to configure the EMIF registers and bit fields to interface the EMIF with the Samsung K4S641632H-TC(L)70 SDRAM and the SHARP LH28F800BJE-PTTL90 8Mb Flash memory.

23.3.2.1 Configuring the SDRAM Interface

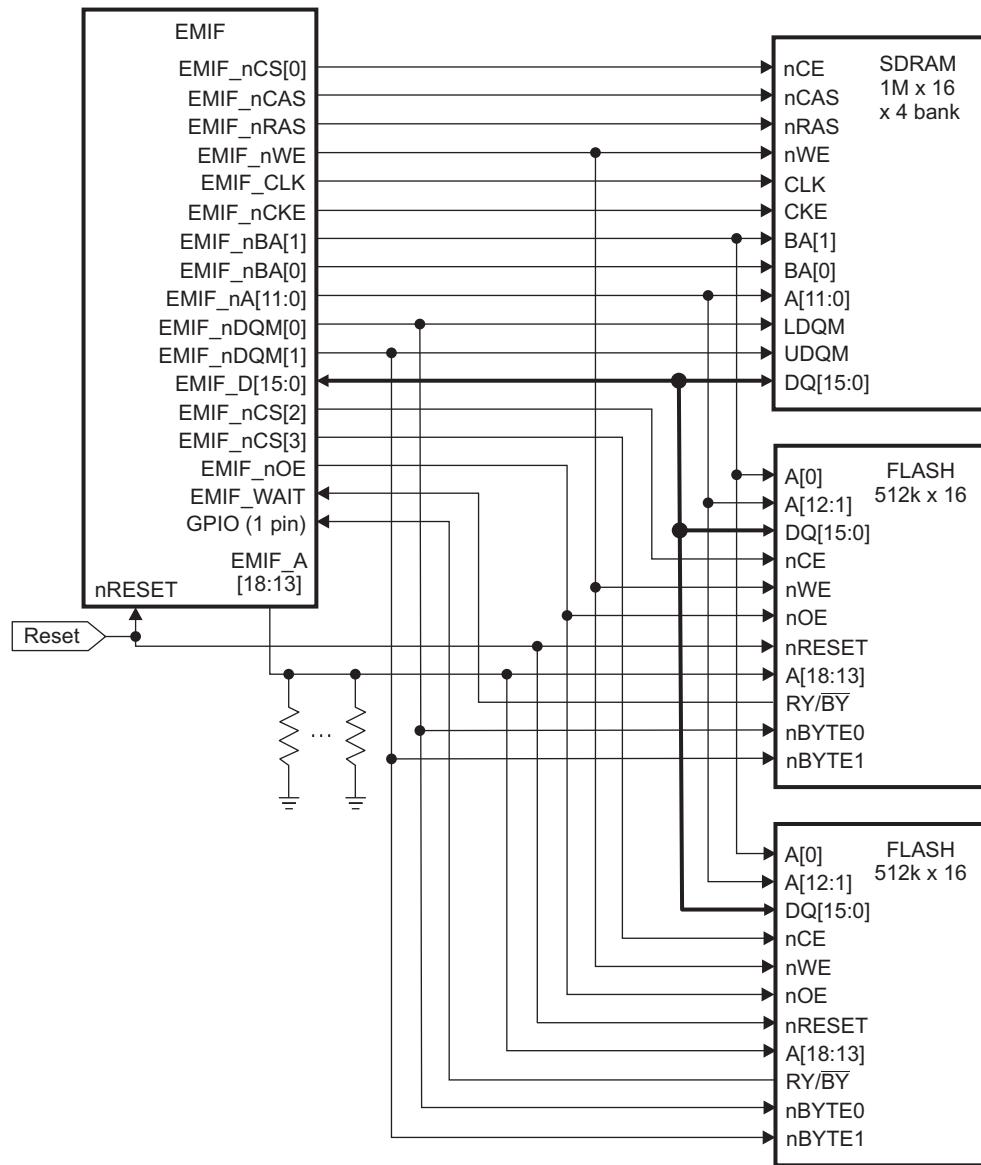
This section describes how to configure the EMIF to interface with the Samsung K4S641632H-TC(L)70 SDRAM with a clock frequency of $f_{EMIF_CLK} = 100$ MHz. Procedure A described in [Section 23.2.5.5](#) is followed which assumes that the SDRAM power-up timing constraint were met during the SDRAM Auto-Initialization sequence after Reset.

23.3.2.1.1 PLL Programming for the EMIF to K4S641632H-TC(L)70 Interface

The device global clock module (GCM) should first be programmed to select the desired EMIF_CLK frequency. Before doing this, the SDRAM should be placed in Self-Refresh Mode by setting the SR bit in the SDRAM configuration register (SDCR). The SR bit should be set using a byte-write to the upper byte of the SDCR to avoid triggering the SDRAM Initialization Sequence. The EMIF_CLK frequency can now be configured to the desired value by selecting the appropriate clock source for the VCLK3 domain. Once the VCLK3 domain frequency has been configured, remove the SDRAM from Self-Refresh by clearing the SR bit in SDCR, again with a byte-write.

Table 23-25. SR Field Value For the EMIF to K4S641632H-TC(L)70 Interface

Field	Value	Purpose
SR	1 then 0	To place the EMIF into the self refresh state

Figure 23-16. Example Configuration Interface


23.3.2.1.2 SDRAM Timing Register (SDTIMR) Settings for the EMIF to K4S641632H-TC(L)70 Interface

The fields of the SDRAM timing register (SDTIMR) should be programmed first as described in [Table 23-26](#) to satisfy the required timing parameters for the K4S641632H-TC(L)70. Based on these calculations, a value of 6111 4610h should be written to SDTIMR. [Figure 23-17](#) shows a graphical description of how SDTIMR should be programmed.

Table 23-26. SDTIMR Field Calculations for the EMIF to K4S641632H-TC(L)70 Interface

Field Name	Formula	Value from K4S641632H-TC(L)70 Datasheet	Value Calculated for Field
T_RFC	$T_{RFC} \geq (t_{RFC} \times f_{EMIF_CLK}) - 1$	$t_{RC} = 68 \text{ ns (min)}^{(1)}$	6
T_RP	$T_{RP} \geq (t_{RP} \times f_{EMIF_CLK}) - 1$	$t_{RP} = 20 \text{ ns (min)}$	1
T_RCD	$T_{RCD} \geq (t_{RCD} \times f_{EMIF_CLK}) - 1$	$t_{RCD} = 20 \text{ ns (min)}$	1
T_WR	$T_{WR} \geq (t_{WR} \times f_{EMIF_CLK}) - 1$	$t_{RDL} = 2 \text{ CLK} = 20 \text{ ns (min)}^{(2)}$	1
T_RAS	$T_{RAS} \geq (t_{RAS} \times f_{EMIF_CLK}) - 1$	$t_{RAS} = 49 \text{ ns (min)}$	4
T_RC	$T_{RC} \geq (t_{RC} \times f_{EMIF_CLK}) - 1$	$t_{RC} = 68 \text{ ns (min)}$	6
T_RRD	$T_{RRD} \geq (t_{RRD} \times f_{EMIF_CLK}) - 1$	$t_{RRD} = 14 \text{ ns (min)}$	1

⁽¹⁾ The Samsung datasheet does not specify a t_{RFC} value. Instead, Samsung specifies t_{RC} as the minimum auto refresh period.

⁽²⁾ The Samsung datasheet does not specify a t_{WR} value. Instead, Samsung specifies t_{RDL} as last data in to row precharge minimum delay.

Figure 23-17. SDRAM Timing Register (SDTIMR)

31	27	26	24	23	22	20	19	18	16
0 0110		001	0		001	0		001	
T_RFC		T_RP	Rsvd		T_RCD	Rsvd		T_WR	
15	12	11	8	7	6	4	3		0
0100		0110	0		001		0000		
T_RAS		T_RC	Rsvd		T_RRD		Reserved		

23.3.2.1.3 SDRAM Self Refresh Exit Timing Register (SDSRETR) Settings for the EMIF to K4S641632H-TC(L)70 Interface

The SDRAM self refresh exit timing register (SDSRETR) should be programmed second to satisfy the t_{XSR} timing requirement from the K4S641632H-TC(L)70 datasheet. [Table 23-27](#) shows the calculation of the proper value to program into the T_XS field of this register. Based on this calculation, a value of 6h should be written to SDSRETR. [Figure 23-18](#) shows how SDSRETR should be programmed.

Table 23-27. RR Calculation for the EMIF to K4S641632H-TC(L)70 Interface

Field Name	Formula	Value from K4S641632H-TC(L)70 Datasheet	Value Calculated for Field
T_XS	$T_{XS} \geq (t_{XSR} \times f_{EMIF_CLK}) - 1$	$t_{RC} = 68 \text{ ns (min)}^{(1)}$	6

⁽¹⁾ The Samsung datasheet does not specify a t_{XSR} value. Instead, Samsung specifies t_{RC} as the minimum required time after CKE going high to complete self refresh exit.

Figure 23-18. SDRAM Self Refresh Exit Timing Register (SDSRETR)

31	0000 0000 0000 0000		16
Reserved			
15	000 0000 0000	5 4	0
Reserved		0 0110	
		T_XS	

23.3.2.1.4 SDRAM Refresh Control Register (SDRCR) Settings for the EMIF to K4S641632H-TC(L)70 Interface

The SDRAM refresh control register (SDRCR) should next be programmed to satisfy the required refresh rate of the K4S641632H-TC(L)70. [Table 23-28](#) shows the calculation of the proper value to program into the RR field of this register. Based on this calculation, a value of 61Ah should be written to SDRCR. [Figure 23-19](#) shows how SDRCR should be programmed.

Table 23-28. RR Calculation for the EMIF to K4S641632H-TC(L)70 Interface

Field Name	Formula	Values	Value Calculated for Field
RR	$RR \leq f_{EMIF_CLK} \times t_{\text{Refresh Period}} / n_{\text{cycles}}$	From SDRAM datasheet: $t_{\text{Refresh Period}} = 64 \text{ ms}$; $n_{\text{cycles}} = 4096$ EMIF clock rate: $f_{EMIF_CLK} = 100 \text{ MHz}$	$RR = 1562 \text{ cycles} = 61Ah \text{ cycles}$

Figure 23-19. SDRAM Refresh Control Register (SDRCR)

31	0 0000 0000 0000		19	18	16
Reserved					
15	13	12			0
000		0 0110 0001 1010 (61Ah)			
Reserved		RR			

23.3.2.1.5 SDRAM Configuration Register (SDCR) Settings for the EMIF to K4S641632H-TC(L)70 Interface

Finally, the fields of the SDRAM configuration register (SDCR) should be programmed as described in [Table 23-25](#) to properly interface with the K4S641632H-TC(L)70 device. Based on these settings, a value of 4720h should be written to SDCR. [Figure 23-20](#) shows how SDCR should be programmed. The EMIF is now ready to perform read and write accesses to the SDRAM.

Table 23-29. SDCR Field Values For the EMIF to K4S641632H-TC(L)70 Interface

Field	Value	Purpose
SR	0	To avoid placing the EMIF into the self refresh state
NM	1	To configure the EMIF for a 16-bit data bus
CL	011b	To select a CAS latency of 3
BIT11_9LOCK	1	To allow the CL field to be written
IBANK	010b	To select 4 internal SDRAM banks
PAGESIZE	0	To select a page size of 256 words

Figure 23-20. SDRAM Configuration Register (SDCR)

31	30	29	28				24
0	0	0		0 0000			
SR	Reserved	Reserved		Reserved			
23			18	17	16		
	00 0000			0	0		
	Reserved			Reserved	Reserved		
15	14	13	12	11	9	8	
0	1	0	0	011		1	
Reserved	NM	Reserved	Reserved	CL			BIT11_9LOCK
7	6		4	3	2	0	
0		010		0	000		
Reserved		IBANK		Reserved			PAGESIZE

23.3.2.2 Configuring the Flash Interface

This section describes how to configure the EMIF to interface with the two of SHARP LH28F800BJE-PTTL90 8Mb Flash memory with a clock frequency of $f_{EMIF_CLK} = 100$ MHz. The example assumes that one flash is connected to EMIF_nCS2 and the other to EMIF_nCS3.

23.3.2.2.1 Asynchronous 1 Configuration Register (CE2CFG) Settings for the EMIF to LH28F800BJE-PTTL90 Interface

The asynchronous 1 configuration register (CE2CFG) and asynchronous 2 configuration register (CE3CFG) are the only registers that is necessary to program for this asynchronous interface (assuming that one Flash is connected to EMIF_nCS[2] and the other to EMIF_nCS[3]). The SS bit (in both registers) should be set to 1 to enable Select Strobe Mode and the ASIZE field (in both registers) should be set to 1 to select a 16-bit interface. The other fields in this register control the shaping of the EMIF signals, and the proper values can be determined by referring to the AC Characteristics in the Flash datasheet and the device datasheet. Based on the following calculations, a value of 8862 25BDh should be written to CE2CFG. Table 23-30 and Table 23-31 show the pertinent AC Characteristics for reads and writes to the Flash device, and Figure 23-21 and Figure 23-22 show the associated timing waveforms. Finally, Figure 23-23 shows programming the CEnCFG ($n = 2, 3$) with the calculated values.

Table 23-30. AC Characteristics for a Read Access

AC Characteristic	Device	Definition	Min	Max	Unit
t_{SU}	EMIF	Setup time, read EMIF_D before EMIF_CLK high	6.5		ns
t_H	EMIF	Data hold time, read EMIF_D after EMIF_CLK high	1		ns
t_D	EMIF	Output delay time, EMIF_CLK high to output signal valid		7	ns
t_{ELQV}	Flash	nCE to Output Delay	90		ns
t_{EHQZ}	Flash	nCE High to Output in High Impedance	55		ns

Table 23-31. AC Characteristics for a Write Access

AC Characteristic	Device	Definition	Min	Max	Unit
t_{AVAV}	Flash	Write Cycle Time	90		ns
t_{ELEH}	Flash	nCE Pulse Width Low	50		ns
t_{EHEL}	Flash	nCE Pulse Width High (not shown in Figure 23-22)	30		ns

Figure 23-21. LH28F800BJE-PTTL90 to EMIF Read Timing Waveforms

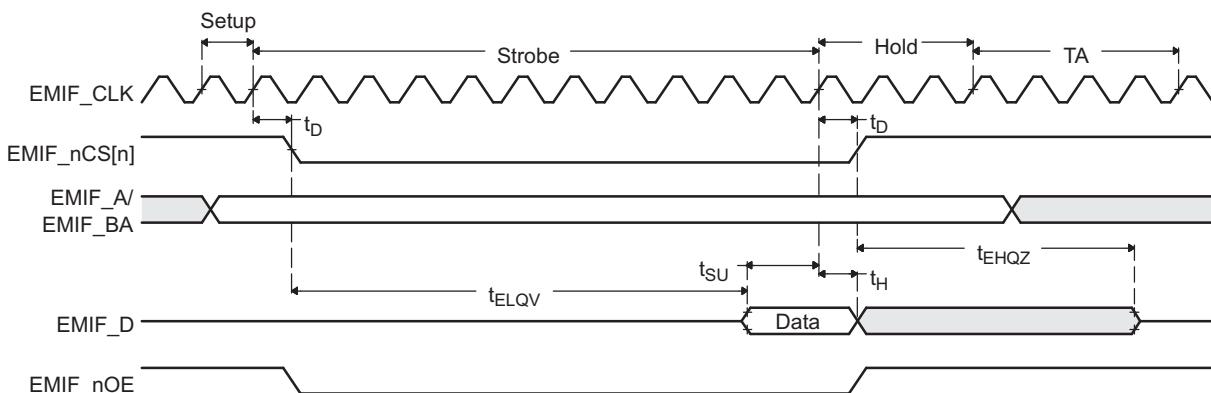
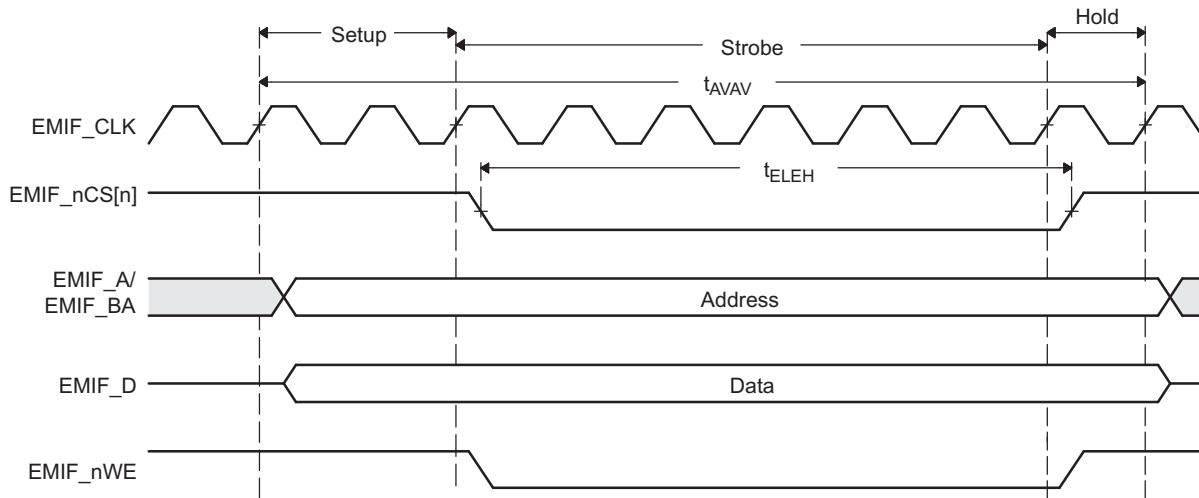


Figure 23-22. LH28F800BJE-PTTL90 to EMIF Write Timing Waveforms

The R_STROBE field should be set to meet the following equation:

$$R_STROBE \geq (t_D + t_{ELQV} + t_{SU}) \times f_{EMIF_CLK} - 1$$

$$R_STROBE \geq (7 \text{ ns} + 90 \text{ ns} + 6.5 \text{ ns}) \times 100 \text{ MHz} - 1$$

$$R_STROBE \geq 9.35$$

$$R_STROBE = 10$$

The R_HOLD field must be large enough to satisfy the EMIF Data hold time, t_H :

$$R_HOLD \geq t_H \times f_{EMIF_CLK} - 1$$

$$R_HOLD \geq 1 \text{ ns} \times 100 \text{ MHz} - 1$$

$$R_HOLD \geq -0.9$$

The R_HOLD field must also combine with the TA field to satisfy the Flash's nCE High to Output in High Impedance time, t_{EHQZ} :

$$R_HOLD + TA \geq (t_D + t_{EHQZ}) \times f_{EMIF_CLK} - 2$$

$$R_HOLD + TA \geq (7 \text{ ns} + 55 \text{ ns}) \times 100 \text{ MHz} - 2$$

$$R_HOLD + TA \geq 4.2$$

The largest value that can be programmed into the TA field is 3h, therefore the following values can be used:

$$R_HOLD = 2$$

$$TA = 3$$

For Writes, the W_STROBE field should be set to satisfy the Flash's nCE Pulse Width constraint, t_{ELEH} :

$$W_STROBE \geq t_{ELEH} \times f_{EMIF_CLK} - 1$$

$$W_STROBE \geq 50 \text{ ns} \times 100 \text{ MHz} - 1$$

$$W_STROBE \geq 4$$

The W_SETUP and W_HOLD fields should combine to satisfy the Flash's nCE Pulse Width High constraint, t_{EHEL} , when performing back-to-back writes:

$$W_{\text{SETUP}} + W_{\text{HOLD}} \geq t_{EHEL} \times f_{\text{EMIF_CLK}} - 2$$

$$W_{\text{SETUP}} + W_{\text{HOLD}} \geq 30 \text{ ns} \times 100 \text{ MHz} - 2$$

$$W_{\text{SETUP}} + W_{\text{HOLD}} \geq 1$$

In addition, the entire Write access length must satisfy the Flash's minimum Write Cycle Time, t_{AVAV} :

$$W_{\text{SETUP}} + W_{\text{STROBE}} + W_{\text{HOLD}} \geq t_{AVAV} \times f_{\text{EMIF_CLK}} - 3$$

$$W_{\text{SETUP}} + W_{\text{STROBE}} + W_{\text{HOLD}} \geq 90 \text{ ns} \times 100 \text{ MHz} - 3$$

$$W_{\text{SETUP}} + W_{\text{STROBE}} + W_{\text{HOLD}} \geq 6$$

Solving the above equations for the Write fields results in the following possible solution:

$$W_{\text{SETUP}} = 1$$

$$W_{\text{STROBE}} = 5$$

$$W_{\text{HOLD}} = 0$$

Adding a 10 ns (1 cycle) margin to each of the periods (excluding TA which is already at its maximum) in this example produces the following recommended values:

$$W_{\text{SETUP}} = 2h$$

$$W_{\text{STROBE}} = 6h$$

$$W_{\text{HOLD}} = 1h$$

$$R_{\text{SETUP}} = 1h$$

$$R_{\text{STROBE}} = Bh$$

$$R_{\text{HOLD}} = 3h$$

$$TA = 3h$$

Figure 23-23. Asynchronous m Configuration Register ($m = 1, 2$) (CE n CFG ($n = 2, 3$))

31	30	29	26	25	24
1	0		0010		00
SS	EW		W_SETUP		W_STROBE
23		20	19	17	16
	0110		001		0
	W_STROBE		W_HOLD		R_SETUP
15	13	12	7	6	4
001		001011	011	11	01
R_SETUP		R_STROBE	R_HOLD	TA	ASIZE

23.4 Registers

23.4.1 EMIF Base Addresses

Table 23-32. EMIF Base Address Table

Device Registers	Register Name	Start Address	End Address
Emif1Regs	EMIF_REGS	0x0004_7000	0x0004_77FF
Emif2Regs ⁽¹⁾	EMIF_REGS	0x0004_7800	0x0004_7FFF
Emif1ConfigRegs	EMIF1_CONFIG_REGS	0x0005_F480	0x0005_F49F
Emif2ConfigRegs	EMIF2_CONFIG_REGS	0x0005_F4A0	0x0005_F4BF

⁽¹⁾ Only available on CPU1.

23.4.2 EMIF_REGS Registers

Table 23-33 lists the memory-mapped registers for the EMIF_REGS. All register offset addresses not listed in Table 23-33 should be considered as reserved locations and the register contents should not be modified.

Table 23-33. EMIF_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	RCSR	Revision Code and Status Register	Section 23.4.2.1	
2h	ASYNC_WCCR	Async Wait Cycle Config Register	Section 23.4.2.2	
4h	SDRAM_CR	SDRAM (EMxCS0n) Config Register	Section 23.4.2.3	
6h	SDRAM_RCR	SDRAM Refresh Control Register	Section 23.4.2.4	
8h	ASYNC_CS2_CR	Async 1 (EMxCS2n) Config Register	Section 23.4.2.5	
Ah	ASYNC_CS3_CR	Async 2 (EMxCS3n) Config Register	Section 23.4.2.6	
Ch	ASYNC_CS4_CR	Async 3 (EMxCS4n) Config Register	Section 23.4.2.7	
10h	SDRAM_TR	SDRAM Timing Register	Section 23.4.2.8	
18h	TOTAL_SDRAM_AR	Total SDRAM Accesses Register	Section 23.4.2.9	
1Ah	TOTAL_SDRAM_ACTR	Total SDRAM Activate Register	Section 23.4.2.10	
1Eh	SDR_EXT_TMNG	SDRAM SR/PD Exit Timing Register	Section 23.4.2.11	
20h	INT_RAW	Interrupt Raw Register	Section 23.4.2.12	
22h	INT_MSK	Interrupt Masked Register	Section 23.4.2.13	
24h	INT_MSK_SET	Interrupt Mask Set Register	Section 23.4.2.14	
26h	INT_MSK_CLR	Interrupt Mask Clear Register	Section 23.4.2.15	
28h	IO_CTRL	IO Control Register	Section 23.4.2.16	
2Ah	IO_STAT	IO Status Register	Section 23.4.2.17	
56h	MODEL_REL_NUM	Module Release Number Register	Section 23.4.2.18	

23.4.2.1 RCSR Register (offset = 0h) [reset = 40000205h]

RCSR is shown in [Figure 23-24](#) and described in [Table 23-34](#).

Revision Code and Status Register

Figure 23-24. RCSR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BE	FR	MODULE_ID													
R-0h	R-1h	R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAJOR_REVISION								MINOR_REVISION							
R-2h								R-5h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-34. RCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BE	R	0h	EMIF endian mode. 0: Little Endian. 1: Big Endian.
30	FR	R	1h	EMIF operating rate. 0: Half Rate. 1: Full Rate.
29-16	MODULE_ID	R	0h	EMIF module ID. 0x0000: EMIF_24. 0x000E: EMIF_24 SDRAM. 0x000F: EMIF_24 ASYNC.
15-8	MAJOR_REVISION	R	2h	Major Revision. EMIF code revisions are indicated by a revision code taking the format major_revision.minor_revision.
7-0	MINOR_REVISION	R	5h	Minor Revision. See major_revision field description.

23.4.2.2 ASYNC_WCCR Register (offset = 2h) [reset = F0000080h]

ASYNC_WCCR is shown in [Figure 23-25](#) and described in [Table 23-35](#).

Async Wait Cycle Config Register

Figure 23-25. ASYNC_WCCR Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	RESERVED	WP0		RESERVED		
R-0h	R-0h	R-0h	R/W-1h		R-0h		
23	22	21	20	19	18	17	16
RESERVED		RESERVED		RESERVED		RESERVED	
R-0h		R-0h		R-0h		R-0h	
15	14	13	12	11	10	9	8
			RESERVED				
7	6	5	4	3	2	1	0
			MAX_EXT_WAIT				
				R/W-80h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-35. ASYNC_WCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	WP0	R/W	1h	Defines the polarity of the EMxWAIT port.: 0: Wait if EMxWAIT port is low. 1: Wait if EMxWAIT port is high.
27-24	RESERVED	R	0h	Reserved
23-22	RESERVED	R	0h	Reserved
21-20	RESERVED	R	0h	Reserved
19-18	RESERVED	R	0h	Reserved
17-16	RESERVED	R	0h	Reserved
15-8	RESERVED	R	0h	Reserved
7-0	MAX_EXT_WAIT	R/W	80h	The EMIF will wait for (max_ext_wait + 1) * 16 clock cycles before an extended asynchronous cycle is terminated.

23.4.2.3 SDRAM_CR Register (offset = 4h) [reset = 620h]

SDRAM_CR is shown in [Figure 23-26](#) and described in [Table 23-36](#).

SDRAM (EMxCS0n) Config Register

Figure 23-26. SDRAM_CR Register

31	30	29	28	27	26	25	24
SR	PD	PDWR		RESERVED		RESERVED	
R/W-0h	R/W-0h	R/W-0h		R-0h		R-0h	
23	22	21	20	19	18	17	16
RESERVED		ROWSIZE		IBANK_POS		RESERVED	BIT_25_17_LOCK
R-0h		R/W-0h		R/W-0h		R-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	NM	RESERVED	RESERVED		CL		BIT_11_9_LOC_K
R-0h	R/W-0h	R-0h	R-0h		R/W-3h		R=0/W=1-0h
7	6	5	4	3	2	1	0
RESERVED		IBANK		RESERVED		PAGESIGE	
R-0h		R/W-2h		R-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-36. SDRAM_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SR	R/W	0h	Self Refresh. Writing a 1 to this bit will cause connected SDRAM devices to be placed into Self Refresh mode and the EMIF to enter the self refresh state. In this state the EMIF will service all asynchronous memory accesses immediately but any SDRAM access will take at least t_ras + 1 cycles due to the time required for the SDRAM devices to exit Self Refresh mode. If an SDRAM access immediately follows the setting of the sr bit, the access will take t_ras + t_xs + 2 cycles. If both sr and pd bits are set, the EMIF will go into Self Refresh.
30	PD	R/W	0h	Power Down. Writing a 1 to this bit will cause connected SDRAM devices to be placed into Power Down mode and the EMIF to enter the power down state. If both sr and pd bits are set, the EMIF will go into Self Refresh.
29	PDWR	R/W	0h	Perform refreshes during Power Down. Writing a 1 to this bit will cause the EMIF to exit the power down state and issue an AUTO REFRESH command every time Refresh May level is set.
28-26	RESERVED	R	0h	Reserved
25-23	RESERVED	R	0h	Reserved

Table 23-36. SDRAM_CR Register Field Descriptions (continued)

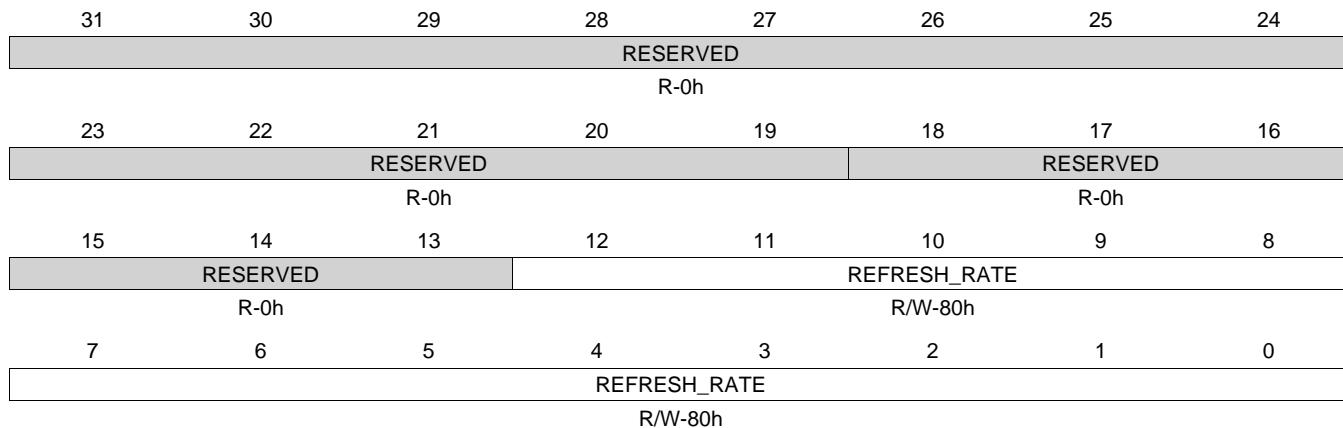
Bit	Field	Type	Reset	Description
22-20	ROWSIZE	R/W	0h	<p>Defines the number of row address bits of connected SDRAM devices :</p> <p>000: 9 row address bits. 001: 10 row address bits. 010: 11 row address bits. 011: 12 row address bits. 100: 13 row address bits. 101: 14 row address bits. 110: 15 row address bits. 111: 16 row address bits.</p> <p>This field is only used when ibank_pos bit in SDRAM Config register is set to 1.</p> <p>A write to this field will cause the EMIF to start the SDRAM initialization sequence.</p>
19	IBANK_POS	R/W	0h	<p>Internal bank position.</p> <p>0: Assign internal bank address bits from VBUSP address as shown in Table 5.</p> <p>1: Assign internal bank address bits from VBUSP address as shown in Table 2,3 and 4.</p>
18-17	RESERVED	R	0h	Reserved
16	BIT_25_17_LOCK	R/W	0h	Bits 25 to 17 can only be written if this bit is set to 1.
15	RESERVED	R	0h	Reserved
14	NM	R/W	0h	<p>Narrow mode. Set to 1 when system bus width to memory bus width is 2:1 for SDR SDRAM. Set to 0 when system bus width to memory bus width is 1:1 for SDR SDRAM.</p> <p>A write to this field will cause the EMIF to start the SDRAM initialization sequence.</p>
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-9	CL	R/W	3h	<p>The value of this field defines the CAS latency to be used when accessing connected SDRAM devices. Only CAS latencies of 2 (cl = 2) and 3 (cl = 3) are supported.</p> <p>A write to this field will cause the EMIF to start the SDRAM initialization sequence.</p>
8	BIT_11_9_LOCK	R=0/W=1	0h	Bits 11 to 9 can only be written if this bit is set to 1.
7	RESERVED	R	0h	Reserved
6-4	IBANK	R/W	2h	<p>Defines number of banks inside connected SDRAM devices:</p> <p>000: 1 bank SDRAM devices. 001: 2bank SDRAM devices. 010: 3 bank SDRAM devices. 011: Reserved. 1xx: Reserved.</p> <p>A write to this field will cause the EMIF to start the SDRAM initialization sequence.</p>
3	RESERVED	R	0h	Reserved

Table 23-36. SDRAM_CR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PAGESIGE	R/W	0h	<p>Defines the internal page size of connected SDRAM devices:</p> <ul style="list-style-type: none"> 000: 256-word pages requiring 8 column address bits. 001: 512-word pages requiring 9 column address bits. 010: 1024-word pages requiring 10 column address bits. 011: 2048-word pages requiring 11 column address bits. 1xx: Reserved. <p>A write to this field will cause the EMIF to start the SDRAM initialization sequence.</p>

23.4.2.4 SDRAM_RCR Register (offset = 6h) [reset = 80h]SDRAM_RCR is shown in [Figure 23-27](#) and described in [Table 23-37](#).

SDRAM Refresh Control Register

Figure 23-27. SDRAM_RCR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-37. SDRAM_RCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	RESERVED	R	0h	Reserved
15-13	RESERVED	R	0h	Reserved
12-0	REFRESH_RATE	R/W	80h	Value in this field is used to define the rate at which connected SDRAM devices will be refreshed, as follows: SDRAM refresh rate = EMIF rate / refresh_rate where EMIF rate is equal to clk rate when full_rate = 1 or half clk rate when full_rate = 0. Writing a value < 0x0020 to this field will cause it to be loaded with (2 * t_rfc) + 1 value from SDRAM Timing register.

23.4.2.5 ASYNC_CS2_CR Register (offset = 8h) [reset = 3FFFFFFDh]ASYNC_CS2_CR is shown in [Figure 23-28](#) and described in [Table 23-38](#).

Async 1 (EMxCS2n) Config Register

Figure 23-28. ASYNC_CS2_CR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SS	EW	W_SETUP				W_STROBE				W_HOLD				R_SE TUP	
R/W-0h	R/W-0h	R/W-Fh				R/W-3Fh				R/W-7h				R/W-Fh	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_SETUP		R_STROBE				R_HOLD				TA		ASIZE		R/W-1h	
R/W-Fh		R/W-3Fh				R/W-7h				R/W-3h		R/W-1h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-38. ASYNC_CS2_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SS	R/W	0h	Select Strobe mode. Set to 1 if chip selects need to have write or read strobe timing.
30	EW	R/W	0h	Extend Wait mode. Set to 1 if extended asynchronous cycles are required based on EMxWAIT.
29-26	W_SETUP	R/W	Fh	Write Strobe Setup cycles. Number of EM_CLK cycles from EMxAy, EMxBAy, EMxDQMy, and EMxCS2n being set to EMxWEn asserted, minus one cycle. The reset value is 16 cycles.
25-20	W_STROBE	R/W	3Fh	Write Strobe Duration cycles. Number of EM_CLK cycles for which EMxWEn is held active, minus one cycle. The reset value is 64 cycles. This field cannot be zero when ew = 1.
19-17	W_HOLD	R/W	7h	Write Strobe Hold cycles. Number of EM_CLK cycles for which EMxAy, EMxBAy, EMxDQMy, and EMxCS2n are held after EMxWEn has been deasserted, minus one cycle. The reset value is 8 cycles.
16-13	R_SETUP	R/W	Fh	Read Strobe Setup cycles. Number of EM_CLK cycles from EMxAy, EMxBAy, EMxDQMy, and EMxCS2n being set to EMxOEn asserted, minus one cycle. The reset value is 16 cycles.
12-7	R_STROBE	R/W	3Fh	Read Strobe Duration cycles. Number of EM_CLK cycles for which EMxOEn is held active, minus one cycle. The reset value is 64 cycles. This field cannot be zero when ew = 1.
6-4	R_HOLD	R/W	7h	Read Strobe Hold cycles. Number of EM_CLK cycles for which EMxAy, EMxBAy, EMxDQMy, and EMxCS2n are held after EMxOEn has been deasserted, minus one cycle. The reset value is 8 cycles.
3-2	TA	R/W	3h	Turn Around cycles. Number of EM_CLK cycles between the end of one asynchronous memory access and the start of another asynchronous memory access, minus one cycle. This delay is not incurred between a read followed by a read, or a write followed by a write to the same chip select. The reset value is 4 cycles.
1-0	ASIZE	R/W	1h	Asynchronous Memory Size. Defines the width of the asynchronous device's data bus : 00: 8 Bit data bus. 01: 16 Bit data bus. 10: 32 Bit data bus. 11: Reserved.

23.4.2.6 ASYNC_CS3_CR Register (offset = Ah) [reset = 3FFFFFFFDh]

ASYNC_CS3_CR is shown in [Figure 23-29](#) and described in [Table 23-39](#).

Async 2 (EMxCS3n) Config Register

Figure 23-29. ASYNC_CS3_CR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SS	EW	W_SETUP				W_STROBE				W_HOLD				R_SE TUP	
R/W-0h	R/W-0h	R/W-Fh				R/W-3Fh				R/W-7h				R/W-Fh	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_SETUP		R_STROBE				R_HOLD				TA		ASIZE			
R/W-Fh		R/W-3Fh				R/W-7h				R/W-3h		R/W-1h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-39. ASYNC_CS3_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SS	R/W	0h	Select Strobe mode. Set to 1 if chip selects need to have write or read strobe timing.
30	EW	R/W	0h	Extend Wait mode. Set to 1 if extended asynchronous cycles are required based on EMxWAIT.
29-26	W_SETUP	R/W	Fh	Write Strobe Setup cycles. Number of EM_CLK cycles from EMxAy, EMxBAy, EMxDQMy, and EMxCS3n being set to EMxWEn asserted, minus one cycle. The reset value is 16 cycles.
25-20	W_STROBE	R/W	3Fh	Write Strobe Duration cycles. Number of EM_CLK cycles for which EMxWEn is held active, minus one cycle. The reset value is 64 cycles. This field cannot be zero when ew = 1.
19-17	W_HOLD	R/W	7h	Write Strobe Hold cycles. Number of EM_CLK cycles for which EMxAy, EMxBAy, EMxDQMy, and EMxCS3n are held after EMxWEn has been deasserted, minus one cycle. The reset value is 8 cycles.
16-13	R_SETUP	R/W	Fh	Read Strobe Setup cycles. Number of EM_CLK cycles from EMxAy, EMxBAy, EMxDQMy, and EMxCS3n being set to EMxOEn asserted, minus one cycle. The reset value is 16 cycles.
12-7	R_STROBE	R/W	3Fh	Read Strobe Duration cycles. Number of EM_CLK cycles for which EMxOEn is held active, minus one cycle. The reset value is 64 cycles. This field cannot be zero when ew = 1.
6-4	R_HOLD	R/W	7h	Read Strobe Hold cycles. Number of EM_CLK cycles for which EMxAy, EMxBAy, EMxDQMy, and EMxCS3n are held after EMxOEn has been deasserted, minus one cycle. The reset value is 8 cycles.
3-2	TA	R/W	3h	Turn Around cycles. Number of EM_CLK cycles between the end of one asynchronous memory access and the start of another asynchronous memory access, minus one cycle. This delay is not incurred between a read followed by a read, or a write followed by a write to the same chip select. The reset value is 4 cycles.
1-0	ASIZE	R/W	1h	Asynchronous Memory Size. Defines the width of the asynchronous device's data bus : 00: 8 Bit data bus. 01: 16 Bit data bus. 10: 32 Bit data bus. 11: Reserved.

23.4.2.7 ASYNC_CS4_CR Register (offset = Ch) [reset = 3FFFFFFDh]ASYNC_CS4_CR is shown in [Figure 23-30](#) and described in [Table 23-40](#).

Async 3 (EMxCS4n) Config Register

Figure 23-30. ASYNC_CS4_CR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SS	EW	W_SETUP				W_STROBE				W_HOLD				R_SE TUP	
R/W-0h	R/W-0h	R/W-Fh				R/W-3Fh				R/W-7h				R/W-Fh	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_SETUP		R_STROBE				R_HOLD				TA		ASIZE			
R/W-Fh				R/W-3Fh				R/W-7h				R/W-3h		R/W-1h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-40. ASYNC_CS4_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SS	R/W	0h	Select Strobe mode. Set to 1 if chip selects need to have write or read strobe timing.
30	EW	R/W	0h	Extend Wait mode. Set to 1 if extended asynchronous cycles are required based on EMxWAIT.
29-26	W_SETUP	R/W	Fh	Write Strobe Setup cycles. Number of EM_CLK cycles from EMxAy, EMxBAy, EMxDQMy, and EMxCS4n being set to EMxWEn asserted, minus one cycle. The reset value is 16 cycles.
25-20	W_STROBE	R/W	3Fh	Write Strobe Duration cycles. Number of EM_CLK cycles for which EMxWEn is held active, minus one cycle. The reset value is 64 cycles. This field cannot be zero when ew = 1.
19-17	W_HOLD	R/W	7h	Write Strobe Hold cycles. Number of EM_CLK cycles for which EMxAy, EMxBAy, EMxDQMy, and EMxCS4n are held after EMxWEn has been deasserted, minus one cycle. The reset value is 8 cycles.
16-13	R_SETUP	R/W	Fh	Read Strobe Setup cycles. Number of EM_CLK cycles from EMxAy, EMxBAy, EMxDQMy, and EMxCS4n being set to EMxOEn asserted, minus one cycle. The reset value is 16 cycles.
12-7	R_STROBE	R/W	3Fh	Read Strobe Duration cycles. Number of EM_CLK cycles for which EMxOEn is held active, minus one cycle. The reset value is 64 cycles. This field cannot be zero when ew = 1.
6-4	R_HOLD	R/W	7h	Read Strobe Hold cycles. Number of EM_CLK cycles for which EMxAy, EMxBAy, EMxDQMy, and EMxCS4n are held after EMxOEn has been deasserted, minus one cycle. The reset value is 8 cycles.
3-2	TA	R/W	3h	Turn Around cycles. Number of EM_CLK cycles between the end of one asynchronous memory access and the start of another asynchronous memory access, minus one cycle. This delay is not incurred between a read followed by a read, or a write followed by a write to the same chip select. The reset value is 4 cycles.
1-0	ASIZE	R/W	1h	Asynchronous Memory Size. Defines the width of the asynchronous device's data bus : 00: 8 Bit data bus. 01: 16 Bit data bus. 10: 32 Bit data bus. 11: Reserved.

23.4.2.8 SDRAM_TR Register (offset = 10h) [reset = 19214610h]

SDRAM_TR is shown in [Figure 23-31](#) and described in [Table 23-41](#).

SDRAM Timing Register

Figure 23-31. SDRAM_TR Register

31	30	29	28	27	26	25	24
T_RFC					T_RP		
R/W-3h					R/W-1h		
23	22	21	20	19	18	17	16
RESERVED	T_RCD			RESERVED	T_WR		
R-0h	R/W-2h			R-0h	R/W-1h		
15	14	13	12	11	10	9	8
T_RAS				T_RC			
R/W-4h				R/W-6h			
7	6	5	4	3	2	1	0
RESERVED	T_RRD			RESERVED			
R-0h	R/W-1h			R-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

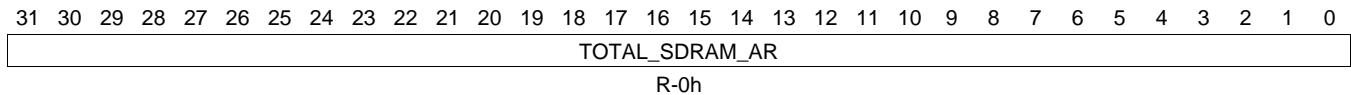
Table 23-41. SDRAM_TR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	T_RFC	R/W	3h	Minimum number of EM_CLK cycles from Refresh or Load Mode to Refresh or Activate, minus one.
26-24	T_RP	R/W	1h	Minimum number of EM_CLK cycles from Precharge to Activate or Refresh, minus one.
23	RESERVED	R	0h	Reserved
22-20	T_RCD	R/W	2h	Minimum number of EM_CLK cycles from Activate to Read or Write, minus one.
19	RESERVED	R	0h	Reserved
18-16	T_WR	R/W	1h	For SDR, this is equal to minimum number of EM_CLK cycles from last Write transfer to Precharge, minus one.
15-12	T_RAS	R/W	4h	Minimum number of EM_CLK cycles from Activate to Precharge, minus one. t_ras >= t_rcd.
11-8	T_RC	R/W	6h	Minimum number of EM_CLK cycles from Activate to Activate minus one.
7	RESERVED	R	0h	Reserved
6-4	T_RRD	R/W	1h	Minimum number of EM_CLK cycles from Activate to Activate for a different bank, minus one.
3-0	RESERVED	R	0h	Reserved

23.4.2.9 TOTAL_SDRAM_AR Register (offset = 18h) [reset = 0h]

TOTAL_SDRAM_AR is shown in [Figure 23-32](#) and described in [Table 23-42](#).

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Figure 23-32. TOTAL_SDRAM_AR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-42. TOTAL_SDRAM_AR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TOTAL_SDRAM_AR	R	0h	Indicates the total number of VBUSP accesses to SDRAM. This counter is incremented by two for a single VBUSP access crossing page boundaries.

23.4.2.10 TOTAL_SDRAM_ACTR Register (offset = 1Ah) [reset = 0h]TOTAL_SDRAM_ACTR is shown in [Figure 23-33](#) and described in [Table 23-43](#).

Total SDRAM Activate Register

Figure 23-33. TOTAL_SDRAM_ACTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOTAL_SDRAM_ACTR																															

R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-43. TOTAL_SDRAM_ACTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TOTAL_SDRAM_ACTR	R	0h	Indicates the total number of SDRAM accesses which required an activate command.

23.4.2.11 SDR_EXT_TMNG Register (offset = 1Eh) [reset = 7h]

SDR_EXT_TMNG is shown in [Figure 23-34](#) and described in [Table 23-44](#).

SDRAM SR/PD Exit Timing Register

Figure 23-34. SDR_EXT_TMNG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED		T_XS					
R-0h																								R-0h		R/W-7h					

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-44. SDR_EXT_TMNG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-5	RESERVED	R	0h	Reserved
4-0	T_XS	R/W	7h	This is equal to minimum number of EM_CLK cycles from Self Refresh exit to any command, minus one. For SDR SDRAM, this count should satisfy tXSR.

23.4.2.12 INT_RAW Register (offset = 20h) [reset = 0h]

INT_RAW is shown in [Figure 23-35](#) and described in [Table 23-45](#).

Interrupt Raw Register

Figure 23-35. INT_RAW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R-0h								WR				LT		AT	
								R/W=1-0h				R/W=1		R/W=1	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

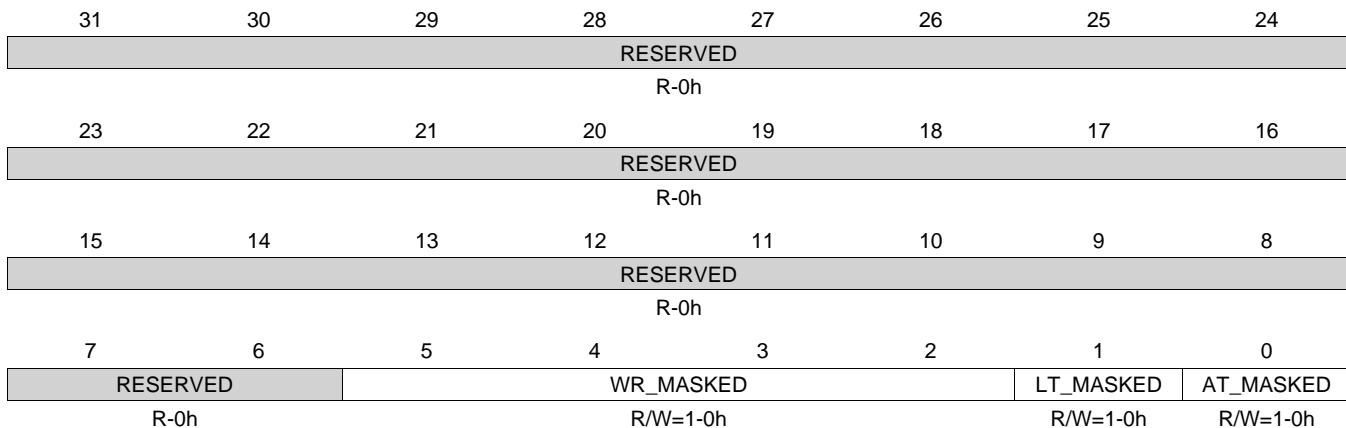
Table 23-45. INT_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5-2	WR	R/W=1	0h	Wait Rise. Set to 1 by hardware to indicate rising edge on the corresponding EMxWAIT has been detected. The WPx bits in the Async Wait Cycle Config register has no effect on these bits. Writing a 1 will clear these bits as well as the wr_masked bits in the Interrupt Masked register. Writing a 0 has no effect.
1	LT	R/W=1	0h	Line Trap. Set to 1 by hardware to indicate illegal memory access type or invalid cache line size. Writing a 1 will clear this bit as well as the lt_masked bit in the Interrupt Masked register. Writing a 0 has no effect.
0	AT	R/W=1	0h	Asynchronous Timeout. Set to 1 by hardware to indicate that during an extended asynchronous memory access cycle, the EMxWAIT signal did not go inactive within the number of cycles defined by the max_ext_wait field in Async Wait Cycle Config register. Writing a 1 will clear this bit as well as the at_masked bit in the Interrupt Masked register. Writing a 0 has no effect.

23.4.2.13 INT_MSK Register (offset = 22h) [reset = 0h]

INT_MSK is shown in [Figure 23-36](#) and described in [Table 23-46](#).

Interrupt Masked Register

Figure 23-36. INT_MSK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

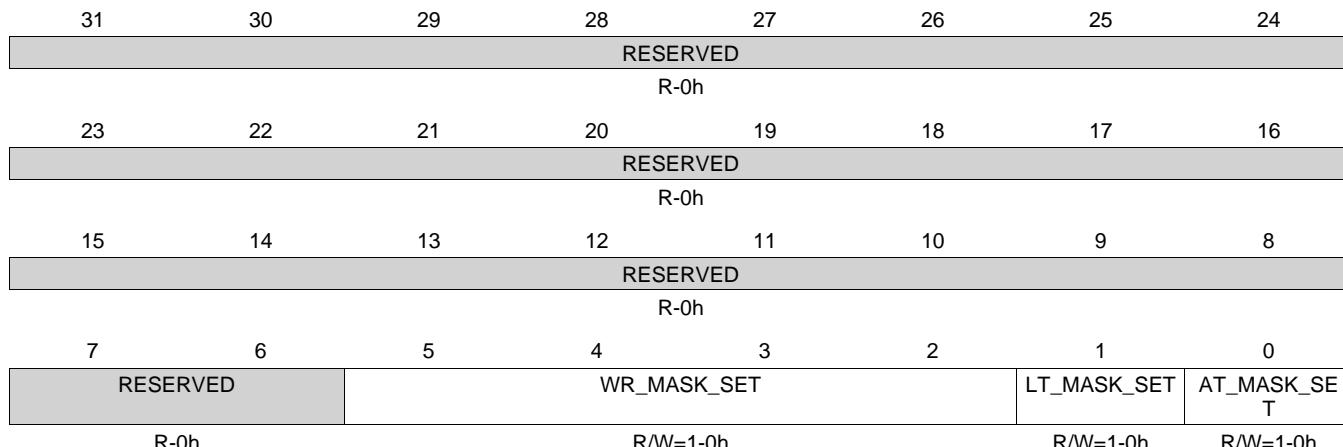
Table 23-46. INT_MSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5-2	WR_MASKED	R/W=1	0h	Masked Wait Rise. Set to 1 by hardware to indicate rising edge on the corresponding EMxWAIT has been detected, only if the wr_mask_set bit in the Interrupt Mask Set register is set to 1. The WPx bits in the Async Wait Cycle Config register has no effect on these bits. Writing a 1 will clear these bits as well as the wr bits in the Interrupt Raw register. Writing a 0 has no effect.
1	LT_MASKED	R/W=1	0h	Masked Line Trap. Set to 1 by hardware to indicate illegal memory access type or invalid cache line size, only if the lt_mask_set bit in the Interrupt Mask Set register is set to 1. Writing a 1 will clear this bit as well as the lt bit in the Interrupt Raw register. Writing a 0 has no effect.
0	AT_MASKED	R/W=1	0h	Masked Asynchronous Timeout. Set to 1 by hardware to indicate that during an extended asynchronous memory access cycle, the EMxWAIT signal did not go inactive within the number of cycles defined by the max_ext_wait field in Async Wait Cycle Config register, only if the at_mask_set bit in the Interrupt Mask Set register is set to 1. Writing a 1 will clear this bit as well as the at bit in the Interrupt Raw register. Writing a 0 has no effect.

23.4.2.14 INT_MSK_SET Register (offset = 24h) [reset = 0h]

INT_MSK_SET is shown in [Figure 23-37](#) and described in [Table 23-47](#).

Interrupt Mask Set Register

Figure 23-37. INT_MSK_SET Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

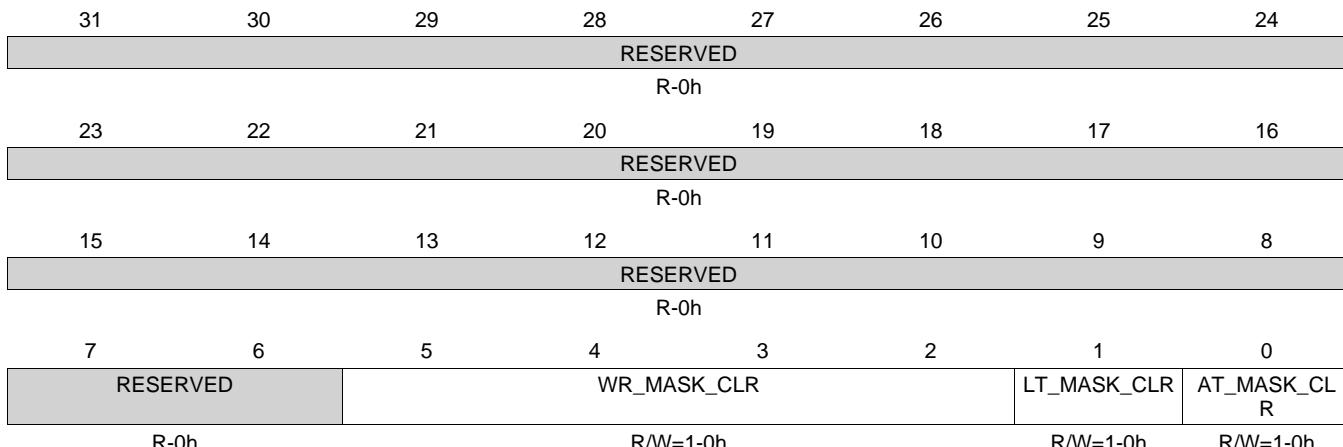
Table 23-47. INT_MSK_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5-2	WR_MASK_SET	R/W=1	0h	Mask set for wr_masked bits in the Interrupt Masked Register. Writing a 1 will enable the interrupts, and set these bits as well as the wr_mask_clr bits in the Interrupt Mask Clear register. Writing a 0 has no effect.
1	LT_MASK_SET	R/W=1	0h	Mask set for lt_masked bit in the Interrupt Masked Register. Writing a 1 will enable the interrupt, and set this bit as well as the lt_mask_clr bit in the Interrupt Mask Clear register. Writing a 0 has no effect.
0	AT_MASK_SET	R/W=1	0h	Mask set for at_masked bit in the Interrupt Masked Register. Writing a 1 will enable the interrupt, and set this bit as well as the at_mask_clr bit in the Interrupt Mask Clear register. Writing a 0 has no effect.

23.4.2.15 INT_MSK_CLR Register (offset = 26h) [reset = 0h]

INT_MSK_CLR is shown in [Figure 23-38](#) and described in [Table 23-48](#).

Interrupt Mask Clear Register

Figure 23-38. INT_MSK_CLR Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-48. INT_MSK_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-6	RESERVED	R	0h	Reserved
5-2	WR_MASK_CLR	R/W=1	0h	Mask clear for wr_masked bits in the Interrupt Masked Register. Writing a 1 will disable the interrupt, and clear these bits as well as the wr_mask_set bits in the Interrupt Mask Set register. Writing a 0 has no effect.
1	LT_MASK_CLR	R/W=1	0h	Mask clear for lt_masked bit in the Interrupt Masked Register. Writing a 1 will disable the interrupt, and clear this bit as well as the lt_mask_set bit in the Interrupt Mask Set register. Writing a 0 has no effect.
0	AT_MASK_CLR	R/W=1	0h	Mask clear for at_masked bit in the Interrupt Masked Register. Writing a 1 will disable the interrupt, and clear this bit as well as the at_mask_set bit in the Interrupt Mask Set register. Writing a 0 has no effect.

23.4.2.16 IO_CTRL Register (offset = 28h) [reset = 0h]

IO_CTRL is shown in [Figure 23-39](#) and described in [Table 23-49](#).

IO Control Register

Figure 23-39. IO_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																IO_CTRL															

R-0h

R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-49. IO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	IO_CTRL	R/W	0h	This register is used to control the IOs such as the VTP calibration of the IOs. The bit field definitions are IO specific and should be described in the IO specification.

23.4.2.17 IO_STAT Register (offset = 2Ah) [reset = 0h]

IO_STAT is shown in [Figure 23-40](#) and described in [Table 23-50](#).

IO Status Register

Figure 23-40. IO_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															IO_STAT															R/W-0h	

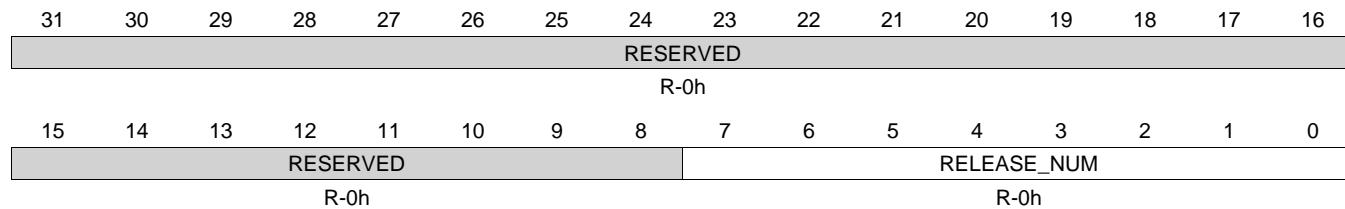
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-50. IO_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	IO_STAT	R/W	0h	This register is used to monitor the status of IOs such as the VTP calibration status of the IOs. The bit field definitions are IO specific and should be described in the IO specification.

23.4.2.18 MODEL_REL_NUM Register (offset = 56h) [reset = 0h]MODEL_REL_NUM is shown in [Figure 23-41](#) and described in [Table 23-51](#).

Module Release Number Register

Figure 23-41. MODEL_REL_NUM Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-51. MODEL_REL_NUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RELEASE_NUM	R	0h	Release Number. This number tracks EMIF code releases.

23.4.3 EMIF1_CONFIG_REGS Registers

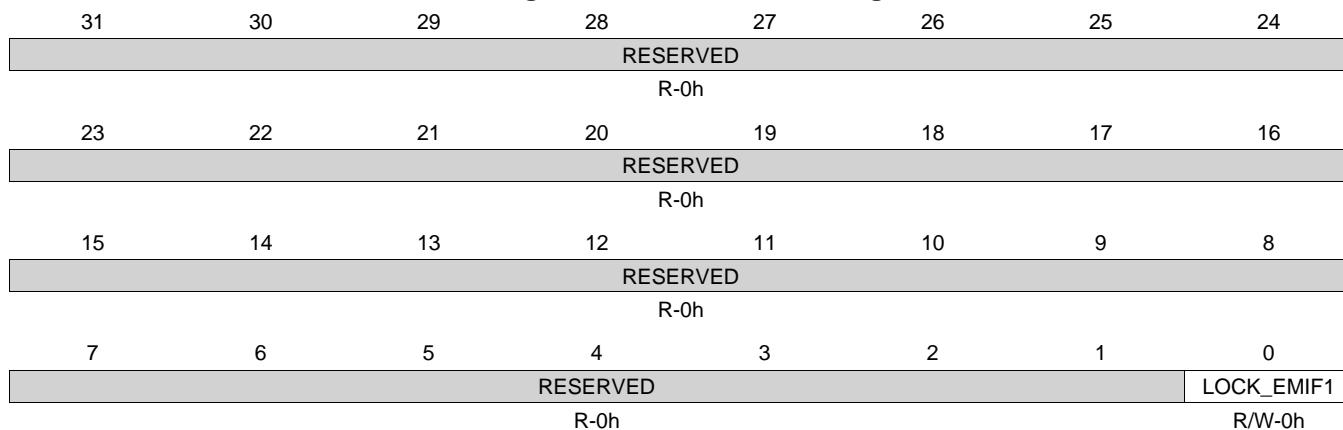
[Table 23-52](#) lists the memory-mapped registers for the EMIF1_CONFIG_REGS. All register offset addresses not listed in [Table 23-52](#) should be considered as reserved locations and the register contents should not be modified.

Table 23-52. EMIF1_CONFIG_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	EMIF1LOCK	EMIF1 Config Lock Register	Section 23.4.3.1	EALLOW
2h	EMIF1COMMIT	EMIF1 Config Lock Commit Register	Section 23.4.3.2	EALLOW
4h	EMIF1MSEL	EMIF1 Master Sel Register	Section 23.4.3.3	EALLOW
8h	EMIF1ACCPROT0	EMIF1 Config Register 0	Section 23.4.3.4	EALLOW

23.4.3.1 EMIF1LOCK Register (offset = 0h) [reset = 0h]EMIF1LOCK is shown in [Figure 23-42](#) and described in [Table 23-53](#).

EMIF1 Config Lock Register

Figure 23-42. EMIF1LOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

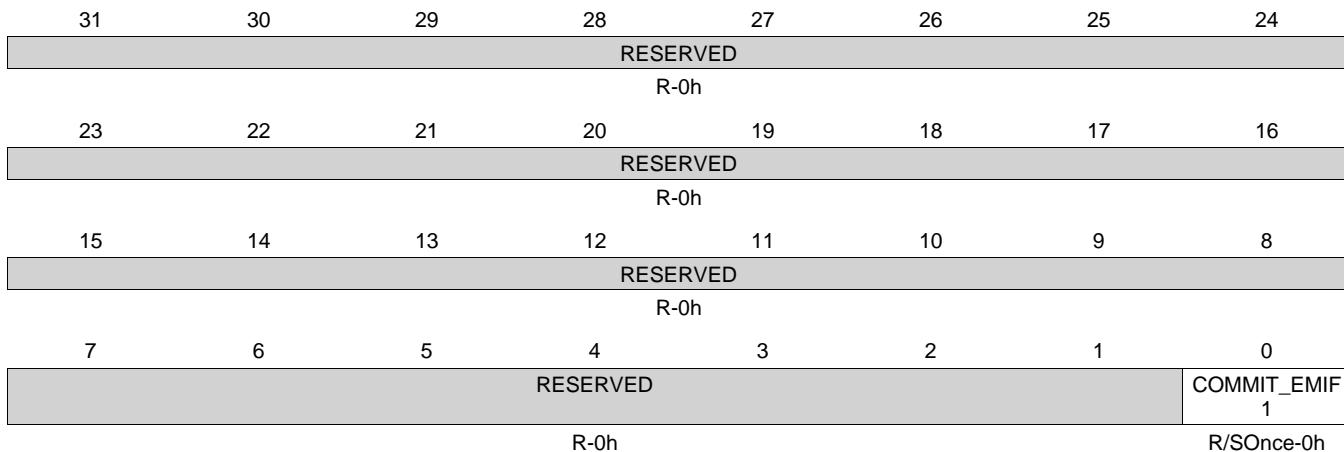
Table 23-53. EMIF1LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	LOCK_EMIF1	R/W	0h	Locks the write to access protection and master select fields for EMIF1: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.

23.4.3.2 EMIF1COMMIT Register (offset = 2h) [reset = 0h]

EMIF1COMMIT is shown in [Figure 23-43](#) and described in [Table 23-54](#).

EMIF1 Config Lock Commit Register

Figure 23-43. EMIF1COMMIT Register

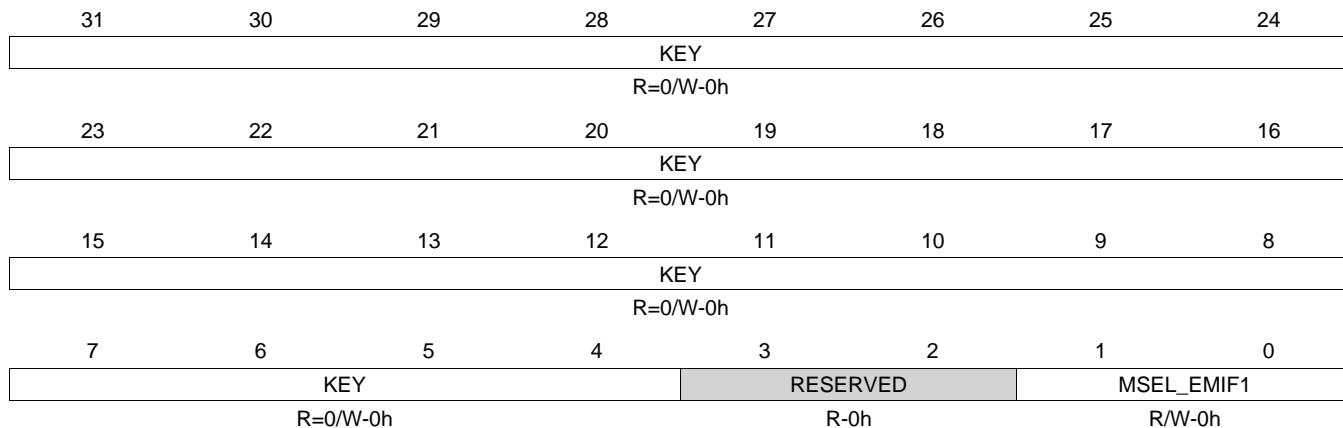
LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-54. EMIF1COMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	COMMIT_EMIF1	R/SOnce	0h	Permanently Locks the write to access protection and master select fields for EMIF1: 0: Write to ACCPROT and Mselect fields are allowed based on value of lock field in EMIF1LOCK register. 1: Write to ACCPROT and Mselect fields are permanently blocked.

23.4.3.3 EMIF1MSEL Register (offset = 4h) [reset = 0h]EMIF1MSEL is shown in [Figure 23-44](#) and described in [Table 23-55](#).

EMIF1 Master Sel Register

Figure 23-44. EMIF1MSEL Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

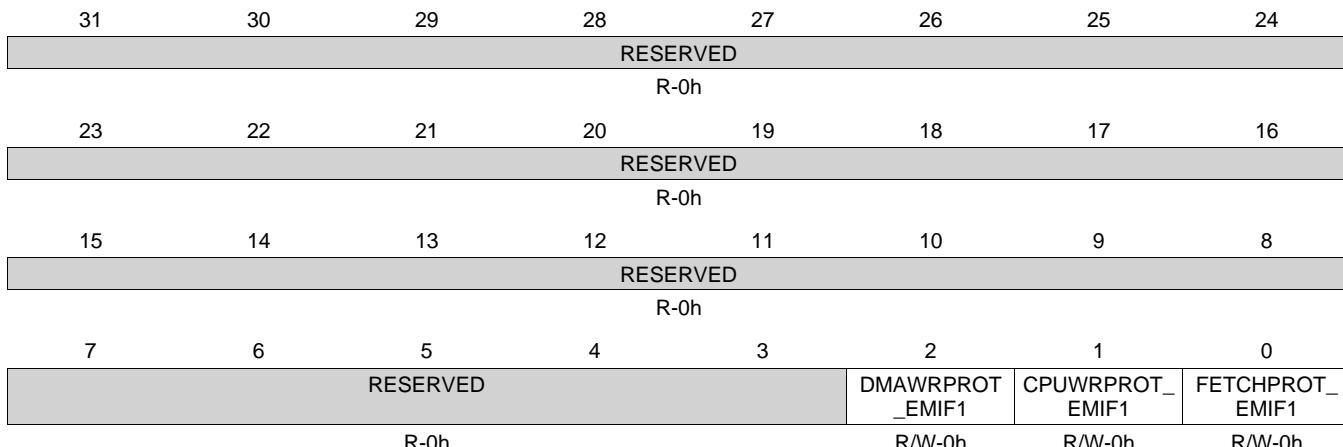
Table 23-55. EMIF1MSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	KEY	R=0/W	0h	Writing the value 0x93A5CE7 will allow the writing of the EMIF1Mselect bits, else writes are ignored. Reads will return 0.
3-2	RESERVED	R	0h	Reserved
1-0	MSEL_EMIF1	R/W	0h	Master Select for EMIF1: 00: CPU1 is master but not grabbed. CPU2 can grabbed the master ownership by changing this value to "10". 01: CPU1 is master. 10: CPU2 is master. 11: CPU1 is master but not grabbed. CPU2 can grabbed the master ownership by changing this value to "10".

23.4.3.4 EMIF1ACCPROT0 Register (offset = 8h) [reset = 0h]

EMIF1ACCPROT0 is shown in [Figure 23-45](#) and described in [Table 23-56](#).

EMIF1 Config Register 0

Figure 23-45. EMIF1ACCPROT0 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-56. EMIF1ACCPROT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-3	RESERVED	R	0h	Reserved
2	DMAWRPROT_EMIF1	R/W	0h	DMA WR Protection For EMIF1: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
1	CPUWRPROT_EMIF1	R/W	0h	CPU WR Protection For EMIF1: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
0	FETCHPROT_EMIF1	R/W	0h	Fetch Protection For EMIF1: 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.

23.4.4 EMIF2_CONFIG_REGS Registers

Table 23-57 lists the memory-mapped registers for the EMIF2_CONFIG_REGS. All register offset addresses not listed in Table 23-57 should be considered as reserved locations and the register contents should not be modified.

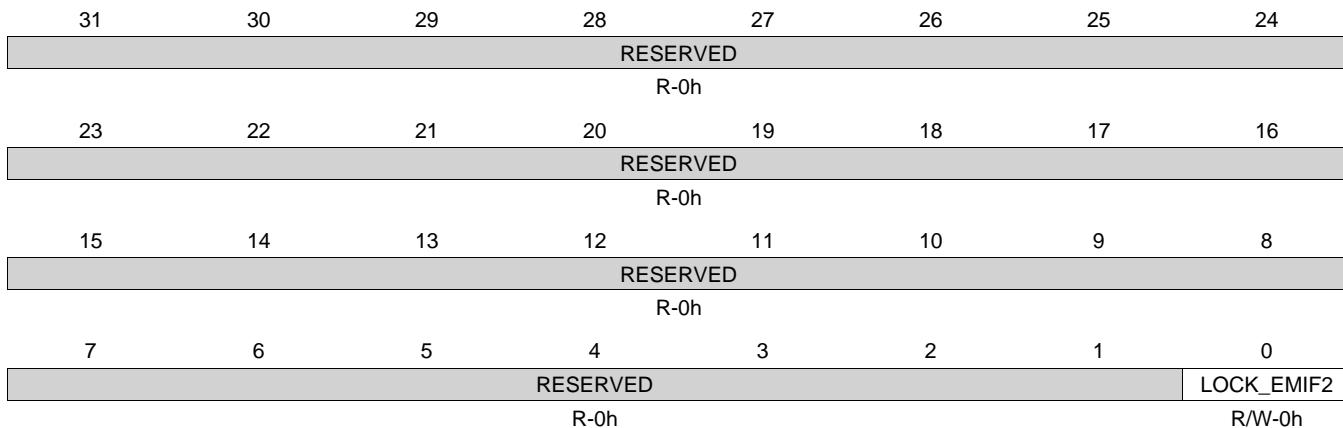
Table 23-57. EMIF2_CONFIG_REGS REGISTERS

Offset	Acronym	Register Name	Section	Write Protection
0h	EMIF2LOCK	EMIF2 Config Lock Register	Section 23.4.4.1	
2h	EMIF2COMMIT	EMIF2 Config Lock Commit Register	Section 23.4.4.2	EALLOW
8h	EMIF2ACCPROT0	EMIF2 Config Register 0	Section 23.4.4.3	EALLOW

23.4.4.1 EMIF2LOCK Register (offset = 0h) [reset = 0h]

EMIF2LOCK is shown in [Figure 23-46](#) and described in [Table 23-58](#).

EMIF2 Config Lock Register

Figure 23-46. EMIF2LOCK Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-58. EMIF2LOCK Register Field Descriptions

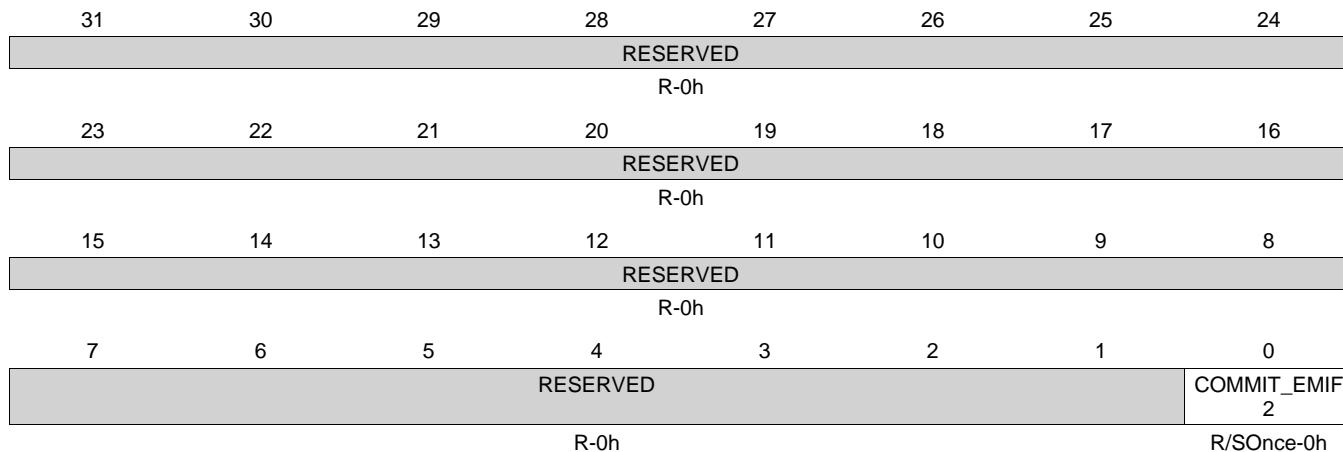
Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	LOCK_EMIF2	R/W	0h	Locks the write to access protection fields for EMIF2: 0: Write to ACCPROT and Mselect fields are allowed. 1: Write to ACCPROT and Mselect fields are blocked.

23.4.4.2 EMIF2COMMIT Register (offset = 2h) [reset = 0h]

EMIF2COMMIT is shown in [Figure 23-47](#) and described in [Table 23-59](#).

EMIF2 Config Lock Commit Register

Figure 23-47. EMIF2COMMIT Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

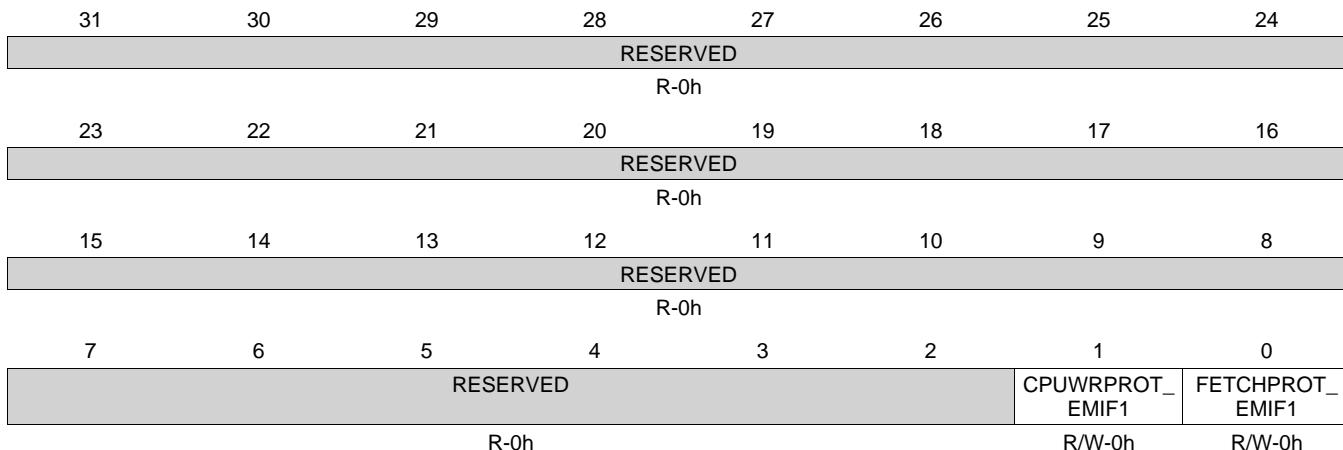
Table 23-59. EMIF2COMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-1	RESERVED	R	0h	Reserved
0	COMMIT_EMIF2	R/SOnce	0h	Permanently Locks the write to access protection fields for EMIF2: 0: Write to ACCPROT fields are allowed based on value of lock field in EMIF2LOCK register. 1: Write to ACCPROT fields are permanently blocked.

23.4.4.3 EMIF2ACCPROT0 Register (offset = 8h) [reset = 0h]

EMIF2ACCPROT0 is shown in [Figure 23-48](#) and described in [Table 23-60](#).

EMIF2 Config Register 0

Figure 23-48. EMIF2ACCPROT0 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 23-60. EMIF2ACCPROT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	RESERVED	R	0h	Reserved
1	CPUWRPROT_EMIF1	R/W	0h	CPU WR Protection For EMIF2: 0: CPU Writes are allowed. 1: CPU Writes are blocked.
0	FETCHPROT_EMIF1	R/W	0h	Fetch Protection For EMIF2 0: CPU Fetch are allowed. 1: CPU Fetch are blocked.

Revision History

Table A-1 lists the changes made since the previous version of this document.

Table A-1. Document Revision History

Chapter	Location	Additions/Modifications/Deletions
GLOBAL	Register Sections for all Chapters	Extensive modifications have been made to several of the register descriptions. It is recommended that you review your specific register for any changes.
ADC	Section 8.1.7.1	BURST Modes Example shows : AdcaRegs.BURSTCTL.BURSTEN = 2; //Enable ADC burst mode Changed to: AdcaRegs.BURSTCTL.BURSTEN = 1; //Enable ADC burst mode
	Figure 8-9	Correction to last two blocks; reversed LO and HI in the name
	Figure 8-2	Revised the graphic
Analog Subsystem	Figure 7-1	Changed ADCINCAL0 -> ADCIN14 Changed ADCINCAL1 -> ADCIN15
BootROM	Section 2.26.9	Added this section
	Section 2.17.2	Replaced IPC1 with IPC0 Replace IPC32 with IPC31
	Section 2.17.3	Replaced IPC1 with IPC0 Replace IPC32 with IPC31
	Table 2-12	Changed column label from IORSn to IO Buffers in Reset State
CAN	Section 20.4	Added the last paragraph to this section, beginning "The CAN module features a module-level interrupt enable..."
CLA	Table 4-1	Inserted the configuration options table
	Figure 4-1	Updated the block diagram
DAC	Section 9.1.1	Added "with programmable gain setting (Gain=1 or Gain=2)" to the "Analog Output Buffer" feature
	Section 9.2	Changed VREFHI and VREFLO to VREFHI and VSSA
DMA	Figure 3-1	Rename the highlighted text from SDxFLTy(1-8) to SDxFLTy (x = 1 to 2, y = 1 to 4) Rename Sigma delta (2x4) as SDFM (8 filter channels)
EMIF	Table 23-32	Moved the EMIF1_CONFIG_REGS and EMIF2_CONFIG_REGS from SYSCONTROL chapter to the EMIF chapter and update the base address tables.
ePWM	Table 12-14	CMPSS0 changed to CMPSS1, CMPSS1 changed to CMPSS2CMPSS7 changed to CMPSS8
	Figure 12-58	Renumbered input 0.0 changed to 0.1, 0.1 changed to 0.2...1.3 changed to 1.4. 31.0 changed to 31.1....31.3 changed to 31.4
	Figure 12-49	Changed X-BAR to EPWM X-BAR; added GPIO Mux and Input X-BAR
	Global	Removed all code examples
	Section 12.1	Deleted bullet beginning with "new registers added at upper..."
	Section 20.11.10	Changed type 2 to type 4

Table A-1. Document Revision History (continued)

Chapter	Location	Additions/Modifications/Deletions
	Section 12.2.3.3	Shortened "Additional Comparators on ePWM type 2" to Additional Comparators; modified the first sentence
	Section 12.2.4.4	Added ePWMS type 2 and later to the first sentence
	Figure 12-27	Removed Note D, beginning " EPWMxB can be used to generate a 50% duty square..."
	Figure 12-30	Modified text note E for clarity
	Section 12.2.5.2	Placed type 2 with type 4 in the second paragraph
	Table 12-10	Added this sentence just preceding the table "The ePWM input clock frequency that these delay values been computed by is 100 MHz."
	Section 12.2.8.1	Changed text in the title from Type 2 to Type 4
	Figure 12-63	Added the footnote to the figure
	Figure 12-5	Removed the footnote beginning "these events are generated..."
	Figure 12-64	Added the footnote, "Starts ADC conversion."
	Figure 12-50	Changed the text on the left hand side from "CPU1.PIEERR" and CPU2.PIEERR" to "CPU1.PIEVETERROR" and "CPU2.PIEVETERROR". Deleted the lines, arrows, and texts of INPUT15 and INPUT16 which is directly below the text in the previous bullet Deleted "If additional external interrupts required (or eCAP modules)"
	Table 12-15	Added TrigRegs to the base address table and register set
	Table 6-8	Changed header row of the table from 0.1, 0.2, 0.3, 0.4 to just 1, 2, 3, 4; CMPSS0 changed to CMPSS1, CMPSS1 changed to CMPSS2CMPSS7 changed to CMPSS8
	Figure 6-5	Renumbered input: 0.0 changed to 0.1, 0.1 changed to 0.2...1.3 changed to 1.4. 31.0 changed to 31.1....31.3 changed to 31.4
	Section 6.3	Included this new section
	Figure 6-6	Changed text on the left side from CPU1.PIEERR" and CPU2.PIEERR" to "CPU1.PIEVETERROR" and "CPU2.PIEVETERROR"
	Table 6-9	Included this new table
	Section 6.1.3.2	Changed the word DSP to MCU
	Table 6-2	Under Number of samples, changed DSP to MCU
	Table 13-5	Revised the entire table
	Section 13.3.1	In the first bullet under the Usage header, deleted 'in MEP_ScaleFactor' In the fourth bullet, deleted the first few words, 'In SFO_TI_Build_V7.lib, the'... Also deleted the last sentence in that bullet beginning with 'In SFO_TI_Build_V7.lib...' "
	Table 13-6	Deleted "in SFO_TI_Build_V7.lib" from the functional description.
	Section 13.3.2	In Step 1, revised the sentence beginning "For this device..." and deleted the full sentence beginning "For other device families, the device-specific equivalent..."
	Table 6-5	Removed USBVBUS and USBID rows from the table
	Section 6.1.6	Added this section
	Table 6-10	Added InputXbarRegs to the address table and list of registers; added notes to the table
	Global	Removed all ePWM type 3 references
	Section 13.2	Reworded the paragraph beginning "To generate an HRPWM waveform..."
	Figure 13-3	Revised the graphic and the Notes attached

Table A-1. Document Revision History (continued)

Chapter	Location	Additions/Modifications/Deletions
	Section 13.2.2	Revised the sentence
	Section 13.2.2	For the auto-conversion mode, minor rewording
	Section 13.2.2	In the note following, deleted from the beginning of the note: "on Type 2 HRPWM module "
	Section 13.2.3	Revised the first paragraph
	Section 13.2.4.1	Revised the first paragraph
	Section 13.2.4.2	Revised this section; assumptions, step 1, and step 2
	Section 13.2.4.2	Revised the note at the end of this section
	Section 13.2.4.3	Revised the paragraph following the bulleted list
	Table 13-4	Revised the paragraph following the table.
	Section 13.2.4.4	In the first paragraph, deleted 'via the TBPRDHR(M) register"'; replaced with "or greater."
	Section 13.2.4.4.1	Made several changes in the Assumptions, Problem, and Solution section.
	Section 13.2.5	Made several changes to the initial paragraph and ordered list
	Section 13.2.6	Revised the section
	Section 13.3.1	Revised the table and text in the Usage section
	Section 13.3.2	Removed "in SFO_TI_Build_V7.lib from the functional description column in the table; Revised text in Step 1.
IPC	Figure 5-3 and Figure 5-4	Added 'Not Allowed' to the arrows pointing to Semaphore state 10 and Semaphore state 01 boxes
McBSP	Section 19.13	Moved the McBSP Base Address Table to the McBSP Registers section.
SDFM	Global	Replace SDSFPARMx with SDDFPARMx Replaced SDFCTLPARMn with SDCTLPARMn Replaced SDFCMPHx with SDCMPHx Replaced SDFCMPLx with SDCMPLx Replaced SOSR with DOSR Replaced SDSFPARMx with SDDFPARMx Replaced SDFCPARMx with SDCPARMx
	Chapter 22	Added over-current and under-current monitoring to the description.
	Figure 11-1	Changed SDRM to SDFM in the graphic
	Section 11.1.1	In the first bullet description for 4 sigma delta clock input pins, changed '1 to 8' to '1 to 4'
		Revised or deleted text from the last three bullets
	Figure 11-2	Removed the Demodulator block from the figure
		Changed Sinc filter to Data filter in the diagram. Underneath the block diagram, revised the bulleted list.
		<ul style="list-style-type: none"> • Changed sinc filter unit to data filter unit. • Deleted integrator unit and demodulator unit. • Added comparator unit In the paragraph underneath the bulleted list, changed SINC filter to Data filter.
	Figure 11-3	Changed Filter Unit to Data Filter Unit; removed SYSCLK; REMOVED 1:1 to 1:16 mode 3 only
	Section 11.2	Changed SINC filter unit to Data filter unit;
	Figure 11-3	Changed SDSFPARMx to SDDFPARMx; removed the Integrator Unit block
	Figure 11-4	Added the note underneath the figure

Table A-1. Document Revision History (continued)

Chapter	Location	Additions/Modifications/Deletions
	Section 11.3	Revised the second sentence beginning "the comparator filter is a configurable sinc filter." In the second paragraph, changed SINC filter unit to Data filter unit.
	Section 11.4	Changed the title from, Sinc Filter Unit to Data Filter Unit; revised the first paragraph
	Section 11.5	The last paragraph after the bullet, " Four filter data acknowledge" has been revised
		Changed the title from Sinc Filter Resolution to Data Filter Resolution
	Figure 11-9	Modified the figure to change the names of the filters
	Table 11-5	Replaced these tables
	Table 11-6	
	Table 11-7	
	Table 11-8	
	Table 11-9	
System Control	Section 21.2.2	Minor revision to the first paragraph for clarity
	Figure 1-21	Modified the graphic; added dma1 read/write and dma2 read/write
	Figure 1-13	Removed reference to HRCAP
	Table 1-8	Changed INT1.13 IPC0 interrupt; INT1.14 IPC1 interrupt; INT1.15 IPC2 interrupt; INT1.16 IPC3 interrupt
	Table 1-6	Replace IPC1 with IPC0; Replace IPC2 with IPC1; Replace IPC3 with IPC2; Replace IPC4 with IPC3
	Global	Removed PIECTRL registers
	Figure 12-7	Added a footnote to the figure
	Figure 1-12	Modified the figure; added the note after the figure
	Figure 1-14	Replaced the figure
	Section 1.5.7	Added "When ECC is programmed and enabled, " preceding both paragraph in this section.
	Section 1.4.1	Changed the working from " set of interrupt inputs" to 'set of CPU interrupt inputs.' Changed working from "the ePIE block can support 192" to "The ePIE block can support up to 192..."
	Section 1.4.1.1.2	Changed IF to (PIEIFRx; changed IE to PIEIERx
	Section 1.4.1.2	Changed the first sentence from "On the control subsystem" to "On C28x devices..."
	Table 1-4	In the Address Range column, ePIE vector row, change 0x000D00 - 0x000EBF to 0x000EFF
	Figure 1-3	Changed the name of the diagram to Reset Flow Diagram; added Yes between VMAP = 1 to Vectors
	Section 1.4.1.3.4	Modified the first paragraph. Replaced 448 x 16 SARAM block with 512 x 16 SARAM blocks. Replaced 'group of eight interrupts' with 'group of 16 interrupts.'
	Section 1.7.2.7	Corrected and added tables in this section.
	Figure 1-19	Updated the figure
	Section 1.10.2	Added a list of instructions to the end of the section.
	Section 1.10.3	Added a list of instructions to the end of the section.
	Section 1.10.4	Added two lists of instructions and a note at the end of this section.
USB	Global	Modified a good portion of this chapter. Please review the full chapter.

Table A-1. Document Revision History (continued)

Chapter	Location	Additions/Modifications/Deletions
	Section 21.4	Added two sentences to the end of the first paragraph, beginning with "The USB standard mandates a frequency tolerance of 1.5% for low speed and 0.25% for full speed..." and "Thus, a high-precision..."

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