Computer Organization

Lab Introduction

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High Performance Computer System (HPCS) Lab
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Notice

- You can use Korean or English (report, question, …).
- Please **check the eTL board** for lab announcement and post your questions of each lecture and lab.
- We will touch you through eTL and e-mail very frequently, so stay tuned!
- If you have any questions, feel free to raise your hand.

Teaching Assistant (T.A.)

- T.A. (alias: ece322-ta@hpcs.snu.ac.kr)
  - Pyeongsu Park (pyeongsu@snu.ac.kr)
  - Eunjin Baek (ebaek@snu.ac.kr)
  - Suheon Bae (sheon.bae@snu.ac.kr)
  - Hunjun Lee (hunjunlee7515@snu.ac.kr)
  - And more (all of our lab members)!
- Office: R851.4-B301
- Phone: 02-880-7298
- Office hour: this lab session (5:00 PM ~ 6:30 PM)
  - If you need more, ask the professor.

Lecture Q&A Rule

- We will care all questions about lab, lecture, research, etc.

- Ground Rule: **eTL Q&A board**.
  - Use eTL Q&A board for the questions about lab and lecture.
  - We got many same questions last year.
- If you have personal questions, use the lab sessions.
- If you need more, make an appointment.

Contact Rule

- If you need to send an email, use the **alias address**.
  - One of our T.A.s will response to your mail.
  - Do not use individual e-mails without specific reasons.

- If you want to visit our lab, **make an appointment** before you come.

- When you send an e-mail about grade, absence, or score statistics, please **cc the professor**. (jangwoo@snu.ac.kr).

Purpose of Lab Sessions

- It's **for YOU**!
  - There have been tremendous requests from the last year students.

- **Explain** new project (total 8+ projects).
- **Grade** your previous project.
- **Q&A** for short questions about lab and lecture.

In-lab Schedule

- T.A.s' role
  - 3 T.A.s → Grade the project
  - 1 T.A. → Dedicated for Q&A.

- Schedule
  - ~ 5:00 PM: Submission
    - eTL: your source code and report
    - Hard copy: printed report
  - 5:00 ~ 5:25: Introducing next project.
  - 5:25 ~ 6:30: Grading previous project.
  - You are free to leave the room after your grading.

CPU-prototyping Projects

- Handful experiences on how to make a real CPU
  - Language: Verilog / Tool: Xilinx Vivado (any version)
  - We only check RTL simulation result.

- Contents: step-by-step
  - ALU – 1 week / Register file – 1 week
  - Vending machine – 1 week / Single cycle CPU – 1 week
  - Multi cycle CPU – 2 week / Pipelined CPU – 3 week
  - Cache – 2 week / DMA – 1 week

Project Materials & Grade

- We will provide
  - Skeleton code for each project
  - Testbench files to grade
  - Project introduction files (via pdf)
  - Project guidelines (via web)
- We will grade based on
  - Functionality using given testbench files (and more)
  - Code explanation
  - Code clarity/Code rule
  - Pop questions
  - Others…

Late Submission & Lab Absence

- Should participate all the project grading sessions
  - If not, **explanation points** will be 0.

- We will give (official) 7 more days.
  - **-10 % for each day** (up to -50 %)
  - Late will be checked based-on code upload time on eTL.
  - Make an appointment with (a) T.A.(s) after the upload.

- But submit all projects even if late. Why?
  - Cannot proceed the next project with the previous.
  - The generous T.A.s may give some points for that.

Team Organization

- **Two students** per team
  - We will let you know how to organize your group soon.

- **One student** per team
  - Can learn more in this way, so we recommend you to do so.
  - Some extra credits
  - Exact points you will get are not determined yet.
    - The professor will assign the extra credit for the letter grade.
  - This extra credit will not hurt two-per-team's grade.

Project Schedule (1/2)

	Description	Due date
3/6	Project 0 (Intro)	
3/13	Project 1 (ALU)	
3/20	Project 2 (Mealy/Moore)	Project 1 (ALU)
3/27	Project 3 (Vending)	Project 2 (Mealy/Moore)
4/3	Project 4 (Single cycle CPU)	Project 3 (Vending)
4/10	Project 5 (Multi cycle CPU)	Project 4 (Single cycle CPU)
4/17	Midterm	

* This is a tentative schedule and can be changed if necessary.

Project Schedule (2/2)

	Description	Due date
4/24	Project 6 (Pipeline)	Project 5 (Multi cycle CPU)
5/1	Q&A	
5/8	Q&A	
5/15	Project 7 (Cache)	Project 6 (Pipeline)
5/22	Buddha's Day	
5/29	Project 8 (DMA)	Project 7 (Cache)
6/5		Project 8 (DMA)
6/12	Final	

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- Thanks