Homework #2:

Due: Apr. 12 (to be collected in class)

Name:( ) SNU_ID:( )

We will grade your answers based on your understanding rather than the correctness of your answers. Therefore, we will give you credits on wrong answers as long as your story makes a good sense. Please try to do your best and just explain your answers. We would not give you credits unless we see reasonable (or required) explanations for your answers.

Please answer following questions.

Q1) Exercise 1.5 (in P&H 5E)

Q2) Exercise 1.6 (in P&H 5E)

Q3) Exercise 1.7 (in P&H 5E)

Q4) Exercise 1.9 (in P&H 5E)

Q5)

You came up with two new design choices to improve the performance of existing CPU.

- The 1st design achieves a speedup of 1.5 for 60% of execution time.
- The 2nd design achieves some greater speedup value for a different 25% of execution time.

(a) If you have to choose only one design, how much of a speedup is necessary in the 2nd design to make the 2nd design better than the 1st design?

(b) Explain Amdahl's Law. How can the outcome of (a) be explained as Amdahl's Law?

Q6)

Assume that your ISA is a load-store architecture, where only load and store instructions are allowed to access the memory as below. You now consider the impact of adding a new ADD instruction, ADDmem, to supports a new register-memory addressing mode for addition.

ADDmem R2, 100(R1) // GPR[R2] ← MEM [GPR[R1] + 100] + GPR[R2]

This instruction can replace a stream of two instructions as below.

LOAD R3, 100(R1)

ADD R2, R2, R3

However, this instruction will increase CPU's clock-cycle time by 15% without affecting CPI. If your target program run showed 26% of instructions as LOADs, what percentage of these LOADs must be replaced by ADDmem instructions to achieve at least the same performance as before?

Q7)

Exercise 4.1 (in P&H 5E)

Q8)

Exercise 4.2 (in P&H 5E)

Q9)

Exercise 4.3 (in P&H 5E)

Q10)

Exercise 4.4 (in P&H 5E)

Q11)

Exercise 4.5 (in P&H 5E)

Q12)

CPU's power consumption is a serious problem in modern computer system designs because we cannot make a faster CPU without resolving power issues. Modern CPUs (as well as any other digital sequential circuits) consume power in two different ways: (a) dynamic power and (b) static power. Dynamic power is the power consumed during transistor switching activities (e.g., computation, memory access,) whereas static power is the power consumed without doing any work (e.g., idle time.) They can be measured as following equations.

Dynamic power = k1 * (Voltage_supply^2) * Frequency // k1 is a constant
Static power = k2 * Voltage_supply * Static current // k2 is a constant
* Static current is proportional to (1/ Voltage_threshold)
* Voltage_threashold is proportional to the technology size (e.g., 90nm, 45nm)

(a) If you want to reduce the dynamic power, what will you do?

(b) If you want to reduce the static power, what will you do?

(c) If you see any contradiction between (a) and (b), what is it and why it happens? In other words, why can't we achieve both low dynamic and low static power consumption?

(d) Why do you think we can't make a faster CPU any more from the perspective of power and performance?