

Computer Organization

[Introduction to **VIVADO**]

Hunjun Lee (hunjunlee7515@snu.ac.kr), Sunghwa Lee
High Performance Computer Systems (HPCS) Lab.

March 6th, 2018

1. Go to Xilinx Website

Use below link:

<https://www.xilinx.com/support/download.html>

Downloads

📺 Installation Overview Video

📺 Doc Navigator Video (5:28)

📄 Licensing Help

Vivado

Embedded
Development

SDx Development
Environments

ISE

Device Models

CAE Vendor Libraries

Version

2017.4

2017.3

2017.2

2017.1

2016.4

Archive

Vivado General Information - 2017.4

Important Information

Using Vivado 2017.4 requires upgrading your license server tools to the Flex 11.14.1 versions listed below. Please note that this is the last release that will support Solaris operating system. Xilinx will continue to support Window and Linux operating systems.

Vivado Design Suite - HLx Editions: Update 1 - 2017.4

Important Information

Vivado Design Suite 2017.4 Update 1 is now available with support for

Production Devices

Download Includes

Last Updated

Answers

Vivado Design Suite HLx Editions (All Editions)

Feb 8, 2018

[2017.4.1 - Vivado Known Issues and Release notes](#)

2. Download Vivado HLx 2016.4: **WebPACK** and Editions

Vivado Design Suite - HLx Editions - 2016.4 Full Product Installation

Version

[2017.4](#)


[2017.3](#)


[2017.2](#)


[2017.1](#)

2016.4

[Archive](#)

 [Vivado HLx 2016.4: WebPACK and Editions - Windows Self Extracting Web Installer \(EXE - 50.44 MB\)](#)
MD5 SUM Value: 68c988206d6d17af24f2a1137a452fff

 [Vivado HLx 2016.4: WebPACK and Editions - Linux Self Extracting Web Installer \(BIN - 80.67 MB\)](#)
MD5 SUM Value: a70505f62ad81db88ab636def9951628

 [Vivado HLx 2016.4: All OS installer Single-File Download \(TAR/GZIP - 20.59 GB\)](#)
MD5 SUM Value: ffe1026646632f1a6bd1ce0d4d2e52d6

Important Information

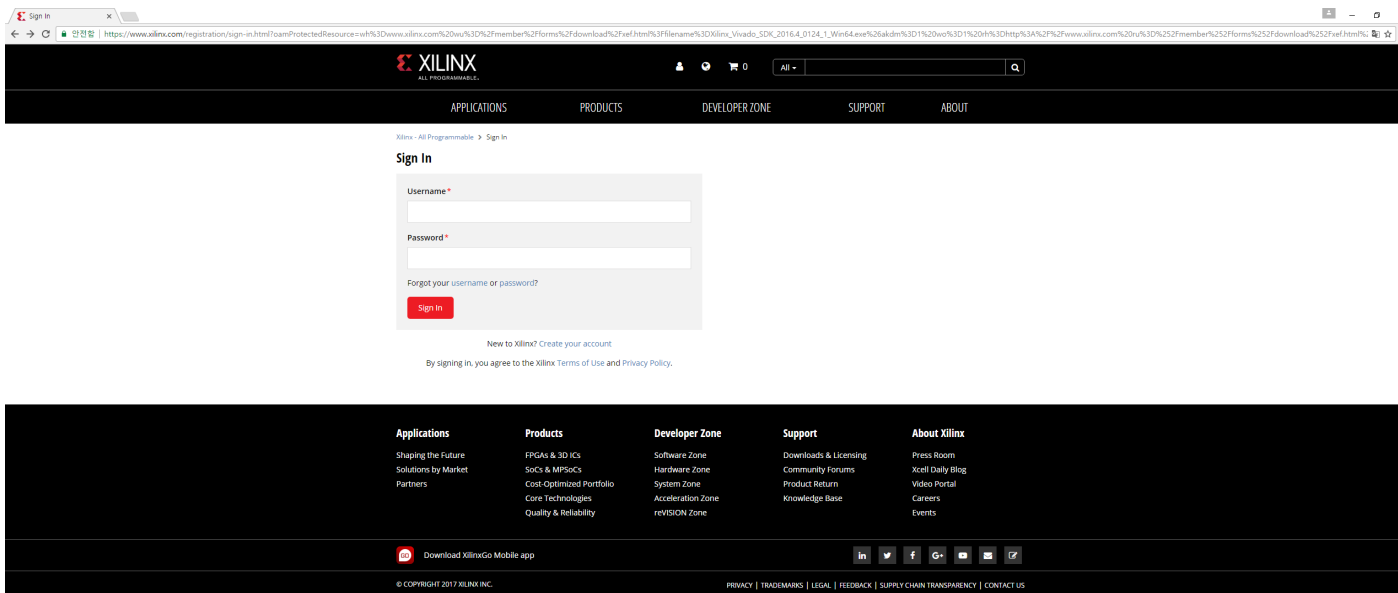
Having trouble downloading?

The download links above require the installation and use of a browser-based (plug-in) download manager. Your company's policy and/or firewall settings may not permit the download manager to be installed or operate properly. If you wish to bypass the use of the Xilinx download manager, please see [AR#68334](#).

In this guide, we assume you are using Microsoft Windows 10. You may want to use other distributions (e.g., linux), but we recommend to use Windows, because we will use Windows 10 for grading.

You may also download newer versions of WebPACK edition, but we encourage downloading the given version.

2-1. Sign in the Xilinx account. If you don't have the account, the you should create your account.



The screenshot shows the Xilinx website's sign-in page. At the top is the Xilinx logo and navigation menu. The main content area features a 'Sign In' section with fields for 'Username*' and 'Password*', a 'Sign in' button, and a link for 'Forgot your username or password?'. Below this is a link for 'New to Xilinx? Create your account' and a note about agreeing to terms. The footer contains detailed links for Applications, Products, Developer Zone, Support, and About Xilinx, along with social media icons and a copyright notice.

Sign In

Username*

Password*

Forgot your username or password?

Sign in

New to Xilinx? Create your account

By signing in, you agree to the Xilinx Terms of Use and Privacy Policy.

Applications
Shaping the Future
Solutions by Market
Partners

Products
FPGAs & 3D ICs
SoCs & MPSoCs
Cost Optimized Portfolio
Core Technologies
Quality & Reliability

Developer Zone
Software Zone
Hardware Zone
System Zone
Acceleration Zone
reVISION Zone

Support
Downloads & Licensing
Community Forums
Product Returns
Knowledge Base

About Xilinx
Press Room
Xilinx Daily Blog
Video Portal
Careers
Events

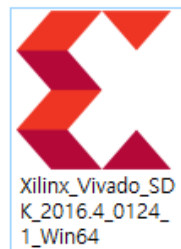
Download XilinxGo Mobile app

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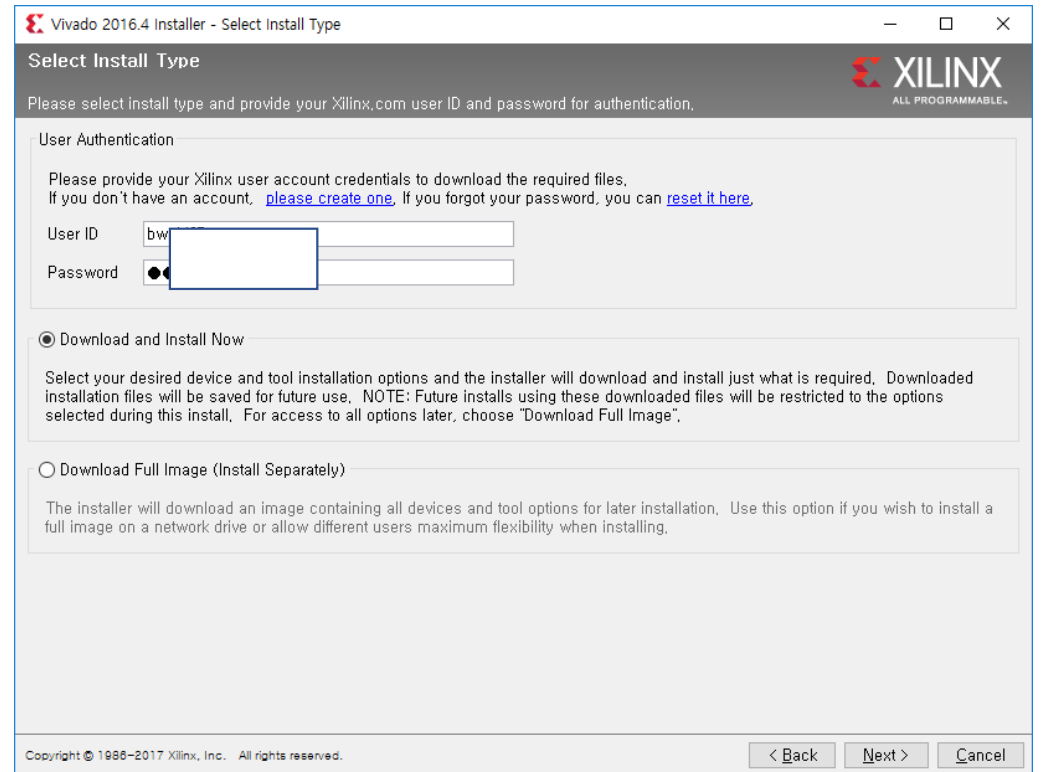
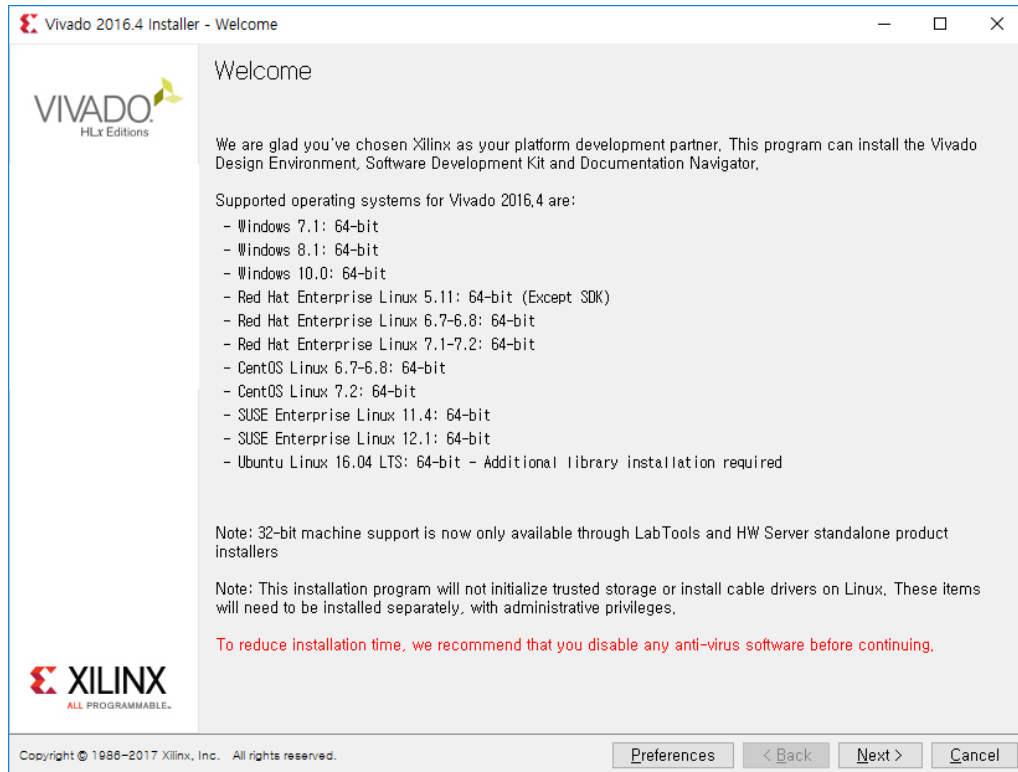
You should create account with SNU email address to get full license



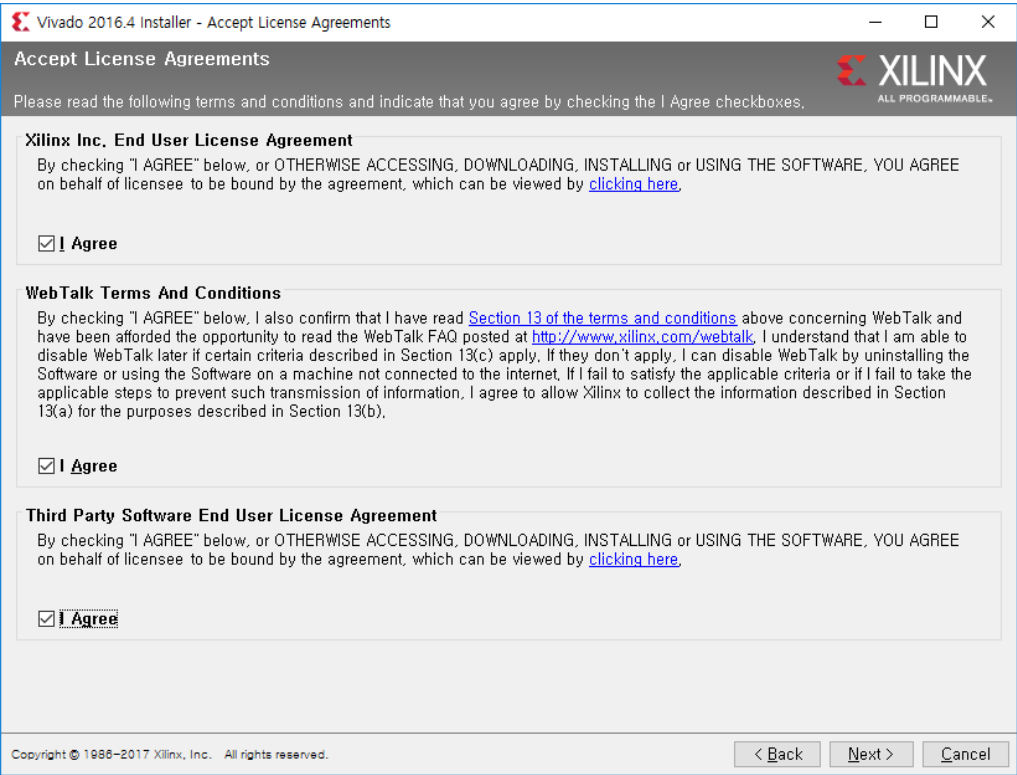
3. Execute Xilinx setup file



4. 5. Press Next



6. Check three "I Agree"s, and press next



Vivado 2016.4 Installer - Accept License Agreements

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

Xilinx Inc. End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ I Agree

WebTalk Terms And Conditions

By checking "I AGREE" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <http://www.xilinx.com/webtalk>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

☒ I Agree

Third Party Software End User License Agreement

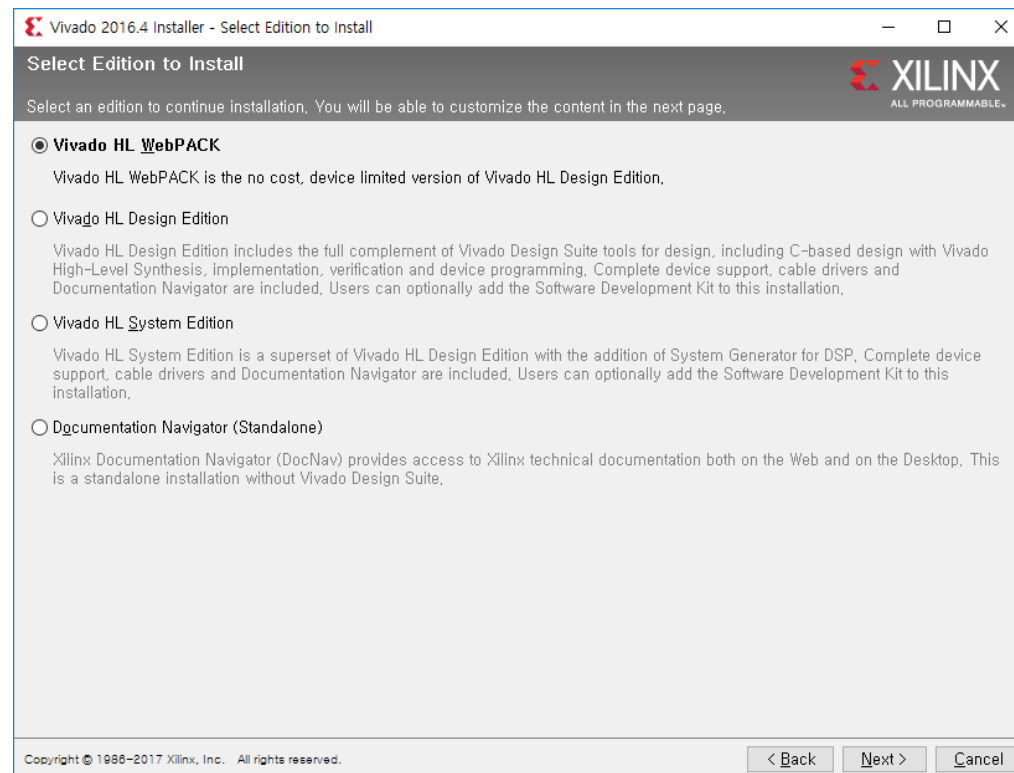
By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ I Agree

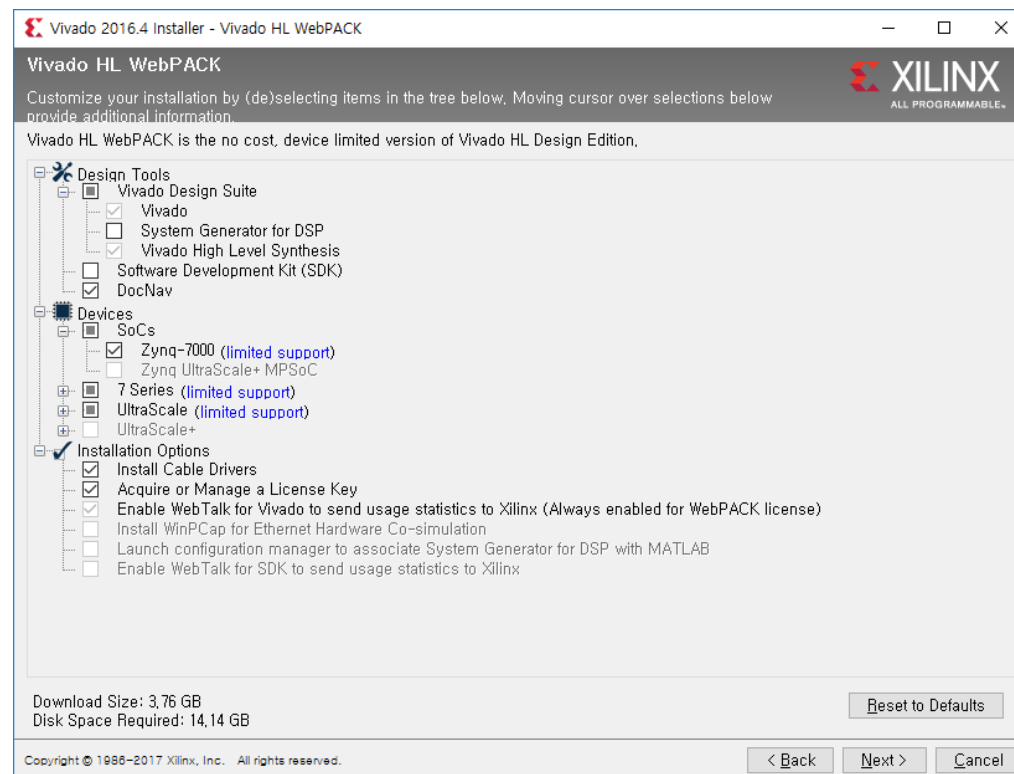
Copyright © 1986-2017 Xilinx, Inc. All rights reserved.

< Back Next > Cancel

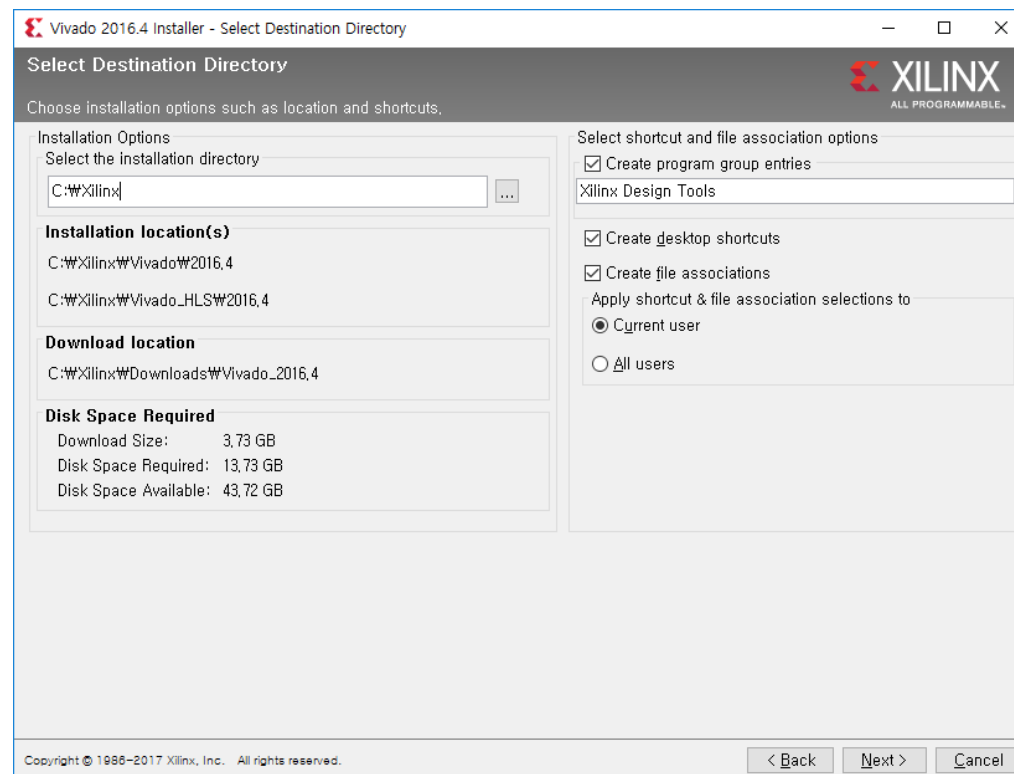
7. Choose WebPACK Edition (It's free!!)



8. Press next



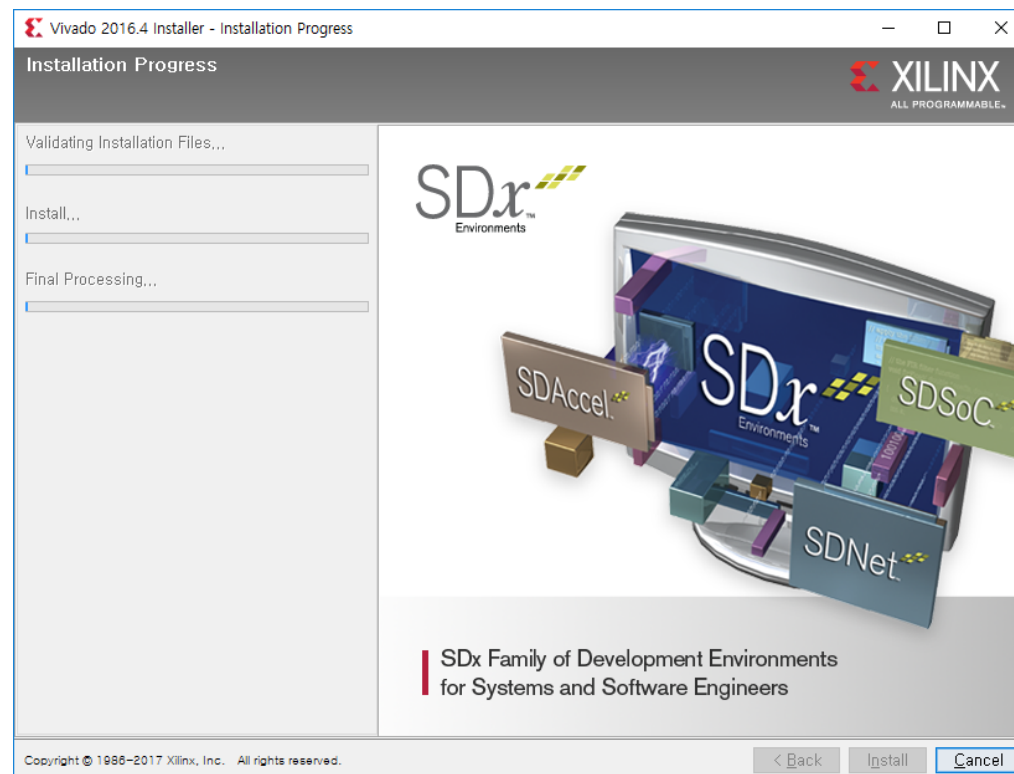
9. Press next



10. Press "Install"



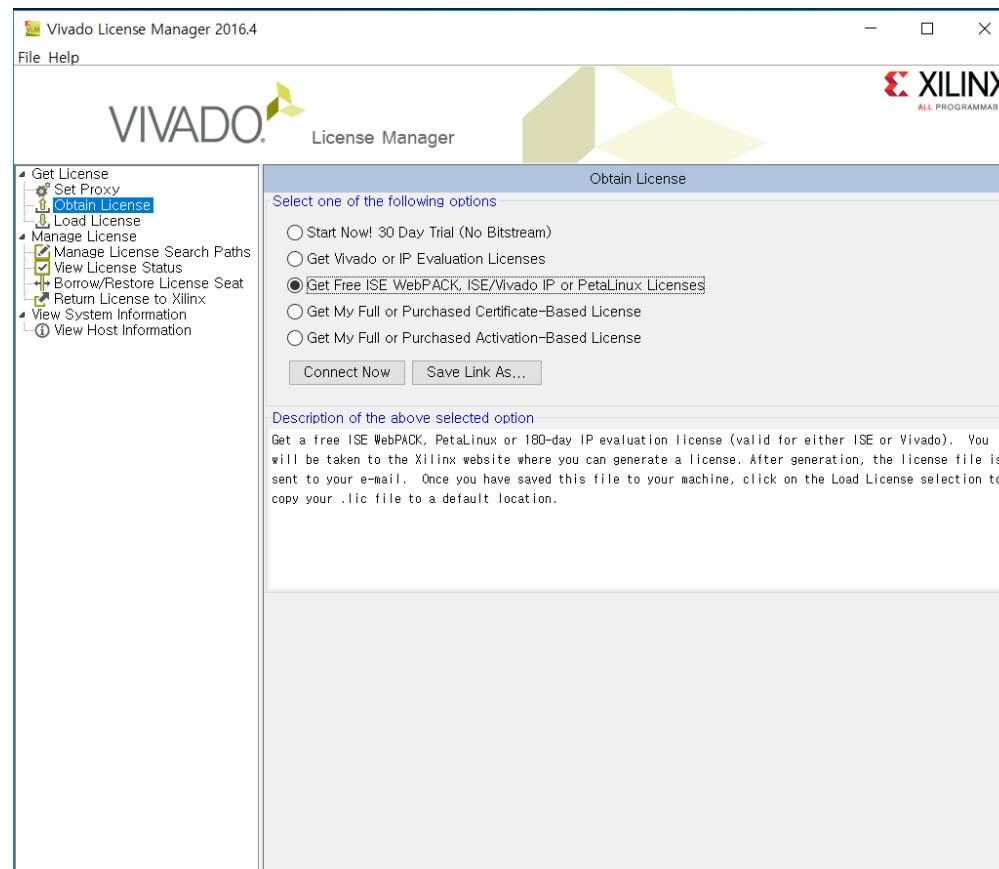
11. Wait until installing is finished.



12. Finish!



13. License Manager:
Check "Get Free ISE WebPACK ISE/Vivado or PetaLinux License",
and click "Connect Now".



You may open
License Manager manually


14. Create a Vivado WebPACK license.

[Home](#) : [Support](#) : Product Licensing


Product Licensing

Create New Licenses

Manage Licenses

 Have a Voucher to Redeem? ?
XXXX-XXXXXX-XXXX-XXXXXX
enter voucher code

Redeem Now

 Evaluation and No Charge Cores ?
Search the **Evaluation** and **No Charge** cores catalog and add specific cores to table below

Search Now

Create a New License File

Create a new license file by making your product selections from the table below.?

Certificate Based Licenses

Product	Type	License	Available Seats	Status	Subscription End Date
<input type="checkbox"/> SDSoC Environment, 60 Day Evaluation License	Certificate - Evaluation	Node	1/1	Current	60 days
<input type="checkbox"/> Model Composer : 90-day Evaluation License	Certificate - Evaluation	Node	1/1	Current	90 days
<input type="checkbox"/> Vivado Design Suite (No ISE): 30-Day Evaluation License	Certificate - Evaluation	Node	1/1	Current	30 days
<input checked="" type="checkbox"/> Vivado Design Suite: HL WebPACK 2015 and Earlier License	Certificate - No Charge	Node	1/1	Current	None
<input checked="" type="checkbox"/> ISE WebPACK License	Certificate - No Charge	Node	1/1	Current	None
<input type="checkbox"/> PetaLinux Tools License	Certificate - Evaluation	Node	1/1	Current	365 days
<input type="checkbox"/> Vivado HLS Evaluation License	Certificate - Evaluation	Node	1/1	Current	30 days

Generate Node-Locked License

Create New Licenses

Manage Licenses

Host Name	Host Type	Host ID	License Type	OS	Created By	Created Date
*	*	*	Node	*	HUNJUN LEE	03 MAR 2018

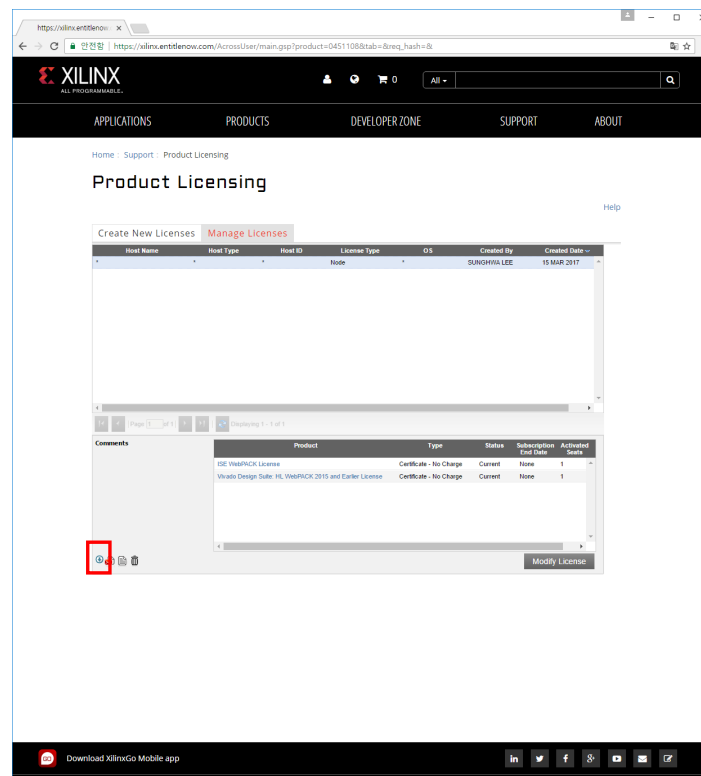
Page 1 of 1 | Displaying 1 - 1 of 1

Comments

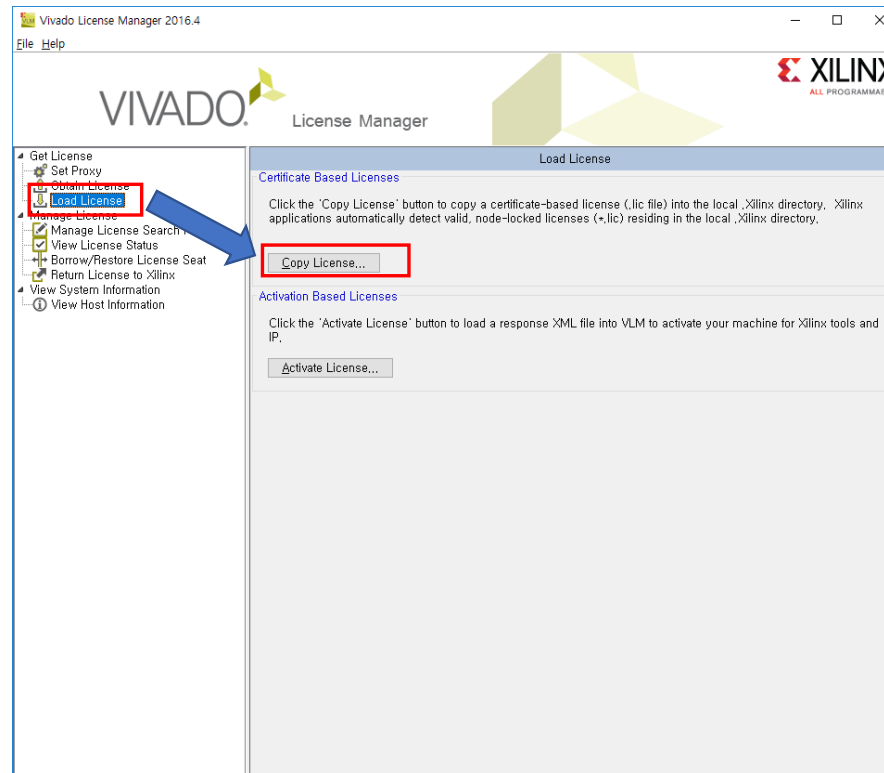
Product	Type	Status	Subscription End Date	Activated Seats
Vivado Design Suite: HL WebPACK 2015 and Earlier License	Certificate - No Charge	Current	None	1
ISE WebPACK License	Certificate - No Charge	Current	None	1

Modify License

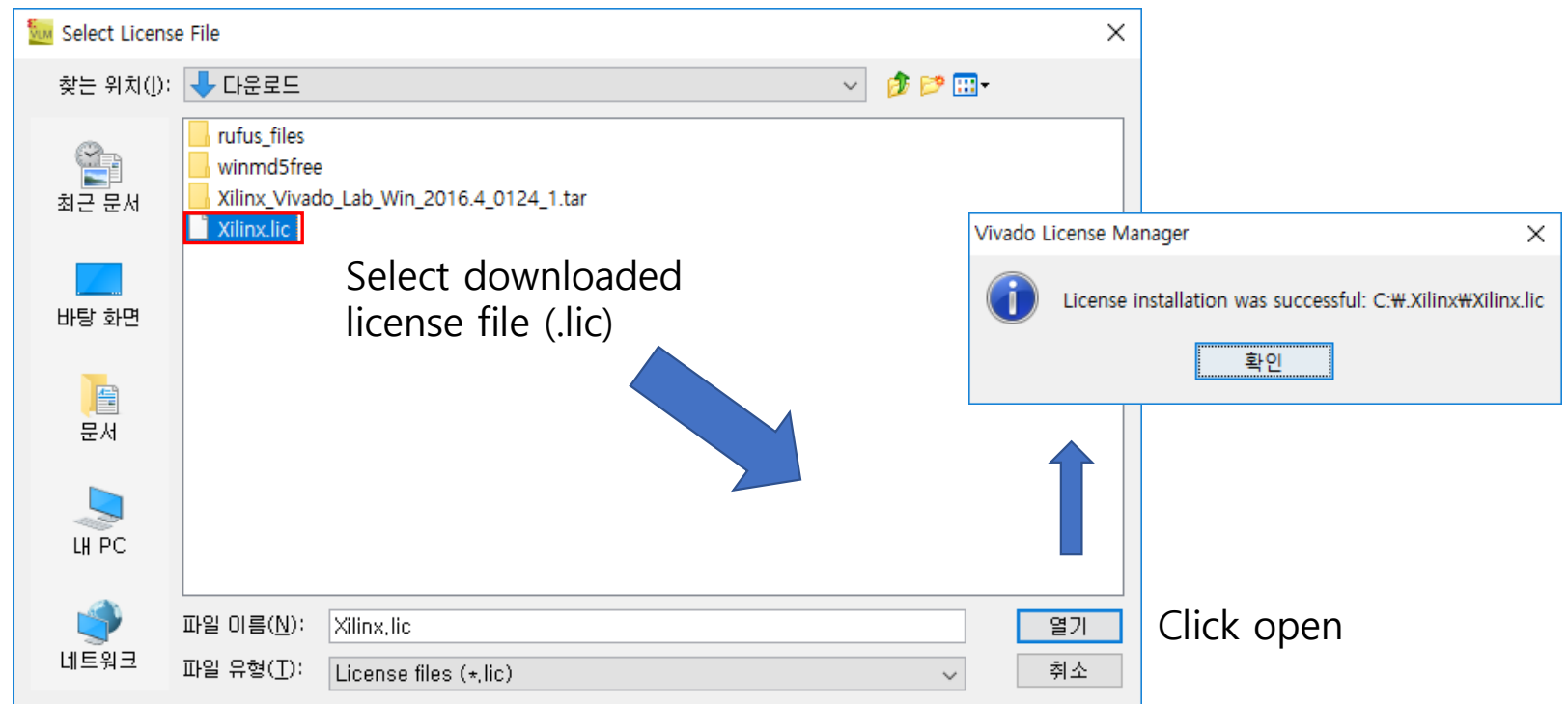
15. Select licenses and Download it



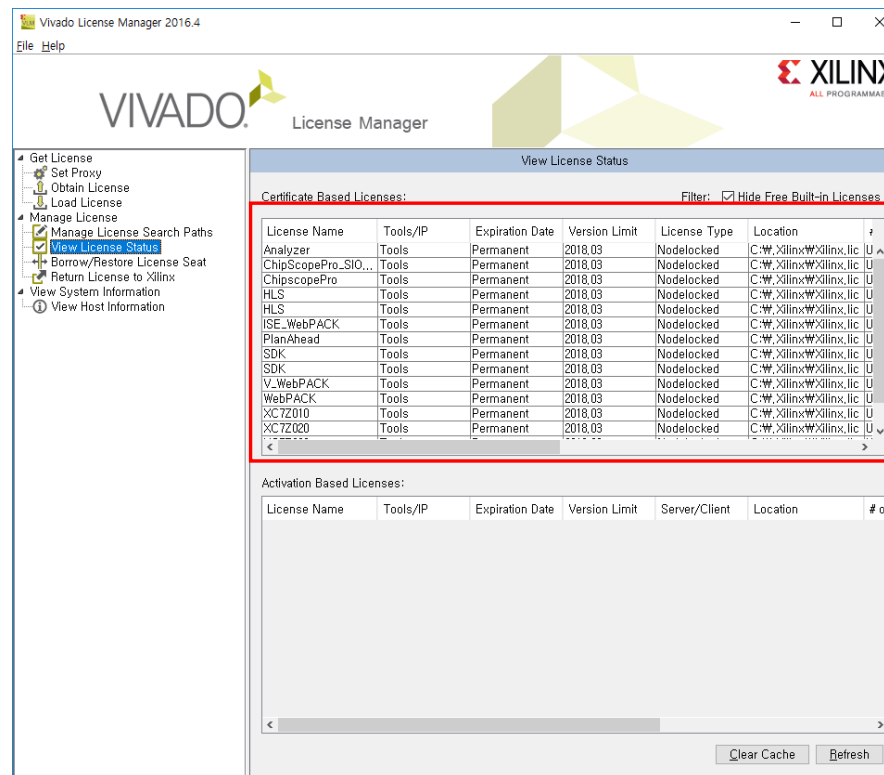
16. Load License



17. Copy License



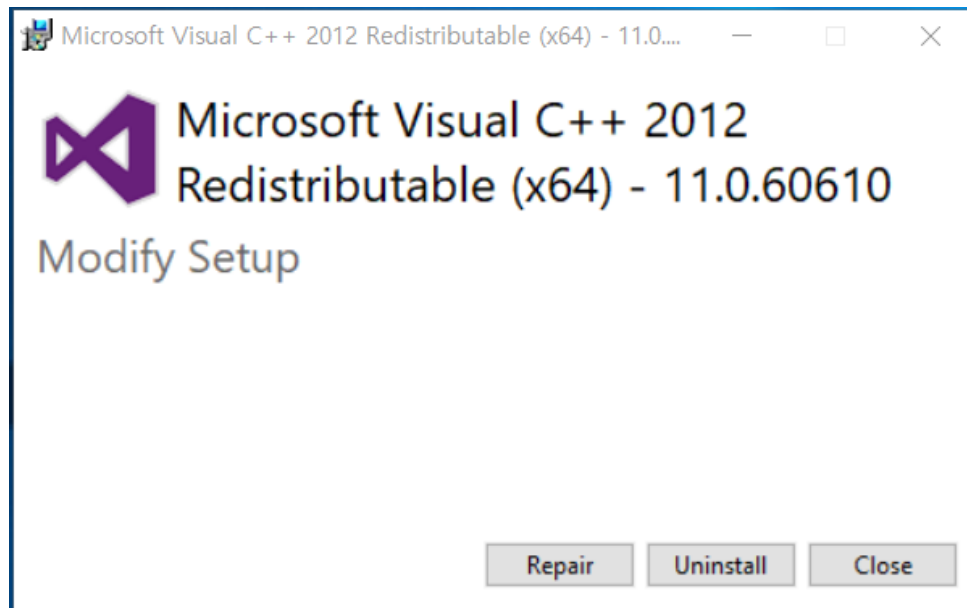
18. Check License Status (FINISH)



TroubleShooting

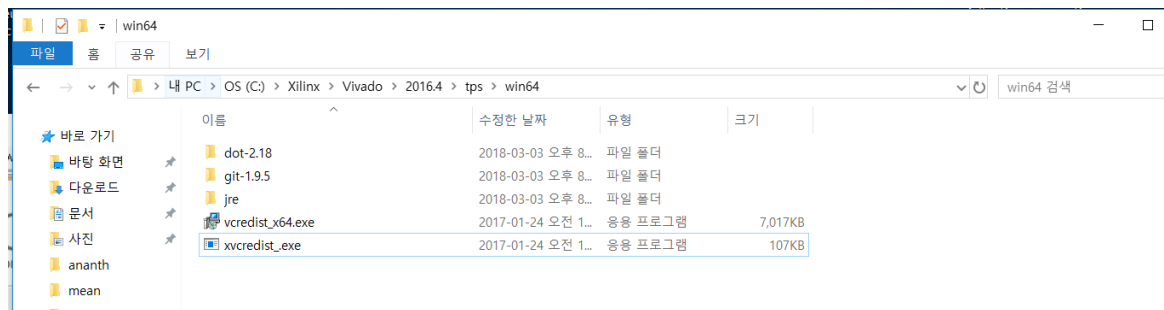
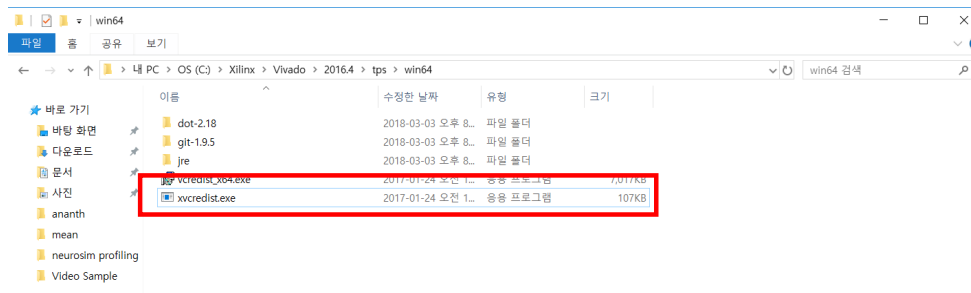
1. Visual C++ 2012 modify setup problem

In some situations, Visual C++ 2012 Redistributable problem occurs after executing Vivado



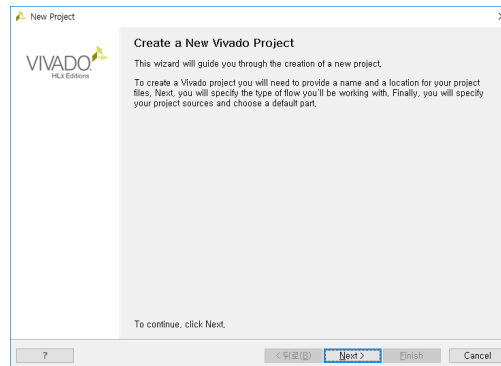
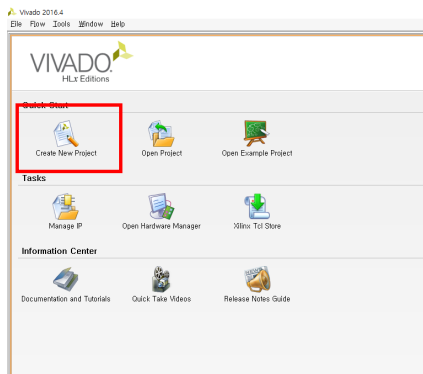
2. Visual C++ 2012 modify setup problem

Change C:/Xilinx/Vivado/<version.no>/tps/win64/xvcredist.exe to C:/Xilinx/Vivado/<version.no>/tps/win64/xvcredist_.exe

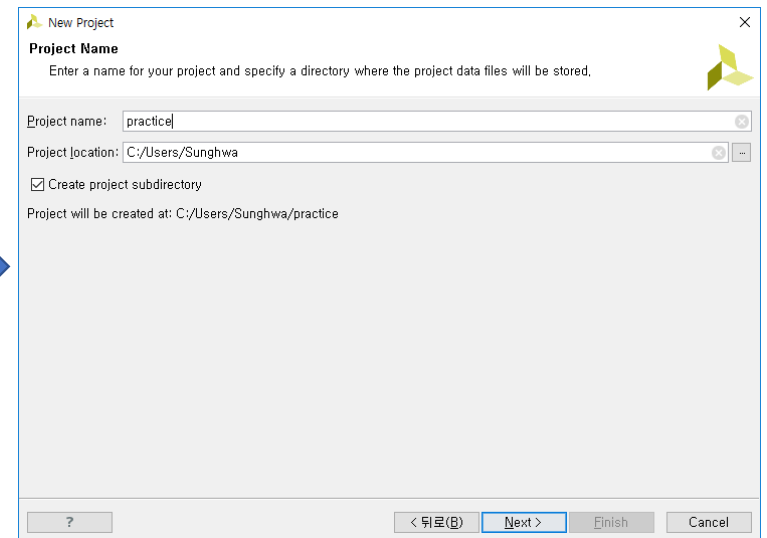


How to make a project

1. Run Vivado and create new project

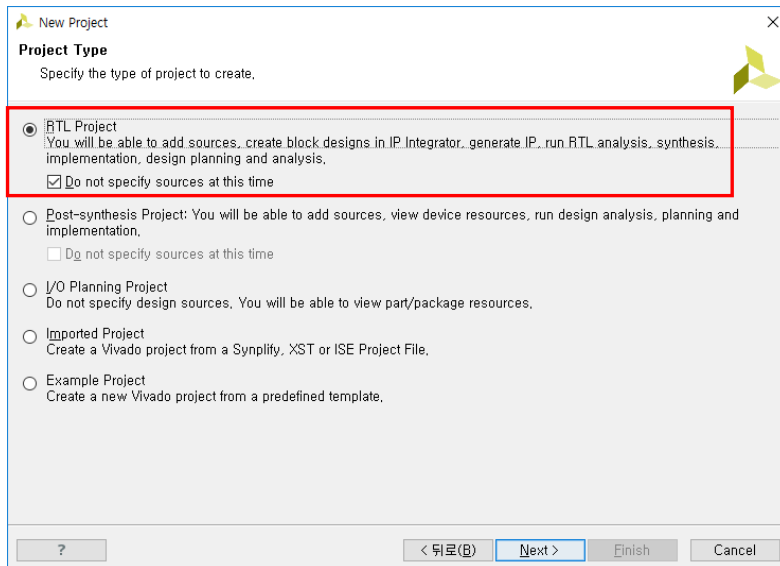


Click Next

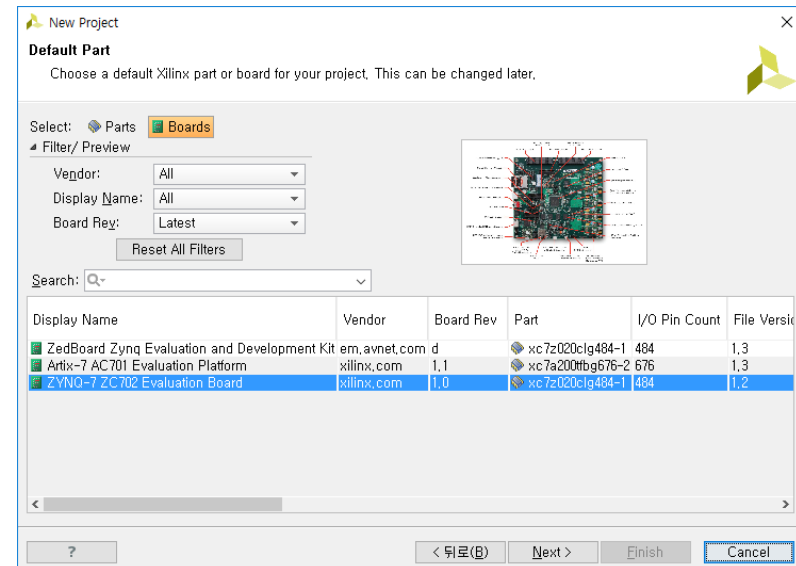


Enter a project name

2. Create a new project



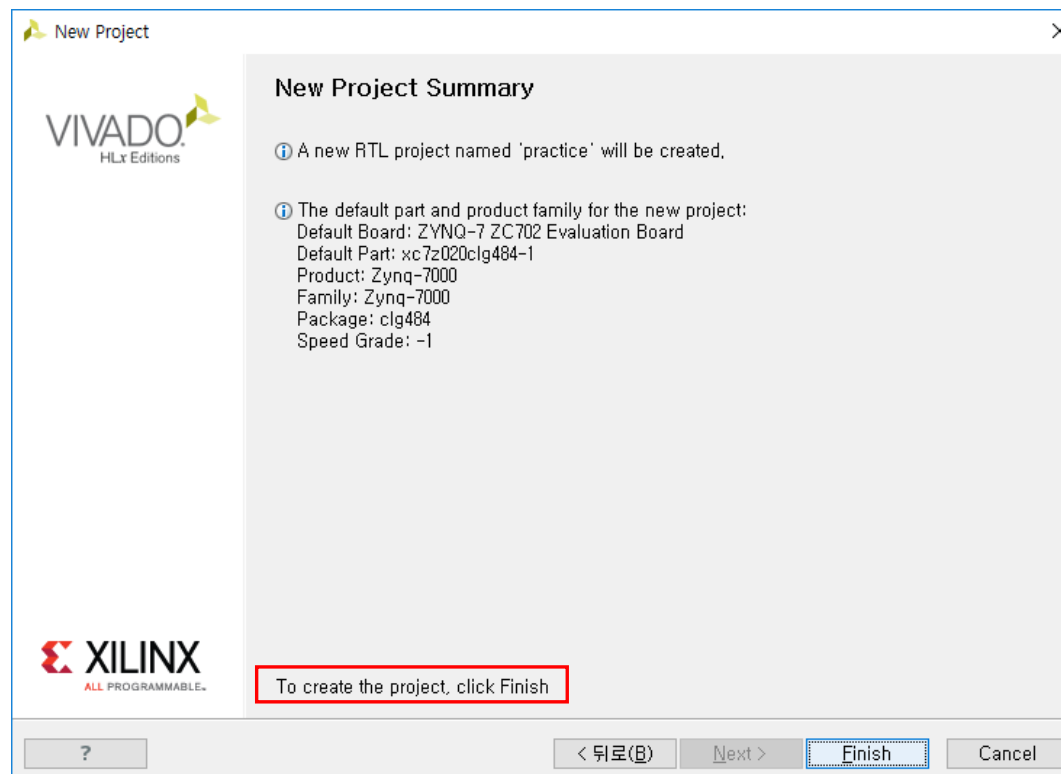
Choose RTL Project



Choose Parts/Boards

- We don't use any boards in this course, so just ignore this part and press next.

3. Create a new project



Simple Verilog Tutorial using Vivado

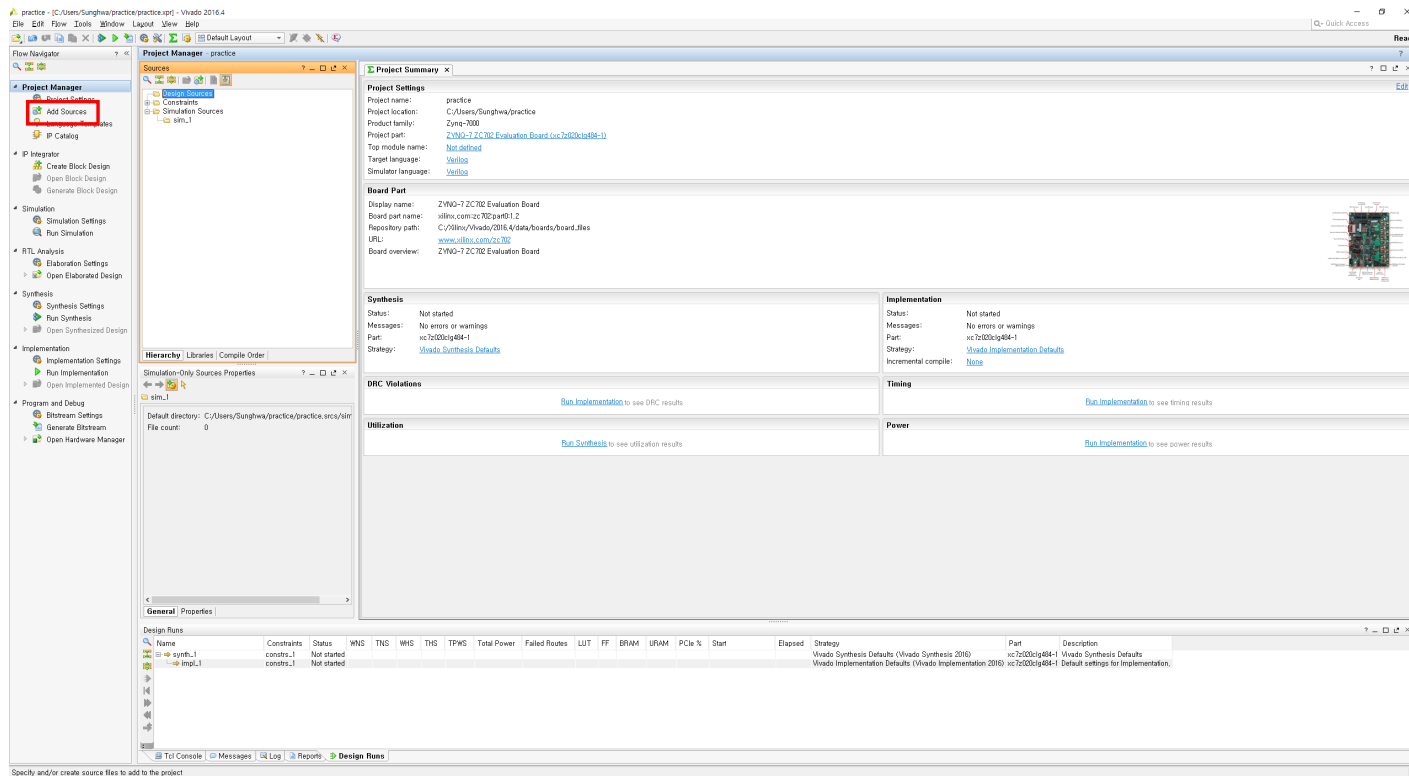
Counter

- 4-bit synchronous up-counter
- That is, the counter is incremented when the clock signal is positive edge.

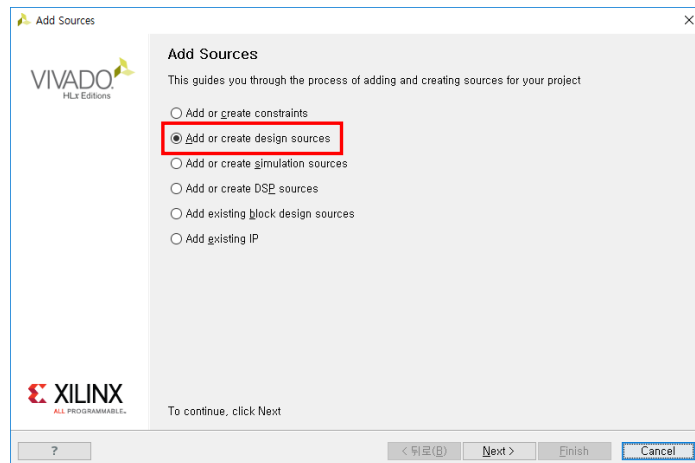


1. Add Design Sources

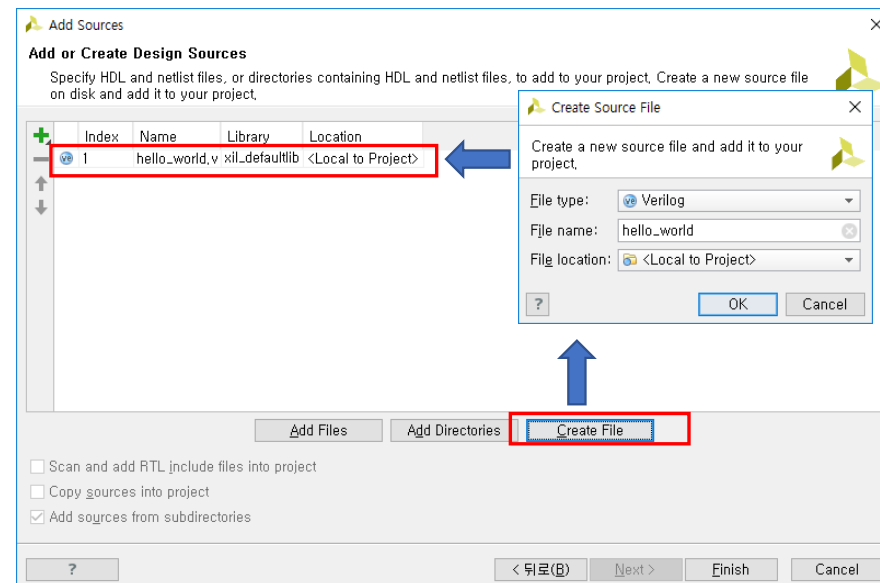
Click
Add Sources



2. Add Design Sources



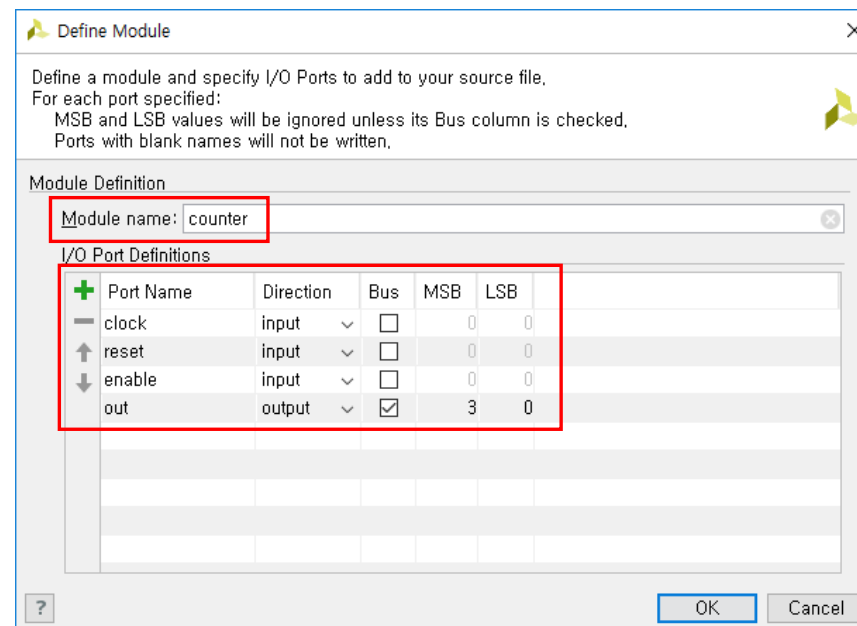
To continue, click Next



1. Click Create File
2. Enter file name ("hello_world")
3. Click Finish

3. Add Design Sources

- Change module name and enter I/O Port Definitions



The image shows a 'Define Module' dialog box with a title bar containing a yellow triangle icon and a close button. The main text area contains instructions: 'Define a module and specify I/O Ports to add to your source file. For each port specified: MSB and LSB values will be ignored unless its Bus column is checked. Ports with blank names will not be written.' Below this is the 'Module Definition' section with a text field for 'Module name' containing the word 'counter'. Underneath is the 'I/O Port Definitions' section, which contains a table with columns: Port Name, Direction, Bus, MSB, and LSB. The table has four rows: 'clock' (input, unchecked), 'reset' (input, unchecked), 'enable' (input, unchecked), and 'out' (output, checked). The first three rows have MSB and LSB values of 0, while the 'out' row has MSB 3 and LSB 0. A red rectangle highlights the 'out' row and its corresponding MSB and LSB values. At the bottom of the dialog are buttons for '?', 'OK', and 'Cancel'.

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: counter

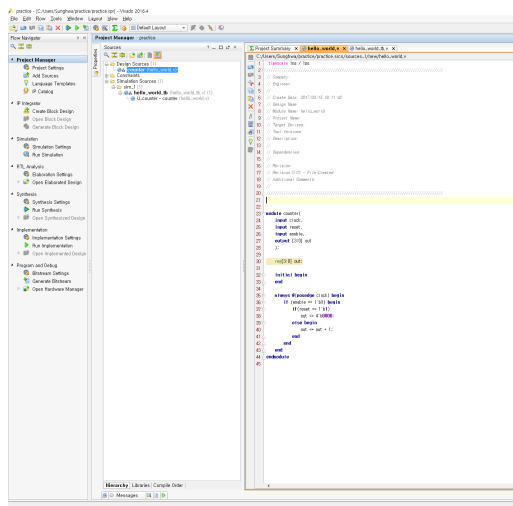
I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
clock	input	<input type="checkbox"/>	0	0
reset	input	<input type="checkbox"/>	0	0
enable	input	<input type="checkbox"/>	0	0
out	output	<input checked="" type="checkbox"/>	3	0

OK Cancel

4. Write code

(* Copy this code and paste it *)



```
`timescale 1ns / 100ps
```

```
module counter (input clock, input reset, input enable, output [3:0] out);  
    reg [3:0] out;
```

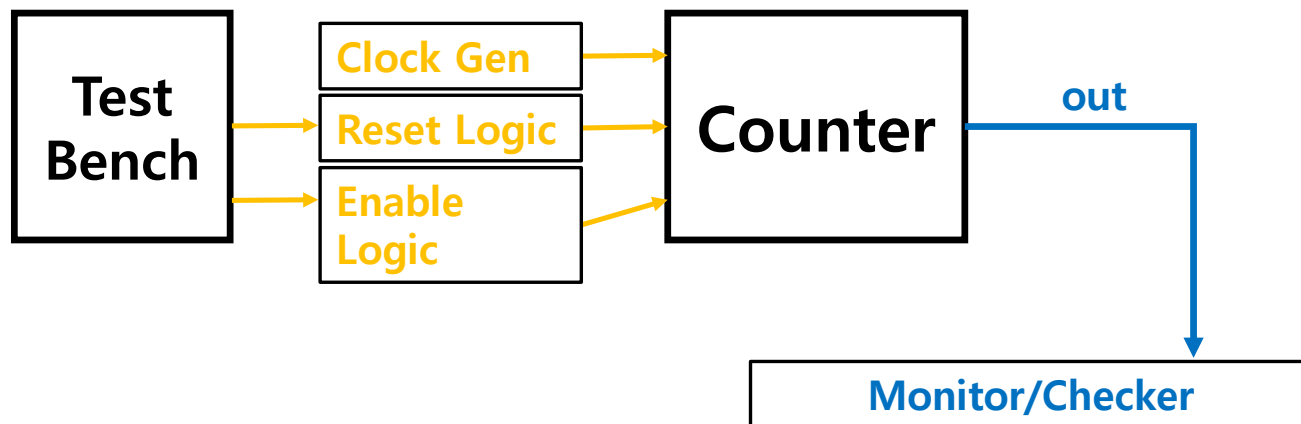
```
    initial begin  
        end
```

```
    always @(posedge clock) begin  
        if (enable == 1'b1) begin  
            if (reset == 1'b1)  
                out <= 4'b0000;  
            else begin  
                out <= out+1;  
            end  
        end
```

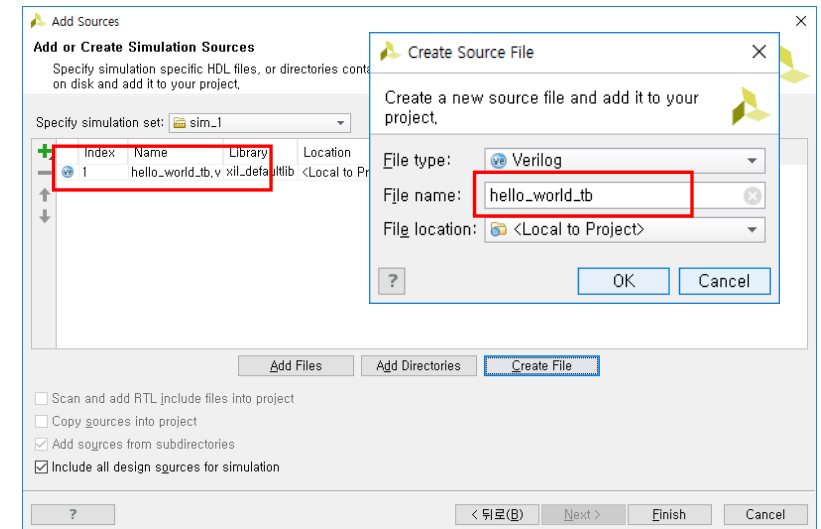
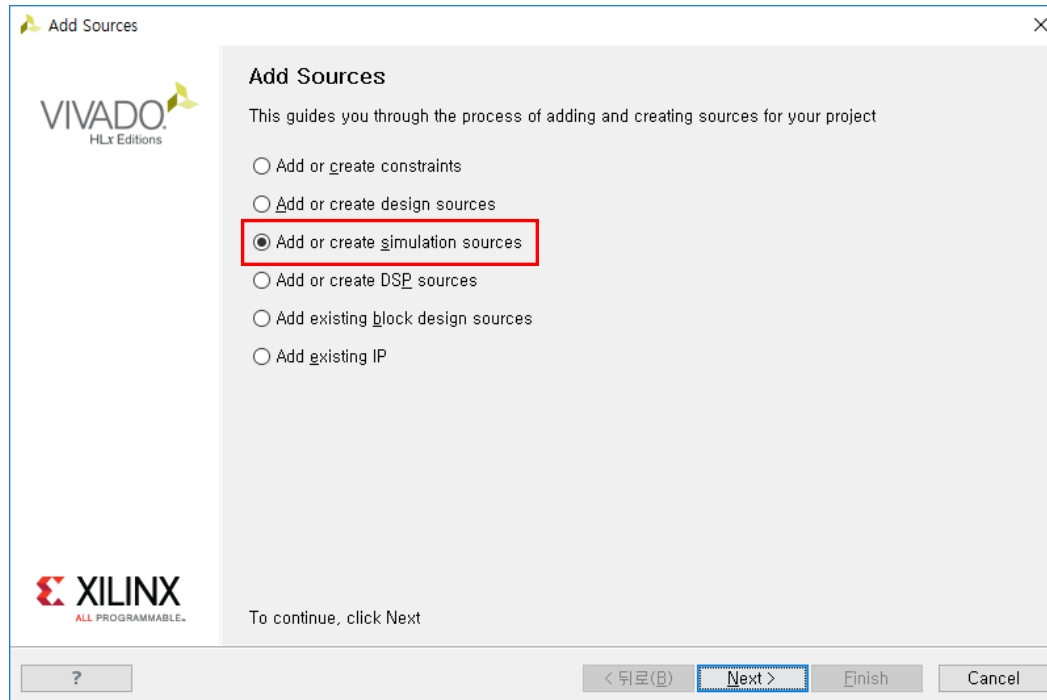
```
    end  
endmodule
```


5. Write down your testbench

- To test the counter, a testbench file is needed.

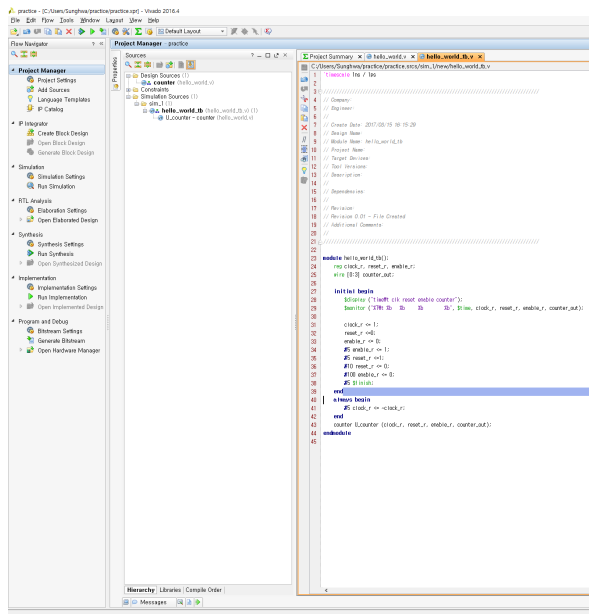


6. Add a testbench source (Click add sources)



7. Write code

(* Copy this code and paste it *)



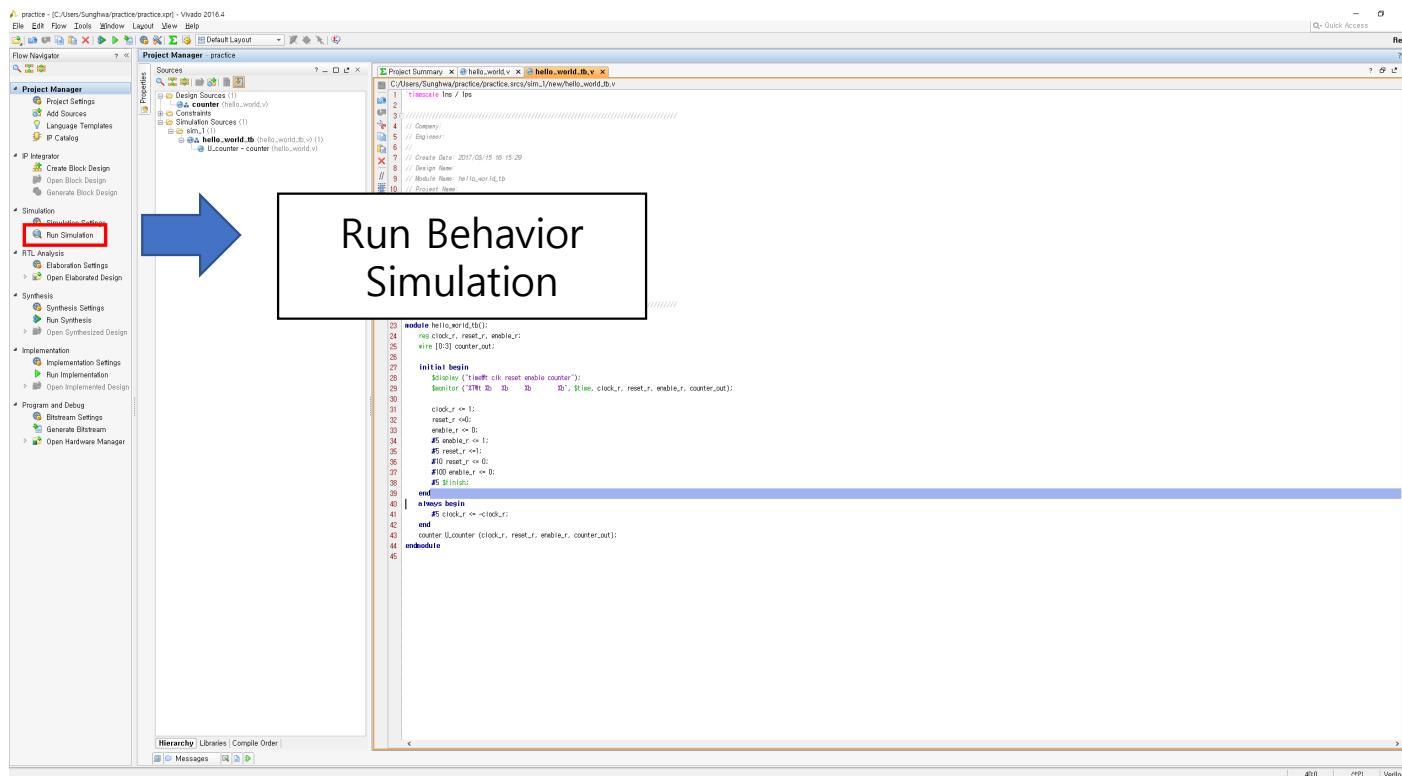
```
module hello_world_tb();
    reg clock_r, reset_r, enable_r;
    wire [3:0] counter_out;

    initial begin
        $display ("time\t clk reset enable counter");
        $monitor ("%T\t %b %b %b %b", $time, clock_r,
reset_r, enable_r, counter_out);

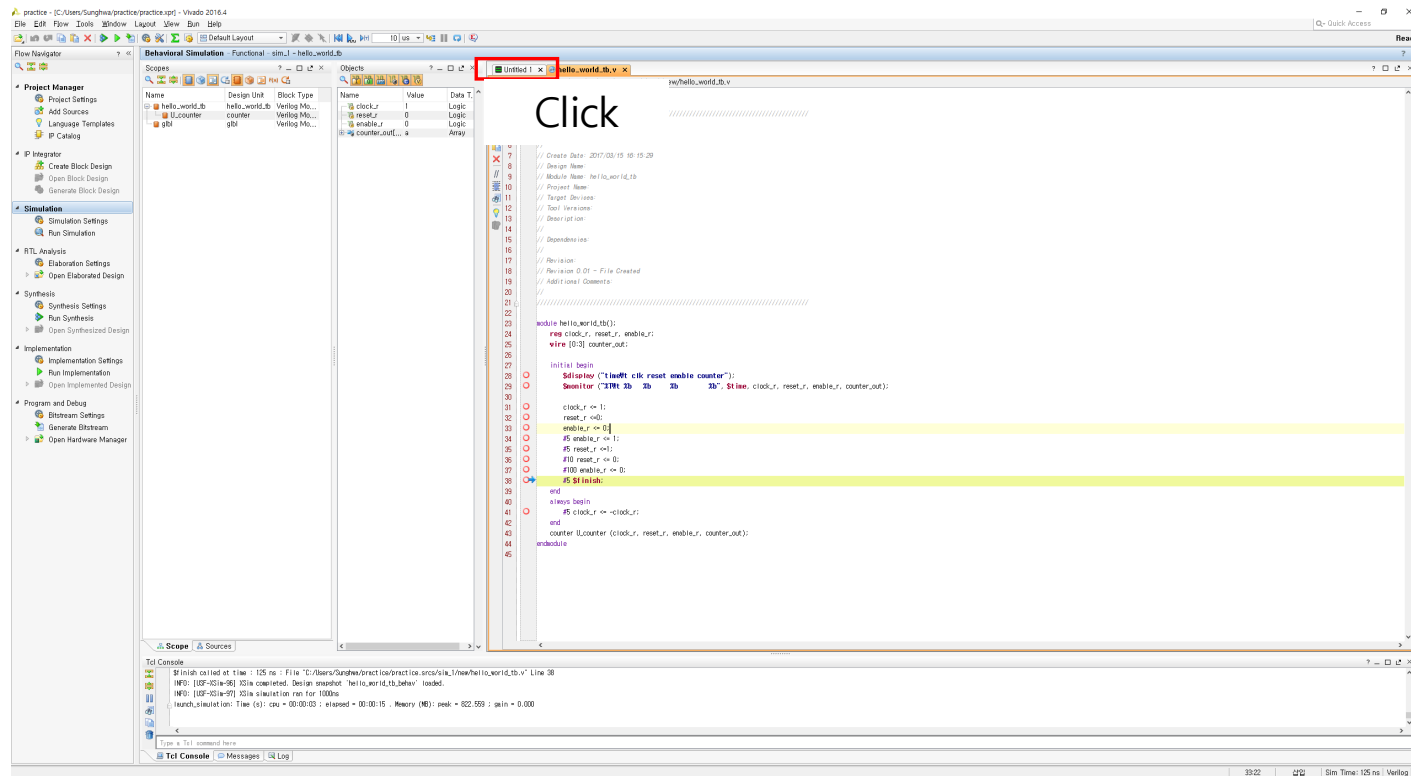
        clock_r <= 1;
        reset_r <= 0;
        enable_r <= 0;
        #5 enable_r <= 1;
        #5 reset_r <= 1;
        #10 reset_r <= 0;
        #100 enable_r <= 0;
        #5 $finish;

    end
    always begin
        #5 clock_r <= ~clock_r;
    end
    counter U_counter (clock_r, reset_r, enable_r, counter_out);
endmodule
```

8. Run Simulation!



9. Run simulation



10. Check the result

