Isolated AC-DC Power Supply with PFC

Team Members:
Colby Young
Ahmed Fahmy

Prepared For:
EEE 572 Advanced Power Electronics

Dec 2, 2023

Overview **3**
Requirements and Specifications **4**
Design Comparisons **4**
System Overview **5**
Boost PFC **5**
Circuit Design 5
Capacitor Selection 6
Inductor Design 6
Boost diode Selection 6
Mosfet Selection 6
Rectifier Bridge Design 6
Boost PFC Control 6
Current loop controller 7
Voltage loop controller 7
Simulation Results 8
Isolated Flyback DC-DC Converter **11**
Circuit Design 11
Inductor Selection 11
Capacitor Selection 11
Diode Selection 11
MOSFET Selection 11
Controller design 12
Plecs Small Signal Analysis 13
Schematic 13
Simulation Result 14
Conclusion 15

Overview

The goal of this project is to develop a system that will efficiently convert alternating current (AC) to direct current (DC). This could be used in a variety of industrial applications such as data centers, factory automation controls, and other high-voltage industries. Common voltages for Industrial facilities in North America include: 208V, 240V, and 480V. This is why having a wide input voltage range is necessary. Having a system that can be powered directly from mains voltage reduces components and wiring on the system level designs.

Industrial power systems face various challenges when it comes to building a reliable and efficient design. Some common challenges include voltage fluctuations, frequency variation, low power factor, overloading, environmental factors, and more. Having a good design can help mediate a lot of these challenges. For voltage fluctuations, input voltage protection can be incorporated into the design to protect the devices from unsafe voltage that could harm the electronics. For designs where frequency variation is common, a phase-locked loop (PLL) could be used to compare the input frequency with a known reference and make adjustments accordingly. As technology advances more and more effort is dedicated to making electrical systems highly efficient. In this case having a high power factor is desirable for having a system that has very low power loss. Lastly, it is important for these applications to have isolation from input to output. Having isolation helps eliminate noise from either input or output from reaching the other side. It also helps reduce EMI and other interference which is important when working with sensitive electronics commonly found in DC applications.

In this report we will examine different topologies used in creating AC/DC converters and compare them to decide which is better for our application. While examining our system design we will also decide on which method is best for solving the various challenges listed above.

Requirements and Specifications

- Input -
  - Voltage Range: 200-500VAC
  - Voltage Nominal: 480VAC
  - Frequency Range: 50-60Hz
  - Current: ~0.5 Amps @max output current

- Output -
  - Voltage: 24VDC
  - Current: 10 Amps
  - Rated Power: 240 Watts
  - Current Ripple (max): 10% @max current
  - Voltage Ripple (max): 5% @max current

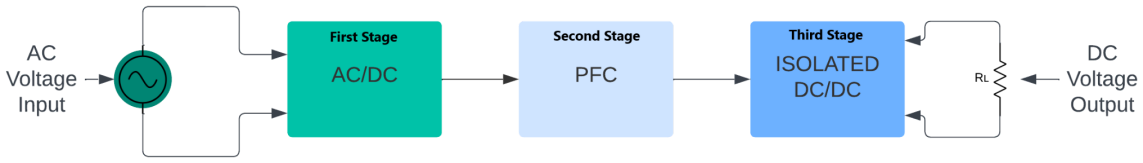
- Protection -
  - Short Circuit and Overload
  - Under/Over Voltage
  - Over Temperature

- Features -
  - Power Factor Correction
  - Isolated Output
  - Low THD

Design Comparisons

TOPOLOGY	POWER RANGE HISTORICALLY USED	TRANSFORMER UTILIZATION	NO. OF ACTIVE SWITCHES	VOLTAGE STRESS ON THE ACTIVE SWITCH	COST
Flyback	< 100W	Single Ended	1	>Vin+N X Vout	Lowest
Forward	50W – 200W	Single Ended	1	>Vin X 2 (For Dmax=0.5)	> Flyback
Active Clamp Forward (ACF)	50W – 300W	Double Ended	2	Vin / (1-D)	Flyback < ACF < Forward
Push-Pull (P-P)	100W – 500W	Double Ended	2	>Vin X 2	> ACF
Half-Bridge	100W – 500W	Double Ended	2	>=Vin / 2	> P-P
Full-Bridge	> 500W	Double Ended	4	>=Vin	> Half-Bridge

System Overview



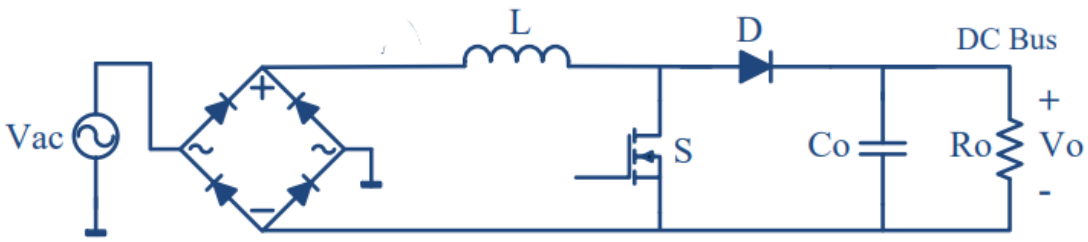
The system design can be divided into 3 different levels; AC to DC rectification,power factor correction and DC-DC isolated conversion. Diode bridge rectifier will be used for conversion from AC to DC. PFC circuit is needed to be able to follow the requirements stated above without the need for bulky filters. For the isolated converter the flyback topology was used due to its low cost and the low power required from the converter.

The below chapters discuss the design, analysis and simulation of each level of the system focusing on achieving the requirements through the appropriate control. Then the 3 levels are integrated and the integration challenges are discussed below. All simulations are done using PLECS software.

Boost PFC

Passive filters for bridge rectifiers usually do not guarantee the required power factor and harmonics requirements and standards and also they are bulky. Thus, the need for power factor correction. There are different power factor correction topologies that can be used, the most common is the boost PFC topology. The boost PFC is the most common due to several factors; it can support universal voltages (120-240)V. More benefits are the high switching frequencies (>100khz) and the high power factor (up to 99%) and the low THD (<3%) that it can achieve.

The circuit is as the below figure, it consists of a bridge rectifier and a PFC based boost converter. The input of the circuit is the AC mains which can be 120-240V and 50-60hz. The output of the boost PFC is then connected to another isolated converter for stepping down and isolating the load.



Circuit Design

$V_0 > 240\sqrt{2}$ V

Let $V_0 = 350$ V

Maximum output Voltage ripple is 10%

Maximum inductor current ripple is 10%

AC Input frequency = 50 - 60 hz

$f_s = 200Khz$

$I_{o,max} = 0.7A$ (From converter design)

Capacitor Selection

$$C_o = \frac{P_{max}}{V_0 \omega} \frac{1}{V_{o_{ripple\ pk-pk}}}$$

Where P_{max} = 250W (larger than the converter's power as a safety margin)

$$C_o = 13\ \mu f$$

$$Capacitor\ Voltage\ rating\ = V_o = 350V$$

$$ESR < \frac{\Delta V_o}{\Delta I_{C_{o\ max}}} = \frac{\Delta V_o}{I_{in_{pk}}} = 11.57\Omega$$

Inductor Design

$$L_{in} = \frac{V_o}{4 f_s \Delta I_{in_{max}}} = 3.04mH$$

Where $I_{in} = \frac{I_{o,max}}{1-D_{max}} = 1.44A$ & $D_{max} = 1 - \frac{V_{in,min}}{1-D_{max}} = 0.514$

$$I_{L,pk} = I_{in,max} + \frac{\Delta I_l}{2} = 1.512A$$

$$I_{L,RMS} = \sqrt{I_{in,max}^{\ 2} + \frac{\Delta I_L^{\ 2}}{12}} = 1.44A$$

$$DC\ bias\colon\ I_{in,max} = \frac{I_{o,max}}{1-D_{max}} = 1.44A$$

Boost diode Selection

$$Voltage\ rating\ = V_o = 350V$$

$$Peak\ Current\ = i_{D,pk} = I_{L,pk} = 1.512A$$

$$Average\ Current\ = i_{D,avg} = I_{o,max} = 0.7\text{A}$$

Mosfet Selection

$$Voltage\ rating\ = V_o = 350V$$

$$Peak\ Current\ = i_{sw,pk} = I_{L,pk} = 1.512A$$

$$RMS\ Current\ = i_{sw,RMS} = I_{in,max}\sqrt{D_{max}} = 1.03A$$

Rectifier Bridge Design

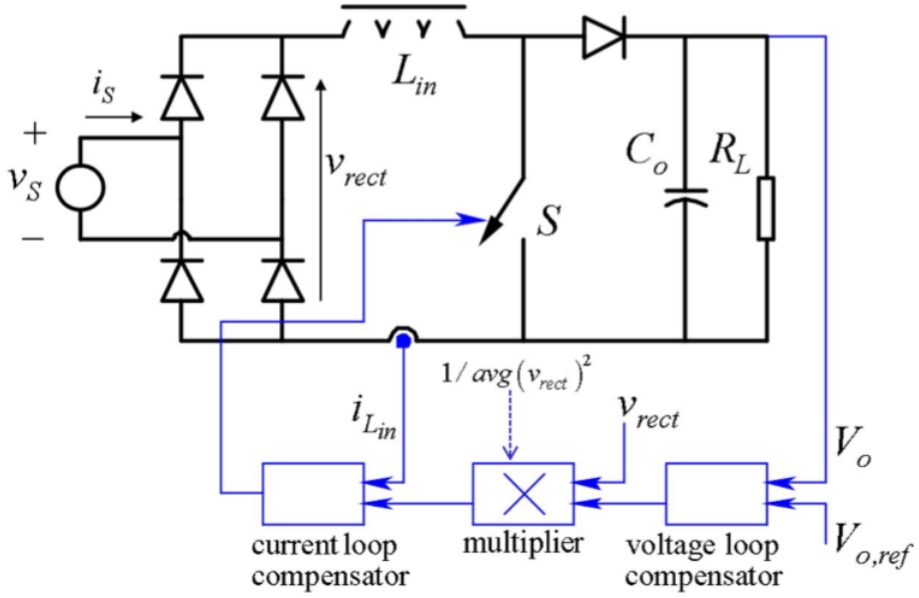
$$I_{avg} = \frac{2\sqrt{2}P_o}{\pi V_{ac,min}} = 1.87A$$

$$P_{bridge} = 2 I_{avg} V_{f,bridge}$$

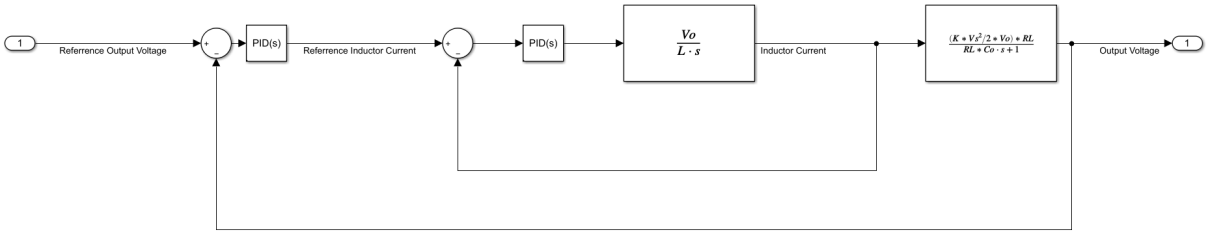
Where $V_{f,bridge} = 1V$ and it is the bridge diode forward voltage drop

Boost PFC Control

The boost PFC is controlled by controlling the output voltage to have a constant voltage and the inductor current is controlled to improve the power factor. The figure below explains the control of the boost PFC where there are two loops; the current control loop (The fast loop) and the voltage control loop (The slow loop). The feedforward is neglected for the design in this document.



The 2 controllers are designed based on K-factor controllers which is a loop shaping control technique that is widely used in DC-DC converters. The current loop controller bandwidth is 20Khz (10 times less than the switching frequency) and the voltage controller bandwidth is 50hz (10 times less than twice the fundamental frequency). The block diagram below shows the transfer functions of the current and voltage loops which are used to design the controllers. Both controllers are type 2 K-factor controllers with desired phase margin of 60 degrees and are designed as per the below equations.



Current loop controller

Type 2 K-factor controller:

$$G_C(S) = \frac{K_C}{S}\frac{(1+\frac{S}{w_z})}{(1+\frac{S}{w_p})}$$

Current loop transfer function:

$$G_P(S) = \frac{i_L(S)}{d(S)} = \frac{V_o}{SL} = \frac{115131.6}{S}$$

Where, bandwidth = 20 Khz and required phase margin = 60 degrees.
The controller transfer function will be as the following:

$$G_C(S) = \frac{36779.5}{S}\frac{(1+\frac{S}{33671.5})}{(1+\frac{S}{468725.6})}$$

Voltage loop controller

Type 2 K-factor controller:

$$G_C(S) = \frac{K_C}{S}\frac{(1+\frac{S}{w_z})}{(1+\frac{S}{w_p})}$$

Voltage loop transfer function:

$$G_P(S) = \frac{v_o(S)}{v_{o_c}(S)} = \frac{KV_s^2}{2V_o}\frac{R_L}{1+SR_LC_o} = \frac{84256.56}{1+0.066S}$$

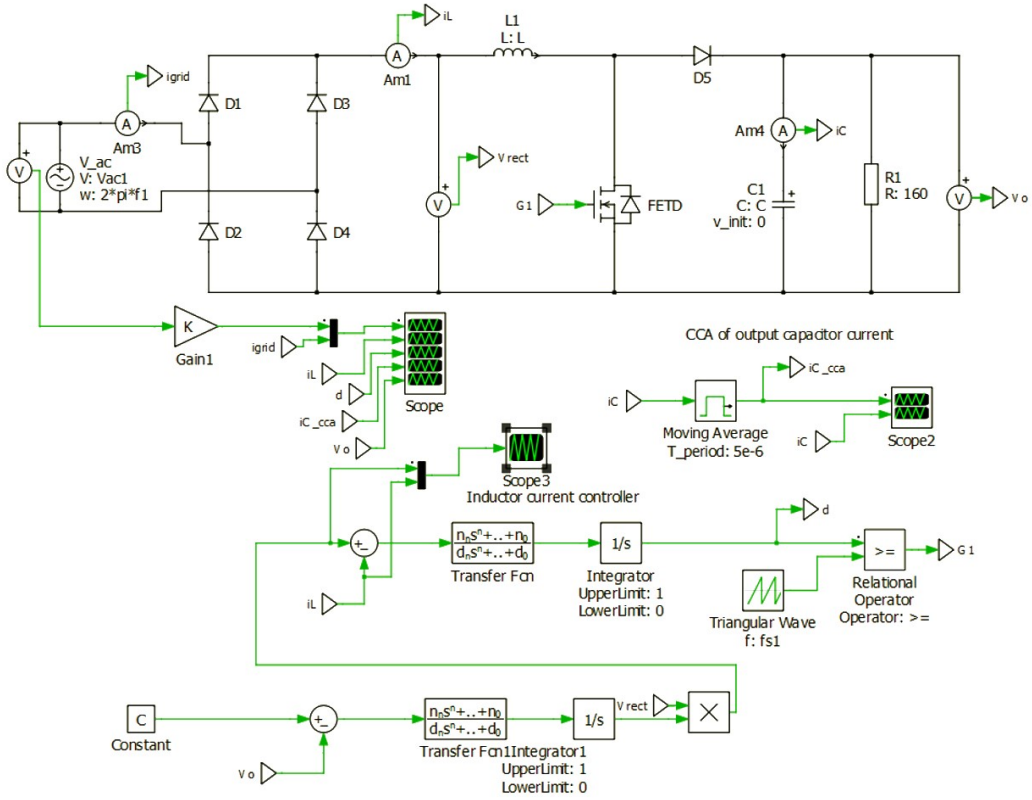
Where; K=1, $R_L = \frac{P_o}{I_o^2} = 510.2\Omega$ bandwidth = 10hz and required phase margin = 60 degrees.

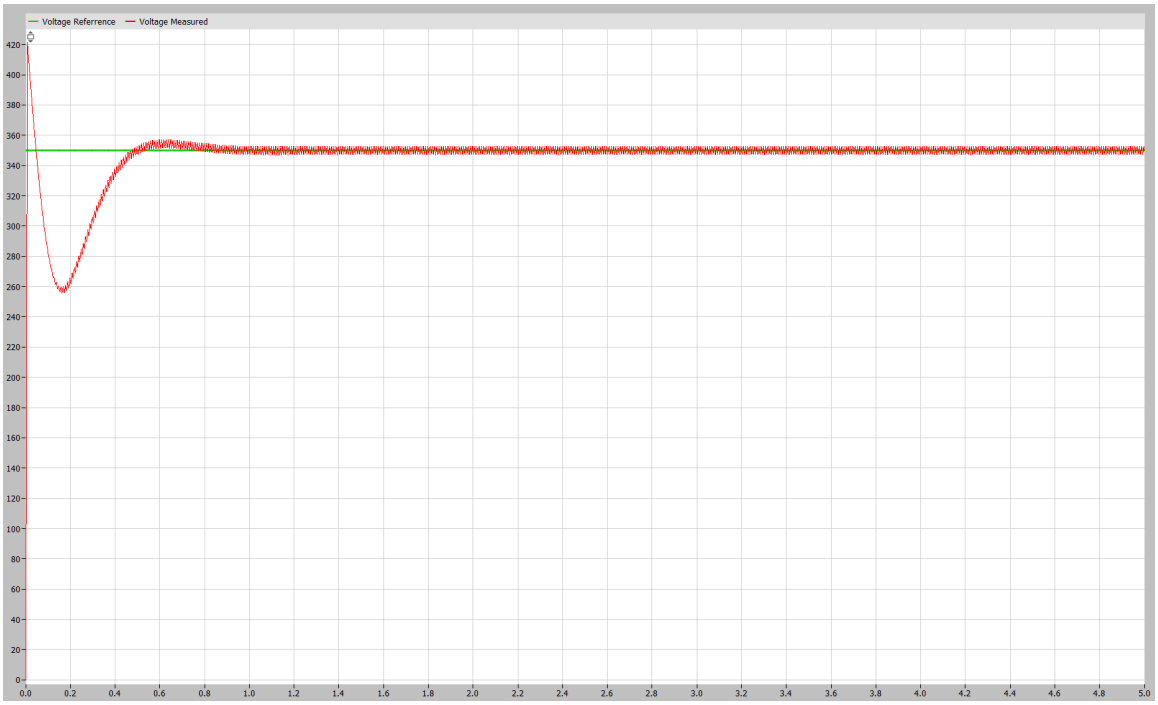
The controller transfer function will be as the following:

$$G_C(S) = \frac{1.278e-3}{S}\frac{(1+\frac{S}{25.13})}{(1+\frac{S}{157.1})}$$

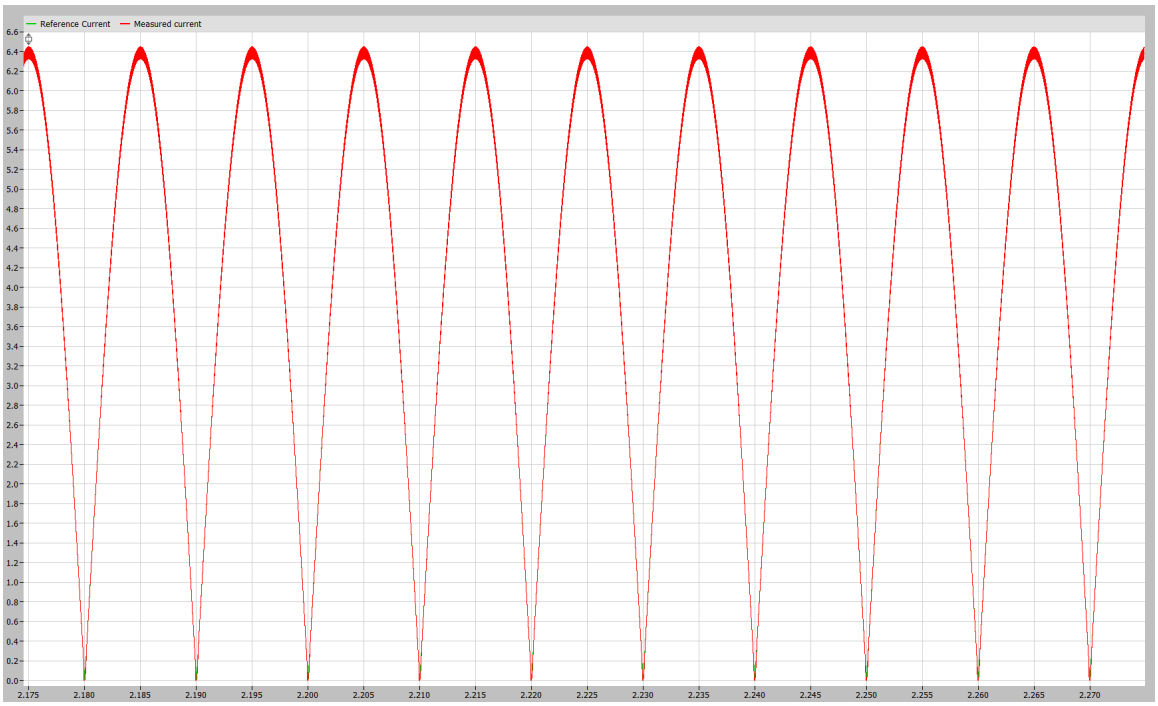
Simulation Results

The boost PFC circuit with its control is simulated with the above parameters using PLECS as in the below figure and the results as in the following figures. The load is simulated as a resistor to test the functionality of the PFC circuit but will be replaced by the isolated DC-DC converter at a later chapter.

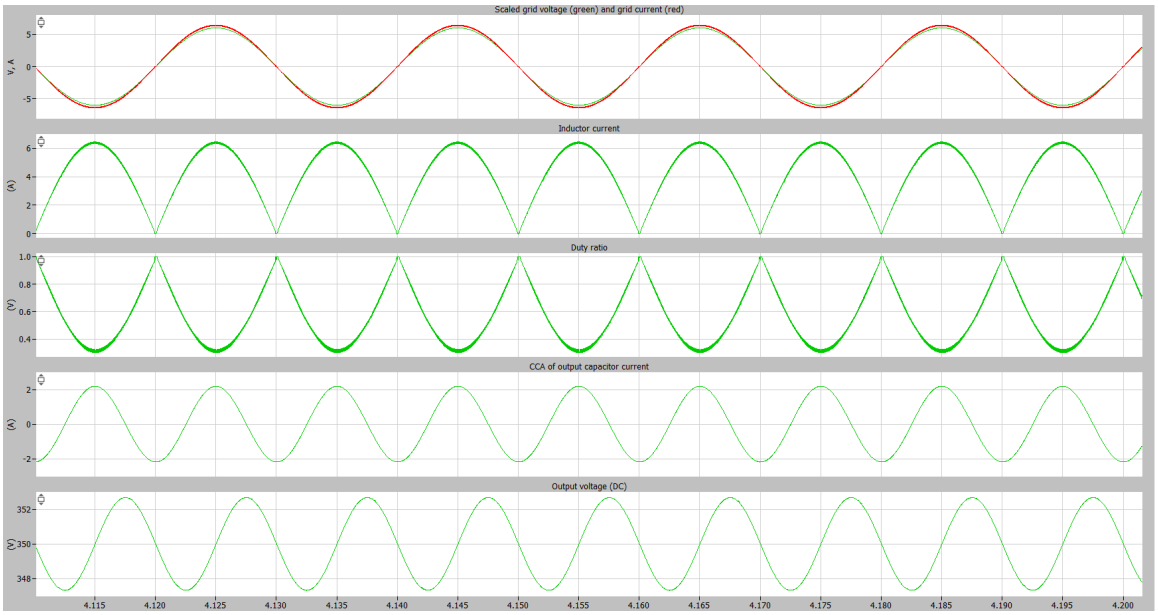




In the above figure, it is noticeable that the measured voltage response is slow compared to the reference which is because of the low bandwidth of the voltage controller. The reference voltage is supposed to be constant anyways so it is acceptable.



For the current reference and measured, the reaction is fast due to the high bandwidth of the current controller.


Scaled grid voltage (green) and grid current (red)
v, A
5
0
-5
Inductor current
(A)
6
4
2
0
Duty ratio
(Y)
1.0
0.8
0.6
0.4
CCA of output capacitor current
(A)
2
0
-2
Output voltage (DC)
(V)
352
350
348
4.115
4.120
4.125
4.130
4.135
4.140
4.145
4.150
4.155
4.160
4.165
4.170
4.175
4.180
4.185
4.190
4.195
4.200

Isolated Flyback DC-DC Converter

Circuit Design

Input Voltage: 350V
Maximum output Voltage ripple is 0.5%
Maximum inductor current ripple is 10%
$f_s = 400Khz$
Phase Margin = 60°

Transformer Design:

$Turns\ Ratio = V_{Primary} / V_{Secondary} = 350/35 = 10$

Inductor Selection

$D = 24/35 \approx 0.7$

$L = \frac{V_o(1-D_{min})T_s}{\Delta I_L} = 36uH$

$I_{L,pk} = I_{o,max} + \frac{\Delta I_l}{2} = 10.5A$

Capacitor Selection

$C > \frac{\Delta I_L}{\Delta V_o} * \frac{1}{8f_s} = 2.6uF$

$ESR < \frac{0.005*24}{1} = 120m\Omega$

$I_{RMS} > \frac{1}{2\sqrt{3}} = 0.29A$

Diode Selection

$Voltage\ rating = 24V + Margin$
$Peak\ current\ rating = I_{L,pk} = 10.5A$
$RMS\ current = I_{o,max} * \sqrt{D_{max}} = 8.9A$

MOSFET Selection

$Voltage\ rating = 350V + Margin$
$Peak\ current\ rating = I_{L,pk}/10 = 1.05A$
$Average\ current = I_{o,max}(1 - 0.6) = 0.42$

Controller design

$wc := 2 \cdot \pi \cdot 10000 \qquad PM := 60 \qquad j := \sqrt{-1} \qquad s := j \cdot wc = 6.283\mathrm{i} \cdot 10^4$

$L := 36 \cdot 10^{-6} \qquad ESR := 0.08 \qquad Co := 2.6 \cdot 10^{-6} \qquad R\_L := 2.4 \qquad Vin := 35 \qquad Vo := 24$

$$Gp := \frac{Vin \cdot (1 + s \cdot Co \cdot ESR)}{1 + s \cdot \left(\frac{L}{R\_L} + Co \cdot ESR\right) + s^2 \cdot L \cdot Co \cdot \left(1 + \frac{ESR}{R\_L}\right)} = 17.042 - 25.603\mathrm{i}$$

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot Co}} = 1.645 \cdot 10^4 \qquad \frac{1}{2 \cdot \pi \cdot ESR \cdot Co} = 7.652 \cdot 10^5$$

$$phi\_sys := -56.35$$

$$phi\_boost := (PM - 90 - phi\_sys) \cdot \frac{\pi}{180} = 0.46$$

$$k := \tan\left(\frac{phi\_boost}{2} + \frac{\pi}{4}\right) = 1.611$$

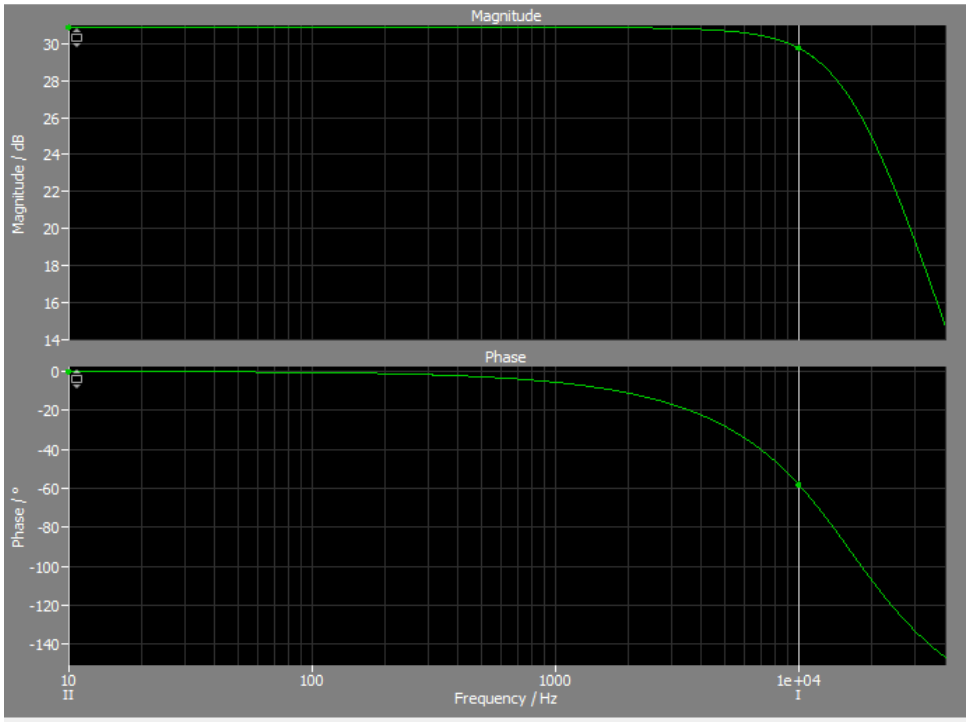
$$wz := \frac{wc}{k} = 3.9 \cdot 10^4 \qquad wp := k \cdot wc = 1.012 \cdot 10^5$$

$$G\_OL\_pre(s) := Gp \cdot \left(\frac{1}{s} \cdot \frac{1 + \frac{s}{wz}}{1 + \frac{s}{wp}}\right)$$

$$Kc := \frac{1}{|G\_OL\_pre(j \cdot wc)|} = 1.268 \cdot 10^3$$

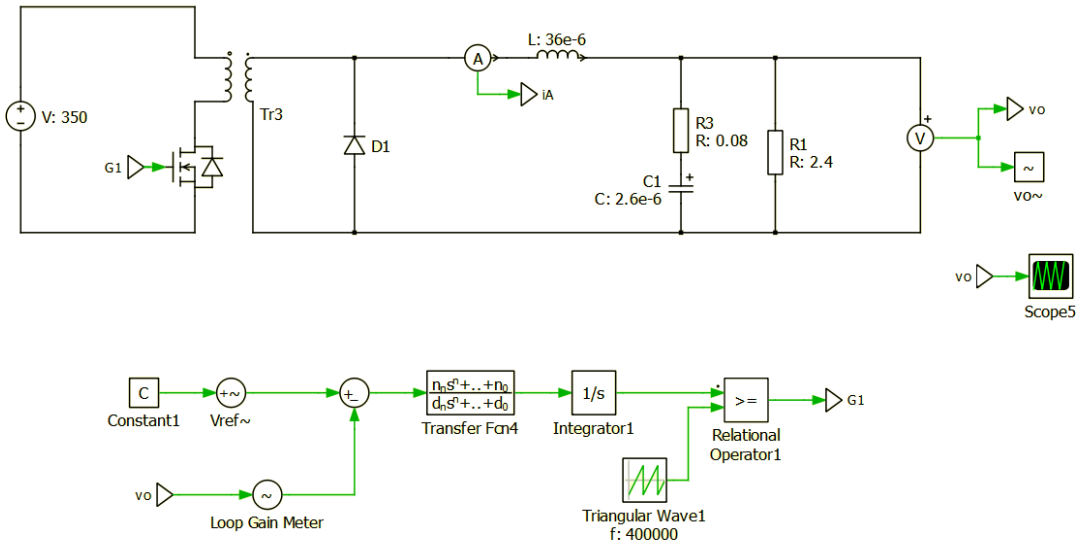
$$Gc(s) := Kc \cdot \left(\frac{1}{s} \cdot \frac{1 + \frac{s}{wz}}{1 + \frac{s}{wp}}\right)$$

Plecs Small Signal Analysis

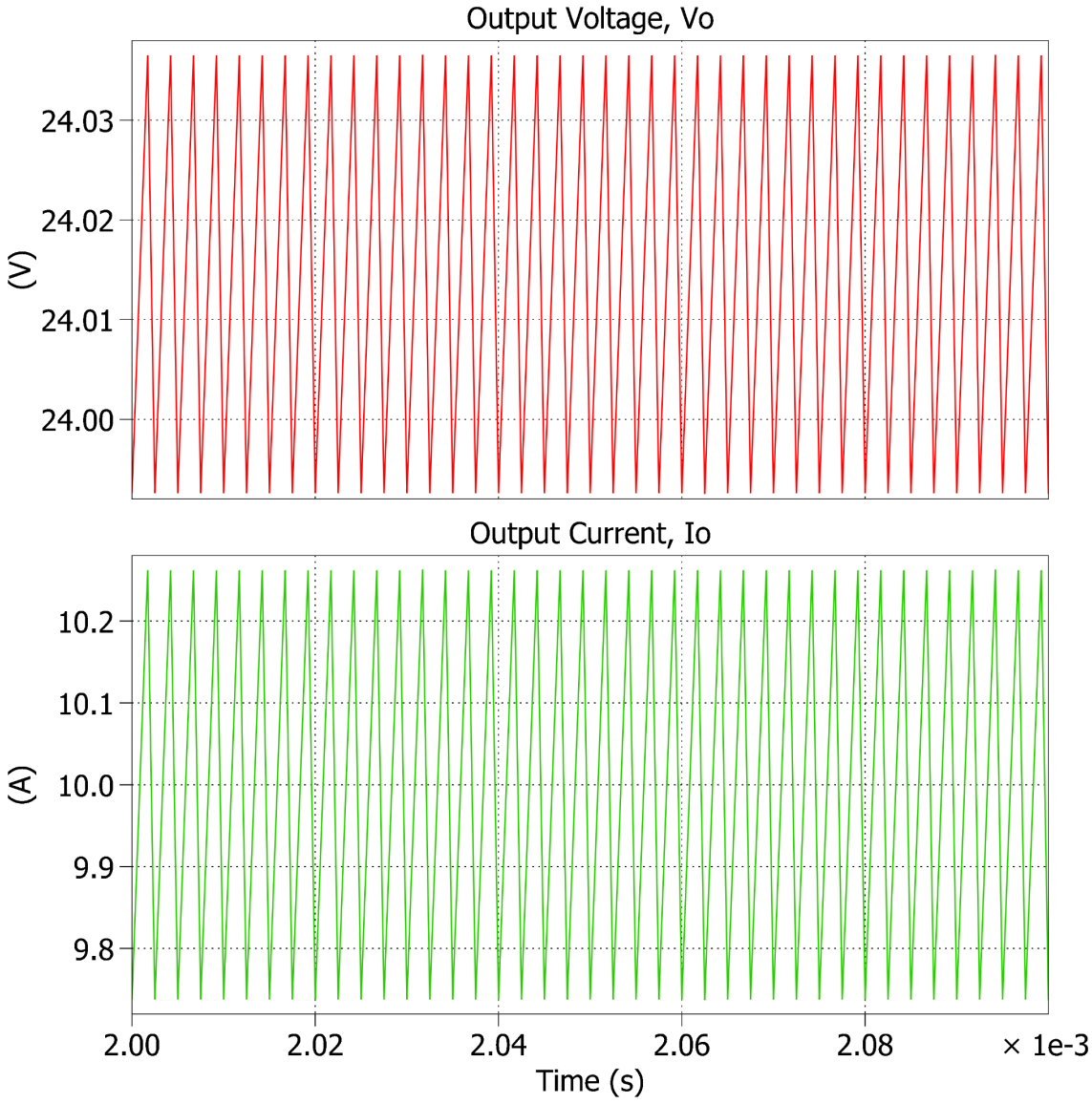


Plecs analysis verifies the calculated values above

Schematic



Simulation Result

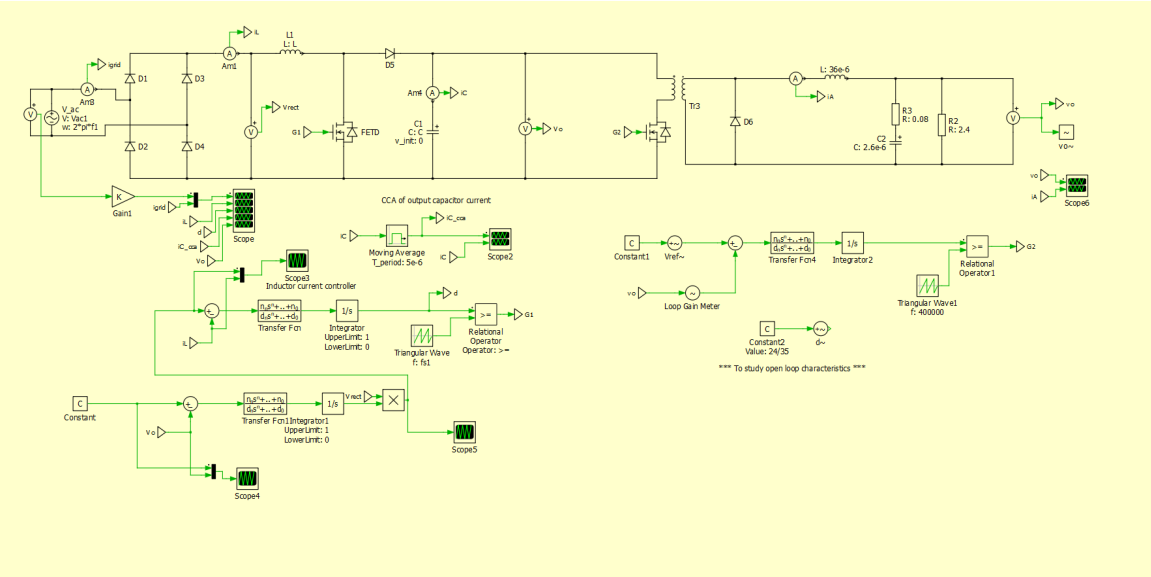


Data

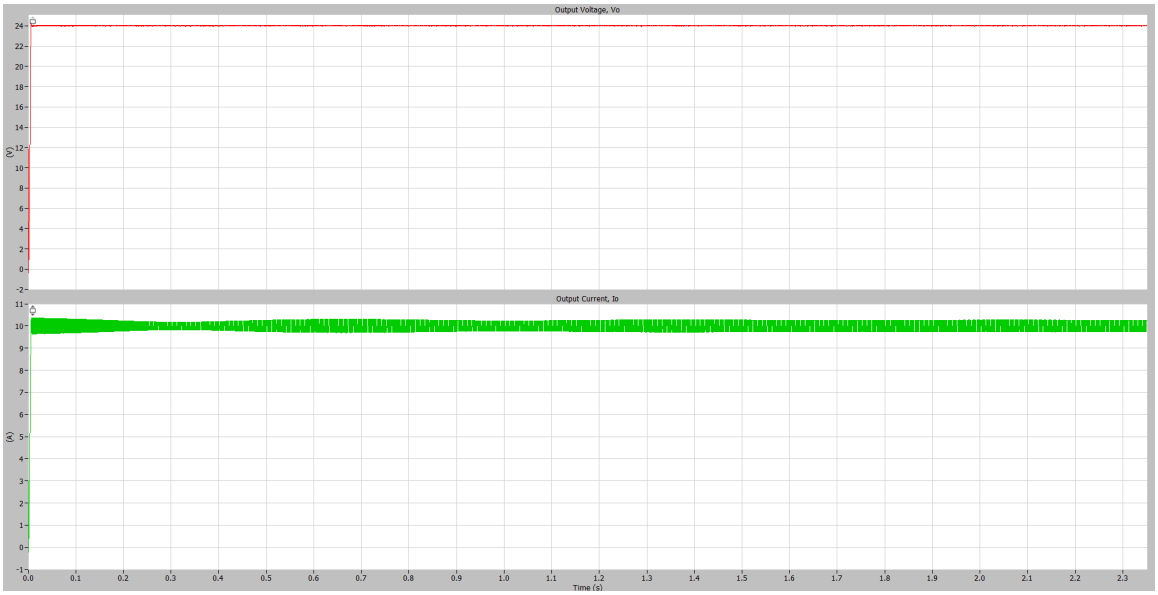
Name	Cursor	Cursor	Min	Max	Mean	RMS
Time	0.003...	0.006...				
Output Voltage, Vo						
Vm5:Measured voltage	23.9926	24.0365	23.9926	24.0365	24.0145	24.0145
Output Current, Io						
Am1:Measured current	9.7377	10.2621	9.7377	10.2621	9.9999	10.001

Conclusion:

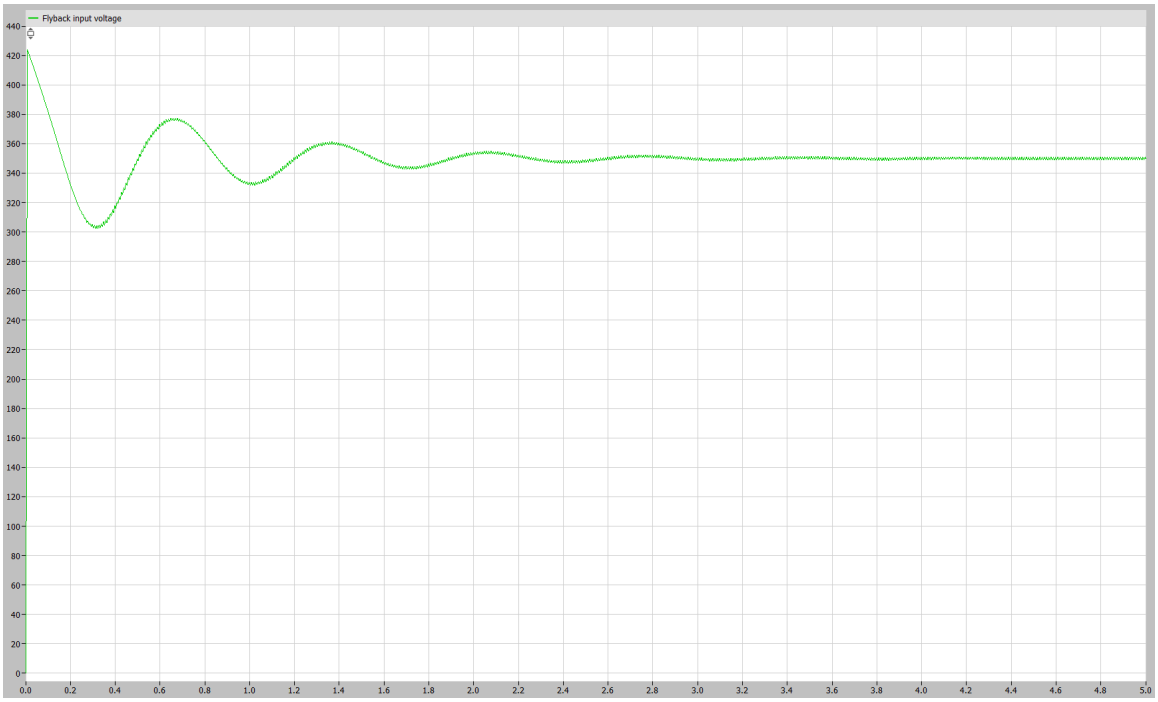
By integrating the 2 circuits discussed above together, we get the below schematic. The AC mains supply a diode bridge rectifier then fed to boost PFC and the DC output is fed as the DC source for the isolated flyback converter.



By simulating the above circuit we notice that the final output voltage and current ripples increase as below but still within the acceptable range. That is due to the added ripple of the input DC as it is not pure perfect DC as it was before.



In the figure below, the output of boost PFC and the input for the isolated flyback converter is plotted. Notice that there are some ripples in the voltage which are accepted (less than 10%) and also the slow behavior of the voltage due to the very low bandwidth of the controller.



The 2 systems integrated together behave more or less the same as independent converters with slight differences that are acceptable and within the limits required. Adding the PFC circuit increased the overall cost of the converter, however it made sure that the system fits the requirements and regulations for the PF and THD.