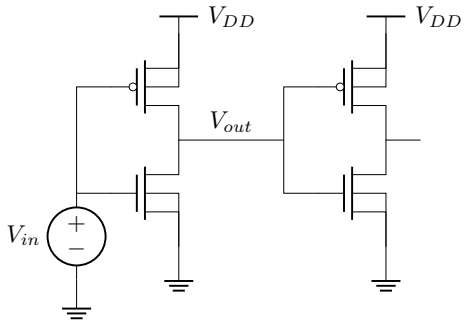
EC 5311 Digital IC Design: Assignment 3
CMOS inverter - transient characteristics

$V_{Tn} = 0.7,$	$\mu_n = 0.025\,\mathrm{m}^2/\mathrm{V}-\mathrm{s},$	$C_{oxn} = 0.00834\,\mathrm{F}/\mathrm{m}^2,$	$vsat_n = 8e4\mathrm{m}/\mathrm{s},$	$\lambda_n = 0.2$
$\lvert V_{Tp}\rvert = 0.7,$	$\mu_p = 0.009\,\mathrm{m}^2/\mathrm{V}-\mathrm{s},$	$C_{oxp} = 0.00816\,\mathrm{F}/\mathrm{m}^2,$	$vsat_p = 3e4\,\mathrm{m}/\mathrm{s},$	$\lambda_p = 0.2.$

1. Consider the static CMOS inverter shown below. It drives another identical inverter. The input V_{in} is a pulse between 0 and V_{DD}, with a rise and fall time equal to 5 ps and a pulse width of 250 ps. The output is V_{out}.



   (a) Set $V_{DD} = 1.8V$. Assume that $L_n = L_p = 0.15\,\mu\mathrm{m}$ and $W_n = 0.42\,\mu\mathrm{m}$. Obtain the delay for $W_p = 0.42\,\mu\mathrm{m}, 0.84\,\mu\mathrm{m}, 1.26\,\mu\mathrm{m}$.

   (b) Set W_p so that delay is minimised. Plot the delay as a function of V_{DD} for $V_{DD} = 1\mathrm{V}$ to $1.8\mathrm{V}$ in steps of 0.1V. How does it compare with analytical estimates?

   (c) Plot the measured and estimated energy-delay product as a function of V_{DD}. What is the optimum V_{DD}?