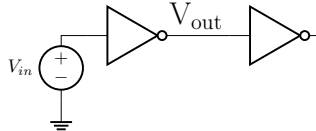


EC 5311 Digital IC Design: Assignment 5
Ring oscillator – post-layout extracted simulation

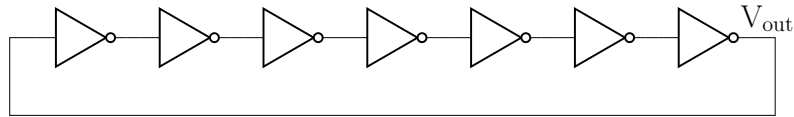
$V_{Tn} = 0.7,$ $\mu_n = 0.025 \text{ m}^2/\text{V} - \text{s},$ $C_{oxn} = 8.34 \text{ fF}/\mu\text{m}^2,$ $vsat_n = 8 \times 10^4 \text{ m/s},$ $\lambda_n = 0.2$ $ V_{Tp} = 0.7,$ $\mu_p = 0.009 \text{ m}^2/\text{V} - \text{s},$ $C_{oxp} = 8.16 \text{ fF}/\mu\text{m}^2,$ $vsat_p = 3 \times 10^4 \text{ m/s},$ $\lambda_p = 0.2.$

1. Draw a DRC and LVS clean layout of the CMOS inverter with the minimum delay from Assignment 3.

- (a) Extract the parasitic values from the layout and find the delay of the inverter using the circuit:



- (b) Measure the delay including the layout parasitic of net V_{out} .
2. Using the inverter layout above, draw the layout of a seven stage ring oscillator shown below.



To ensure oscillation in the transient simulation, set the node $V_{out} = 0\text{V}$ initially using: `.ic v(Vout)=0`

- (a) Measure the oscillating frequency for $V_{DD} = 1.8\text{V}$ with the layout parasitics.
 - (b) Plot the oscillating frequency and time period as a function of V_{DD} for $V_{DD} = 1\text{V}$ to 1.8V in steps of 0.1V .
 - (c) Compare the frequencies against pre-layout simulation in Assignment 4.