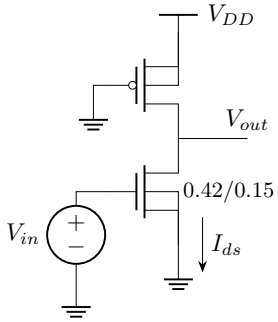
EC 5311 Digital IC Design: Assignment 2
CMOS inverter - DC characteristics

$V_{Tn} = 0.7,$	$\mu_n = 0.025m^2/V-s,$	$C_{oxn} = 0.00834F/m^2,$	$vsat_n = 8.e4m/s,$	$\lambda_n = 0.18$
$\lvert V_{Tp}\rvert = 0.7,$	$\mu_p = 0.009m^2/V-s,$	$C_{oxp} = 0.00816F/m^2,$	$vsat_p = 2.5e4m/s,$	$\lambda_p = 0.18.$

1. Consider the pseudo-nMOS inverter shown below.



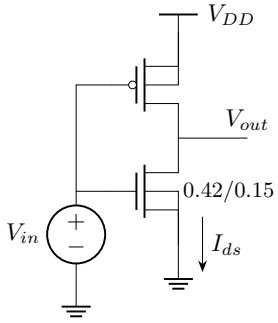
Size the pMOS transistor so that $V_{OL} = 0.1V$. Using Ngspice, plot the DC transfer characteristic.

(a) Find the inverter threshold voltage.

(b) Plot the derivative and obtain the high and low noise margins. Do an approximate calculation using the analytical models and compare with the simulated value.

(c) Assuming $V_{in} = V_{DD}$, find the average power dissipated and compare with the analytically obtained value.

2. For the static inverter shown below



find $(W/L)_p$ so that the inverter threshold voltage $V_{inv} = V_{DD}/2$. Plot the DC transfer characteristic.

(a) Plot the derivative and obtain the noise margins.

(b) How does the characteristic change if $(W/L)_p$ is increased by a factor of 10? Decreased by a factor of 10?

(c) Obtain the DC transfer characteristic for V_{DD} ranging from $0.2V$ to 1.8V in steps of 0.2V. Can it be used as an inverter for these supply voltages? When possible, you can resize pMOS transistor to get the inverter threshold voltage to be approximately $V_{DD}/2$. If the circuit does not behave as an inverter for some supply voltage, what change can be made to the pMOS width or length to turn it into an inverter?

(d) Plot the I_{ds} vs V_{in} for $V_{DD} = 0.2, 0.8, 1.8V$. Find the peak I_{ds} for each scenario and compare it with the analytical value.