Logic Synthesis

Electronic Design Automation (Fall 2022)

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Outline

Introduction

What is Logic Synthesis

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- Behaviour -> Gate Level Implementation

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    - Logic Optimization
    - ~~Technology Mapping~~

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- Multiple Steps:
    - Translation
    - Logic Optimization
    - ~~Technology Mapping~~
- High Level Synthesis
- Gate Level Synthesis

Some things to know

- What is ’synthesizable’ ?

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- What is ’synthesizable’ ?
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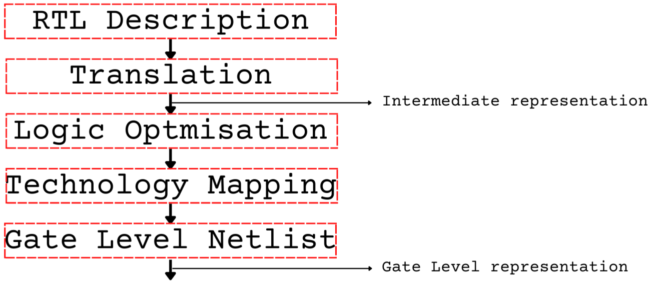
- Objects to be synthesized
    - Boolean functions
    - State Machines
- How do you know if it’s done correctly?
    - Gate level equivalence checking

Logic Synthesis Flow

Steps in Logic Synthesis



Logic Synthesis Flow

Exploring ABC

Installing ABC

```
$ git clone https://github.com/berkeley-abc/abc.git
$ cd abc; make -j$(nproc)
```

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- Represented in terms of AND and INV only

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- Try it out! $a'b + ab + a(a' + b)$

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- Represented in terms of AND and INV only
- Try it out! $a'b + ab + a(a' + b)$
- Oh wait this seems complex. let’s slow down!

Truth Table Optimisations - 2 level

- What is a truth table?
    - tells the truth of a function (in terms of inputs)

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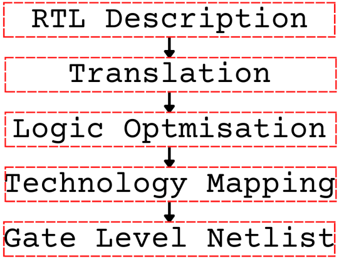
- What is a truth table?
    - tells the truth of a function (in terms of inputs)
    - write a simple one (and it's kmap)
    - let's understand this, and optimize it

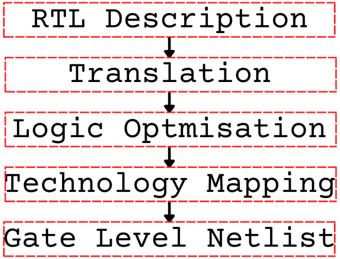
Description - Optimisation (Activity)

- Write an FSM



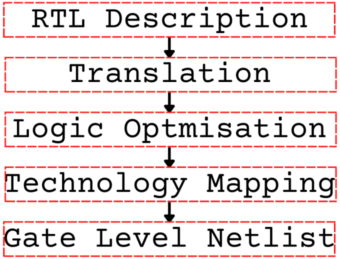
Description - Optimisation (Activity)

- Write an FSM
- Write it’s boolean form



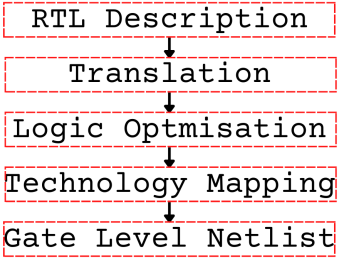
Description - Optimisation (Activity)

- Write an FSM
- Write it's boolean form
- Break it down



Description - Optimisation (Activity)

- Write an FSM
- Write it's boolean form
- Break it down
- ~~Convert it to NAND2~~



Same thing using ESPRESSO - A Heuristic Approach

Levels of minimisation

- Two level
  - AND plane
  - OR plane
  - Goal is to reduce num. of AND gates and their inputs.
- Multi level
  - let’s not get into this for now :)

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    - EXPAND - expand this cover

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    - REDUCE - shrink this cover

Two-Level Minimisation

- Steps:
    - EXPAND - expand this cover
    - IRREDUNDANT - keep only essential ones
    - REDUCE - shrink this cover
- Until timeout or stable covers are obtained[1]

[1]Multiple times - Heuristic Approach

A detailed explaination using k-maps

- k-maps as cubes
- live example

An example from RISC-V instruction decoder

- show op_addr_mask from decode_box
- show abc script in misc/ from decode_box

Logic Synthesis using Yosys

Install and Setup Yosys

```
$ git clone https://github.com/YosysHQ/yosys.git
$ cd yosys; make -j$(nproc); sudo make install
```

Steps for Logic Synthesis (using Yosys)

```
yosys> read -sv design_name.v /* Read using verilog frontend */
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yosys> techmap /* map to generic (internal) library */
yosys> write_verilog synth.v /* write the netlist */
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yosys> write_verilog synth.v /* write the netlist */
yosys> dfflibmap -liberty my_library.lib /* map seq elements */
yosys> abc -liberty my_library.lib /* map comb cells */
```

Writing sample design using bsv

synthesizing your own design (live demo) - and sending it through OpenLane

Conclusion

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Use opensource tools (!!)

Open for Discussions

Thank You