PES UNIVERSITY
ELECTRONIC CITY CAMPUS

The Landscape of Near- / Sub-Threshold Computing

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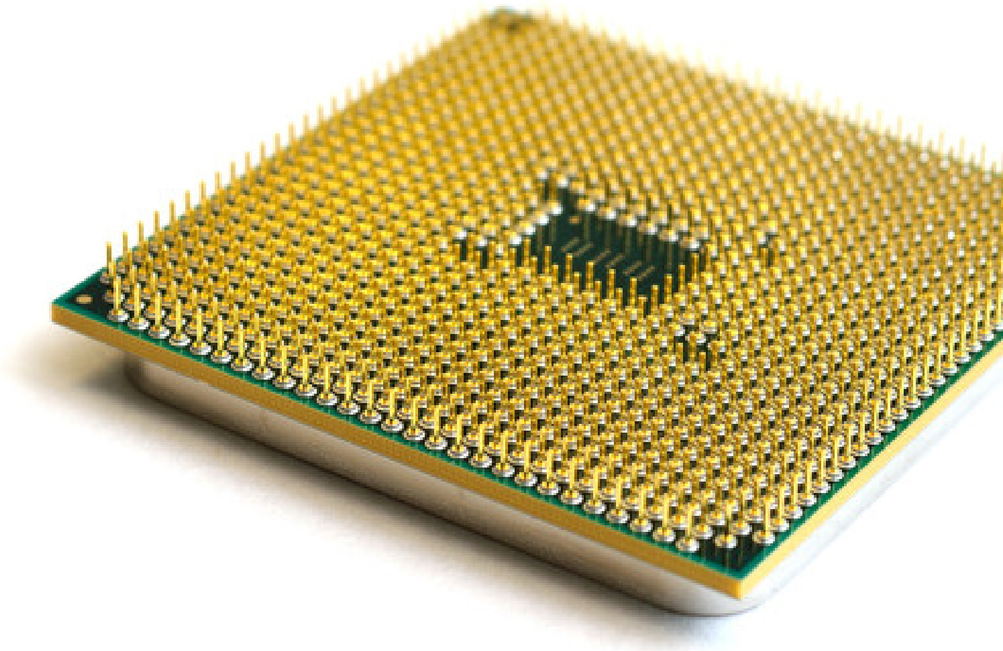


About Me

- I am a senior year undergraduate student at PES University, Electronic City Campus, Bengaluru with a major in Electronics and Communication Engineering

- I am currently working at the Centre for Heterogeneous and Intelligent Processing Systems on multi-objective optimization for the design of energy-efficient standard-cell-based RISC-V architectures

- My research interests are in Digital System Design and Very Large Scale Integrations of Low-power Digital circuits

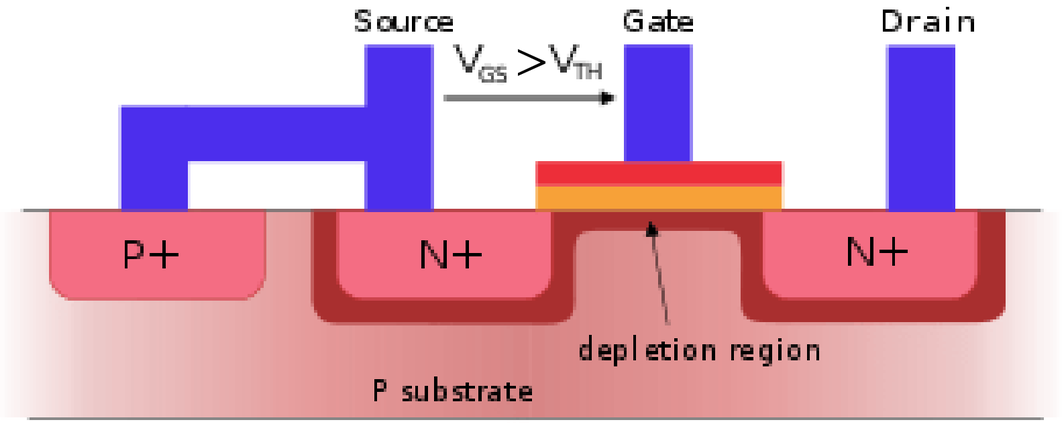
Presentation Outline

- Trends and Challenges in Near - / Sub- Threshold Computing
- Applications of Near- / Sub- Threshold Circuits and Comparison with conventional circuits
- EDA for Subthreshold Optimized CMOS
- Performance analysis of unoptimized subthreshold circuits

Operation of a MOS Field Effect Transistor

Operation of a MOSFET

- Bias voltage at gate and body
- Channel between Source and Drain
- Minimum bias voltage for channel formation - threshold (Vth)
- Effect of field at gate (insulator - SiO2)



Transistor Sizing

- IV characteristics are different
- mobility of electrons is much larger than the mobility of holes.
- UMC's commercial 180nm bulk CMOS (Wp/Wn)

- 13.28 for sub-vt
- 9.63 for regular

- UMC's commercial 28nm high-k bulk CMOS (Wp/Wn)

- 10.28 for sub-vt
- 6.22 for regular

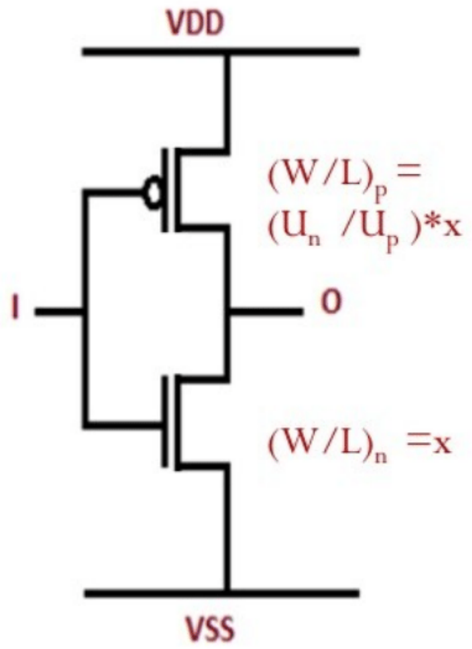
The standard cells are sized as

$$(W/L)_p = U_n / U_p \text{ x } (W/L)_n$$

- An increase in Wp/Wn

- improves the output-high swing
- degrades the output-low voltage

- further compounded by process variations.



Why Near- / Sub- Threshold?

Presentation Outline

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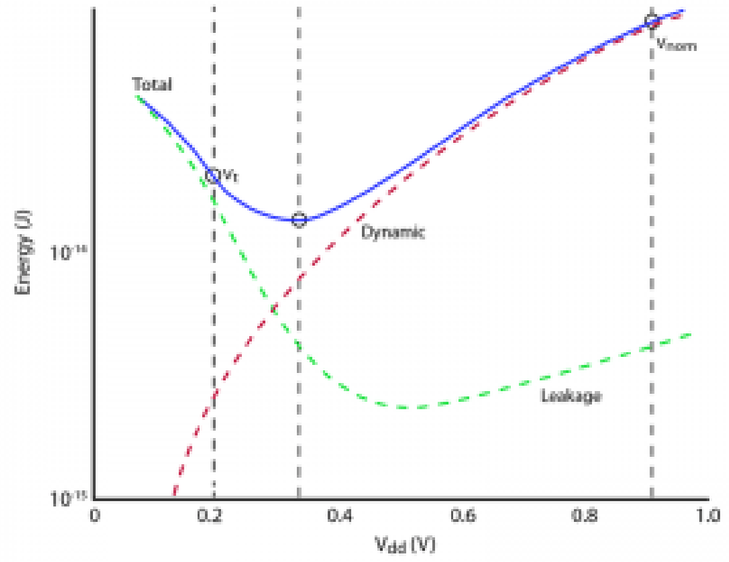
Why Near- / Sub- Threshold?

- Energy budget for portable applications
- Reducing circuit supply voltage also minimizes heat.
- Aim: take as much advantage as possible of fCV^2
- Voltage scaling is a known technique to reduce energy consumption.

What are the challenges?

Challenges of Near-Threshold

- Reduction in operating frequency
- Less control
- Requires additional power supplies
- Threshold can vary
- SRAM designs - high bitline leakage
- Retention becomes a problem



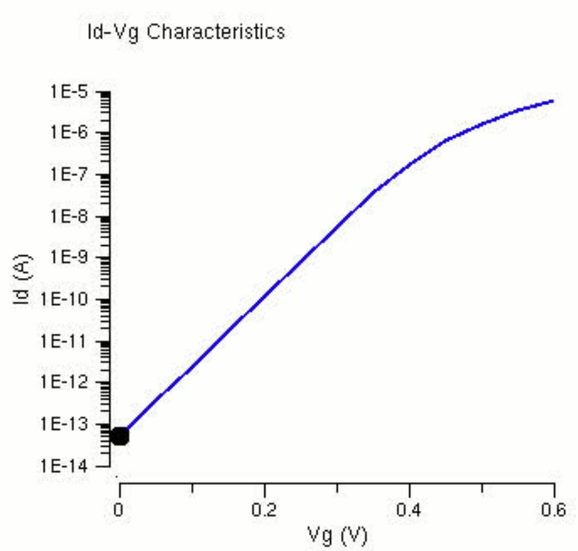
Challenges of Sub-Threshold

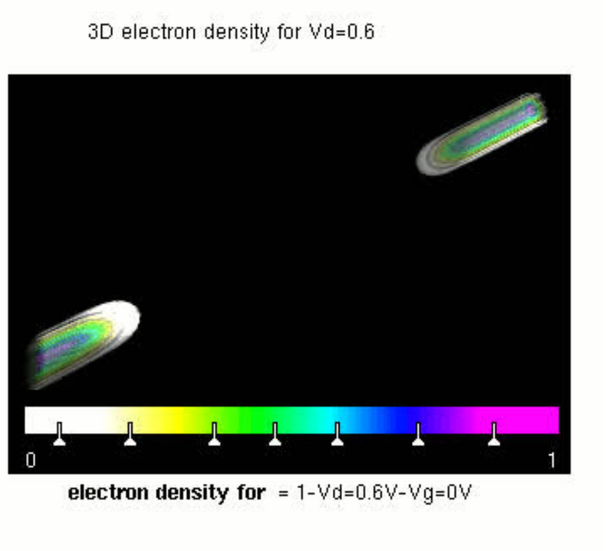
- Custom Standard Cells
- Isub increases
- Poor transistor models
- Logic swings and noise
- Sensitivity to operating conditions
- Logistical challenges

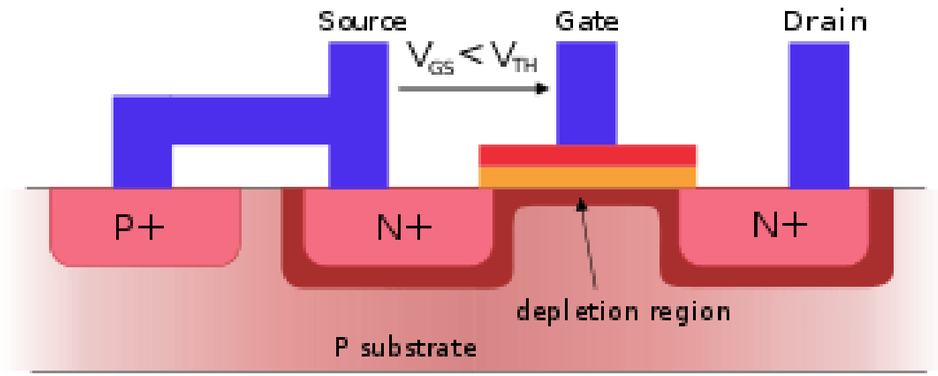
What is Sub-Threshold Operation?

Sub-Threshold Operation

- Gate-to-source voltages below the threshold voltage
- Insufficient charge concentration
- Incomplete channel formation







Where is Subthreshold used?

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Applications of Subthreshold Devices

- IoT devices
- Biomedical sensors/implants
- Self-sustainable systems - outer space applications
- Processors with low energy budget
- FPGAs

Subthreshold Design Effort

Subthreshold Design Effort

- Custom standard cell library - custom sizing
- Intensive MC analysis - Process variations
- Minimisation of switching activity - isolation circuitry
- Minimisation of switched capacitance - logic level
- Exhaustive Testing

Some Existing Subthreshold Devices

Subthreshold FPGAs

What is an FPGA ?

- Matrix of configurable logic blocks (CLBs)
- Connected via programmable interconnects
- Reprogrammable
- One-time programmable ones are available
- Dominant types are SRAM based

Applications of FPGAs

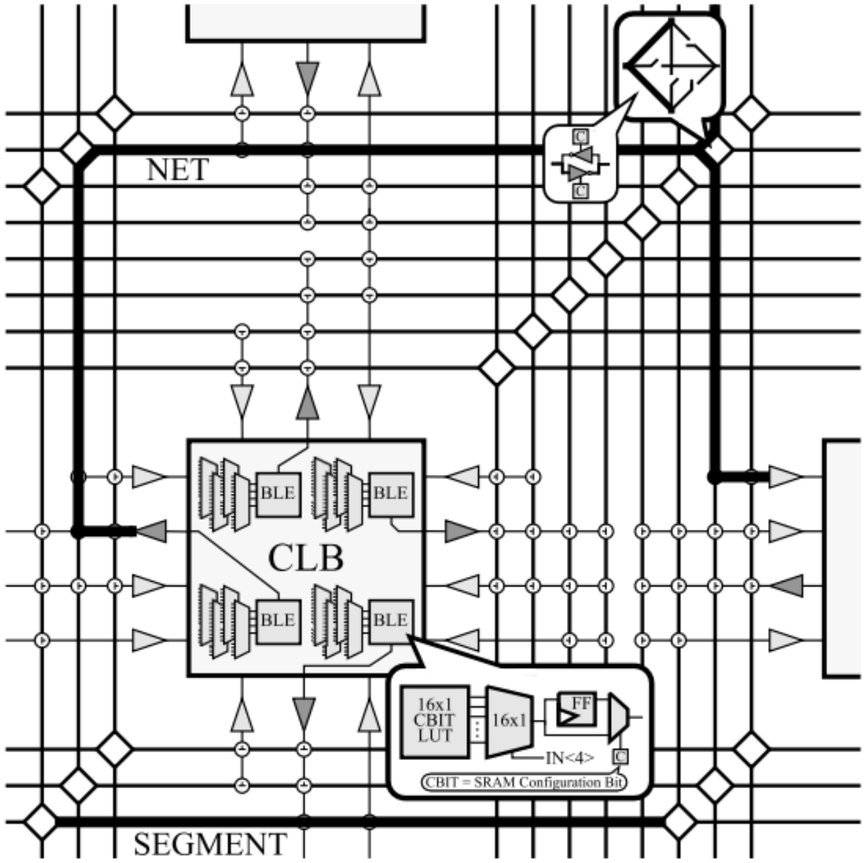
- Aerospace & Defense - Radiation tolerance
- ASIC prototyping - SoC system modeling
- Automotive - driver assistance systems
- Data Centres - high-bandwidth, low-latency servers, networking, and storage applications
- Accelarators - Large workloads
- Wired and Wireless Communications - connectivity, transport and networking

Subthreshold FPGAs

Virginia'a Custom Case

University of Virginia - RLP VLSI

- 9 BLEs in a CLB vs 4 BLEs
- Bi-directional tristate drivers -> TG single passgate switches
- Low swing (0.4 Vdd)
- Async sense amp for swing - clock driver
- independent async sense amp - dual Vdd
- 2.5x area efficient
- 7x faster
- 25x energy efficient
- number of FETs reduced by 3X



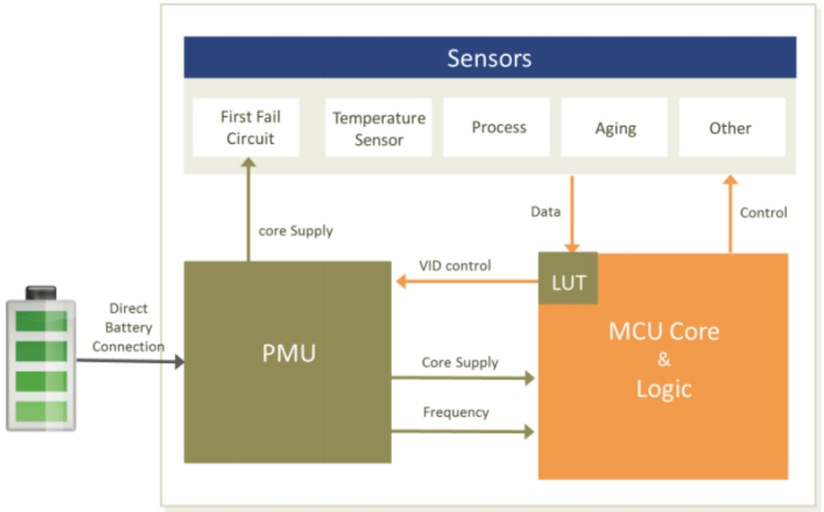
Near- / Sub- Threshold Processors

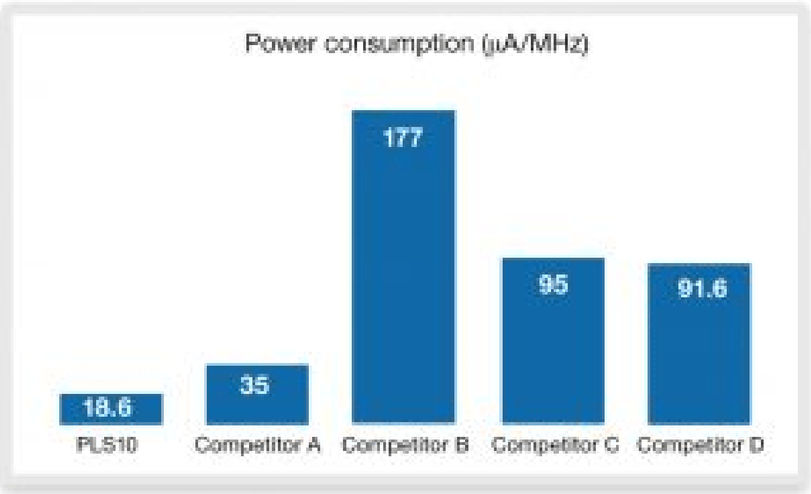
Subthreshold Processors

Synopsys' ARC using PLSense's subthreshold libraries

PLSense PLS10 IC based on Synopsys' ARC Data Fusion Subsystem

- DSP Processor
- FS and SF corners
- 312 K-80 MHz
- Adaptive Dynamic Voltage Control (ADVC)
- First-Fail Circuitry - DLLs





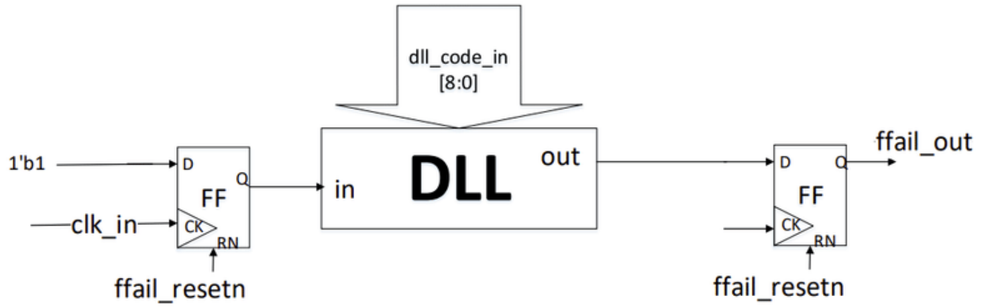
Subthreshold Processors

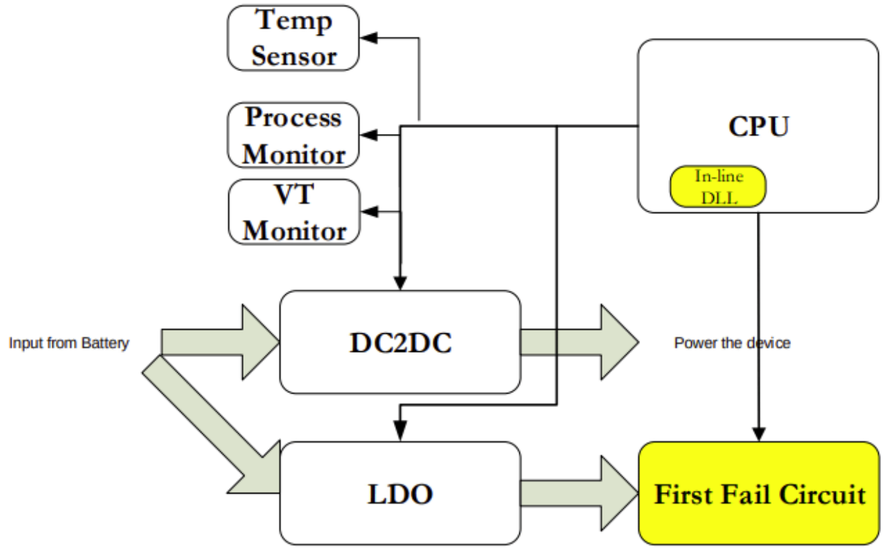
Synopsys' ARC using PLSense's subthreshold libraries

PLSense PLS10 IC based on Synopsys' ARC Data Fusion Subsystem

First-Fail Circuit

- Critical path monitor
- FFail indicated delay match
- Voltage is scaled until DLL path is matched

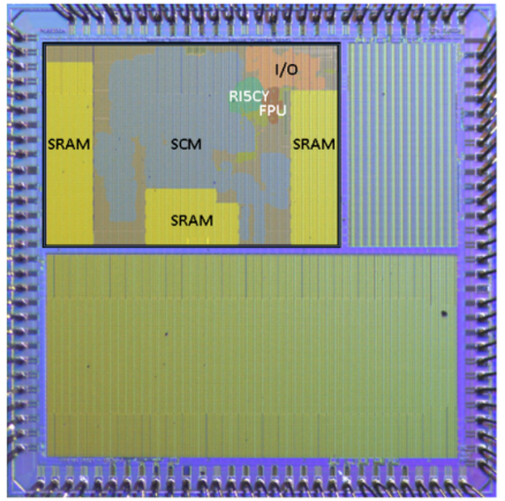




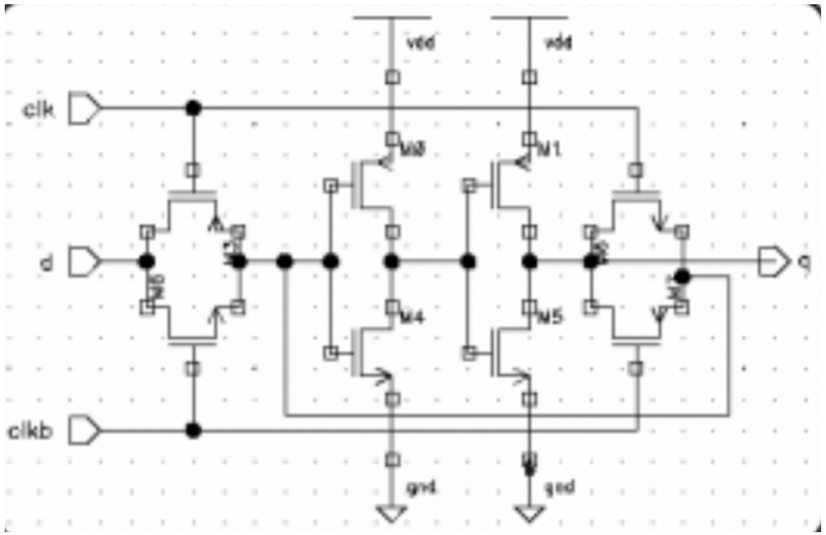
Near- Threshold Processors

Quentin
PULP - ETH Zurich

- Heterogeneous SCM + SRAM
- Power gated SRAM
- Separate supplies for SRAM, SCM and BB
- Peak 670 MHz without FBB
- Large area overhead



Technology	CMOS 22nm FDX
Transistor Type	Flip-Well (LVT)
SoC Area	2.3mm^2
VDD range	0.5V - 0.8V
Body Bias Range	0.0V - 1.4V
Memory Transistors	24.8M
Logic Transistors	4.18M
Frequency Range (with ABB)	32 kHz - 670 MHz
	32 kHz - 938 MHz
Power Range (with ABB)	300 µW - 10.4 mW
	300 µW - 66.2 mW



How are these designed?

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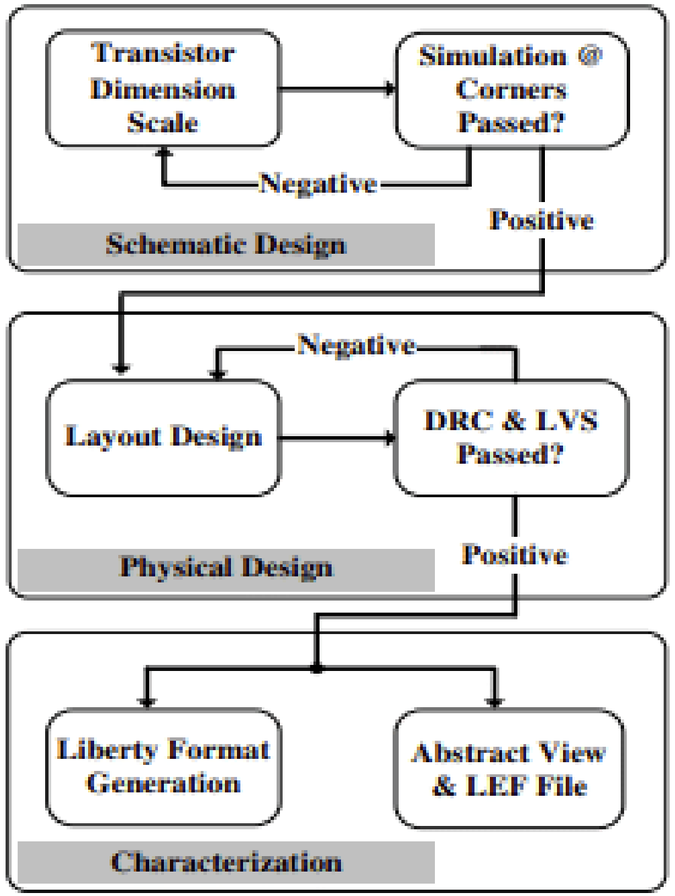
EDA for Sub-Threshold optimized CMOS

Standard Cell Creation

- SF and FS corners vs TT corners
- Large FETs - Transistor Sizing
- Less Polysilicon
- Low voltage MC analysis
- PVT Variations

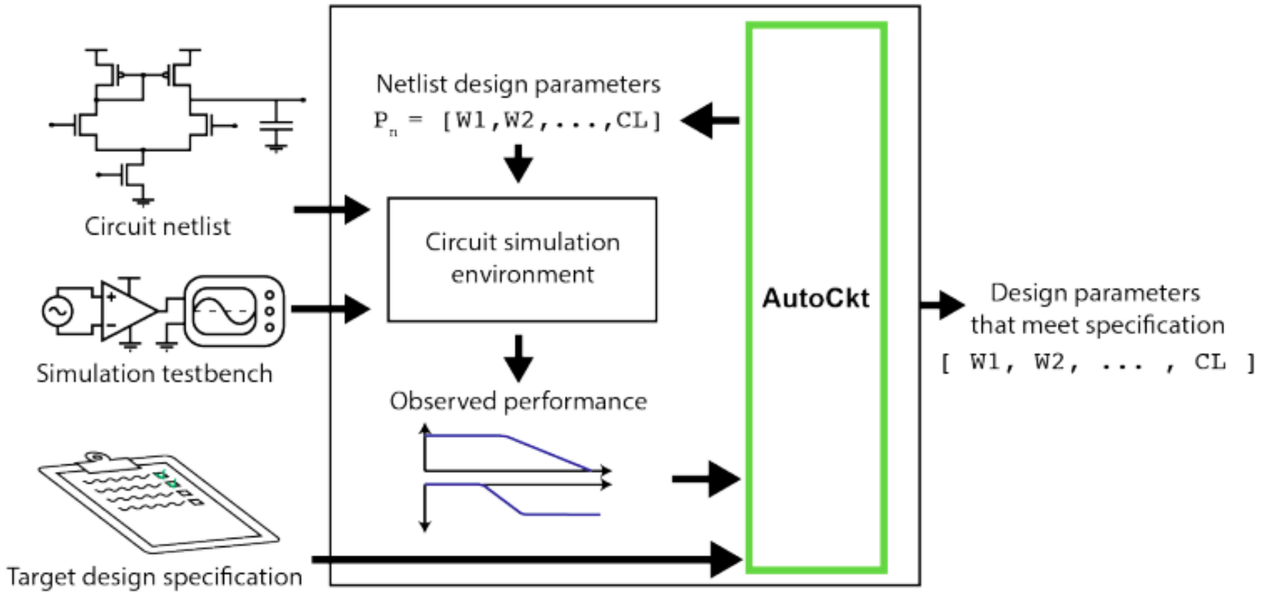


ECTs for Device Sizing

- Particle Swarm
- Simulated Annealing
- Genetic Algorithms
- Pareto Search (Preference based)

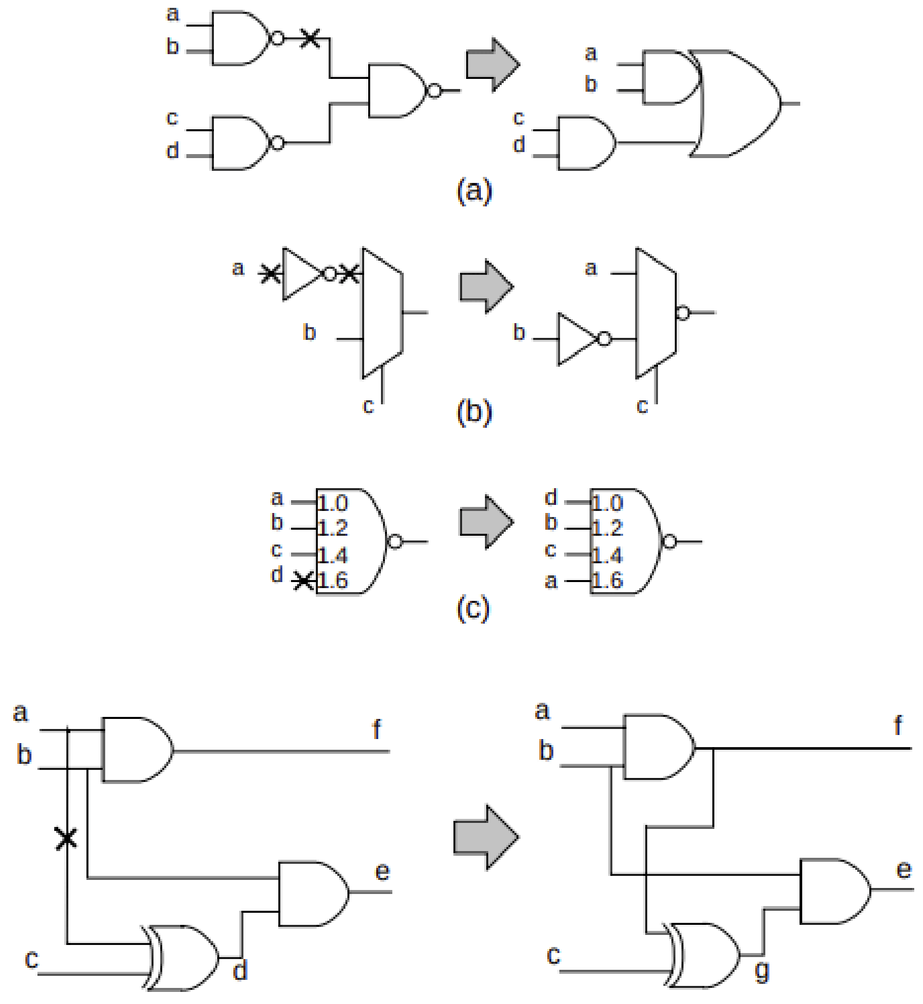
ML for Device Sizing

- Reward based
- More iterations
- Unconstrained
- Convergence is not guarenteed



Logic Synthesis for Low Power

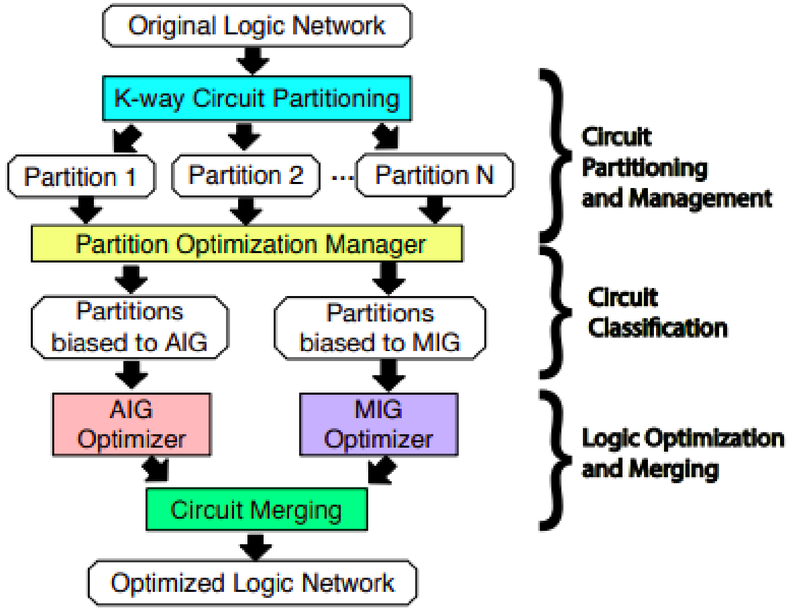
- Re-factoring (1a)
- Polarity assignment (1b)
- Pin Swapping (1c)
- Re-wiring transformation



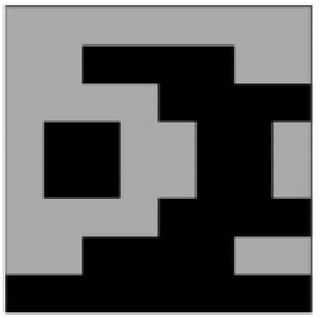
ML for Logic Synthesis

LSOracle - Utah

- KMImages
- DNNs for Image classification
- k-way partitioning
- AIG/MIG optimizers



ABC \ DEF	000	001	011	010	110	111	101	100
000	1	1	1	1	1	1	1	1
001	1	1	0	0	0	0	1	1
011	1	1	1	1	0	0	0	0
010	1	0	0	1	1	0	0	1
110	1	0	0	1	1	0	0	1
111	1	1	1	1	0	0	0	0
101	1	1	0	0	0	0	1	1
100	0	0	0	0	0	0	0	0

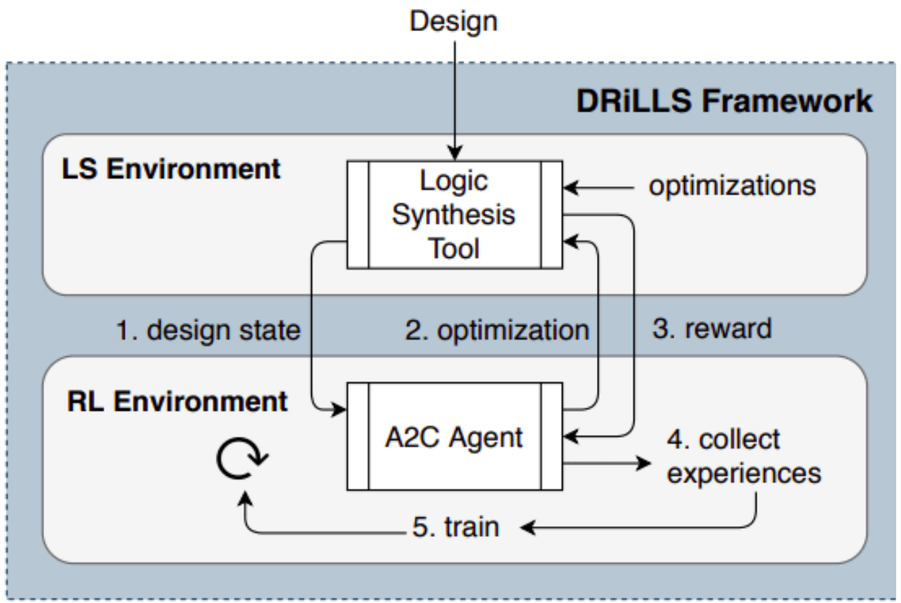


KMImage

ML for Logic Synthesis

DRiLLS

- Multi-objective reward function - area and delay
- Actor - Critic
- Primary objective - Reduction in area



			Optimizing (Area)		
			Decr.	*None*	*Incr.*
Constraint (Delay)	Met		+++	*0*	-
	Not Met	*Decr.*	+++	++	+
		None	++	0	- -
		Incr.	-	- -	- - -

How do these designs compare?

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Sub- Vt vs Near- Vt vs Super- Vt

- Low Vt is not always Low Power
- Area is almost same in sub vt and near vt
- No body bias required for subvt
- Separate standard cells required for subvt

	Sub-Vt	Near-Vt	Super-Vt
Area	High	High	Low
Power	High	Low	Highest
Delay	High	High	Low

Synthesis results (UMC 180)

- Standard cell library – 180nm – 7 cells
- Unconstrained synthesis
- All cells are symmetric

	8 bit ALU		
Parameter	Subvt cells	With XOR (Subvt)	Regular cells
Critical path	26.37 us	26.12 us	7.162 ns
Parameter	Subvt cells	With XOR (Subvt)	Regular cells
Leakage	12.27 nW	12.05 nW	102.39 nW
Internal	12.38 uW	12.18 uW	282.44 uW
Switching	29.49 uW	29.20 uW	1.00 mW
Total power	41.90 uW	41.40 uW	1.29 mW

We are yet to complete charecterizing the 28nm subvt standard cell library with parasitic in order to show a comparison

Conclusion

- Use sub-threshold circuits throughout by default
- Use near-threshold in those few cases where it’s possible
- Use super-threshold in those few cases where required for speed or bandwidth

Questions?

References

1. Zhai et al. A 2.60pJ/Inst Subthreshold Sensor Processor for Optimal Energy Efficiency (2006)
2. Huang et al. Machine Learning for Electronic Design Automation: A Survey (2021)
3. Hosny et al. DRiLLS: Deep Reinforcement Learning for Logic Synthesis (2020)
4. Calhoun et al. Sub-threshold Circuit Design with Shrinking CMOS Devices (2009)
5. Schiavone et al. Quentin: an Ultra-Low-Power PULPissimo SoC in 22nm FDX (2018)
6. Neto et al. LSOracle: a Logic Synthesis Framework Driven by Artificial Intelligence: Invited Paper (2019)
7. Luca Benini, Giovanni De Michelli LOGIC SYNTHESIS FOR LOW POWER
8. Settaluri et al. AutoCkt: Deep Reinforcement Learning of Analog Circuit Designs (2020)
9. Sankaranarayanan et al. A Single-VDD Ultra-Low Energy Sub-threshold FPGA (2012)
10. Grossmann et al. A Prototype FPGA Tile for Subthreshold-Optimized CMOS
11. Hrishikesh Kanitkar, Subthreshold circuits: Design, implementation and application (2008)
12. Li et al. Sub-threshold Standard Cell Library Design for Ultra-Low Power Biomedical Applications (2013)
13. Zangi et al. 0.45 v and 18 µA/MHz MCU SOC with Advanced Adaptive Dynamic Voltage Control (ADVC) (2018)
14. Chowdhury et al. Computing With Subthreshold Leakage: Device/Circuit/Architecture Co-Design for Ultralow-Power Subthreshold Operation (2005)
15. Keane et al. Subthreshold logical effort: a systematic framework for optimal subthreshold device sizing (2006)

Links

1. http://blaauw.engin.umich.edu/wp-content/uploads/sites/342/2018/02/Zhai-A-2.60pJInst.-Subthreshold-Sensor-Processor.pdf
2. https://arxiv.org/pdf/2102.03357.pdf
3. https://sci-hub.st/10.1109/ASP-DAC47756.2020.9045559 https://github.com/scale-lab/DRiLLS
4. https://rlpvlsi.ece.virginia.edu/sites/rlpvlsi.virginia.edu/files/Calhoun_ISCAS2009subvt_slides.pdf
5. https://www.research-collection.ethz.ch/bitstream/handle/20.500.11850/338279/S3S_Quentin.pdf?sequence=1&isAllowed=y
6. https://github.com/lnis-uofu/LSOracle https://lsoracle.readthedocs.io/en/master/
7. https://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.9.5435&rep=rep1&type=pdf
8. https://arxiv.org/abs/2001.01808 https://github.com/ksettaluri6/AutoCkt
9. https://sci-hub.st/10.1109/VLSI-SoC.2012.7332104
10. https://archive.ll.mit.edu/HPEC/agendas/proc10/Day1/PA12_Grossmann_abstract.pdf
11. https://core.ac.uk/download/pdf/232133726.pdf
12. https://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.712.687&rep=rep1&type=pdf
13. https://res.mdpi.com/d_attachment/jlpea/jlpea-08-00014/article_deploy/jlpea-08-00014.pdf https://www.synopsys.com/dw/ipdir.php?ds=smart-data-fusion-subsystem
14. https://swarup.ece.ufl.edu/papers/J/J28.pdf
15. https://sci-hub.st/10.1145/1146909.1147022

Additional Links

1. https://www.truechip.net/articles-details/low-power-design-techniques-basics-concepts-in-chip-design/26234
2. https://www.techdesignforums.com/practice/guides/subthreshold-near-threshold-computing-logic-ntv/
3. https://www-cnx--software-com.cdn.ampproject.org/c/s/www.cnx-software.com/2021/08/22/ultra-low-power-risc-v-system-on-chip-features-adaptive-body-biasing-technology/?amp=1
4. https://www.techdesignforums.com/practice/technique/sub-threshold-circuit-techniques-to-iot-device-design/
5. https://www.edn.com/sub-threshold-design-a-revolutionary-approach-to-eliminating-power/
6. http://iis-projects.ee.ethz.ch/index.php/Standard_Cell_Compatible_Memory_Array_Design
7. https://rlpvlsi.ece.virginia.edu/project-type/energy-efficient-circuit-design
8. https://mtlsites.mit.edu/researchgroups/icsystems/pubs/conferences/2004/aliwang_isscc2004_paper.pdf

Thank you!

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