1.

(a)

```
set_multicycle_path 2 -start -from CLK1 -to CLK2
set_multicycle_path 1 -hold -start -from CLK1 -to CLK2
```

(b)

```
set_multicycle_path 4 -setup -end      -from CLK1 -to CLK2
set_multicycle_path 3 -hold -end       -from CLK1 -to CLK2
```

2.

(2)

```
program automatic RAND_NUM(input clk,INF.RAND_NUM inf);


    class random_num;
        rand reg[5:0] num;
        constraint num_cons{
            (enable==0)->num inside{0}
            (enable==1&&mode==0) num inside{[1:31]}
            (enable==1&&mode==1) num inside{[32:63]}
        }
    Endclass

    random_num num_test = new();
    int i;

    initial begin
        always@(posedge clk)begin
            i = num_test.randomize();
            Inf.ans = i;
        end
    end
endprogram
```

(2) 0810121 李裕祥

(a) When the FIFO memory is full, the wfull pin will become High. voltage, it mean should input data anymore, and when FIFO memory is empty, the rempty will become. High voltage, it mean shouldn't read out another data anymore.

(b) When using gray code, the probability of error can be reduce, and also the time to shift the bits can also be reduced.

(c) this can let the synthesizer don't optimize the synchronizer, because if it optimize with other cell, may lead to some error.

2.

(1) (a) program can be executed in reactive region, and only initial block is allow.

(b) struct is used to group a set of signal, and each occupy spaces, but union only single piece of storage, it just can be used to represent different types that had been defined.

(2)

在第一頁.

3.

(1)

because the coverage will be update when the sample event ocuur, so there is no need to write the sample part, just delete. the whole always_ff block. can be correct.

(2)

(a) assert property (@(posedge clk)

A===0 |->##[2:$] B===1).

else $fatel;

(b) assert property (@(posedge clk)

(A===1) |-> (post(B,5).===1.[2*])).

else $fatel;

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4.

(a) static power = ① reduce the Vt, so the leakage can be reduce, ② reduce VDD, so the power can be reduce because P=IV.

dynamic power = ① clock gating, because clock gating can reduce some latch togling ② multi voltage, when a block switch between different voltage, when low voltage the power can be reduce.

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(b)

because OR gate will fie output to high when sleep, then the. Flip Flop that connect to the output will not consume a lot power because the latch inside will not togle.

(c).

VCD file contain the time when the signal change.

SAIF file has the time information and togle count, just like cumulative information of VCD.

If want to analysis peak power should use VCD, because it has the information of when signal change.

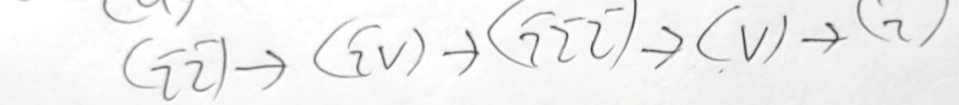
5.

(1) because there will be some optimize after CTS.

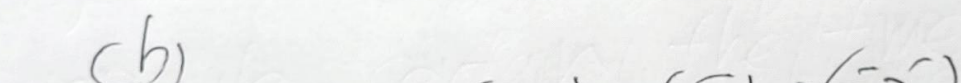
(2) ① layer switching
② wiring spacing

(3)

(a)



(b)



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6.

(a) IR drop because wire resistence, can add more power pad, or let the strip became more.

(b) rail analysis is a method to analysis IR drop.
power analysis is analysis the power of whole chip

7.

(a) SEC use formal engine to test different input, check whether to design have the same function.

(b)
waive can be use to waive clock gating enable pairs.