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| To be filled by Student | | | | |
| **Course** | Computer Organization and Architecture Lab | | | |
| **Course Instructor** | Dr. Saeed Ur Rehman | | **Lab Instructor** | Miss Ayesha Sadiq |
| **Student Name(s)** | **Hamza Umar** (FA19-BCE-007), **Muhammad Kaleem Ullah** (FA19-BCE-007) | | | |
| **Project Title** | Implementation of SAP-1 In Verilog | | | |
| **Project Proposal Summary** | The Simple-As-Possible (SAP)-1 computer is a very basic model of a microprocessor explained by Albert Paul Malvino. The SAP-1 design contains the basic necessities for a functional microprocessor. Its primary purpose is to develop a basic understanding of how a microprocessor works, interacts with memory and other parts of the system like input and the output. The instruction set is very limited and is simple as possible. | | | |
| Recommendations by Instructor | | | | |
| Range of Complex  Problem Solving | Range of Conflicting Requirements |  | | |
| Depth of Analysis Required |  | | |
| Depth of Knowledge Required |  | | |
| Interdependencies |  | | |
| Range of Complex Problem Activities | Range of Resources |  | | |
| Level of Interactions and Innovations |  | | |
| Familiarity |  | | |