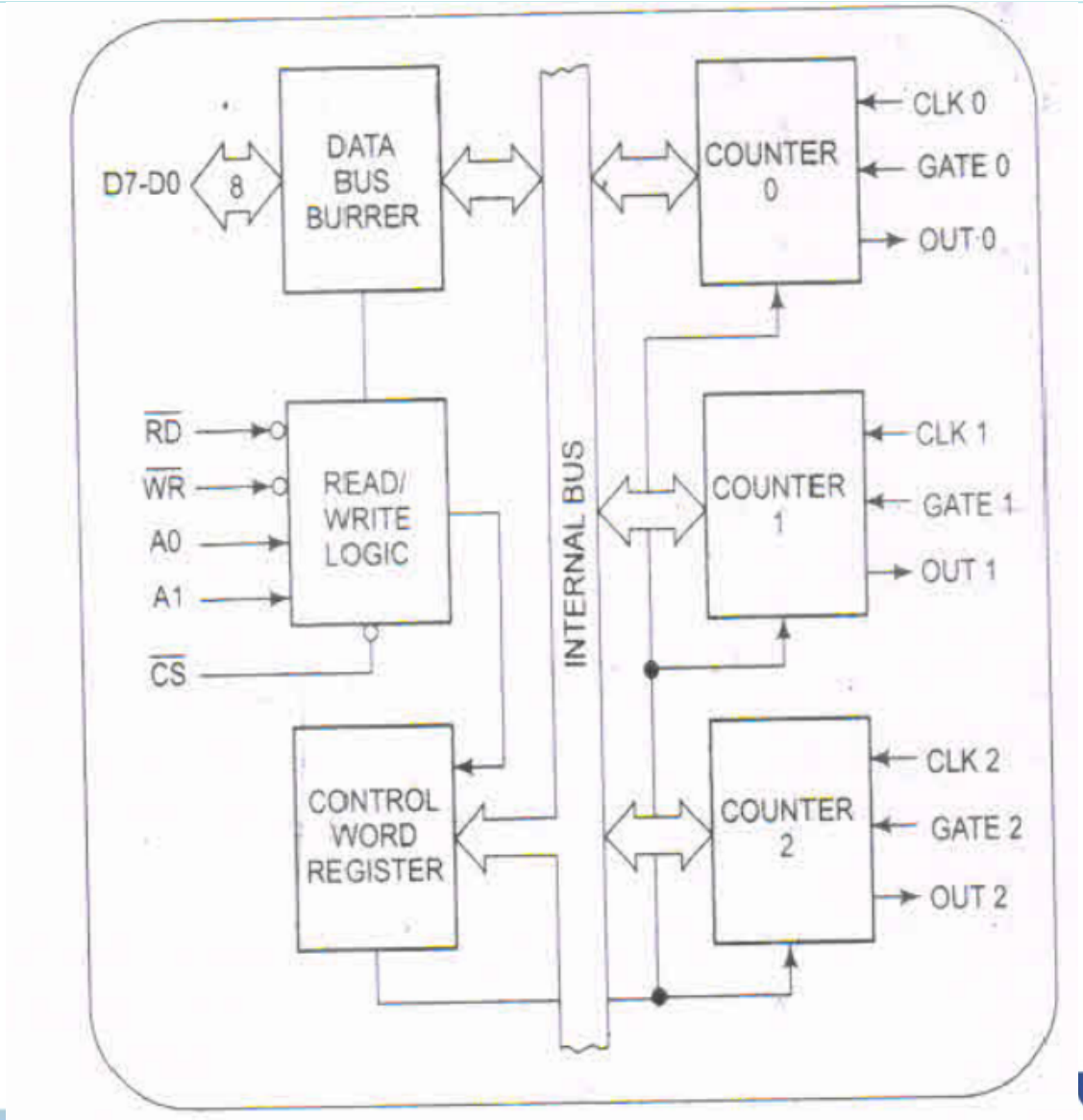
Interfacing

8253/8254 Software Programmable Timer/ Counter

8254 - software programmable timer/ counter

- Three counters
- different modes of operation
- 8253/ 8254 - identical in function with similar pin details
- 8253/8254 - differs in maximum input clock frequency
- 8254 has Read-back feature - latch the value in all the counters and their status at any point
- Software programmable - loading the count value, start and stop are done with instructions
- programmable - count and control bytes are sent to the port similar to how data can be sent to the port

8254 internal block diagram



- clock frequency - upto 8 MHz
- GATE input to each counter - start or stop the counter with an external hardware signal
- Gate input high - counter is enabled
- Gate input low - counter is disabled
- OUT pin - output signal from each counter

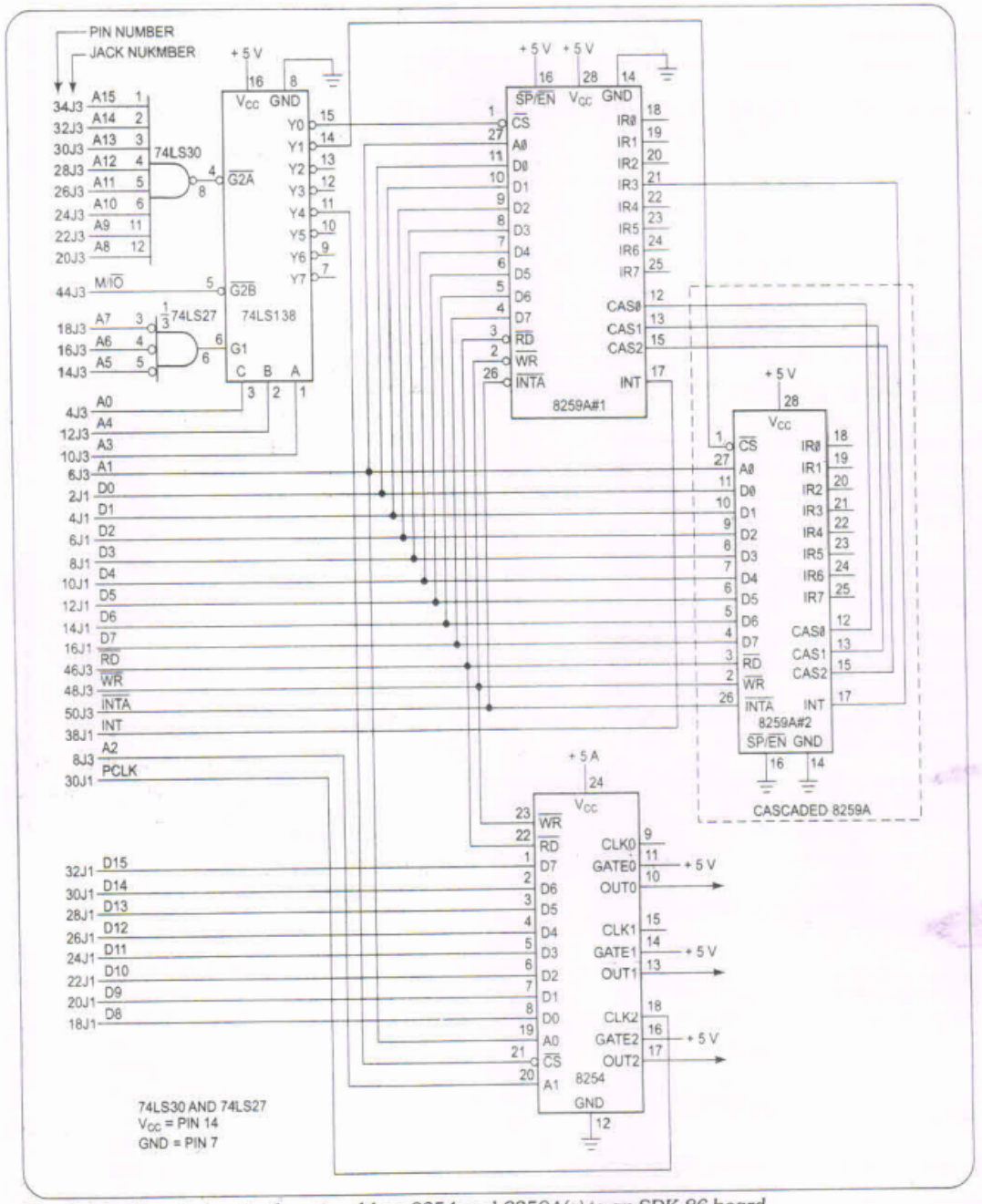


Fig. 8.14 *Circuit showing how to add an 8254 and 8259A(s) to an SDK-86 board.*

- Address decoder - 74LS138 - produces chip select signals to 8254, 8259 and other I/O devices
- only one of the output pins are asserted at any moment
- peripheral devices have only 8 data lines
- for an odd-addressed device, data lines are connected to the upper 8 system data lines
- for an even-addressed device, data lines are connected to the lower 8 system data lines

A8-A15	A5-A7	A4	A3	A2	A1	A0	M/IO	Y OUTPUT SELECTED	SYSTEM BASE ADDRESS	DEVICE
1	0	0	0	X	X	0	0	0	FF00	8259A#1
1	0	0	1	X	X	0	0	1	FF08	8259A #2
1	0	1	0	X	X	0	0	2	FF10	
1	0	1	1	X	X	0	0	3	FF18	
1	0	0	0	X	X	1	0	4	FF01	8254
1	0	0	1	X	X	1	0	5	FF09	
1	0	1	0	X	X	1	0	6	FF11	
1	0	1	1	X	X	1	0	7	FF19	
ALL OTHER STATES								NONE		

Truth table for 74LS138 address decoder in Figure 8.14.

Initialising 8254

- Find the system base address from the address decoder table (base address of 8254 is FF01 H as given in the Address decoder TT)
- Determine the Internal address for each of the ports, timers, control registers and status registers from the device data sheet
- Add internal address to the system base address to find the system address
- This is the actual address where we need to send control words, timer values
- Odd address indicate the device is connected on the upper half of the data bus

- control words/command words/mode words
- to initialise 8254, send control word to the control register for each counter
- starting count value is also sent to the control registers for each counter a separate count value has to be sent
- Three counters - one control word register - control words for all the three counters are sent to the same address
- All the three counters are down counter
- count value for each counter may be BCD or binary
- Largest number to be loaded in binary is FFFF H
- largest number to be loaded in bcd is 9999

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC–SELECT COUNTER:

SC1	SC0	
0	0	SELECT COUNTER 0
0	1	SELECT COUNTER 1
1	0	SELECT COUNTER 2
1	1	READ-BACK COMMAND (SEE READ OPERATIONS)

RW–READ/WRITE:

RW1	RW0	
0	0	COUNTER LATCH COMMAND (SEE READ OPERATIONS)
0	1	READ/WRITE LEAST SIGNIFICANT BYTE ONLY.
1	0	READ/WRITE MOST SIGNIFICANT BYTE ONLY.
1	1	READ/WRITE LEAST SIGNIFICANT BYTE FIRST, THEN MOST SIGNIFICANT BYTE.

M –MODE:

M2	M1	M0	
0	0	0	MODE0 – INTERRUPT ON TERMINAL COUNT
0	0	1	MODE 1 – HARDWARE ONE-SHOT
X	1	0	MODE 2 – PULSE GENERATOR
X	1	1	MODE 3 – SQUARE WAVE GENERATOR
1	0	0	MODE 4 – SOFTWARE TRIGGERED STROBE
1	0	1	MODE 5 – HARDWARE TRIGGERED STROBE

BCD:

0	BINARY COUNTER 16-BITS
1	BINARY CODED DECIMAL (BCD) COUNTER (4 DECADES)

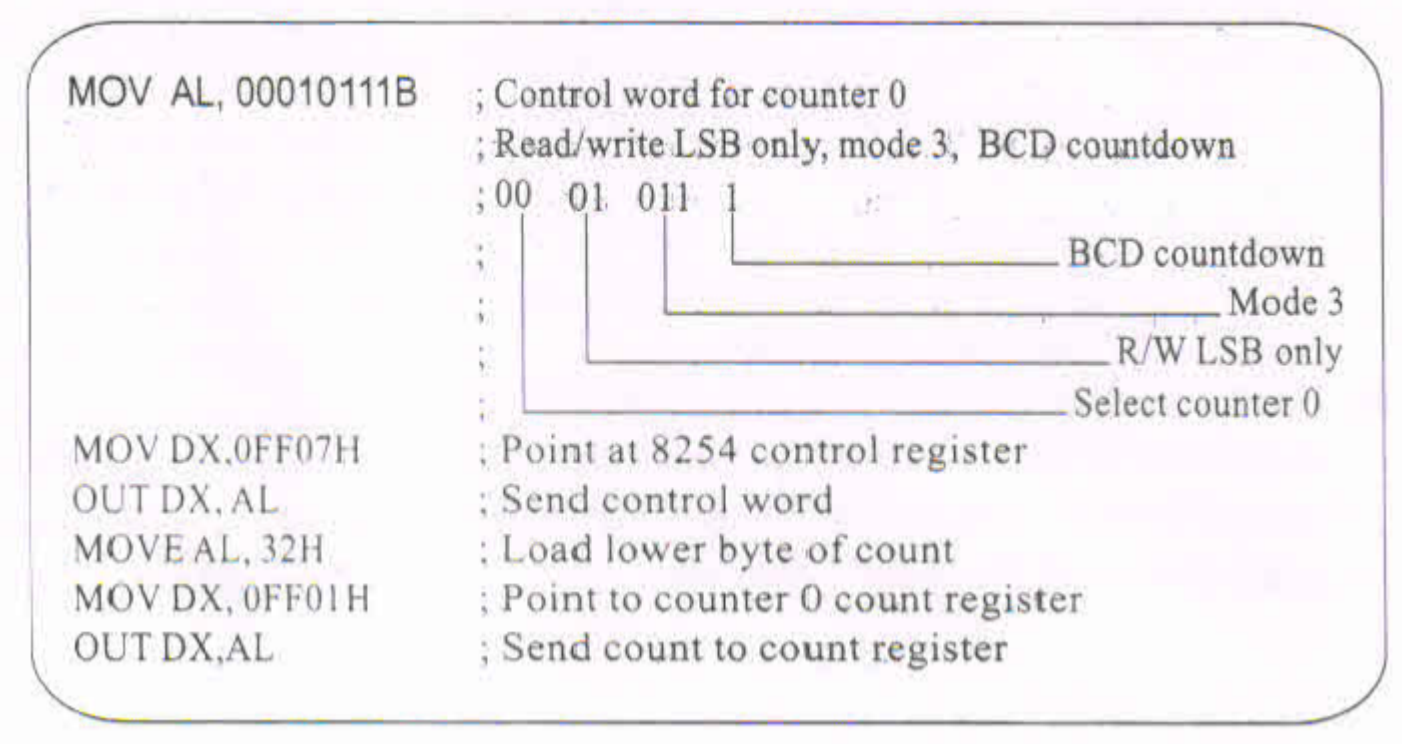
NOTE: DON'T CARE BITS (X) SHOULD BE 0 TO INSURE COMPATIBILITY WITH FUTURE INTEL PRODUCTS.

- The values in M2, M1, M0 specifies the effect that gate input will have on counting and the waveform that will be produced on OUT pin.
- Mode 3 - square wave mode - output will be high for first half of the loaded count and low for the second half of the loaded count
- When the count reaches zero the original count is automatically reloaded and the count down repeated.
- Eg: Use counter 0 of the 8254 to produce a stable square wave signal (mode 3)

MOV AL, High byte of the count

OUT DX, AL

- High byte and low byte of the count should be sent to the same address



```
MOV  AL, 00010111B    ; Control word for counter 0
                      ; Read/write LSB only, mode 3,  BCD countdown
                      ; 00   01   011   1
                      ;                 |__ BCD countdown
                      ;                 |___ Mode 3
                      ;                 |____ R/W LSB only
                      ;                 |_____ Select counter 0
MOV DX,0FF07H         ; Point at 8254 control register
OUT DX, AL            ; Send control word
MOVE AL, 32H          ; Load lower byte of count
MOV DX, 0FF01H        ; Point to counter 0 count register
OUT DX,AL             ; Send count to count register
```

Steps to initialise any programmable peripheral device

1. Find the system base address
2. Find the internal addresses for each of the control registers, ports, timers, status registers.
3. Add each of the internal addresses to the system base address to determine the system address of each of the parts of the device
4. Select the format of the control word
5. Construct the control word required to initialise the device
6. Send the control word to the control register address for the device

COUNTER MODES

MODE 0 - INTERRUPT ON TERMINAL COUNT

MODE 1 - HARDWARE RETRIGGERABLE ONE-SHOT

MODE 2 - TIMED INTERRUPT GENERATOR

MODE 3 - SQUARE WAVE MODE

MODE 4 - SOFTWARE TRIGGERED STROBE

MODE 5 - HARDWARE TRIGGERED STROBE

Read the count from an 8254 counter

Counters in an 8254 have latches on their output

Reading the count from counter = reading the data on the outputs of latches

A strange value will be read if we count while the counter is counting

To read the count value - stop counting and latch the count value

3 ways of stop counting -

- turn off the clock signal or making the GATE input low
- latch the current count with a counter latch command, then read the latched count
- A counter is latched by sending a control word to control register address in 8254
- To latch the counter - RW1 and RW0 bits zero
- SC1 and SC0 - which counter to latch
- lower 4 bits of the control word are 0 (don’t cares)

The sequence of instructions to latch and read the LSB and MSB from counter 1 of 8254

```
MOV AL, 01000000 B; Counter1 latch command
MOV DX, 0FF07 H; point at 8254 control register
OUT DX, AL; send latch command
MOV DX, 0FF03 H; point at counter 1 address
IN AL, DX; read lsb
MOV AH, AL; save lsb
IN AL, DX; read msb
XCHG AH, AL; count in AX
```

Reading the count - third way - only in 8254 read back command

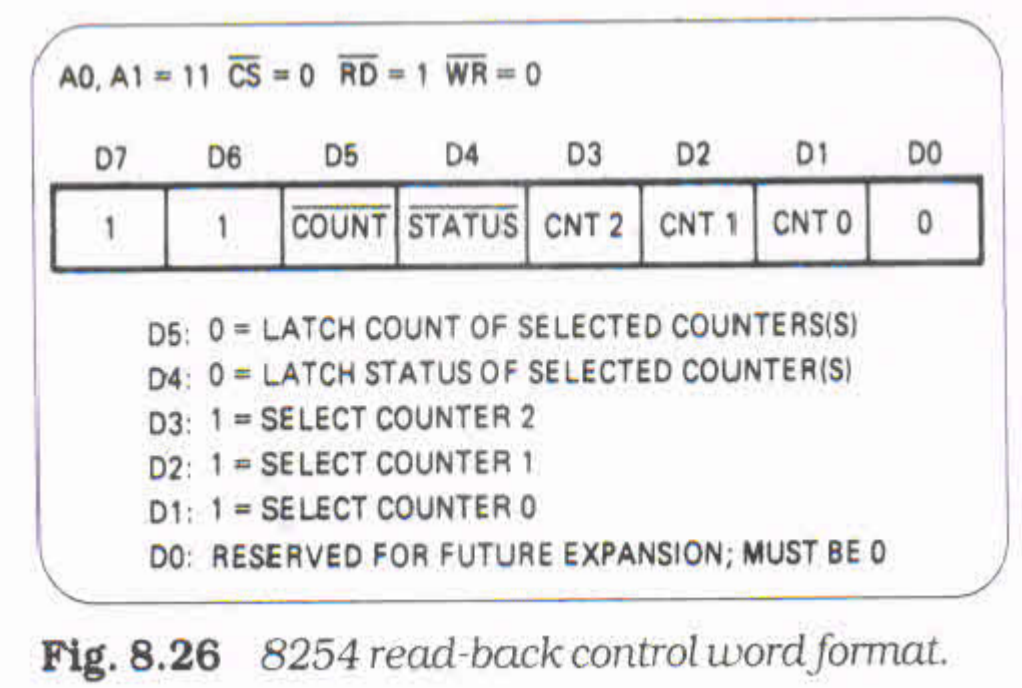


Fig. 8.26 *8254 read-back control word format.*

- D7 and D6 bits identify read back command and it is set to 1
- bit D5 of the control word = 1 ; to latch the count
- Latch one or more counters by placing 1 in the appropriate bit
- Once a counter is latched, the count is read