Interfacing

8259A Priority Interrupt Controller

8259A - Priority Interrupt Controller

- Interrupt - break the sequence of operation
- A program is being executed, interrupt occurs, the execution sequence is altered and it gets transferred to Interrupt service routine (a sub-program or procedure like) and returns back to the main program execution flow.
- 8086 - 2 pins for interrupt, NMI (non-maskable interrupt) and INTR (256 types)

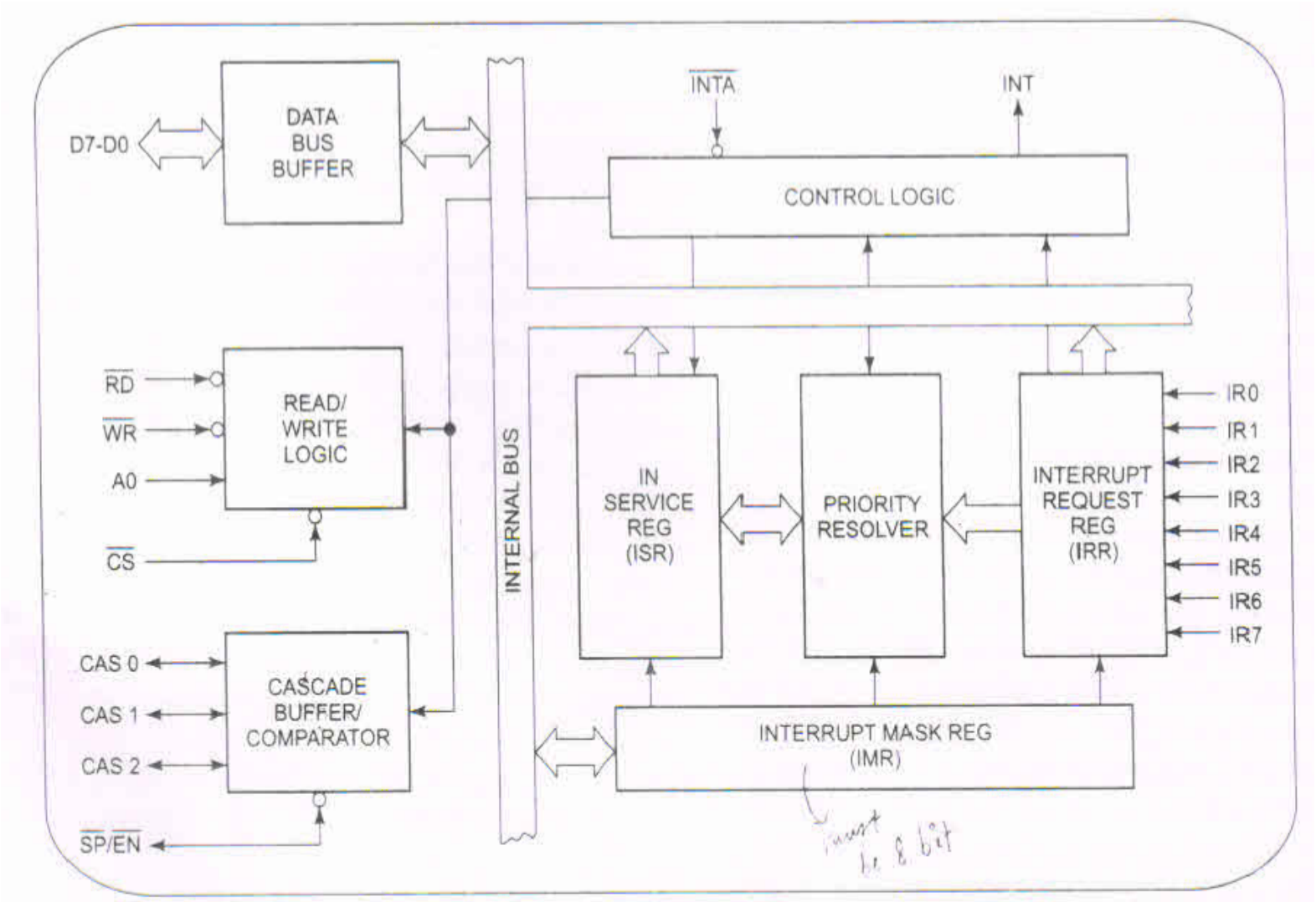
8259A - Priority Interrupt Controller

- Any interrupt signal to NMI, it cannot be disabled
- If more than one type of INTR input occurs at a time, then 8259 is needed to resolve them
- Interrupts -
- Read ASCII characters in from a keyboard (external interrupt)
- Count interrupts from a timer to produce a real time clock of secs, mins, hrs
- Each of the interrupt applications requires a separate interrupt input
- Internal interrupt - divide by zero, overflow, INT instructions

Interrupt response of 8086

If the Interrupt flag is set and the INTR input is high, then 8086 responds as follows.

- Sends 2 INT acknowledge signals through INTA pin to 8259 A
- 8259 sends the interrupt type signal to 8086
- Multiply by 32 and get the address from the Interrupt vector table
- Push all flags
- Clear IF, TF
- Push return address on stack
- Get the starting address for the interrupt procedure from IVT and load them in CS and IP
- Execute Interrupt service procedure


D7-D0
DATA BUS BUFFER
INTA
INT
CONTROL LOGIC
RD
WR
A0
CS
READ/ WRITE LOGIC
INTERNAL BUS
IN SERVICE REG (ISR)
PRIORITY RESOLVER
INTERRUPT REQUEST REG (IRR)
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CAS 0
CAS 1
CAS 2
CASCADE BUFFER/ COMPARATOR
INTERRUPT MASK REG (IMR)
SP/EN

8259A - Priority Interrupt Controller

- Interrupt inputs - 8 (IR0 to IR 7)
- If any pin out of this 8 goes high, and if the IF is set, then 8259 sends an INT signal to 8086 and 8086 responds with Interrupt service sequence.
- 8259 funnels interrupt signals from 8 sources into the 8086 INTR input
- For each of the 8 interrupt inputs of 8259, it sends the interrupt type to 8086

8259A - Priority Interrupt Controller

- What if 2 Interrupt pins goes high at the same time ? IR2 and IR4
- Fixed priority mode - IRO has highest priority and IR1 next highest priority ..
- If two interrupts are enabled, it will service the highest priority interrupt
- In 8259 - Interrupt Request Register(IRR), Interrupt Mask Register(IMR), Inservice Register(ISR), Priority Resolver(PR)

8259A - Priority Interrupt Controller

- IMR - enable or disable individual interrupt inputs
- IRR - keeps track which interrupt is asking for service
- ISR - keeps track of which interrupt inputs are currently being serviced
- PR - determines if and when an interrupt request on one of the IR inputs gets serviced

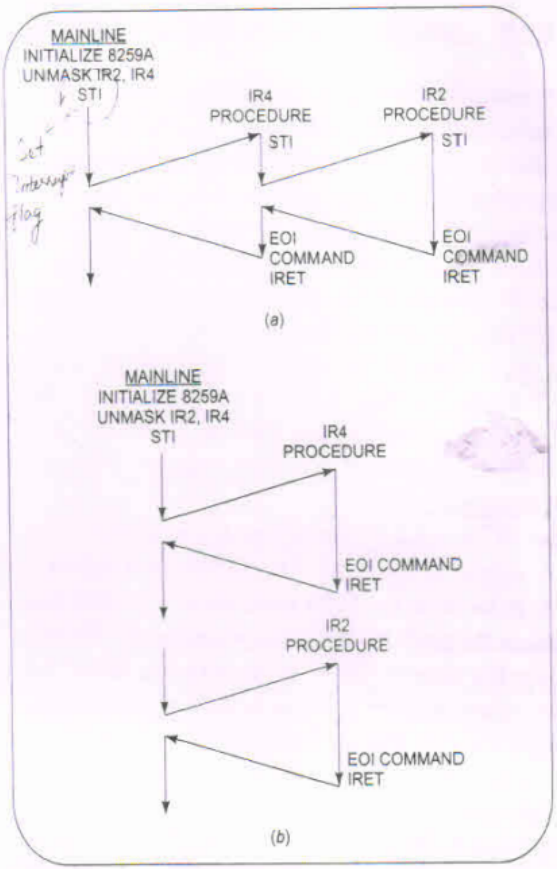


Fig. 8.28 *8259A and 8086 program flow for IR4 interrupt followed by IR2 interrupt. (a) Response with INTR enabled in IR4 procedure (b) Response with INTR not enabled in IR4 procedure.*