University of Rajshahi
Department of Computer Science and Engineering
B.Sc. Engg.(CSE) 1st Year EVEN Semester 2016
Course: CSE1211 (Introduction to Digital Electronics)
Time: 3 Hrs. Full Marks: 52.5
[N.B. Answer SIX questions taking at least THREE from each Section.]

Part A

1. (a) Convert $(1001010.1101001)_2$ to base 16 and $(231.07)_8$ to base 10. 2
   (b) Realize XOR gate using only 4 NAND gates. 1
   (c) Construct a 4-bit odd parity generator circuit using logic gates. 3.75
   (d) Represent $(-200)_{10}$ using 2's complement binary form. 2

2. (a) What are min terms and max terms? 2
   (b) Design a combinational circuit to convert BCD code to excess-3 code. 3.75
   (c) Convert the following function into sum of product form: (AB+C)(B+C'D) 1
   (d) Subtract $(1011)_2$ from $(0100)_2$ using 2's complement method. 2

3. (a) A small process-control computer uses hexadecimal codes to represent its 16 bit memory address. Answer the following: 3
   (i) How many Hex digits are required? (ii) Write the range of addresses in binary and in Hex. (iii) In Hex, how many memory locations are there?
   (b) Design a logic circuit that will allow a signal to pass to the output only when control inputs B and C are both HIGH; otherwise the output will stay LOW. 1
   (c) You have to design a logic circuit that controls an elevator door in a two-story building. Consider a logic signal say O that indicates when the elevator is moving (O=1) or stopped (O=0). A_1 and A_2 are floor indicator signals that are normally LOW, and they go HIGH only when the elevator is positioned at the level of that particular floor. Draw the truth table for open and from it, write the logic expression and design the logic circuit. (For example, when elevator is lined up with the first floor, A_1 =1 and A_2 =0. The circuit output is the open signal, which is normally LOW and will go HIGH when the elevator door is to be opened) 4.75

4. Simplify the following Boolean function using Quine-McClusky method F = (A, B, C, D, E)= $\sum$ m (0, 1, 3, 7, 8, 13, 14, 21, 26) + $\sum$ d (2, 5, 9, 11, 17, 24). 8.75

Part B

5(a) Explain the master slave J-K flip-flop with timming diagram in detail. 7
   (b) What is setup and hold times? 1.75

6(a) Define the following terms: 2.75
   (i) Fan in and fan out
   (ii) Noise immunity
   (b) Design a TTL NAND gate circuit and beriefly explain its operation. 3
   (c) Design the circuit diagram of DTL-NAND gate and beriefly explain its operation. 3

7(a) What is sampling and quantization? What are the applications of ADC and DAC? 3
   (b) An R/2R ladder DAC has binary input of 1001. If a HIGH = +5.0 V and a LOW = 0.0V, what will be equivalent analog output? 2
   (c) Draw the block diagram of a successive approximation ADC and explain its working principal with a suitable example. 3.75

8(a) Write the funtions of each pin of 555 timer. 2.75
   (b) Design an astablemultivibrator using 555 timer and explain its operation. 4
   (c) An Astable 555 multivibratoris constructed using the following components, R1 = 1kΩ, R2 = 2kΩ and capacitor C = 10μF. Calculate the output frequency from the multivibrator and the duty cycle of the output waveform. 2

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. Engg. Part-I Even Semester 2015
Course: CSE1211 (Introduction to Digital Electronics)
Time: 3 Hrs. **Full Marks: 52.5**
[N.B. Answer SIX questions taking at least THREE from each Section.]

Part A

1. (a) Do the following conversions: 4
   i) $(378)_{10}$ to 16 bit binary number;
   ii) $(1010110.1100)_2 = (?)_{10}$;
   iii) $(10101100)_2 = (?)_8$;
   iv) $(743)_{16} = (?)_2$.
   (b) Compare between BCD and Binary code. 2
   (c) What is Gray code? Explain with examples, how do you convert binary to Gray and Gray to binary? 2.75

2. (a) Subtract $(100111)_2$ from $(001100)_2$ using 2's complement method. Why do you need 2's complement method? 2
   (b) Apply the input waveforms of fig-1 to a NOR gate, and draw the output waveform. Then repeat the output waveform with C hold permanently LOW. 2

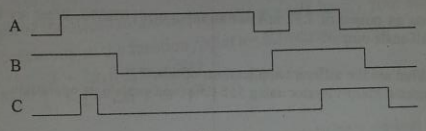

Fig-1

   (c) Determine the truth table for the circuit of fig-2. 2

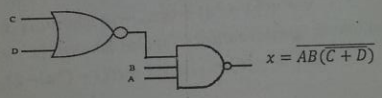

Fig-2

   (d) Show that a two-input NAND gate can be constructed from two-input NOR gate. Simplify the following: $(\overline{A+B})(\overline{\bar{A}+\bar{B}})$ 2.75

3. (a) What is DeMorgan's theorem? Explain with truth table. 2.75
   (b) Simplify the expression $x = \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC + A\bar{B}\bar{C} + A\bar{B}C$ using Boolean algebra. 2
   (c) Minimize the Boolean function f(a,b,c,d) $= \sum_M(1,4,6,8,10)$ 4

4. (a) Simplify the following expression using K-map method 5
   f(A,B,C,D) $= \sum_M(7, 9, 10, 11, 12, 13, 14, 15)$
   (b) Design the circuit corresponding to the truth table shown in Table-1. 3.75

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table-1

Part B

5. (a)	Explain the clocked S-R flip-flop in detail.	6
(b)	Explain D type flip-flop.	2.75
6. (a)	Draw the basic DTL gates to implement NAND gate. Explain its operation.	2
(b)	Discuss the characteristic of TTL gates. Explain the operation of open collector TTL gates.	2.75
(c)	Where ECL is more suitable? Draw and explain ECL to implement OR and NOR gates.	4
7. (a)	Define transducer, analog-to-digital converter (ADC) and digital-to-analog converter (DAC).	3
(b)	Draw the basic R/2R ladder DAC of 4-bit and write the V_{OUT} expression.	2
(c)	Assume the V_{REF} =5V for the 4-bit DAC. What are the resolution and full-scale output of this converter?	1.75
(d)	An 8-bit DAC has an output of 3.92 mA for an input of 01100010. What are the DAC's resolution and full-scale output?	2
8. (a)	What is timer? What are the different applications of timer?	3
(b)	Design an monostable multi-vibrator using 555 timer and explain its operation.	5.75

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. Engg. (CSE) Part-1 Even Semester Exam-2014
Course: CSE 1211 (Introduction to Digital Electronics)
Full Marks:52.5 **Time: 3 Hours**

[N.B. Answer SIX questions taking THREE from each part]

Part-A

1. (a) Do the following conversions: 4
   (i) $(10101011.1101)_2=(?)_{10}$ (ii) $(20345.125)_{10}=(?)_2$ (iii) $(80914.25)_{10}=(?)_8$
   (iv) $(3AE8F.2D)_{16}=(?)_8$ (v) $(1011001110)_2=(?)_4$
   (b) Add $(110111)_2$ with $(100111)_2$. Subtract $(100110)_2$ from $(110011)_2$ using 2's complement method. 3
   (c) Represent $(-17)_{10}$ in sign magnitude, 1's complement and 2's complement representation. 1.75

2. (a) Write the procedure to convert a binary code to gray code with example. 4
   (b) With the help of example explain excess-3 code. 3
   (c) Write the BCD code for $(9248)_{10}$. 0.75
   (d) How can you easily generate 3 bit gray code . 1

3. (a) Define and draw the truth table of a 3-input X-OR gate. 2.75
   (b) Show that NAND gate can be used as universal gate. Simplify the following using De-Morgan's theorem 3
   $\overline{\left(A+\overline{B}\right)}\overline{\left(\overline{A}+B\right)}$
   (c) Simplify the following Boolean expressions to a minimum number of literals: 3
   (i) $ABC+A'B+ABC'+AC$ (ii) $A'B(D'+CD)+B(A+A'CD)$

4. Simplify the following logic function using Quine-McCluskey technique 8.75
   $f(A,B,C,D)=\sum m(0,1,3,7,8,9,11,15)$

Part-B

5. (a) Write the difference between asynchronous and synchronous system. 1.75
   (b) Explain the operation of a positive-edge triggered SR flip-flop by timing diagram. 4
   (c) Discuss how an SR latch is converted into D-latch. 3

6. (a) Explain the operation of a JK flip-flop using timing diagram. 3.75
   (b) Mention the limitations of a JK flip-flop. 2
   (c) Describe how a D-latch operates differently from an edge-triggered D flip-flop. 3

7. (a) Discuss the operation of an 8-bit DAC using op-am summing amplifier with binary weighted registers. 3
   (b) Define R/2R ladder DAC with basic circuit diagram. Write the benefits of R/2R circuit. 3
   (c) Briefly discuss the operation of the digital ramp ADC. 2.75

8. (a) Draw the block diagram of a 555 timer and explain about its each pin. 3
   (b) Design an astable multi-vibrator using 555 timer and explain its operation. 5.75

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. (Engg.) Examination-2013, Year-I, Semester-II
Course: CSE-1211 (Introduction to Digital Electronics)
Full Marks-52.5 Time: 3 hours

[N.B. Answer any six questions taking THREE from each of the groups]

Part-A

1. a) Convert 1001.1001 into decimal. Perform the 2's complement operation on $(10100)_2$. 3
   b) What are the advantages of Gray code? Convert the number $(0101)_2$ to ets Gray code equivalent. 3
   c) Subtract $(1011)_2$ from $(0101)_2$ using 1's and 2's complement method. 2.75

2. a) Define and draw the truth table of a 3-input X-NOR gate. 2.75
   b) Show that NOR gate can be used as universal gate. Simplify the following using De Morgan's theorem $\overline{(M+\bar{N})}(\bar{M}+N)$. 3
   c) Define Active LOW and Active HIGH with necessary diagram. 3

3. a) Minimize the Boolean function f(a, b, c, d)=$\sum_M(1, 3, 6, 8, 10)$. 4
   b) Minimize the following function using Quine-Mc Cluskey method (up to level one): f(a, b, c, d)= $\sum_M(0, 1, 2, 4, 6, 8, 12, 14)$. 4.75

4. a) What do you mean by fan in and fan out? 2.75
   b) Draw the circuit diagram of DTL-NAND gate. 3
   c) Design a NOT gate using MOSFET. 3

Part-B

5. a) Explain the operation of NAND gate latch with its logic circuit and typical waveform. 4
   b) What is the difference between asynchronous and synchronous system. 2.75
   c) Mention some application of FF. 2

6. a) How does the binary counter work as a frequency divider? 2
   b) What is the frequency of the output of 8th FF when the input clock frequency is 512 KHz? 1.75
   c) Design a full adder circuit. 5

7. a) Define Multiplexer. How can you design an eight-input MUX by using two 4-input MUX. 3
   b) What is the difference between DeMUX and decoder? 1
   c) Design a decimal weighted table in binary equivalent for a three-digit BCD number. Using the table convert 100100110101(BCD) to binary. 4.75

8. Write short notes (any three) from the following: 8.75
   a) Successive Approximation ADC
   b) Analog to Digital Conversion.
   c) TTL and METL.
   d) Shift Register.

University of Rajshahi
Dept. Of Computer Science and Engineering
B. Sc. Engg.(CSE) 1st Year Even Semester Examination 2012
Course: CSE 1211 (Introduction to Digital Electronics)
Full Mark: 52.5 Duration: 4 hours
Answer 6 questions taking at least 3 from each part

Part -A

1.	a)	What is coding? Discuss how parity bits can be used to detect error in bits.	2
	b)	Convert 146_{10} to octal, then from octal to binary.	1.75
	c)	Mention some advantages of using BCD compared to other coding.	1.5
	d)	Perform the 2's compliment operation on $(10000)_2$	1.5
	e)	Add the (1010+1011) in binary. Check your result by doing the addition in decimal.	2
2.	a)	What do you mean by minterm and maxterm?	1
	b)	Simplify the following Boolean expressions to a minimum number of literals: i) $ABC + A'B + ABC' + AC$ ii) $A'B(D' + CD) + B(A + A'CD)$	2
	c)	Minimize the following switching function using Quine-McCluskey method. $f(w,x,y,z) = \sum_m (0,1,2,4,5,6,8,9,12,13,14)$	5.75
3.	a)	Which gates are called Universal gate? Why?	2.75
	b)	Minimize the Boolean function $f(x_1,x_2,x_3,x_4) = \sum_m (0,5,7,8,9,10,11,14,15)$ using k-map.	4
	c)	State and prove De-Morgan's law.	2
4.	a)	Draw and explain the circuit operation of a 2-input TTL NOR gate.	3
	b)	Draw and explain the circuit operation of a 2-input CMOS NOR gate.	4
	c)	Write a short note on the ECL family.	1.75

Part -B

5.	a)	Explain the operation of a positive-edge triggered SR flip-flop by timing diagram.	4
	b)	How can you convert an SR latch into a D-latch?	3
	c)	Draw the circuit diagram of a master/slave JK flip-flop.	1.75
6.	a)	With the help of timing diagram, explain the operation of a clocked JK flip-flop.	3
	b)	What are the limitations of a JK FF?	2
	c)	Describe how a D flip-flop operates differently from an edge triggered D flip-flop.	3.75
7.	a)	Draw and explain the operation of 555 timer as astable multivibrator.	4
	b)	Briefly discuss a simple DAC using Op-Amp.	3
	c)	What is timer? Mention some applications of timer circuit.	1.75
8.	a)	What is the function of a transducer and actuator?	1.75
	b)	Draw the circuit diagram of R-2R ladder DA Converter.	1.5
	c)	Which factor affect DA conversion accuracy?	1.5
	d)	Define full scale error and settling time.	2
	e)	Briefly discuss the operation of the digital ramp ADC. Write its applications.	2

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. Engg.(CSE) 1st Year 2nd Semester 2011
Course: CSE 1211 (Digital Electronics-II)
Time: 4 Hrs. Full Marks: 52.5
[N.B. Answer SIX questions taking at least THREE from each part.]

PART-A

1. a) Draw the diagram of a NAND gate latch and show that it has two possible resting states when SET=RESET=1. — 2
   b) With the help of timing diagram, explain the operation of positive-edge triggered J-K flip-flop. — 3
   c) What are hold time and setup time? — 1.75
   d) Discuss the potential timing problem in FF circuits with necessary timing diagram. — 2
2. a) What is shift register? Discuss with timing diagram the operation of a four-bit shift register using J-K flip-flop. — 2.5
   b) Show that J-K flip-flop can be used as a binary counter. — 2.5
   c) What is free running multi-vibrator? Discuss the circuit operation of a 555 timer IC as a clock generator circuit. — 3.75
3. a) What is D latch? Describe how a D latch operates differently from an edge-triggered D flip-flop. — 3
   b) What is the impact of propagation delay between the transitions of a flip-flop? — 1
   c) Define shift-register. Construct two 3-bits shift registers X and Y, and show how the bits stored in register X are transferred to register Y with a shift pulse. Explain. — 4.75
4. a) What is priority encoder? Discuss the logic circuit for an 8-to-3 encoder with diagram. — 3
   b) Draw the circuit for keyboard entry of 2-digit number into storage register. — 2.75
   c) Discuss the circuit of a four-input multiplexer with function table and diagram. — 3

PART-B

5. a) Differentiate between asynchronous counter and synchronous counter. — 2
   b) Show that how the 74LS293 IC wired as a MOD-16 counter with a 10KHz clock input. Determine the frequency at Q_2. — 2
   c) What is the difference between the counting sequences of an up-counter and a down-counter? — 1.75
   d) Describe the circuit operation of a MOD-8 down-counter with timing diagram. — 3
6. a) Draw the logic diagram for a BCD-to-Decimal decoder. Give its logic symbol and truth table. Explain how it can be combined with a counter to provide timing and sequencing operations. — 6
   b) Can more than one decoder output be activated at one time? Explain. — 2.75
7. a) Discuss the operation of a 8-bit DAC using an op-amp summing amplifier with binary weighted registers. — 2
   b) What is R/2R ladder? What are the benefits of R/2R circuit? Draw the basic circuit of R/2R ladder DAC. — 3
   c) How a DAC can be used to control the amplitude of an analog signal? Discuss with diagram. — 2
   d) Draw the circuit diagram of digital RAMP ADC. — 1.75
8. Write short notes on the followings (any three): — 8.75
   a) Analog to digital conversion.
   b) Master/Slave flip-flops.
   c) BCD-to-7 segment decoder/driver.
   d) 1-to-8 line De-multiplexer.