Chapter 4
8085 Microprocessor Architecture and Memory Interfacing

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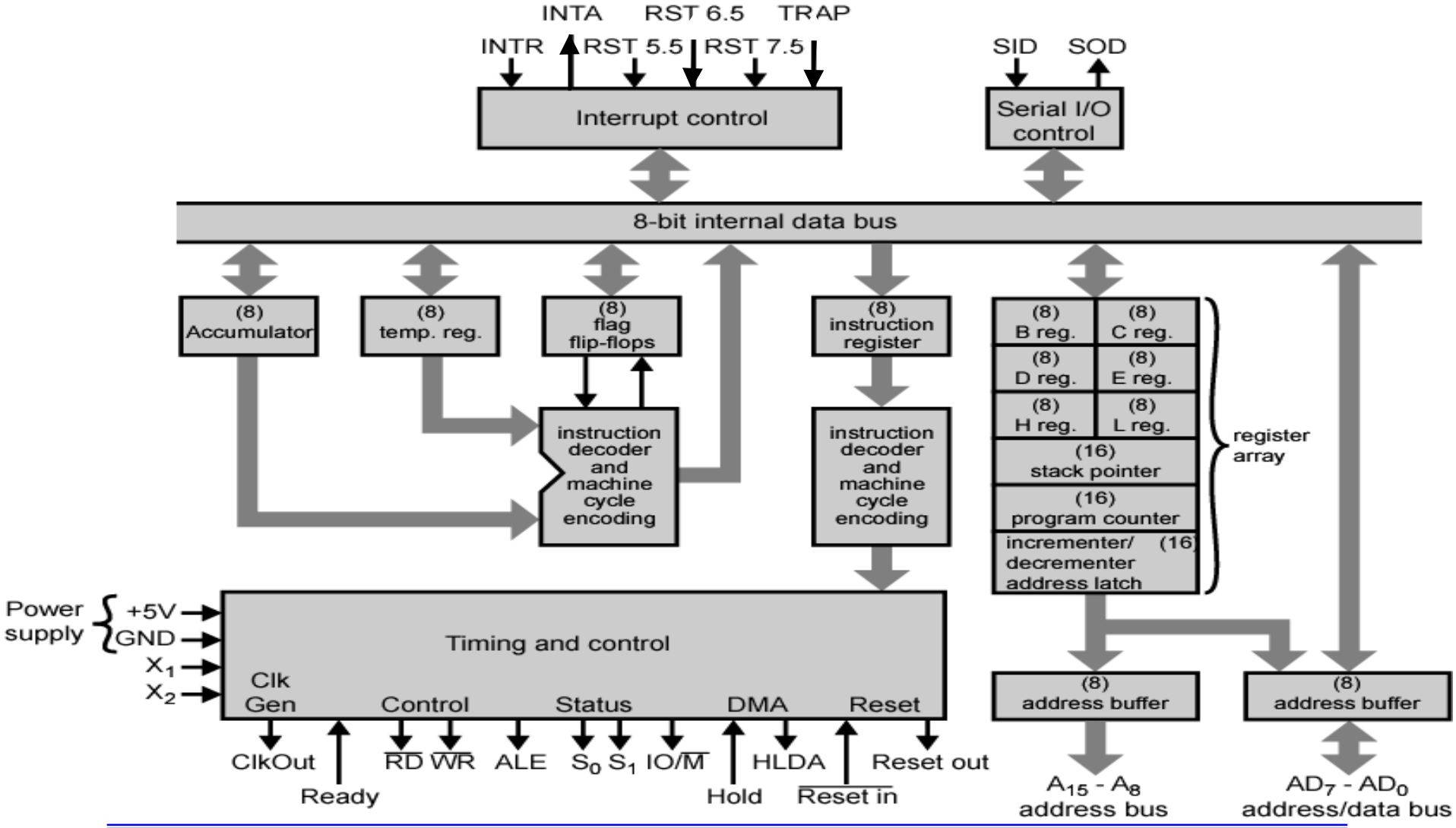
Points to be Discussed

- 8085 Microprocessor
- 8085 Microprocessor (CPU) Block Diagram
- Control & Status Signals
- Interrupt Signals
- 8085 Microprocessor Signal Flow Diagram
- 8085 Microprocessor Pin Diagram
- Demultiplexing the AD7 to AD0
- Generation of Control Signals
- 8085 Single-Board Microcomputer System
- Data Flow from Memory to MPU
- Instruction cycle, Machine cycle & T-state
- Timing Diagram for executing MVI A,32H
- Timing Diagram of Memory Read Cycle
- Timing Diagram of Memory Write Cycle
- Any Quarries?

8085 Microprocessor

- 8-bit Microprocessor.
- The device has 40 pins.
- Clock frequency = 3MHz.
- Internally crystal frequency is divided by 2. So to operate at 3MHz, crystal frequency must be 6MHz.
- 8085A-2 version supports clock frequency 0f 5MHz.
- 64K Byte addressable memory.

8085 Microprocessor (CPU) Block Diagram



Control & Status Signals

TABLE 4.1
8085 Machine Cycle Status and Control Signals

Machine Cycle	Status			Control Signals
	$IO/\overline{M}$	S_1	S_0	
Opcode Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt Acknowledge	1	1	1	$\overline{INTA} = 0$
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA} = 1$
Hold	Z	X	X	
Reset	Z	X	X	

NOTE: Z = Tri-state (high impedance)
X = Unspecified

Interrupt Signals

- 8085 µp has several interrupt signals as shown in the following table.

TABLE 4.2
8085 Interrupts and Externally Initiated Signals

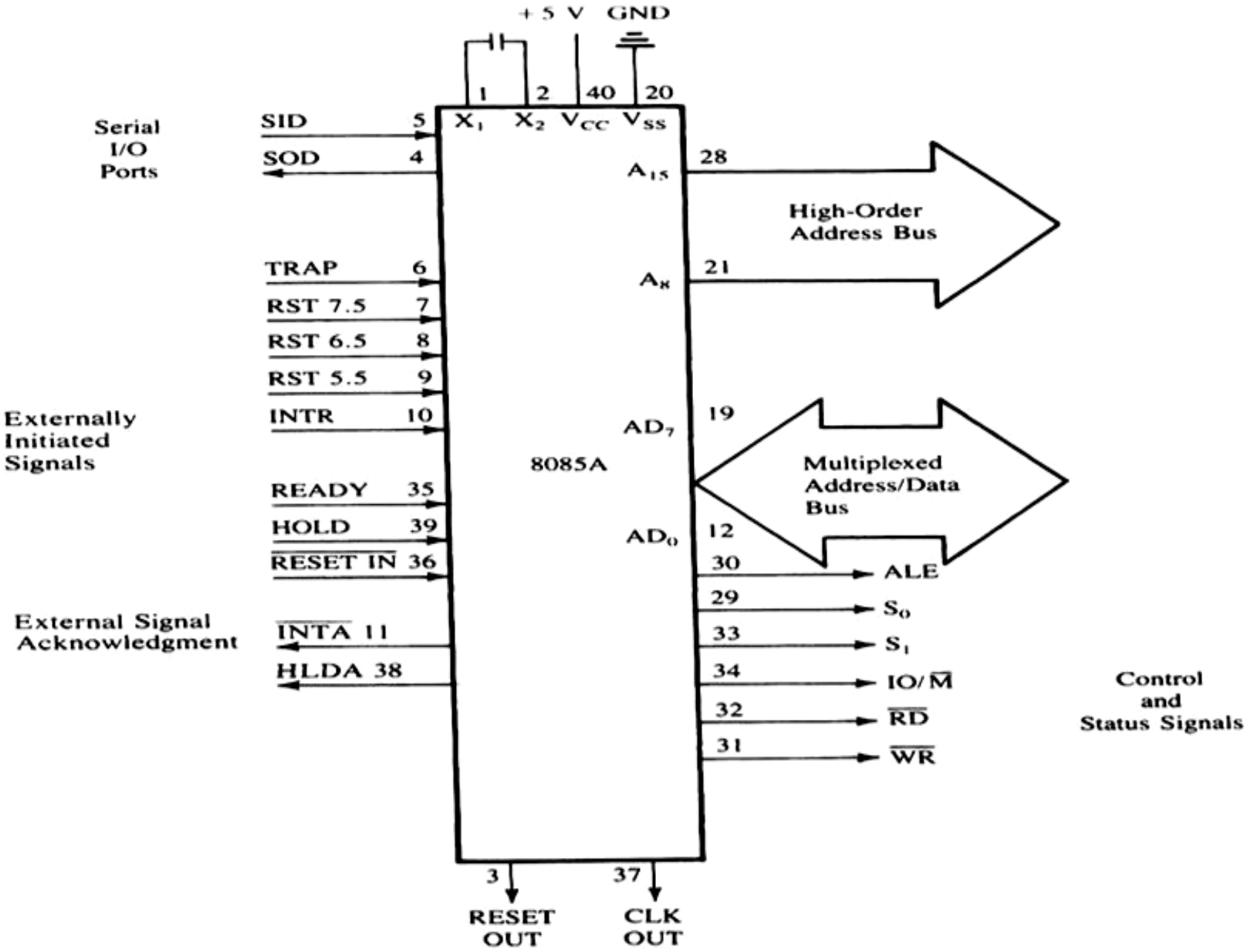
☐ INTR (Input)	Interrupt Request: This is used as a general-purpose interrupt; it is similar to the INT signal of the 8080A.
☐ $\overline{\text{INTA}}$ (Output)	Interrupt Acknowledge: This is used to acknowledge an interrupt.
☐ RST 7.5 (Inputs) RST 6.5 RST 5.5	Restart Interrupts: These are vectored interrupts that transfer the program control to specific memory locations. They have higher priorities than the INTR interrupt. Among these three, the priority order is 7.5, 6.5, and 5.5.
☐ TRAP (Input)	This is a nonmaskable interrupt and has the highest priority.
☐ HOLD (Input)	This signal indicates that a peripheral such as a DMA (Direct Memory Access) controller is requesting the use of the address and data buses.
☐ HLDA (Output)	Hold Acknowledge: This signal acknowledges the HOLD request.
☐ READY (Input)	This signal is used to delay the microprocessor Read or Write cycles until a slow-responding peripheral is ready to send or accept data. When this signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

Interrupt Signals

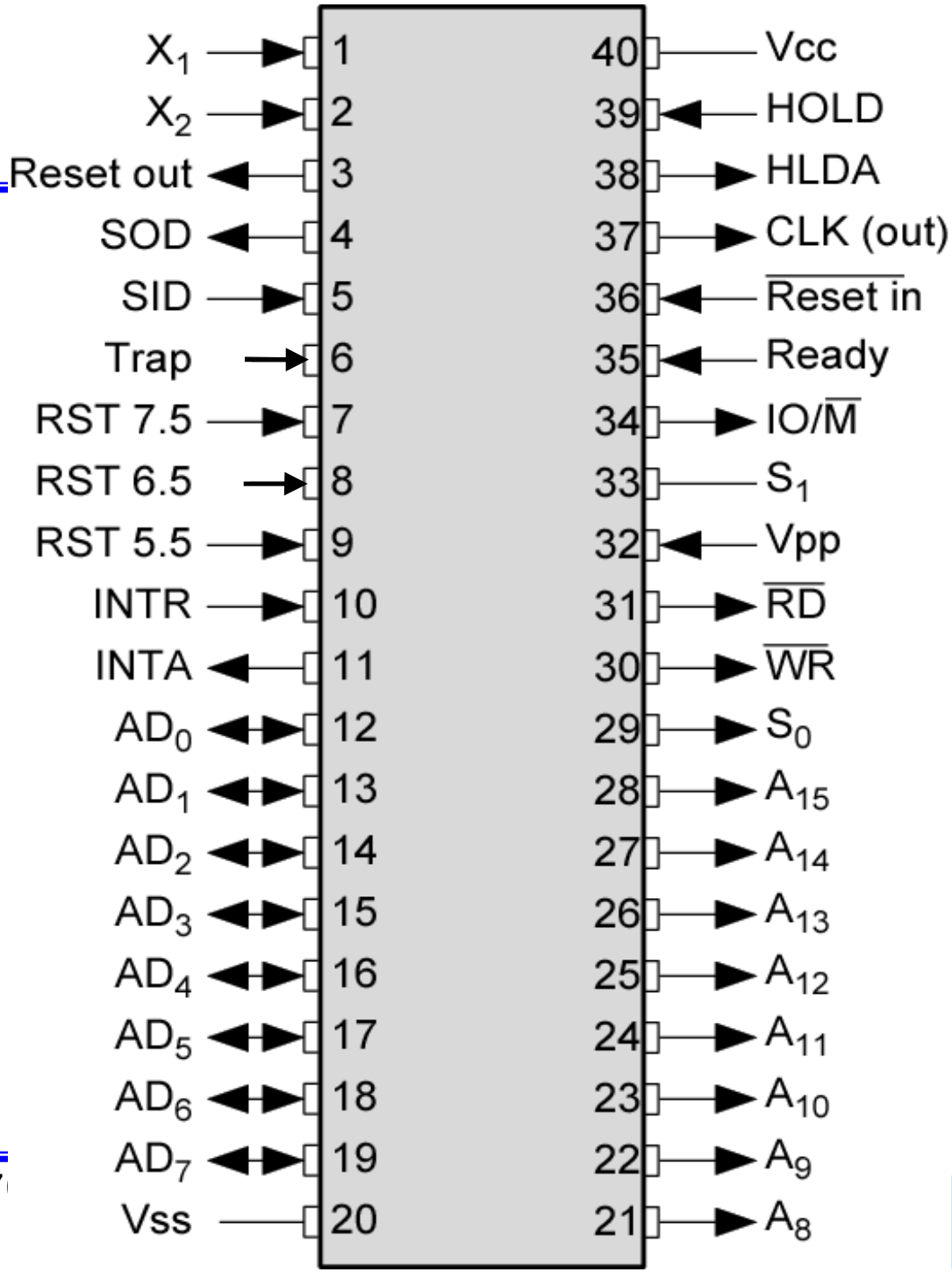
- An interrupt is a hardware-initiated subroutine CALL.
- When interrupt pin is activated, an ISR will be called, interrupting the program that is currently executing.

Pin	Subroutine Location
TRAP	0024
RST 5.5	002C
RST 6.5	0034
RST 7.5	003C
INTR	*
Note: * the address of the ISR is determined by the external hardware.	

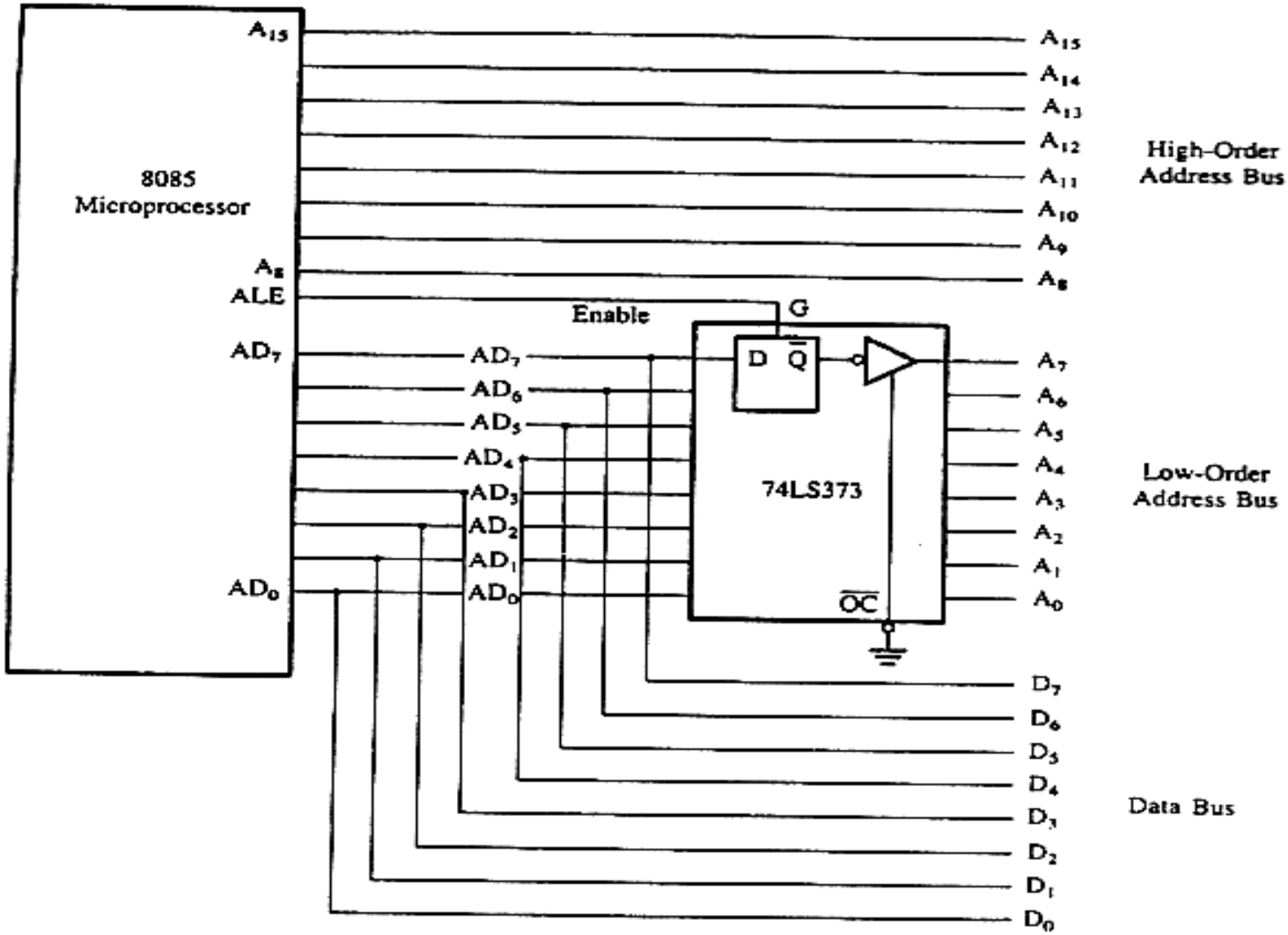
8085 Microprocessor Signal Flow Diagram



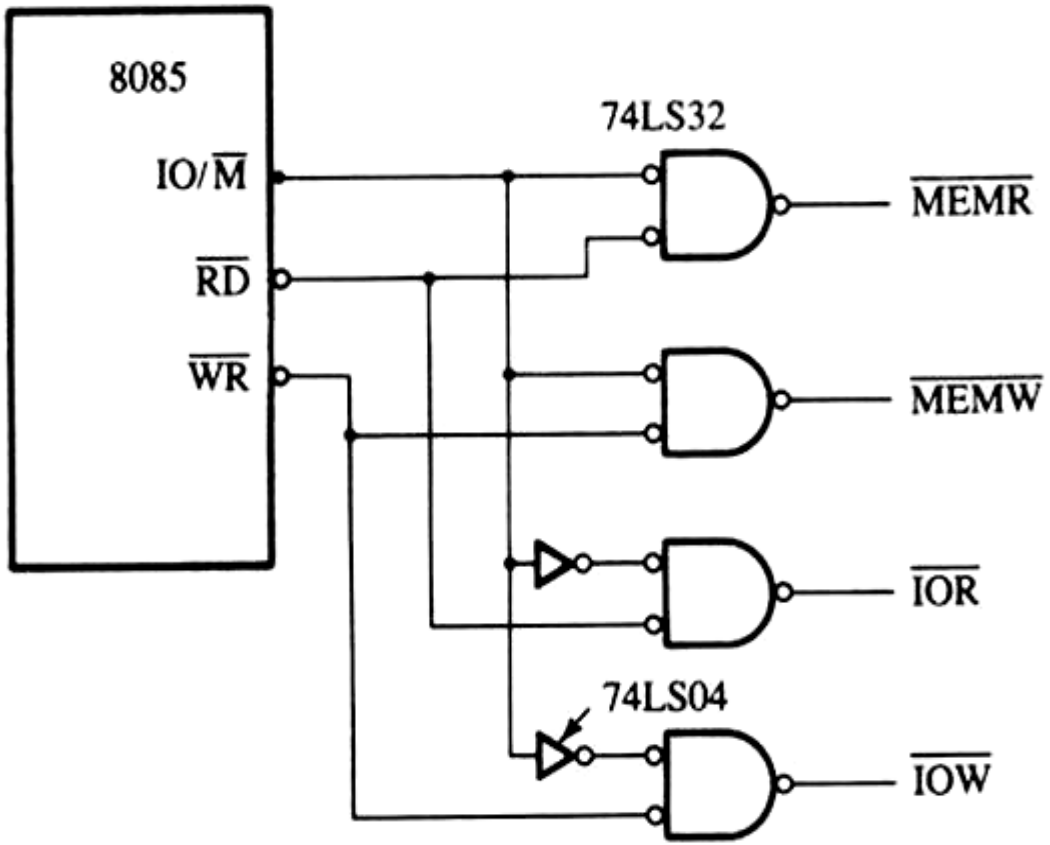
8085 Microprocessor Pin Diagram



Demultiplexing the AD_7 to AD_0

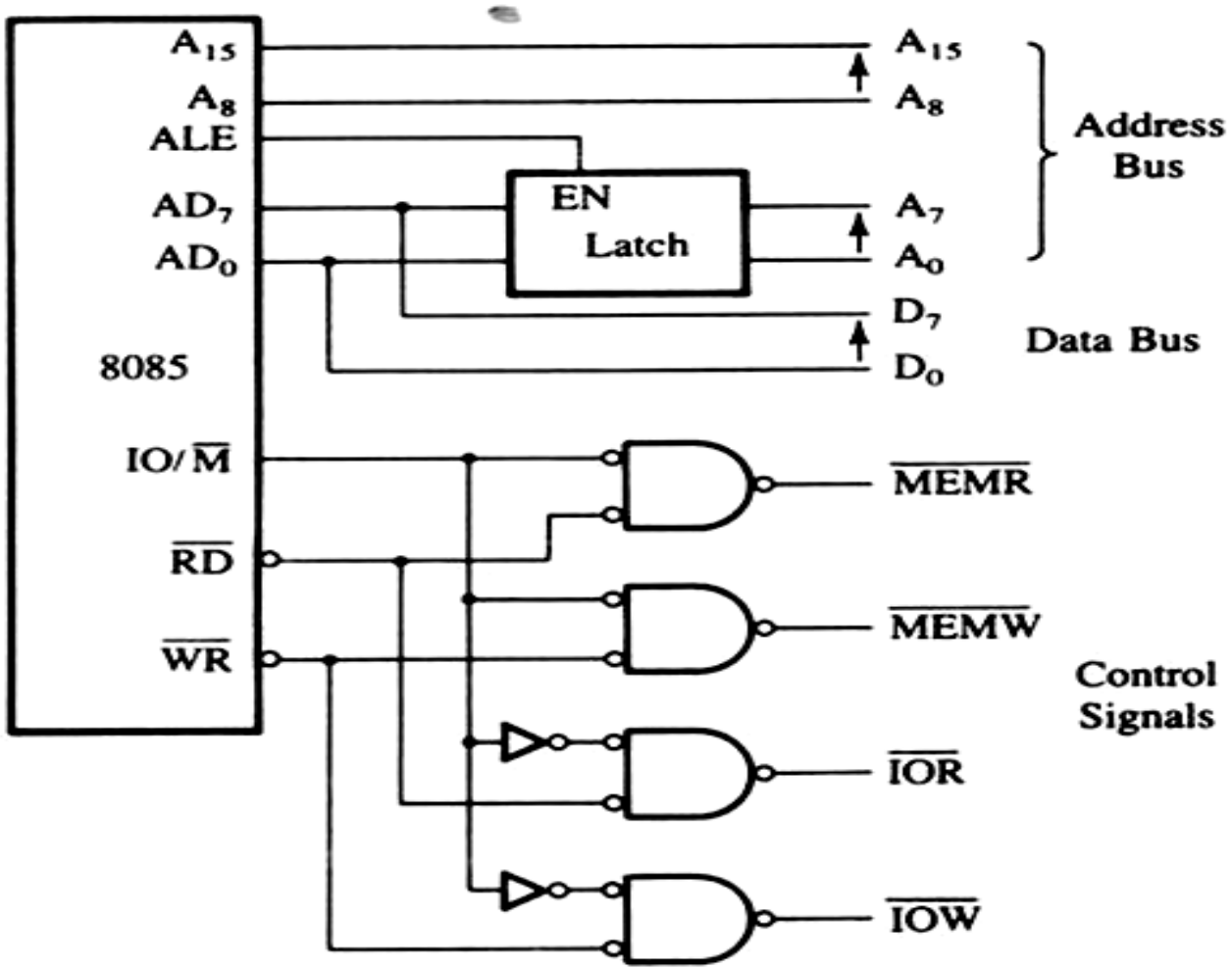


Generation of Control Signals



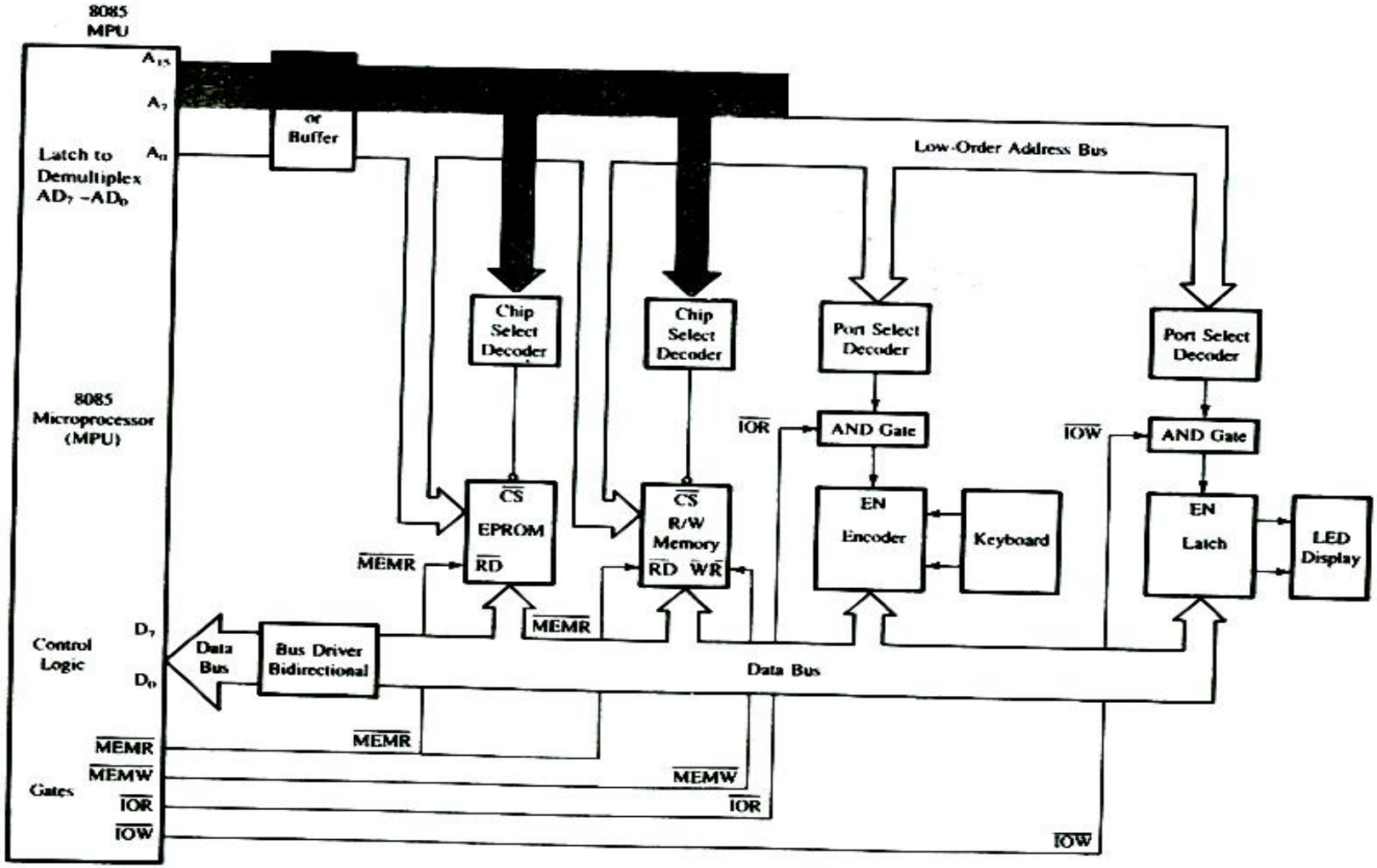
Example of schematic diagram to generate control signals.

Control Signals and Demultiplexing



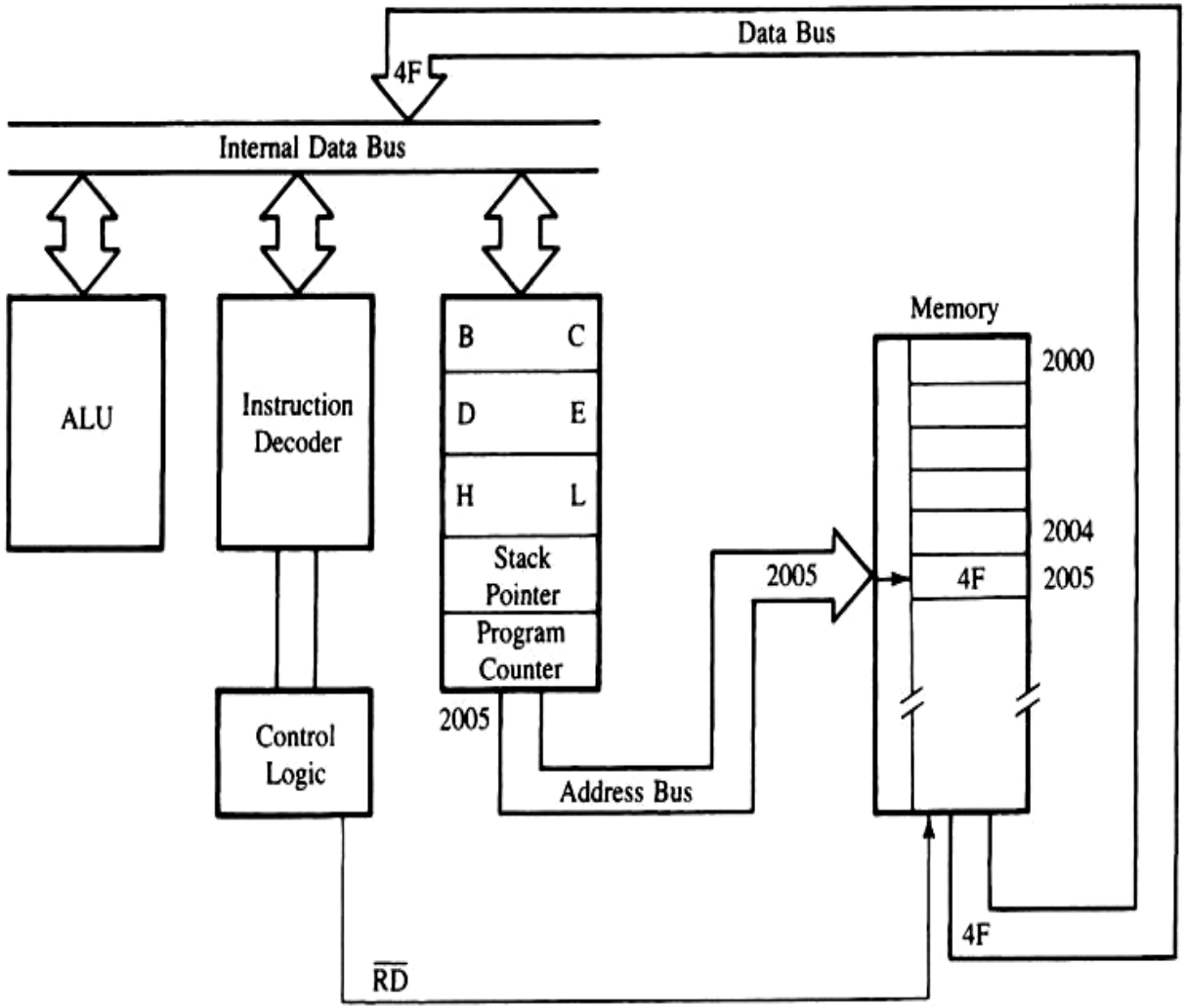
The combination of control signals as well as demultiplexing the bus system.

8085 Single-Board Microcomputer System



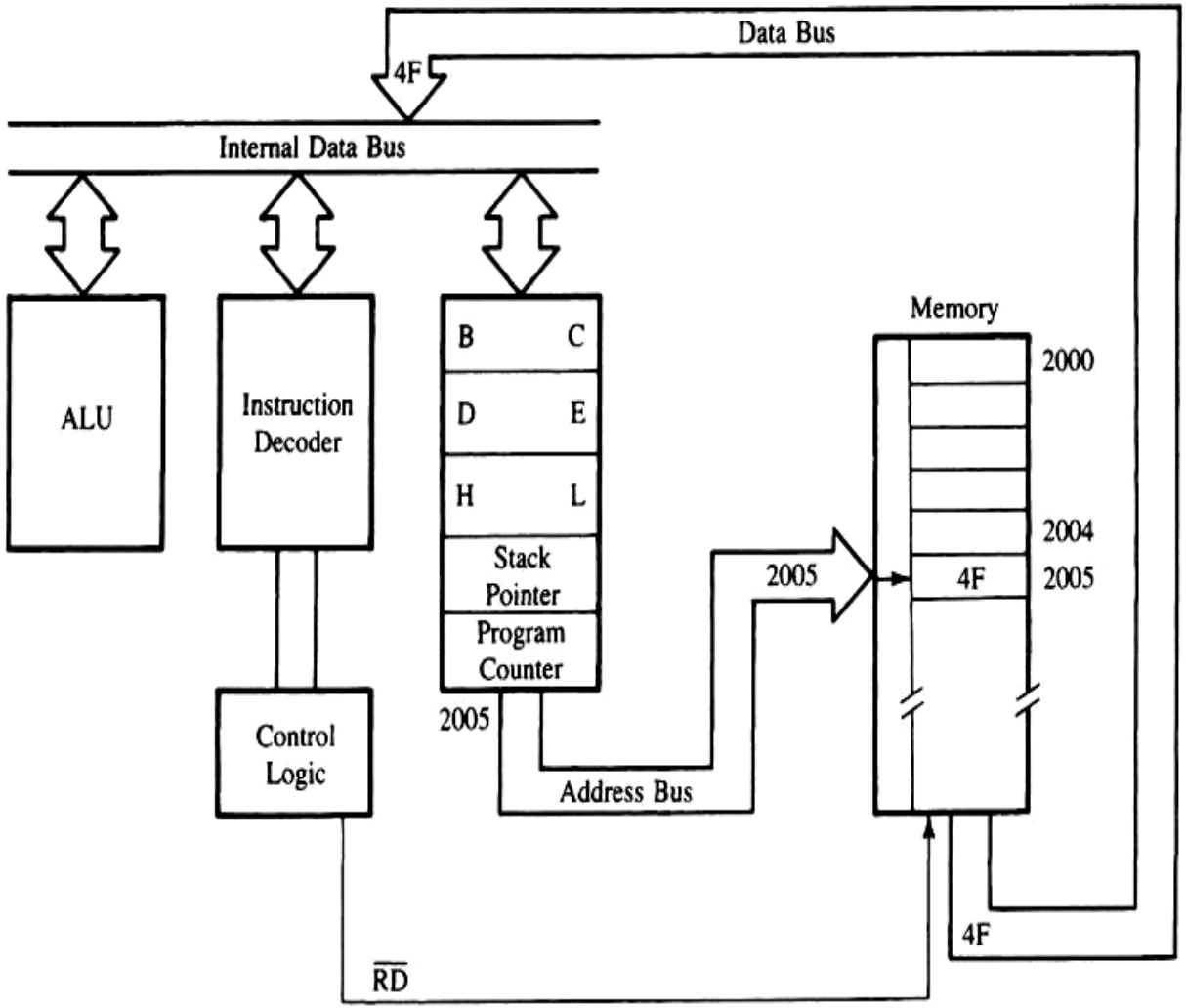
Data Flow from Memory to MPU

- Instruction byte 4FH (mov C,A) is being fetched from the memory location 2005H



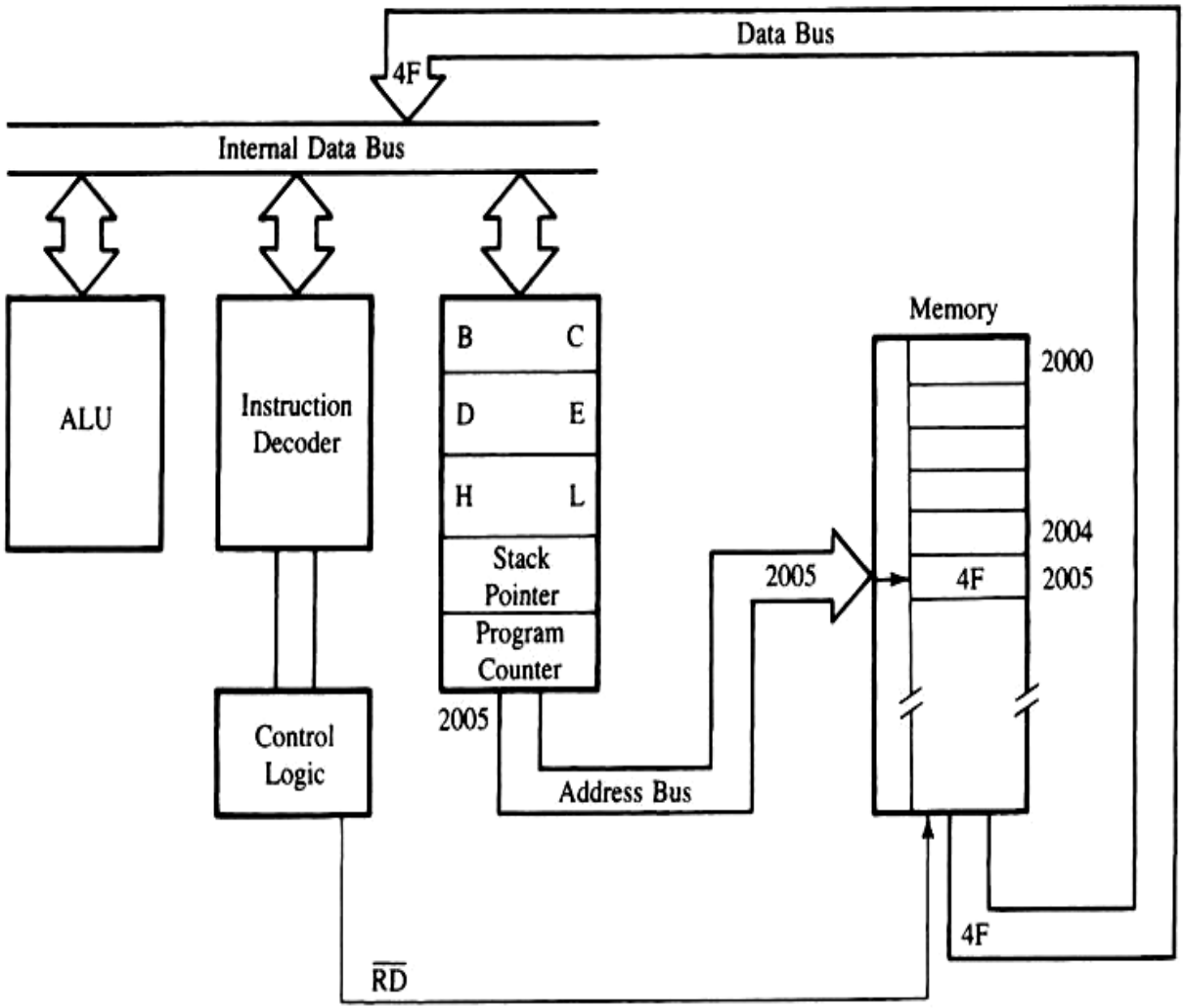
Data Flow from Memory to MPU

- Step 1: The microprocessor places the 16-bit memory address from the PC on address bus.



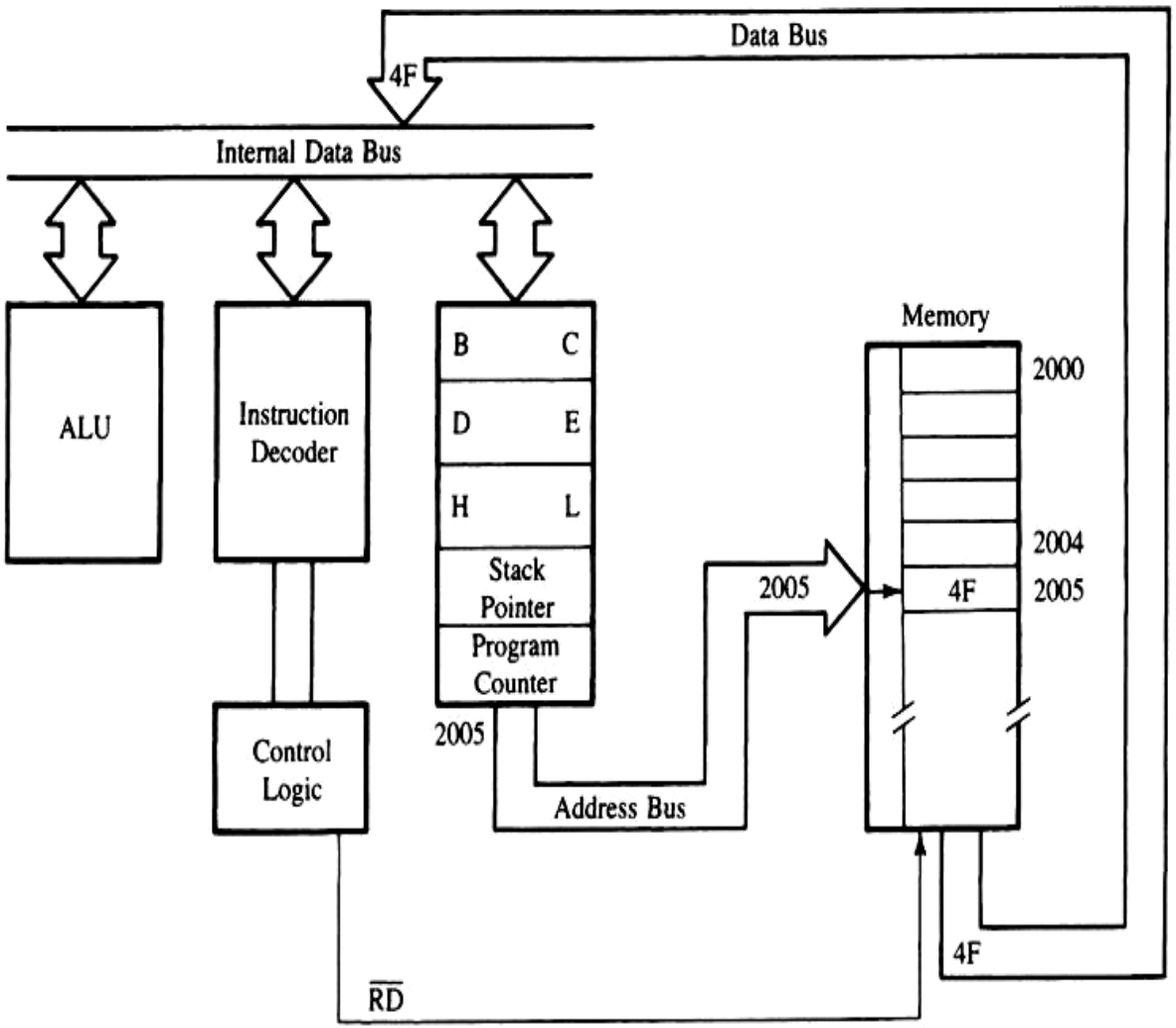
Data Flow from Memory to MPU

- Step 2: The control unit send the control signal $\overline{RD}$ to enable the memory chip.

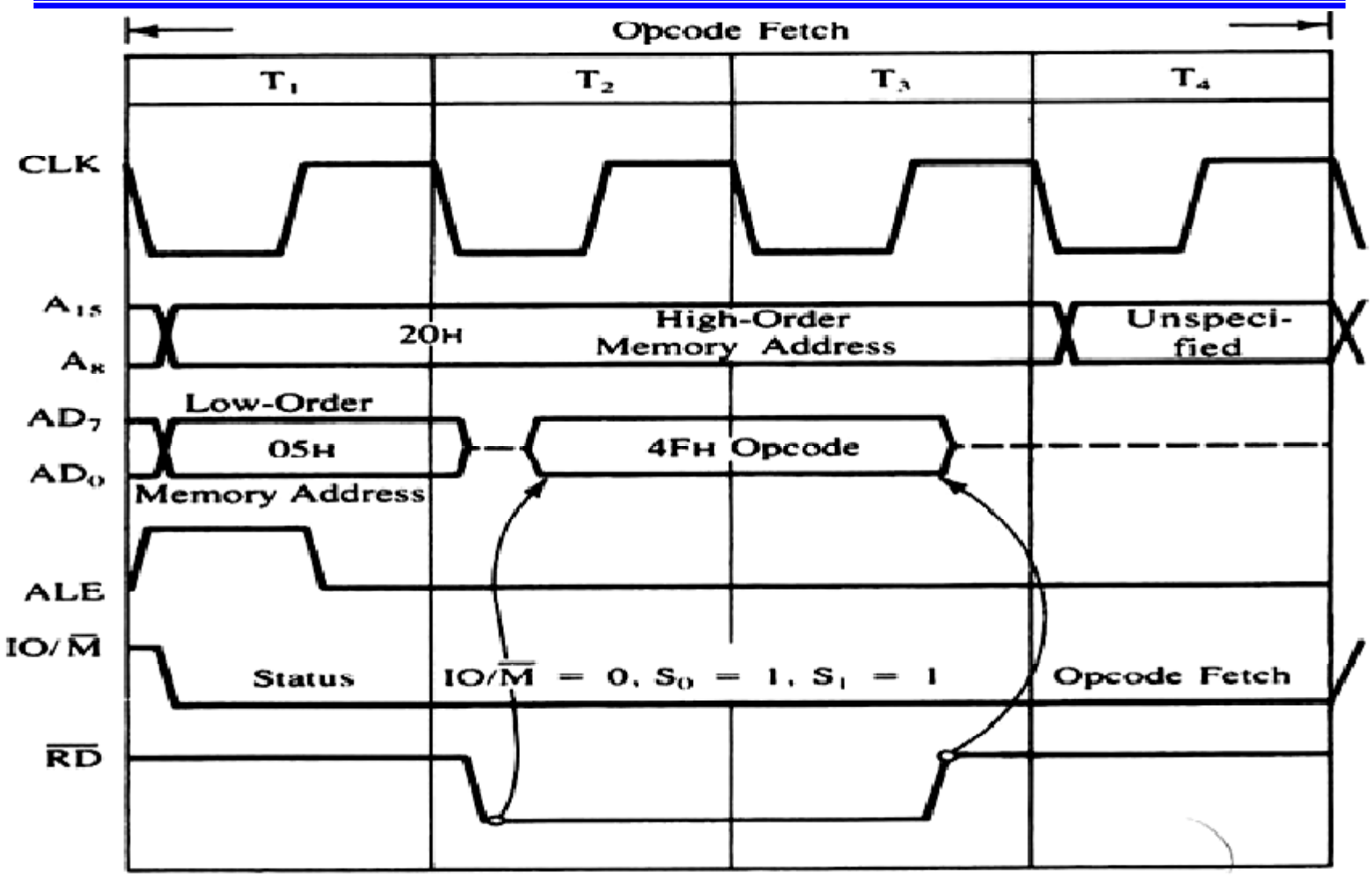


Data Flow from Memory to MPU

- Step 3: The byte from the memory location is placed on the data bus.
- Step 4: The byte is placed in the instruction decoder of the microprocessor, and the task is carried out according to the instruction.



Timing Diagram for Opcode Fetch (mov C,A)

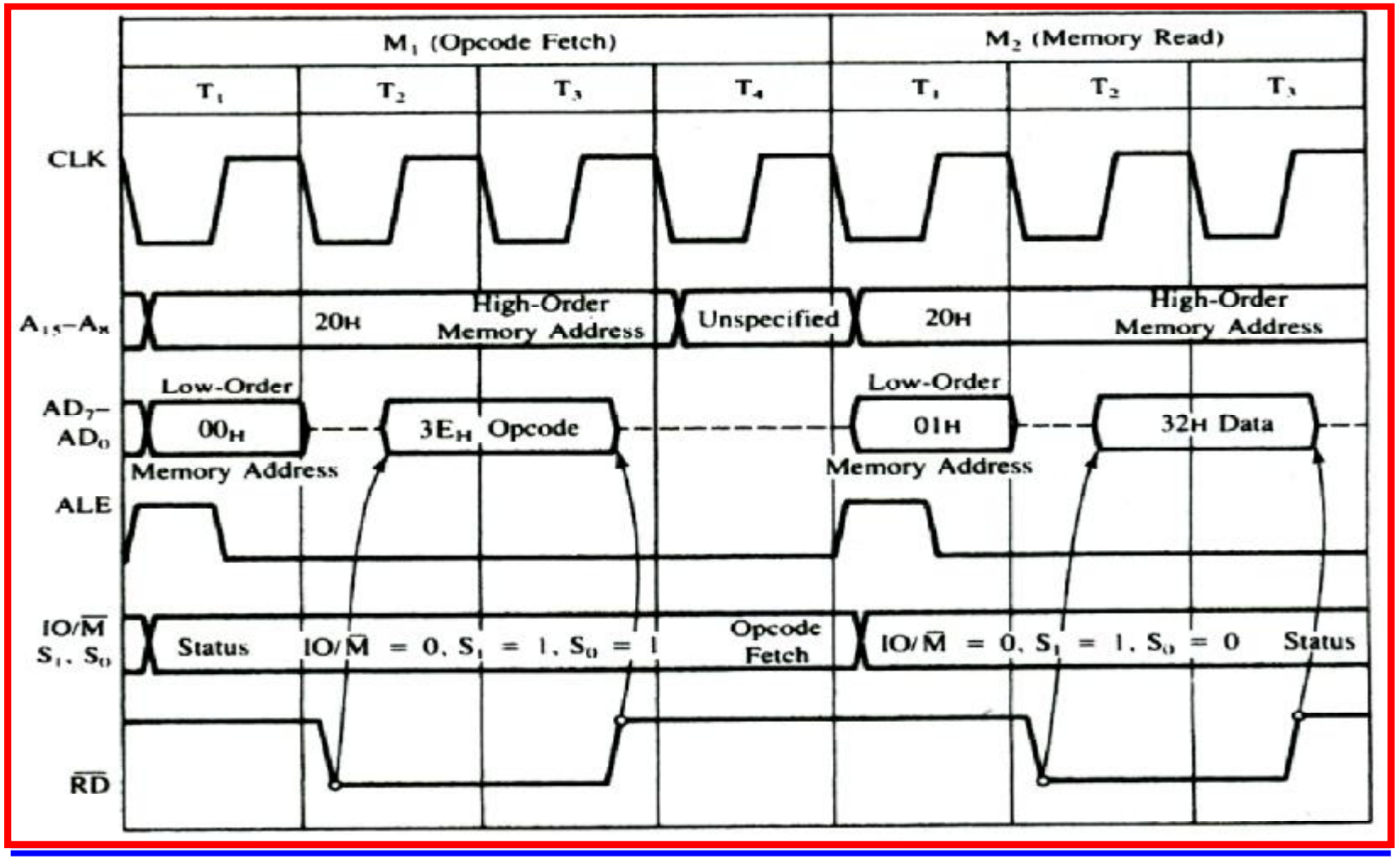


Instruction cycle, Machine cycle & T-state

- Instruction Cycle:
  - It is defined as the time required to complete the execution of an instruction.
  - The 8085 instruction cycle consists of one to six machine cycles or operations.
- Machine Cycle:
  - It is defined as the time required to complete one operation of accessing memory, I/O, or acknowledging an external request.
  - This may consist of three to six T-states (cycles).
- T-state:
  - It is defined as one subdivision of operation performed in one clock period.
  - Generally it is equal to one clock cycle.

Timing Diagram for executing MVI A,32H

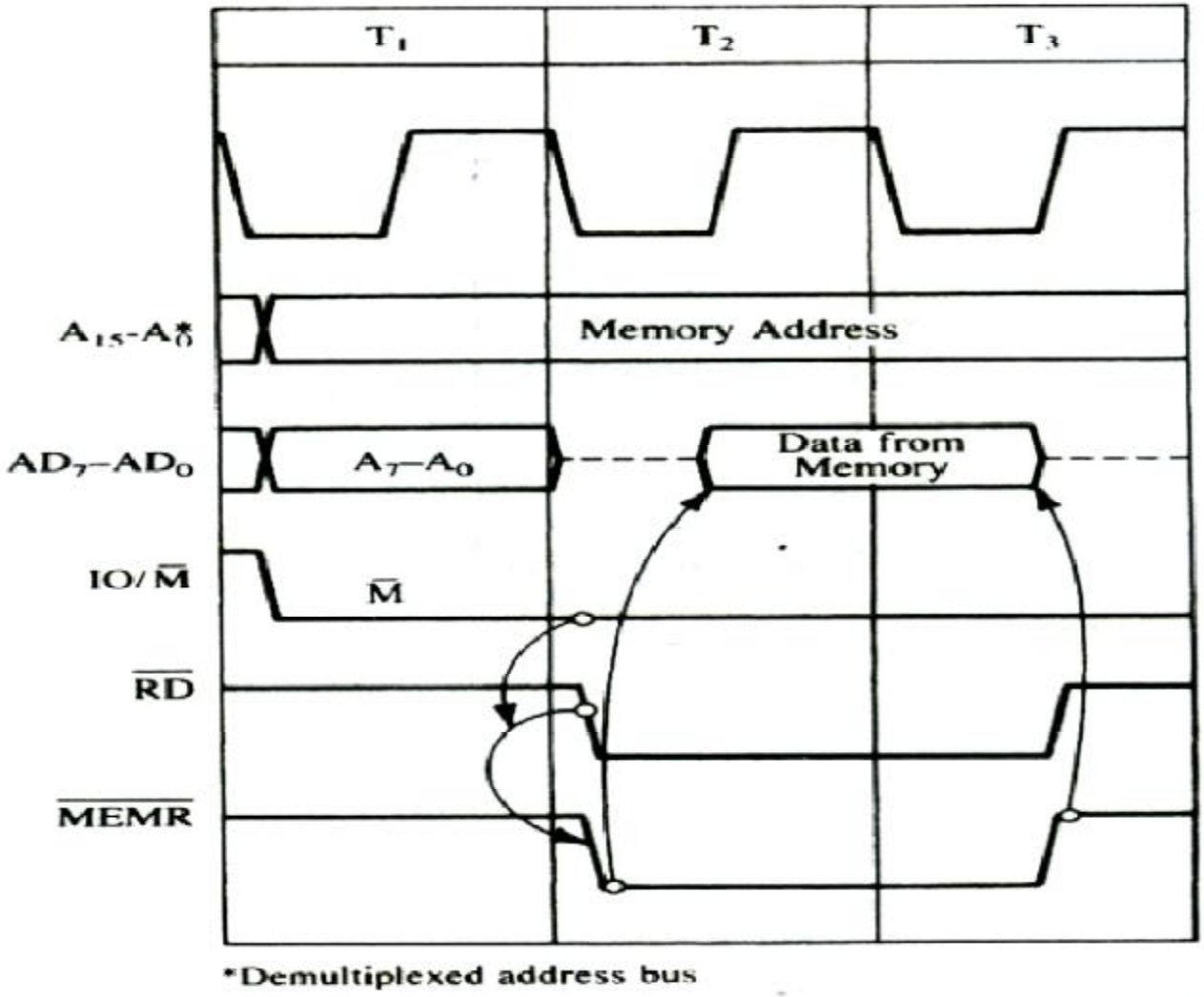
- Fetch Completed in T3 State. During T4 State, 8085 decodes the opcode



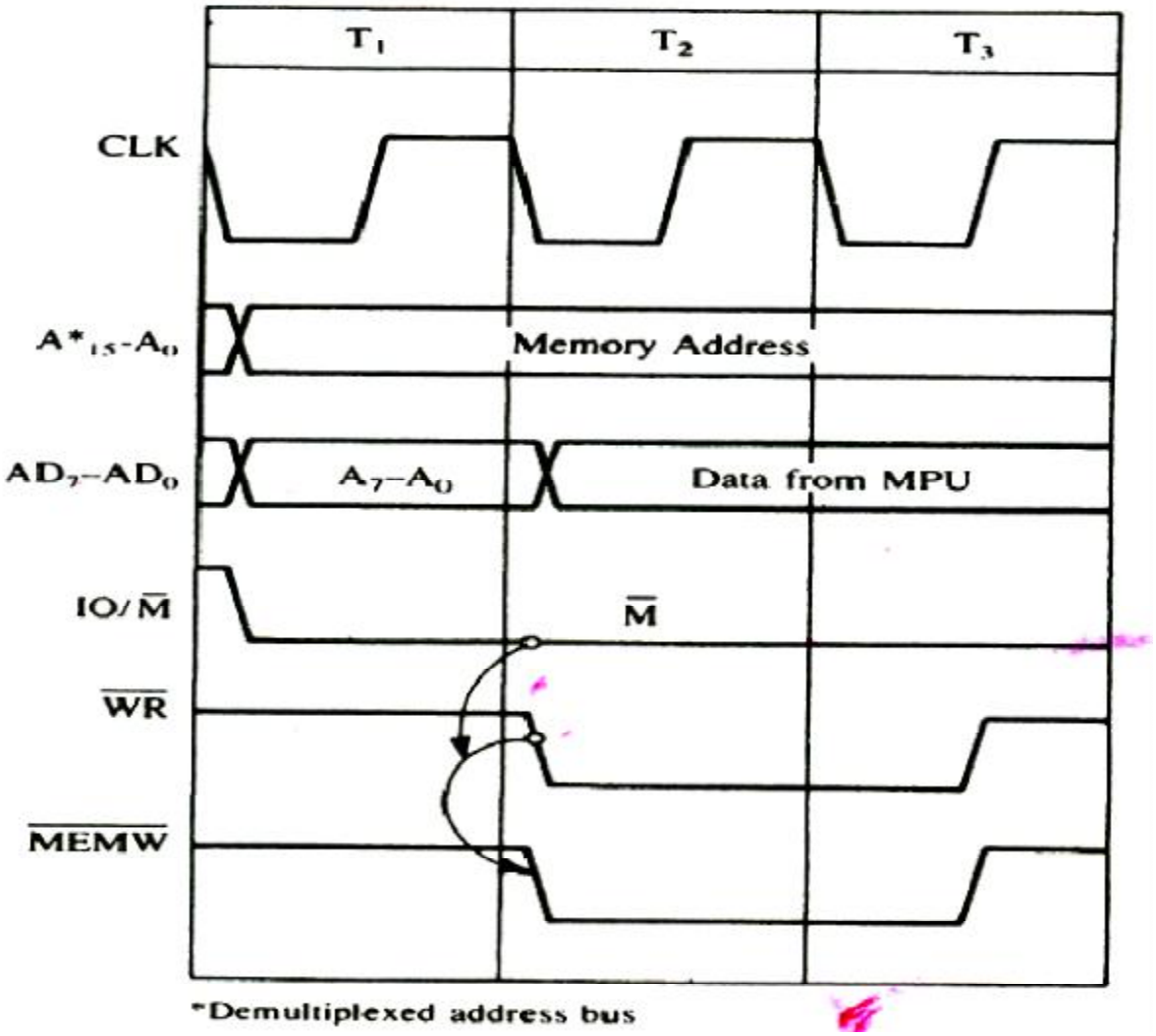
Executing time for MVI A,32H

- Total Execution Time:
  - Clock Frequency, f = 2MHz
  - T-state = clock period = (1/2)µSec = 0.5 µSec
  - Execution time for:
    - Opcode fetch = 4T X 0.5 µSec = 2 µSec
    - Memory Read = 3T X 0.5 µSec = 1.5 µSec
  - Total execution time for instruction = 7T X 0.5 µSec
    = 3.5 µSec

Timing Diagram of Memory Read Cycle



Timing Diagram of Memory Write Cycle



Thank you
Any Quarries?