Enperiment Name: Implementation of Ripple Counter (Asynchronous counter).

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Course: CSE-2112

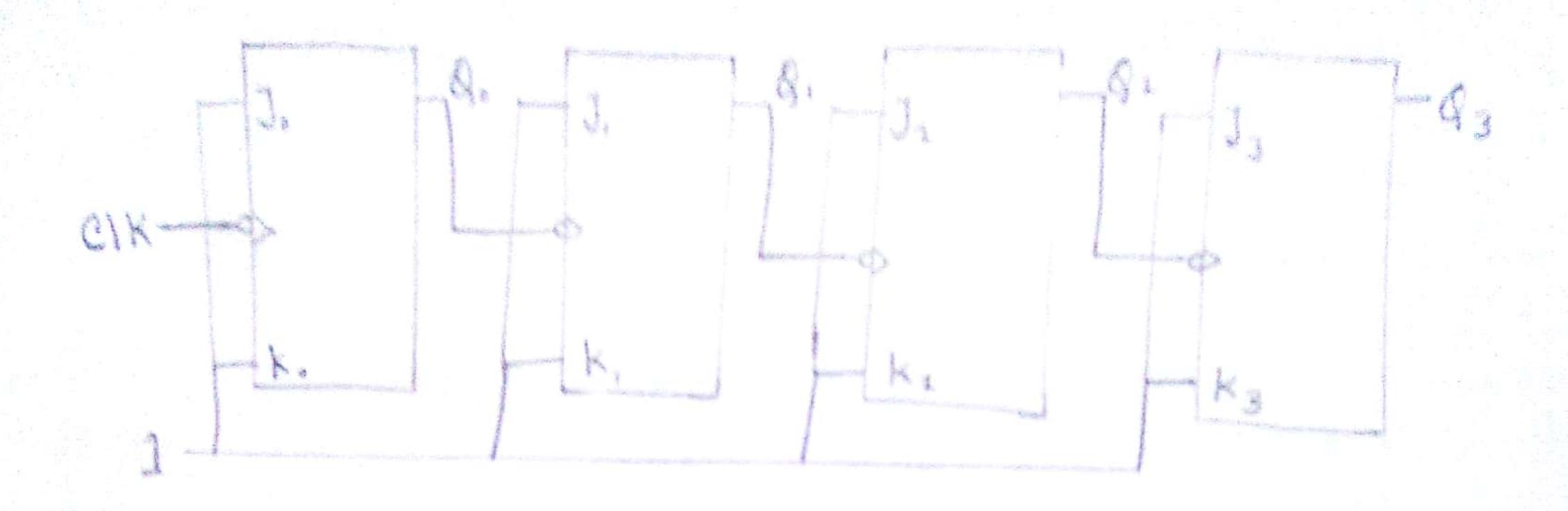
Date: 13.05-2018

Enperiment: Implementation of Ripple Counter
(Asynchronous counter).

Theory: Ripple counter is mainly an Agynchronous counter. This take an Agynchronous counter. This take an input and that is pulse. From the input and that is pulse. From the pulse using J.K flip-flop ripple counter gives outputs. Depending on outputs it counts sequentially from up to down or down to up.

Instruments: wire, bread-board, power source, J.k Flip-Flop.

circuit;



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Truth Table.

Sequence	CIK	93	02	9,	0
0	T	0	0	(*)	
	7	0	O	0	1
2	1	0	0		0
3	1	D	0	1	4
4	1	0		0	0
5	1	0	1	0	
6	1	0		1	0
7	1	O	1	1)
8	1	1	0	O	0
9	1	1	0	0	1
10		1	0		
11	1	1	Ö	1	1
12	1	1	1	-	
13	T	1	,	0	0
14	1				1
And where the consequence of the	1	The state of the s	1	1	0
16 (Reopel)	*	1	1	1	1
in the same	Part State Contract of the Con	O .	0	0	0

Result and Discussion: From the circuit one have designed the results we got are similar to the results of the truth table. The results we got are valid.

So, the circuit is right.

Pre-caustion:

- 1. connect the circuit when there design is complete.
- 2. please check the circuit before connecting.
- 3. Ware shoes in the lab.
- 4. After finishing enperiment switch off the power source.