Experiment Name: Implementation of Synchronous counter (Any sequence).

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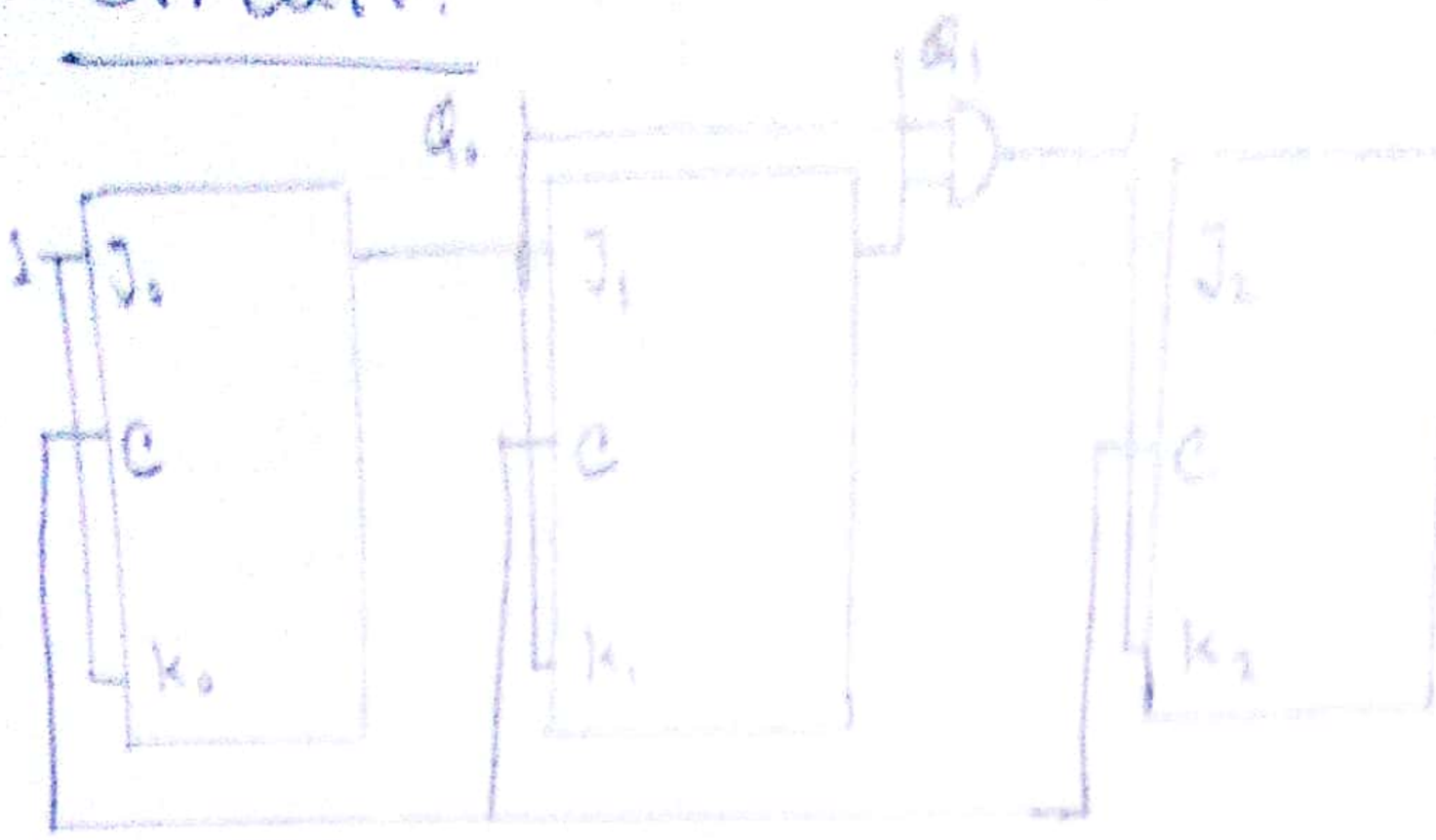
Experiment: Implementation of Synchronous counter (Any sequence).

Theory: Synchronous counter is a register where we use same clock pulse to all flip flop. As this counter get clock same time so all flip flop work at a time. To design a n-bit synchronous counter we need n numbers of flip-flop.

Instruments: wire, bread-board, power source, J-k flip-flop, AND gate.

Circuit:



Truth Table:

Present state			Next state			State of JK FF					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	1	1	0	X	1	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
0	1	1	0	0	1	0	X	X	1	X	0
1	0	0	1	1	1	X	0	1	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	1	0	1	X	0	X	1	X	0

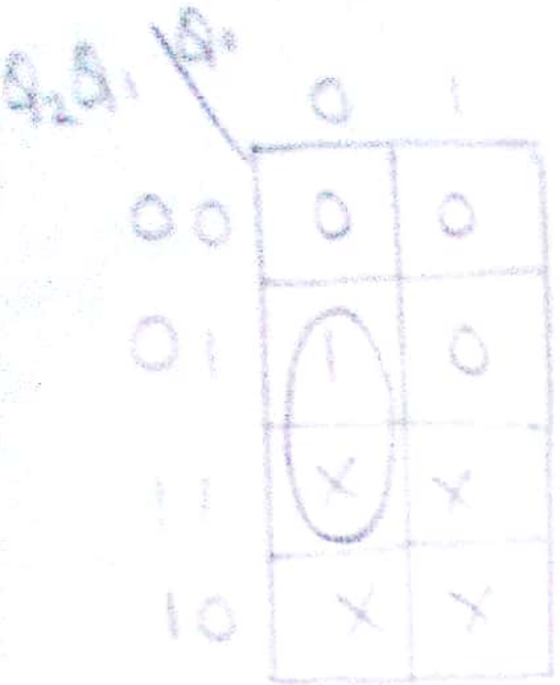
Sequence:
0, 3, 1, 2, 4, 7, 5, 6

Table for JK Flip-Flop:

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

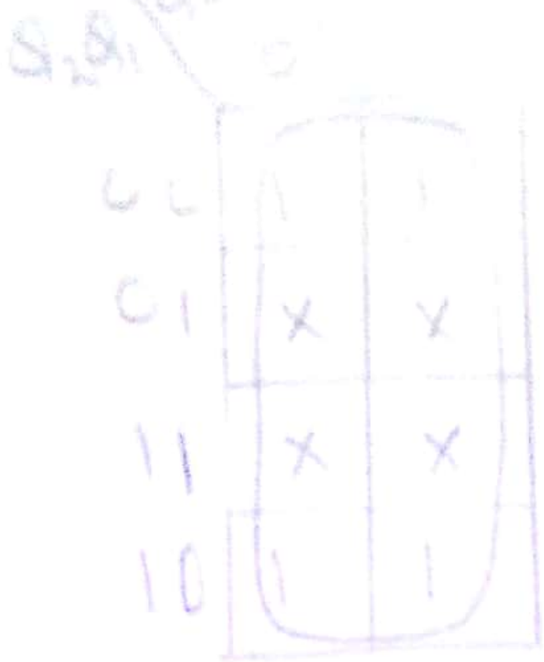
k-map from truth table:

J_2



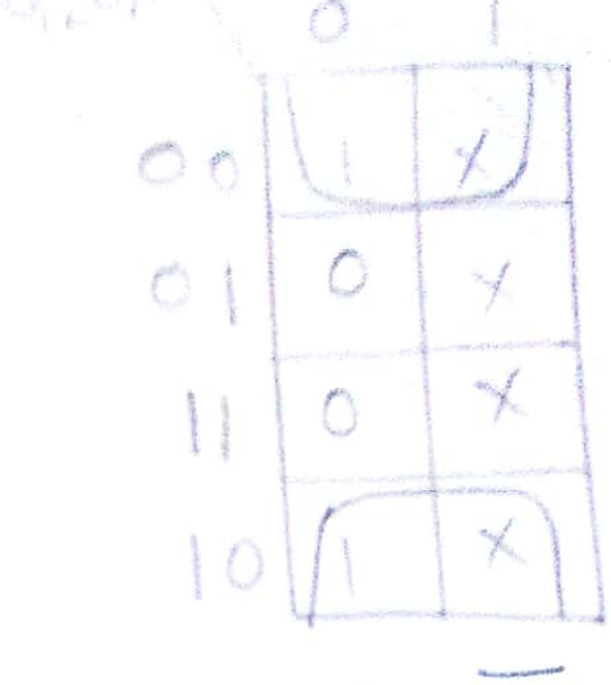
$J_2 = Q_1\overline{Q_0}$

J_1



$J_1 = 1$

J_0



$J_0 = \overline{Q_1}$

K_2

$K_2 = Q_1\overline{Q_0}$

K_1

$K_1 = 1$

K_0

$K_0 = \overline{Q_1}$

Result and Discussion: From the circuit we have designed the result we got is similar to the sequence we have taken to implement. All of our results are valid. So the truth table, k-map, Expression and circuit are right.

Pre-caustion:

1. Connect the circuit when design is completed.

2. Please check the circuit before connecting

3. Ware shoes in the lab.

4. After finishing experiment power off the power sourec.