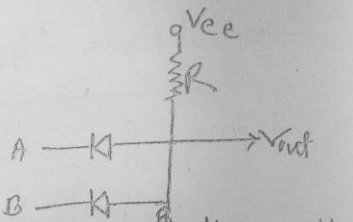
Diode logic (DL) gate:

DL for AND gate:

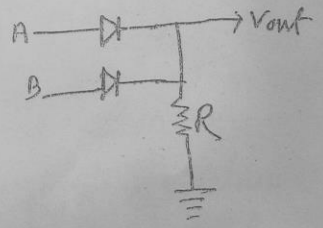


(i) When both inputs are high (logic-1) then diodes D1 & D2 are off. As a result, no current flows through the resistor and there will not be any voltage drops across the resistor. Here the output voltage will be +5 volt (logic-1).

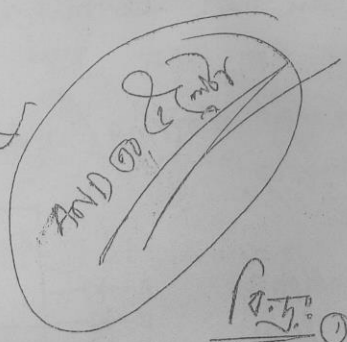
A	B	output
0	0	0
0	1	0
1	0	0
1	1	1

(ii) When A=0 & B=0 / A=0 & B=1 / A=1 & B=0,
the Diodes D1 & D2 on / D1 ON, D2 OFF / D1 → off, D2 → on → respectively, and acts on a short circuits. Here the output voltage will be 0 volt (logic-0).

DL for OR gate:



0+0 = 0
0+1 = 1
1+0 = 1
1+1 = 1



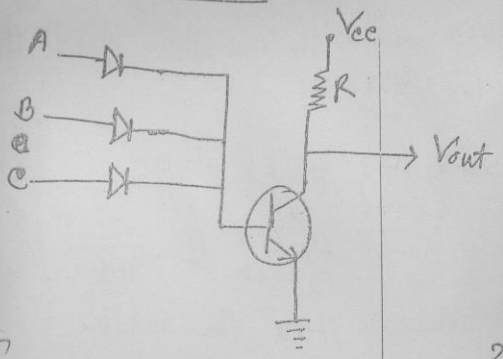
P.T.O. (i) AND গেট (সার্কিট) → Diode - Reverse Bias ব্যবহৃত,

(ii) OR গেট (সার্কিট) → Diode - Forward Bias ব্যবহৃত।

Diode-Transistor Logic Gate (DTL):

→ **Advantage:** one advantage of DTL over RTL is its better noise margin.

NOR Gate for DTL:



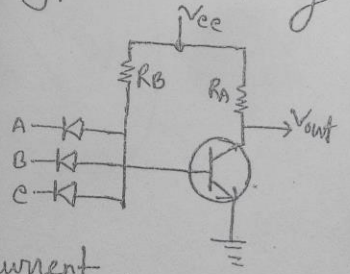
OR	NOR
0+0=0	1
0+1=1	0
1+0=1	0
1+1=1	0

1. When any inputs goes high (logic-1), then the transistor saturates and the output voltage Vout is low (logic-0).
2. If all inputs are low, the transistor cuts off and the Vout goes high.
3. This is a NOR gate.

→ **Problem:** "Current Hogging" is a problem because the bipolar transistors can not be matched previously.

⇒ **Cutting off:** act on of stopping/interrupting the supply.

NAND Gate:



(i) If all inputs are high, the transistor saturates and Vout goes low.

(ii) If any inputs goes low, the base current is diverted out through the input diode. The transistor cuts off and Vout goes high.

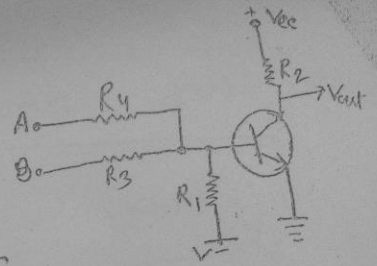
(iii) This is a NAND Gate.

	NAND
0.0=0	1
0.1=0	1
1.0=0	1
1.1=1	0

Register-Transistor Logic gate (RTL):

$0+0=0$ / '0'
$1+1=1$

It consists of a common-emitter stage with a base resister connected between the base and the input voltage source.



fig③: RTL NOR gate.

Working principles:

① If all the inputs are low (logic 0), the transistor is cut-off. The pull down resistor R_1 biases the transistor to the appropriate on-off threshold. Then the output V_{out} = 5 Volt (logic-1).

② If A = 1 and B = 1 / ~~A = 0, B = 1 / A = 1, B = 0, then~~ the Resister R_4, R_5 take voltage and ~~the transistor~~ the transistor turned on, i.e the base take the voltage and transistor saturated. ∴ The Vcc is drop out the ground and $V_{out} = 0$.

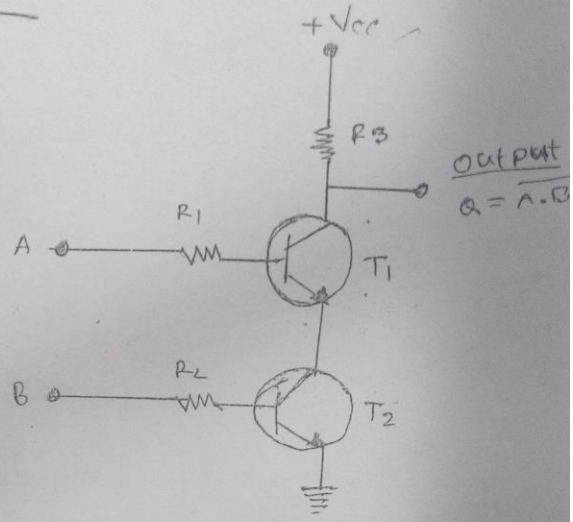
③ A = 0, B = 1 / A = 1, B = 0 ⟶ Transistor on, $V_{out} = 0$.

Advantages: ① It used a minimum number of transistors.

Limitations: ① Its high power dissipation when the transistor is ~~turned~~ switched on by current flowing in the collector and base resistors.

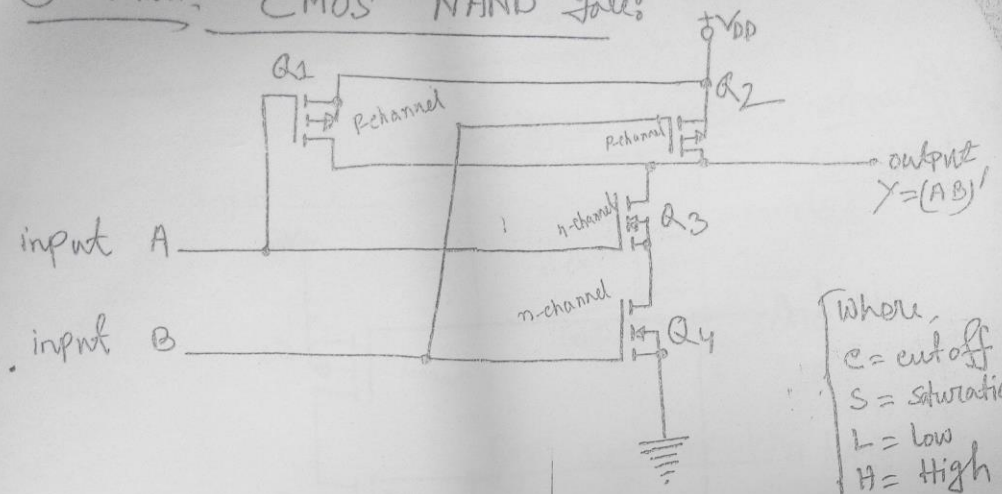
RTL NAND Gate

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



0.0 = 0 | 1
0.1 = 0 | 1
1.0 = 0 | 1
1.1 = 1 | 0

Question: CMOS NAND gate:



Where,
C = cut off (off)
S = saturation (on
L = low
H = High

Fig①: CMOS NAND gate.

Truth Table:

A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	H
H	L	C	S	S	C	H
H	H	C	C	S	S	L

Working Principle:

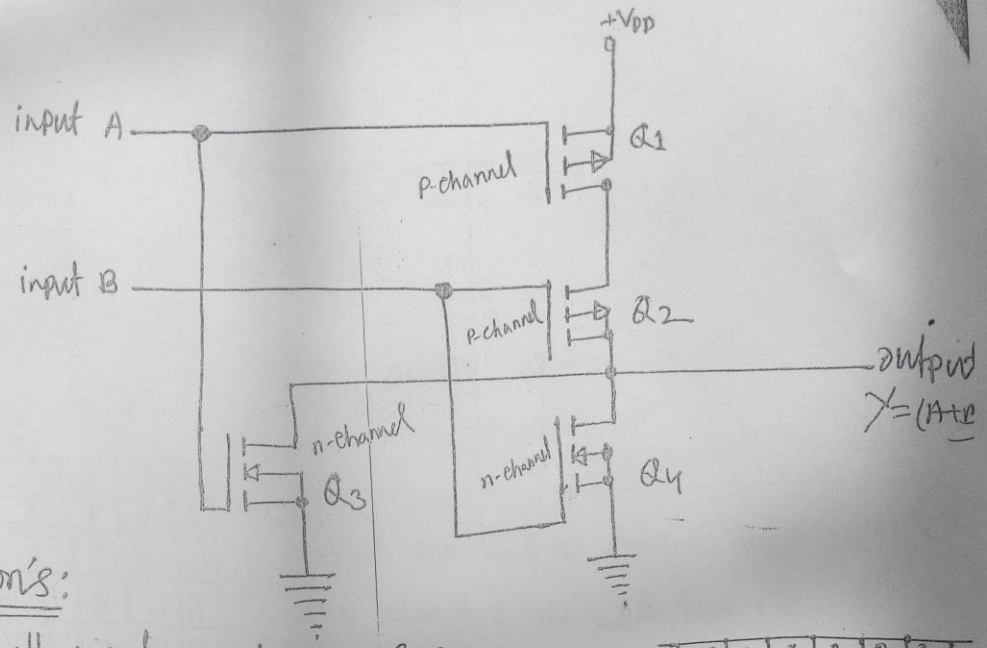
(i) When both inputs (A & B) are low, the Q_1 and Q_2 are saturated (ON) and Q_3 and Q_4 are off. The output is pulled high through the on resistance of Q_1 and Q_2 in Parallel.

(ii) When input A is low and input B is high, Q_1 and Q_4 are on and Q_2 & Q_3 are off. The output is pulled high through the low on resistance of Q_1.

(iii) When input A is high and input B is low, Q_1 & Q_4 are off and Q_2 & Q_3 are on. The output is pulled high through the low on resistance of Q_2.

(iv) Finally, when both inputs are high, Q_1 & Q_2 are off and Q_3 & Q_4 are on. The output is pulled low through the on resistance of Q_3 and in series to ground.

2012 Question:: CMOS NOR Gate:



Operations:

(i) When both inputs are low, Q_1 & Q_2 are on, and Q_3 & Q_4 are off. The output is pulled high through the on resistance of Q_1 and Q_2 in series.

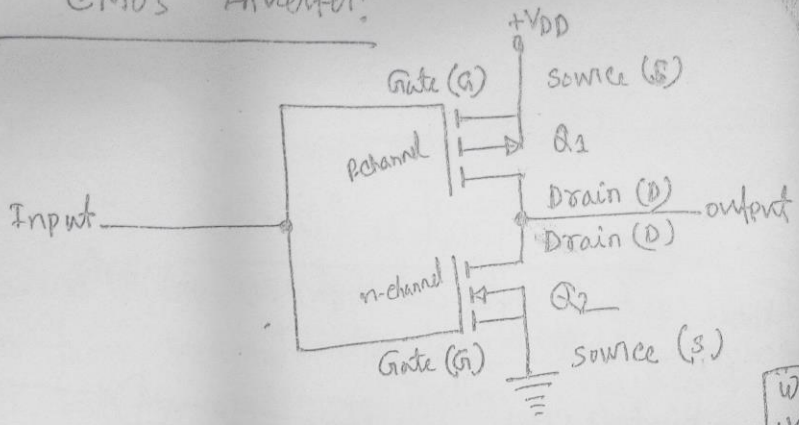
A	B	Q_1	Q_2	Q_3	Q_4	x
L	L	S	S	C	C	H
L	H	S	C	C	S	L
H	L	C	S	S	C	L
H	H	C	C	S	S	L

(ii) When input A is low, B is high, The Q_1 & Q_4 are on and Q_2 & Q_3 are off. The output is pulled Low through the low on resistance of Q_4 to ground.

(iii) When input A is high, B is low, Q_1 & Q_4 are off and Q_2 & Q_3 are on. The output is pulled low through the low resistance of Q_3 to ground.

(iv) When both inputs are high, Q_1 & Q_2 are off and Q_3 & Q_4 are on. The output is pulled low through the on resistance of Q_3 and Q_4 in parallel to ground.

Question: CMOS Inverter:



Where,
+VDD = DC supply voltage

fig ⓐ: COM inverter.

Complementary MOS (CMOS) logic uses the MOSFET in complementary pairs as its basic element. A complementary pair uses both p-channel and n-channel enhancement MOSFET's as shown in fig ⓐ.

Operations:

When a high is applied to the input fig ⓑ:, the p-channel MOSFET Q_1 is off and n-channel MOSFET Q_2 is on. This condition connects the output to ground through the on resistance of Q_2, resulting in a low output.

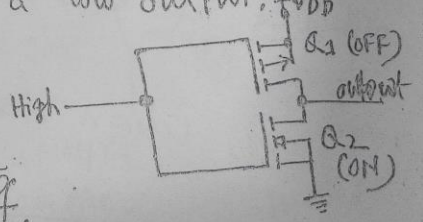


fig ⓑ

Operations: When a low is applied to the input as fig ⓒ:, Q_1 is on and Q_2 is off. This condition connects the output to +VDD through the on resistance of Q_1, resulting in a high output.

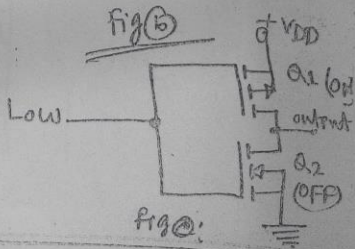
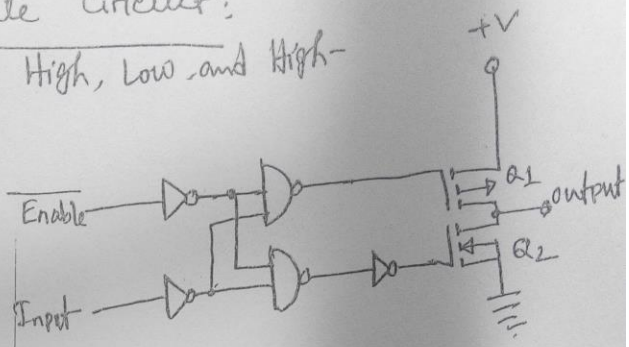


fig ⓒ:

Question: cmos - Tristate circuit:

Ans: The three output states are High, Low, and High-impedence (high-Z).

circuiting in a tristate CMOS gate, as shown fig@: allows each of the output transistors Q_1 and Q_2 to be turned off at the same time, thus disconnecting the output from the rest of the circuit.



Fig@: Tristate - CMOS circuit

When the enable input is low, the device is enabled for normal logic operation.

When the enable input is high, both Q_1 and Q_2 are turned off and the circuit is in the high-Z state.

∴ when Enable low = enbled

Enable	Input	Q_1	Q_2	output
0	0	ON	ON	0
0	1	off	off	1

...uction: MOSFET:

P-type / holes → Majority
N-type / electron minority.

→ Metal-oxide semiconductor field-effect transistors are the active switching elements in CMOS circuits.

→ These devices differs greately in construction and internal operations from bipolar function transistors used used in TTL circuits, but the switching action is basically the same; they function ideally as open or closed switches, depending on the input.

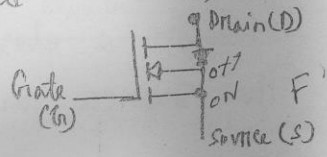


Fig ⓐ: n-channel

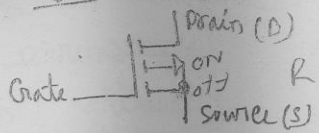


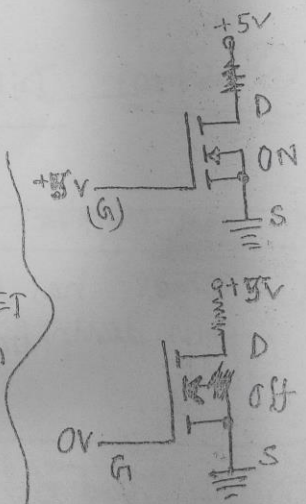
Fig ⓑ: P-channel

Fig ⓐ & ⓑ: show the n-channel and P-channel MOSFE ~~respectively~~ respectively. As indicated, the three terminals of a MOSFET are Gate, drain, source.

n-channel operations:

⇒ (i) When the gate voltage of an n-channel is more ~~positive~~ than the source, the MOSFET is on and there is ideally, a closed switch between the drain and the source.

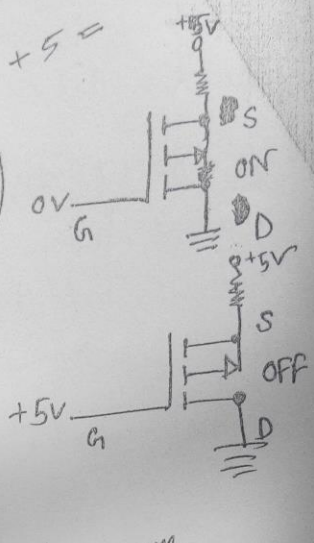
(ii) When the gate to source voltage is zero, the MOSFET is off (cutoff) and there is ideally, an open switch between the drain and source.



ON = +5

off = 0

⇒ P-channel operation's:



(i) When the gate voltage of an P-channel MOSFET is zero, the MOSFET is on (saturated) and there is ideally a closed switch between the source and drain.

(ii) When the gate voltage of P-channel is more positive than the source, the MOSFET is off (cutoff) and there is ideally an open switch between the source and the drain.

Question: Difference between CMOS and TTL:

CMOS	TTL (Bipolar
(i) CMOS has lower power dissipation than TTL.	(i) TTL has higher power dissipation than CMOS
(ii) Its speed is low.	(ii) Its speed is high

FACULTY OF ENGINEERING
UNIVERSITY OF RAJSHAHI

No. 012107

Class Test

Total Marks

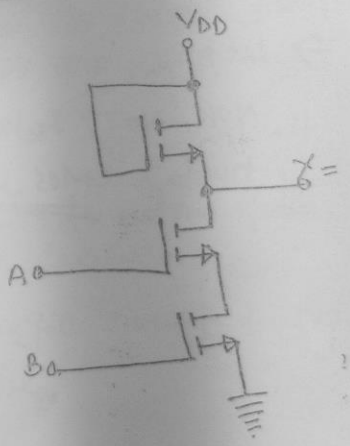
Roll Number/Student ID No. .....
Course Code .....
Exam. Date .....

Signature of Invigilator

RUP-40,000/C.S. 413/Date: 15.10.2016

Question: MOSFET NAND gate circuit:

The NAND gate shown in fig(a) uses transistors in series. Inputs A and B must both be high for all transistors to conducts and cause the output to go low.



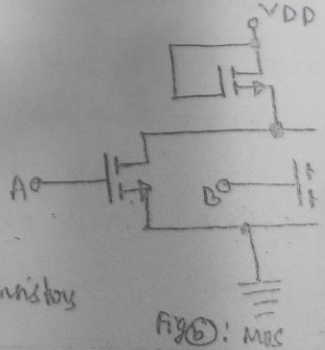
Fig(a): MOS NAND

If either input is low, the corresponding transistor is turned off and the output y high.

Question: MOSFET ~~using~~ NOR gate circuit:

Fig(b): uses transistors in parallel.

(i) If either input is high, the corresponding transistor conducts and the output is low.
(ii) If all inputs are low, the corresponding all transistors are off and the output is high.



Fig(b): MOS

CMOS

P.S.: [redacted] Remember to follow:

(i) The n-channel MOS conducts, when its gate to source voltage is p

(ii) The p-channel MOS conducts, when its gate to source voltage is negati

(iii) Either type of device is turned off its gate to source voltage is zero.

⇒ lecture [redacted] MOSFET ? , part ? ? MOS NAND, NOR, NOT/ Inverter , CMOS, CMOS NAND, NOR, Inverter, tristate CMOS.

Questions.

Difference between ECL & TTL:

(i) Emitter coupled logic circuits is faster than TTL

(ii) ECL has more power than TTL.

(iii) ECL has less noise margin than TTL.

Define:

(i) Current sinking: The action of a logic circuit which it accepts current into its output from load.

(ii) Current Sourcing: The action of a logic circuit which it sends current from its output to load.

(iii) Noise Immunity: The ability of a logic circuit to reg. unwanted signals/noise.

(iv) Noise Margin: The difference between the maximum low output of a gate and the maximum acceptable le input of an equivalent gate; also the difference betw the minimum high output of a gate and the min. high input of an equivalent gate.

(v) Power Dissipation: The product of the dc supply voltage the dc supply current in an electronic circuit.

(vi) Propagation Delay Time: The time interval between the occurance of an input transition and the occurance of the corresponding output transition in a logic circuit.

(vii) Totem Pole: A type of output in TTL circuits.

(viii) Tristate: A type of output in logic circuits that exhibits three states: High, low and high-Z (high impedance)

2012 marks: 4.75

Question: Short note on: ECL (Emitter-coupled logic) circuit

⇒ Emitter-coupled logic circuit is a bipolar technology. The typical ECL circuit consists of a different amplifier input circuit, a bias circuit and emitter-follower outputs.

- The ECL is much faster than TTL, because the transistors do not operate in saturation and is used in more specialized high speed application.

- In this circuits, saturation is not possible. The lack of saturation results in higher power consumption and limited voltage swing (less than 1 V) but it permits high frequency switching.

2017 (5 marks)

Question: Design a Inverter NOT gate using MOSFET.

V.V.I

⇒ The inverter of MOSFET circuit shown in fig ⓐ: uses two MOS devices.

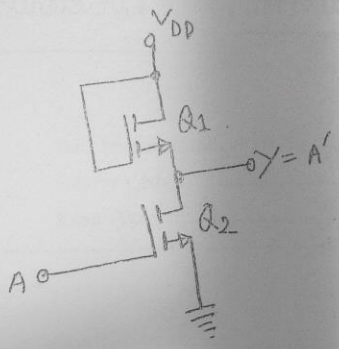


Fig ⓐ: Inverter MOS/MOSFET

Q_1 acts as the load resistor and Q_2 acts as the active device.

The load resistor MOS has its gate connected to V_{DD}, thus maintaining it always in the conduction state.

V_T = Threshold Voltage

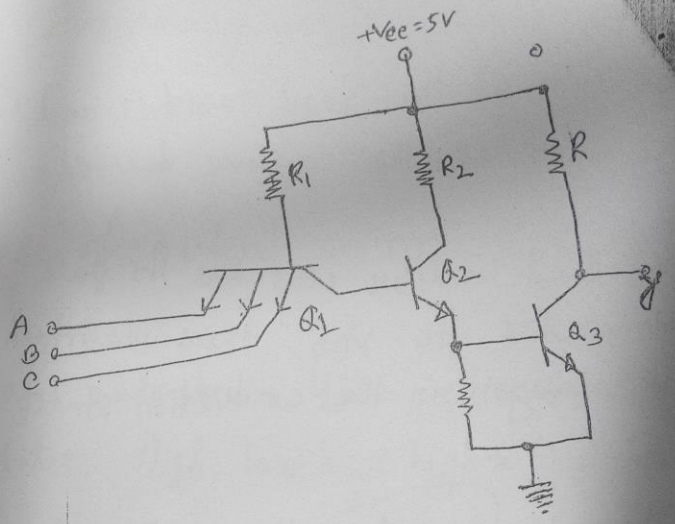
When the input voltage (A) is low (below V_T), Q_2 turns off. Since the Q_1 is always on, the output voltage is at about V_{DD}.

When the input voltage (A) is high, Q_2 turns on. Current flows from V_{DD} through the load resistor Q_1 and into Q_2.

The geometry of the two MOS devices must be such that the resistance of Q_2, when conducting is much less than the resistance of Q_1 to maintain the output Y at a voltage below V_T (Threshold voltage).

2014

Question: characteristics of TTL. Operations of Open col



fig@: Open collector TTL

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Class Test

Total Marks

Roll Number/Student ID No. .....

Course Code .....

Exam. Date .....

Signature of Invigilator

RUP-40,000/C.S. 413/Date: 15.10.2016

Question: Tristate - TTL gate: