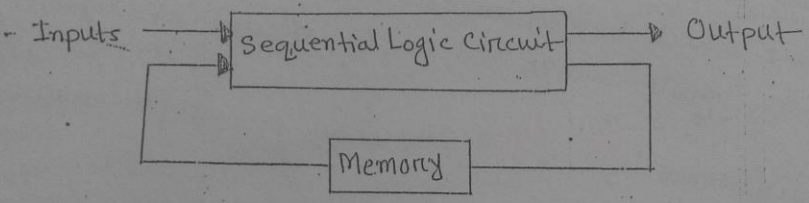
M

Mim 1

* what is sequential logic circuit ?

Ans: Sequential logic circuit: The present output depends not only on the present input but also on the previous logic states of the output are called sequential logic circuit. It consists of a combinational logic circuit and one memory element. It has feedback system.

Example of sequential logic circuit are SR, JK, D and T Flip Flop.



Block diagram of sequential logic circuit

* what is Flip Flop? Write the application of Flip Flop.

Ans: Flip Flop: The memory elements used in clocked sequential circuits are called Flip Flop. It has two outputs, one for the normal value and one for the complement value of the bit.

The application of Flip Flop are given below:—

i) Used for data storage.
ii) " " " transfer.
iii) " " frequency division
iv) " " flip flop synchronization
v) " in counting circuits.

1. What is synchronous and asynchronous logic circuit? Differentiate between them.

Ans: Synchronous Circuit: A synchronous circuit is a sequential logic circuit which behaviour can be defined from the knowledge of its signal at discrete instants of time.

Asynchronous circuit: A asynchronous circuit is a sequential circuit which behaviour can be defined from the knowledge of its signals change and can be affected at any instant of time.

The difference between synchronous and asynochronous circuit are given below:—

Synocronous circuit	Asynocronous circuit.
1. Definition:- - - - - - - - - -	1. Definition: - - - - - - - - -
2. It builts to operate at a clocked reate.	2. It builts to operate without clocking.
3. It is also known as clocked sequential circuit.	3. It is also known as unclocked sequential circuit.
4. It can not regarded as a combinational logic circuit with feedback.	4. It can regarded as a combinational logic circuit with feedback.
5. For example: Magnetic tape Readers.	5. For example: Touch tone telephone system.

* Write the classification of Flip Flop.

Ans: There are four types of flip flops. They are

i) SR Flip Flop
ii) JK " "
iii) D " " and
iv) T " ".

* Why flip flop is used in sequential circuit?

Ans: Flip flop is used in sequential circuit because it has clock pulse (c.p) which gives the present state output and next state output. Also it performs data transfers, data storage, frequency division and counting circuits.

* Some important definition *

State table: The time sequence of inputs, outputs and Flip Flop states may be represented in a state table. It consists of three section labeled i.e present state, next state and output. It is also known as Transition table.

State diagram: The information in a state table may be represented graphically in a state diagram. In this diagram, a state is represented by a circle. It provides the same information as the state table and often used as the initial design specification of a sequential circuit.

State equation: A state equation is an algebraic expression that specifies the conditions for a F-F state transition. The left side of the equation denotes the next state of a flip flop and the right side a boolean function.

Characteristics table: Characteristics table is one kind of logical table which is useful for analysis and defining the operation of Flip Flop.

Excitation table: Excitation table is one kind of logical table that lists the required inputs for a given changes of states. It consists of two column columns Q(t) and Q(t+1) and a column for each input to show how the required transition is achived.

Clock Pulse (CP): A clock pulse may be either positive or negative. The positive transition is defined as the positive edge and the negative transition as the negative edge.

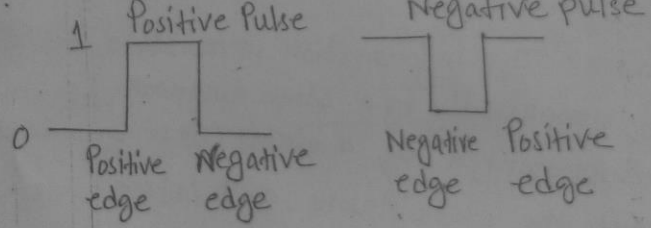
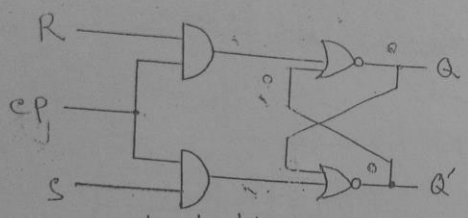


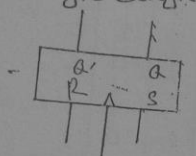
Fig: Definition of clock Pulse (CP)

* Describe the operation of clocked RS flip-flop with suitable logic diagram, characteristics table and equations. V.V.I

Ans: Clocked RS FlipFlop: It consists of basic NOR F-F and two AND gates. It has clock pulse system.



Logic diagram



Graphic symbol

Q \ SR	00	01	11	10
0			X	1
1	1		X	1

$Q(t+1) = S + QR'$

$SR = 0$

Characteristic equation

cp	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

Characteristics table

Operation:

i) Q is the present binary state of the F-F.

ii) Q(t+1) is the state of the F-F after the occurance of a clock pulse.

iii) In the set state $S = 1, R = 0$ and $CP = 1$.

iv) In the clear state $S = 0, R = 1$ and $CP = 1$

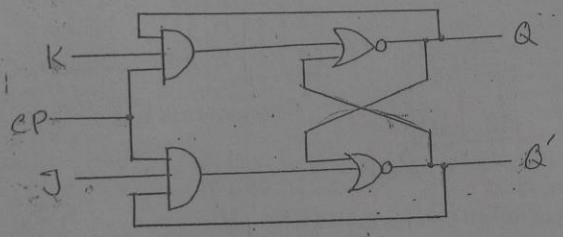
v) When the CP is removed, the state of the F-F is indeterminate.

vi) When $CP = 0$, regardless of the value S and R inputs.

vii) When $CP = 1$, the value S and R inputs is allowed to reach the basic F-F

*Describe the operation of JK F-F with suitable logic diagram, characteristics table and equation.

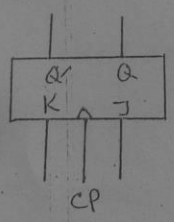
Ans: JK Flip Flop: A JK F-F is a refinement of the RS F-F in that the indeterminate state of the RS type is defined in the JK type.



Logic diagram

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

characteristics table



Graphic symbol

Q \ JK	00	01	11	10
0			1	1
1	1			1

$Q(t+1) = Q'J + QK'$

$= JQ' + K'Q$

characteristics ~~table~~ equation

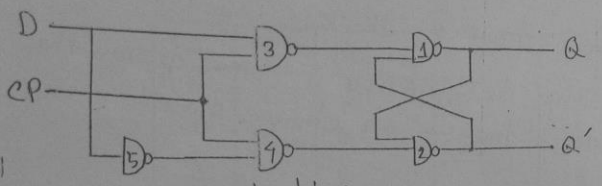
Operation: The JK F-F like as RS F-F except when both J and K are equal to 1.

when $J = 1, K = 1$ and $Q = 0$ then $Q(t+1) = 1$

Again when $J = 1, K = 1$ and $Q = 1$ the $Q(t+1) = 0$

* Describe the operation of D F-F with suitable logic diagram, characteristics table and equation.

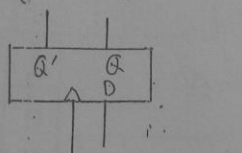
Ans: D-Flip flop: It is basically an RS F-F with an inverter in the R input.



Logic diagram

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Characteristics table



Graphic diagram

Q \ D	0	1
0		1
1		1

Q(t+1) = D

Characteristics equation

operation: NAND gates 1 and 2 form a basic F-F and gates 3 and 4 modify it into a clocked RS F-F. Gate 5 complement of input.

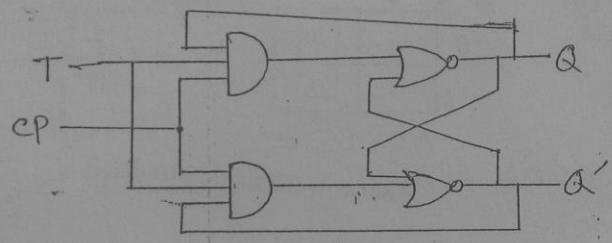
When cp = 0, then gate 3 and 4 have a 1. the output gate-3 goes to 0;

Again cp = 1 and D = 1, the F-F is switched to set state. the output gate-4 goes to 1,

If D = 0, the F-F is switched to clear state.

*Describe the operation of T F-F with suitable logic diagram, characteristics table and equation.

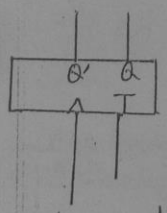
Ans: T Flip Flop: It is a single input version of the JK F-F which obtained from a JK type if both inputs are tied together. The designation T comes from the ability of the FF to 'toggle' or 'change state'.



Logic diagram

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristics table



Graphic diagram

Q \ T	0	1
0		1
1	1	

$Q(t+1) = Q'T + QT'$

Characteristic equation

Draw the Flip Flop characteristic table and excitation table for SR, JK, D and T Flip Flop.

Ans:

Characteristic Table

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	?

Excitation Table

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

D	Q(t+1)
0	0
1	1

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

* What is Master-Slave Flip Flop?

Ans: Master slave Flip Flop: A MS F-F is constructed from two seperate F-Fs. One as a Master and another as a slave and the overall circuit is called M-S F-F.

* Explain the operation of RSMS F-F with suitable logic diagram.

Ans: SR MS FF: RSMS F-F consists of a master flip flop, a slave flip flop and an inverter. The logic diagram of RSMSFF are shown in Fig-@.

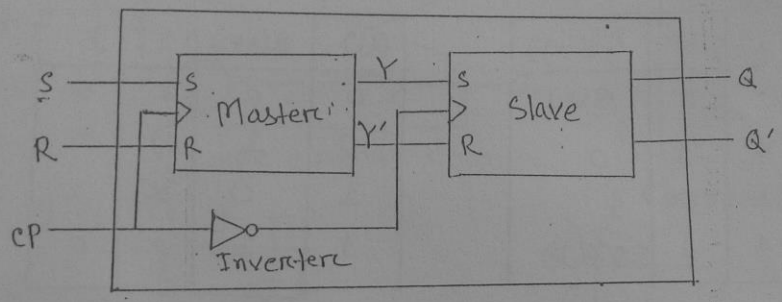
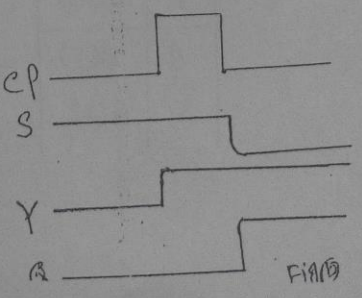


Fig-@: Logic diagram of RSMS FF.

Operation: When CP = 0, the output of the inverter is 1. In this case, Master F-F is disabled and it is isolated from slave FF and the slave F-F is enabled and the output $Q = Y$ and $Q' = Y'$.

Again, when CP = 1, the output of the inverter is 0. In this case, Master F-F is enabled and the slave F-F is disabled and it is isolated as long as CP = 1.

The timing relationships are shown in Fig(b):



Fig(b)

Explain the operation of MSJKFF with suitable logic diagram.

Ans: MSJKFF: The master slave JK Flip Flop constructed with NAND gates is shown in Fig-①. It consists of two F-F; gates 1 through 4 form the master F-F and gates 5 through 8 form the slave F-F.

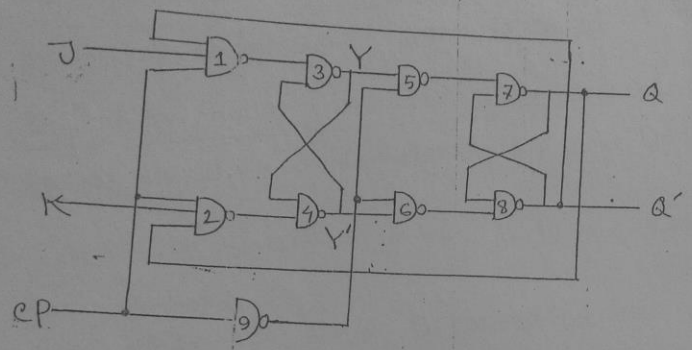


Fig-②: Logic diagram of MSJKFF.

Operation: The slave F-F is a clocked RS type. When the clock is 0, the output of gate 9 is 1 so that the output Q=Y and Q'=Y'. when CP = 1, the Master F-F is affected and may switch states. The slave FF is isolated. ~~as long as the clock is at the 1 level~~

Again when CP = 0, the Master FF is isolated from the J and K inputs and the slave FF goes to the same state as the master F-F.

* what is converter? what is Analog to Digital Converter. Digital to Analog converter?

Ans: Converter: A converter is a machine/Program which converts one signal to another signal.

Analog to Digital Converter: The process of conversion of a analog signal to digital signal is called A-to-D converter.

Digital to Analog Converter: The process of conversion of a digital signal to analog signal is called D-to-A converter.

* Explain the classification of A-to-D converter.

~~Ans: To Some~~

Ans: Kinds of A-to-D converter are given below:—

i) Parallel-Comparator A-to-D converter,
ii) Counting A-to-D " ,
iii) Dual Shope A-to-D " ,
iv) Successive-Approximation A-to-D " ,
v) Using Voltage to Time Conversion,
vi) " Voltage to Frequency " .

* Explain the classification of D-to-A converter.

Ans: Kinds of D-to-A converter are given below:—

i) Weighted Resistor D-to-A converter
ii) R-2R Ladder D-to-A " .

* Write the application of A/D and D/A converter.

Ans: The application of A to D converter :—

i) A-to-D converter are used together with different transducers to convert physical sence and measurement such as temperature, pressure, speed, sound, vibration, picture etc in digital signal for further processing by microprocessor.

ii) Some examples of A-to-D converter usage are digital Volt meters, cell phone, thermocouples and digital oscilloscope.

The application of D to A converter :—

i) Digital audio ← CD/MP3 players, HD radio, Digital telephones

ii) " Video — DVD player, DTV, Computer displays.

iii) Industrial Control system:— Motor. control, valves, transducer excitation.

iv) Waveform function generation, test equipment

v) Built in self test, Calibration/tuning in embedded systems.

* Explain the operation of Digital to Analog (D/A) converter.

Ans: Operation of D/A converter: The process of conversion of a digital signal into analog signal is called D/A converter. In D/A converter, the possible number of digital signal is fixed. For example, in a 4-bit D/A converter, there are $2^4 = 16$ possible inputs.

The equation for analog output voltage (V_o) or current (I_o) of an n-bit binary D/A converter is

$$V_o \text{ or } I_o = K\left(2^{n-1} b_{n-1} + 2^{n-2} b_{n-2} + \ldots\ldots + 2b_1 + b_0\right)$$

where K is a proportionally factor.

$b_n = 1$ if the nth bit of the digital input is 1

$= 0$ " " " " " " " " " " 0

The block diagram of D/A converter are given below:—

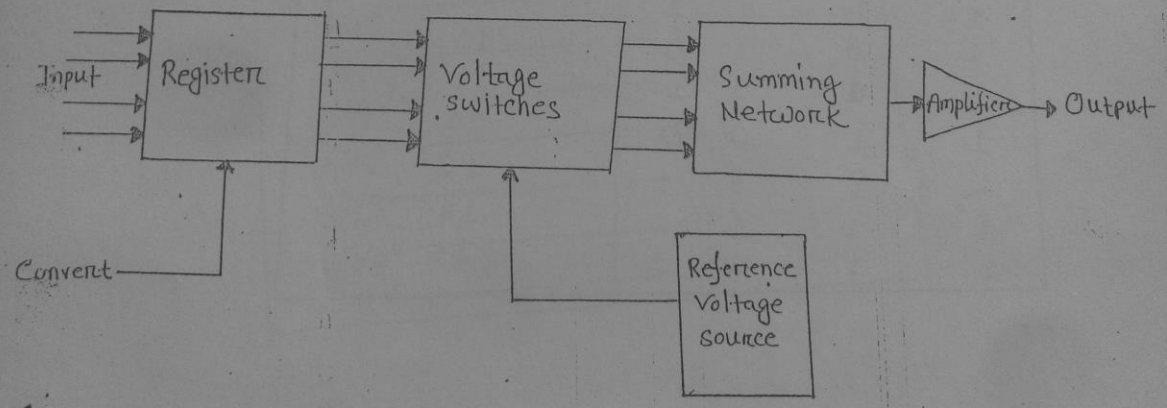


Fig: Block diagram of D/A converter

The analog output voltage (V_o) or current (I_o) for 4-bit D/A converter are shown in Table-1.

Table-1

Digital Input				Analog output
b_3	b_2	b_1	b_0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

*Explain the operation of Analog to Digital (A/D) converters.

Ans: Operation of A/D converters: The process of conversion of an analog signal into digital signal is called A/D converters. In an A/D converters, the input analog voltage can have any value in the range.

Consider an analog voltage in the range of 0 to V and a 3-bit digital output any voltage in this range.

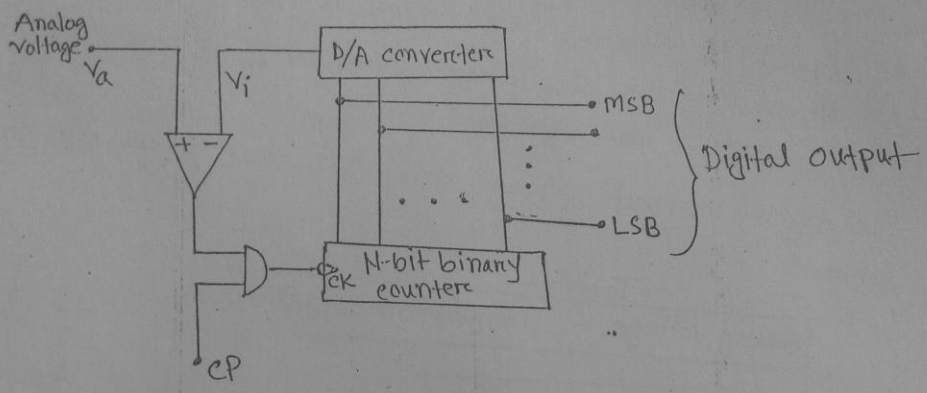
Let us, divide the hole range of analog voltage in an intervals (3-bit output) of the size $s = V/8$.

The digital output voltage for A/D converters are shown in Table-1.

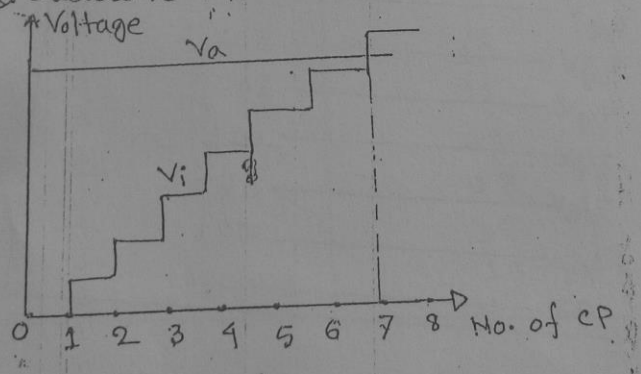
Table-1

Analog voltage	Equivalent digital value
V	
7/8 V	111
6/8 V	110
5/8 V	101
4/8 V	100
3/8 V	011
2/8 V	010
1/8 V	001
0 V	000

The block diagram and waveforms for A/D converter are given below:—



Fig(a): Successive-Approximation A/D converter



Fig(b): Waveform of counting A/D converter