Pandit Deendayal Energy University

School of Technology

RTL TO GDSII WORKSHOP

PROJECT REPORT

Design and Physical Implementation of an 8x1 Multiplexer for 8-bit Inputs

Including RTL Design in Verilog HDL and GDS-II Generation using Synopsys Flowscripts

Nihar Prajapati 23BEC173

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1 Introduction

The RTL to GDSII flow is a critical process in the design and manufacturing of integrated circuits. This project focuses on the design and physical implementation of an 8x1 multiplexer for 8-bit inputs using Verilog HDL and Synopsys tools. The process encompasses RTL design, verification, synthesis, and physical design, culminating in the generation of a GDS-II layout.

2 Objectives and Learning Outcomes

The primary objectives of this project are:

- To understand the complete RTL to GDSII flow for digital circuit design.
  - Design and verify an 8x1 multiplexer using Verilog HDL.
  - Synthesize the design using Synopsys Design Compiler.
  - Perform physical design and layout using Synopsys IC Compiler II.
- To gain hands-on experience with industry-standard EDA tools and methodologies.

The learning outcomes of this project include:

- Proficiency in using Verilog HDL for RTL design.
- Understanding the synthesis process and the use of Synopsys Design Compiler.
- Knowledge of physical design stages, including floorplanning, power planning, placement, CTS, and routing.
- Experience with static timing analysis using Synopsys PrimeTime.

3 Equipment and Tools

- Synopsys Design Compiler for synthesis.
- Synopsys IC Compiler II for physical design.
- Synopsys Verdi for verification and debugging.
- Synopsys PrimeTime for timing analysis.

4 Methodology

4.1 RTL Design and Verification

The Register Transfer Level (RTL) design of the 8x1 multiplexer was implemented using Verilog Hardware Description Language (HDL). The design process involved creating a functional description of the multiplexer, which selects one of the eight 8-bit inputs based on a 3-bit select signal and forwards the selected input to the output.

4.1.1 Design Logic

- **Input and Output Definitions:**
  - **Inputs:** The multiplexer has eight 8-bit data inputs (I0, I1, . . . , I7), a 3-bit select input (Sel), and a clock input (Clock).
  - **Output:** The multiplexer has one 8-bit output (y).
- **Multiplexer Logic:**
  - The 3-bit select signal (Sel) determines which of the eight inputs is connected to the output. The binary value of Sel corresponds to the input selected.

Verilog Code for 8x1 Multiplexer

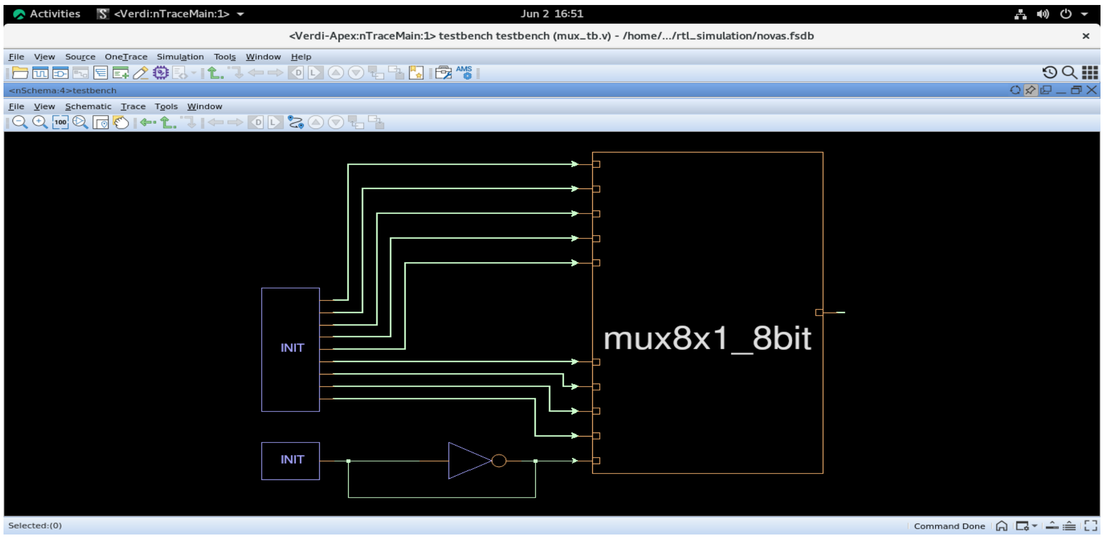
```
module mux8x1_8bit (
    input  wire [7:0] I0, I1, I2, I3, I4, I5, I6, I7,
    input  wire [2:0] Sel,
    input  wire       Clock,
    output reg  [7:0] y
);

    reg [7:0] mux_out;

    // Combinational MUX logic (outside clocked block)
    always @(*) begin
        case (Sel)
            3'd0: mux_out = I0;
            3'd1: mux_out = I1;
            3'd2: mux_out = I2;
            3'd3: mux_out = I3;
            3'd4: mux_out = I4;
            3'd5: mux_out = I5;
            3'd6: mux_out = I6;
            3'd7: mux_out = I7;
            default: mux_out = 8'b0;
        endcase
    end

    // Registered output (synchronous with clock)
    always @(posedge Clock) begin
        y <= mux_out;
    end

endmodule
```

4.1.2 Verification

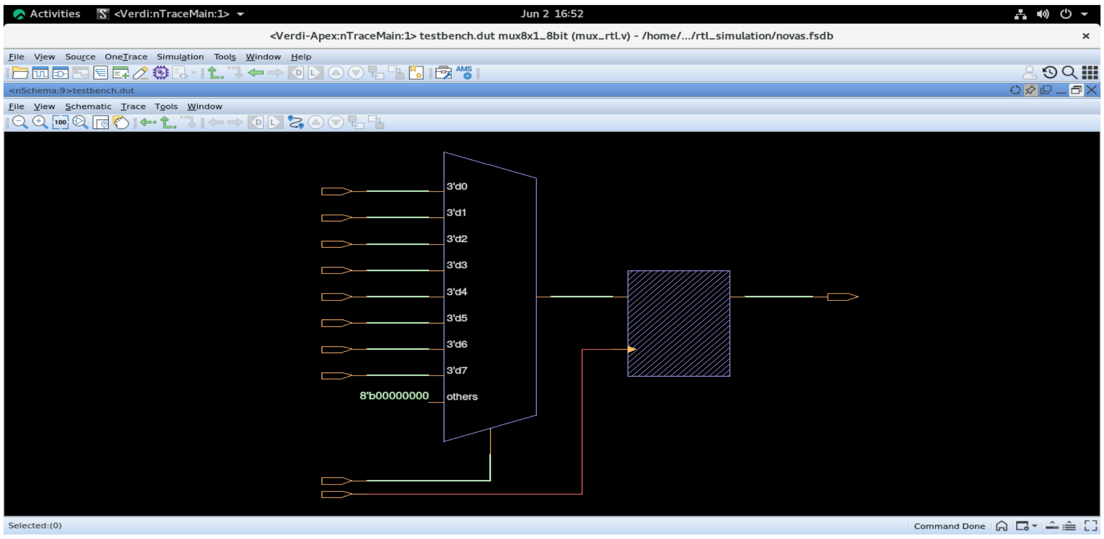
The RTL design was verified using a testbench and waveforms were analyzed using Synopsys Verdi. The testbench applied various input combinations to ensure that the multiplexer correctly selected the appropriate input based on the select signal.

Testbench Code

```
‘timescale 1ns/1ns
‘include "mux_rtl.v"

module testbench;

    reg  Clock;
    reg  [7:0]  I0, I1, I2, I3, I4, I5, I6, I7;
    reg  [2:0]  Sel;
    wire [7:0]  y;

    // Instantiate the Device Under Test (DUT)
    mux8x1_8bit dut (
        .Clock(Clock),
        .I0(I0), .I1(I1), .I2(I2), .I3(I3),
        .I4(I4), .I5(I5), .I6(I6), .I7(I7),
        .Sel(Sel),
        .y(y)
    );

    // Clock generation: toggle every 5 ns (10 ns period)
    initial Clock = 0;
    always #5 Clock = ~Clock;

    // Apply test vectors
    initial begin

    $fsdbDumpvars();
        // Initialize input values
        I0 = 8’hAA; I1 = 8’hBB; I2 = 8’hCC; I3 = 8’hDD;
        I4 = 8’hEE; I5 = 8’hFF; I6 = 8’h11; I7 = 8’h22;

     // Apply selection inputs with delay (one clock cycle each)
        Sel = 3’d0; #10;
        Sel = 3’d1; #10;
        Sel = 3’d2; #10;
        Sel = 3’d3; #10;
        Sel = 3’d4; #10;
        Sel = 3’d5; #10;
        Sel = 3’d6; #10;
        Sel = 3’d7; #10;

        $finish;
    end

endmodule
```


Activities
<Verdi:nTraceMain:1>
Jun 2 16:51
<Verdi-Apex:nTraceMain:1> testbench testbench (mux_tb.v) - /home/.../rtl_simulation/novas.fsdb
File View Source OneTrace Simulation Tools Window Help
<nSchema:4>testbench
File View Schematic Trace Tools Window
INIT
INIT
mux8x1_8bit
Selected:(0)
Command Done

(a) Schematic Outer View


Activities
<Verdi:nTraceMain:1>
Jun 2 16:52
<Verdi-Apex:nTraceMain:1> testbench.dut mux8x1_8bit (mux_rtl.v) - /home/.../rtl_simulation/novas.fsdb
File View Source OneTrace Simulation Tools Window Help
<nSchema:9>testbench.dut
File View Schematic Trace Tools Window
3'd0
3'd1
3'd2
3'd3
3'd4
3'd5
3'd6
3'd7
8'b00000000
others
Selected:(0)
Command Done

(b) Schematic Inner View

Figure 1: Schematic Views of 8x1 Multiplexer

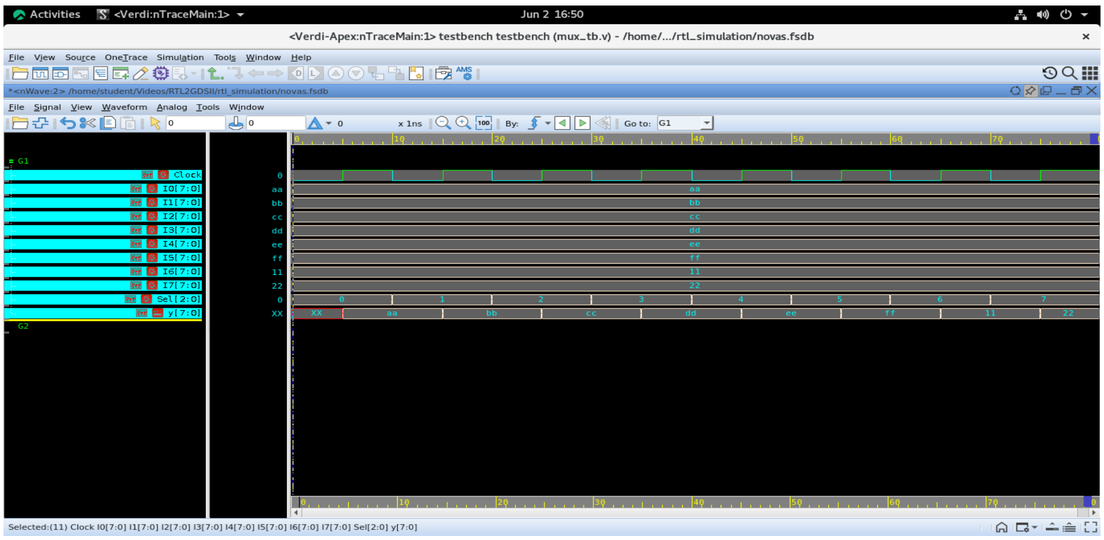

Activities
<Verdi:nTraceMain:1>
Jun 2 16:50
<Verdi-Apex:nTraceMain:1> testbench testbench (mux_tb.v) - /home/.../rtl_simulation/novas.fsdb
File View Source OneTrace Simulation Tools Window Help
*<nWave:2> /home/student/Videos/RTL2GDSII/rtl_simulation/novas.fsdb
File Signal View Waveform Analog Tools Window
x 1ns
By:
Go to: G1
G1
Clock
I0[7:0]
I1[7:0]
I2[7:0]
I3[7:0]
I4[7:0]
I5[7:0]
I6[7:0]
I7[7:0]
Sel[2:0]
y[7:0]
G2
0
aa
bb
cc
dd
ee
ff
11
22
0
XX
Selected:(11) Clock I0[7:0] I1[7:0] I2[7:0] I3[7:0] I4[7:0] I5[7:0] I6[7:0] I7[7:0] Sel[2:0] y[7:0]

Figure 2: Waveform of 8x1 Multiplexer

4.2 Synthesis using Design Compiler

- The RTL design was synthesized using Synopsys Design Compiler.
- The synthesis process involved optimizing the design for area, power, and timing.

Key Synthesis Metrics:

- **Slack:** Slack is the difference between the required time and the arrival time of a signal. A positive slack indicates the design meets timing requirements, while negative slack indicates a timing violation.
- **Leaf Cell Count:** This refers to the number of standard library cells (excluding hierarchy and module instances) used in the synthesized netlist. It's a measure of design complexity and size.
- **Area:** This is the total silicon area occupied by the synthesized cells. It is often reported in terms of μm^2 (square micrometers).
- **Units:** Units used in Design Compiler reports typically include:
  - Time – nanoseconds (ns)
  - Power – microwatts (µW) or milliwatts (mW)
  - Area – square micrometers (µm^2)

4.3 Overview of the Design Compiler TCL Script

The Design Compiler TCL script (`run_dc.tcl`) is a key automation script that controls the synthesis process converting RTL code into a gate-level netlist. The main operations in the script include:

- **Environment Setup and Library Configuration:**
  Initial setup involves defining the working library and loading necessary environment settings.
- **RTL File Analysis and Design Elaboration:**
  The RTL source files are analyzed and elaborated to form the internal design representation required for synthesis.
- **Leaf Cell Selection and Optimization:**
  Using `set_dont_use`, specific standard cells such as adders and logic gates are excluded to optimize the design's timing, area, or power by controlling the cell library usage.
- **Application of Timing Constraints:**
  The script reads the associated SDC file to impose timing constraints, guiding the synthesis tool to meet the required performance metrics.
- **Synthesis Compilation and Optimization:**
  The `compile_ultra` command triggers high-effort optimizations for improved timing and area results.

- **Reporting and Output Generation:**
  Post-synthesis timing and quality reports are generated, and the final netlist is exported for subsequent design stages.

This script enables a streamlined, repeatable synthesis flow ensuring timing closure and design quality.

Sample TCL Script for Synthesis

Design Compiler TCL Script (`run_dc.tcl`)

```
source -echo -verbose ./rm_setup/dc_setup.tcl
set RTL_SOURCE_FILES ./../rtl/mux_rtl.v

define_design_lib WORK -path ./WORK

set_dont_use [get_lib_cells */FADD*]
set_dont_use [get_lib_cells */HADD*]
set_dont_use [get_lib_cells */AO*]
set_dont_use [get_lib_cells */OA*]
set_dont_use [get_lib_cells */NAND*]
set_dont_use [get_lib_cells */XOR*]
#set_dont_use [get_lib_cells */NOR*]
set_dont_use [get_lib_cells */XNOR*]
set_dont_use [get_lib_cells */MUX*]

analyze -format verilog ${RTL_SOURCE_FILES}
elaborate ${DESIGN_NAME}
current_design

read_sdc ./../CONSTRAINTS/mux.sdc

compile_ultra
report_timing
write -format verilog -hierarchy -output
${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}
report_qor
```

4.4 Role and Importance of the Synopsys Design Constraints (SDC) File

The Synopsys Design Constraints (SDC) file defines timing and physical constraints that direct the synthesis and timing analysis processes. Key components of the SDC file include:

- **Clock Definition:**
  Defines the primary clock period and timing reference using the `create_clock` command.
- **Input and Output Timing Constraints:**
  Specifies the maximum input and output delays relative to the clock to account for external timing factors.

- **Signal Transition Constraints:**
  Sets the maximum input transition times and internal signal slew rates, enabling accurate timing modeling.
- **Clock Uncertainty Settings:**
  Models clock jitter and skew to ensure conservative and reliable timing analysis.

Properly defining these constraints ensures the synthesized design meets timing requirements and functions correctly at the target clock frequency.

Sample SDC File for Timing Constraints

Timing Constraints File (mux.sdc)

```
create_clock -period 1.9 [get_ports Clock]

set_input_delay -max 0.5 -clock Clock [all_inputs]
set_input_transition 0.5 [all_inputs]

set_output_delay -max 0.5 -clock Clock [all_outputs]

set_clock_uncertainty -setup 0.300 [get_clocks Clock]
set_clock_uncertainty -hold 0.100 [get_clocks Clock]

set_max_transition 0.250 [current_design]
set_max_transition -clock_path 0.150 [get_clocks Clock]
```

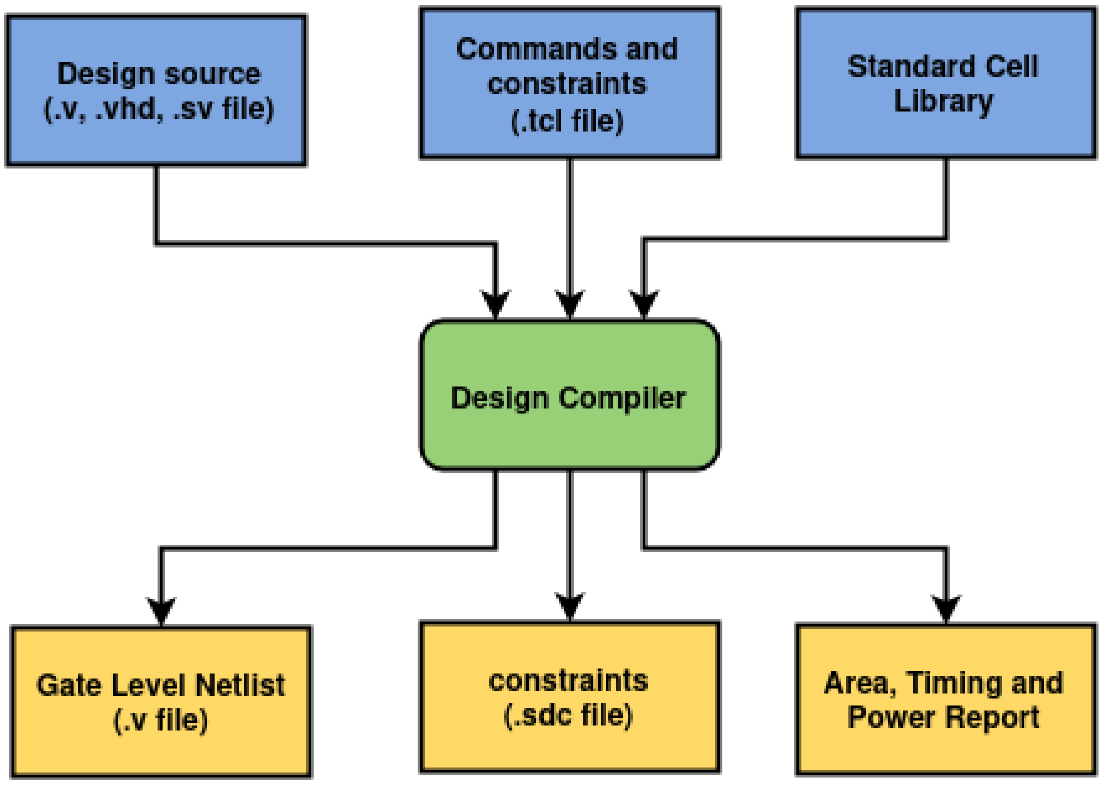
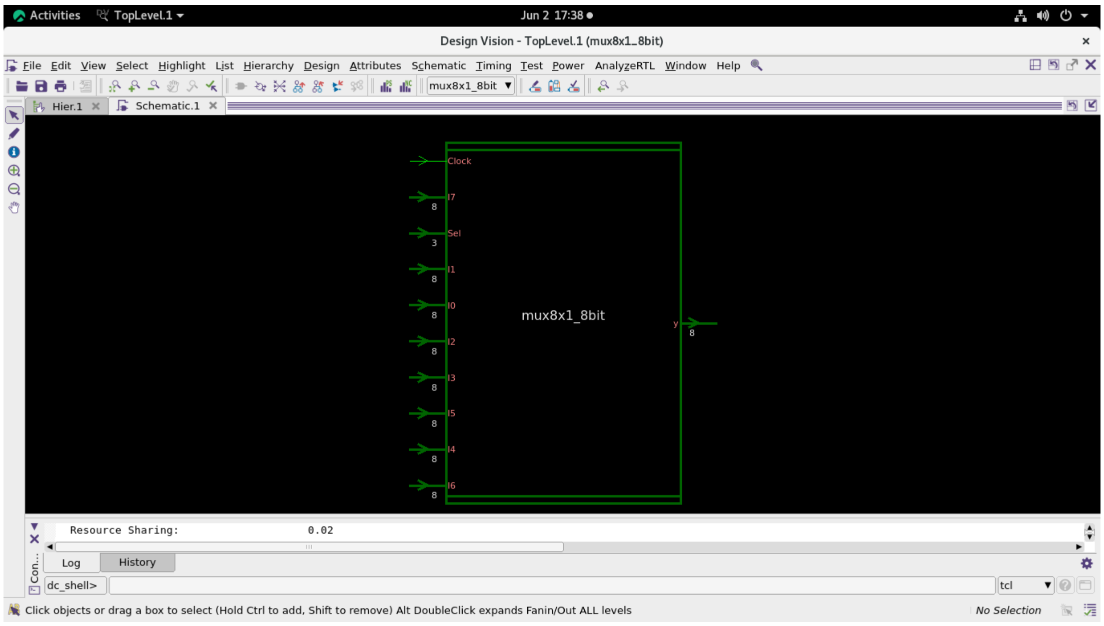


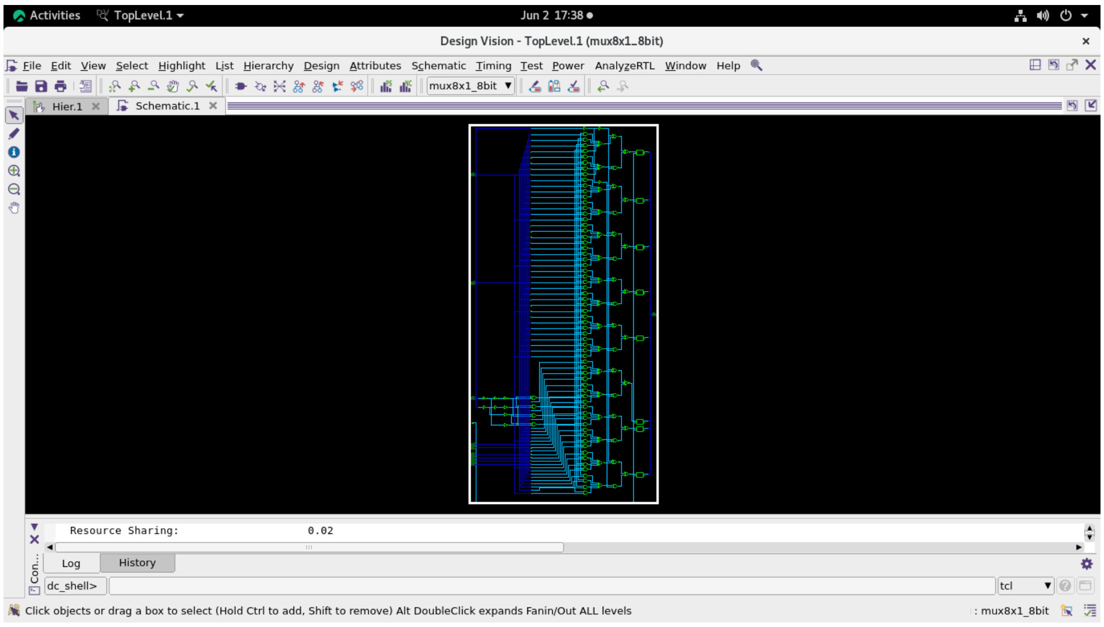
Figure 3: Synthesis Results in Design Compiler


Activities
TopLevel.1
Jun 2 17:38
Design Vision - TopLevel.1 (mux8x1_8bit)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
mux8x1_8bit
Hier.1
Schematic.1
Clock
I7
8
Sel
3
I1
8
I0
8
I2
8
I3
8
I5
8
I4
8
I6
8
mux8x1_8bit
y
8
Log
History
dc_shell>
tcl
No Selection

```
Resource Sharing:                    0.02
```

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels

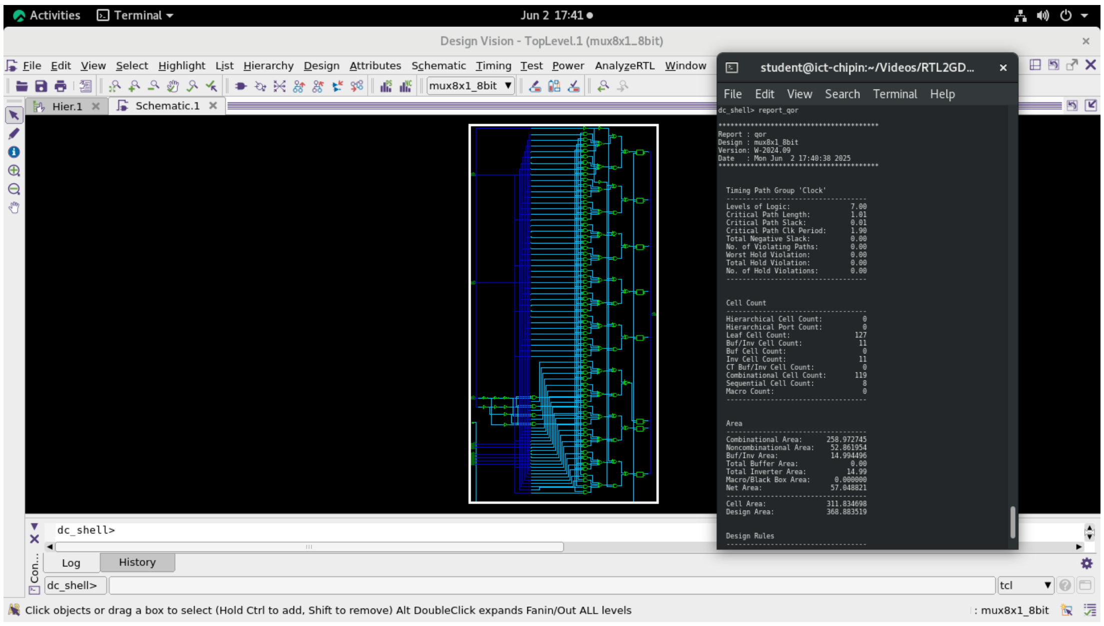
Figure 4: Synthesized Schematic


Activities
TopLevel.1
Jun 2 17:38
Design Vision - TopLevel.1 (mux8x1_8bit)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
mux8x1_8bit
Hier.1
Schematic.1
Log
History
dc_shell>
tcl
: mux8x1_8bit

```
Resource Sharing:                    0.02
```

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels

Figure 5: Inner View of Synthesized Schematic

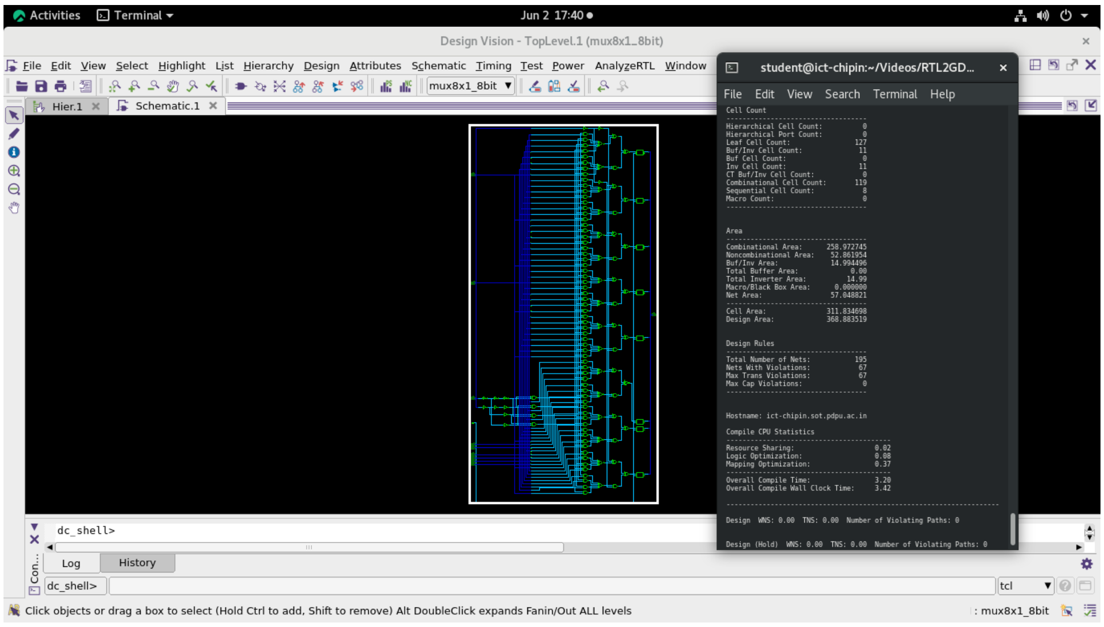

Activities
Terminal
Jun 2 17:41
Design Vision - TopLevel.1 (mux8x1_8bit)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window
mux8x1_8bit
Hier.1
Schematic.1
student@ict-chipin:~/Videos/RTL2GD...
File Edit View Search Terminal Help
Log
History
tcl
: mux8x1_8bit

```
dc_shell> report_qor

****************************************
Report : qor
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:40:38 2025
****************************************


  Timing Path Group 'Clock'
  -----------------------------------
  Levels of Logic:               7.00
  Critical Path Length:          1.01
  Critical Path Slack:           0.01
  Critical Path Clk Period:      1.90
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:          0
  Hierarchical Port Count:          0
  Leaf Cell Count:                127
  Buf/Inv Cell Count:              11
  Buf Cell Count:                   0
  Inv Cell Count:                  11
  CT Buf/Inv Cell Count:            0
  Combinational Cell Count:       119
  Sequential Cell Count:            8
  Macro Count:                      0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:      258.972745
  Noncombinational Area:    52.861954
  Buf/Inv Area:             14.994496
  Total Buffer Area:             0.00
  Total Inverter Area:          14.99
  Macro/Black Box Area:      0.000000
  Net Area:                 57.048821
  -----------------------------------
  Cell Area:               311.834698
  Design Area:             368.883519


  Design Rules
  -----------------------------------
```

```
dc_shell>
```

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels

Figure 6: QoR Report - Part 1

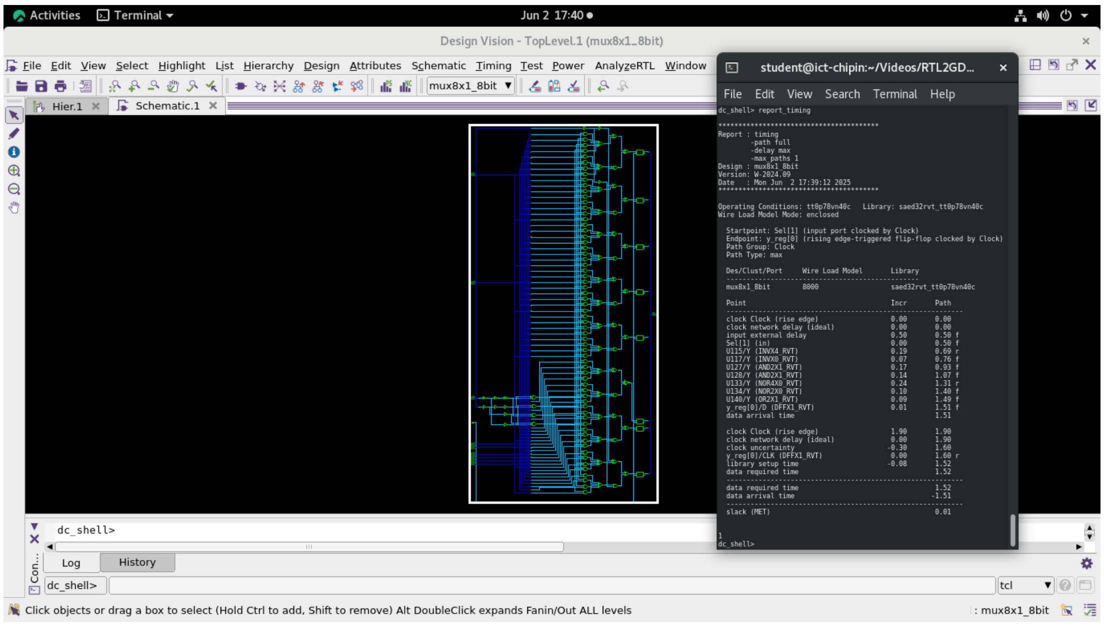

Activities
Terminal
Jun 2 17:40
Design Vision - TopLevel.1 (mux8x1_8bit)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window
mux8x1_8bit
Hier.1
Schematic.1
student@ict-chipin:~/Videos/RTL2GD...
File Edit View Search Terminal Help
Log
History
tcl
: mux8x1_8bit

```
  Cell Count
  -----------------------------------
  Hierarchical Cell Count:          0
  Hierarchical Port Count:          0
  Leaf Cell Count:                127
  Buf/Inv Cell Count:              11
  Buf Cell Count:                   0
  Inv Cell Count:                  11
  CT Buf/Inv Cell Count:            0
  Combinational Cell Count:       119
  Sequential Cell Count:            8
  Macro Count:                      0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:      258.972745
  Noncombinational Area:    52.861954
  Buf/Inv Area:             14.994496
  Total Buffer Area:             0.00
  Total Inverter Area:          14.99
  Macro/Black Box Area:      0.000000
  Net Area:                 57.048821
  -----------------------------------
  Cell Area:               311.834698
  Design Area:             368.883519


  Design Rules
  -----------------------------------
  Total Number of Nets:           195
  Nets With Violations:            67
  Max Trans Violations:            67
  Max Cap Violations:               0
  -----------------------------------


  Hostname: ict-chipin.sot.pdpu.ac.in

  Compile CPU Statistics
  --------------------------------------
  Resource Sharing:                 0.02
  Logic Optimization:               0.08
  Mapping Optimization:             0.37
  --------------------------------------
  Overall Compile Time:             3.20
  Overall Compile Wall Clock Time:  3.42

  --------------------------------------------------------------------

  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


  Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0
```

```
dc_shell>
```

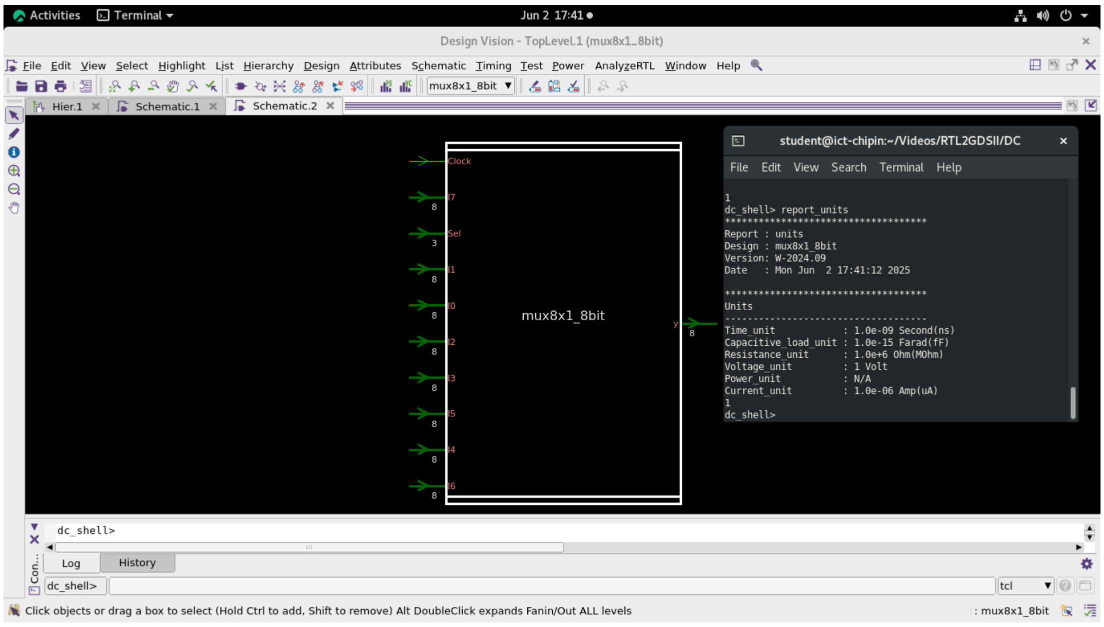
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels

Figure 7: QoR Report - Part 2


Activities
Terminal
Jun 2 17:40
Design Vision - TopLevel.1 (mux8x1_8bit)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window
mux8x1_8bit
Hier.1
Schematic.1
student@ict-chipin:~/Videos/RTL2GD...
File Edit View Search Terminal Help
dc_shell>
Log
History
dc_shell>
tcl
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels
: mux8x1_8bit

```
dc_shell> report_timing

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:39:12 2025
****************************************

Operating Conditions: tt0p78vn40c   Library: saed32rvt_tt0p78vn40c
Wire Load Model Mode: enclosed

  Startpoint: Sel[1] (input port clocked by Clock)
  Endpoint: y_reg[0] (rising edge-triggered flip-flop clocked by Clock)
  Path Group: Clock
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mux8x1_8bit        8000                  saed32rvt_tt0p78vn40c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock Clock (rise edge)                  0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.50       0.50 f
  Sel[1] (in)                              0.00       0.50 f
  U115/Y (INVX4_RVT)                       0.19       0.69 r
  U117/Y (INVX0_RVT)                       0.07       0.76 f
  U127/Y (AND2X1_RVT)                      0.17       0.93 f
  U128/Y (AND2X1_RVT)                      0.14       1.07 f
  U133/Y (NOR4X0_RVT)                      0.24       1.31 r
  U134/Y (NOR2X0_RVT)                      0.10       1.40 f
  U140/Y (OR2X1_RVT)                       0.09       1.49 f
  y_reg[0]/D (DFFX1_RVT)                   0.01       1.51 f
  data arrival time                                   1.51

  clock Clock (rise edge)                  1.90       1.90
  clock network delay (ideal)              0.00       1.90
  clock uncertainty                       -0.30       1.60
  y_reg[0]/CLK (DFFX1_RVT)                 0.00       1.60 r
  library setup time                      -0.08       1.52
  data required time                                  1.52
  -----------------------------------------------------------
  data required time                                  1.52
  data arrival time                                  -1.51
  -----------------------------------------------------------
  slack (MET)                                         0.01


1
dc_shell>
```

Figure 8: Report Timing Results


Activities
Terminal
Jun 2 17:41
Design Vision - TopLevel.1 (mux8x1_8bit)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
mux8x1_8bit
Hier.1
Schematic.1
Schematic.2
Clock
I7
8
Sel
3
I1
8
I0
8
I2
8
I3
8
I5
8
I4
8
I6
8
mux8x1_8bit
y
8
student@ict-chipin:~/Videos/RTL2GDSII/DC
File Edit View Search Terminal Help
dc_shell>
Log
History
dc_shell>
tcl
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels
: mux8x1_8bit

```
1
dc_shell> report_units
****************************************
Report : units
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:41:12 2025

****************************************
Units
-----------------------------------
Time_unit           : 1.0e-09 Second(ns)
Capacitive_load_unit : 1.0e-15 Farad(fF)
Resistance_unit     : 1.0e+6 Ohm(MOhm)
Voltage_unit        : 1 Volt
Power_unit          : N/A
Current_unit        : 1.0e-06 Amp(uA)
1
dc_shell>
```

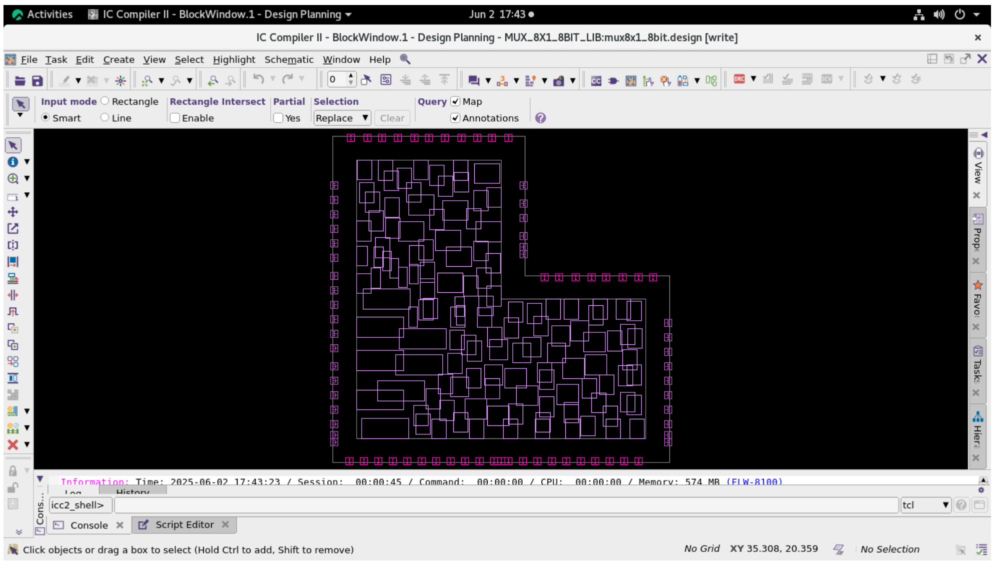
Figure 9: Report Units Results

5 Physical Design using IC Compiler II

The physical implementation of the synthesized netlist was carried out using Synopsys IC Compiler II (ICC2). The flow consists of several backend stages including floorplanning, power planning, placement, clock tree synthesis (CTS), and routing.

5.1 Floorplanning

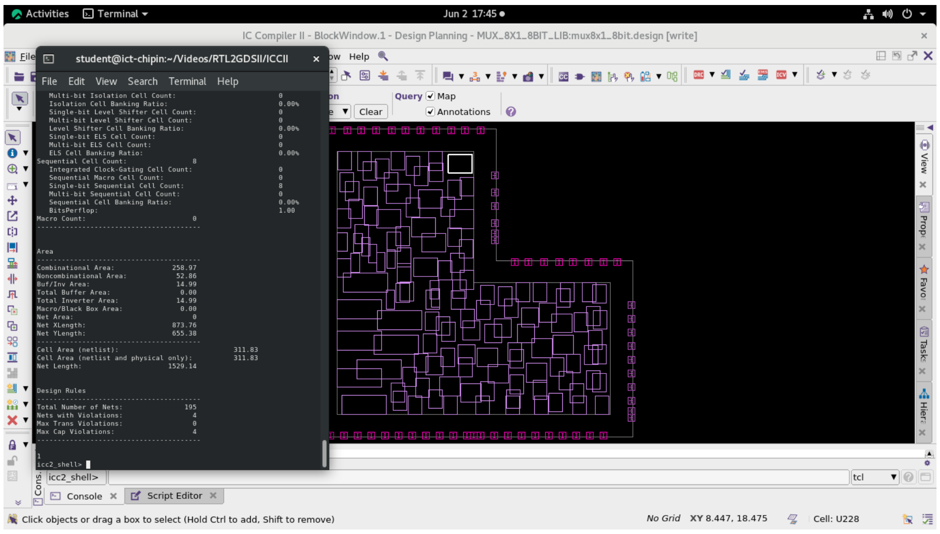
Floorplanning defines the die area, core area, IO pin locations, and placement blockages. It is the first step in defining the physical layout.



```
Information: Time: 2025-06-02 17:43:23 / Session:  00:00:45 / Command:  00:00:00 / CPU:  00:00:00 / Memory: 574 MB (FLW-8100)
```

Figure 10: Floorplan View 1

Reports:

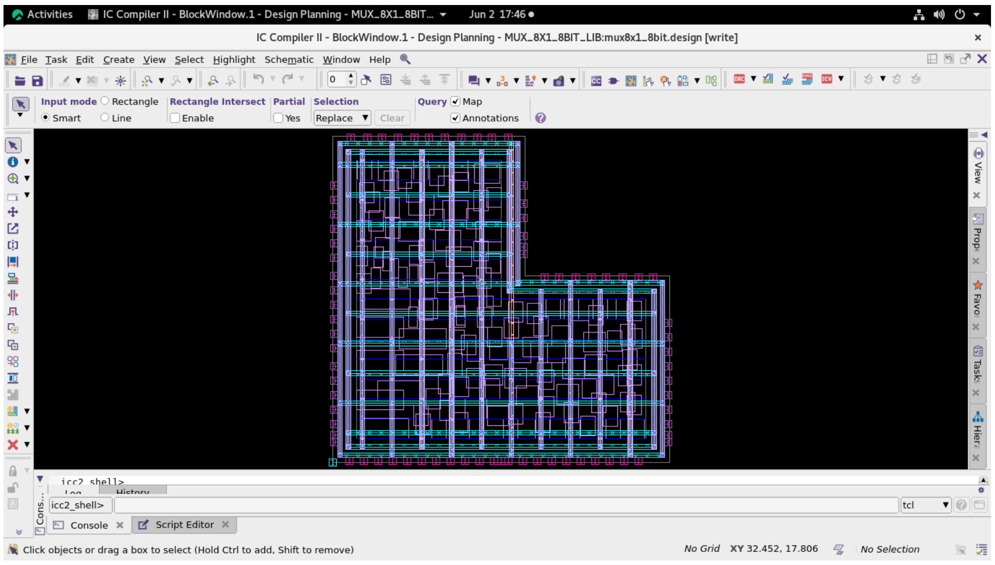


```
   Multi-bit Isolation Cell Count:                      0
   Isolation Cell Banking Ratio:                        0.00%
   Single-bit Level Shifter Cell Count:                 0
   Multi-bit Level Shifter Cell Count:                  0
   Level Shifter Cell Banking Ratio:                    0.00%
   Single-bit ELS Cell Count:                           0
   Multi-bit ELS Cell Count:                            0
   ELS Cell Banking Ratio:                              0.00%
Sequential Cell Count:                  8
   Integrated Clock-Gating Cell Count:                  0
   Sequential Macro Cell Count:                         0
   Single-bit Sequential Cell Count:                    8
   Multi-bit Sequential Cell Count:                     0
   Sequential Cell Banking Ratio:                       0.00%
   BitsPerflop:                                         1.00
Macro Count:                            0
----------------------------------------


Area
----------------------------------------
Combinational Area:                258.97
Noncombinational Area:              52.86
Buf/Inv Area:                       14.99
Total Buffer Area:                   0.00
Total Inverter Area:                14.99
Macro/Black Box Area:                0.00
Net Area:                               0
Net XLength:                       873.76
Net YLength:                       655.38
----------------------------------------
Cell Area (netlist):                              311.83
Cell Area (netlist and physical only):            311.83
Net Length:                       1529.14


Design Rules
----------------------------------------
Total Number of Nets:                 195
Nets with Violations:                   4
Max Trans Violations:                   0
Max Cap Violations:                     4
----------------------------------------

1
icc2_shell> 
```

Figure 11: Floorplan - QoR Report

5.2 Power Planning

This step creates power and ground rings, straps, and connections to ensure IR drop is minimized and current delivery is efficient.



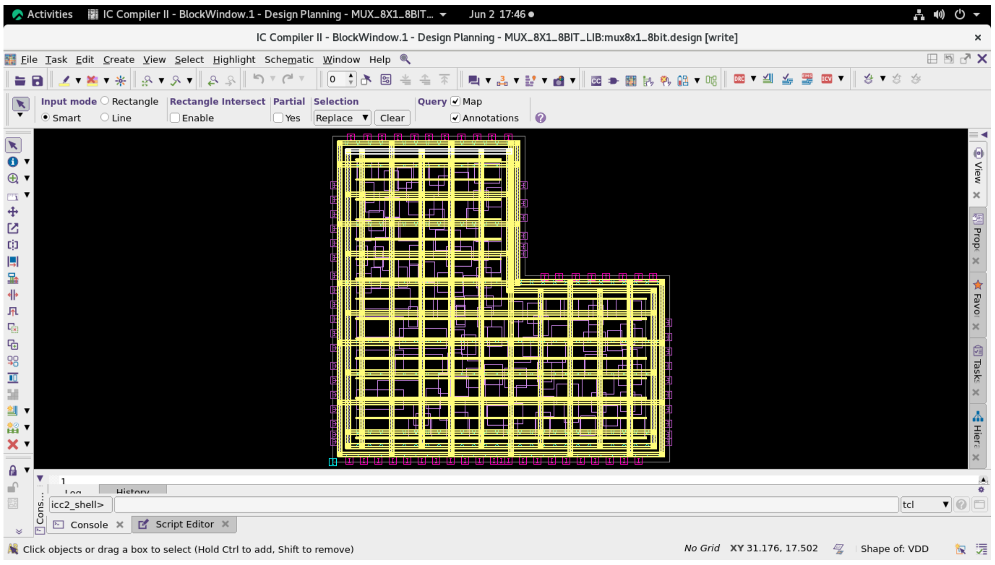
IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux8x1_8bit.design [write]

```
icc2_shell>
```

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)

XY 32.452, 17.806

Figure 12: Power Plan View 1



IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux8x1_8bit.design [write]

```
1
icc2_shell>
```

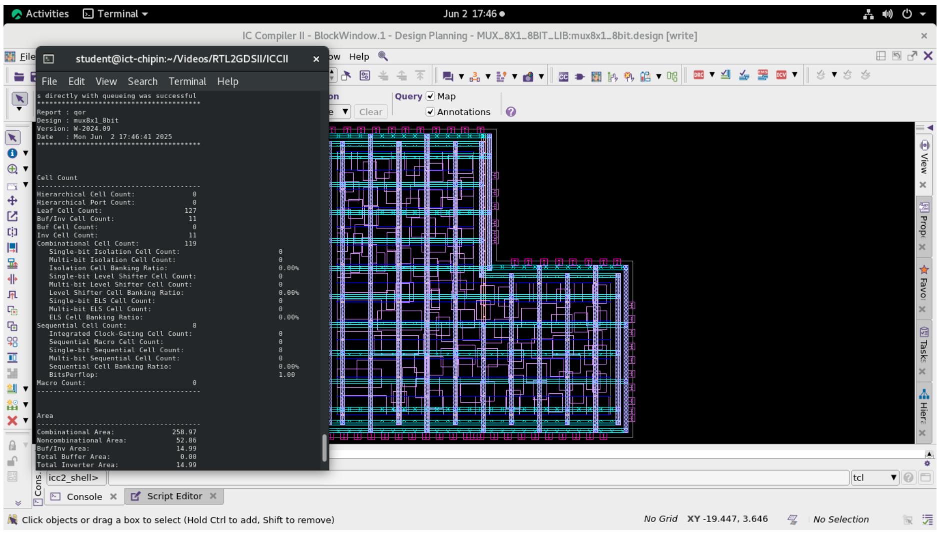
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)

XY 31.176, 17.502

Shape of: VDD

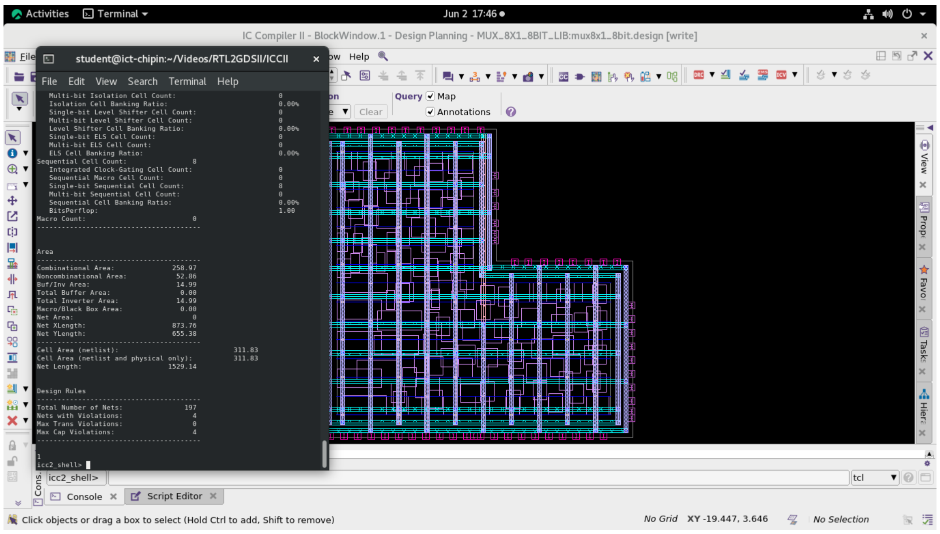
Figure 13: Power Plan Nets Highlighted View

Reports:


Activities
Terminal
Jun 2 17:46
IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux8x1_8bit.design [write]
student@ict-chipin:~/Videos/RTL2GDSII/ICCII
File Edit View Search Terminal Help
icc2_shell>
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid XY -19.447, 3.646
No Selection

```
s directly with queueing was successful
****************************************
Report : qor
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:46:41 2025
****************************************



Cell Count
----------------------------------------
Hierarchical Cell Count:               0
Hierarchical Port Count:               0
Leaf Cell Count:                     127
Buf/Inv Cell Count:                   11
Buf Cell Count:                        0
Inv Cell Count:                       11
Combinational Cell Count:            119
   Single-bit Isolation Cell Count:                     0
   Multi-bit Isolation Cell Count:                      0
   Isolation Cell Banking Ratio:                        0.00%
   Single-bit Level Shifter Cell Count:                 0
   Multi-bit Level Shifter Cell Count:                  0
   Level Shifter Cell Banking Ratio:                    0.00%
   Single-bit ELS Cell Count:                           0
   Multi-bit ELS Cell Count:                            0
   ELS Cell Banking Ratio:                              0.00%
Sequential Cell Count:                 8
   Integrated Clock-Gating Cell Count:                  0
   Sequential Macro Cell Count:                         0
   Single-bit Sequential Cell Count:                    8
   Multi-bit Sequential Cell Count:                     0
   Sequential Cell Banking Ratio:                       0.00%
   BitsPerflop:                                         1.00
Macro Count:                           0
----------------------------------------



Area
----------------------------------------
Combinational Area:               258.97
Noncombinational Area:             52.86
Buf/Inv Area:                      14.99
Total Buffer Area:                  0.00
Total Inverter Area:               14.99
```

Figure 14: Power Planning - QoR Report


Activities
Terminal
Jun 2 17:46
IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux8x1_8bit.design [write]
student@ict-chipin:~/Videos/RTL2GDSII/ICCII
File Edit View Search Terminal Help
icc2_shell>
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid XY -19.447, 3.646
No Selection

```
   Multi-bit Isolation Cell Count:                      0
   Isolation Cell Banking Ratio:                        0.00%
   Single-bit Level Shifter Cell Count:                 0
   Multi-bit Level Shifter Cell Count:                  0
   Level Shifter Cell Banking Ratio:                    0.00%
   Single-bit ELS Cell Count:                           0
   Multi-bit ELS Cell Count:                            0
   ELS Cell Banking Ratio:                              0.00%
Sequential Cell Count:                 8
   Integrated Clock-Gating Cell Count:                  0
   Sequential Macro Cell Count:                         0
   Single-bit Sequential Cell Count:                    8
   Multi-bit Sequential Cell Count:                     0
   Sequential Cell Banking Ratio:                       0.00%
   BitsPerflop:                                         1.00
Macro Count:                           0
----------------------------------------



Area
----------------------------------------
Combinational Area:               258.97
Noncombinational Area:             52.86
Buf/Inv Area:                      14.99
Total Buffer Area:                  0.00
Total Inverter Area:               14.99
Macro/Black Box Area:               0.00
Net Area:                              0
Net XLength:                      873.76
Net YLength:                      655.38
----------------------------------------
Cell Area (netlist):                            311.83
Cell Area (netlist and physical only):          311.83
Net Length:                      1529.14


Design Rules
----------------------------------------
Total Number of Nets:                197
Nets with Violations:                  4
Max Trans Violations:                  0
Max Cap Violations:                    4
----------------------------------------


1
icc2_shell>
```

Figure 15: Power Planning - QoR Report

5.3 Placement

Placement determines the exact location of each standard cell, optimizing wire length, timing, congestion, and power.

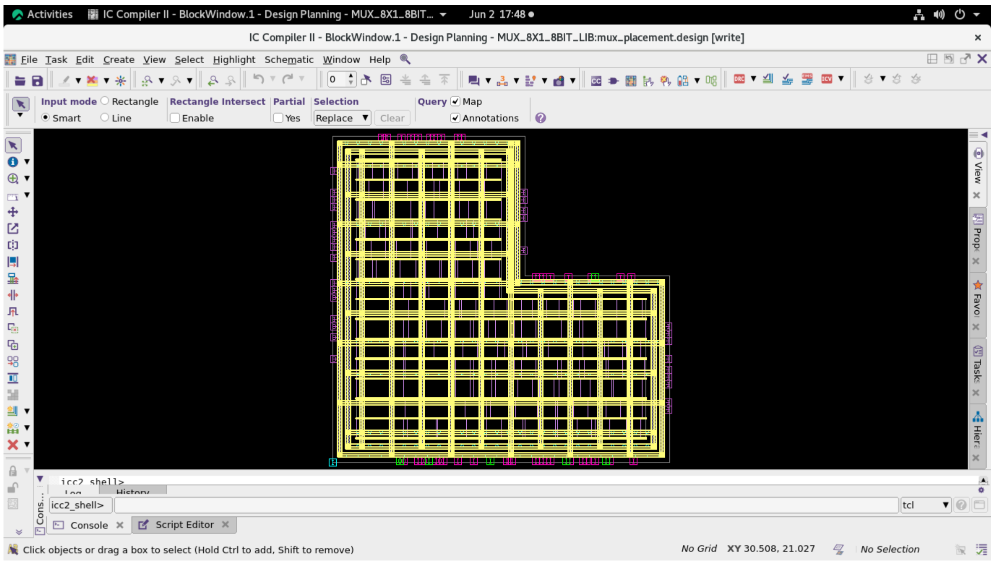
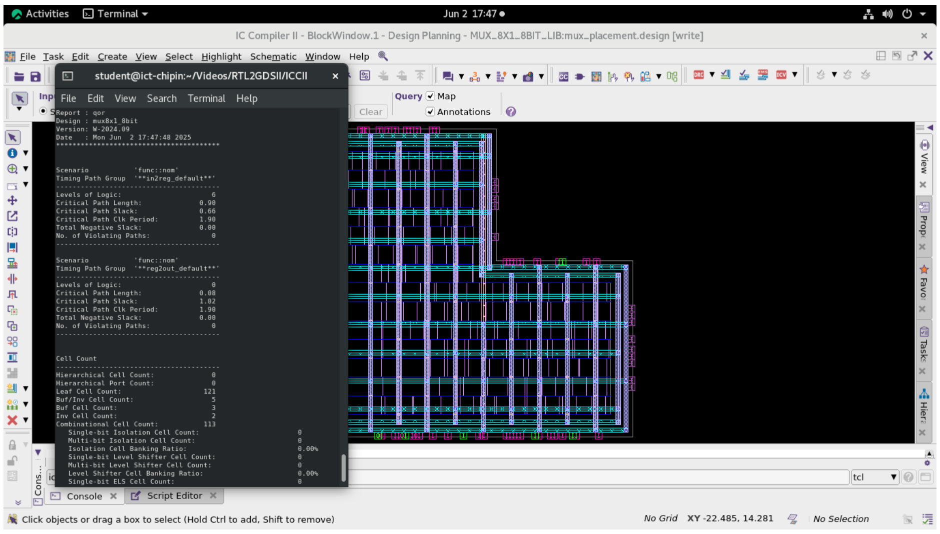

IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux_placement.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
icc2_shell>
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid XY 30.508, 21.027
No Selection

Figure 16: Placement View 1

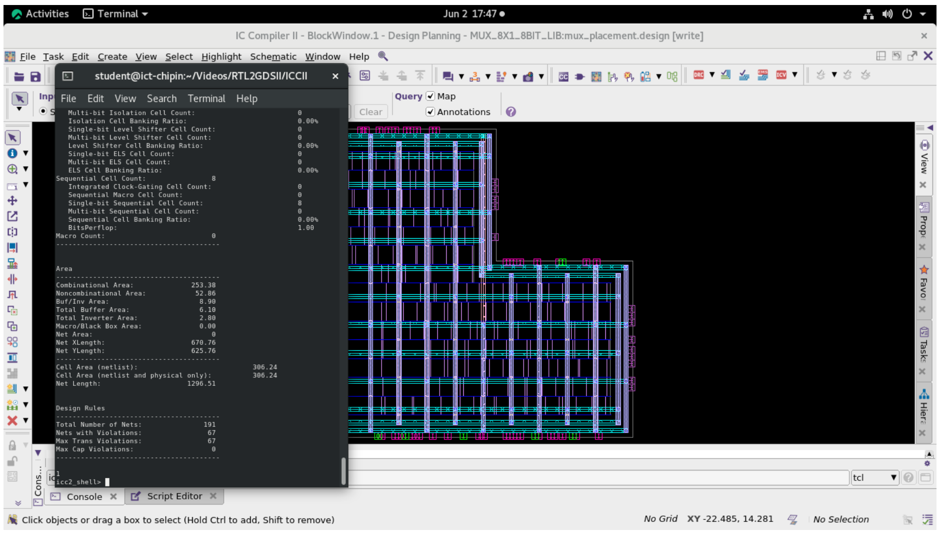
Reports:


student@ict-chipin:~/Videos/RTL2GDSII/ICCII
File Edit View Search Terminal Help

```
Report : qor
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:47:48 2025
****************************************


Scenario           'func::nom'
Timing Path Group  '**in2reg_default**'
----------------------------------------
Levels of Logic:                       6
Critical Path Length:               0.90
Critical Path Slack:                0.66
Critical Path Clk Period:           1.90
Total Negative Slack:               0.00
No. of Violating Paths:                0
----------------------------------------

Scenario           'func::nom'
Timing Path Group  '**reg2out_default**'
----------------------------------------
Levels of Logic:                       0
Critical Path Length:               0.08
Critical Path Slack:                1.02
Critical Path Clk Period:           1.90
Total Negative Slack:               0.00
No. of Violating Paths:                0
----------------------------------------


Cell Count
----------------------------------------
Hierarchical Cell Count:               0
Hierarchical Port Count:               0
Leaf Cell Count:                     121
Buf/Inv Cell Count:                    5
Buf Cell Count:                        3
Inv Cell Count:                        2
Combinational Cell Count:            113
   Single-bit Isolation Cell Count:                      0
   Multi-bit Isolation Cell Count:                       0
   Isolation Cell Banking Ratio:                         0.00%
   Single-bit Level Shifter Cell Count:                  0
   Multi-bit Level Shifter Cell Count:                   0
   Level Shifter Cell Banking Ratio:                     0.00%
   Single-bit ELS Cell Count:                            0
```

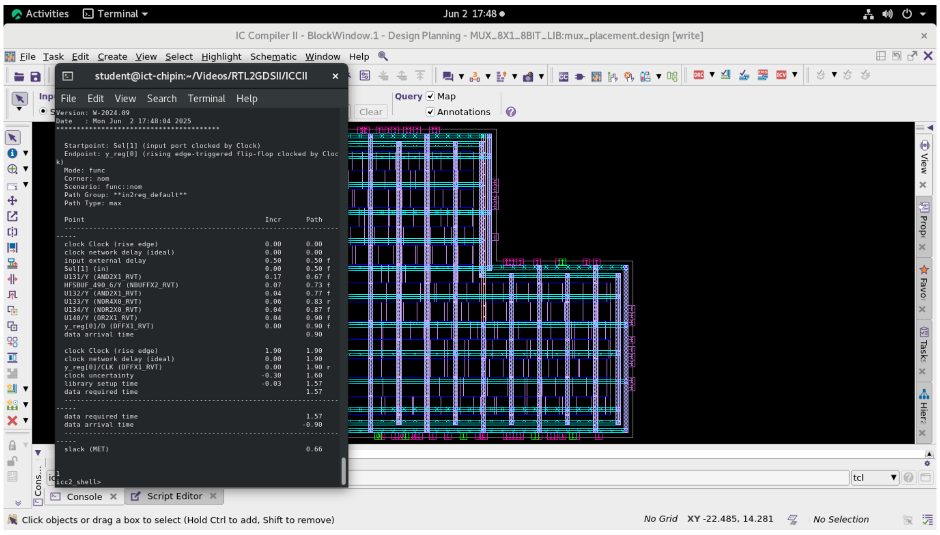
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid XY -22.485, 14.281
No Selection

Figure 17: Placement - QoR Report



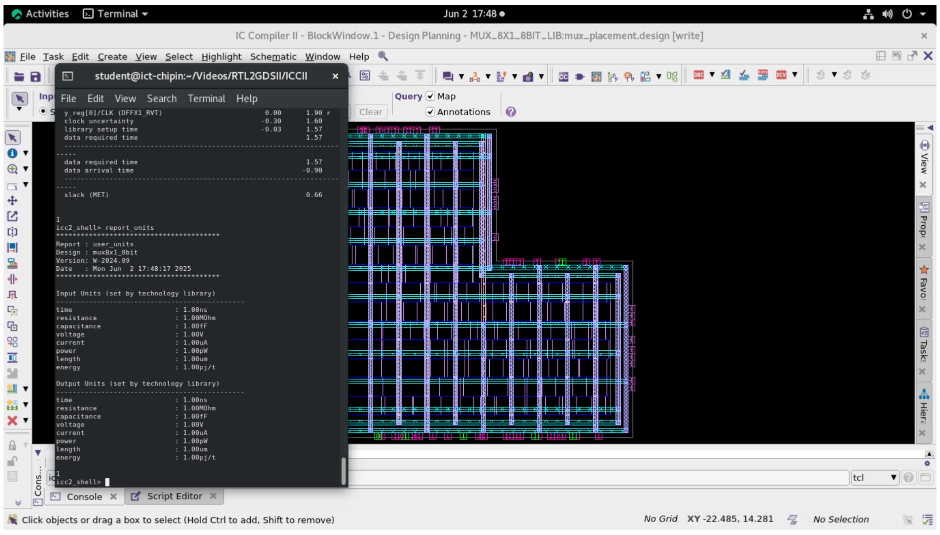
```
  Multi-bit Isolation Cell Count:                     0
  Isolation Cell Banking Ratio:                       0.00%
  Single-bit Level Shifter Cell Count:                0
  Multi-bit Level Shifter Cell Count:                 0
  Level Shifter Cell Banking Ratio:                   0.00%
  Single-bit ELS Cell Count:                          0
  Multi-bit ELS Cell Count:                           0
  ELS Cell Banking Ratio:                             0.00%
Sequential Cell Count:                   8
  Integrated Clock-Gating Cell Count:                 0
  Sequential Macro Cell Count:                        0
  Single-bit Sequential Cell Count:                   8
  Multi-bit Sequential Cell Count:                    0
  Sequential Cell Banking Ratio:                      0.00%
  BitsPerflop:                                        1.00
Macro Count:                             0
----------------------------------------


Area
----------------------------------------
Combinational Area:                 253.38
Noncombinational Area:               52.86
Buf/Inv Area:                         8.90
Total Buffer Area:                    6.10
Total Inverter Area:                  2.80
Macro/Black Box Area:                 0.00
Net Area:                                0
Net XLength:                        670.76
Net YLength:                        625.76
----------------------------------------
Cell Area (netlist):                               306.24
Cell Area (netlist and physical only):             306.24
Net Length:                        1296.51


Design Rules
----------------------------------------
Total Number of Nets:                  191
Nets with Violations:                   67
Max Trans Violations:                   67
Max Cap Violations:                      0
----------------------------------------

1
icc2_shell>
```

Figure 18: Placement - QoR Report



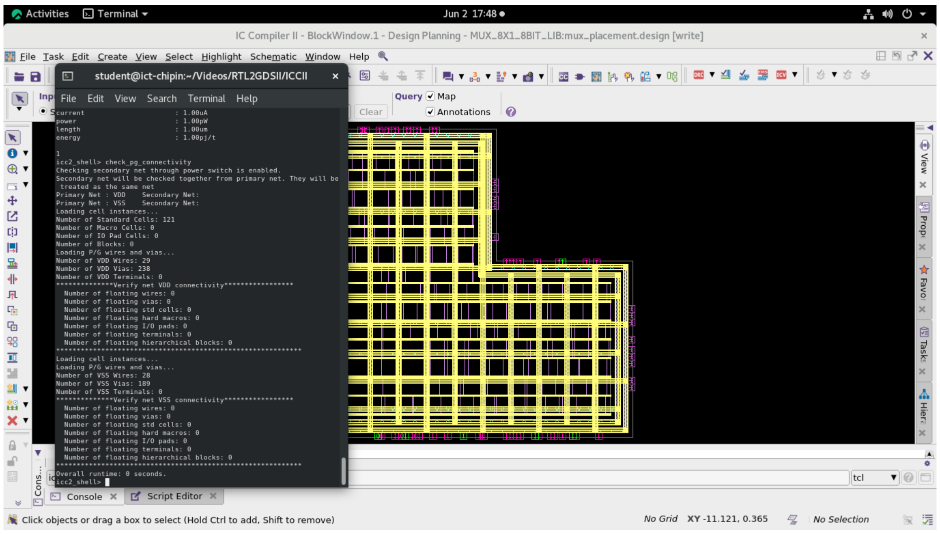
```
Version: W-2024.09
Date   : Mon Jun  2 17:48:04 2025
****************************************

  Startpoint: Sel[1] (input port clocked by Clock)
  Endpoint: y_reg[0] (rising edge-triggered flip-flop clocked by Cloc
k)
  Mode: func
  Corner: nom
  Scenario: func::nom
  Path Group: **in2reg_default**
  Path Type: max

  Point                                          Incr      Path
  -------------------------------------------------------------------
-----
  clock Clock (rise edge)                        0.00      0.00
  clock network delay (ideal)                    0.00      0.00
  input external delay                           0.50      0.50 f
  Sel[1] (in)                                    0.00      0.50 f
  U131/Y (AND2X1_RVT)                            0.17      0.67 f
  HFSBUF_490_6/Y (NBUFFX2_RVT)                   0.07      0.73 f
  U132/Y (AND2X1_RVT)                            0.04      0.77 f
  U133/Y (NOR4X0_RVT)                            0.06      0.83 r
  U134/Y (NOR2X0_RVT)                            0.04      0.87 f
  U140/Y (OR2X1_RVT)                             0.04      0.90 f
  y_reg[0]/D (DFFX1_RVT)                         0.00      0.90 f
  data arrival time                                        0.90

  clock Clock (rise edge)                        1.90      1.90
  clock network delay (ideal)                    0.00      1.90
  y_reg[0]/CLK (DFFX1_RVT)                       0.00      1.90 r
  clock uncertainty                             -0.30      1.60
  library setup time                            -0.03      1.57
  data required time                                       1.57
  -------------------------------------------------------------------
-----
  data required time                                       1.57
  data arrival time                                       -0.90
  -------------------------------------------------------------------
-----
  slack (MET)                                              0.66


1
icc2_shell>
```

Figure 19: Placement - Timing Report



```
  y_reg[0]/CLK (DFFX1_RVT)                       0.00      1.90 r
  clock uncertainty                             -0.30      1.60
  library setup time                            -0.03      1.57
  data required time                                       1.57
  -------------------------------------------------------------------
-----
  data required time                                       1.57
  data arrival time                                       -0.90
  -------------------------------------------------------------------
-----
  slack (MET)                                              0.66


1
icc2_shell> report_units
****************************************
Report : user_units
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:48:17 2025
****************************************

Input Units (set by technology library)
---------------------------------------------
time                          : 1.00ns
resistance                    : 1.00MOhm
capacitance                   : 1.00fF
voltage                       : 1.00V
current                       : 1.00uA
power                         : 1.00pW
length                        : 1.00um
energy                        : 1.00pj/t

Output Units (set by technology library)
---------------------------------------------
time                          : 1.00ns
resistance                    : 1.00MOhm
capacitance                   : 1.00fF
voltage                       : 1.00V
current                       : 1.00uA
power                         : 1.00pW
length                        : 1.00um
energy                        : 1.00pj/t

1
icc2_shell>
```

Figure 20: Placement - Units Report



```
current                        : 1.00uA
power                          : 1.00pW
length                         : 1.00um
energy                         : 1.00pj/t

1
icc2_shell> check_pg_connectivity
Checking secondary net through power switch is enabled.
Secondary net will be checked together from primary net. They will be
 treated as the same net
Primary Net : VDD    Secondary Net:
Primary Net : VSS    Secondary Net:
Loading cell instances...
Number of Standard Cells: 121
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 29
Number of VDD Vias: 238
Number of VDD Terminals: 0
**************Verify net VDD connectivity*****************
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 0
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 28
Number of VSS Vias: 189
Number of VSS Terminals: 0
**************Verify net VSS connectivity*****************
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 0
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
Overall runtime: 0 seconds.
icc2_shell>
```

Figure 21: Placement - Connectivity Report

5.4 Clock Tree Synthesis (CTS)

CTS adds clock buffers and routes clock nets to balance skew and meet clock latency constraints across sequential elements.

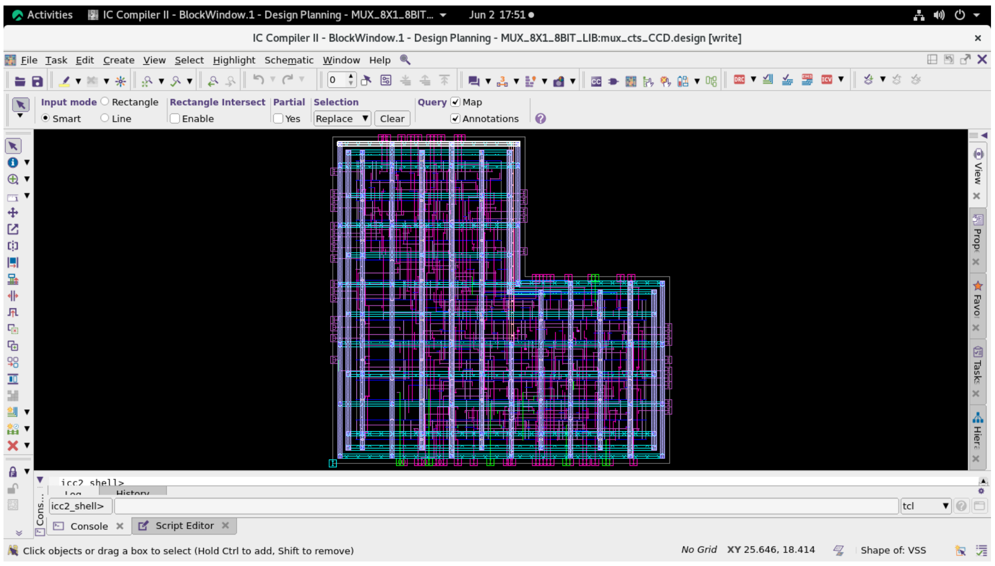

IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux_cts_CCD.design [write]
Jun 2 17:51
No Grid XY 25.646, 18.414
Shape of: VSS

Figure 22: CTS View

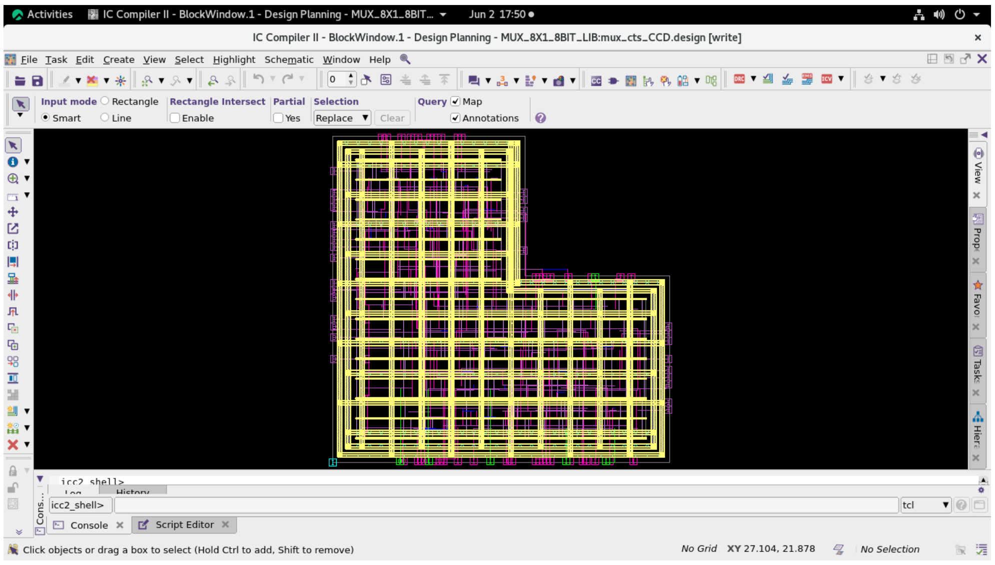
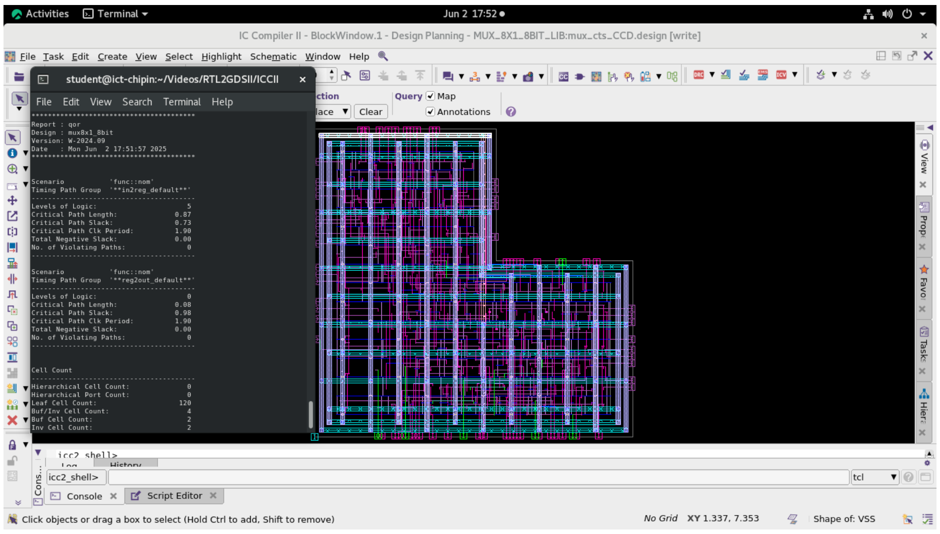

IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux_cts_CCD.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid XY 27.104, 21.878
No Selection

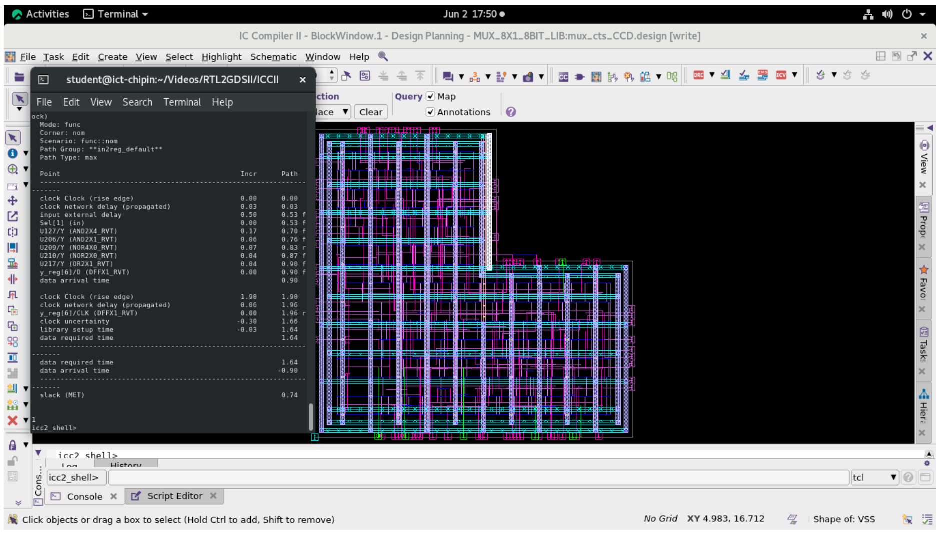
Figure 23: CTS Highlighted View

Reports:


student@ict-chipin:~/Videos/RTL2GDSII/ICCII
File Edit View Search Terminal Help
IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux_cts_CCD.design [write]
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid XY 1.337, 7.353
Shape of: VSS

```
****************************************
Report : qor
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:51:57 2025
****************************************


Scenario           'func::nom'
Timing Path Group  '**in2reg_default**'
----------------------------------------
Levels of Logic:                       5
Critical Path Length:               0.87
Critical Path Slack:                0.73
Critical Path Clk Period:           1.90
Total Negative Slack:               0.00
No. of Violating Paths:                0
----------------------------------------

Scenario           'func::nom'
Timing Path Group  '**reg2out_default**'
----------------------------------------
Levels of Logic:                       0
Critical Path Length:               0.08
Critical Path Slack:                0.98
Critical Path Clk Period:           1.90
Total Negative Slack:               0.00
No. of Violating Paths:                0
----------------------------------------


Cell Count
----------------------------------------
Hierarchical Cell Count:               0
Hierarchical Port Count:               0
Leaf Cell Count:                     120
Buf/Inv Cell Count:                    4
Buf Cell Count:                        2
Inv Cell Count:                        2
```

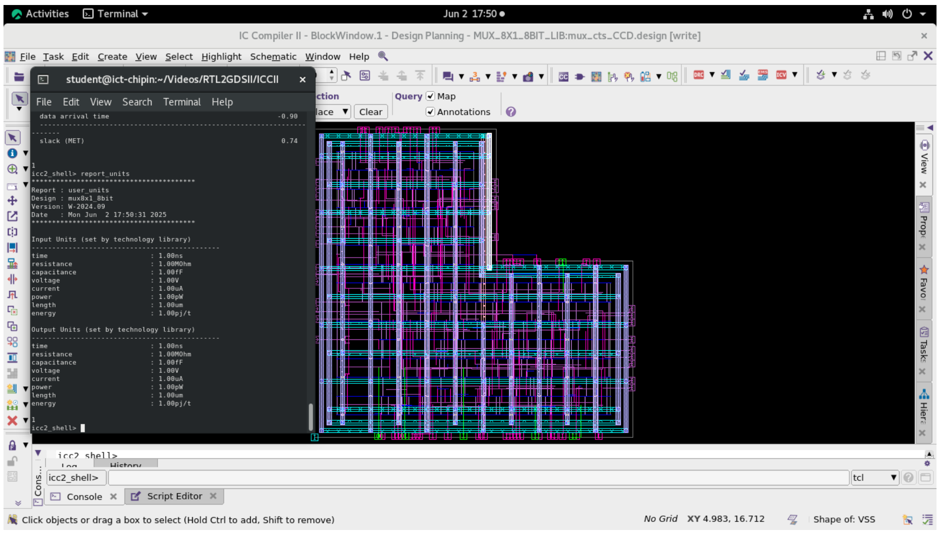
Figure 24: CTS - QoR Report


Activities
Terminal
Jun 2 17:50
IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux_cts_CCD.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
student@ict-chipin:~/Videos/RTL2GDSII/ICCII
File Edit View Search Terminal Help
Query
Map
Annotations
Clear
Console
Script Editor
No Grid XY 4.983, 16.712
Shape of: VSS

```
ock)
  Mode: func
  Corner: nom
  Scenario: func::nom
  Path Group: **in2reg_default**
  Path Type: max

  Point                                              Incr       Path
  ------------------------------------------------------------------
-------
  clock Clock (rise edge)                            0.00       0.00
  clock network delay (propagated)                   0.03       0.03
  input external delay                               0.50       0.53 f
  Sel[1] (in)                                        0.00       0.53 f
  U127/Y (AND2X4_RVT)                                0.17       0.70 f
  U206/Y (AND2X1_RVT)                                0.06       0.76 f
  U209/Y (NOR4X0_RVT)                                0.07       0.83 r
  U210/Y (NOR2X0_RVT)                                0.04       0.87 f
  U217/Y (OR2X1_RVT)                                 0.04       0.90 f
  y_reg[6]/D (DFFX1_RVT)                             0.00       0.90 f
  data arrival time                                             0.90

  clock Clock (rise edge)                            1.90       1.90
  clock network delay (propagated)                   0.06       1.96
  y_reg[6]/CLK (DFFX1_RVT)                           0.00       1.96 r
  clock uncertainty                                 -0.30       1.66
  library setup time                                -0.03       1.64
  data required time                                            1.64
  ------------------------------------------------------------------
-------
  data required time                                            1.64
  data arrival time                                            -0.90
  ------------------------------------------------------------------
-------
  slack (MET)                                                   0.74


1
icc2_shell>
```

```
icc2_shell>
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
```

Figure 25: CTS - Timing Report


Activities
Terminal
Jun 2 17:50
IC Compiler II - BlockWindow.1 - Design Planning - MUX_8X1_8BIT_LIB:mux_cts_CCD.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
student@ict-chipin:~/Videos/RTL2GDSII/ICCII
File Edit View Search Terminal Help
Query
Map
Annotations
Clear
Console
Script Editor
No Grid XY 4.983, 16.712
Shape of: VSS

```
  data arrival time                                            -0.90
  ------------------------------------------------------------------
-------
  slack (MET)                                                   0.74


1
icc2_shell> report_units
****************************************
Report : user_units
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:50:31 2025
****************************************

Input Units (set by technology library)
-----------------------------------------------------
time                              : 1.00ns
resistance                        : 1.00MOhm
capacitance                       : 1.00fF
voltage                           : 1.00V
current                           : 1.00uA
power                             : 1.00pW
length                            : 1.00um
energy                            : 1.00pj/t

Output Units (set by technology library)
-----------------------------------------------------
time                              : 1.00ns
resistance                        : 1.00MOhm
capacitance                       : 1.00fF
voltage                           : 1.00V
current                           : 1.00uA
power                             : 1.00pW
length                            : 1.00um
energy                            : 1.00pj/t

1
icc2_shell>
```

```
icc2_shell>
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
```

Figure 26: CTS - Units Report

5.5 Routing

Routing connects the logical nets physically using metal layers. This stage completes the layout and prepares it for GDS-II generation.

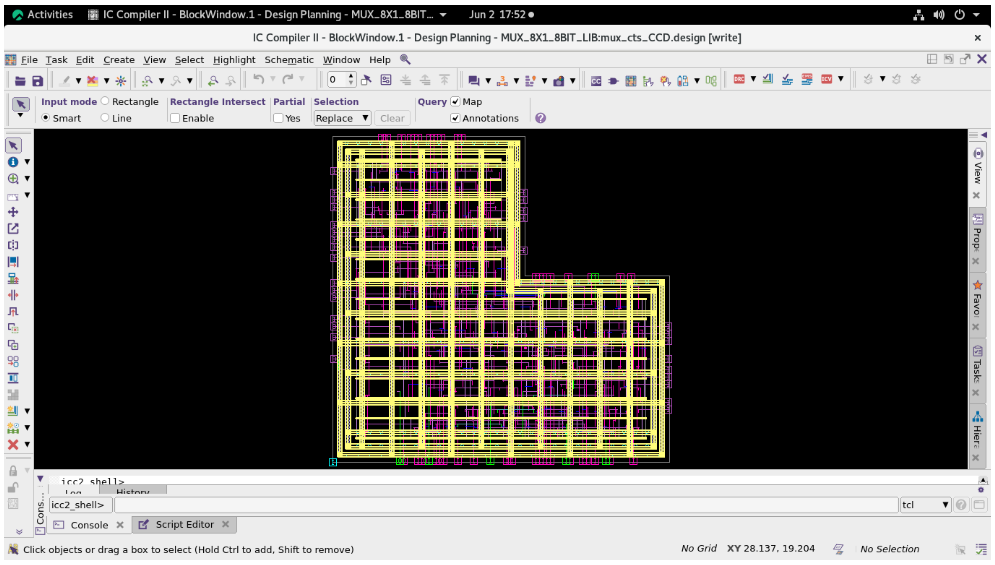
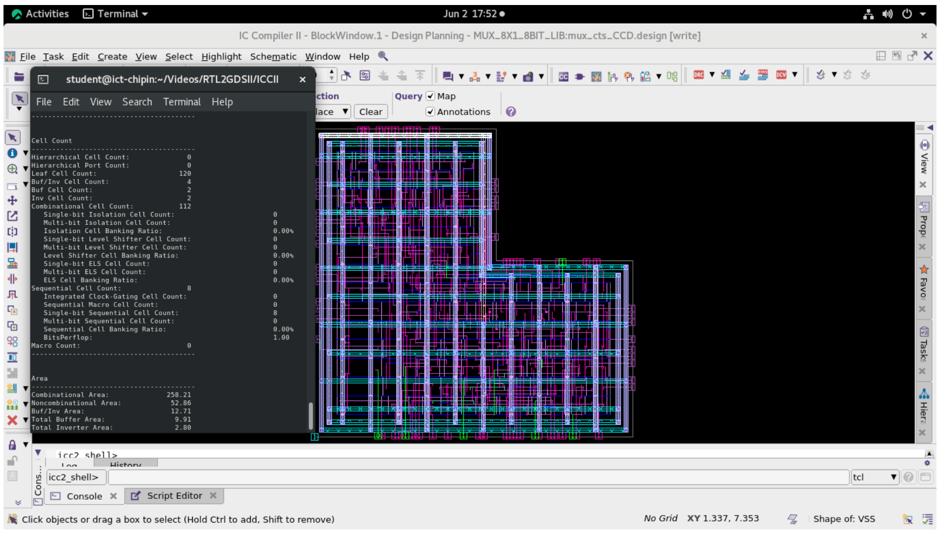


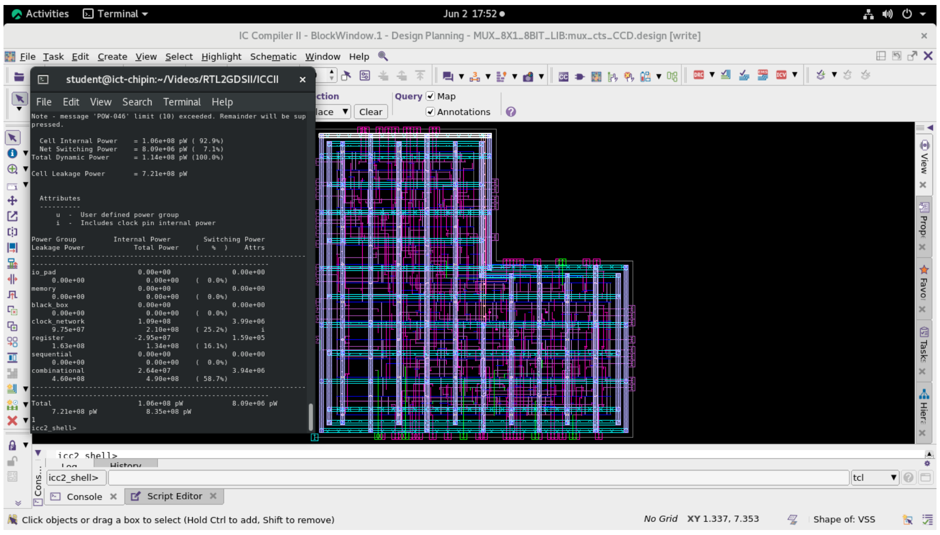
Figure 27: Routing Highlighted View

Reports:



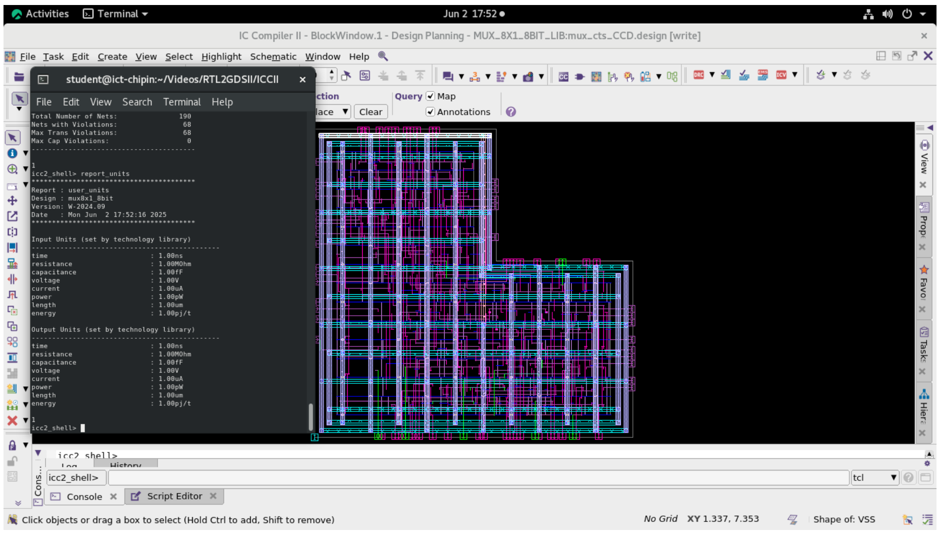
```
----------------------------------------


Cell Count
----------------------------------------
Hierarchical Cell Count:               0
Hierarchical Port Count:               0
Leaf Cell Count:                     120
Buf/Inv Cell Count:                    4
Buf Cell Count:                        2
Inv Cell Count:                        2
Combinational Cell Count:            112
   Single-bit Isolation Cell Count:                    0
   Multi-bit Isolation Cell Count:                     0
   Isolation Cell Banking Ratio:                       0.00%
   Single-bit Level Shifter Cell Count:                0
   Multi-bit Level Shifter Cell Count:                 0
   Level Shifter Cell Banking Ratio:                   0.00%
   Single-bit ELS Cell Count:                          0
   Multi-bit ELS Cell Count:                           0
   ELS Cell Banking Ratio:                             0.00%
Sequential Cell Count:                 8
   Integrated Clock-Gating Cell Count:                 0
   Sequential Macro Cell Count:                        0
   Single-bit Sequential Cell Count:                   8
   Multi-bit Sequential Cell Count:                    0
   Sequential Cell Banking Ratio:                      0.00%
   BitsPerflop:                                        1.00
Macro Count:                           0
----------------------------------------


Area
----------------------------------------
Combinational Area:               258.21
Noncombinational Area:             52.86
Buf/Inv Area:                      12.71
Total Buffer Area:                  9.91
Total Inverter Area:                2.80
```

Figure 28: Routing - QoR Report



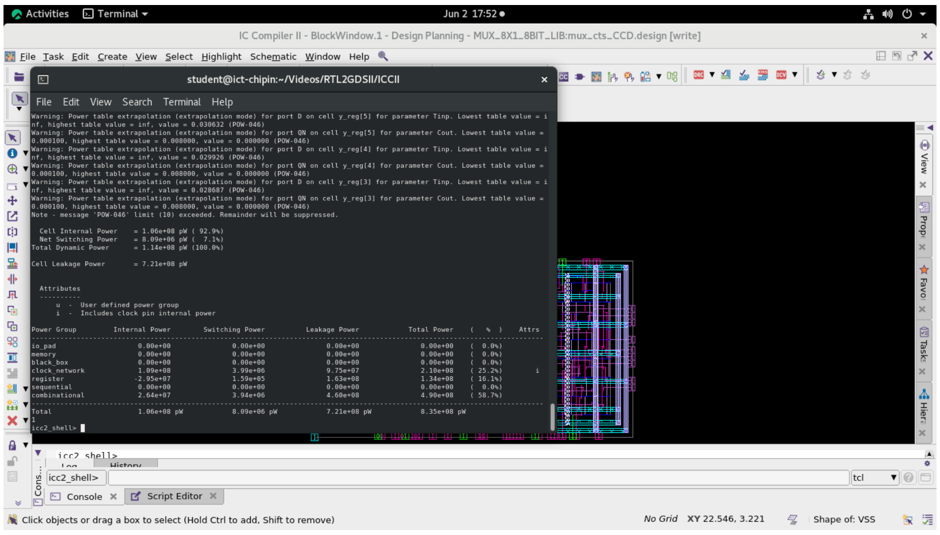
```
Note - message 'POW-046' limit (10) exceeded. Remainder will be sup
pressed.

  Cell Internal Power    = 1.06e+08 pW ( 92.9%)
  Net Switching Power    = 8.09e+06 pW (  7.1%)
Total Dynamic Power      = 1.14e+08 pW (100.0%)

Cell Leakage Power       = 7.21e+08 pW


  Attributes
  ----------
      u  -  User defined power group
      i  -  Includes clock pin internal power

Power Group          Internal Power        Switching Power
Leakage Power             Total Power    (   %  )    Attrs
--------------------------------------------------------------------
----------------------------------------------------------
io_pad                    0.00e+00              0.00e+00
     0.00e+00               0.00e+00    (  0.0%)
memory                    0.00e+00              0.00e+00
     0.00e+00               0.00e+00    (  0.0%)
black_box                 0.00e+00              0.00e+00
     0.00e+00               0.00e+00    (  0.0%)
clock_network             1.09e+08              3.99e+06
     9.75e+07               2.10e+08    ( 25.2%)         i
register                 -2.95e+07              1.59e+05
     1.63e+08               1.34e+08    ( 16.1%)
sequential                0.00e+00              0.00e+00
     0.00e+00               0.00e+00    (  0.0%)
combinational             2.64e+07              3.94e+06
     4.60e+08               4.90e+08    ( 58.7%)
--------------------------------------------------------------------
----------------------------------------------------------
Total                     1.06e+08 pW           8.09e+06 pW
     7.21e+08 pW            8.35e+08 pW
1
icc2_shell>
```

Figure 29: Routing - Timing Report



```
Total Number of Nets:                190
Nets with Violations:                 68
Max Trans Violations:                 68
Max Cap Violations:                    0
---------------------------------------


1
icc2_shell> report_units
****************************************
Report : user_units
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:52:16 2025
****************************************

Input Units (set by technology library)
---------------------------------------------
time                          : 1.00ns
resistance                    : 1.00MOhm
capacitance                   : 1.00fF
voltage                       : 1.00V
current                       : 1.00uA
power                         : 1.00pW
length                        : 1.00um
energy                        : 1.00pj/t

Output Units (set by technology library)
---------------------------------------------
time                          : 1.00ns
resistance                    : 1.00MOhm
capacitance                   : 1.00fF
voltage                       : 1.00V
current                       : 1.00uA
power                         : 1.00pW
length                        : 1.00um
energy                        : 1.00pj/t

1
icc2_shell>
```

Figure 30: Routing - Units Report



```
Warning: Power table extrapolation (extrapolation mode) for port D on cell y_reg[5] for parameter Tinp. Lowest table value = i
nf, highest table value = inf, value = 0.030632 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port QN on cell y_reg[5] for parameter Cout. Lowest table value =
0.000100, highest table value = 0.008000, value = 0.000000 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port D on cell y_reg[4] for parameter Tinp. Lowest table value = i
nf, highest table value = inf, value = 0.029926 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port QN on cell y_reg[4] for parameter Cout. Lowest table value =
0.000100, highest table value = 0.008000, value = 0.000000 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port D on cell y_reg[3] for parameter Tinp. Lowest table value = i
nf, highest table value = inf, value = 0.028687 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port QN on cell y_reg[3] for parameter Cout. Lowest table value =
0.000100, highest table value = 0.008000, value = 0.000000 (POW-046)
Note - message 'POW-046' limit (10) exceeded. Remainder will be suppressed.

  Cell Internal Power    = 1.06e+08 pW ( 92.9%)
  Net Switching Power    = 8.09e+06 pW (  7.1%)
Total Dynamic Power      = 1.14e+08 pW (100.0%)

Cell Leakage Power       = 7.21e+08 pW


  Attributes
  ----------
      u  -  User defined power group
      i  -  Includes clock pin internal power

Power Group          Internal Power        Switching Power          Leakage Power            Total Power    (   %  )    Attrs
--------------------------------------------------------------------------------------------------------------------------------
io_pad                    0.00e+00              0.00e+00              0.00e+00              0.00e+00    (  0.0%)
memory                    0.00e+00              0.00e+00              0.00e+00              0.00e+00    (  0.0%)
black_box                 0.00e+00              0.00e+00              0.00e+00              0.00e+00    (  0.0%)
clock_network             1.09e+08              3.99e+06              9.75e+07              2.10e+08    ( 25.2%)         i
register                 -2.95e+07              1.59e+05              1.63e+08              1.34e+08    ( 16.1%)
sequential                0.00e+00              0.00e+00              0.00e+00              0.00e+00    (  0.0%)
combinational             2.64e+07              3.94e+06              4.60e+08              4.90e+08    ( 58.7%)
--------------------------------------------------------------------------------------------------------------------------------
Total                     1.06e+08 pW           8.09e+06 pW           7.21e+08 pW           8.35e+08 pW
1
icc2_shell>
```

Figure 31: Routing - Power Report

6 Static Timing Analysis using PrimeTime

After synthesis, the design was analyzed using Synopsys PrimeTime (PT) to verify timing closure and check if the design meets the required constraints.

6.1 Final Slack

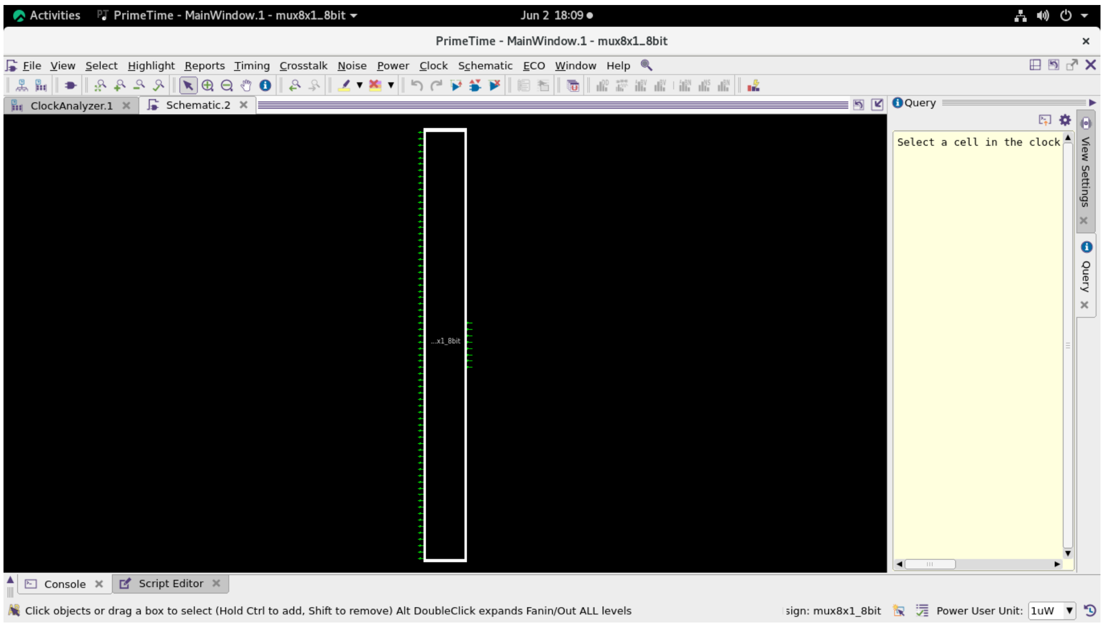
The final slack obtained from PrimeTime is shown below:

```
Final Slack = +0.800148 ns
```

Importance of Slack:
Slack is a critical timing metric that indicates the difference between the required arrival time and the actual arrival time of signals at timing endpoints (like registers or output pins).

- **Positive Slack:** Indicates that the design meets timing requirements. The larger the positive slack, the more timing margin the design has.
- **Slack between 0 and 1 ns:** While still positive, slack values closer to zero indicate tighter timing margins. Slack in this range means the design is just meeting the timing requirements but has limited tolerance for variations (process, voltage, temperature).
- **Negative Slack:** Indicates a timing violation where the signal arrives later than required, causing potential functional errors at the system level.

Synthesized Schematic Views:

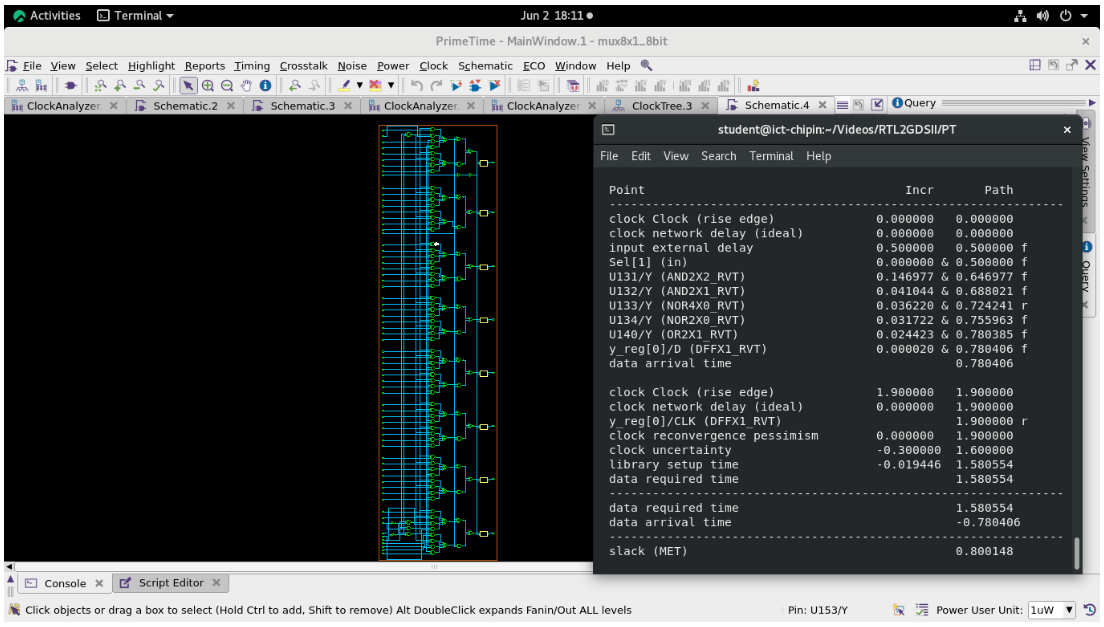

Activities
PrimeTime - MainWindow.1 - mux8x1_8bit
Jun 2 18:09
PrimeTime - MainWindow.1 - mux8x1_8bit
File View Select Highlight Reports Timing Crosstalk Noise Power Clock Schematic ECO Window Help
ClockAnalyzer.1
Schematic.2
Query
View Settings
Query
...x1_8bit
Console
Script Editor
sign: mux8x1_8bit
Power User Unit: 1uW

Select a cell in the clock

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels

Figure 32: PrimeTime Schematic View 1

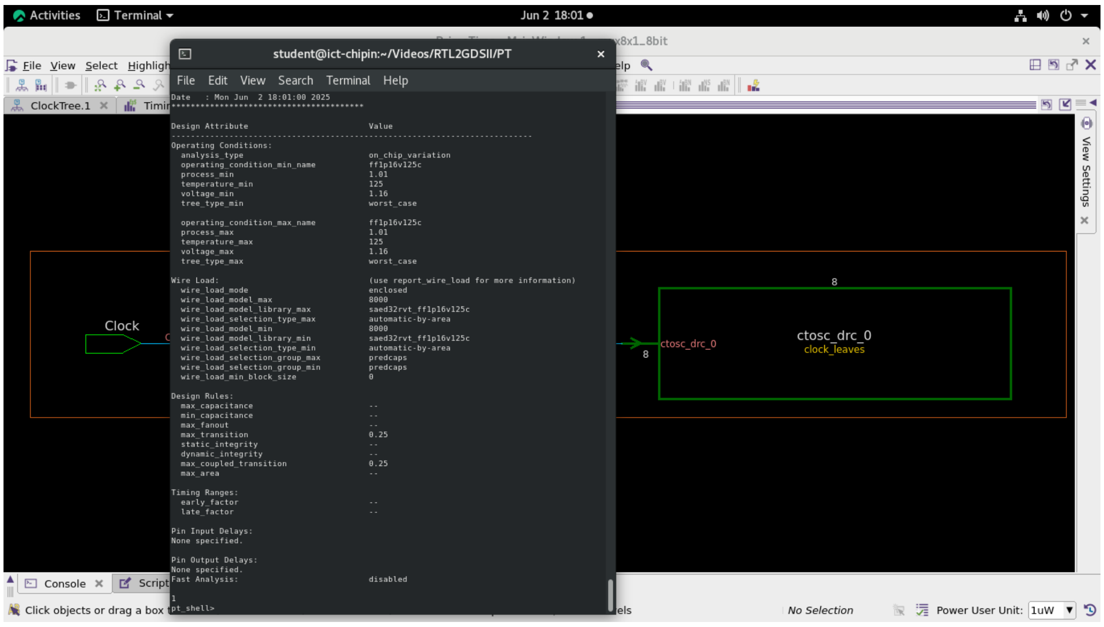
PrimeTime Reports:



```
Point                                          Incr       Path
------------------------------------------------------------------
clock Clock (rise edge)                      0.000000   0.000000
clock network delay (ideal)                  0.000000   0.000000
input external delay                         0.500000   0.500000 f
Sel[1] (in)                                  0.000000 & 0.500000 f
U131/Y (AND2X2_RVT)                          0.146977 & 0.646977 f
U132/Y (AND2X1_RVT)                          0.041044 & 0.688021 f
U133/Y (NOR4X0_RVT)                          0.036220 & 0.724241 r
U134/Y (NOR2X0_RVT)                          0.031722 & 0.755963 f
U140/Y (OR2X1_RVT)                           0.024423 & 0.780385 f
y_reg[0]/D (DFFX1_RVT)                       0.000020 & 0.780406 f
data arrival time                                       0.780406

clock Clock (rise edge)                      1.900000   1.900000
clock network delay (ideal)                  0.000000   1.900000
y_reg[0]/CLK (DFFX1_RVT)                                1.900000 r
clock reconvergence pessimism                0.000000   1.900000
clock uncertainty                           -0.300000   1.600000
library setup time                          -0.019446   1.580554
data required time                                      1.580554
------------------------------------------------------------------
data required time                                      1.580554
data arrival time                                      -0.780406
------------------------------------------------------------------
slack (MET)                                             0.800148
```

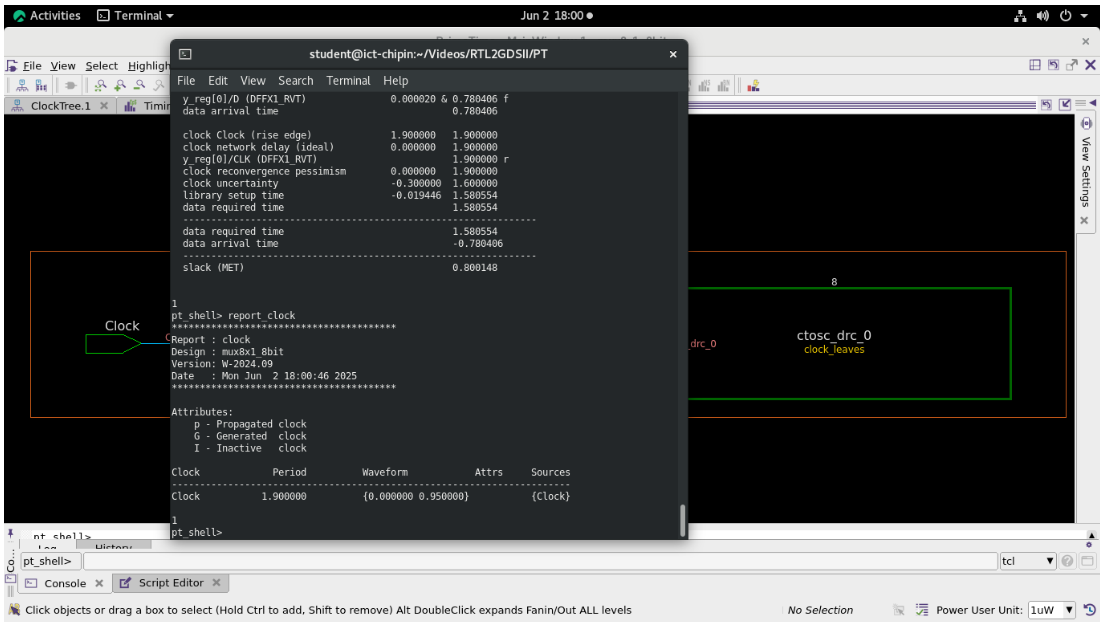
Activities
Terminal
Jun 2 18:11
PrimeTime - MainWindow.1 - mux8x1_8bit
File View Select Highlight Reports Timing Crosstalk Noise Power Clock Schematic ECO Window Help
ClockAnalyzer
Schematic.2
Schematic.3
ClockTree.3
Schematic.4
Query
student@ict-chipin:~/Videos/RTL2GDSII/PT
File Edit View Search Terminal Help
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels
Pin: U153/Y
Power User Unit: 1uW

Figure 33: PrimeTime Schematic View 2



```
Date   : Mon Jun  2 18:01:00 2025
****************************************

Design Attribute                         Value
---------------------------------------------------------------------------
Operating Conditions:
  analysis_type                          on_chip_variation
  operating_condition_min_name           ff1p16v125c
  process_min                            1.01
  temperature_min                        125
  voltage_min                            1.16
  tree_type_min                          worst_case

  operating_condition_max_name           ff1p16v125c
  process_max                            1.01
  temperature_max                        125
  voltage_max                            1.16
  tree_type_max                          worst_case

Wire Load:                               (use report_wire_load for more information)
  wire_load_mode                         enclosed
  wire_load_model_max                    8000
  wire_load_model_library_max            saed32rvt_ff1p16v125c
  wire_load_selection_type_max           automatic-by-area
  wire_load_model_min                    8000
  wire_load_model_library_min            saed32rvt_ff1p16v125c
  wire_load_selection_type_min           automatic-by-area
  wire_load_selection_group_max          predcaps
  wire_load_selection_group_min          predcaps
  wire_load_min_block_size               0

Design Rules:
  max_capacitance                        --
  min_capacitance                        --
  max_fanout                             --
  max_transition                         0.25
  static_integrity                       --
  dynamic_integrity                      --
  max_coupled_transition                 0.25
  max_area                               --

Timing Ranges:
  early_factor                           --
  late_factor                            --

Pin Input Delays:
None specified.

Pin Output Delays:
None specified.
Fast Analysis:                           disabled

1
pt_shell>
```

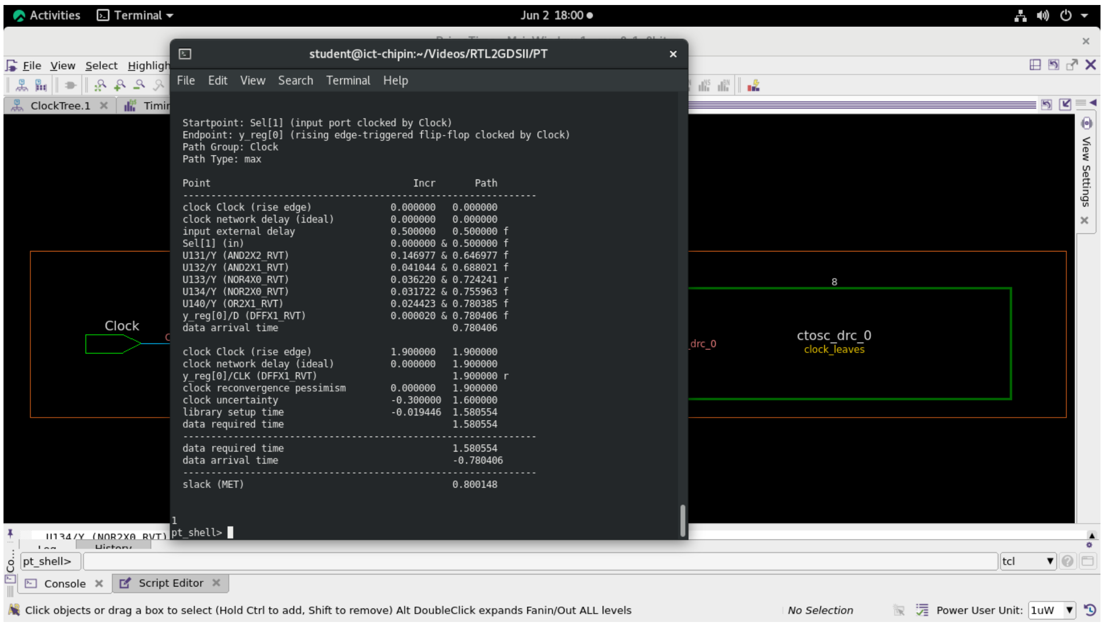
Figure 34: PrimeTime Design Report



```
  y_reg[0]/D (DFFX1_RVT)              0.000020 & 0.780406 f
  data arrival time                              0.780406

  clock Clock (rise edge)             1.900000   1.900000
  clock network delay (ideal)         0.000000   1.900000
  y_reg[0]/CLK (DFFX1_RVT)                       1.900000 r
  clock reconvergence pessimism       0.000000   1.900000
  clock uncertainty                  -0.300000   1.600000
  library setup time                 -0.019446   1.580554
  data required time                             1.580554
  ---------------------------------------------------------------
  data required time                             1.580554
  data arrival time                             -0.780406
  ---------------------------------------------------------------
  slack (MET)                                    0.800148


1
pt_shell> report_clock
****************************************
Report : clock
Design : mux8x1_8bit
Version: W-2024.09
Date   : Mon Jun  2 18:00:46 2025
****************************************

Attributes:
    p - Propagated clock
    G - Generated  clock
    I - Inactive   clock

Clock             Period          Waveform            Attrs     Sources
--------------------------------------------------------------------------
Clock           1.900000          {0.000000 0.950000}           {Clock}

1
pt_shell>
```

```
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels
```

Figure 35: PrimeTime Clock Report



```
  Startpoint: Sel[1] (input port clocked by Clock)
  Endpoint: y_reg[0] (rising edge-triggered flip-flop clocked by Clock)
  Path Group: Clock
  Path Type: max

  Point                                   Incr       Path
  ---------------------------------------------------------------
  clock Clock (rise edge)             0.000000   0.000000
  clock network delay (ideal)         0.000000   0.000000
  input external delay                0.500000   0.500000 f
  Sel[1] (in)                         0.000000 & 0.500000 f
  U131/Y (AND2X2_RVT)                 0.146977 & 0.646977 f
  U132/Y (AND2X1_RVT)                 0.041044 & 0.688021 f
  U133/Y (NOR4X0_RVT)                 0.036220 & 0.724241 r
  U134/Y (NOR2X0_RVT)                 0.031722 & 0.755963 f
  U140/Y (OR2X1_RVT)                  0.024423 & 0.780385 f
  y_reg[0]/D (DFFX1_RVT)              0.000020 & 0.780406 f
  data arrival time                              0.780406

  clock Clock (rise edge)             1.900000   1.900000
  clock network delay (ideal)         0.000000   1.900000
  y_reg[0]/CLK (DFFX1_RVT)                       1.900000 r
  clock reconvergence pessimism       0.000000   1.900000
  clock uncertainty                  -0.300000   1.600000
  library setup time                 -0.019446   1.580554
  data required time                             1.580554
  ---------------------------------------------------------------
  data required time                             1.580554
  data arrival time                             -0.780406
  ---------------------------------------------------------------
  slack (MET)                                    0.800148


1
pt_shell>
```

```
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels
```

Figure 36: PrimeTime Timing Report and Slack

7 Results

Synthesis Results

Table 1: Synthesis Results

Area	**Power**	**Timing**	**Slack**
1900000	0.780406 mW	1.900000 ns	0.800148 ns

Physical Design Results

Table 2: Physical Design Results

Stage	**Area**	**Power**
Floor Planning	1900000	0.780406 mW
Placement	1900000	0.780406 mW
CTS	1900000	0.780406 mW
Routing	1900000	0.780406 mW

Table 3: Power Distribution

Power Group	**Internal Power**	**Switching Power**	**Leakage Power**	
io_pad	0.00e+00	0.00e+00	0.00e+00	
memory	0.00e+00	0.00e+00	0.00e+00	
black-box	0.00e+00	0.00e+00	0.00e+00	
clock-network	1.95e+07	1.50e+07	1.34e+08	
sequential	2.04e+08	3.04e+08	4.60e+08	
combinational	2.04e+07	8.09e+06	7.21e+08	
Total	1.06e+08 pW	8.09e+06 pW	7.21e+08 pW	

Table 4: Total Power Distribution

Power Group	**Total Power (pW)**
io_pad	0.00e+00
memory	0.00e+00
black-box	0.00e+00
clock-network	1.68e+08
sequential	9.68e+08
combinational	7.42e+08
Total	8.35e+08

Total Power: 8.35e+08 pW

8 Discussion

The RTL to GDSII flow is a comprehensive process that involves multiple stages of design and verification. Each stage, from RTL design to final layout generation, plays a crucial role in ensuring the functionality and performance of the integrated circuit. The use of industry-standard tools like Synopsys Design Compiler and IC Compiler II provides valuable insights into the practical aspects of digital design.

8.1 RTL Design and Verification

The RTL design of the 8x1 multiplexer was successfully implemented and verified using Verilog HDL and Synopsys Verdi. The verification process ensured that the design met the specified functional requirements.

8.2 Synthesis and Physical Design

The synthesis process optimized the design for area, power, and timing, resulting in a highly efficient implementation. The physical design stages, including floor planning, placement, CTS, and routing, were carefully executed to achieve optimal performance and minimal area usage.

9 Conclusion

This project provided a comprehensive understanding of the RTL to GDSII flow for digital circuit design. The hands-on experience with industry-standard EDA tools and methodologies was invaluable in gaining practical insights into the design and implementation of integrated circuits. The successful completion of the project demonstrates the ability to design, verify, and implement complex digital circuits using advanced EDA tools.

References

[1] Synopsys Design Compiler User Guide, https://www.synopsys.com/.

[2] Synopsys IC Compiler II User Guide, https://www.synopsys.com/.

[3] Verilog HDL Reference, https://www.verilog.com/.

For the complete project files, including additional code and documentation, please visit the GitHub repository:
https://github.com/iamnrp7/8x1MUX_8BIT/
Note: This repository contains all source files, constraints, synthesis reports, and physical design stages for the 8x1 multiplexer with 8-bit inputs.

A Scripts and Files Used in the Project

A.1 Common Setup TCL Script

Common Setup TCL Script

```
puts "RM-Info: Running script [info script]\n"

set DESIGN_NAME "mux8x1_8bit"
set PDK_PATH "./../ref/"
set DESIGN_REF_DATA_PATH ""

set HIERARCHICAL_DESIGNS ""
set HIERARCHICAL_CELLS ""

set ADDITIONAL_SEARCH_PATH
"$PDK_PATH $PDK_PATH/tech/milkyway $PDK_PATH/tech/star_rcxt"

set TARGET_LIBRARY_FILES
"$PDK_PATH/lib/stdcell_rvt/saed32rvt_tt0p78vn40c.db"
set ADDITIONAL_LINK_LIB_FILES ""

set MIN_LIBRARY_FILES ""

set MW_REFERENCE_LIB_DIRS ""
set MW_REFERENCE_CONTROL_FILE ""

set TECH_FILE "$PDK_PATH/tech/milkyway/saed32nm_1p9m_mw.tf"
set MAP_FILE "saed32nm_tf_itf_tluplus.map"
set TLUPLUS_MAX_FILE "saed32nm_1p9m_Cmax.tluplus"
set TLUPLUS_MIN_FILE "saed32nm_1p9m_Cmin.tluplus"

set MIN_ROUTING_LAYER "M1"
set MAX_ROUTING_LAYER "M5"

set LIBRARY_DONT_USE_FILE ""
set LIBRARY_DONT_USE_PRE_COMPILE_LIST ""
set LIBRARY_DONT_USE_PRE_INCR_COMPILE_LIST ""

set PD1 ""
set VA1_COORDINATES {}
set MW_POWER_NET1 "VDD1"

set PD2 ""
set VA2_COORDINATES {}
set MW_POWER_NET2 "VDD2"

set PD3 ""
set VA3_COORDINATES {}
set MW_POWER_NET3 "VDD3"

set PD4 ""
set VA4_COORDINATES {}
set MW_POWER_NET4 "VDD4"
```

A.2 Floor Plan File

Here is the content of the floor plan file:

Floor Plan File

```
set PDK_PATH ./../ref

create_lib -ref_lib
$PDK_PATH/lib/ndm/saed32rvt_c.ndm MUX_8X1_8BIT_LIB

read_verilog {./../DC/results/full_adder.mapped.v}
-library MUX_8X1_8BIT_LIB -design mux8x1_8bit -top mux8x1_8bit

initialize_floorplan -shape L -core_offset 2
-coincident_boundary true
set_individual_pin_constraints -ports [get_ports {A B}] -sides 6
place_pins -self
create_placement -floorplan -effort medium

save_block
save_lib
```

A.3 Power Planning Script

Here is the TCL script used for power planning:

Power Planning Script

```
create_net -power {VDD}
create_net -ground {VSS}

connect_pg_net -all_blocks -automatic

create_pg_ring_pattern core_ring_pattern -horizontal_layer M7
-horizontal_width .4 -horizontal_spacing .3 -vertical_layer M8
-vertical_width .4 -vertical_spacing .3

set_pg_strategy core_power_ring -core -pattern
{{name : core_ring_pattern}{nets : {VDD VSS}}{offset : {.5 .5}}}

compile_pg -strategies core_power_ring

create_pg_mesh_pattern mesh
-layers { {{vertical_layer: M6}{width: .34} {spacing: interleaving}{pitch: 5} 

set_pg_strategy core_mesh -pattern { {pattern:mesh} {nets: VDD VSS}} -core -ex

compile_pg -strategies core_mesh

create_pg_std_cell_conn_pattern std_cell_rail
-layers {M1} -rail_width 0.06

set_pg_strategy rail_strat -core -pattern {{name: std_cell_rail} {nets: VDD VS

compile_pg -strategies rail_strat

save_block
save_lib
```

A.4 Placement Script

Here is the TCL script used for placement:

Placement Script

```
set mode1 "func"
set corner1 "nom"
set scenario1 "${mode1}::${corner1}"
remove_modes -all
remove_corners -all
remove_scenarios -all

create_mode $mode1
create_corner $corner1
create_scenario -name func::nom -mode func -corner nom
current_mode func
current_scenario func::nom

source ./../CONSTRAINTS/mux.sdc

set_dont_use [get_lib_cells */FADD*]
set_dont_use [get_lib_cells */HADD*]
set_dont_use [get_lib_cells */AO*]
set_dont_use [get_lib_cells */OA*]
set_dont_use [get_lib_cells */NAND*]
set_dont_use [get_lib_cells */XOR*]
set_dont_use [get_lib_cells */NOR*]
set_dont_use [get_lib_cells */XNOR*]
set_dont_use [get_lib_cells */MUX*]

current_corner nom
current_scenario func::nom

set parasitic1 "p1"
set tluplus_file$parasitic1
"$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus"
set layer_map_file$parasitic1
"$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
set parasitic2 "p2"
set tluplus_file$parasitic2
"$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmin.tluplus"
set layer_map_file$parasitic2
"$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
read_parasitic_tech -tlup $tluplus_filep1
-layermap $layer_map_filep1 -name p1
read_parasitic_tech -tlup $tluplus_filep2
-layermap $layer_map_filep2 -name p2
set_parasitic_parameters -late_spec
$parasitic1 -early_spec $parasitic2
set_app_options -name place.coarse.continue_on_missing_scandef
-value true
place_pins -self
place_opt
legalize_placement
save_block -as mux_placement
save_lib
```

A.5 Routing Script

Here is the TCL script used for routing:

Routing Script

```
set_app_options -name route.global.timing_driven -value true
set_app_options -name route.global.crosstalk_driven -value false

set_app_options -name route.track.timing_driven -value true
set_app_options -name route.track.crosstalk_driven -value true

set_app_options -name route.detail.timing_driven -value true
set_app_options -name route.detail.save_after_iterations -value false
set_app_options -name route.detail.force_max_number_iterations -value false
set_app_options -name route.detail.antenna -value true
set_app_options -name route.detail.antenna_fixing_preference -value use_diodes
set_app_options -name route.detail.diode_libcell_names -value */ANTENNA_RVT

route_global
route_track
route_detail
route_opt

write_verilog ./results/mux.routed.v
write_sdc -output ./results/mux.routed.sdc
write_parasitics -format spef -output ./results/mux${scenario1}.spef
```