Experiment 1: Part 1

Prasann Viswanathan Roll Number **190070047**
EE-214, WEL, IIT Bombay
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Overview of the experiment:

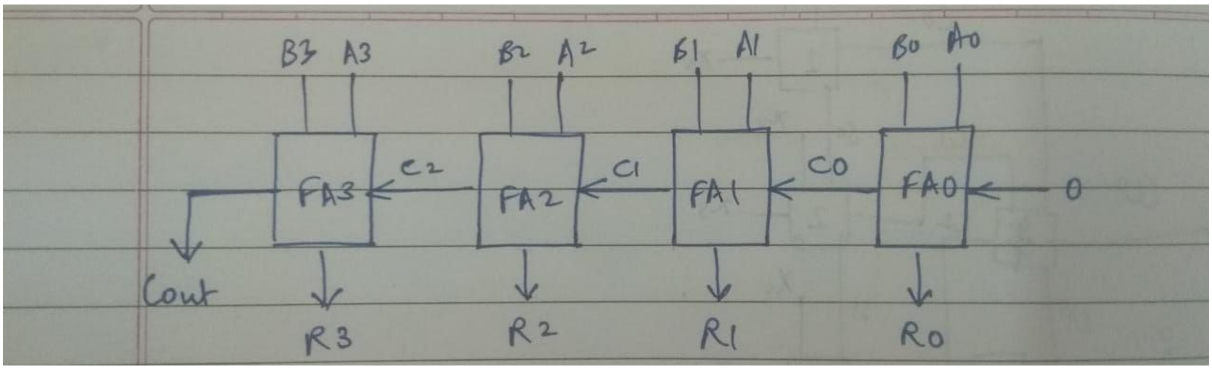
The purpose of the experiment was to design a four-bit adder to add two four bit binary numbers and display the output.

To perform the experiment I used a predefined Full Adder gate as a component to implement a four bit adder.

The following is the data I used.

Approach to the experiment:

To perform this experiment, I used four full adders, FA0, …, FA3 each to add bits Ai, Bi and the Carry generated by the previous Full Adder. This is known as a Ripple Carry Adder architecture. Note that carry for FA0 was given to be ‘0’, effectively rendering it a Half Adder.



Design document and VHDL code if relevant:

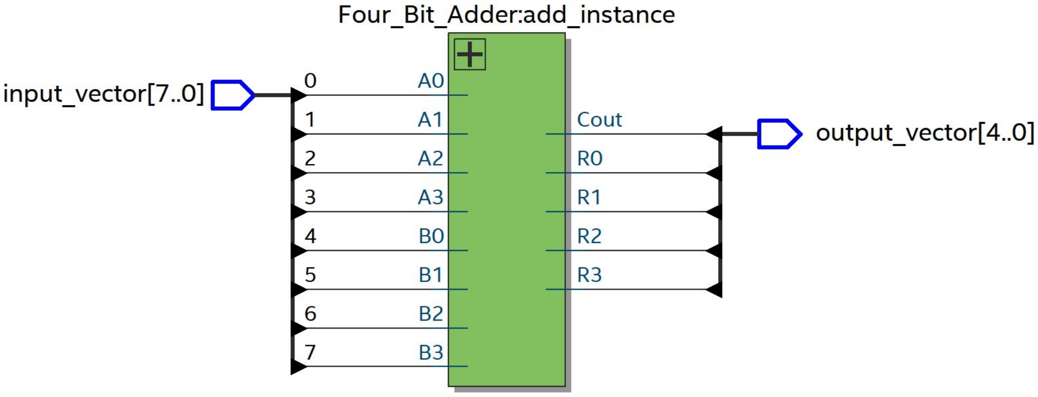
The only relevant code was the Four Bit Adder implementation:

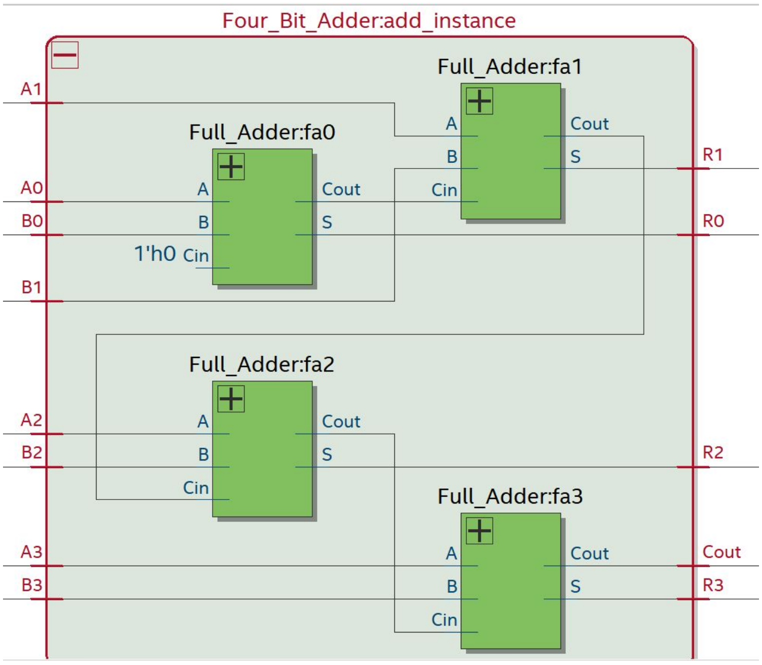
```
architecture Struct of Four_Bit_Adder is

        -- Only full adder components are used
        component Full_Adder is
                port (A, B, Cin: in std_logic; S, Cout: out std_logic);
        end component Full_Adder;

        -- Carry signals are intermediate
        signal C1, C2, C3: std_logic;

-- Port maps explicitly depict the connections and logic of the circuit

begin
        -- component instances
        fa0: Full_Adder
                port map (A => A0, B => B0, Cin => '0', S => R0, Cout => C1);
```

```
	fa1: Full_Adder
		port map (A => A1, B => B1, Cin => C1, S => R1, Cout => C2);

	fa2: Full_Adder
		port map (A => A2, B => B2, Cin => C2, S => R2, Cout => C3);

	fa3: Full_Adder
		port map (A => A3, B => B3, Cin => C3, S => R3, Cout => Cout);

end Struct;
```

Here the main logic, via port maps has been documented.

RTL View:





DUT Input/Output Format:

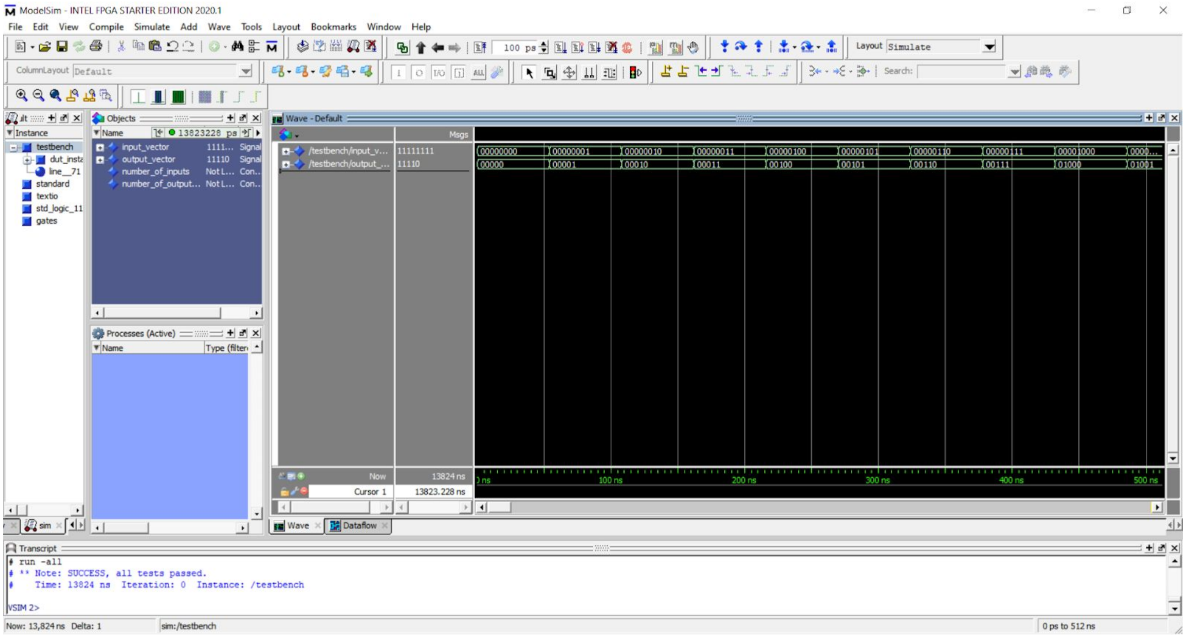
Input - 8 bit vector, Output - 5 bit vector, resulted from addition of least significant and most significant nibbles of input.

TRACEFILE example cases:

00001111 01111 11111

00010000 00001 11111
00010001 00010 11111
00010010 00011 11111
00010011 00100 11111

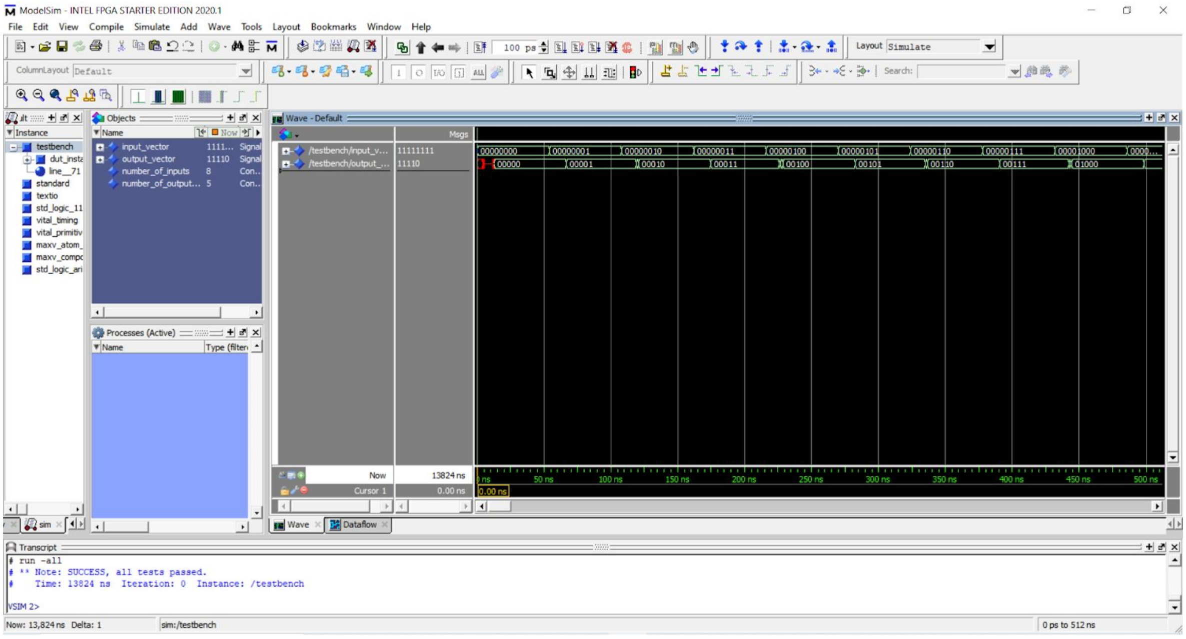
RTL Simulation:



```
# run -all
# ** Note: SUCCESS, all tests passed.
#    Time: 13824 ns  Iteration: 0  Instance: /testbench
VSIM 2>
```

Note ‘All test cases passed’ in bottom left

Gate-level Simulation:



```
# run -all
# ** Note: SUCCESS, all tests passed.
#    Time: 13824 ns  Iteration: 0  Instance: /testbench
VSIM 2>
```

References:

NA