# Stacked Pentacene Layer Organic Thin-Film Transistors with Improved Characteristics

Y.-Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson

***Abstract*—Using two layers of pentacene deposited at different substrate temperatures as the active material, we have fabricated photolithographically defined organic thin-film transistors (OTFT's) with improved field-effect mobility and subthreshold slope. These devices use photolithographically defined gold source and drain electrodes and octadecyltrichlorosilane-treated silicon dioxide gate dielectric. The devices have field-effect mobility as large as 1.5 cm$^2$/V-s, on/off current ratio larger than $10^8$, near zero threshold voltage, and subthreshold slope less than 1.6 V per decade. To our knowledge, this is the largest field-effect mobility and smallest subthreshold slope yet reported for any organic transistor, and the first time both of these important characteristics have been obtained for a single device.**

## I. Introduction

RECENTLY, organic thin-film transistors (OTFT's) with field-effect mobility and on/off current ratio comparable to hydrogenated amorphous silicon thin-film transistors (a-Si : H TFT's) have been fabricated using pentacene as the active material [1]. However, compared to a-Si : H TFT's, these devices had large threshold voltage and large subthreshold slope.

Since a-Si : H is the most widely used material for thin-film transistors (TFT's) it provides a useful basis for comparison. Typically, a-Si : H TFT's have field-effect mobility larger than 0.5 cm$^2$/V-s, on/off current ratio greater than $10^8$, near zero threshold voltage, and subthreshold slope less than about 1.0 V/decade. Until recently, OTFT's were not able to equal any of these characteristics. For example, OTFT's using $\alpha$-sexithienyl as the active material typically have field-effect mobility less than 0.1 cm$^2$/V-s, current on/off ratio near or less than $10^6$, and subthreshold slope greater than 5 V/decade [2], [3]. We recently fabricated OTFT's using pentacene as the active material with field-effect mobility near 0.7 cm$^2$/V-s, and current on/off ratio greater than $10^8$ [1]. However, these early devices had subthreshold slope near 5 V/decade and were on for zero applied gate voltage, requiring a significant gate voltage to turn the devices fully off. Both of these characteristics are problematic for device applications in low-voltage circuits that require large on/off current ratio.

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Subthreshold slope in particular is a concern since to our knowledge *no* OTFT's with low subthreshold slope have yet been demonstrated. The carrier transport in organic semiconductors is not well understood, but it is possible that hopping-dominated transport, trap-limited transport, or narrow-band transport in organic materials might limit subthreshold slope to an unacceptably large value. Pentacene is a strong molecular-crystal former and this characteristic, common to many small-molecule organic semiconductors [4], [5], is believed to be an important factor in obtaining large field-effect mobility. When deposited onto amorphous substrates at temperatures in the 60–100 °C range pentacene films are typically dendritic with grain size in the micron or several microns range. The large grain size requires substantial surface mobility for the depositing pentacene molecules and a not unexpected related result is that interaction with many substrates, including silicon dioxide ($SiO_2$), is minimal. Since the interface between the organic active material and the gate dielectric material is a critical part of the field-effect device, control of this interface is important. We have found that the characteristics of pentacene TFT's can be improved by using a self-organizing material like octadecyltrichlorosilane (OTS) between the $SiO_2$ gate dielectric and the pentacene active layer [6]. Fig. 1 shows an atomic force microscopy image of a pentacene film with an average thickness of 50 nm deposited onto an OTS-treated $SiO_2$ substrate at 90 °C; dendritic grains with single molecular step terraces are easily seen. X-ray diffraction data also indicates that this film is well-ordered, and that pentacene films deposited at high temperature typically have more pronounced diffraction peaks [7] at the lattice spacing expected for single-crystal triclinic pentacene. However, as shown in Fig. 1, high temperature deposited pentacene films also tend to have voids, possibly due to the high surface mobility of the deposited pentacene molecules, and we expect the carrier transport through this material will be degraded significantly by the voids. To address this problem, we use a stacked structure with a first layer of pentacene deposited at high temperature to obtain improved film ordering, and a second pentacene layer deposited at lower temperature to help fill-in voids and improve film continuity.

## II. Device Fabrication and Characteristics

The stacked pentacene layer TFT device structure used in this study is shown in Fig. 2. For simplicity, our devices were fabricated using heavily doped silicon as the substrate and gate electrode, with thermally grown silicon dioxide as the TFT gate dielectric. Gold source and drain contacts were deposited

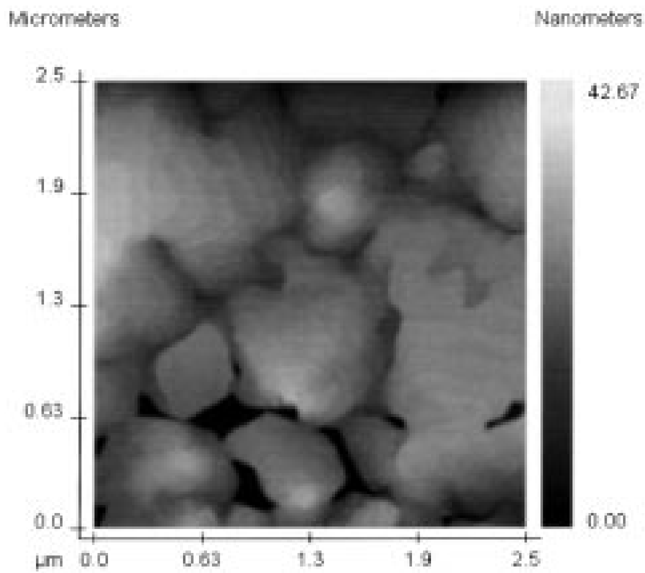


Fig. 1. Atomic force microscopy image of 50 nm thick pentacene deposited onto OTS treated $SiO_2$ substrate at 90 °C.

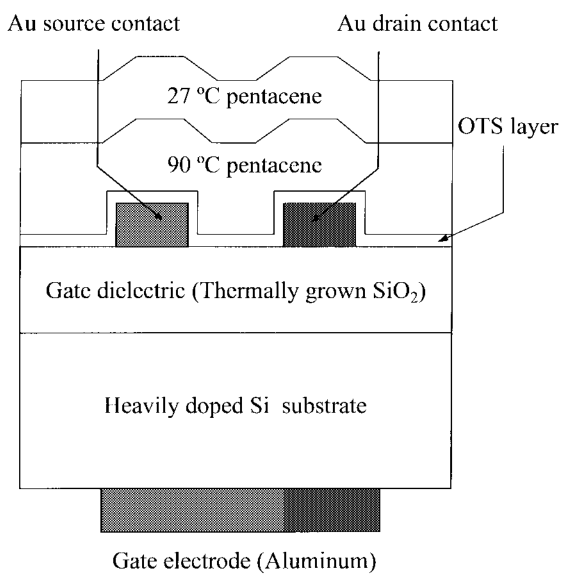


Fig. 2. The schematic of stacked pentacene layer TFT.

and patterned by photolithography. Octadecyltrichlorosilane (OTS), a self-organizing material, was then deposited from a 2% solution in ethanol. Although OTS ideally forms an organized single monolayer on $SiO_2$, no characterization was done to confirm this result. After OTS treatment, 30 nm of pentacene purified by vacuum gradient sublimation [7] was deposited by thermal evaporation at a pressure of $5 \times 10^{-7}$ Torr onto substrates held at 90 °C. After the substrate was cooled to room temperature, 20 nm of pentacene was deposited on top of the previous 30-nm pentacene layer.

Fig. 3 shows the linear $I_D$–$V_{DS}$ characteristics for a pentacene TFT fabricated as described above with channel length and width of 20 $\mu$m and 50 $\mu$m, respectively, and a gate dielectric thickness of 350 nm. Fig. 4 shows the $\sqrt{(I_D)}$–$V_{GS}$ characteristics and the $\log(I_D)$–$V_{GS}$ characteristics for the same device. From the $\sqrt{(I_D)}$–$V_{GS}$ characteristics, we extract

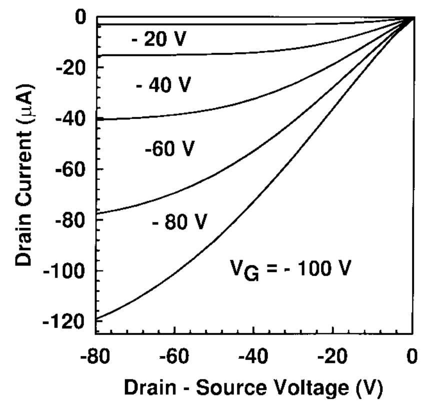


Fig. 3. $I_D$ versus $V_{DS}$ characteristics for a typical stacked pentacene layer TFT with gate length and width of 20 and 50 $\mu$m, respectively, and 350 nm gate dielectric thickness.

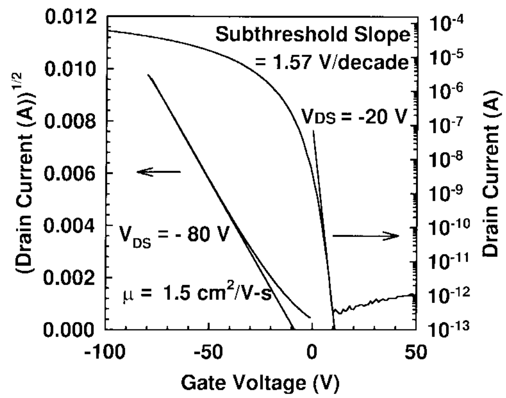


Fig. 4. $I_D^{1/2}$ versus $V_{GS}$ characteristics and $\mathrm{Log}_{10}(I_D)$ versus $V_{GS}$ characteristics for the pentacene TFT of Fig. 3.

a field-effect mobility of 1.5 $cm^2$/V-s at $V_{DS} = -80$ V and a threshold voltage of about $-8$ V. The stacked pentacene layer TFT is a well-behaved square-law device, and the fitting line used for mobility extraction fits the data over a wide range of gate voltage. The $\log(I_D)$–$V_{GS}$ characteristics show the maximum on/off current ratio is greater than $10^8$ at $V_{DS} = -20$ V and the subthreshold slope is about 1.6 V/decade at $V_{DS} = -20$ V. The device parameters for these organic devices are comparable to results typically obtained for hydrogenated amorphous silicon devices.

Importantly, these results demonstrate that the large subthreshold slope commonly observed for organic thin-film transistors is not an intrinsic property. Although the result obtained here, 1.6 V/decade, is larger than that typically observed for a-Si : H devices, it is low enough to allow OTFT use in many applications.

All measurements reported here were made in room air with no precautions taken to prevent degradation of the pentacene film. Although pentacene is a fairly reactive material and oxidation in air might be expected, the device characteristics were essentially unchanged after three months; longer term stability has not been investigated.

## III. Conclusion

The results presented above demonstrate that large subthreshold slope is not an intrinsic property of organic thin-film transistors, and that large threshold voltage is not a necessary property of pentacene thin-film transistors. The device performance improvement obtained by treating the active material/dielectric interface with a self-organizing material underlines the importance of this interface in organic field-effect devices. The photolithographically defined devices described, with field-effect mobility as large as 1.5 $cm^2$/V-s, on/off current ratio larger than $10^8$, near zero threshold voltage, and subthreshold slope less than 1.6 V per decade, are the first OTFT's demonstrated with all these characteristics comparable to a-Si : H TFT's.

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