CS220A Lab#2
Use of Push Buttons

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Sketch

- Assignment#1: seven-bit adder
- Assignment#2: eight-bit comparator
- Assignment#3: adding five four-bit numbers

Lab#2

- Make new folders Lab2_1, Lab2_2, Lab2_3 under CS220Labs to do the assignments
- Refer to lab#1 slides for Xilinx ISE instructions
- Finish pending assignments from lab#1 first

Assignment#1

- Seven-bit adder
  - Only four slide switches on board, but need to input two seven-bit numbers
  - Idea is to divide each input (say, A and B) into two halves and use the four push buttons
    - Place the slide switches in position for the lower four bits of A and push one of the push buttons PB1 (say, BTN_NORTH)
    - Place the slide switches in position for the higher three bits of A and push another push button PB2 (say, BTN_SOUTH)
    - The Verilog module should be written such that when PB1's posedge comes, A[3:0] is stored and when PB2's posedge comes, A[6:4] is stored
    - Input B using the remaining two push buttons

Assignment#1

- Push buttons
  - Read pages 16 and 17 from https://www.xilinx.com/support/documentation/boards_and_kits/ug230.pdf
  - We will use BTN_EAST, BTN_WEST, BTN_SOUTH, and BTN_NORTH along with the slide switches for feeding the inputs in this assignment
  - The seven-bit sum and carry-out should be shown on the eight LEDs
    - LED0 should be sum[0], …, LED6 should be sum[6], and carry-out should be LED7

Assignment#1

- Plan the Verilog modules
  - 1st level: a full adder module that can add two bits with a carry-in
  - 2nd level: an array of seven full adders in ripple-carry mode (carry-in of LSB should be set to 0)
    - Inputs: PB1, PB2, PB3, PB4, Y where Y is a four-bit number; four bits of Y are the slide switch inputs
    - Outputs: seven-bit sum and carry-out
    - Structure:
      - Four always blocks, one each for posedge PB1/2/3/4; sequential assignment for A[3:0], A[6:4], B[3:0], B[6:4] in the always blocks (one assignment per always block); for example, A[3:0] <= Y; A[6:4] <= Y[2:0];
      - Array of seven full adders (outside always blocks)

Assignment#1

- Write a suitable Verilog Test Fixture for ISim simulation
- Run PlanAhead to assign pins to inputs and outputs
  - Make sure to use exactly same IOSTANDARD, PULLUP/PULLDOWN, SLEW, DRIVE for the pins as shown in Chapter 2 of https://www.xilinx.com/support/documentation/boards_and_kits/ug230.pdf
  - Manually add the following in the .ucf file
    - NET "PB1" CLOCK_DEDICATED_ROUTE = FALSE;
    - Same for PB2, PB3, PB4
- Synthesize the seven-bit adder on FPGA

Assignment#2

- Eight-bit comparator
  - Compares two eight-bit inputs A and B
  - Outputs whether A<B, A>B, A==B
  - Accept inputs same way as the previous assignment
  - LED0 should glow if A<B, LED1 should glow if A>B, LED2 should glow if A==B

Assignment#2

- Verilog modules
  - Decompose the eight-bit comparator as follows
    - Number the bit positions 0 to 7 from LSB to MSB
    - Focus on bit position k comparing a_k and b_k
    - Start comparing from MSB and the first bit position where $a_k \neq b_k$ decides whether A<B or A>B; this observation leads to the first level module
    - 1st level: inputs are two bits (a, b) to be compared and less, greater, equal indication from the next MSB position
      - If the less input is 1, the output is less irrespective of a, b
      - If the greater input is 1, the output is greater irrespective of a, b
      - If equal input is 1, output is a<b, a>b, or a==b

Assignment#2

- Verilog modules
  - 2nd level
    - Array of eight 1st level comparators
    - The equal input of MSB comparator should be 1 and the less, greater inputs should be 0
    - The outputs of the LSB comparator are the final outputs
- Write a Verilog Test Fixture with appropriate inputs for ISim
- Use PlanAhead to assign pins and synthesize your hardware on FPGA
  - Manually add the following in the .ucf file
    - NET “PB1" CLOCK_DEDICATED_ROUTE = FALSE;
    - Same for PB2, PB3, PB4

Assignment#3

- Adding five four-bit numbers
  - Let the four-bit numbers be A, B, C, D, E
  - We will make use of the four push buttons and the slide switches to take four four-bit inputs
  - We will make use of the rotary push button (ROT_CENTER) and the slide switches to take the fifth four-bit input
  - Read pages 17, 18, 19 from https://www.xilinx.com/support/documentation/boards_and_kits/ug230.pdf
    - No need to understand the rotary shaft encoder at this point

Assignment#3

- Verilog modules
  - Compute X=A+B and Y=C+D using two four-bit adders
  - Since X and Y are five-bit outputs (including carry-out), compute Z=X+Y using a five-bit adder
  - Since Z is a six-bit output (including carry-out), compute the final output Z+E using a six-bit adder

Assignment#3

- Verilog modules
  - 1st level: full adder module that can add two bits and a carry-in
  - 2nd level: make use of the 1st level module to design three modules: four-bit adder, five-bit adder, six-bit adder
  - 3rd level: connect two four-bit adders, one five-bit adder, and one six-bit adder to design a module that can add the five inputs
  - The output of the six-bit adder is the final output; show the sum in LED0 to LED5 (LSB to MSB) and carry-out in LED6

Assignment#3

- Write a suitable Verilog Test Fixture for ISim
- Use PlanAhead to assign pins
  - Make sure to assign the correct IOSTANDARD, PULLUP/PULLDOWN, SLEW, DRIVE
  - Manually add the following in the .ucf file
    - NET “PB1" CLOCK_DEDICATED_ROUTE = FALSE;
    - Same for PB2, PB3, PB4, PB5
- Synthesize the hardware on the FPGA