Master Slave Flip Flop

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What is flip flop?

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- Flip-flops are used as data storage elements. It is the basic storage element in sequential logic.
- Flip-flops are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

Flip flop v/s Latch

The basic difference between a latch and a flip-flop is a gating or clocking mechanism. For example, let us talk about SR latch and SR flip-flops.

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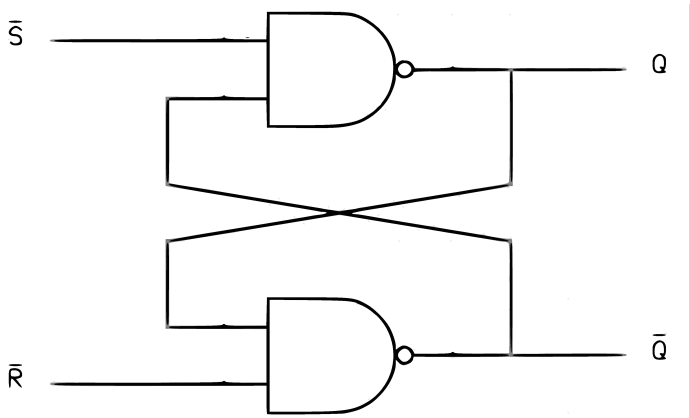
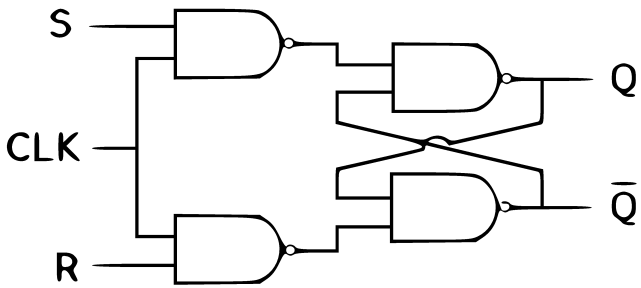


Figure: SR latch



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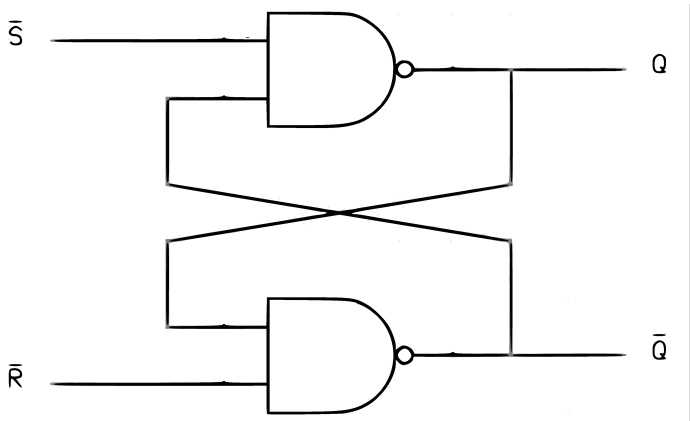

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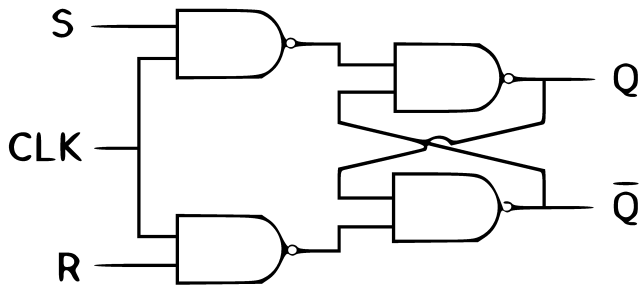

Figure: SR flip flop

A flip flop is synchronous and is also known as gated or clocked SR latch.The output only changes when a active high clock is given.

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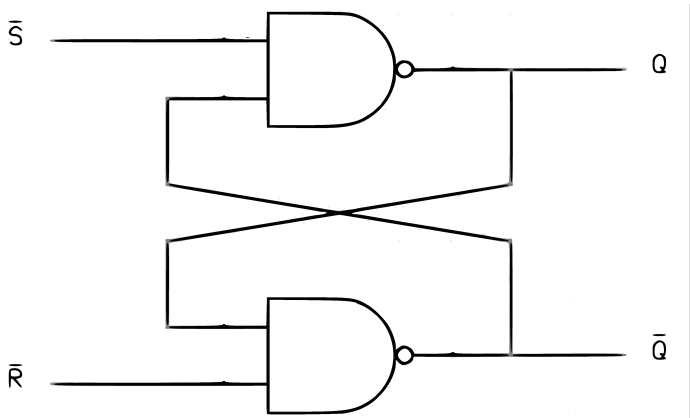

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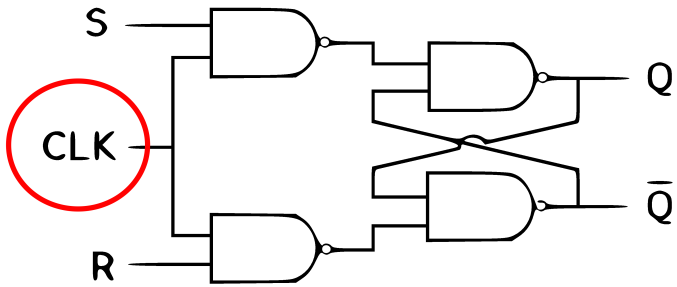

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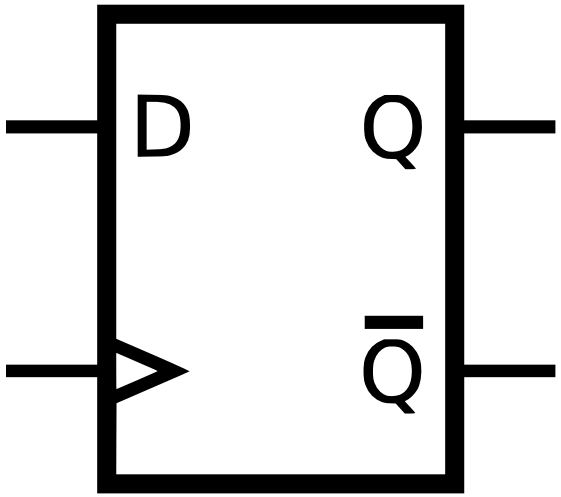

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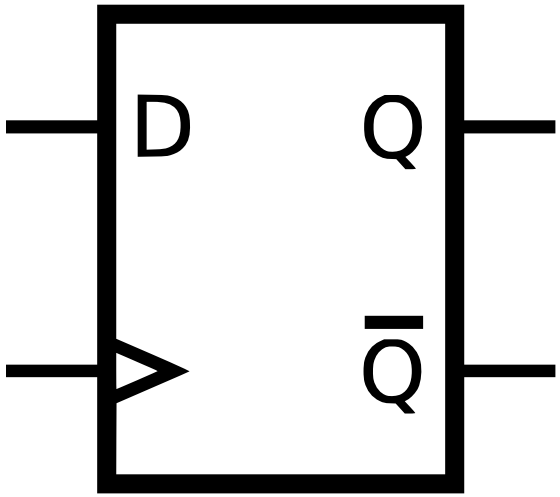
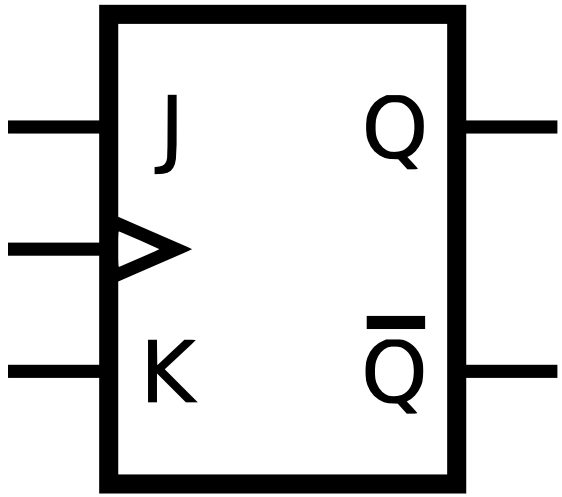


Figure: D type Flip Flop

Clock	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

- D Flip Flop
- JK Flip Flop



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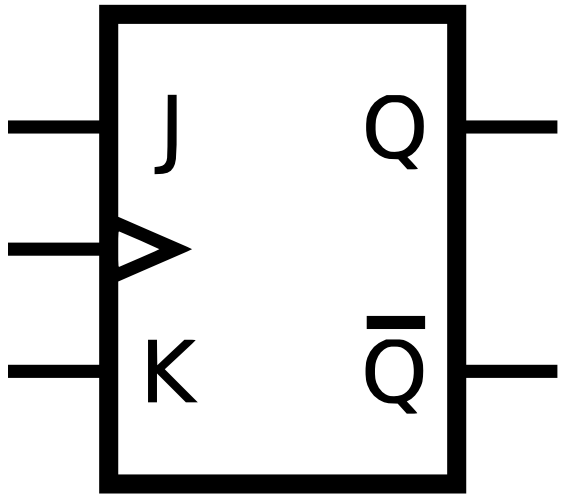

Figure: JK type Flip Flop

J	K	$Q_{(t+1)}$	
0	0	$Q_{(t)}$	*unchanged*
0	1	0	*reset*
1	0	1	*set*
1	1	$\overline{Q}_{(t)}$	*output inversion*

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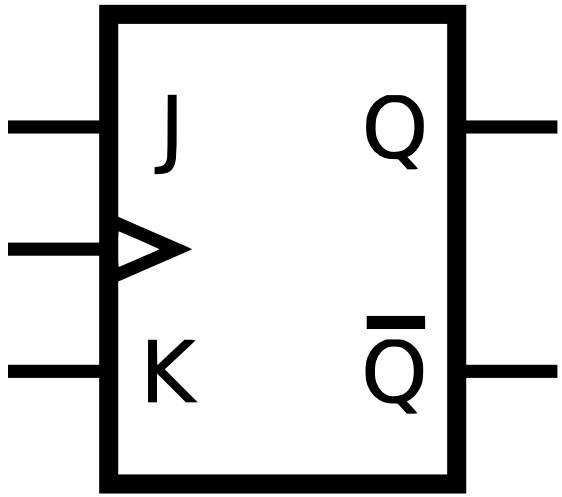

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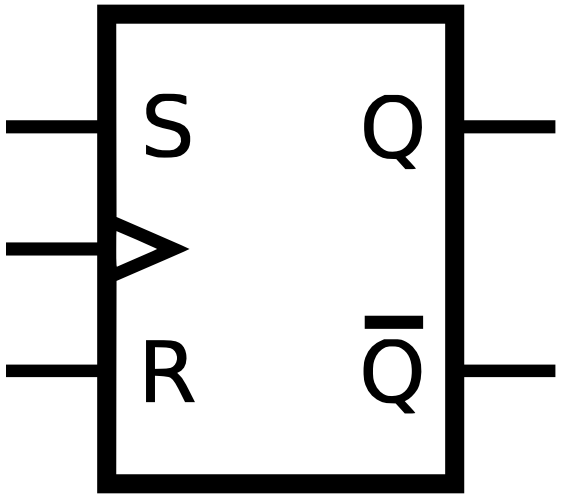

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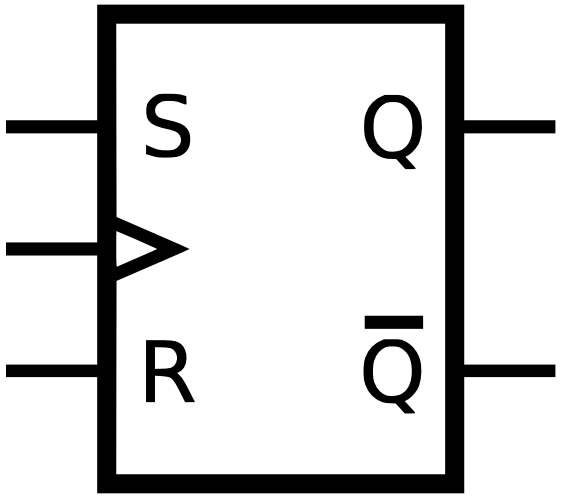

Figure: SR type Flip Flop

S	R	Q	$\overline{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	∞	∞

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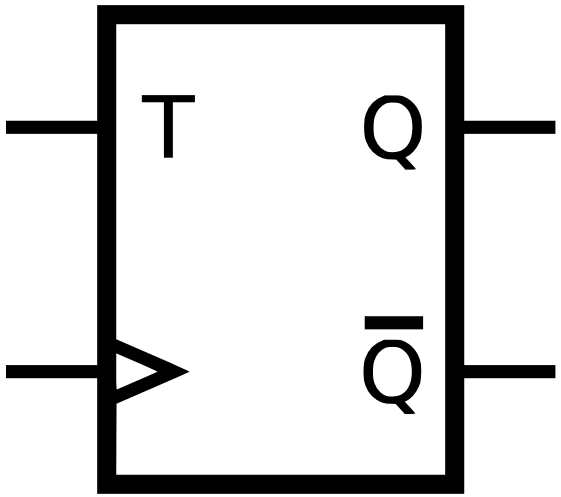

Figure: T type Flip Flop

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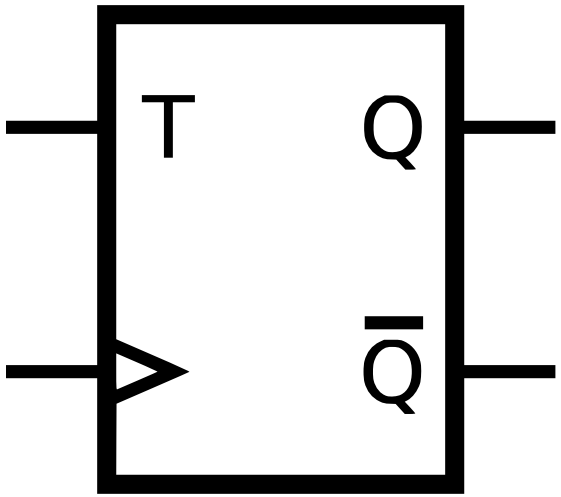

Figure: T type Flip Flop

The truth table of a T-flip-flop

T	Q_{t+1}
0	Q_t
1	$\overline{Qt}$

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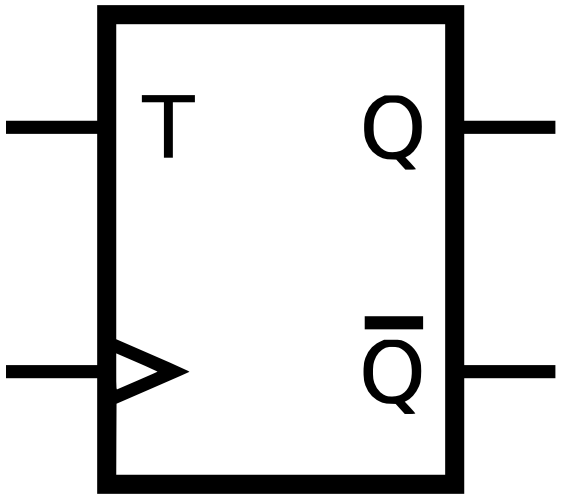

Figure: T type Flip Flop

The truth table of a T-flip-flop

T	Q_{t+1}
0	Q_t
1	$\overline{Qt}$

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- Master Slave flip flop are the cascaded combination of two flip-flops among which the first is designated as master flip-flop while the next is called slave flip-flop (Figure 1).

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- The master flip-flop is triggered by the external clock pulse train while the slave is activated at its inversion i.e. if the master is positive edge-triggered, then the slave is negative-edge triggered and vice-versa.

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- The master flip-flop is triggered by the external clock pulse train while the slave is activated at its inversion i.e. if the master is positive edge-triggered, then the slave is negative-edge triggered and vice-versa.
- This means that the data enters into the flip-flop at leading/trailing edge of the clock pulse while it is obtained at the output pins during trailing/leading edge of the clock pulse. Hence a master-slave flip-flop completes its operation only after the appearance of one full clock pulse for which they are also known as pulse-triggered flip-flops.

Master slave implementation using different flip flops

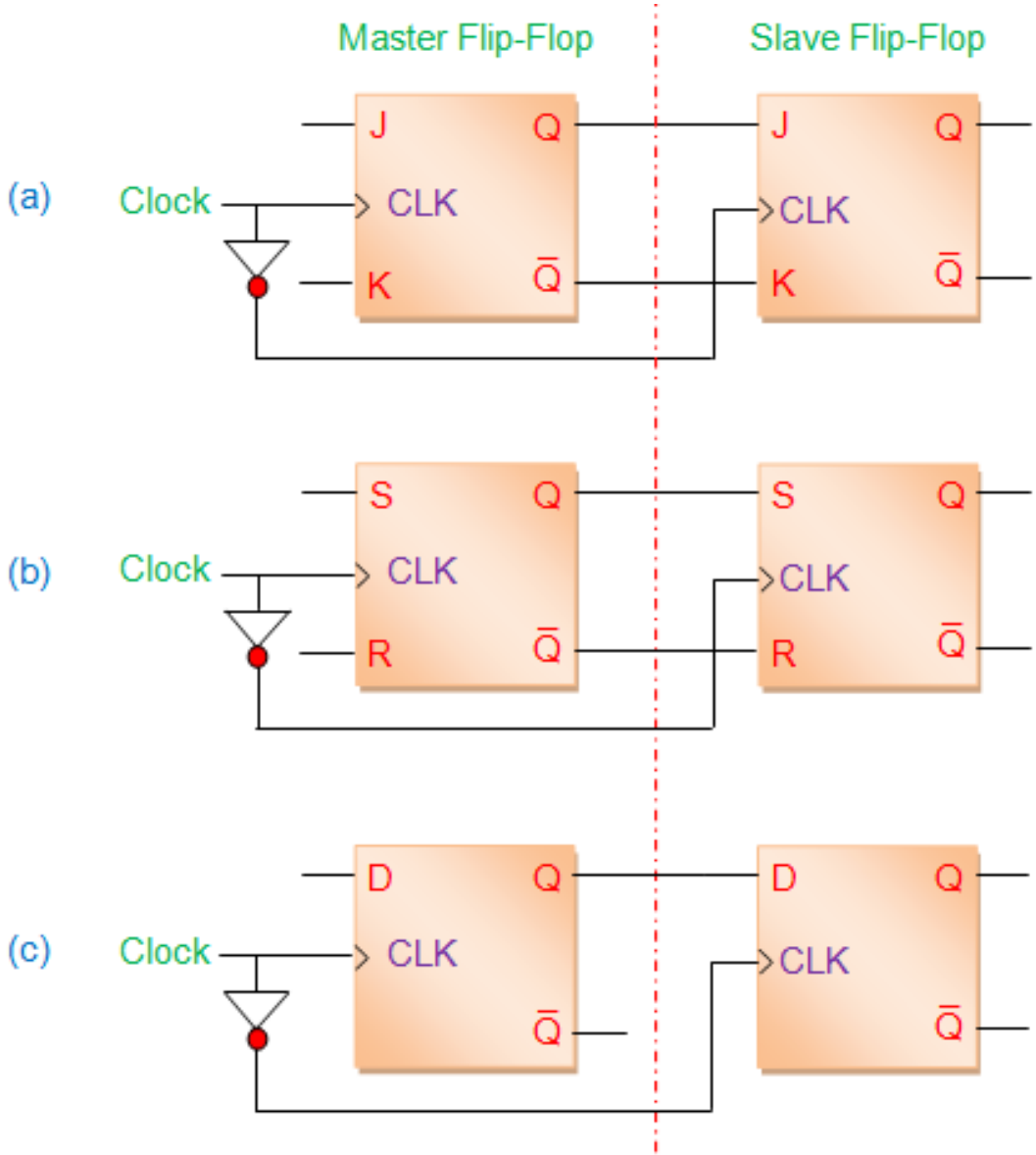

Figure 1 (a) Master-Slave JK flip-flop (b) Master-Slave SR flip-flop (c) Master-Slave D flip-flop

Implementation with gates

We will learn how to implement Master Slave D flip flop with NAND gates.

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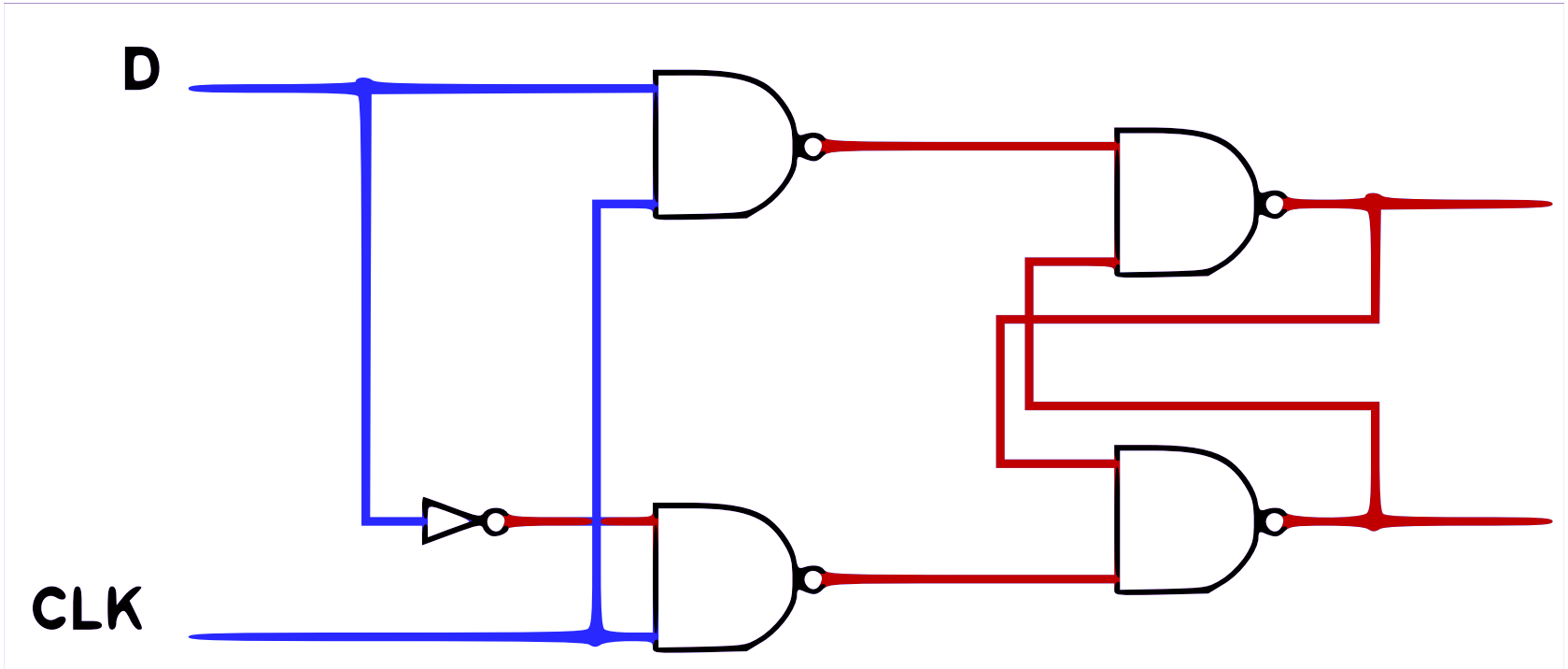

Implementation with gates

Let's construct the second part of our Master Slave flip flop.

Implementation with gates

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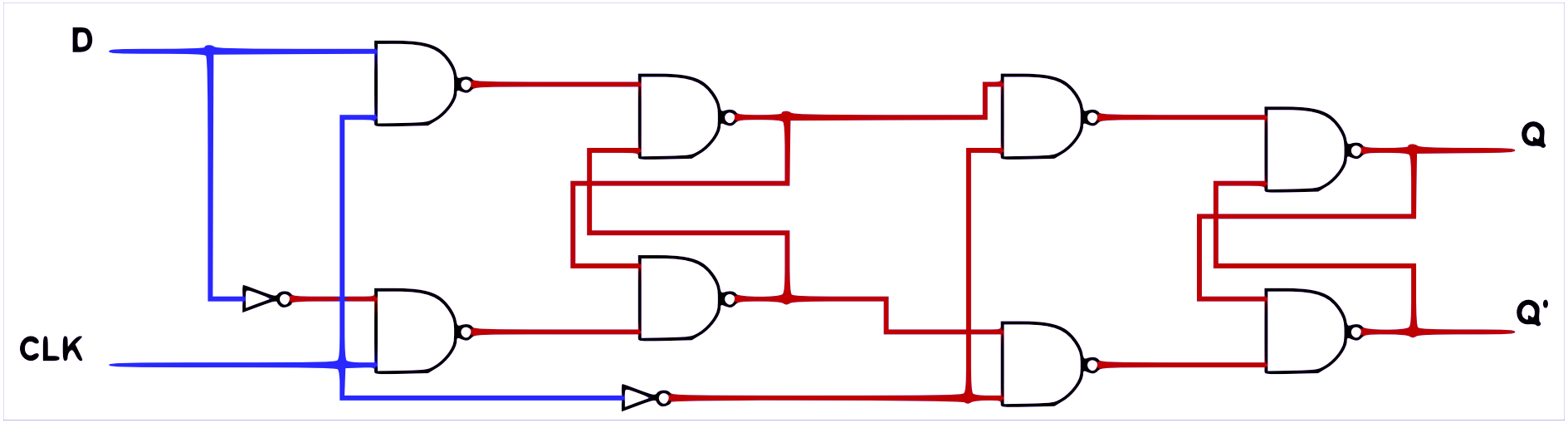
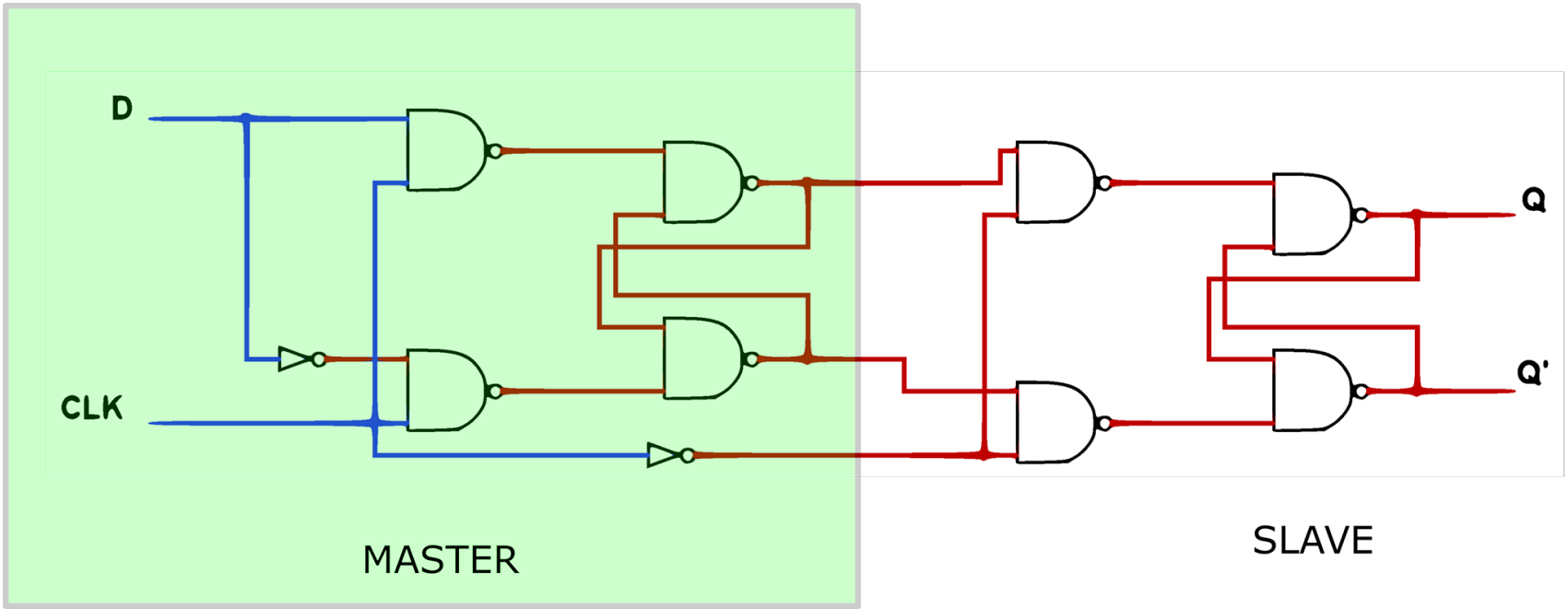


Implementation with gates



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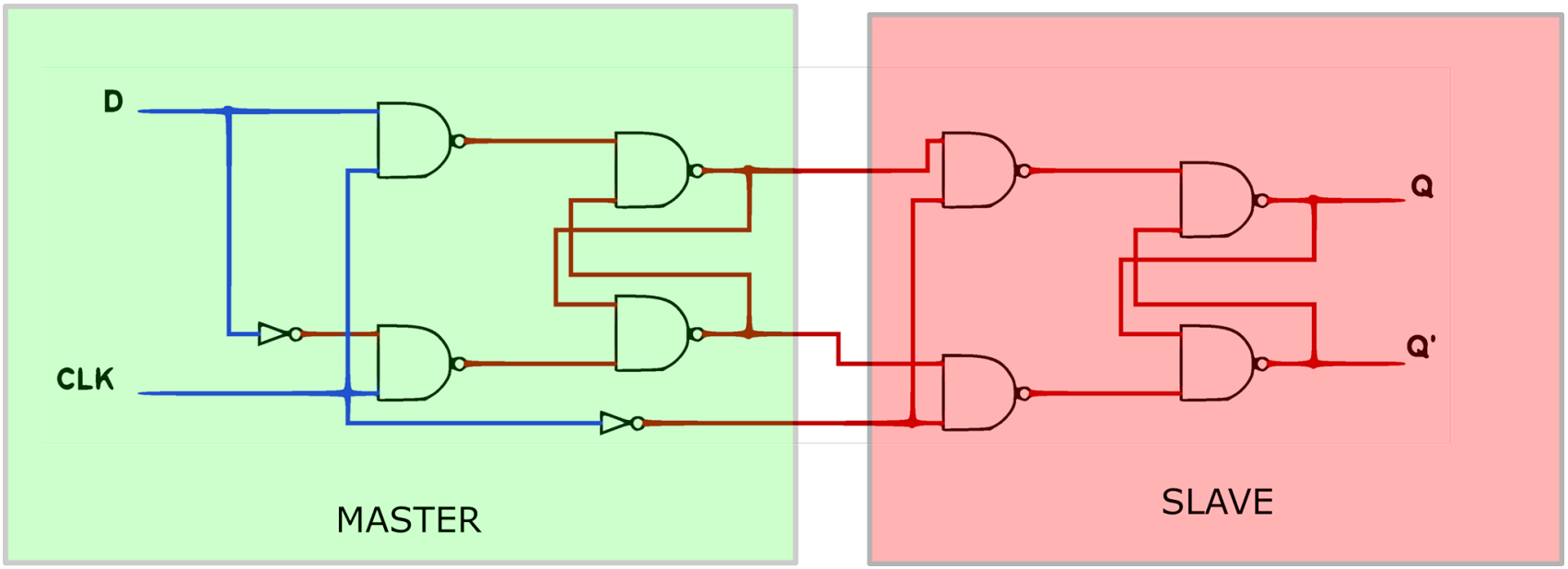

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What should we add to Preset and Clear?

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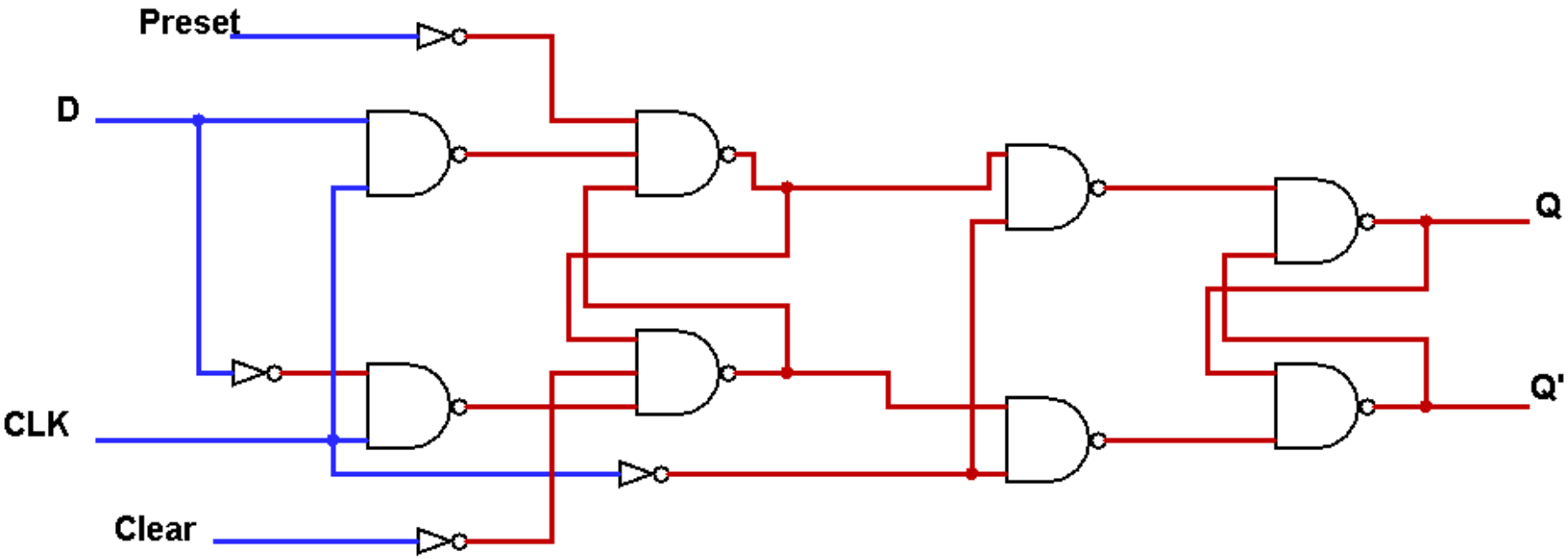
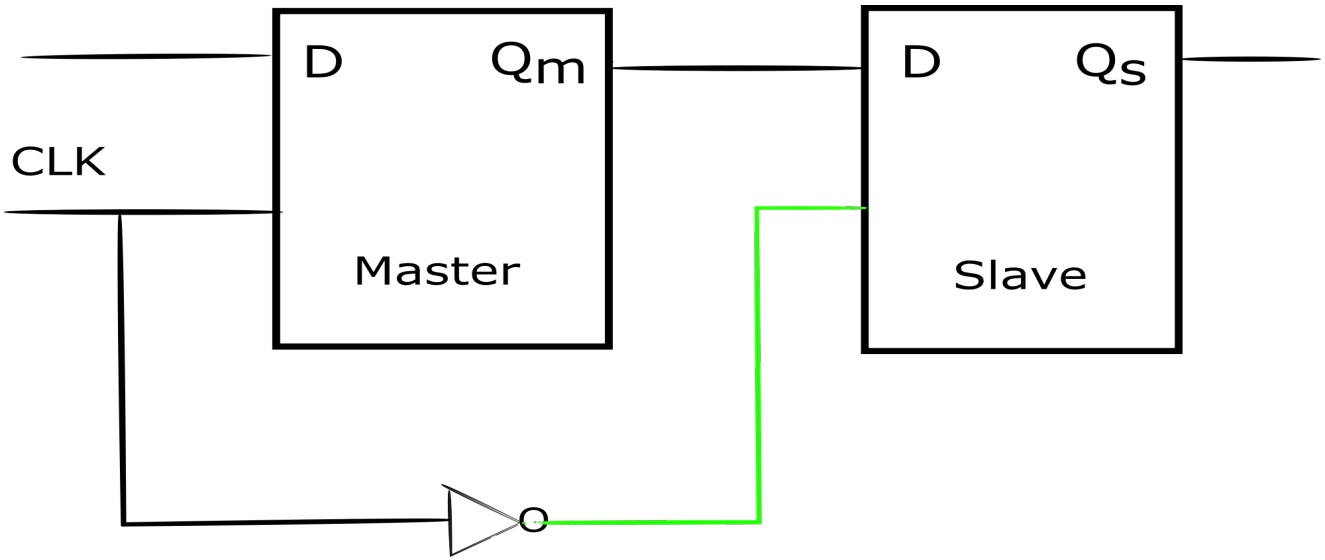
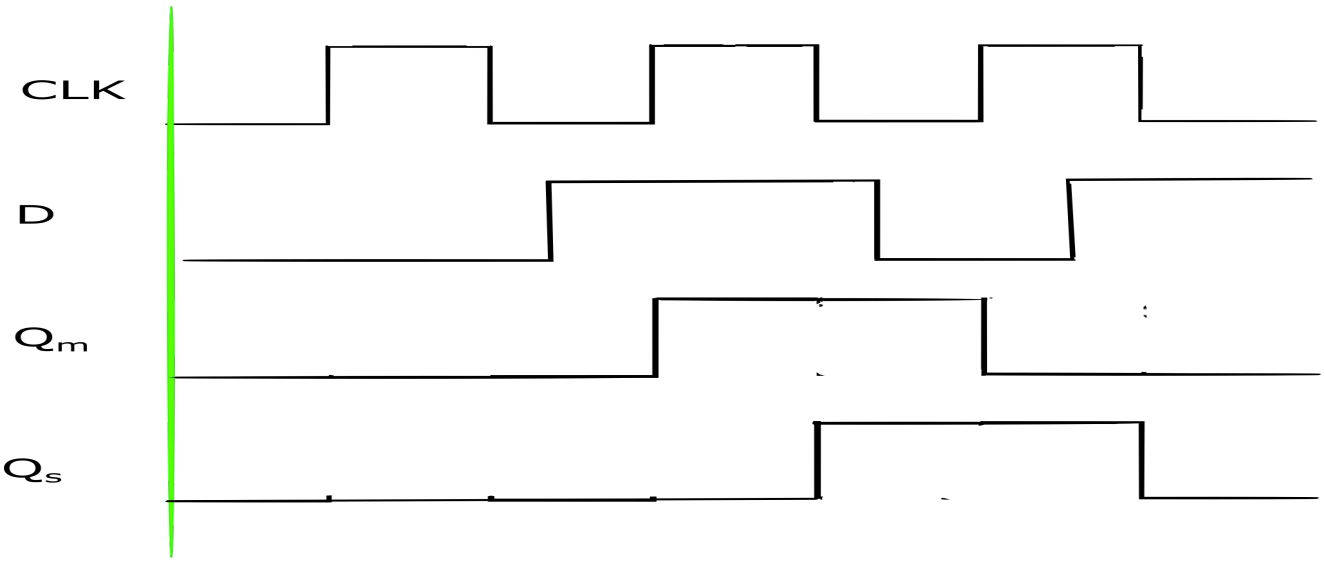


Simulation of Master Slave D flip flop





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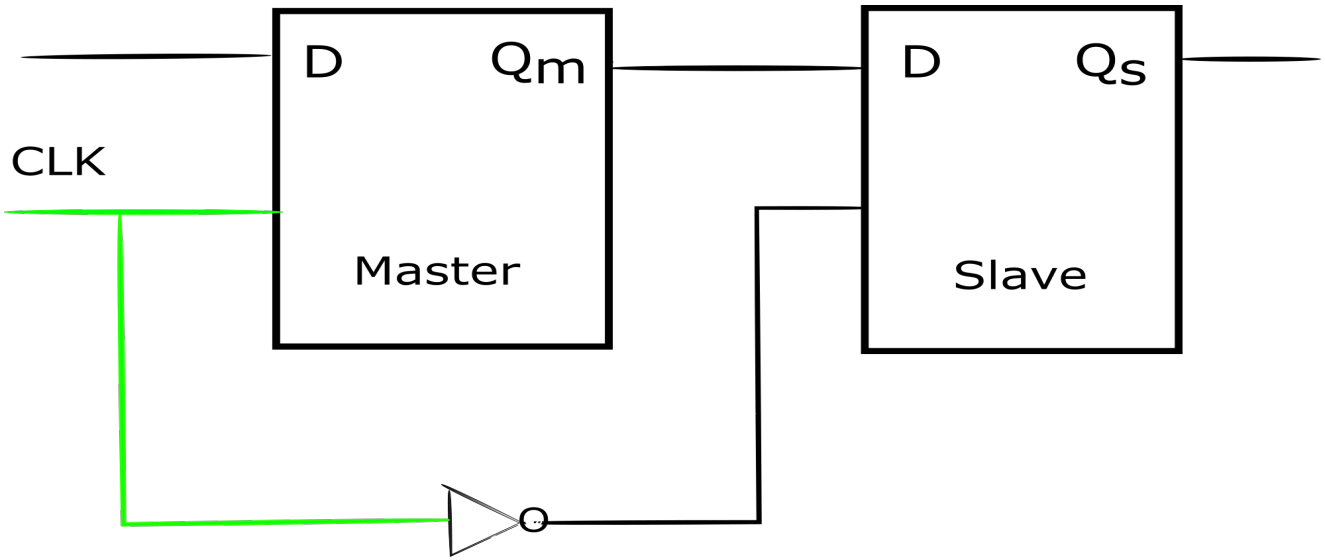

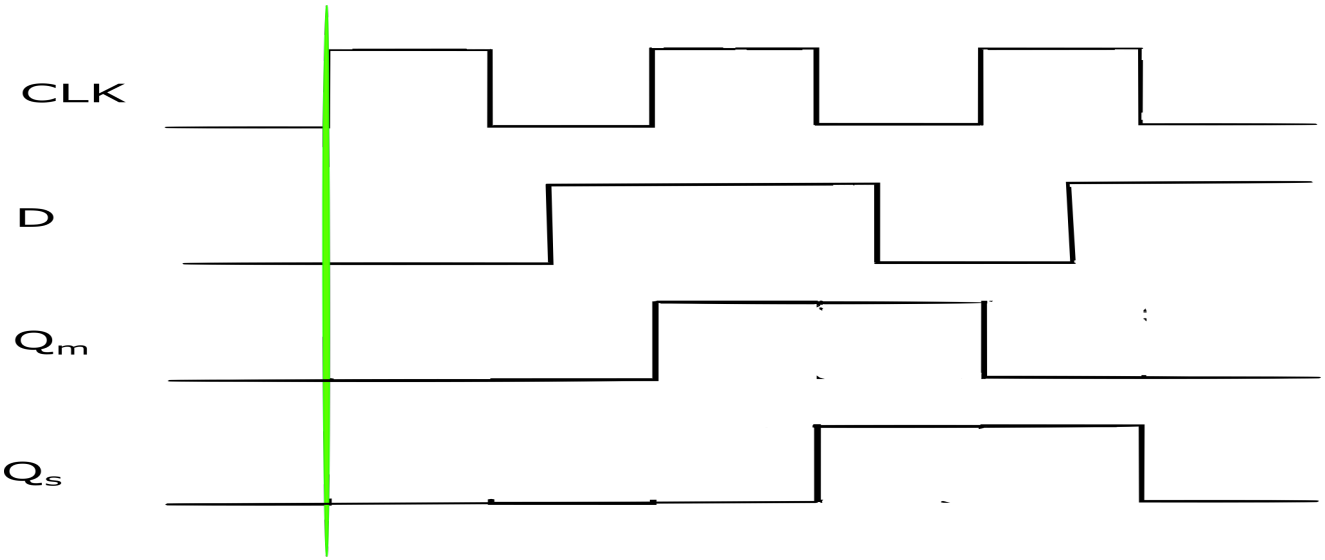

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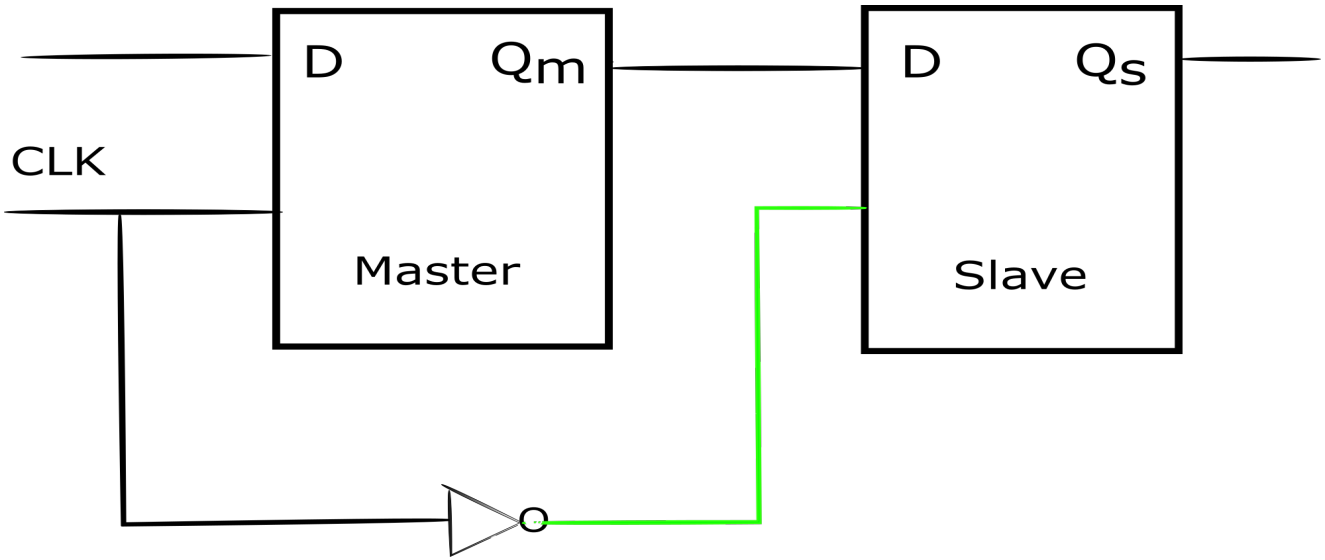

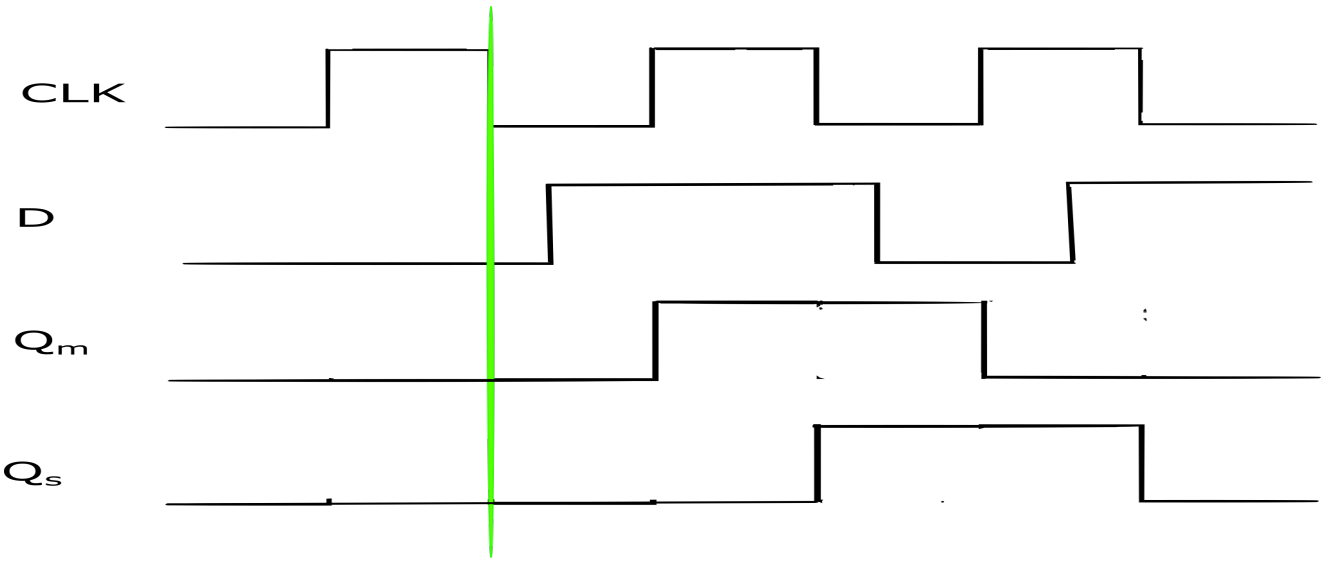

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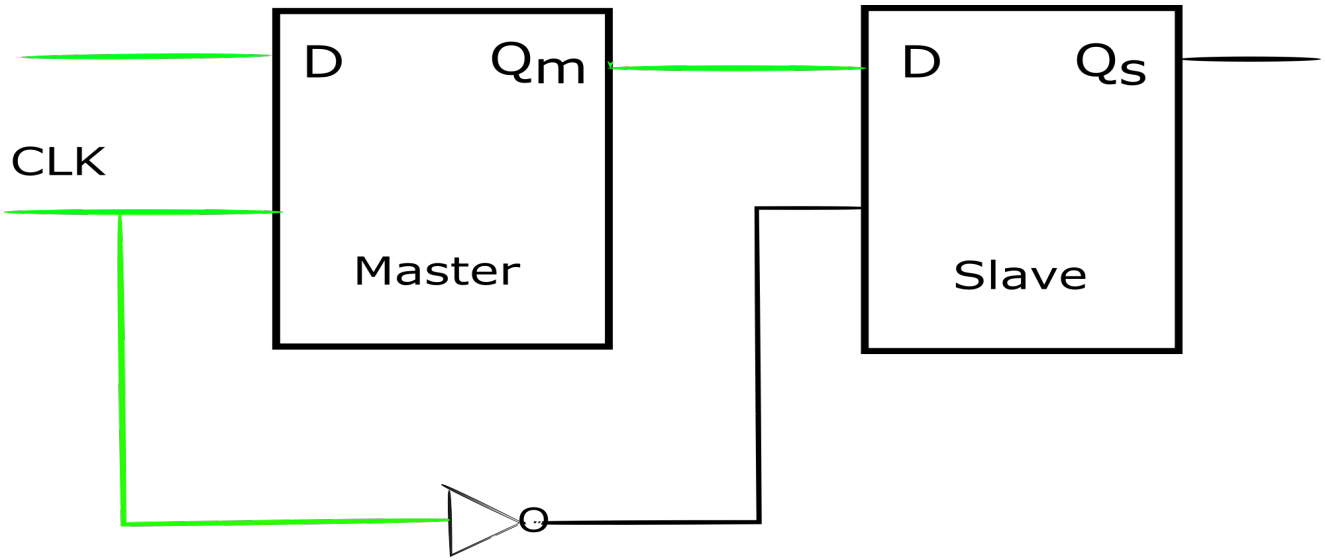

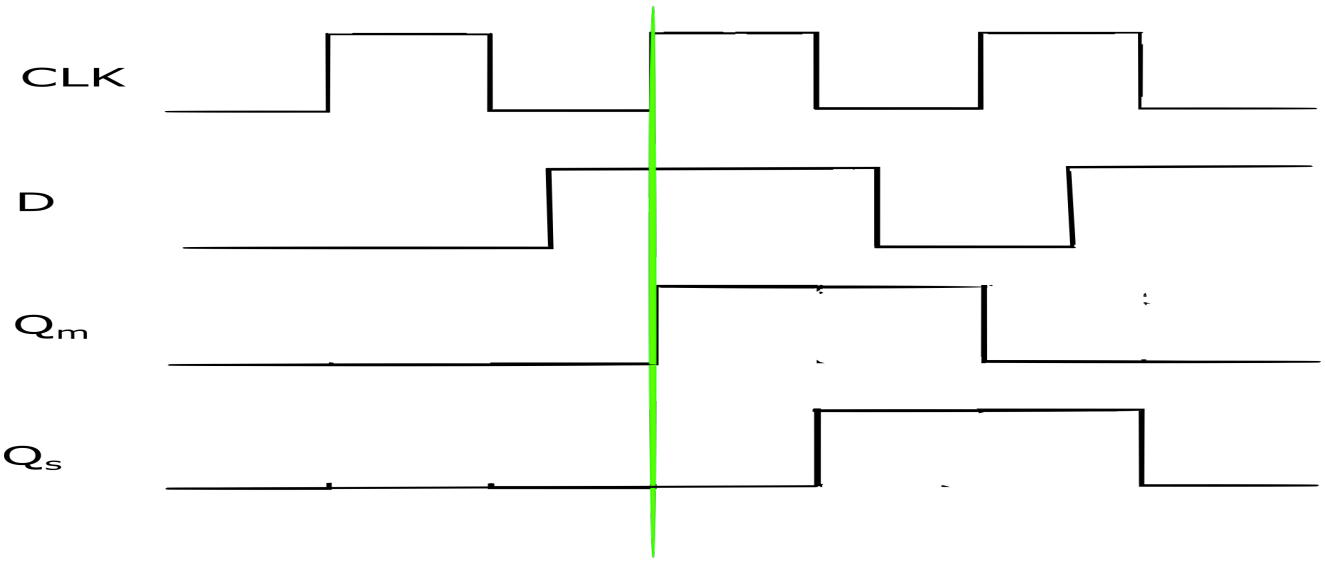

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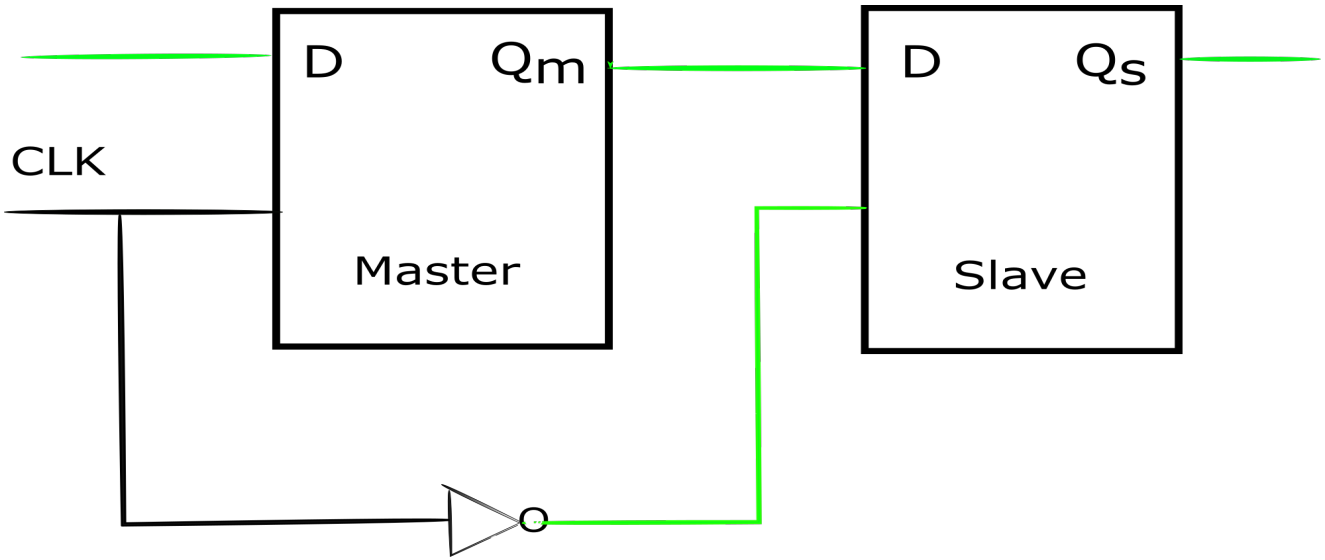

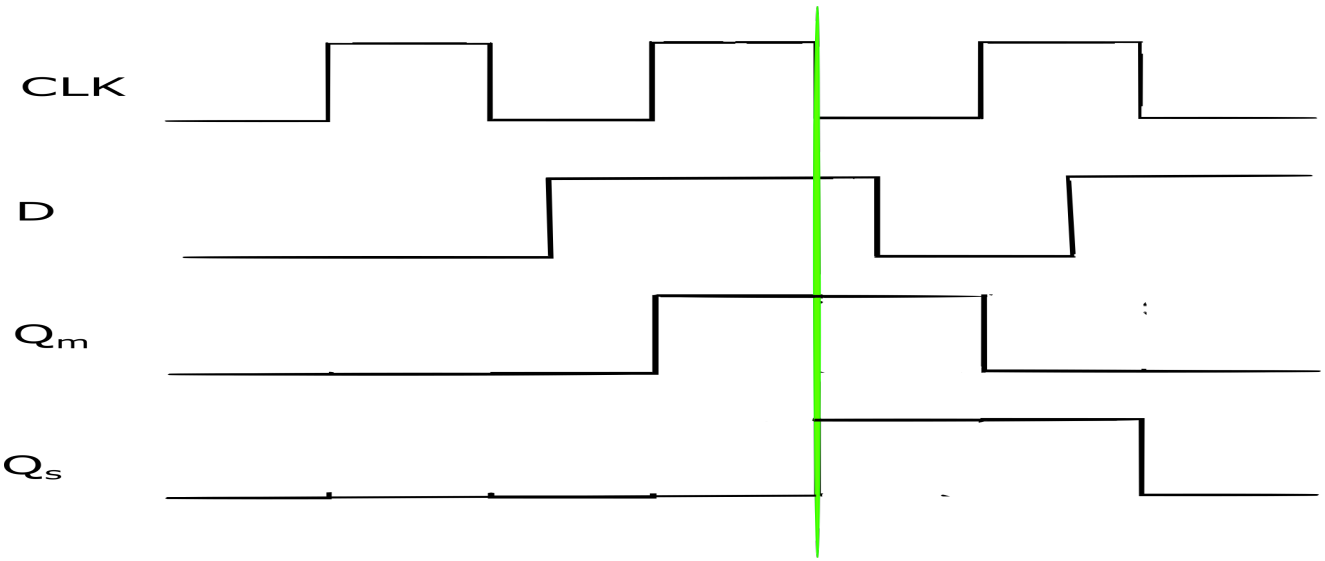

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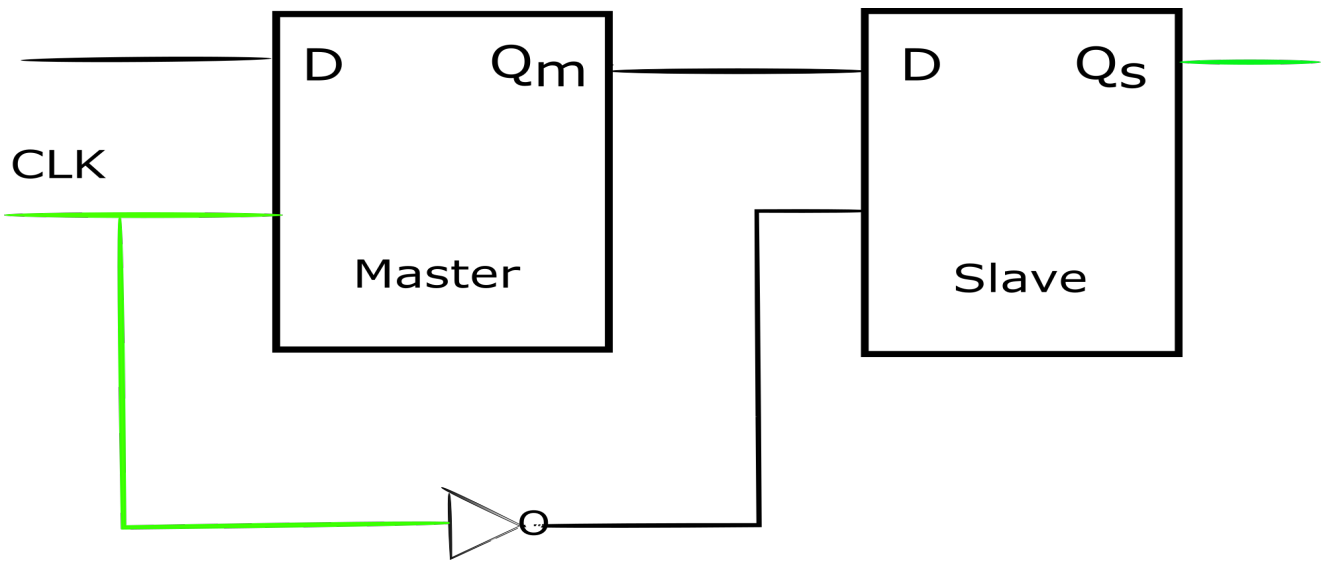

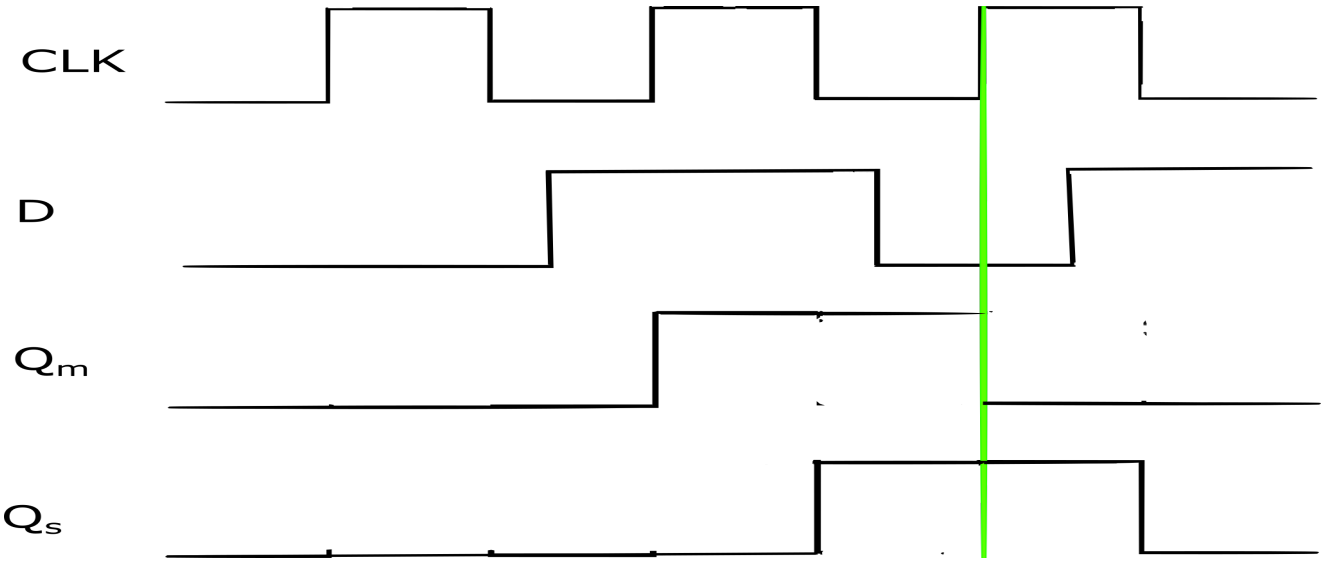

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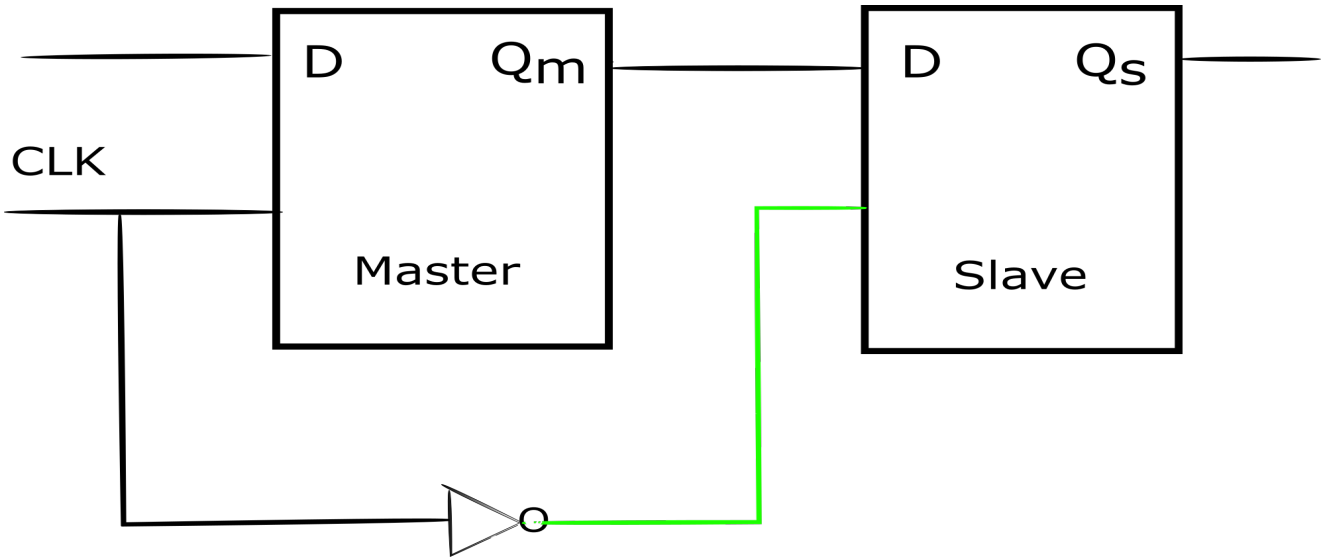

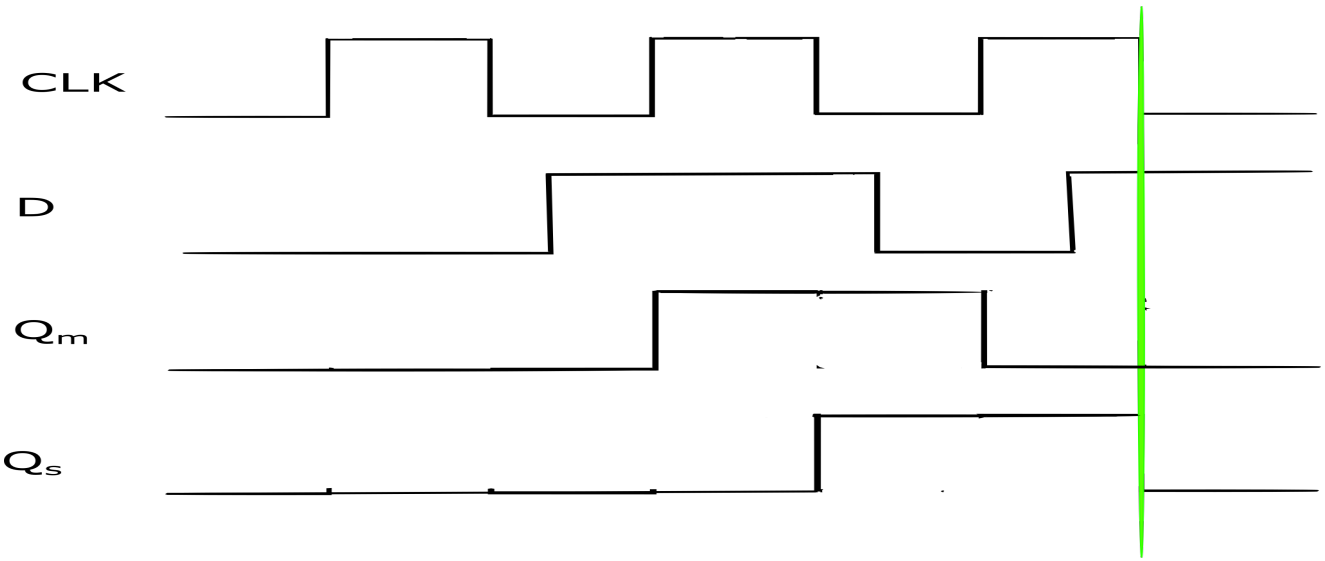

What will be the timing diagram for negative edge triggered Master Slave flip flop?

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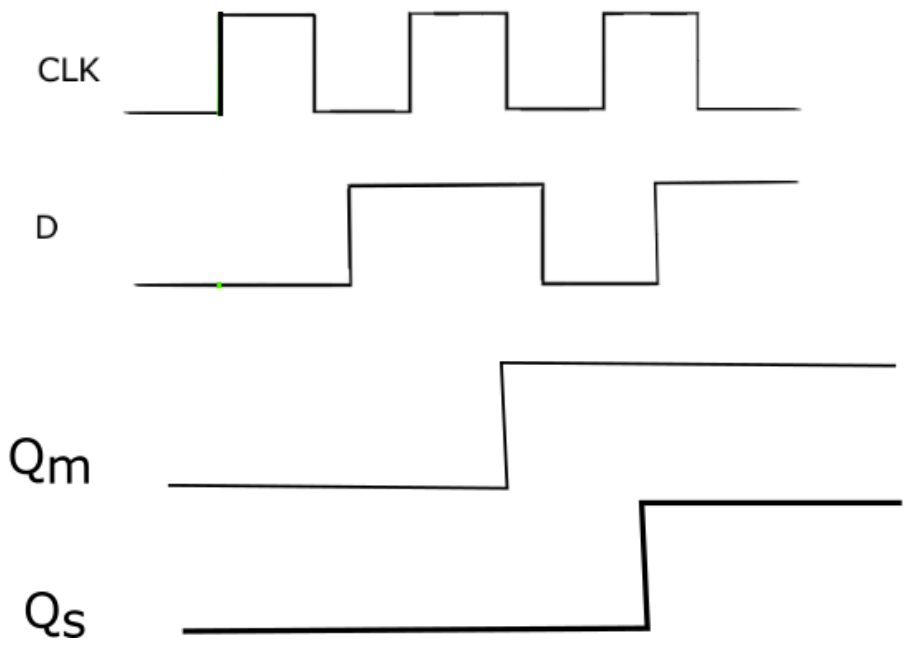

End of Slides

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