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Assignment 5

1) What other parameters could offer insight into the workings of this out-of-order processor?

- One key parameter that would offer a very insight into the workings of this out-of-order processor would be CPI. A low CPI would indicate that the out-of-order execution allows the processor to use all available resources very efficiently, avoiding as much idle time as possible. Some of the other parameters that I think might be useful are “average overall miss latency” and “average gap between requests”.

2) Same as last lab, pick two parameters from those recorded above and plot the results from them based on the data from the various configurations of our CPU to show some kind of meaningful conclusion. Give a brief summary of what you think is happening and what the data is telling you.

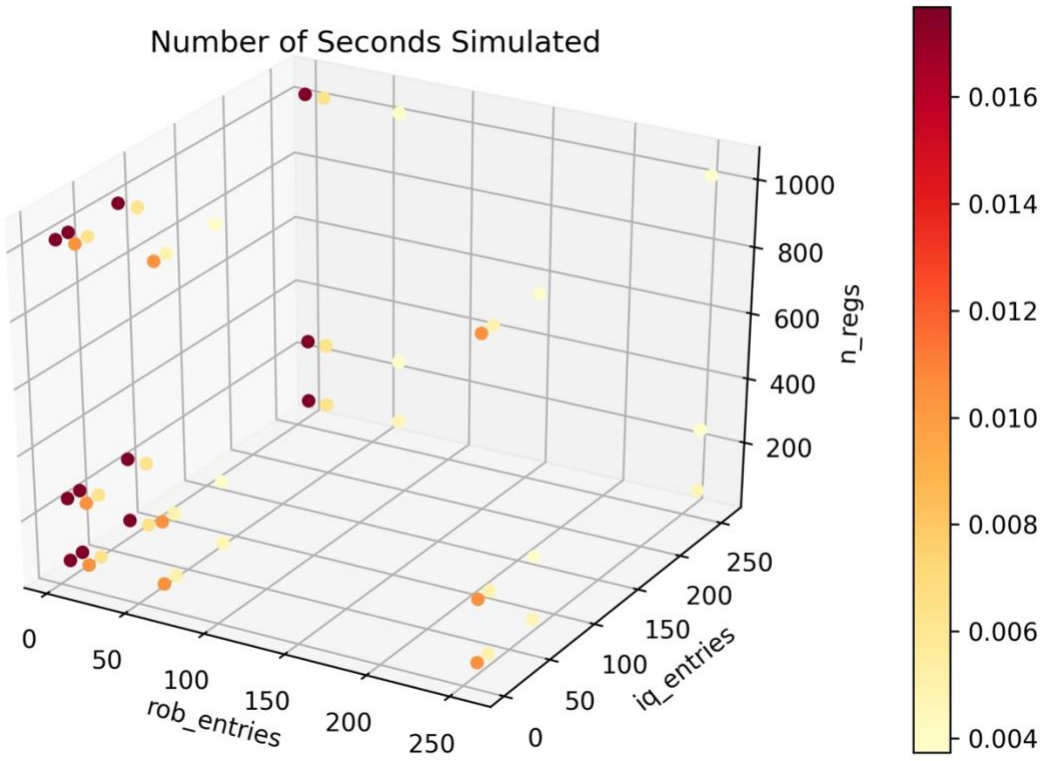

Fig1: Number of Seconds Simulated Variation with Different Parameters

The figure above shows the variation of number of seconds simulated with respect to the 3 parameters (num_rob_entries, num_iq_entries, num_phys_int_regs). One of the first things we can notice from the plot is that “number of simulated seconds” has a strong negative correlation with the number of reorder buffer entries. We see that “sim_seconds” drastically change from very high (maroon) to very low (yellow) as we move along the x-axis towards higher reorder buffer entries. There also seems to be some weak negative correlation of “sim_seconds” with the “number of instruction queue entries”. We can see some experiments where the “sim_seconds” decreases slightly as we increase the number of instruction queue entries. Finally, we also notice that the number of physical integer registers seem to have extremely low to no correlation with the “sim_seconds” metrics. The results are very reasonable for an out-of-order processor. With higher reorder buffer entries and number of instruction queue entries, we are able to make available a larger amount of input data and the out-of-order execution can reorder and execute that data making maximal use of resources which in turn allows the simulation to be completed faster.

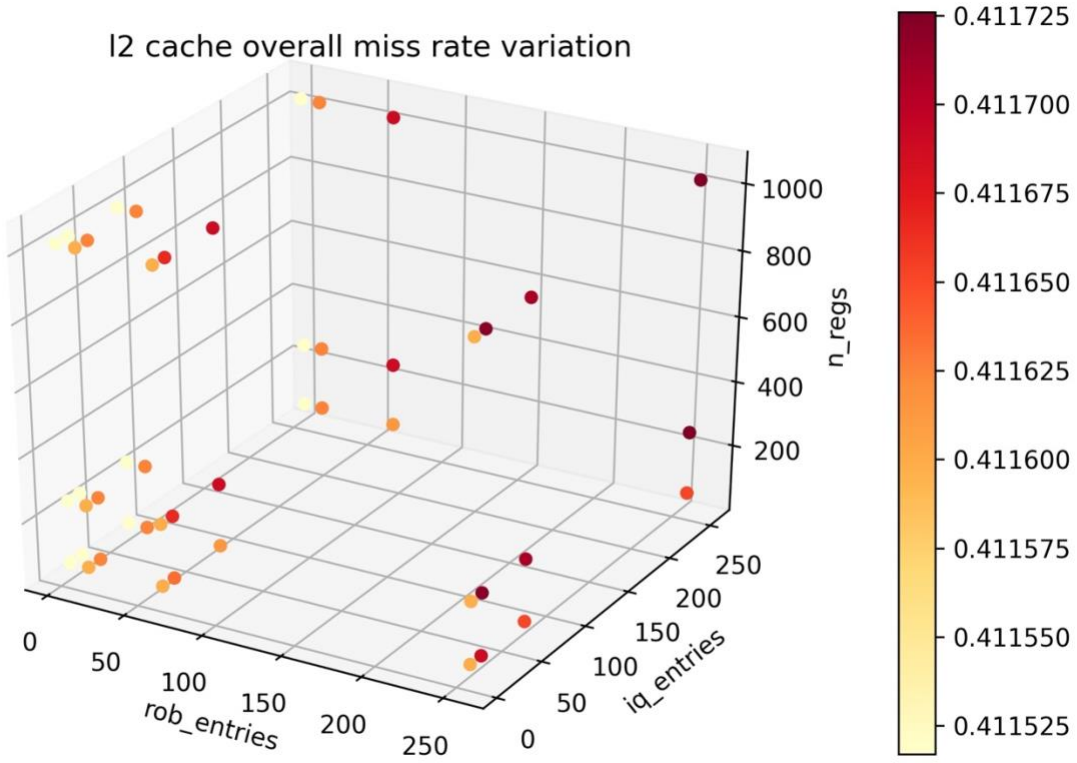

Fig2: L2 Cache Miss Rate Variation with Different Parameters

The figure above shows the variation of number of seconds simulated with respect to the 3 parameters (num_rob_entries, num_iq_entries, num_phys_int_regs). One of the first things we can notice from the plot is that “l2 miss rate” has a strong positive correlation with the number of instruction queue entries. We see that “l2 cache overall miss rate” drastically increases from very low (yellow/orange) to very high (red/maroon) as we move along the y-axis towards higher instruction queue entries. There also seems to be some positive correlation of “l2_miss_rate” with the “number of reorder buffer entries”. We can see some experiments where the “l2_miss_rate” increases as we move along the x-axis and increase the number of reorder buffer entries. Finally, as with “number of simulate seconds”, even with L2 Cache Miss Rate, we notice that the number of physical integer registers seem to have extremely low to no-correlation with the “L2 cache miss rate” metrics. The results are reasonable for an out-of-order processor.