REPORT – 10

- SIDDHANT CHOUDHARY
- HARDIK AGGARWAL

In this assignment the aim was to adjust the last pipeline model to accommodate the operations such as floating point arithmetic or memory accesses in a pipelined processor require variable delays. A floating point computation may depend on the data operands. A memory access may exhibit variable delays due to the cache hierarchy. This can be modeled as follows,

1. The operation completes in one cycle with a probability x (this is considered a HIT).

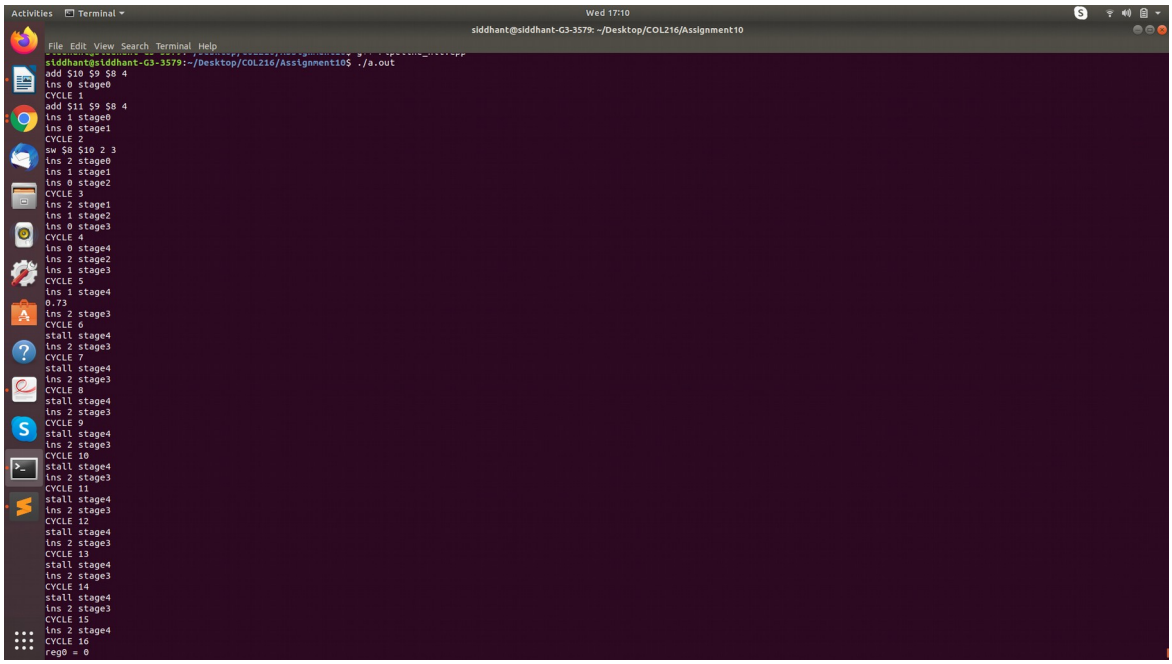
2. The operation requires N cycles with a probability 1-x (this is considered a MISS).

3. Upon a memory request, at end of one cycle, the memory indicates whether the operation was a HIT or MISS. If HIT, the operation is complete. If not, the operation completes N-1 cycles later.

In the implementation of the above model, the variable delays have been considered only for lw and sw instructions as they are the only ones involving the interaction with memory.

We have used a random number generator which generates a random value between 0 and 1.
We have assumed if the random value is greater than a particular value (x=probability of hit) then we will assume that this is a miss and will stall according to N.

TEST CASE -
add $10 $9 $8 4
add $11 $9 $8 4
sw $8 $10 2 3



INITIAL VALUES -

```
reg[8]=8;
reg[9]=9;
reg[10]=10;
ins[8]="13";
ins[9]="14";
ins[14]="15";
ins[10]="10";
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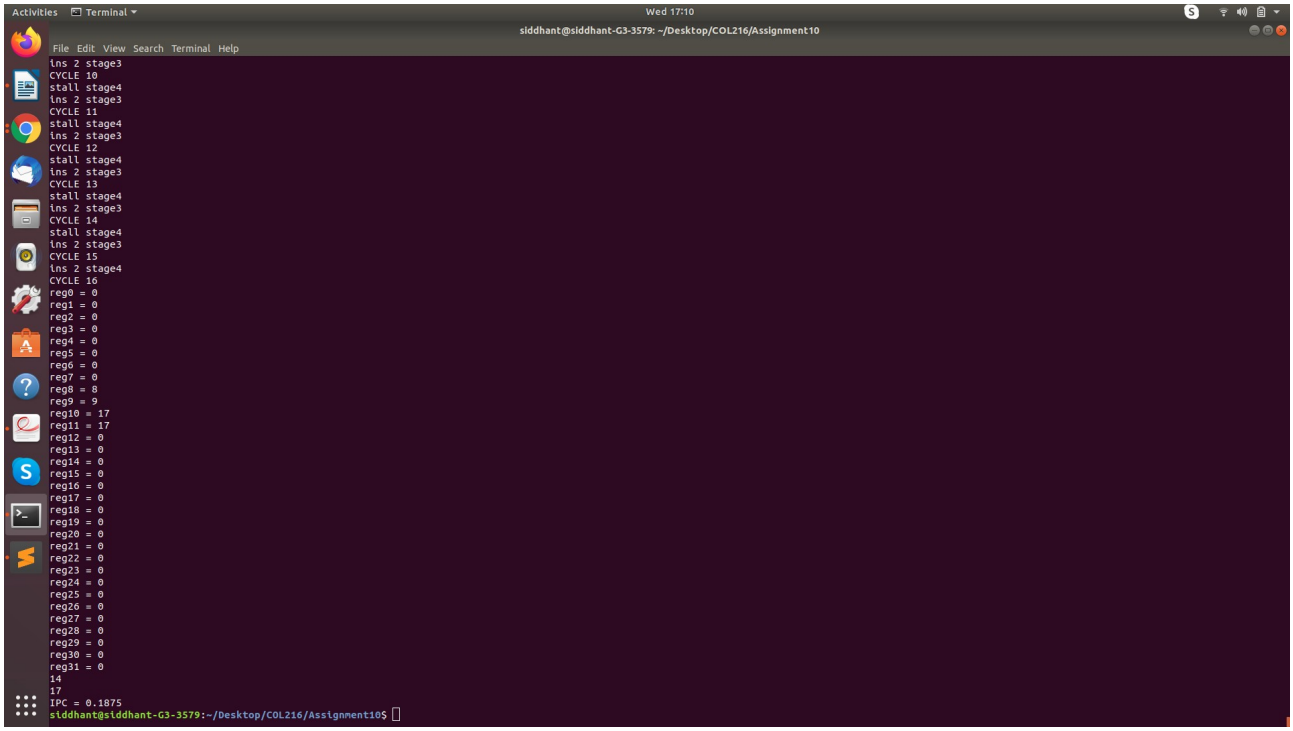
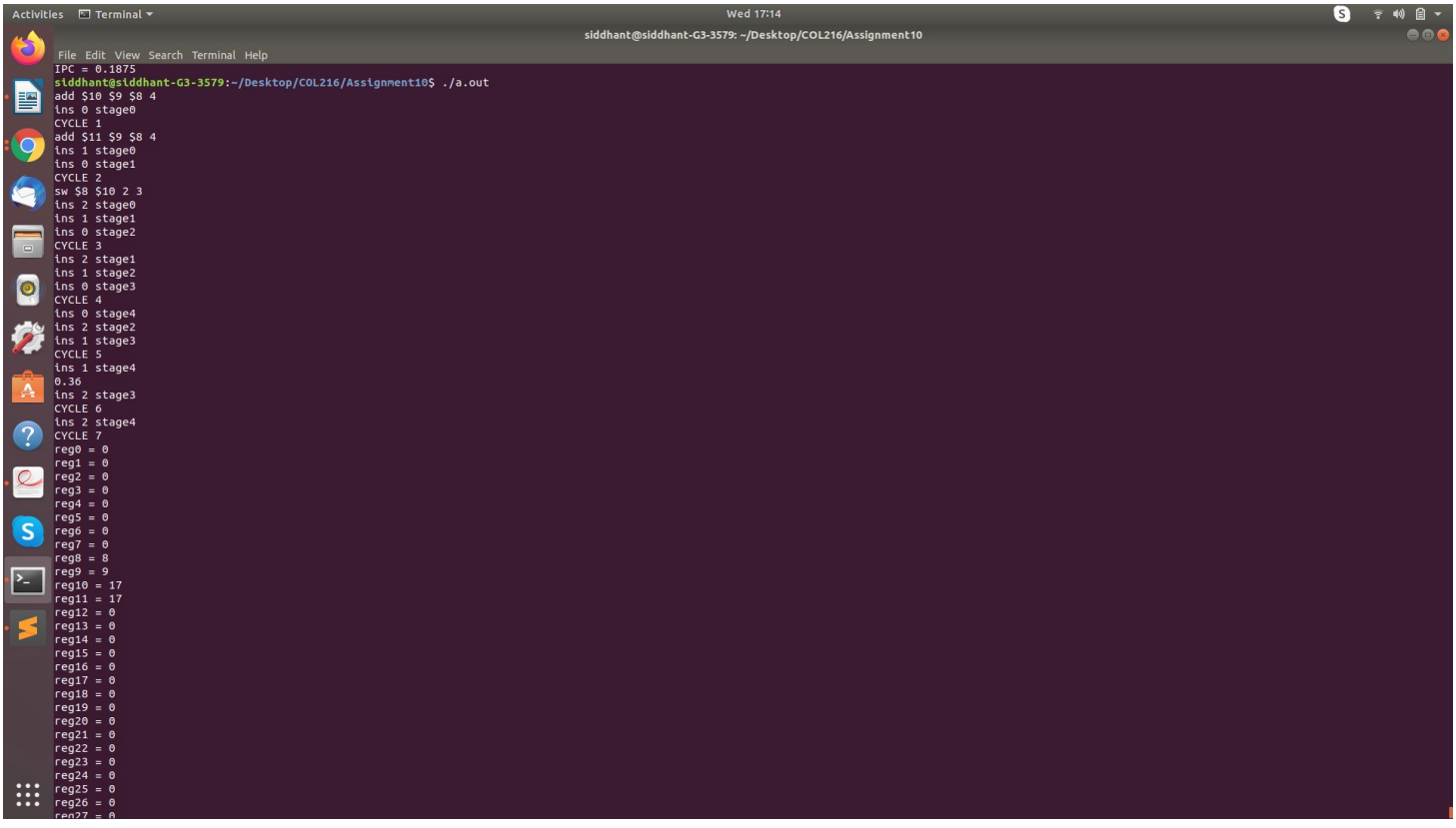
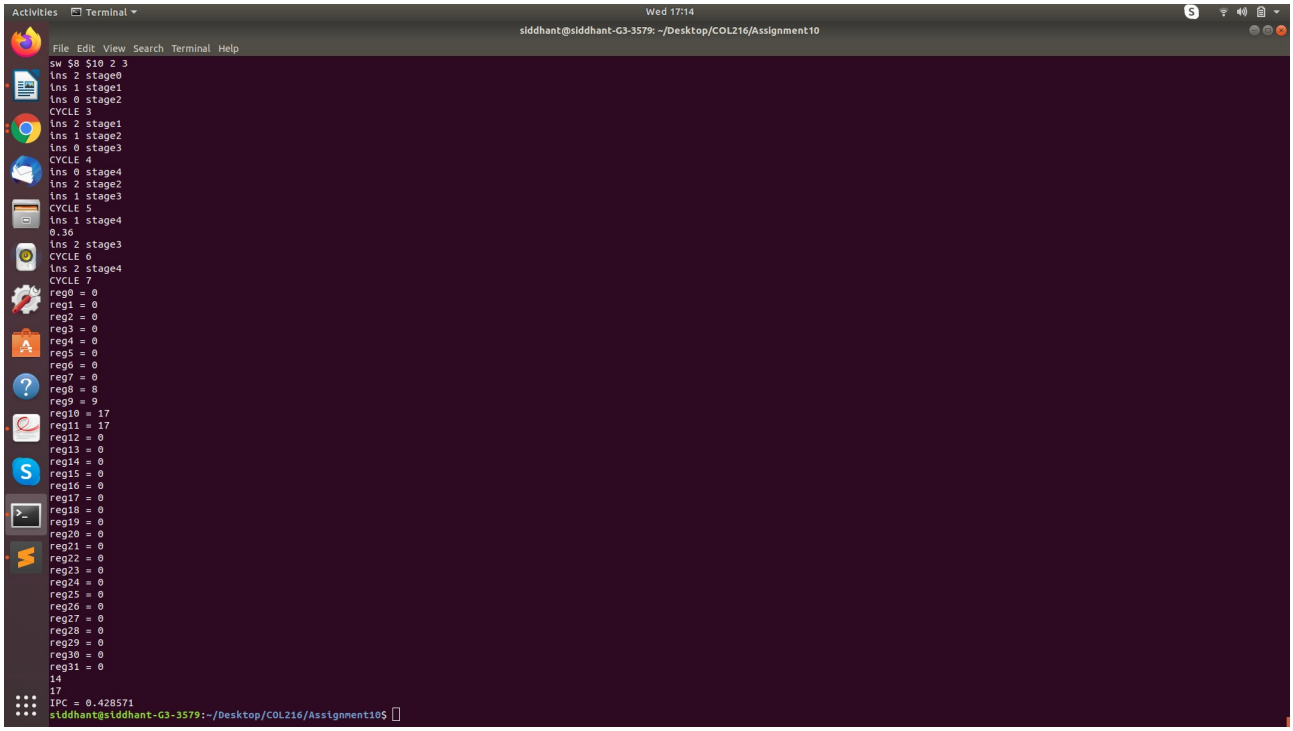


In the above case, since the random number generated is greater then 0.5 it leads to a miss hence the number of cycle become 16. The next case invloves hit hence 7 cycles since the value of N=1.





The ouptut is same for both the cases the only difference is the number of cycles involved.