

REPORT – 10

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In this assignment the aim was to adjust the last pipeline model to accommodate the operations such as floating point arithmetic or memory accesses in a pipelined processor require variable delays. A floating point computation may depend on the data operands. A memory access may exhibit variable delays due to the cache hierarchy. This can be modeled as follows,

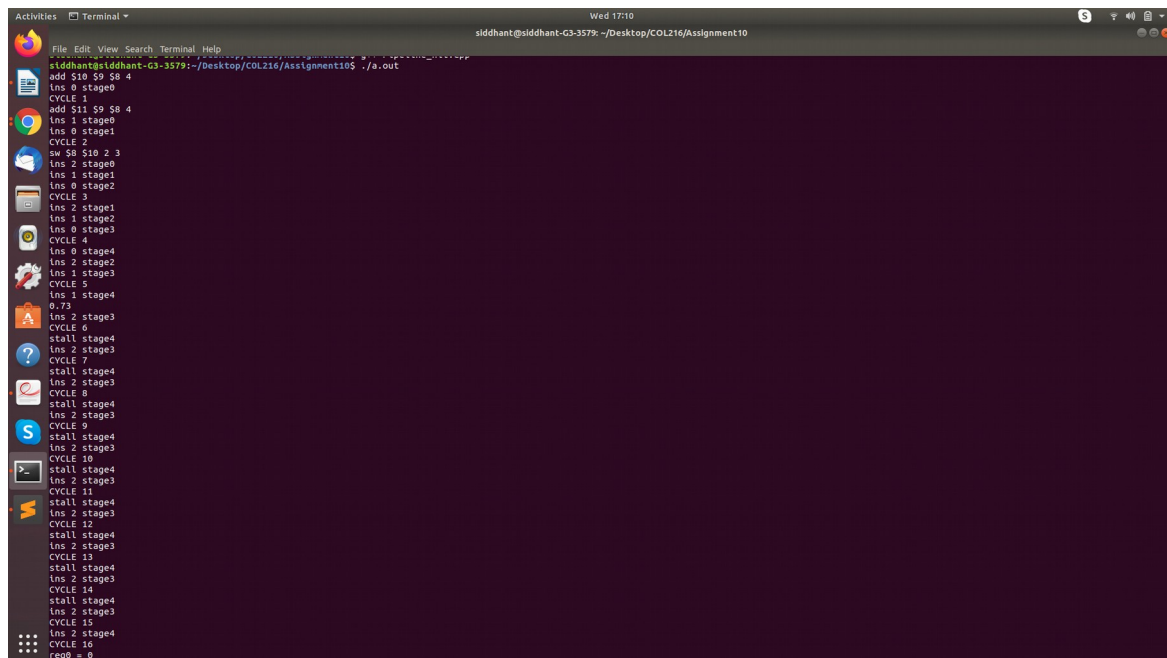
1. The operation completes in one cycle with a probability x (this is considered a HIT).
2. The operation requires N cycles with a probability $1-x$ (this is considered a MISS).
3. Upon a memory request, at end of one cycle, the memory indicates whether the operation was a HIT or MISS. If HIT, the operation is complete. If not, the operation completes $N-1$ cycles later.

In the implementation of the above model, the variable delays have been considered only for lw and sw instructions as they are the only ones involving the interaction with memory.

We have used a random number generator which generates a random value between 0 and 1. We have assumed if the random value is greater than a particular value (x =probability of hit) then we will assume that this is a miss and will stall according to N .

TEST CASE -

```
add $10 $9 $8 4
add $11 $9 $8 4
sw $8 $10 2 3
```



```
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siddhant@siddhant-G3-3579: ~/Desktop/COL216/Assignment10
add $10 $9 $8 4
ins 0 stage0
CYCLE 1
add $11 $9 $8 4
ins 1 stage0
ins 0 stage1
CYCLE 2
sw $8 $10 2 3
ins 2 stage0
ins 1 stage1
ins 0 stage2
CYCLE 3
ins 2 stage1
ins 1 stage2
ins 0 stage3
CYCLE 4
ins 0 stage4
ins 2 stage2
ins 1 stage3
CYCLE 5
ins 1 stage4
0.75
ins 2 stage3
CYCLE 6
stall stage4
ins 2 stage3
CYCLE 7
stall stage4
ins 2 stage3
CYCLE 8
stall stage4
ins 2 stage3
CYCLE 9
stall stage4
ins 2 stage3
CYCLE 10
stall stage4
ins 2 stage3
CYCLE 11
stall stage4
ins 2 stage3
CYCLE 12
stall stage4
ins 2 stage3
CYCLE 13
stall stage4
ins 2 stage3
CYCLE 14
stall stage4
ins 2 stage3
CYCLE 15
ins 2 stage4
CYCLE 16
reg0 = 0
```

INITIAL VALUES -

```
reg[8]=8;
reg[9]=9;
reg[10]=10;
ins[8]="13";
ins[9]="14";
ins[14]="15";
ins[10]="10";
```

```
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ins 2 stage3
CYCLE 10
stall stage4
ins 2 stage3
CYCLE 11
stall stage4
ins 2 stage3
CYCLE 12
stall stage4
ins 2 stage3
CYCLE 13
stall stage4
ins 2 stage3
CYCLE 14
stall stage4
ins 2 stage3
CYCLE 15
ins 2 stage4
CYCLE 16
reg0 = 0
reg1 = 0
reg2 = 0
reg3 = 0
reg4 = 0
reg5 = 0
reg6 = 0
reg7 = 0
reg8 = 8
reg9 = 9
reg10 = 17
reg11 = 17
reg12 = 0
reg13 = 0
reg14 = 0
reg15 = 0
reg16 = 0
reg17 = 0
reg18 = 0
reg19 = 0
reg20 = 0
reg21 = 0
reg22 = 0
reg23 = 0
reg24 = 0
reg25 = 0
reg26 = 0
reg27 = 0
reg28 = 0
reg29 = 0
reg30 = 0
reg31 = 0
16
17
IPC = 0.1875
siddhant@siddhant-G3-3579:~/Desktop/COL216/Assignment10$
```

In the above case, since the random number generated is greater than 0.5 it leads to a miss hence the number of cycle become 16. The next case involves hit hence 7 cycles since the value of N=1.

```
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IPC = 0.1875
siddhant@siddhant-G3-3579:~/Desktop/COL216/Assignment10$ ./a.out
add $10 $9 $8 4
ins 0 stage0
CYCLE 1
add $11 $9 $8 4
ins 1 stage0
ins 0 stage1
CYCLE 2
sw $8 $10 2 3
ins 2 stage0
ins 1 stage1
ins 0 stage2
CYCLE 3
ins 2 stage1
ins 1 stage2
ins 0 stage3
CYCLE 4
ins 0 stage4
ins 2 stage2
ins 1 stage3
CYCLE 5
ins 1 stage4
0.36
ins 2 stage3
CYCLE 6
ins 2 stage4
CYCLE 7
reg0 = 0
reg1 = 0
reg2 = 0
reg3 = 0
reg4 = 0
reg5 = 0
reg6 = 0
reg7 = 0
reg8 = 8
reg9 = 9
reg10 = 17
reg11 = 17
reg12 = 0
reg13 = 0
reg14 = 0
reg15 = 0
reg16 = 0
reg17 = 0
reg18 = 0
reg19 = 0
reg20 = 0
reg21 = 0
reg22 = 0
reg23 = 0
reg24 = 0
reg25 = 0
reg26 = 0
reg27 = 0
```

```
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sw $0 $10 2 3
ins 2 stage0
ins 1 stage1
ins 0 stage2
CYCLE 3
ins 2 stage1
ins 1 stage2
ins 0 stage3
CYCLE 4
ins 0 stage4
ins 2 stage2
ins 1 stage3
CYCLE 5
ins 1 stage4
0.36
ins 2 stage3
CYCLE 6
ins 2 stage4
CYCLE 7
reg0 = 0
reg1 = 0
reg2 = 0
reg3 = 0
reg4 = 0
reg5 = 0
reg6 = 0
reg7 = 0
reg8 = 0
reg9 = 9
reg10 = 17
reg11 = 17
reg12 = 0
reg13 = 0
reg14 = 0
reg15 = 0
reg16 = 0
reg17 = 0
reg18 = 0
reg19 = 0
reg20 = 0
reg21 = 0
reg22 = 0
reg23 = 0
reg24 = 0
reg25 = 0
reg26 = 0
reg27 = 0
reg28 = 0
reg29 = 0
reg30 = 0
reg31 = 0
14
17
IPC = 0.428571
siddhant@siddhant-G3-3579:~/Desktop/COL216/Assignment10$
```

The output is same for both the cases the only difference is the number of cycles involved.