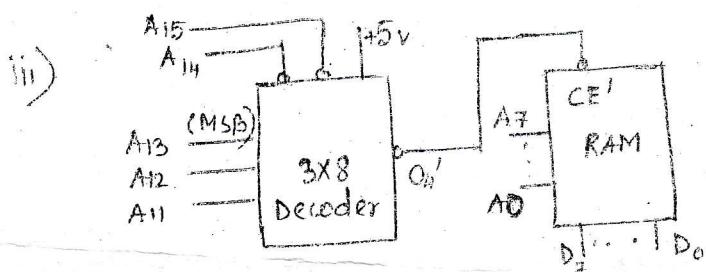
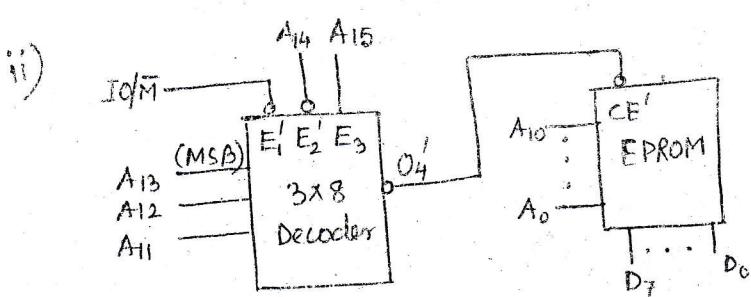
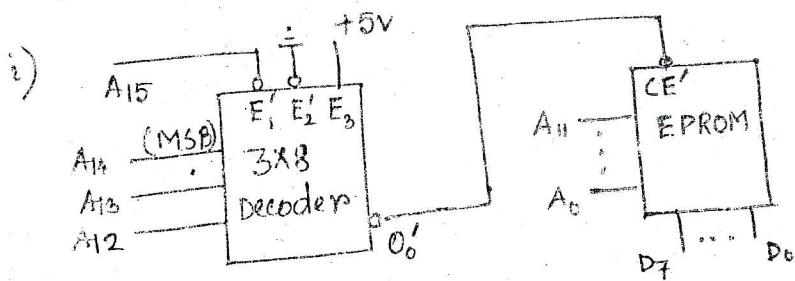


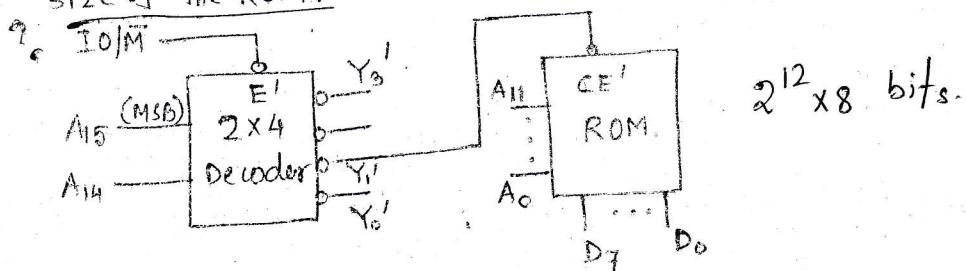
## Microprocessor

1. What do you mean by microprocessor? What is microcontroller? How they differ?
2. Discuss the organization of microprocessor based system with bus architecture.
3. What are the different registers available in 8085 μP? Explain the functions of each.
4. What are the different category of instruction available in 8085? Explain with examples.
5. Discuss the opcode format of 8085A μP.
6. What do you mean by addressing mode? What are the different addressing modes available in 8085A? Discuss with example.
7. How does 8085 differentiate between data and opcode?
8. List four operations commonly performed by MPU.
9. What is databus, address bus and controlbus? Why data bus is bidirectional?
10. Discuss the functions of different pins available in 8085A.
11. What do you mean by multiplexing of data and address bus? What are its disadvantages? How these disadvantages can be solved by demultiplexing?
12. Define: T-state, machine-cycle and Instruction cycle.
13. Illustrate the steps and timing diagram of Opcode fetch operation stored at location  $2000H$ . What are the steps performed in decoding and execution of an instruction.
14. Draw and illustrate the timing diagram of memory read, memory write, opcode fetch, I/O read and I/O write. If clock frequency of 8085 is 2MHz, find execution time of each operations mentioned above.
15. What do you mean by absolute (Full) and partial address decoding? What are their advantages and disadvantages? What is fold back memory?  
Aijf Pot.

Q6. Explain the decoding logic and find its memory address range of the following circuits.



Q7. Identify the primary address range and mirror (foldback) address range of memory chip for the given circuit. Also find the size of the ROM.



Q8. What do you mean by memory mapped I/O and I/O (peripheral) mapped I/O. Explain relative advantages and disadvantages.

A18. Can an input port and output port have the same port address?

Q19. Can an input port and output port have the same port address if we decode the high

20. How will the port number be affected if we decode the high

? Order address lines A15-A8 rather than AD<sub>7</sub>-AD<sub>0</sub> in 8085?

21. In a memory mapped-I/O, how does microprocessor differentiate between an I/O and memory?

? Can an I/O have the same address as a memory register?

22. Why is 16-bit address stored in memory in reverse order -

? ... auto first followed by higher order byte?

23. In I/O mapped I/O, can an input port and an output port have the same port address? How 8085 differentiate between the ports?

24. Explain why a latch is used for an output port but a tristate buffer is used for an input port.

25. Draw the timing diagram and state the machine cycle and T-state required by each of the following instructions.

MOV Rd, Rs ; MVI R, 8-bit; IN 8-bit addr ; OUT 8bit addr;

ADD R; ADI 8-bit; JMP 16-bit addr; JC 16-bit addr; NOP;  
HLT;

26. Specify the contents of the registers and the flag status as the following programs are executed. Specify the output at port when applicable.

i) MVI A, 00<sub>H</sub>  
MVI B, F8<sub>H</sub>  
MOV C, A  
MOV D, B

iv) MVI A, 5E<sub>H</sub>  
ADI A2<sub>H</sub>  
MOV C, A

vii) MVI A, A9<sub>H</sub>  
MVI B, 57<sub>H</sub>  
ADD B  
ORA A.

ii) MVI B, 82<sub>H</sub>  
MOV A, B  
MOV C, A  
MVI D, 37<sub>H</sub>  
OUT PORT

v) MVI A, F8<sub>H</sub>  
SUI 69<sub>H</sub>

viii) XRA A  
MVI B, 4A<sub>H</sub>  
SUI 4F<sub>H</sub>  
ANA B.

iii) MVI A, F2<sub>H</sub>  
MVI B, 7A<sub>H</sub>  
ADD B  
OUT PORT.

vi) SUB A  
MOV B, A  
DCR B  
INR B  
SUI 01<sub>H</sub>

X  
Y  
0  
0  
0  
1  
1  
0  
1  
0

27. Consider the execution of the following two programs. Is there any difference?

i) MVI A, FF<sub>H</sub>  
ADI 01<sub>H</sub>

ii) MVI A, FF<sub>H</sub>  
INR A.

28. What happens in a microcomputer when the power is turned on and the reset key is pushed?

29. What is monitor program?

30. How does the microprocessor differentiate among positive number, negative number and bit pattern?

31. How jump instructions (JMP, JC, ...) are executed in 8085?

32. What is the purpose of the following instructions?

ADD A, SUB A, XRA A, ANI 00H, XRJL FFH;

33. What is the output of the following instructions (program) ?

i) MVI A, 8FH

ADI 72H

JC DISPLAY

OUT PORT

HLT

DISPLAY: XRA A

OUT PORT

HLT

ii) MVI A, BYTE

MOV B,A

SUI 50H

JC DELETE

MOV A,B

SUI 80H

JC DISPLAY

DELETE: XRA A

OUT PORT

HLT

DISPLAY: MOVA,B

OUT PORT

HLT

34. Specify the ~~size~~ function of the following programs. What is the purpose of ORA instruction in these programs.

i) MVI A, BYTE

ORA A

JP OUTPORT

XRA A

OUTPORT: OUT F2H

HLT

ii) MVI A, BYTE

ORA A

JM OUTPORT

OUT 01H

HLT

OUTPORT: CMA

ADI 01H

OUT 01H

HLT

35. Describe the function and draw the timing diagram of the following instructions.

LXI R, 16-bit ; MOV R,M ; LDAX B/D ; STAX B/D ;

LDA 16 bit; STA 16 bit; MVI M, 8 bit ; ADD M ; INR M ;

RLC ; RAL ; RRC ; RAR ; CMP R ; CMP M ; CPI 8-bit data.

36. What is the purpose of the following programs. What is the requirement of ORA?

i) STC

CMC

RAR

ii) STC

CMC

RAL

iii) ORA A

RAR

iv) ORA A

RAL

37. Specify the register contents as each of the following instructions being executed.

i) MVI C, FFH

LXI H, 2070H

LXI D, 2070H

MOV M,C

LDAX D

...

ii) LXI H, 2090

SUB A

MVI D, OFH

LOOP: MOV M,A

INX H

DCR D

JNZ LOOP

iii) LXI H, 2055H

MVI M, 8AH

MVI A, 76H

ADD M

STA 2055H

[Specify the content at memory 2055]

- i) LXI H, 2065H      v) MVI A, B7H      vi) MVI A, B7H  
 MVI M, FFH      ORA A      ORA A  
 INRM      RLC      RAL
- [specify content at 2065]
- vii) MVI A, 80H      viii) MVI A, C5H      ix) MVI A, A7H  
 ORA A      ORA A      ORA A  
 RAR      RAL      RAR  
 RRC.
- x) MVI A, FFH      xi) LXI H, 2070H      xii) MVI A, 78H  
 ORA A      MVI M, 64H      RRC  
 CPI A2H      MVI A, 8FH      RRC.  
 CMP M,

38. Explain the mathematical function performed by the following program.

```
MVI A, 07H
RLC
MOV B,A
RLC
RLC
ADD B
```

39. How many times the following loops are executed?

i) LXI B, 0007H LOOP: DCX B JNZ LOOP	ii) LXI B, 0007H LOOP: DCX B MOV A,B ORA C JNZ LOOP
--	---

40. The following programs are intended to clear ten memory locations starting from  $0009H$  to  $0000H$ . What will be the effect of the program.

```
LXI H, 0009
LOOP: MVI M, 00H
DCX H
JNZ LOOP
```

41. Find the maximum delay using i) single register ii) Register pair for a MPU with 2MHz clock.

42. Calculate the delay in the following programs with 2MHz clock.

i) LXI B, 12FFH LOOP: DCX B XTHL XTHL NOP NOP MOV A,C ORA B JNZ LOOP	ii) MVI A, 17H LOOP: ORA A RRC JNC LOOP	iii) MVI A, 17H LOOP: ORA A RAL JNC LOOP
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iv) MVI A, 17H  
LOOP: ORAL  
ORA A  
JNC LOOP

43. calculate the COUNT to obtain a 100 $\mu$ s loop delay and express the value in Hex. (Assume clock frequency 2MHz).

i) MVI B, COUNT  
LOOP: NOP  
NOP  
DCR B  
JNZ LOOP

ii) MVI B, 14H  
LOOP2: LXI D, COUNT  
LOOP1: DCX D  
MOV A,D  
ORA E  
JNZ LOOP1  
DCR B  
JNZ LOOP2

44. What are the task of PUSH and POP operations of 8085. Describe with example.

45. Write a program to reset all flag bits.

46. How CALL and RET instructions are executed in 8085. Discuss with example.

47. What do you mean by conditional call and return? What is nesting of subroutine?

48. Explain the function of the following routines.

i) LXI SP, 209FH  
MVI C, 00H  
PUSH B  
POP PSW  
RET

ii) LXI SP, 209FH  
PUSH B  
PUSH D  
POP B  
POP D  
RET.

49. Read the following program and answer the questions:

2000: LXI SP, 2100H  
LXI B, 0000H  
PUSH B  
PUSH PSW  
LXI H, 2003H  
CALL 2064H  
OUT 01H

2010: HLT.

DELAY: 2064 PUSH H  
PUSH B  
LXI B, 80FFH  
LOOP: DCX B  
MOV A,B  
ORAC  
JNZ LOOP  
POP B  
RET.

i) What is the status of the flags and content of accumulator after the execution of POP instruction located at 2007H?

ii) Specify the stack locations and their contents after execution of CALL instruction.

iii) What are the content of SP and PC after execution of CALL instruction?

iv) Specify the memory location where the program returns after the subroutine.

(3)

50. What are the functions of the following instructions :  
 LHLD 16-bit ; SHLD 16-bit ; XCHG ; XTHL ; SPHL ; PCHL ; ADC R ;  
 ACI 8-bit ; ADC M ; SBB R ; SBS M ; SBI 8-bit ; DAA ; DAD.
51. What is the task of EI and DI instruction in 8085 ?
52. What do you mean by interrupt ? What is Interrupt Service Routine (ISR) ?  
 What are the steps followed by 8085 when an interrupt occurs in  
 INTR line ?
53. Draw the timing diagram of RST n instruction.
54. Is there a minimum pulse width required for INTR signal ?
55. How long can be the interrupt INTR pulse stay high ?
56. Can the microprocessor be interrupted again before the completion of  
 first interrupt service routine ?
57. What do you mean by S/W, H/W, maskable, non-maskable, vectored and  
 scalar interrupt ? Give examples.
58. Show the priority, clock sensitivity, masking property, and vector  
 location of different interrupt available in 8085.
59. Write short note on : RIM and SIM.
60. Write code to enable all interrupts in 8085.
61. Assume that 8085 is completing RST 7.5 interrupt request. Check  
 if RST 6.5 is pending or not. If it is pending, enable RST 6.5 without  
 affecting any other interrupts; Otherwise return to main program.  
 Write a subroutine to do the above.
62. What do you mean by DMA ? What happens when HOLD & INTR line  
 goes high simultaneously ?
63. How can you interface a keyboard with 8085 MPU ? What do you  
 mean by key bounce ? How can it be solved ?
64. How can you interface LED and SSD with 8085 MPU ?
65. What are the major differences among 8085 and 8086 MPU ?
66. Describe the register set of 8086 MPU.
67. What are the addressing modes supported by 8086 MPU ?
68. What is the purpose of MN/MX pin in 8086 ?
69. What is the basic difference between 8086 and 8088 MPU ?
70. Write a short note on 8086 MPU.