

Digital Electronics

1. What do you mean by Half adder and Full Adder? What are the differences between these?
2. Draw the truth table of H/A and implement using logic gates.
3. Implement H/A using minimum number of NAND gates (5 gates).
4. Draw the truth table of F/A and implement using logic gates.
5. Implement F/A using minimum number of NAND gates (9 gates only).
6. Implement F/A using H/A(s) and other necessary logic gates.
7. What do you mean by Full-Subtractor and Half-subtractor? How they differ?
8. Draw the truth table of H/S & F/S and implement using logic gates.
9. Draw the circuit diagrams of H/S and F/S using minimum number of NAND gates.
10. Implement F/S with two H/S and an OR gate.
11. What is binary parallel adder? Design a n-bit parallel adder. What is its complexity?
12. What do you mean by CLA? How it differs from parallel adder?
13. Design a 4-bit Carry Look-ahead Adder.
14. Design a BCD adder and discuss its operation.
15. What is the requirement of code conversion circuit? Design a BCD to excess 3 code converter.
16. Design a combinational circuit converts
 - i) 8,4,-2,-1 code to BCD
 - ii) 2,4,2,1 code to 8,4,-2,-1 code.
 - iii) binary to gray code.
 - iv) gray code to binary code.
17. Show how a F/A can be converted to a F/S with addition of one inverter circuit.
18. Design an BCD to -excess 3 code converter using 4-bit Full-adder.
19. Design an adder-subtractor circuit using 4-bit parallel adder?
20. Design an excess 3 to BCD code converters using 4-bit parallel adder.
21. Design an combinational circuit to implement magnitude comparator.
22. Design a circuit using magnitude comparators & other gates to detect a number x is satisfying the condition $10 \leq x \leq 15$.
23. Design a circuit to add 16-bit numbers using 4-bit parallel adders.
24. Design a serial adder that add two numbers of infinite length.
25. What are the differences between Parallel & serial adder.

26. What is decoder? Why decoder is called as minterm generator?
27. Design a 2×4 and 3×8 Decoder with enable line using i) basic gates and ii) Universal gates.
28. Design a BCD to decimal decoder with minimum number of gates.
29. Implement a F/A using decoder and two OR gates.
30. Design a 4×16 decoder with two 3×8 decoder with enable line.
31. Design a BCD to excess 3 code converter with BCD to decimal decoder.
32. A combinational circuit is defined by the following three functions:
- $$F_1 = x'y' + xy'z'$$
- $$F_2 = z' + y$$
- $$F_3 = x'y + x'y'$$
- Design the circuit with a decoder and external gates.
33. Design a 2×4 Decoder with active low output and active low enable line. Implement the combinational circuit defined by the following two functions by means of the decoder and NAND gates.

$$F_2(x,y) = \sum(1,2,3)$$

$$F_1(x,y) = \sum(0,3)$$

34. Construct a 5×32 decoder with four 3×8 decoder chip with enable line and a 2×4 decoder.
35. Draw the logic diagram of a 2×4 decoder with enable line using NOR gate only.
36. "A decoder with enable input can be considered as demultiplexers" - discuss.
37. Design a 2×4 Decoder / demultiplexer circuit.
38. What is encoder? Design an octal to binary encoder? What are the disadvantages of encoders? How priority encoder removes the disadvantages? Design a 4×2 priority encoder circuit.
39. What is multiplexer? Design a 4×1 MUX. "MUX is also called data selector" - discuss.
40. Design a quad 2×1 MUX.
41. Implement the function $F(A,B,C) = \sum(1,3,5,6)$ using 8×1 , 4×1 and 2×1 MUX.
42. Implement the function $F(A,B,C,D) = \sum(0,3,1,4,8,9,15)$ using MUX.
43. Design a 4×1 MUX with 2×1 MUX(s).
44. Show that MUX is functionally complete.
45. Implement F/A using MUX.
46. Implement a 4×2 priority encoder. Include an output E to indicate that at least one input is a 1.
47. Design 4×16 decoder using 2×4 decoder circuits only.

48. Implement $F_1(A_1, A_0) = \sum(1, 2, 3)$ & $F_2(A_1, A_0) = \sum(0, 2)$ using ROM.

49. Design a combinational circuit using a ROM. The circuit accepts a 3 bit number and generates a output equal to square of input.

50. What is PLA? How it differs from ROM. Implement $F_1 = AB' + AC$ & $F_2 = AC + BC$ using PLA.

51. Implement the following function with a PLA having three inputs, four product terms and two outputs.

$$F_1(A, B, C) = \sum(3, 5, 6, 7) \quad F_2(A, B, C) = \sum(0, 2, 4, 7)$$

52. Derive the PLA for a combinational circuit that squares a 3-bit number.

53. Design a PLA for the BCD to excess 3 code converter.

54. Design a PLA to convert 4-bit binary number to its corresponding gray code.

55. Design a ROM to perform BCD to excess-3 conversion.

56. Write the differences between sequential & combinational circuit?

57. What is flip flop? Design S-R latch using NAND gates and explain its operation. Do the same using NOR gates only.

58. Design a clocked R-S flip flop and explain its operation.

59. What is the disadvantages of S-R latch? How D-flip flop overcomes it? Draw a logic diagram of D-latch using NAND gates.

60. Is there any disadvantage of D-latch? How J-K latch overcomes it? Draw the truth table and logic diagram of J-K latch.

61. What is racing 1 in J-K flip flop? How it can be solved?

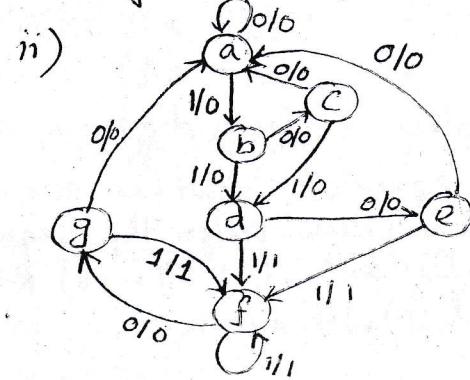
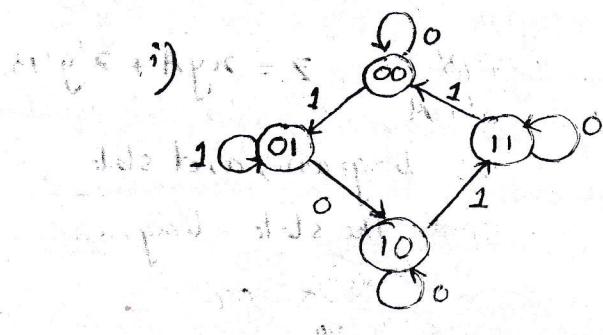
62. Draw the truth table, characteristic equation & logic diagram of T/F/F.

63. What do you mean by positive & negative edge trigger flip flop?

64. What is master-slave F/F? What is its advantage? Draw a master-slave F/F using NAND gates only & explain its operation.

65. Write steps to convert an latch 1 to latch 2. Hence convert SR latch to D, JK to T, SR to JK.

66. Draw sequential circuit whose state diagrams are given below:



67. Design a sequential circuit using J-K flip-flops to satisfy the following state equations:

$$\begin{aligned} i) \quad A(t+1) &= C \oplus D \\ B(t+1) &= A \\ C(t+1) &= B \\ D(t+1) &= C. \end{aligned}$$

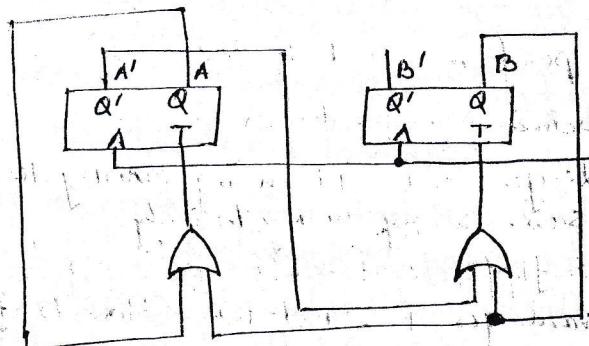
$$\begin{aligned} ii) \quad A(t+1) &= A'B'CD + A'B'C + Aed + AC'D' \\ B(t+1) &= A'C + CD' + A'BC' \\ C(t+1) &= B \\ D(t+1) &= D. \end{aligned}$$

68. Do the same of Q67 using D flip-flops.

69. consider a JK' flip flop, i.e., a J-K flip flop with an inverter between external input K' and internal input K.

- i) Obtain the characteristic table.
- ii) Obtain the characteristic equation.
- iii) Show that tying the two external inputs together forms a D F/F.

70. Derive the state table and state diagram of the sequential circuit:



71. A sequential circuit has four F/F's A, B, C, D and an input α . It is described by the following state equations:

$$A(t+1) = (CD' + C'D)\alpha + (CD + C'D')\alpha'$$

$$B(t+1) = A$$

$$C(t+1) = B$$

$$D(t+1) = C$$

a) Obtain the sequence of states when $\alpha = 1$, starting from $ABCD = 0001$.

b) Obtain the same when $\alpha = 0$ and $ABCD = 0000$.

72. A sequential circuit has two F/Fs (A & B), two inputs (x & y) and an output (z). The flip-flop input functions and the circuit output functions are as follows:

$$J_A = xB + y'B'$$

$$J_B = xA'$$

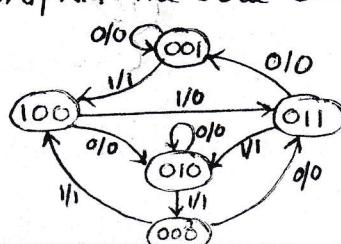
$$J_K = xy'B'$$

$$K_B = xy' + A$$

$$z = xyA' + x'y'B.$$

Obtain the logic diagram, state table, state diagram, and state equation.

73. A sequential circuit has one input & one output. The state diagram is shown below. Design the sequential circuit with (i) T F/Fs (ii) R-S F/Fs and (iii) J-K F/Fs.



74. Design the sequential circuit described by the following state equations.

Use J-K FFs.

$$A(t+1) = \bar{x}AB + \bar{y}A'c + xy$$

$$B(t+1) = \bar{x}AC + \bar{y}BC'$$

$$C(t+1) = \bar{x}'B + \bar{y}AB'$$

75. Design a 4-bit register with parallel load using (i) SR FFs (ii) D-FFs, and describe the working principle.

76. Draw a bidirectional shift register and describe its operation. Give Timing diagram for illustration.

77. What is universal shift register? Draw a circuit for 4 bit universal shift register.

78. Draw the diagram of a 4-bit ripple (a) UP (b) DOWN and (c) UP/DOWN counter and explain its operation.

79. Design asynchronous (a) mod-6 (b) Mod- 7 and (c) Decade counter. Illustrate with help of timing-diagram.

80. Show the synchronous 4-bit (a) UP (b) DOWN & (c) UPDOWN counter and explain its operation.

81. Design a synchronous mod-6 counter and explain its operation.

82. Design synchronous counter to count

(a) 0, 2, 4, 6, 0, 2, 4, ... // EVEN COUNTER

(b) 2, 3, 5, 7, 11, 13, 2, 3, 5, ... // ~~PRIME~~ COUNTER PRIME.

(c) 0, 1, 2, 3, 2, 1, 0, 1, ...

83. The output of a J-K flipflop is given by $Q(q, J, K) = Jq \square Kq$. This means if $q=0$ then $J=Q$ and $K=\phi$. If $q=1$ then $J=\phi$ and ~~K=Q~~ $K=Q$. draw the characteristic table & excitation table of J-K flipflop. Hence draw a synchronous decade counter.

84. The output of a T F/F is given by $Q(q, T) = Tq \oplus Tq$. This means if $q=Q$ then $T=0$ and if $q=Q'$ then $T=1$. draw the characteristic table of the T F/F.

85. Four J-K flipflops are connected in the following manner:

$$J_0 = K_0 = 1, J_1 = q_0 q_3, K_1 = q_0, J_2 = K_2 = q_0 q_1, J_3 = q_0 q_1 q_2, K_3 = q_0.$$

construct the state table and determine the functionality of the given circuit.

86. Design a 4-bit weighted register D-A converters and state its drawbacks.

87. Design a 4-bit R-2R ladder converter for D/A conversion and explain its operation. What do you mean by resolution.

88. Explain counter method for A/D conversion. state the drawbacks of this method.
89. Explain the operation of a 4-bit successive-approximation A/D converter.
90. Design a sequence generator to generate the sequence 110100110100.
91. Define rise-time, setup time, hold time, propagation delay time and duty cycle.
92. Distinguish between SSI, MSI, LSI, VLSI and ULSI.
93. Realize AND and OR gate using diodes.
94. Realize NOT gate using transistor.
95. Draw DTL NAND gate and explain its operation.
96. Draw RTL NOR gate and explain its operation.
97. Draw TTL NAND gate with totem-pole outputs.
98. Draw TTL NAND gate with open-collector output. What is its advantage?
99. Define fan in and fan out.
100. Explain the working principle of seven segment display.