REV

POWER DAUGHTER BOARD (DTR)

HIERARCHY VIEW

ENABLE LOOPS CAN TRANSCEIVER LOOP VOLTAGE MONITOR PG. 3

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5	DSP_CORE	J2, J3
6	IN_COND	
7	POWER	J4
8	X_PORTS	

CONNECTOR KEYING TABLE

Jx	TYPE	KEY
J1	HEADER 5X2	NA
J2	HEADER 7X2	NA
J3	HEADER 4X1	NA
J4	HEADER 2X1	NA
P6	HEADER 20X2	NA
P8	HEADER 15X2	NA
P35	HEADER 20X2	NA

SCHEMATIC DESIGN NOTES

- 1. ALL RESISTANCE VALUES ARE IN OHMS
- 2. PARTIAL REF DES ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. & SUBASSY DESIGNATION.
- 3. TERMINAL NO. ARE SHOWN FOR REFERENCE ONLY & MAY NOT APPEAR ON THE COMPONENT.

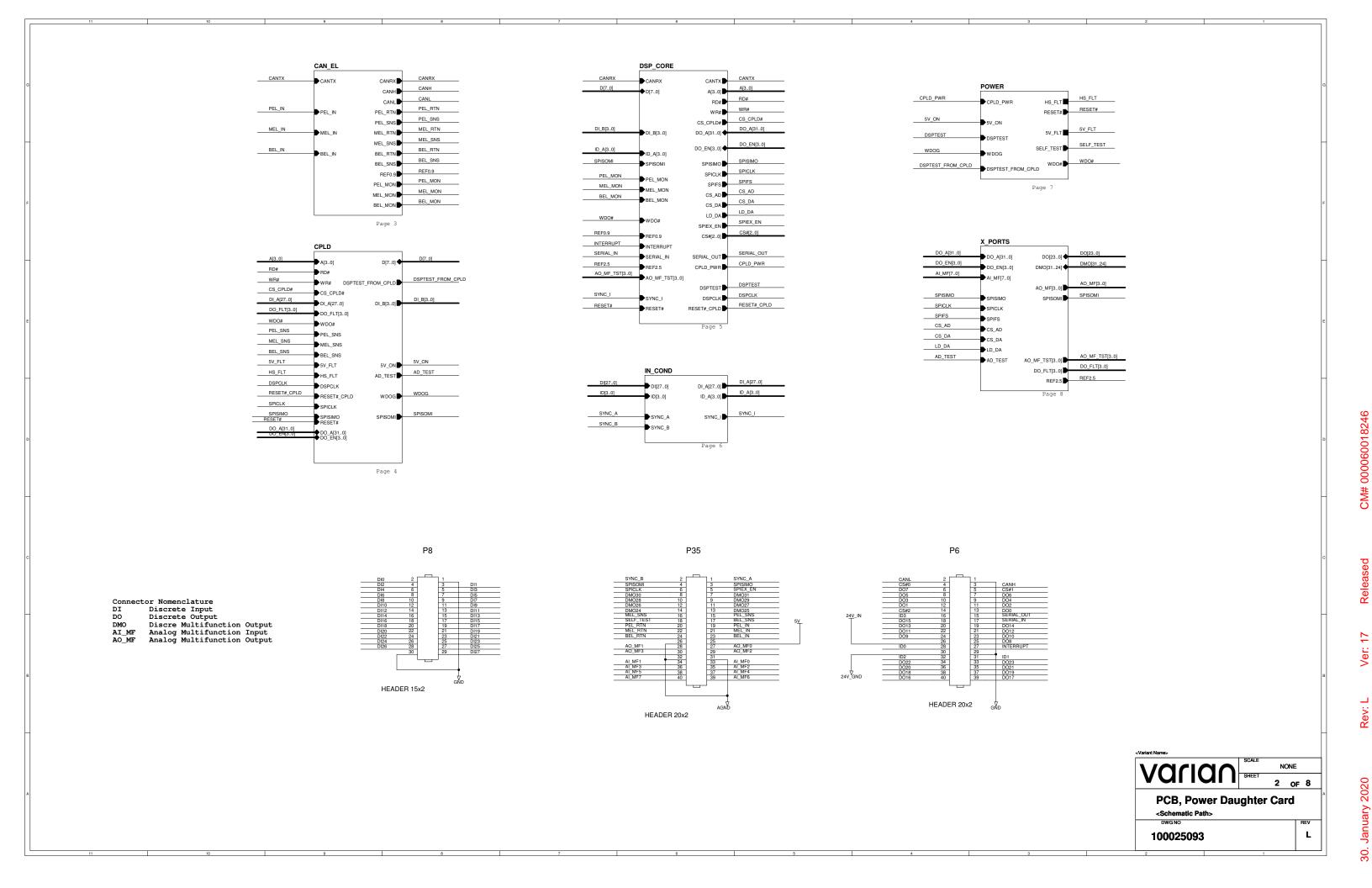
	Actel Hardwired FPGA PG. 4
	DSP CORE EEPROM , SRAM TEMPERATURE SENSING PG. 5
	DISCRETE INPUTS IDENTIFICATION INPUTS PG.6
	POWER RESET, WATCHDOG SELF TEST PG. 7
	DISCRETE OUTPUTS ANALOG MULTIFUNCTION OUTPUTS ANALOG MULTIFUNCTION INPUTS PG. 8

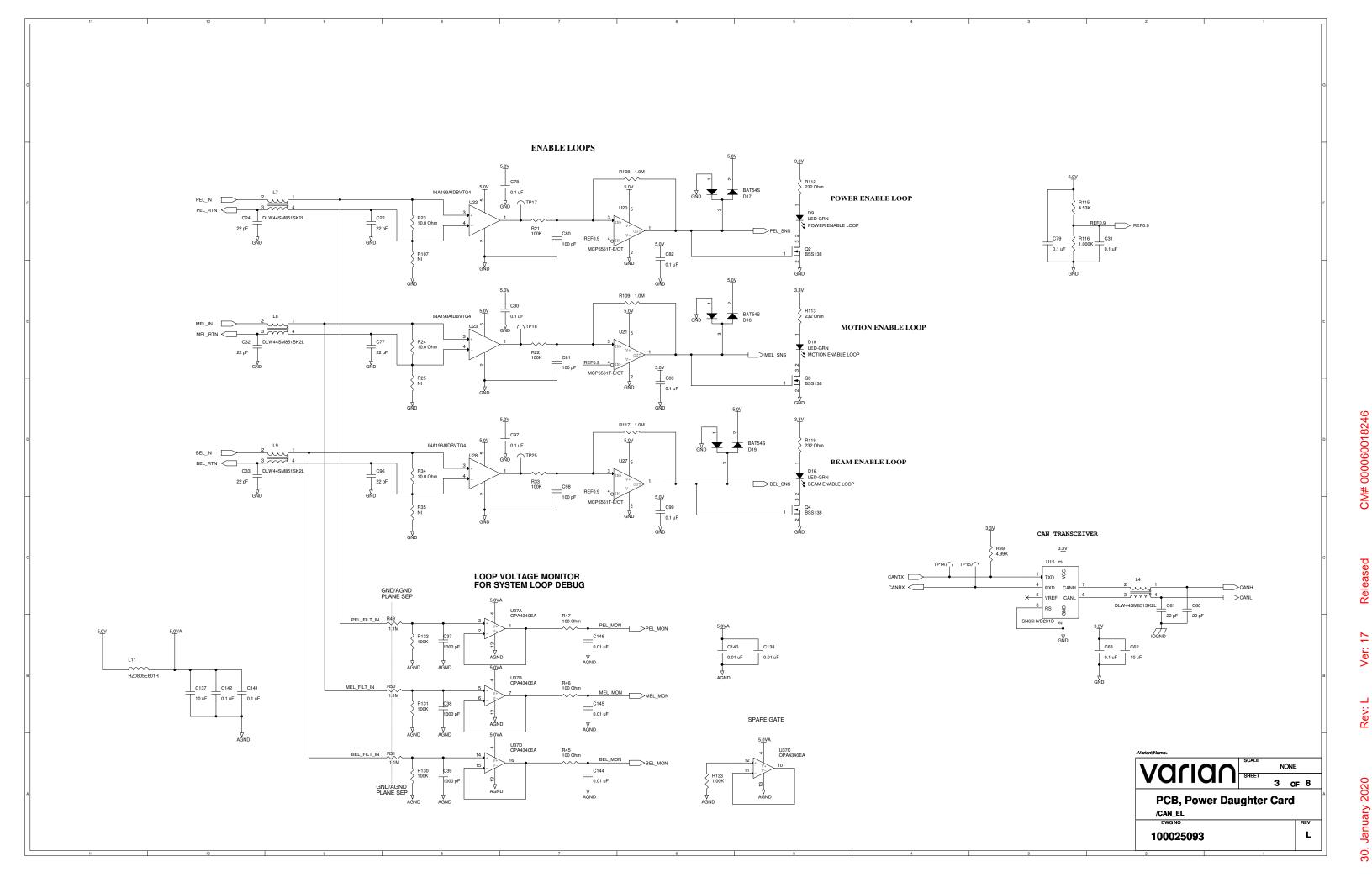
COVER_PAGE PG. 1

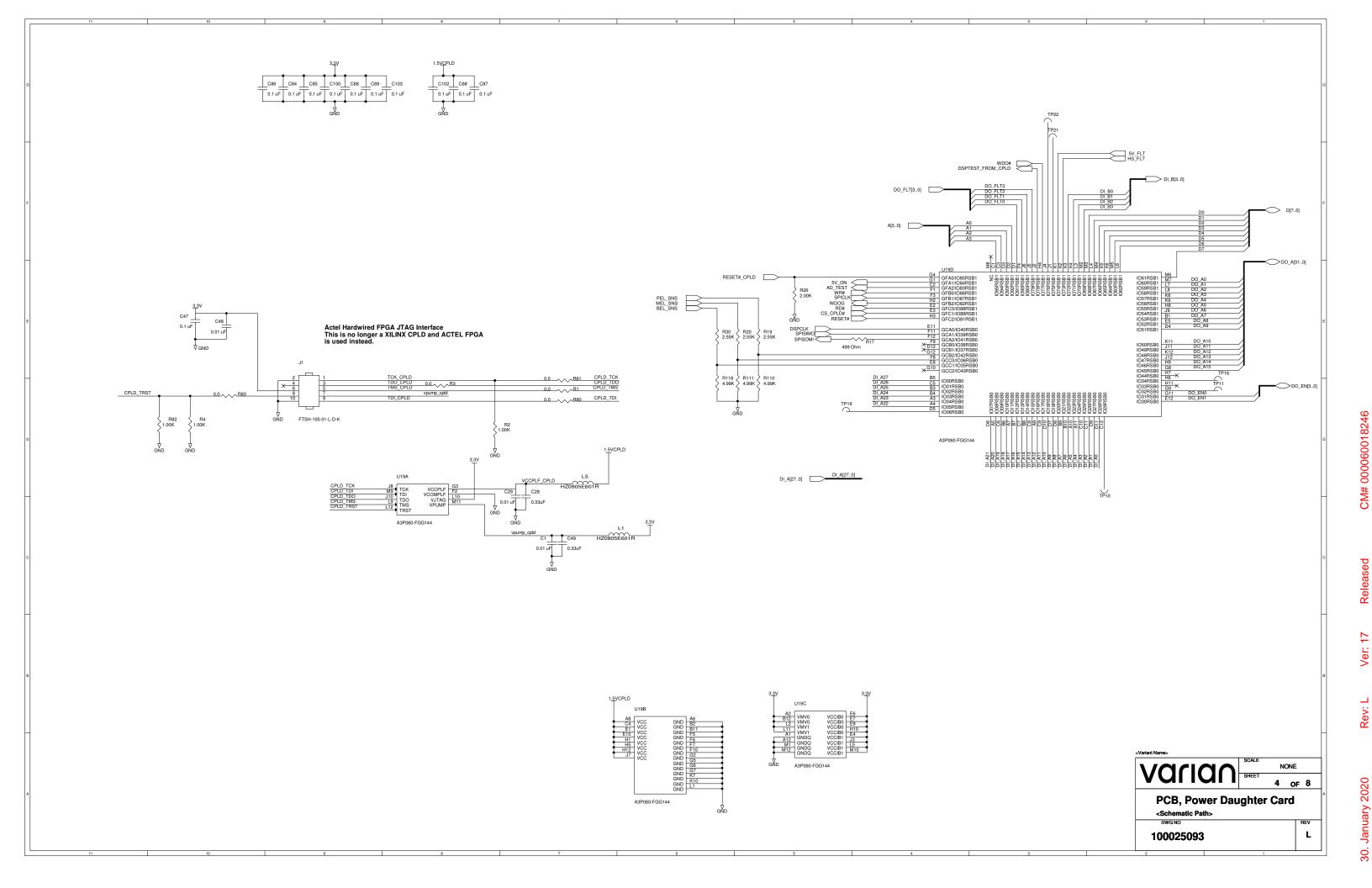
<variant name=""></variant>												
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ECO	200106967	1077190	200107333	200106022	1075743	DATE: 1/29/09	1000					

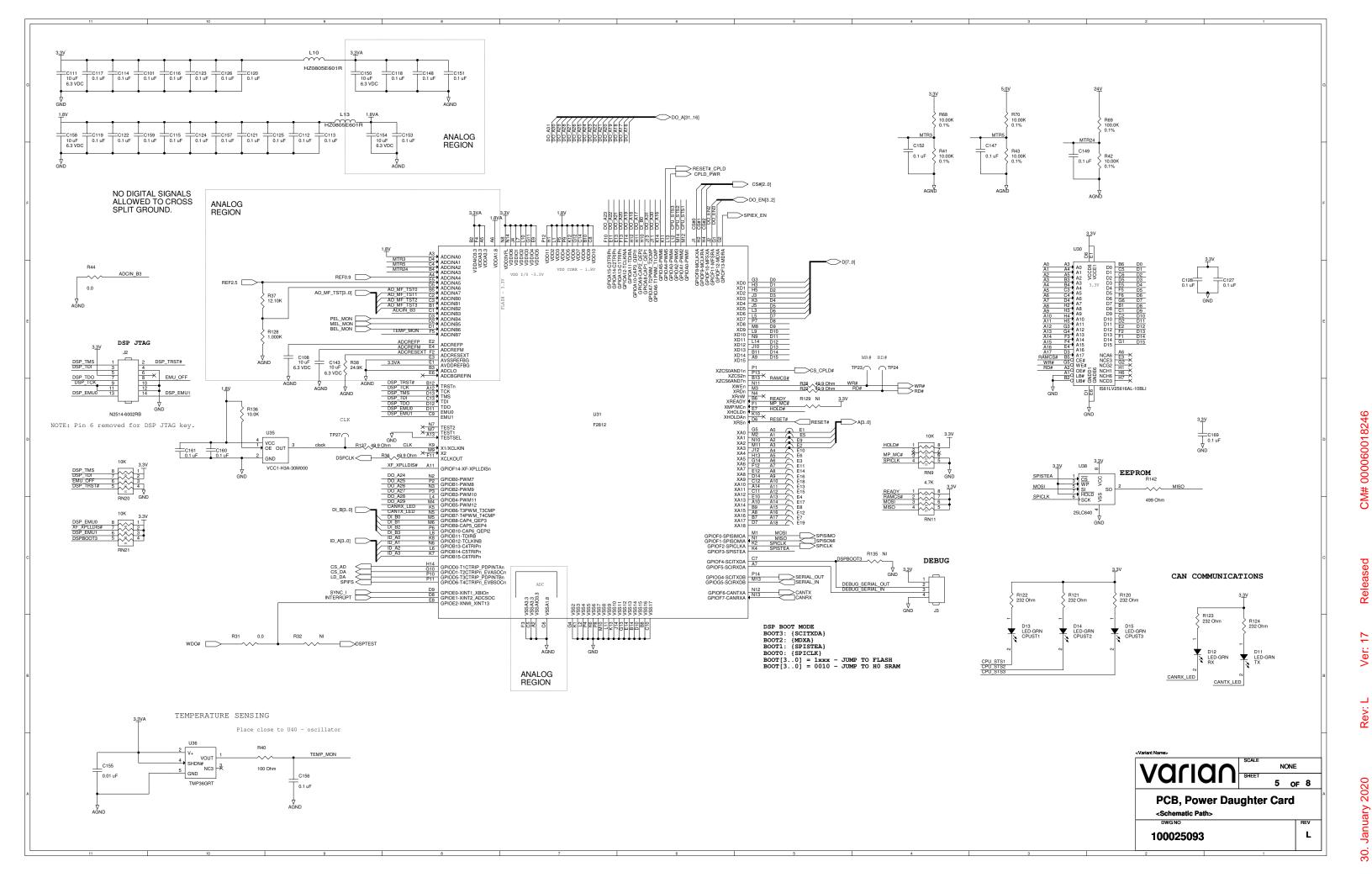
ORCAD CAPTURE SIZE

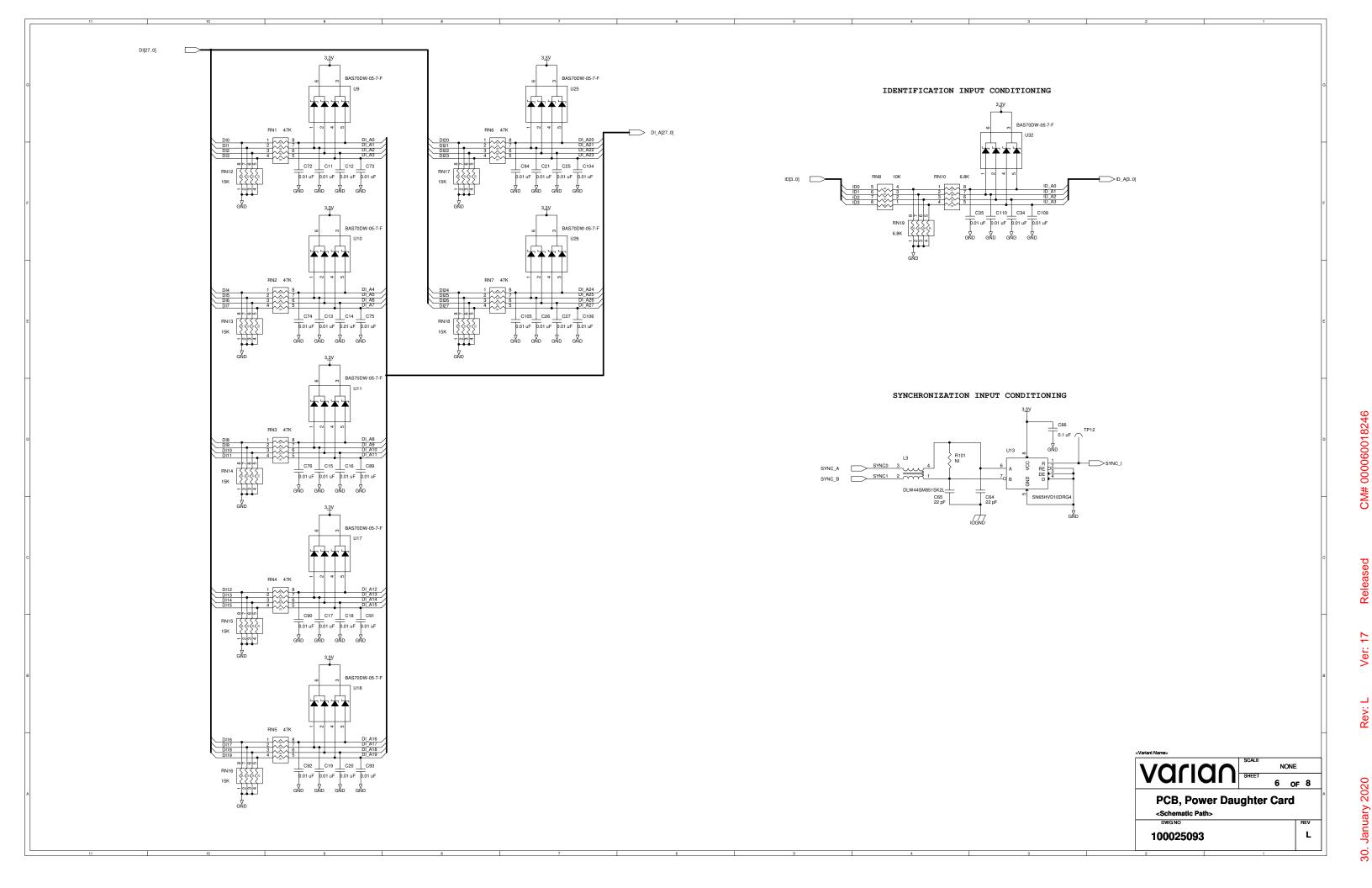
DWG NO

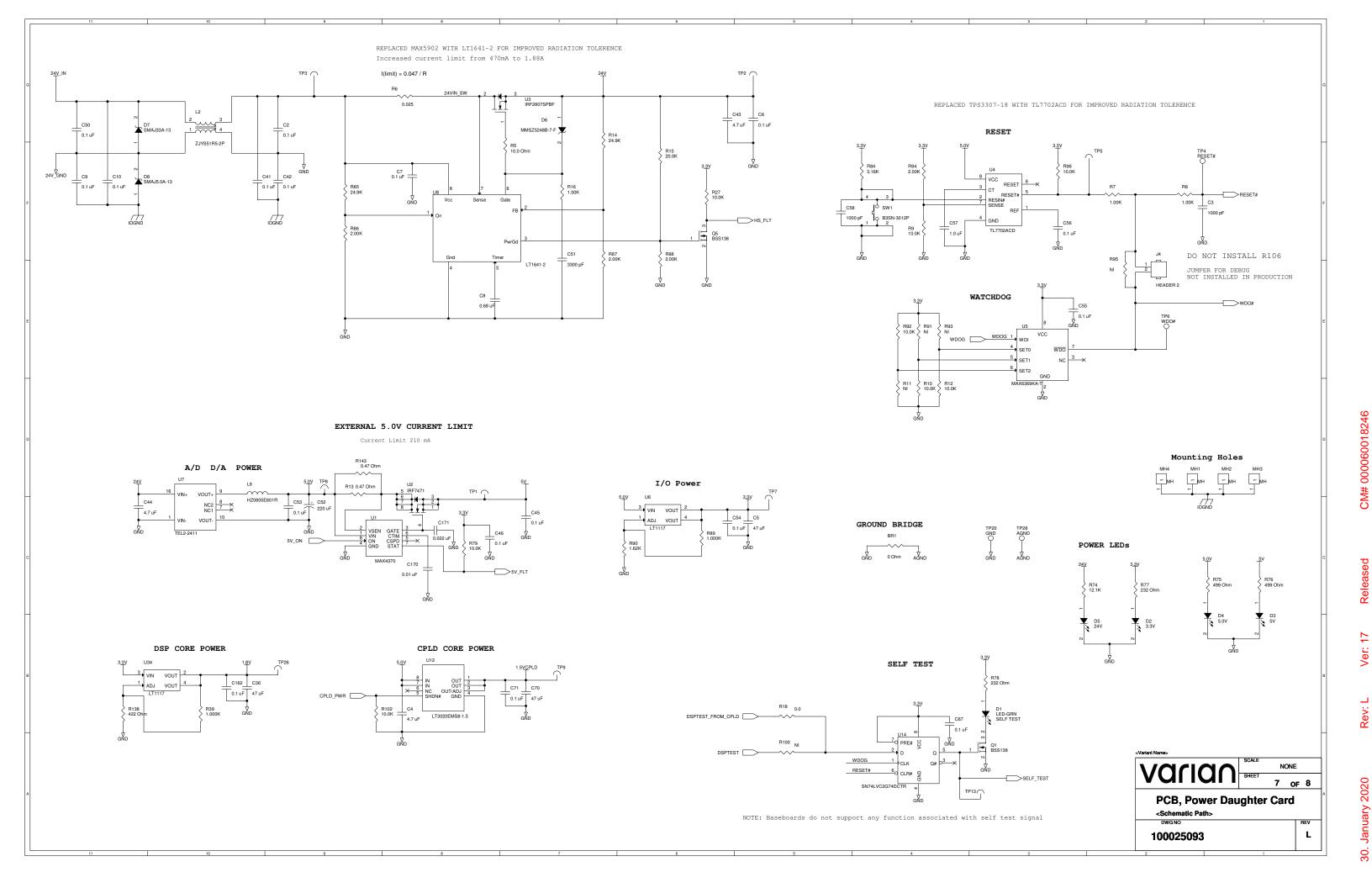


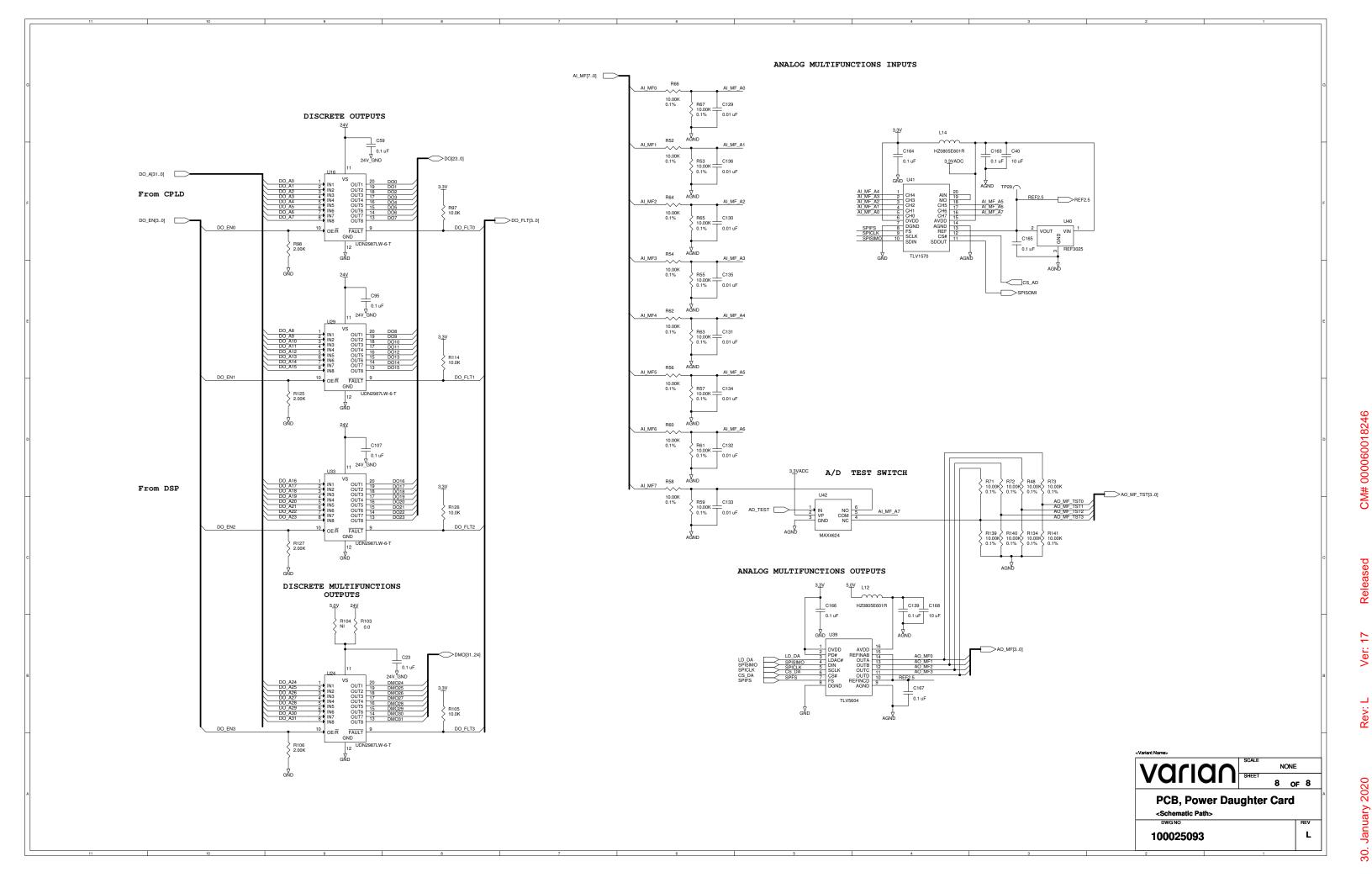












Signature File



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Description: PCB, POWER DAUGHTER CARD, SCHEMATIC

Change Master Number: 60018246 ECN Number: 200107333

ECN Description:

Signature list

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20, January 2020	21:37:28	Jing Xie	Approved
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