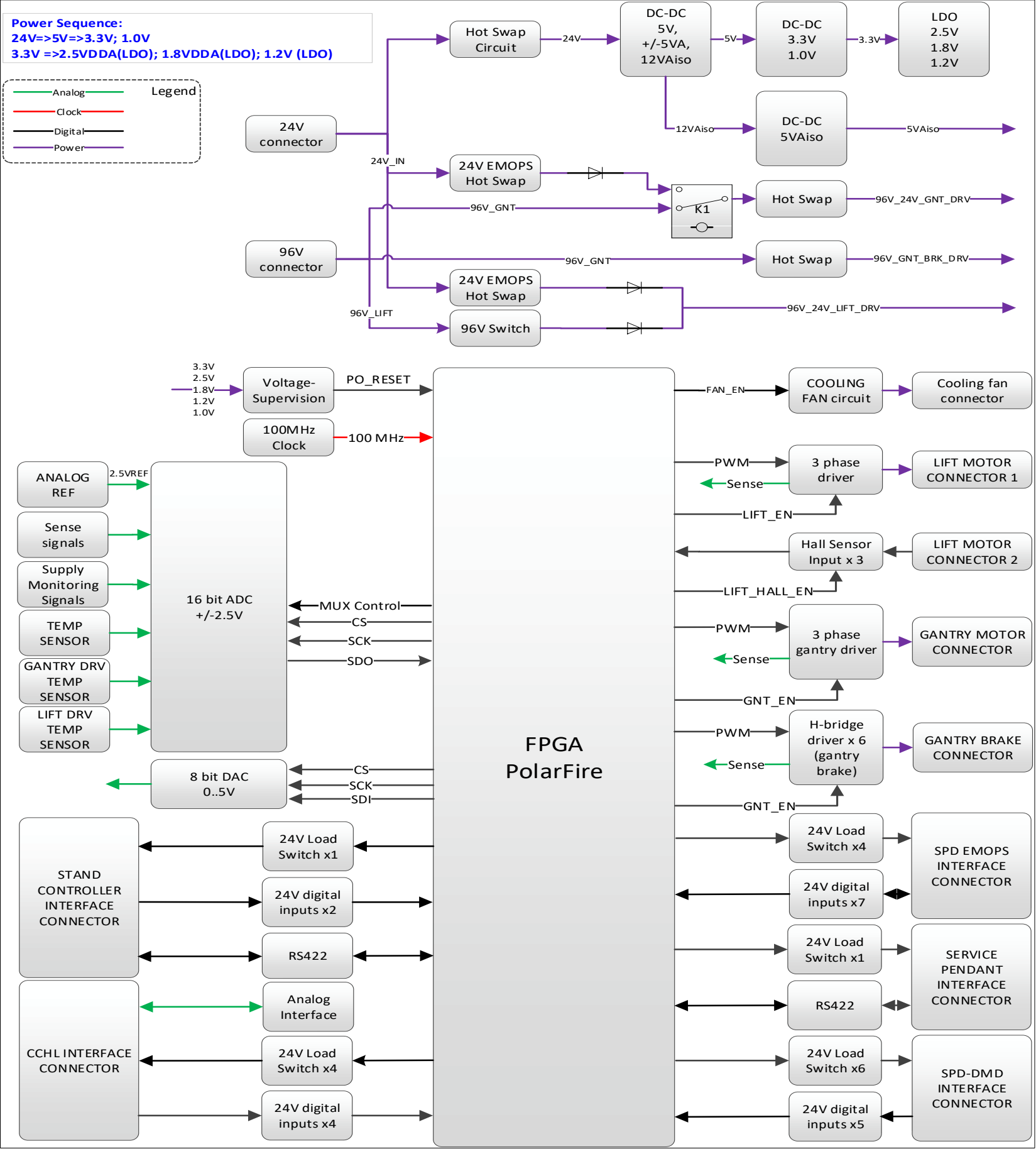


DUAL MOTOR DRIVER



NOTES:

1. RESISTANCE VALUES ARE IN OHMS
2. CAPACITANCE VALUES ARE IN MICROFARADS

REFERENCE INFORMATION

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CONNECTOR KEYING TABLE

Jx	TYPE	FUNCTION	KEY
J1	HEADER 13x2 RIBBON	STAND CONTROLLER	8
J6	HEADER 4x2	LIFT HALL SENSOR	NA
J7	HEADER 2x1	COOLING FAN	NA
J8	DSUB 15-R	STAND CONTROL PANEL	2
J9	HEADER 10x2	DMD_24V, SPD DMD IF	18
J10	HEADER 13x2 RIBBON	STAND POWER DISTRIBUTION	11
J11	FTSH-105-01-L-D-K	FPGA JTAG	NA
J12	DSUB 26 HD RECEPTACLE	COUCH CONTROLLER	NA
J17	HEADER 2X3	GANTRY/LIFT 96V INPUT POWER	NA
J18	HEADER 4X1	EMOPS 24V	NA
J19	HEADER 5x2	TEST POINT HEADER	NA
J20	HEADER 5x2	TEST POINT HEADER	NA
J21	HEADER 10x2	TEST POINT / SWITCH HEADER	NA
J22	HEADER 4X1	GANTRY DRIVER OUTPUT	TBD
J23	HEADER 4X1	LIFT DRIVER OUTPUT	3
J24	DSUB 26 HD RECEPTACLE	GANTRY BRAKE	NA

VARIANT01

THIS DOCUMENT CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF VARIAN MEDICAL SYSTEMS. REPRODUCTION, DISCLOSURE, OR RELEASE TO OTHERS, MANUALLY OR ELECTRONICALLY, WITHOUT THE PRIOR WRITTEN CONSENT OF VARIAN MEDICAL SYSTEMS IS STRICTLY PROHIBITED.			THE ELECTRONIC SIGNATURE RECORD WILL BE APPENDED TO THE LAST PAGE OF THE SECURED DOCUMENT			
DESCRIPTION OF CHANGE	INITIAL RELEASE	<div>-CHANGED TO 7890970571 (CURRENT SENSOR; HE, 40A, 8-SOIC, ROHS - ALLEGRO MICROSYSTEMS INC ACS723LLCTR-40AU-T); U34 -CHANGED TO 4180200371 (CAP, 1000PF, 10%, 50V, 0805, ROHS - AVX/KYOCERA 08055C102KAT2A); C234 C263 C264 C265 C266 C340 C341 -CHANGED TO 4180200171 (CAP, 0.1UF, 10%, 50V, 0805, ROHS - AVX/KYOCERA 08055C104KAT2A); C82 C125 C226 R621 -CHANGED TO 3141621371 (RES, 1000, 1%, 1/10W, 0603, ROHS - KOA SPEER RK73H1JTTD1001F); R621 -ADDED/CHANGED TO 3141630971 (RES, 10.0K, 1%, 1/10W, 0603, ROHS - KOA SPEER RK73H1JTTD1002F); R428 R24 R273 R354 R1000 (ADDED THROUGH REWORK) -CHANGED TO 3141633871 (RES, 20.0K, 1%, 1/10W, 0603, ROHS - KOA SPEER RK73H1JTTD2002F); R351 -CHANGED TO 3141627171 (RES, 4.02K, 1%, 1/10W, 0603, ROHS - KOA SPEER RK73H1JTTD4021F); R63 R369 R373</div>	varian		TITLE: PCB, DUAL MOTOR DRIVER /	
			DRAWN: Rami A.	SHEET 1 OF 21	D	P1060973
			DATE: 06/22/2023			B
ECO REV	A	B	ORCAD CAPTURE	SIZE	DWG NO	REV

Logic +5V DC/DC

Nominal output voltage (ADC input):
 5V_MON = 4.55V
 5V_A_POS_MON = 4.55V

VAR-MH250R156

IOGND

Mounting Holes (connected to Chassis GND through standoffs)

The schematic shows the power supply circuit starting from a 24V input. A 10µF capacitor (C161) filters the input. The CTRL pin of the U78 regulator is active low and connected to ground via a 50VDC source. The VIN pin is connected to the filtered 24V through a 20.0K resistor (R351). The CTRL pin is connected to the base of a BSS123 transistor (Q48) through a 2.0K resistor (R350). The emitter of Q48 is grounded, and its collector is connected to the VOUT+ pin of the U78 regulator. The U78 regulator's GND CASE pin is connected to ground through a 10.0K resistor (R352). The output of the U78 regulator is connected to the TP123 test point (12V_{iso}). The output is also connected to a 12V_{iso} test point. The output is filtered by a 10µF 25V capacitor (C115) and a 22µF capacitor (C116). The output is connected to the LM4050AEM3-2.5/NOPB precision centaur voltage reference (U58). The LM4050 has a 2.0K resistor (R226) between its 5V_{iso} pin and the 2.5V_{ref_iso} 3.8V output. It also has a 0.1µF capacitor (C381) at the 5V_{iso} pin and a 0.1µF capacitor (C382) at the NC pin. The output of the LM4050 is connected to the TP141, TP140, TP107, TP108, and TP109 test points. The output is also connected to the TP143 and TP144 test points. The output is connected to the TP143 and TP144 test points.

Nominal output voltages
(ADC inputs):

12V ISO MON = 3.89V
5V ISO MON = 2.01V
TEMP = 0.75V

```

Nominal output voltages
(ADC inputs):

12V_ISO_MON = 3.89V
5V_ISO_MON = 2.01V
TEMP = -0.75V

```

Temperature Sensor

Nominal output voltage (ADC input):
TEMP = 0.75V

The diagram shows a temperature sensor circuit. A 5V supply is connected to a 10.0K resistor (R271) and a 0.1 uF capacitor (C59). The resistor is connected to the V+ pin of the TMP36GRT (U70). The capacitor is connected to the SHDN# pin (pin 4) of the TMP36GRT. The GND pin (pin 5) of the TMP36GRT is connected to AGND. The VOUT pin (pin 1) of the TMP36GRT is connected to a 10.0K resistor (R273) and a 0.1 uF capacitor (C125). The output of the divider is connected to the TP131 TEMP pin, which is labeled TEMP 17 and is also connected to AGND.

varian	SCALE	NONE
	SHEET	2 OF 21
DUAL MOTOR DRIVER		
DWG NO		REV
P1060973		B

HIGH CURRENT 40A
FROM J17

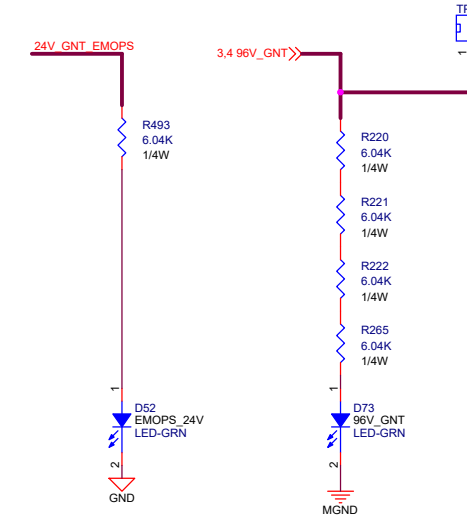
GANTRY EMOPS

HIGH CURRENT 15A

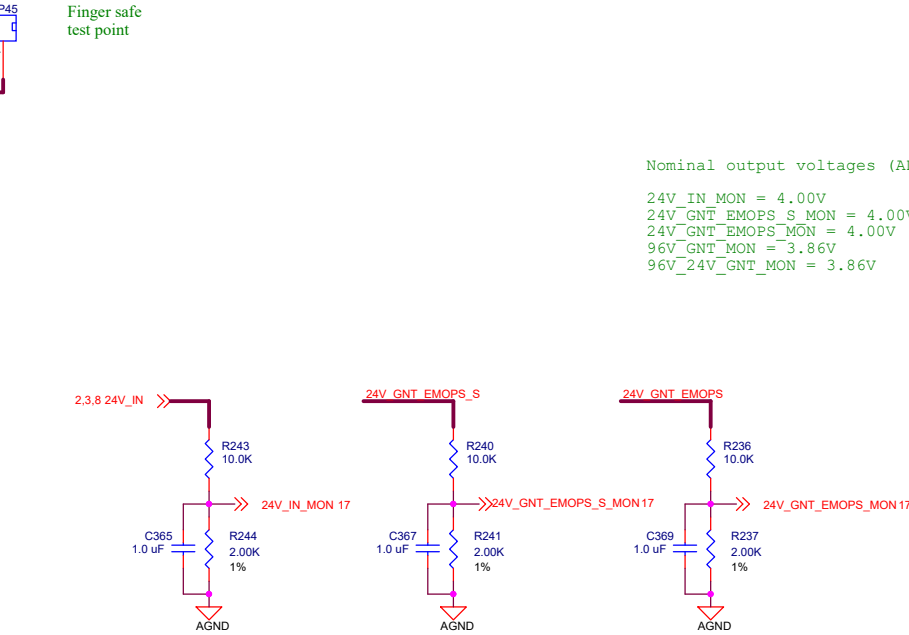
HIGH CURRENT 40A

HIGH CURRENT 20A

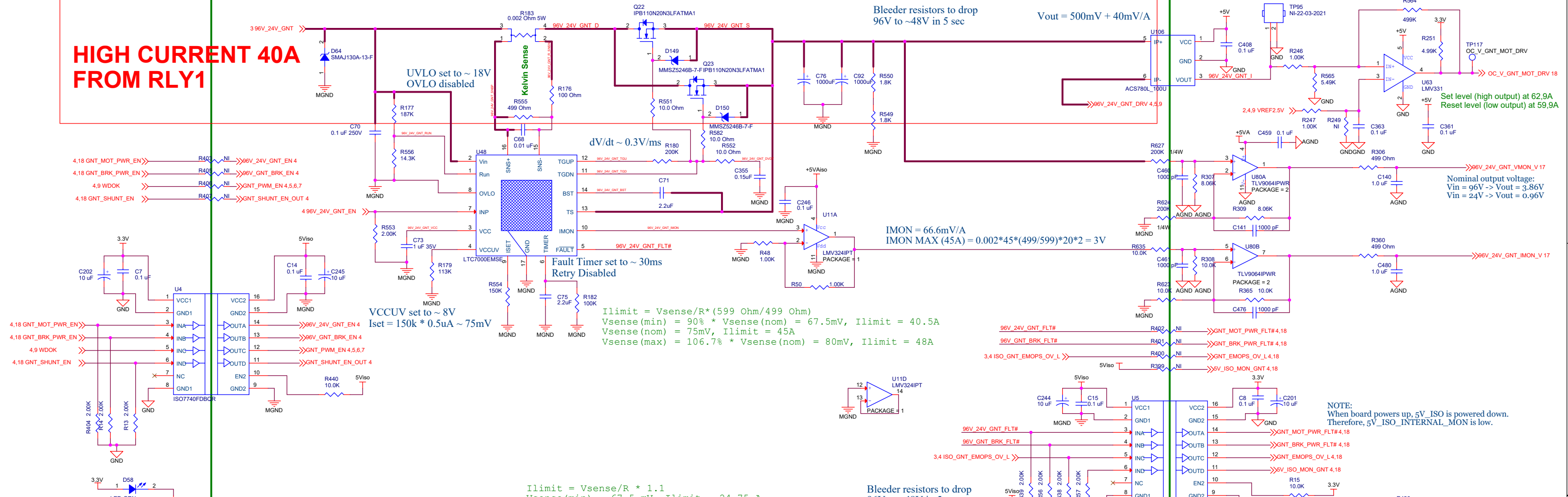
HIGH CURRENT 40A



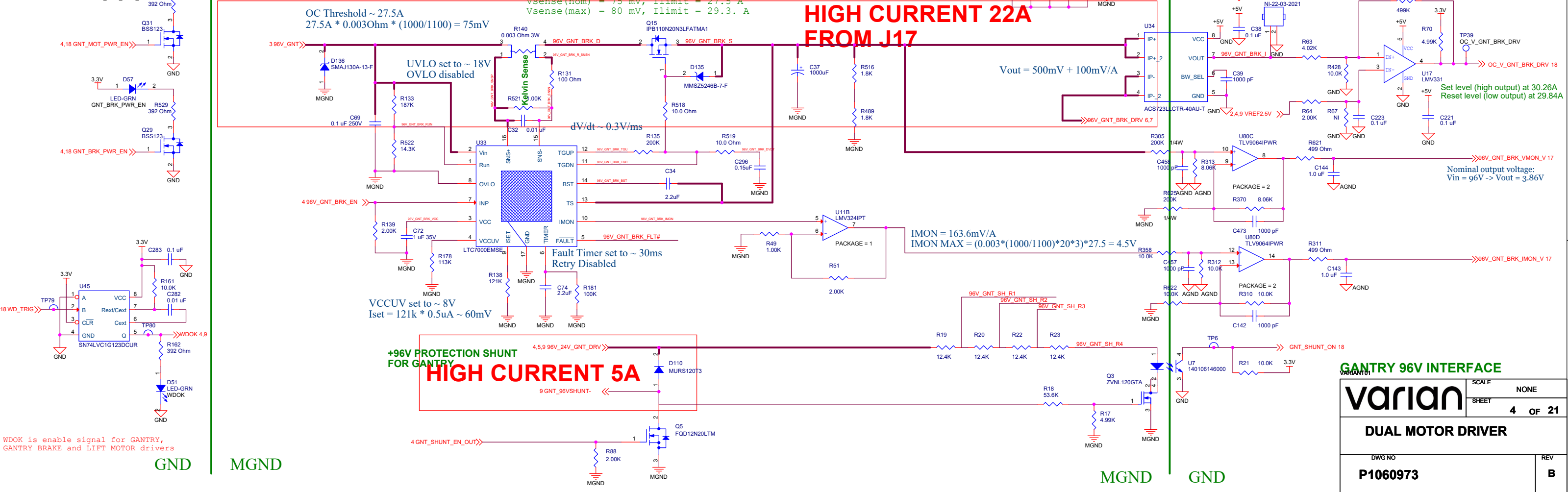
Finger safe
test point



HIGH CURRENT 40A FROM RLY1



HIGH CURRENT 5A FROM J17



HIGH CURRENT 5A FROM J17

+96V PROTECTION SHUNT FOR GANTRY

SCALE

NONE

SHEET

4 OF 21

DWG NO

P1060973

REV

B

WDOK is enable signal for GANTRY,
GANTRY BRAKE and LIFT MOTOR drivers

GND

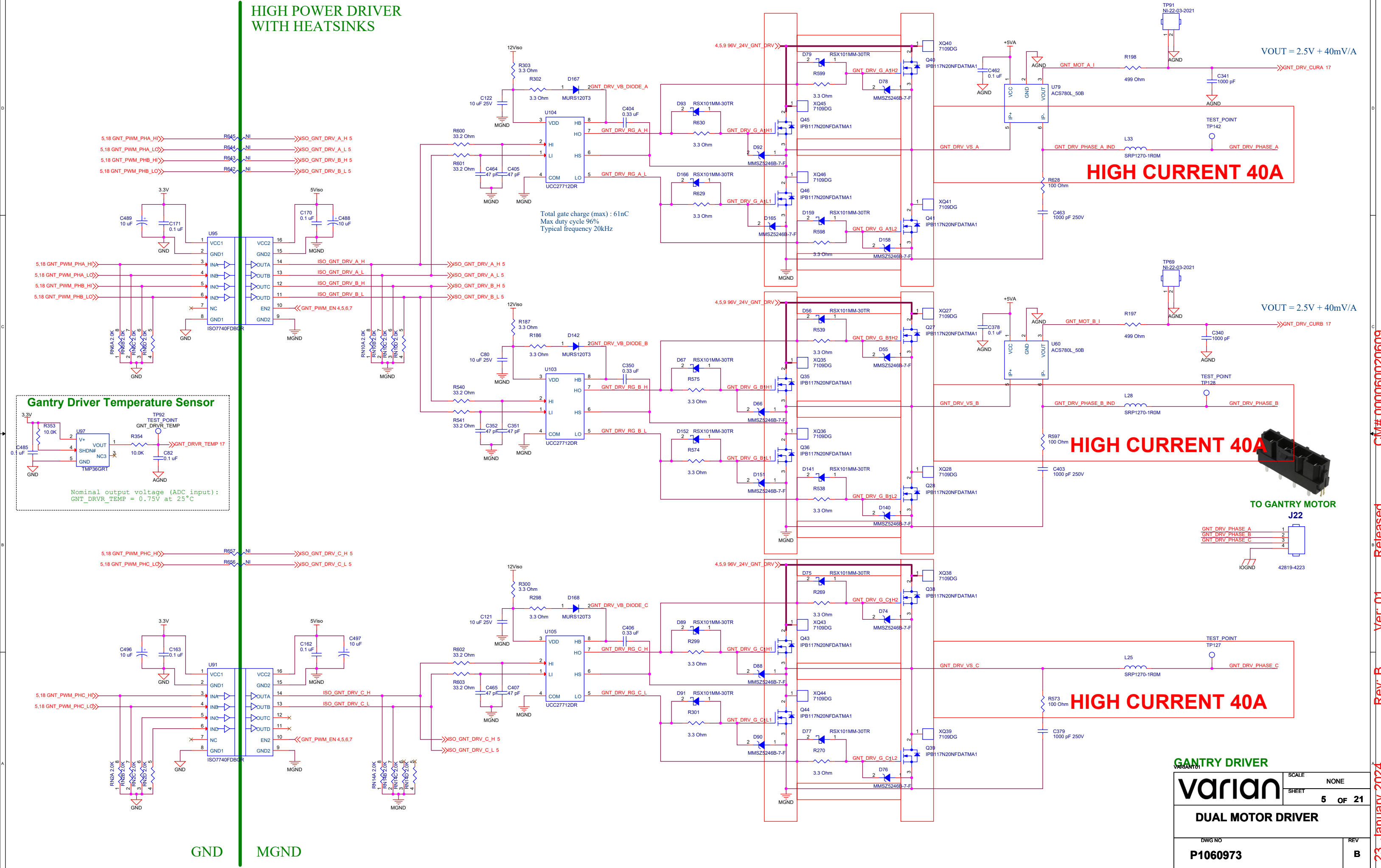
MGND

MGND

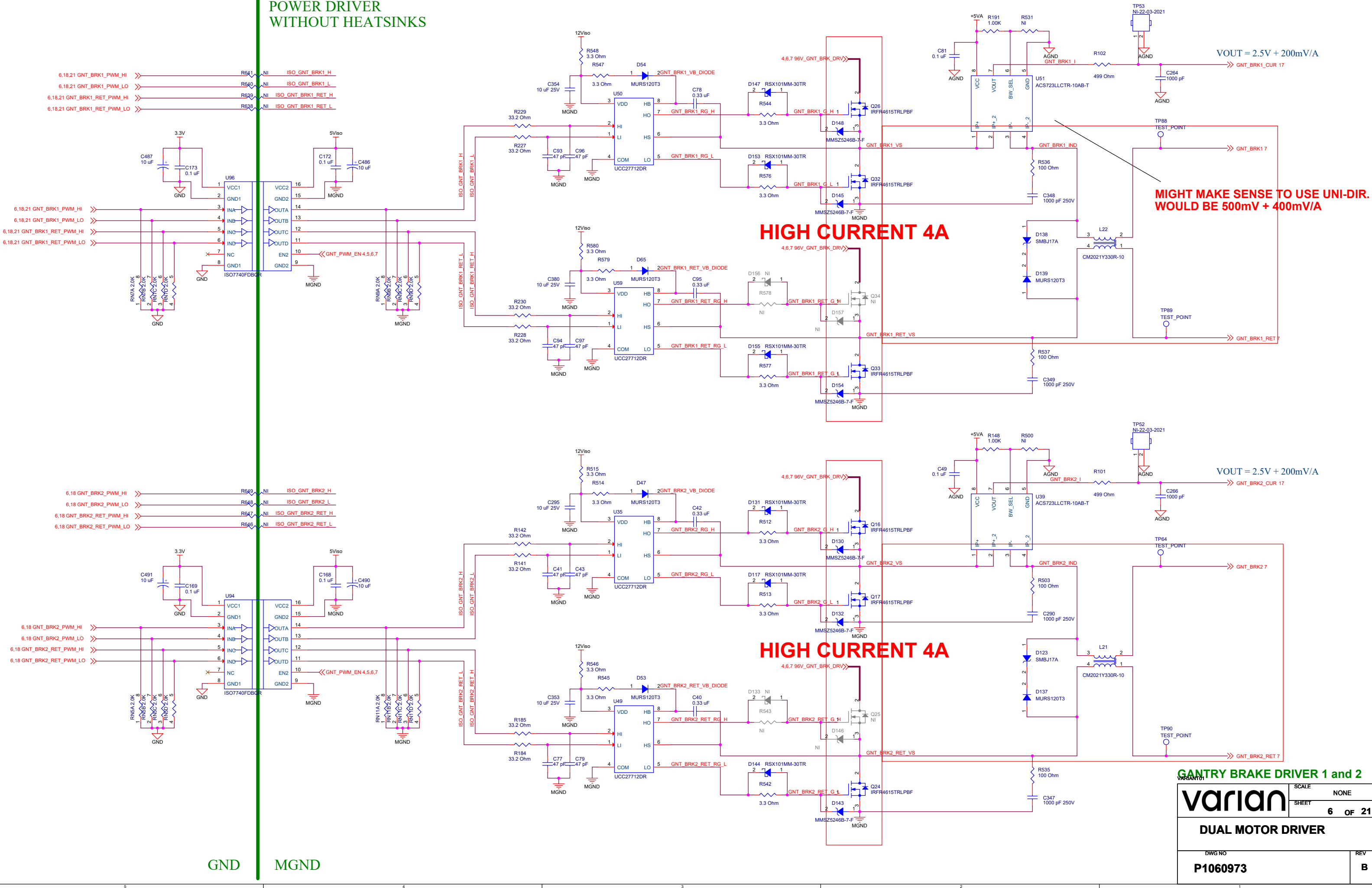
GND

CM# 000060020609
Released
Ver: 01
Rev: B
23. January 2024

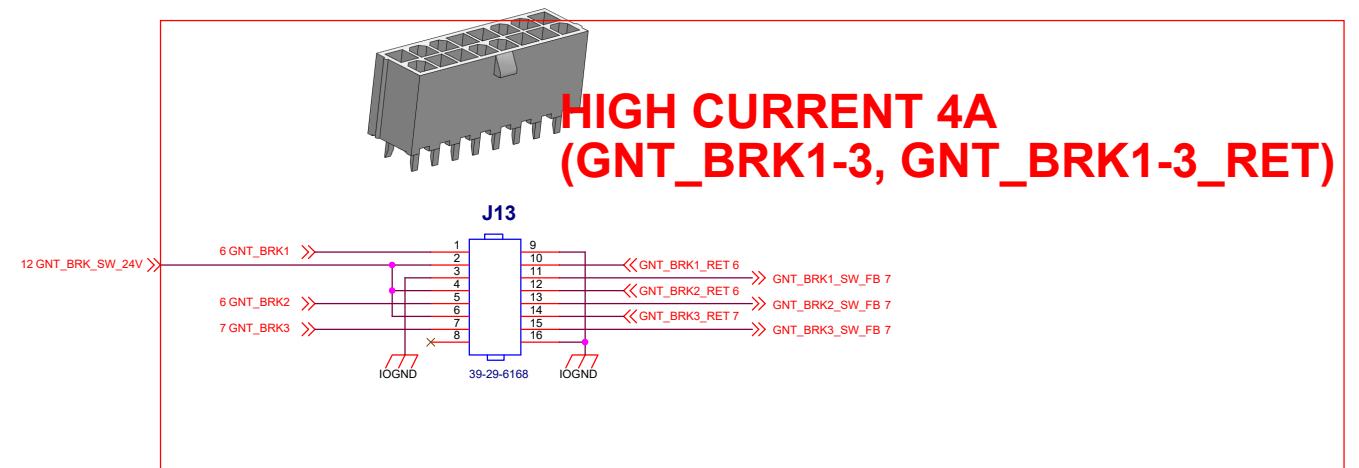
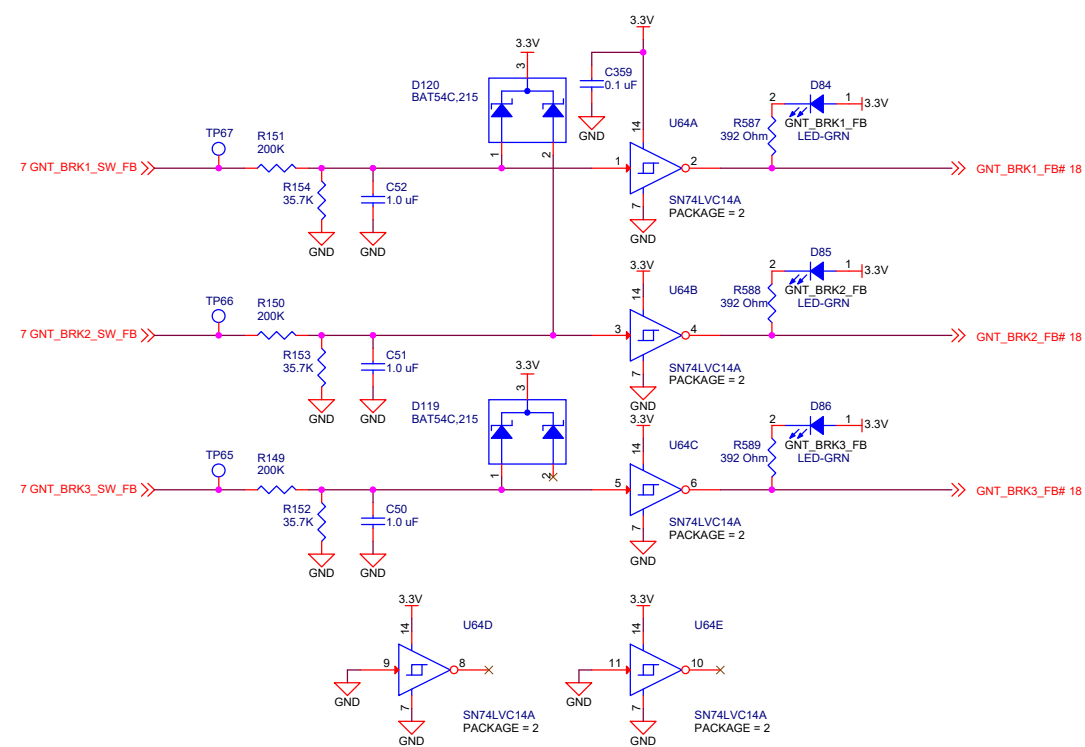
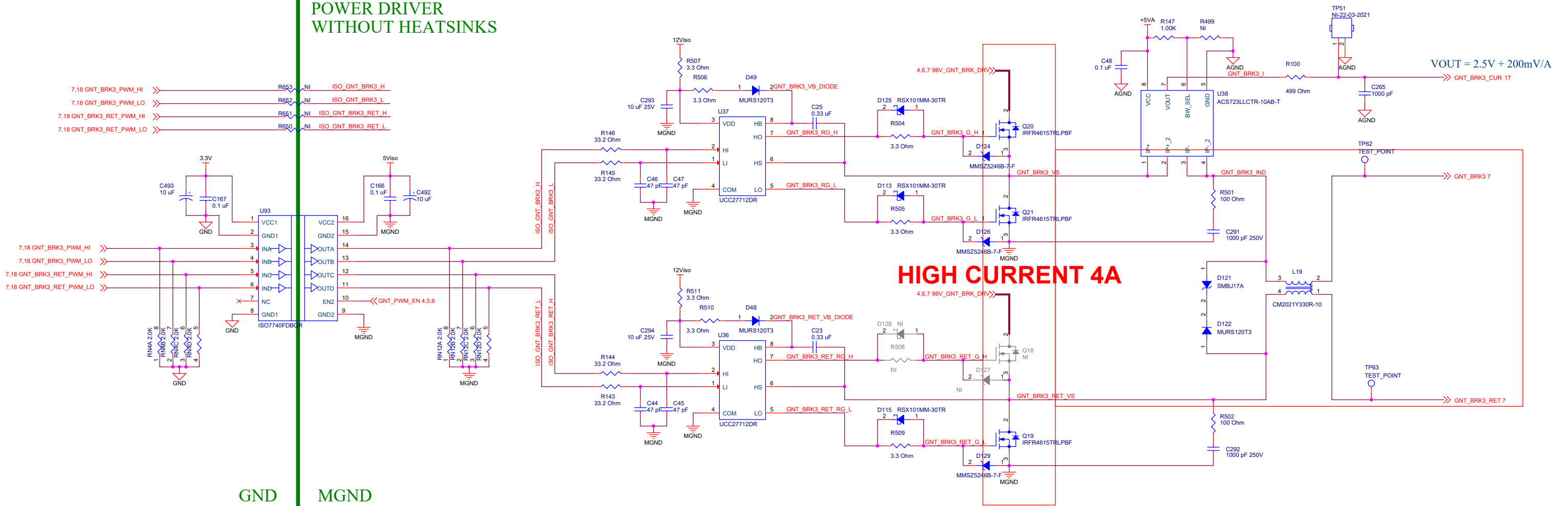
HIGH POWER DRIVER WITH HEATSINKS



POWER DRIVER
WITHOUT HEATSINKS



POWER DRIVER WITHOUT HEATSINKS



GANTRY BRAKE DRIVER 3 AND FEEDBACK

3.8 96V_LFT >> HIGH CURRENT 20A FROM J17

LIFT EMOPS

CURRENT LIMIT = 16.7A
 $I_{lim} = (50mV)/R_s = 16.666A$

HIGH CURRENT 15A FROM J18

The schematic shows a MOSFET driver circuit. The input is 2.3 24V_IN, which goes through a 0.003 Ohm 3W resistor (R4) to the gate of a MOSFET (Q1, STH180N10F3-2). The MOSFET's source is connected to ground (0V) and its drain is connected to the 24V_LIFT_EMOPS_S line. A 0.1 uF capacitor (C4) is connected between the drain and the 24V_LIFT_EMOPS_S line. The 24V_LIFT_EMOPS_S line then goes through a diode bridge rectifier (D1, D2, D3, D4, MBR2020CT4G) to the 24V_LIFT_EMOPS line. The diode bridge is connected to the 24V_LIFT_EMOPS line through a 0.003 Ohm 3W resistor (R7). The output of the diode bridge is connected to the 24V_LIFT_EMOPS line through a 0.1 uF capacitor (C4).

LIFT EMOPS

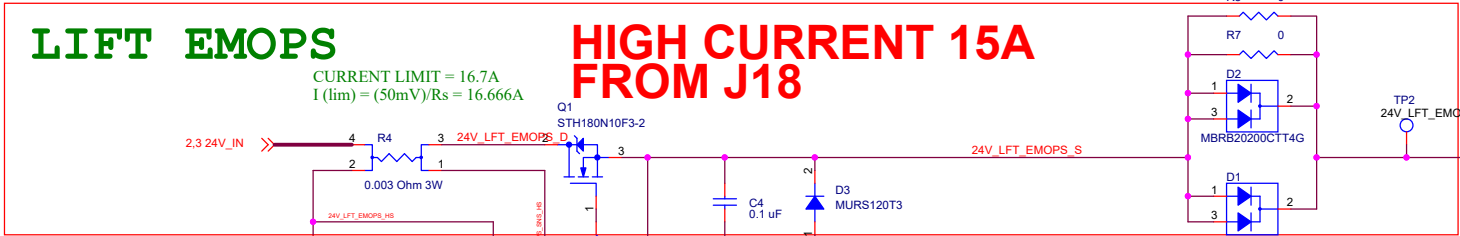
CURRENT LIMIT = 16.7A
 $I_{lim} = (50mV)/R_s = 16.666A$

HIGH CURRENT 15A FROM J18

The schematic shows a MOSFET driver circuit. The input is 2.3 24V_IN, which goes through a 0.003 Ohm 3W resistor (R4) to the gate of a MOSFET (Q1, STH180N10F3-2). The MOSFET's source is connected to ground (0V) and its drain is connected to the 24V_LIFT_EMOPS_S line. A 0.1 uF capacitor (C4) is connected between the drain and the 24V_LIFT_EMOPS_S line. The 24V_LIFT_EMOPS_S line then goes through a diode bridge rectifier (D1, D2, D3, D4, MBR2020CT14G) to the 24V_LIFT_EMOPS line. The diode bridge is connected to a 24V_LIFT_EMOPS_S line, which is then connected to the 24V_LIFT_EMOPS line. The diode bridge is also connected to a 24V_LIFT_EMOPS line, which is then connected to the 24V_LIFT_EMOPS line. The diode bridge is also connected to a 24V_LIFT_EMOPS line, which is then connected to the 24V_LIFT_EMOPS line.

HIGH CURRENT 20A

5V LFT 5
4V LFT_EMOPS 4
RLY1
1
3
2
HAT901CSDC24-1
24V
TP90
96V_24V_LIFT
96V_24V_LFT 8,9



The schematic diagram shows the LMV331 op-amp circuit. The non-inverting input (IN+) is connected to a voltage divider consisting of R46 (11.8K) and R47 (200K) connected to 2.3 2.5Vref_iso. The inverting input (IN-) is connected to a voltage divider consisting of R443 (10.0K) and R444 (1.0M) connected to 5Viso. The output (OUT) is connected to a load capacitor C249 (0.1 uF) to MGND. The op-amp is powered by VCC and GND.

24V_LFT_EMOPS

3.8 96V_LFT

R523
6.04K
1/4W

D59
EMOPS, 24V
LED-GRN

GND

R94
6.04K
1/4W

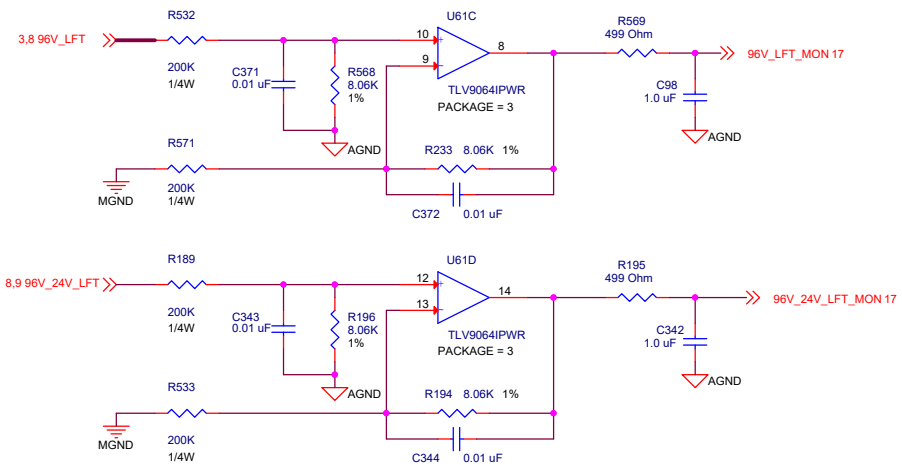
R93
6.04K
1/4W

R91
6.04K
1/4W

R87
6.04K
1/4W

D36
96V_GNT
LED-GRN

MGND



LIFT 96V EMOPS

VARIANT01

varian

varian

DUAL MOTOR DRIVER

DWG NO	REV
P1060973	B

CM# 000060020609

23. January 2024^A

**HIGH CURRENT 20A
FROM RLY2**

UVLO set to ~18V
OVLO disabled

$dV/dt \sim 0.3V/ms$

Fault Timer set to ~30ms
Retry Disabled

VCCUV set to ~8V
 $I_{set} = 121k * 0.5uA \sim 60mV$

$I_{limit} = V_{sense}/R$
 $V_{sense}(min) = 54mV, I_{limit} = 18A$
 $V_{sense}(nom) = 60mV, I_{limit} = 20A$
 $V_{sense}(max) = 64mV, I_{limit} = 21.3A$

Bleeder resistors to drop
96V to ~48V in 5 sec

$V_{out} = 500mV + 100mV/A$

$IMON = 180mV/A$
 $IMON_{MAX} = 0.003 * 20 * 20 * 3 = 3.6V$

Set level (high output) at 24.608A
Reset level (low output) at 24.5A

Nominal output voltage:
 $V_{in} = 96V \rightarrow V_{out} = 3.86V$
 $V_{in} = 24V \rightarrow V_{out} = 0.96V$

NOTE:
When board powers up, 5V_ISO is powered down.
Therefore, 5V_ISO_INTERNAL_MON is low.

**COMBINED CONNECTOR FOR
LIFT AND GANTRY SHUNT**

HIGH CURRENT 3A

HIGH CURRENT 5A

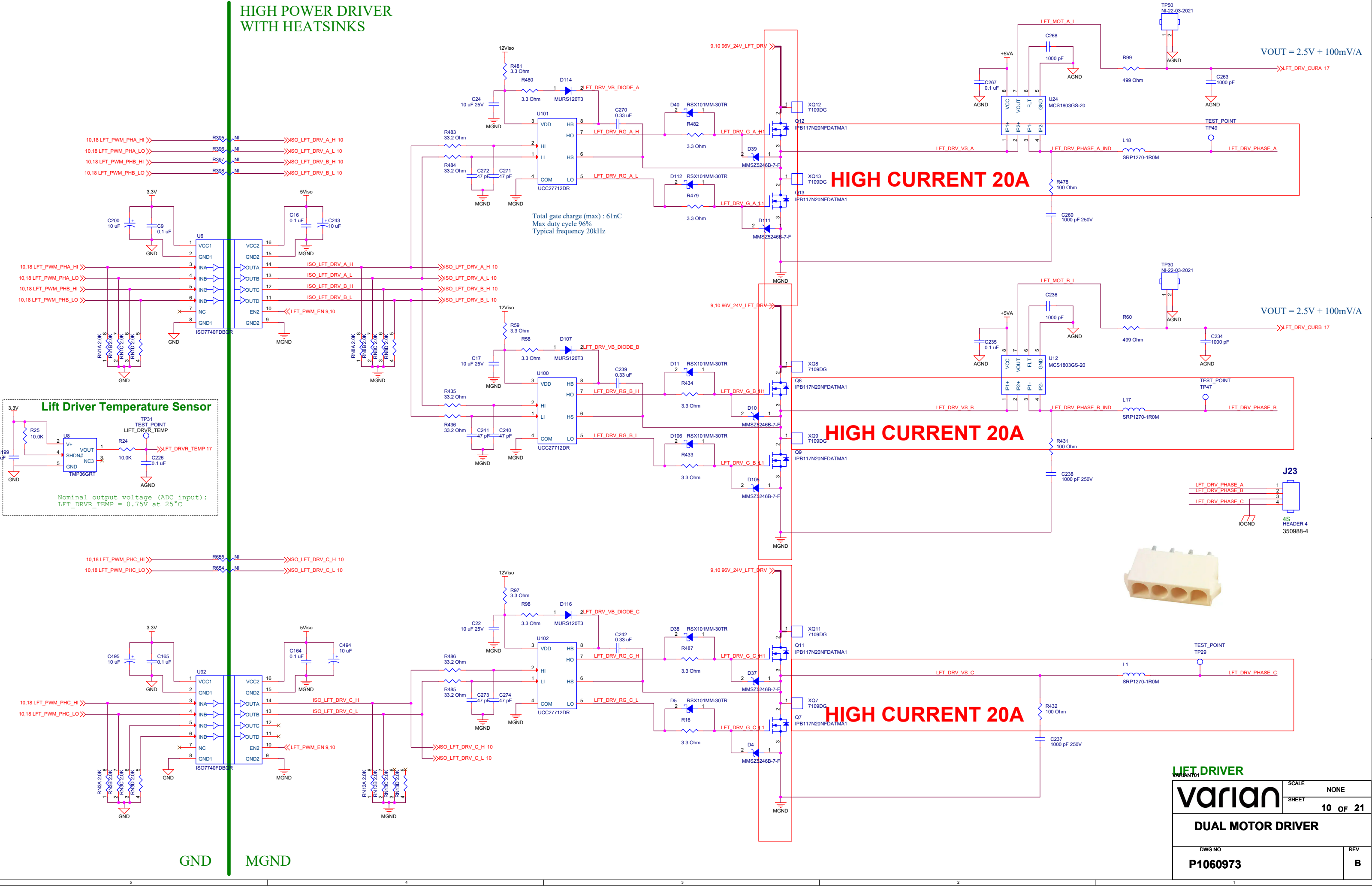
+96V PROTECTION SHUNT
FOR LIFT

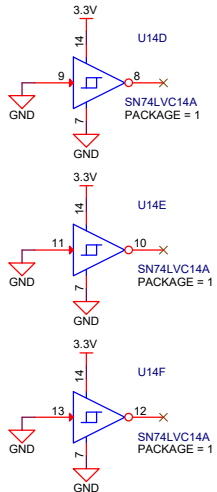
HIGH CURRENT 3A

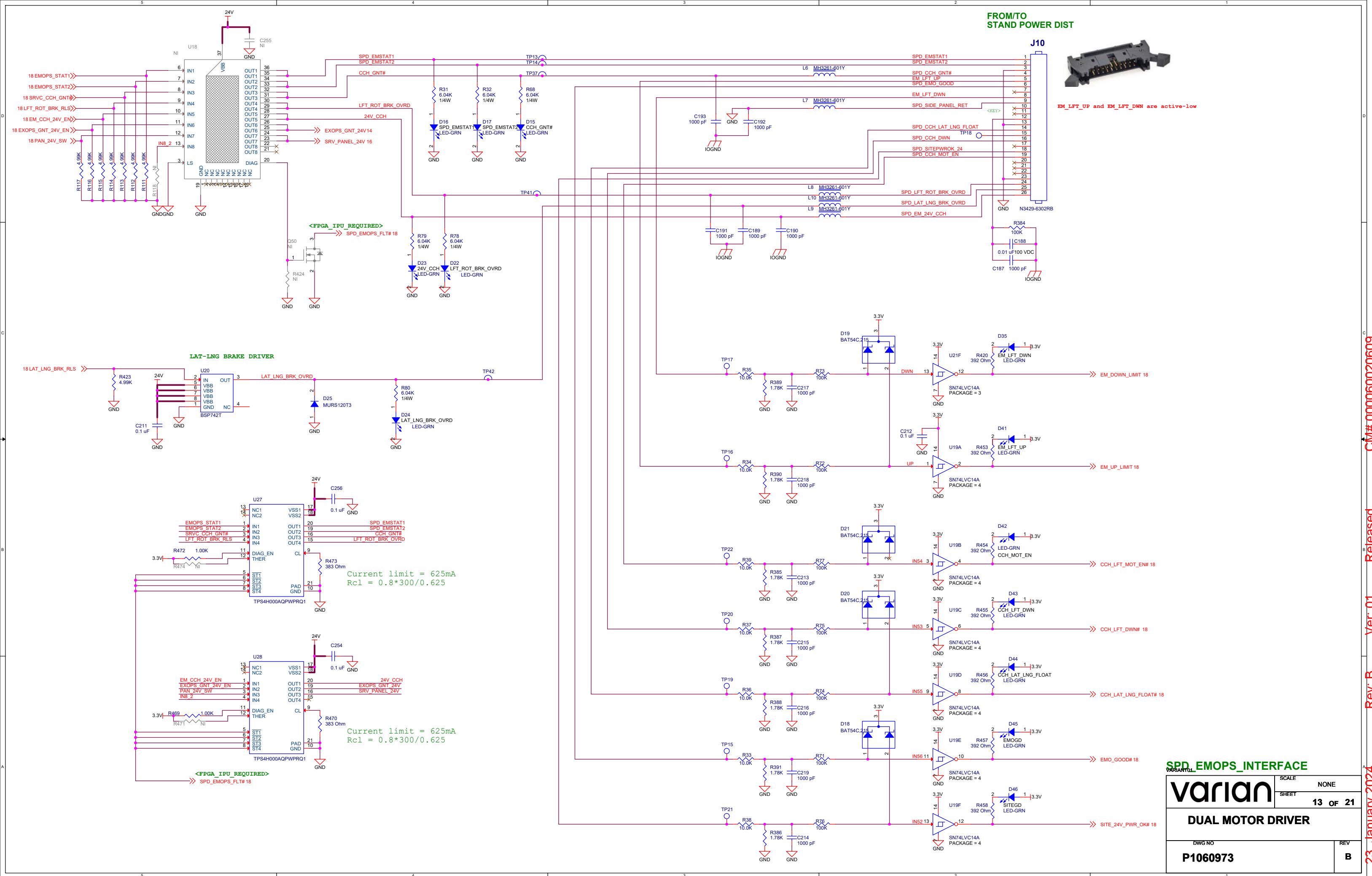
LIFT 96V INTERFACE

varian	SCALE	NONE
	SHEET	9 OF 21
DUAL MOTOR DRIVER		
DWG NO	REV	
P1060973	B	

HIGH POWER DRIVER WITH HEATSINKS







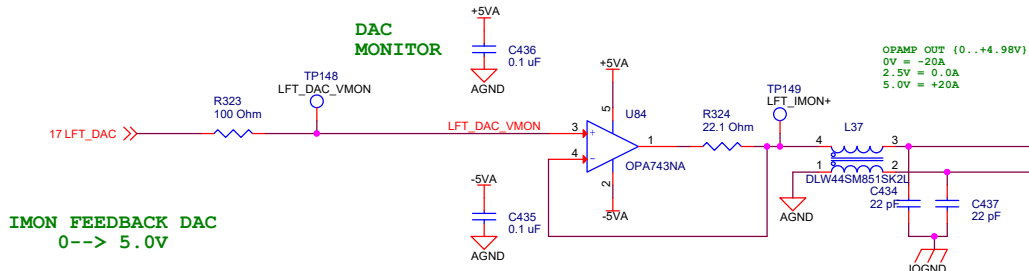


FROM/TO CCHL

J12

ANALOG INTERFACE

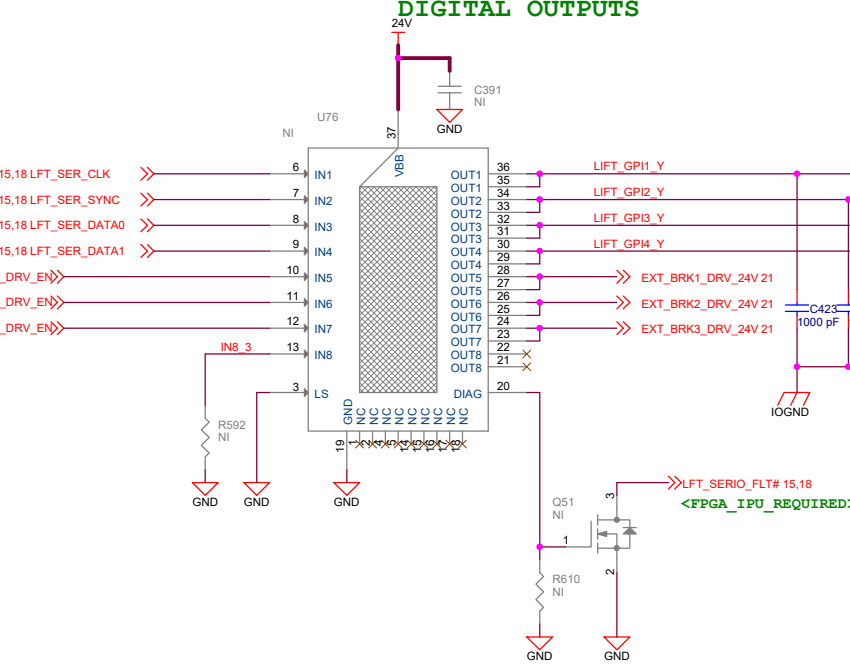
DAC MONITOR



IMON FEEDBACK DAC
0--> 5.0V

OPAMP OUT (0...+4.98V)
0V = -20A
2.5V = 0.0A
5.0V = +20A

DIGITAL OUTPUTS

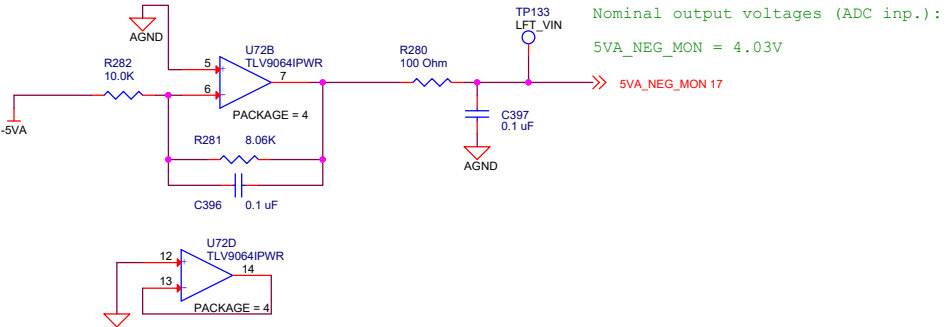
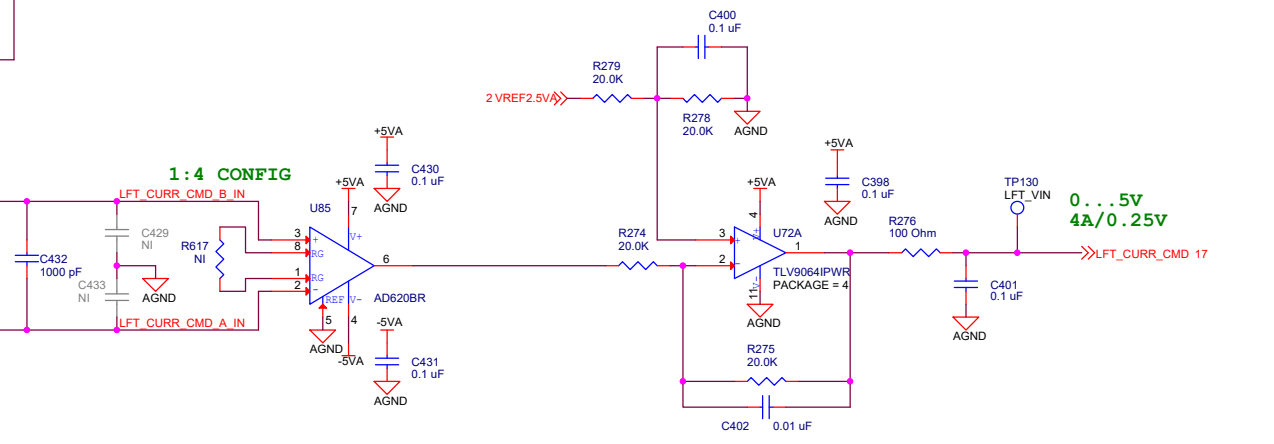


Current limit = 51mA
Rcl = 0.8*300/0.05

Current limit = 625mA
Rcl = 0.8*300/0.625

1:4 CONFIG

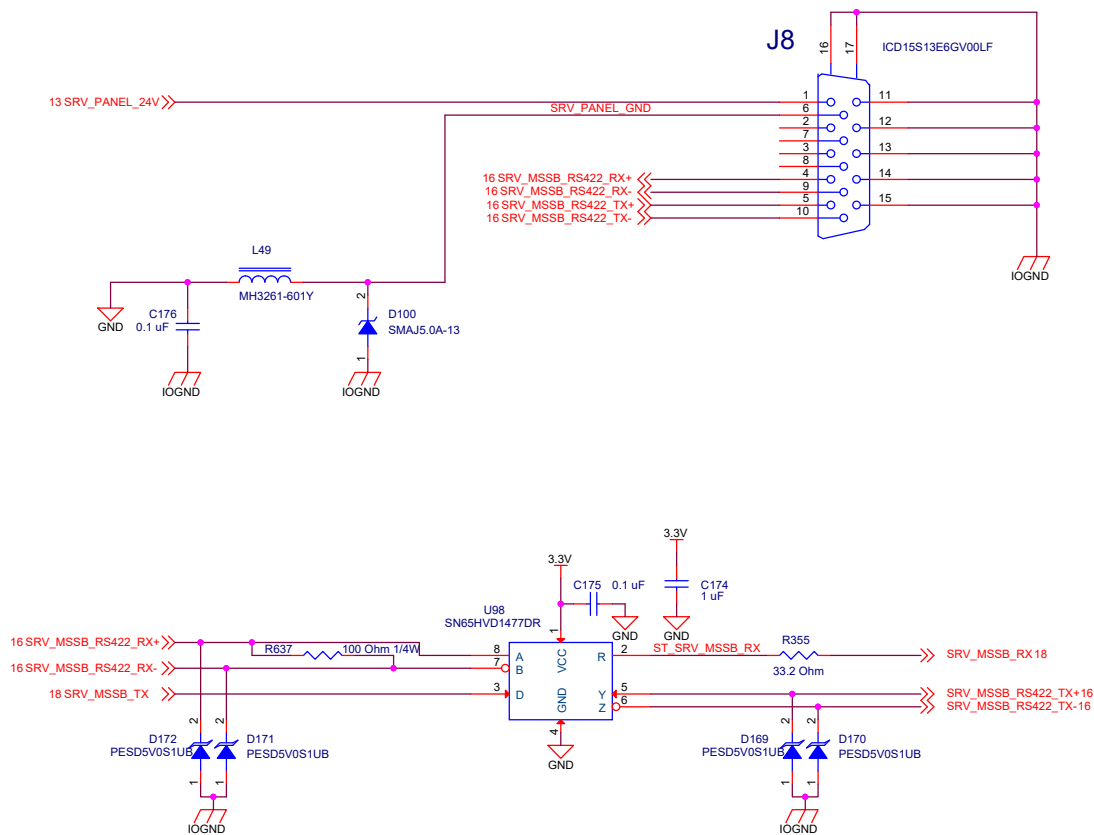
Input Diff. Range: +/-10V
Scaling: 4A/1V



Nominal output voltages (ADC inp.):
5VA_NEG_MON = 4.03V

CCHL INTERFACE

SCALE		NONE
SHEET		15 OF 21
DUAL MOTOR DRIVER		
DWG NO		REV
P1060973		B

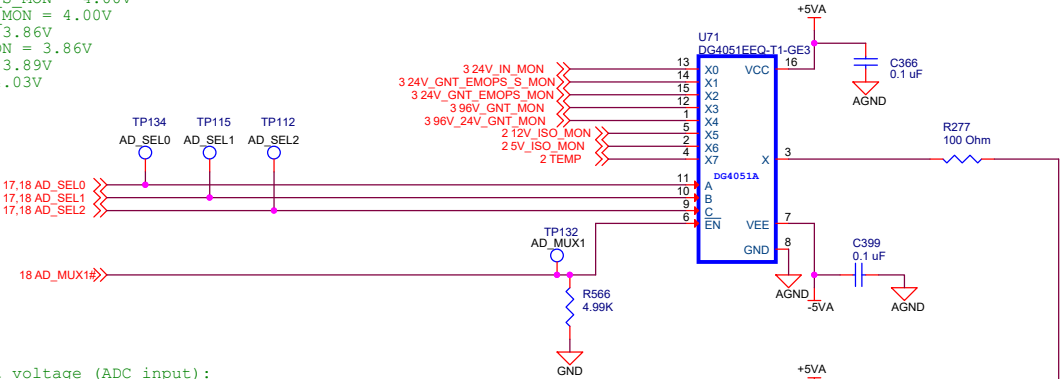


SERVICE PENDANT

varian	SCALE	NONE
	SHEET	16 OF 21
DUAL MOTOR DRIVER		
DWG NO	REV	
P1060973	B	

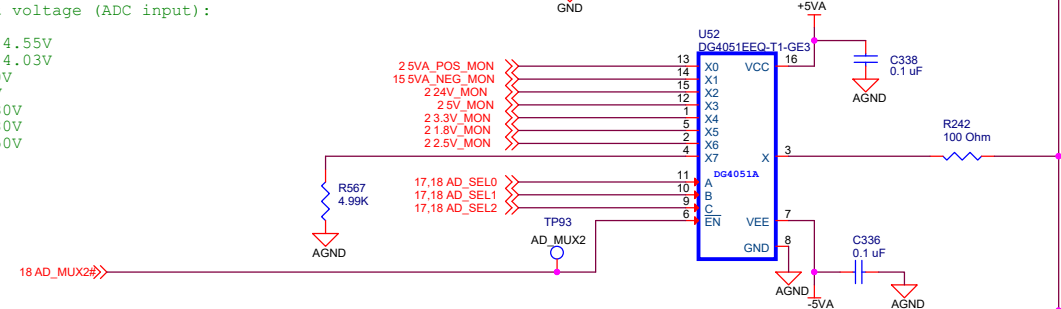
Nominal output voltages (ADC inputs):

24V IN_MON = 4.00V
24V_GNT_EMOPS_S_MON = 4.00V
24V_GNT_EMOPS_MON = 4.00V
96V_GNT_MON = 3.86V
96V_24V_GNT_MON = 3.86V
12V_ISO_MON = 3.89V
5V_ISO_MON = 4.03V
TEMP = 0.75V



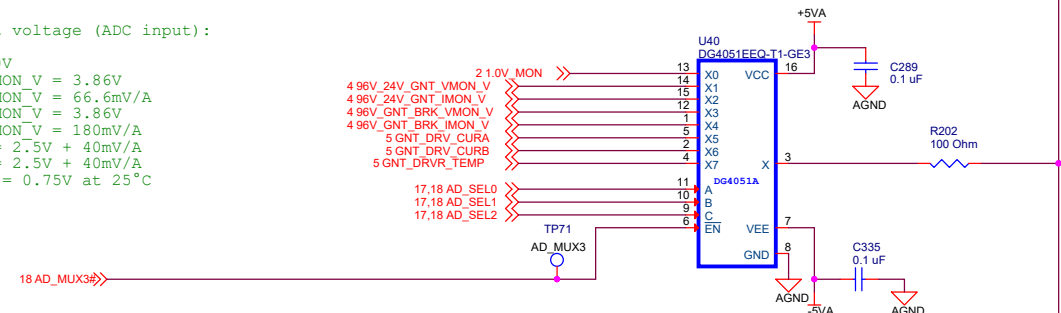
Nominal output voltage (ADC input):

5VA_POS_MON = 4.55V
5VA_NEG_MON = 4.03V
24V_MON = 4.00V
5V_MON = 4.55V
3.3V_MON = 3.30V
1.8V_MON = 1.80V
2.5V_MON = 2.50V



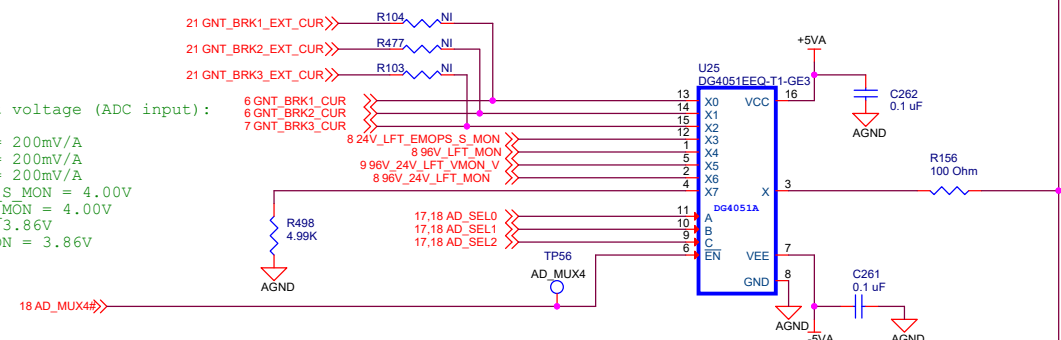
Nominal output voltage (ADC input):

1.0V_MON = 1.0V
96V_24V_GNT_VMON_V = 3.86V
96V_24V_GNT_IMON_V = 66.6mV/A
96V_GNT_BRK_VMON_V = 3.86V
96V_GNT_BRK_IMON_V = 180mV/A
GNT_DRV_CURA = 2.5V + 40mV/A
GNT_DRV_CURB = 2.5V + 40mV/A
GNT_DRV_TEMP = 0.75V at 25°C



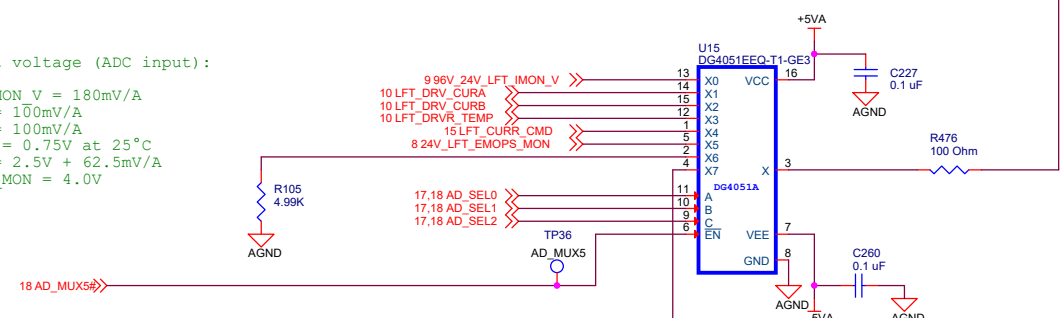
Nominal output voltage (ADC input):

GNT_BRK1_CUR = 200mV/A
GNT_BRK2_CUR = 200mV/A
GNT_BRK3_CUR = 200mV/A
24V_LFT_EMOPS_S_MON = 4.00V
24V_LFT_EMOPS_MON = 4.00V
96V_LFT_MON = 3.86V
96V_24V_LFT_MON = 3.86V



Nominal output voltage (ADC input):

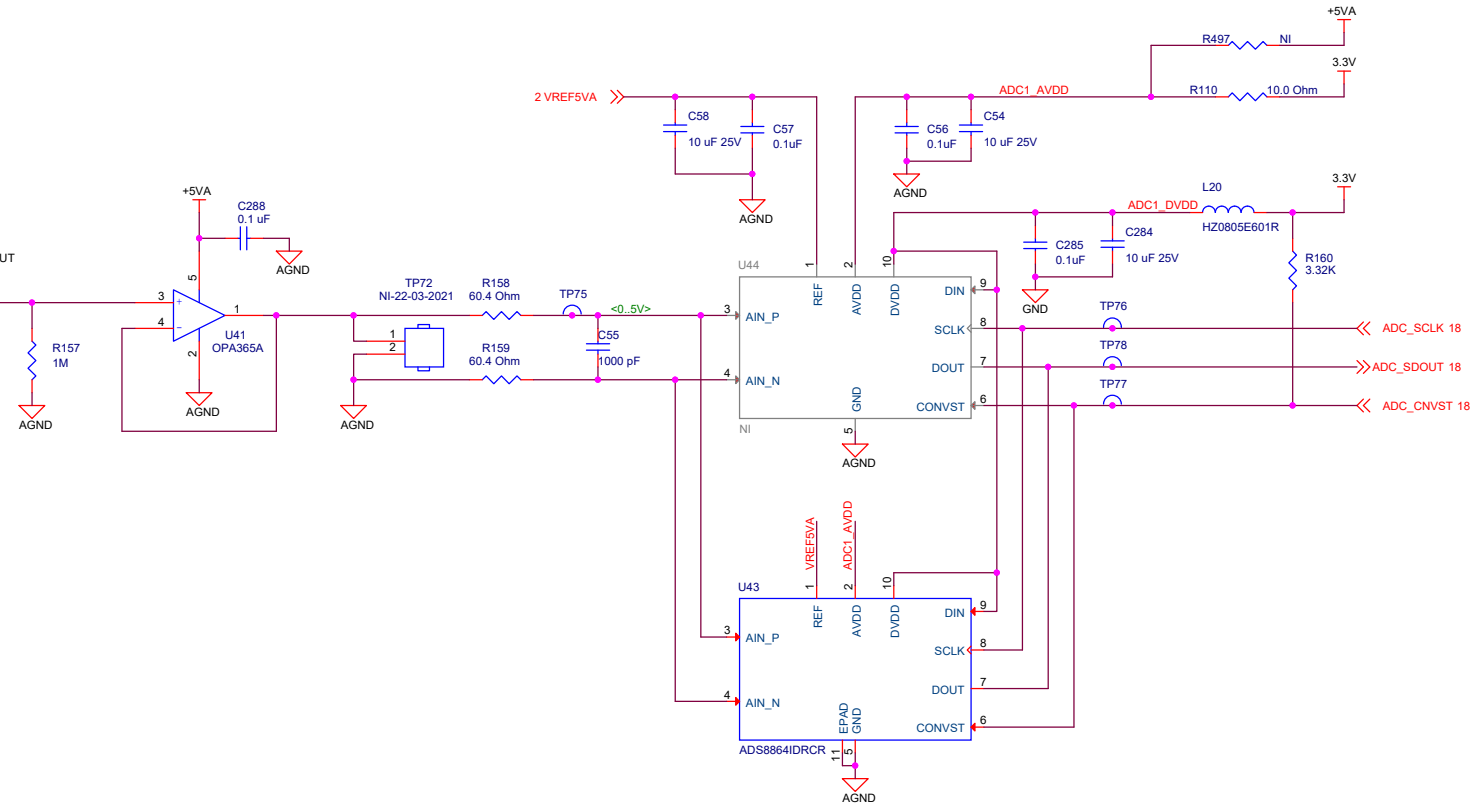
96V_24V_LFT_IMON_V = 180mV/A
LFT_DRV_CURA = 100mV/A
LFT_DRV_CURB = 100mV/A
LFT_DRV_TEMP = 0.75V at 25°C
LFT_CURR_CMD = 2.5V + 62.5mV/A
24V_LFT_EMOPS_MON = 4.0V



- Max. input voltage 5V
- Resolution (typ) = 16-bit
- Analog Input Range = 0..4.95V
- LSB = 76.3uV

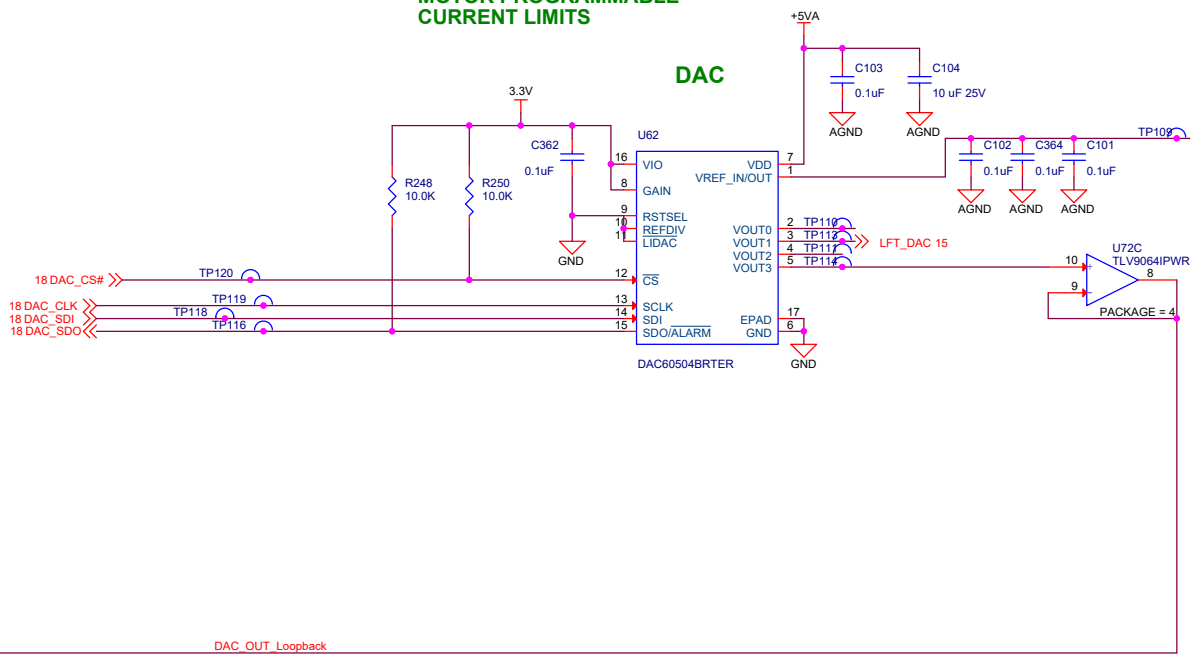
Note: Keep digital AD-signals inside GND plane region. Do not route into AGND region

5V for compatibility with ADS8339



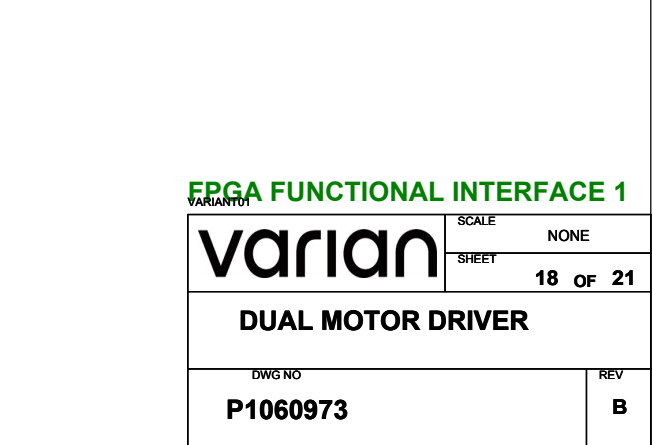
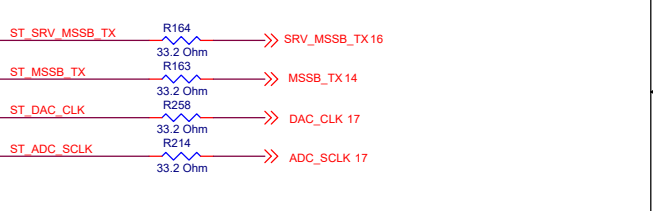
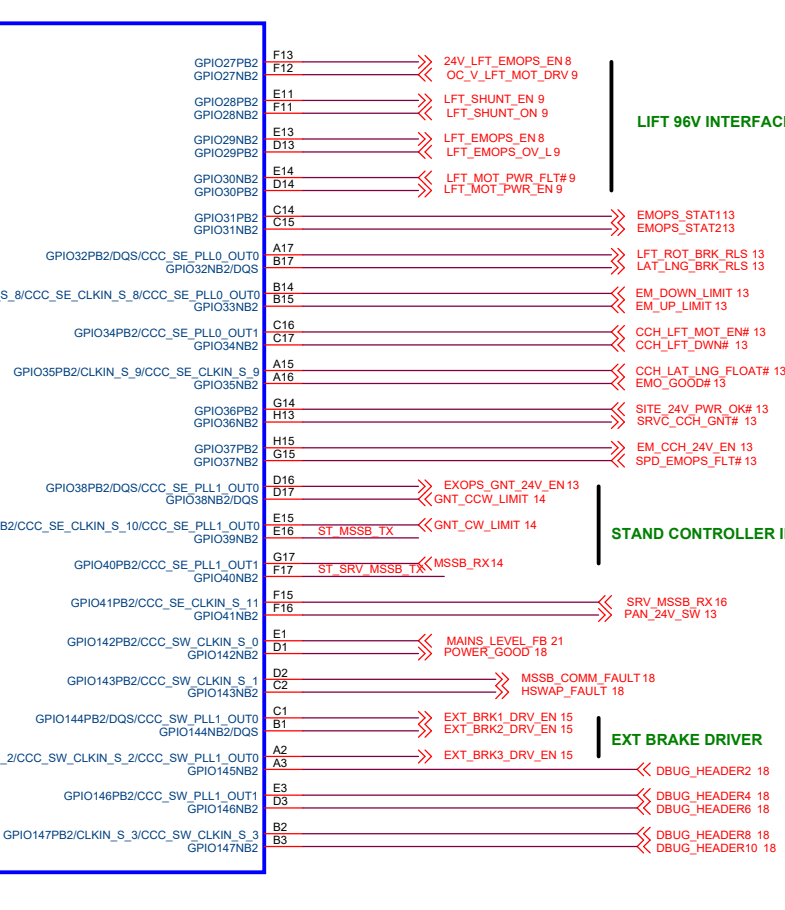
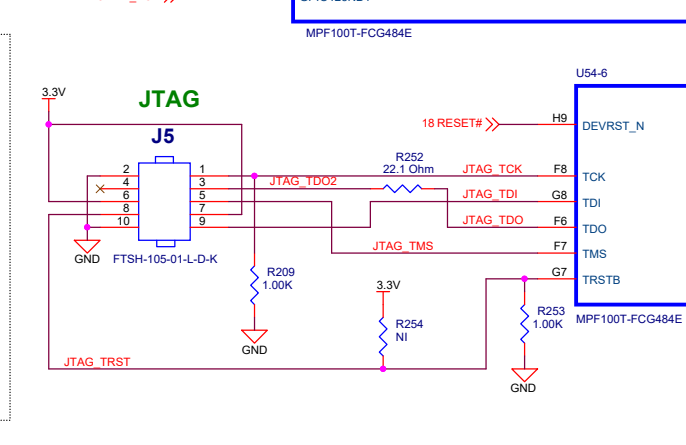
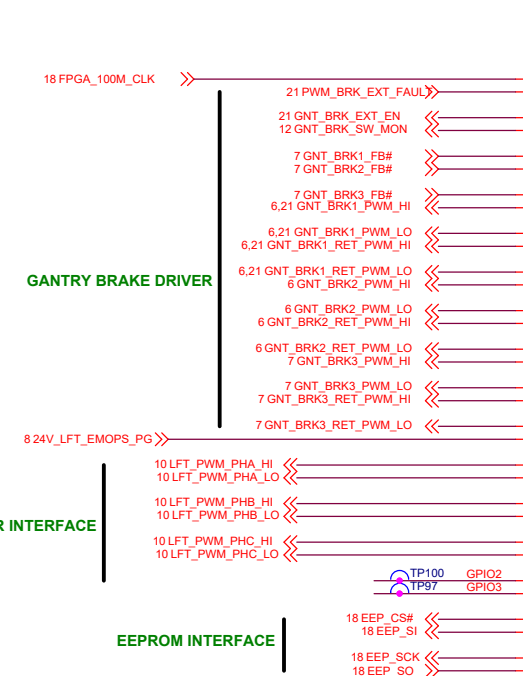
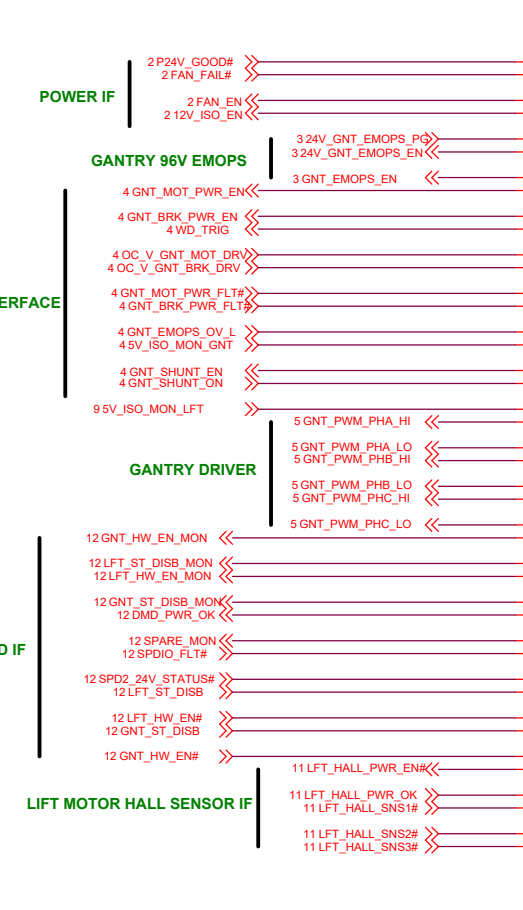
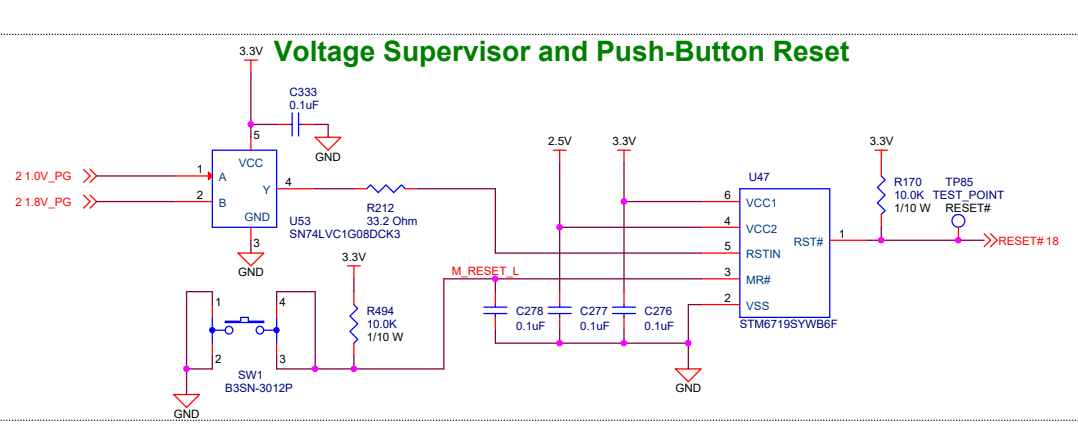
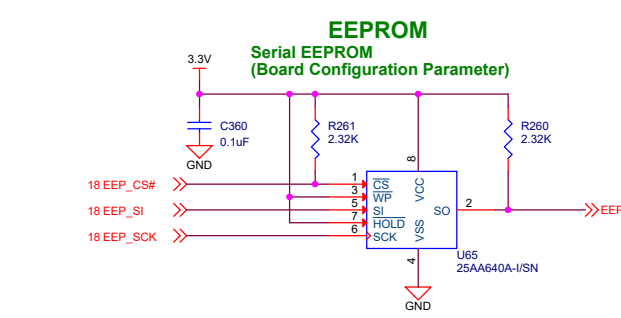
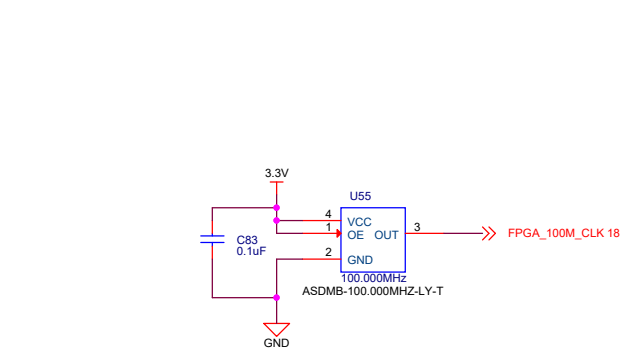
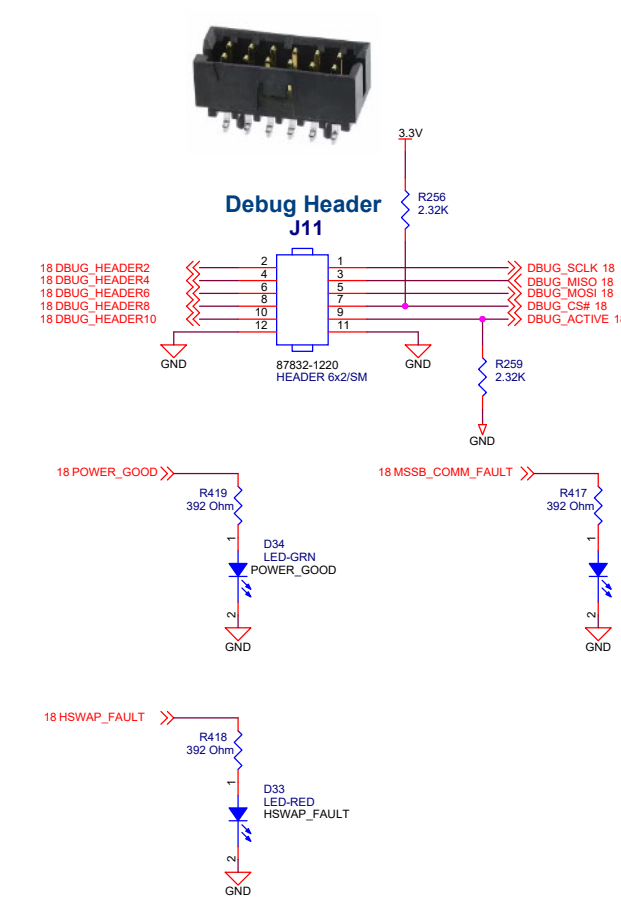
MOTOR PROGRAMMABLE
CURRENT LIMITS

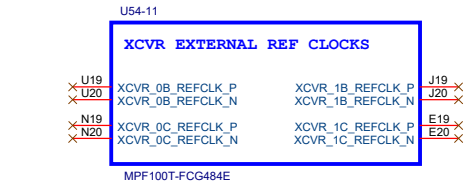
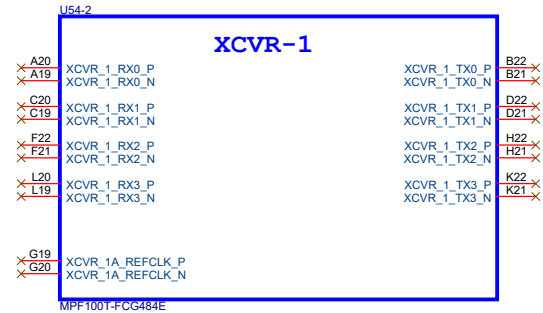
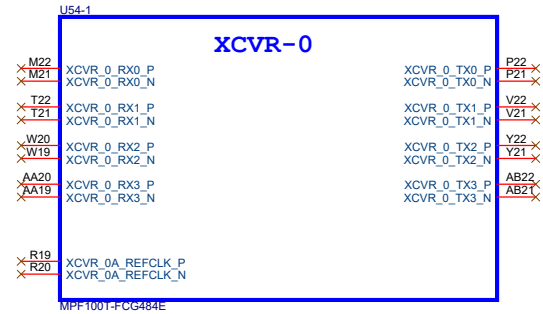
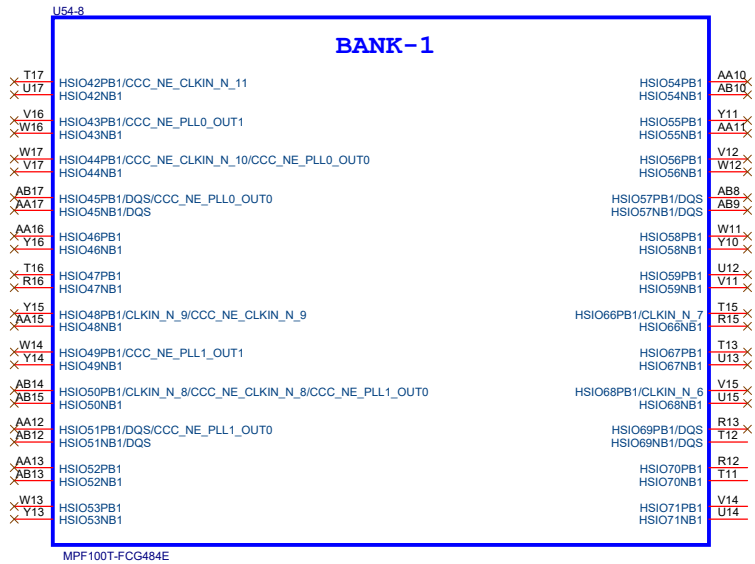
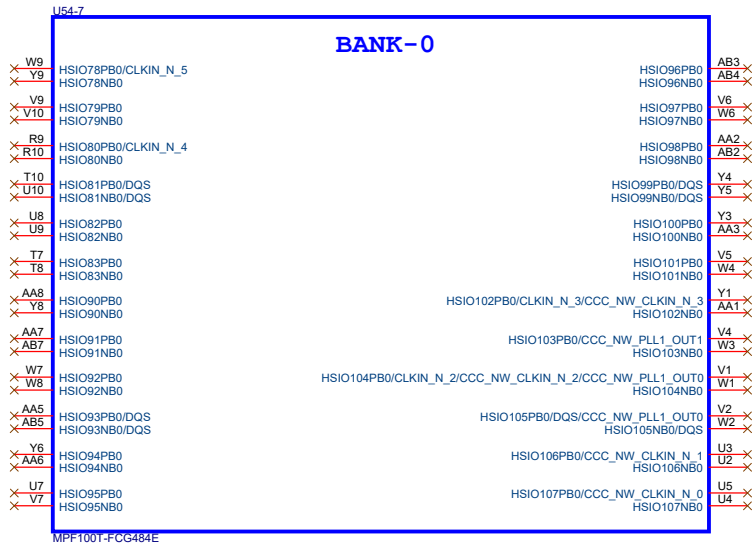
DAC



AD AND D/A CONVERTERS

VARIATION		SCALE	NONE
varian		SHEET	17 OF 21
DUAL MOTOR DRIVER			
/		REV	
DWG NO		B	
P1060973			





EPGA FUNCTIONAL INTERFACE 2

varian	SCALE	NONE
	SHEET	19 OF 21
DUAL MOTOR DRIVER		
DWG NO	REV	
P1060973	B	

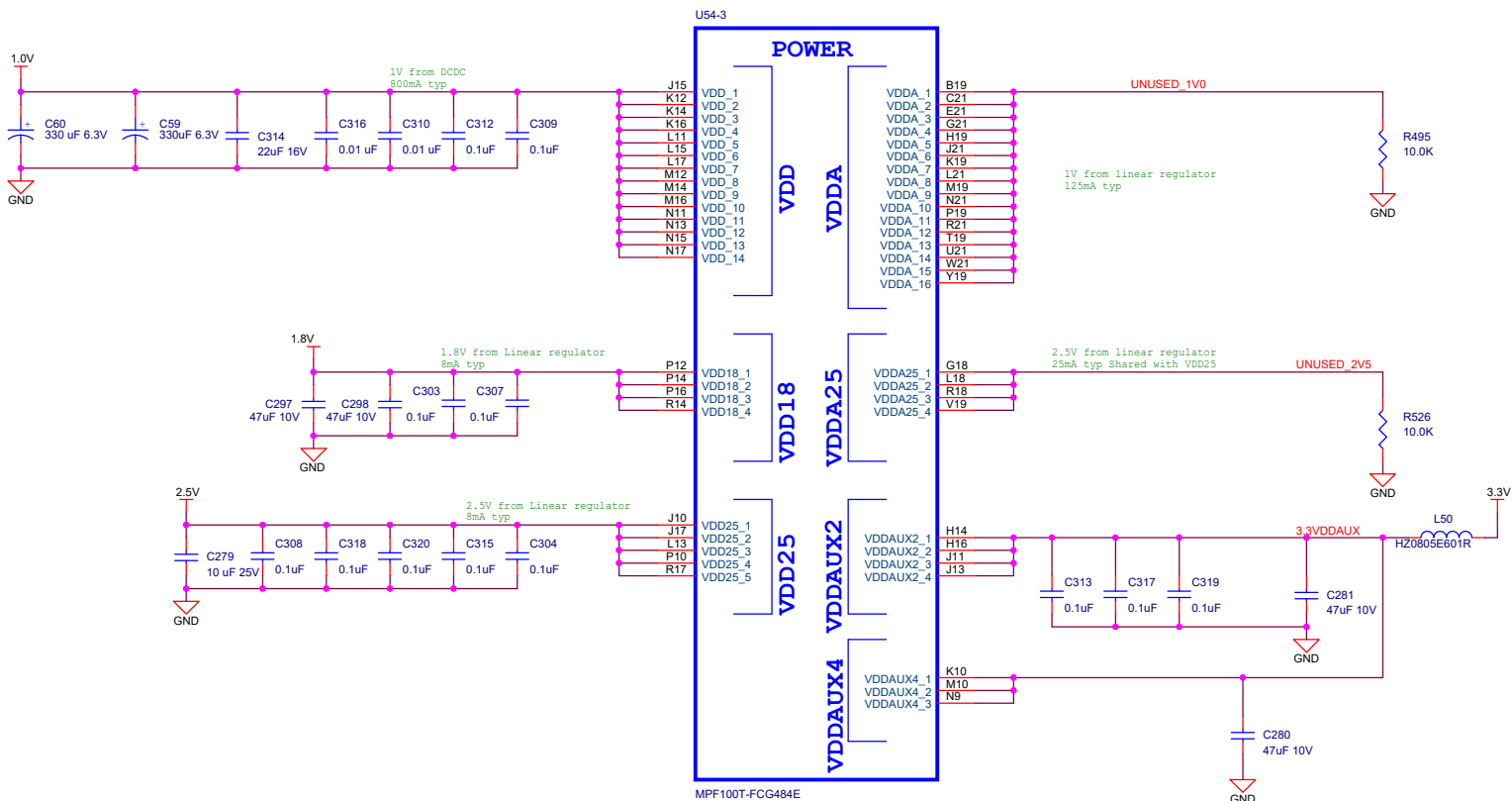


Figure 1 • Power Supplies

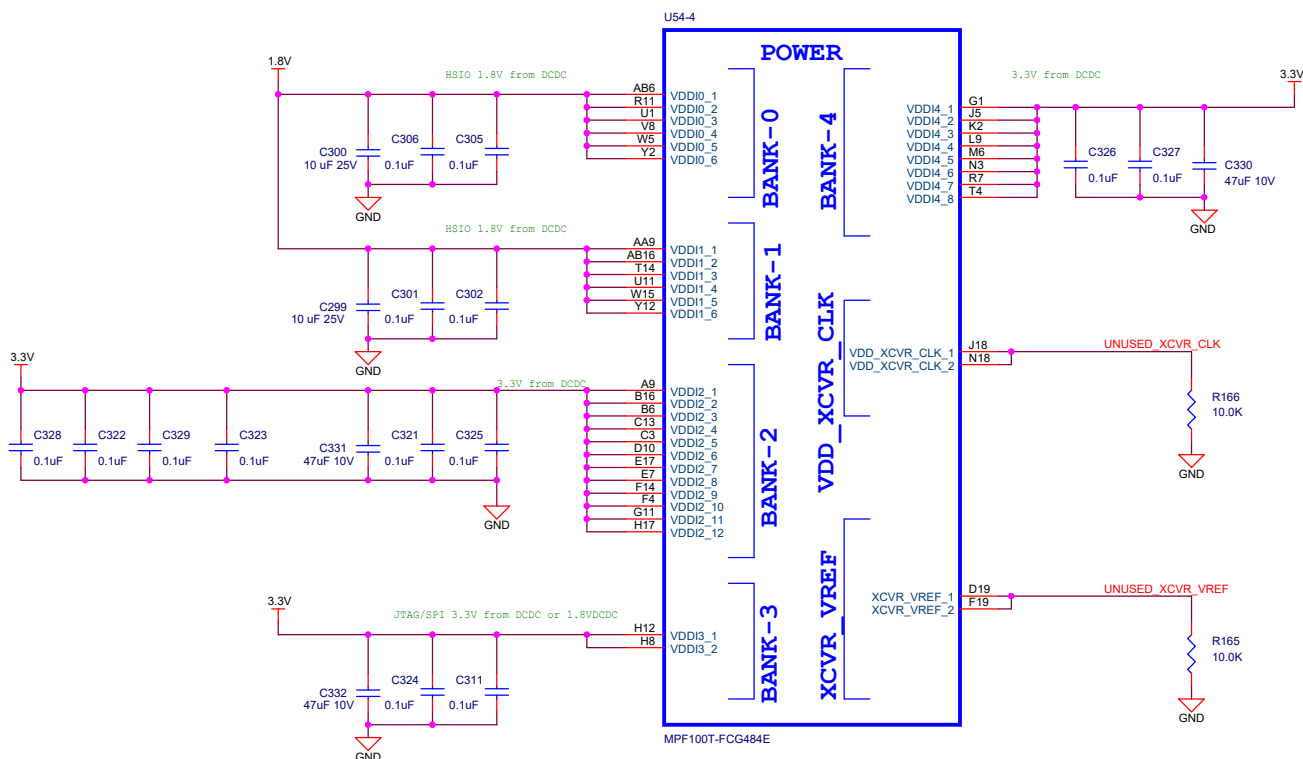
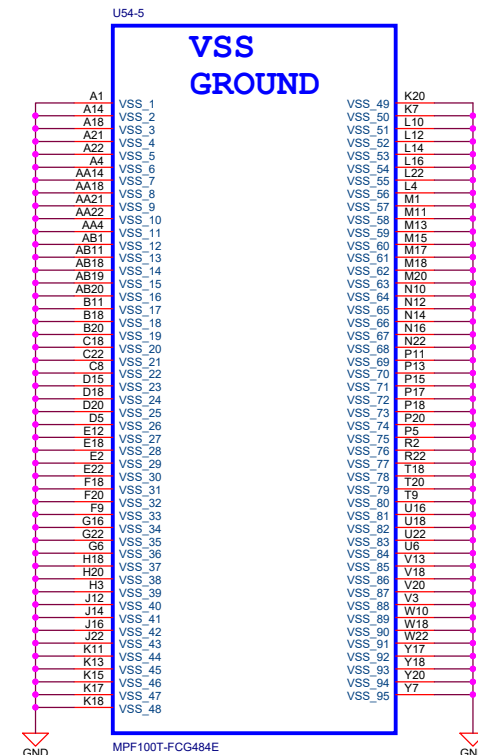
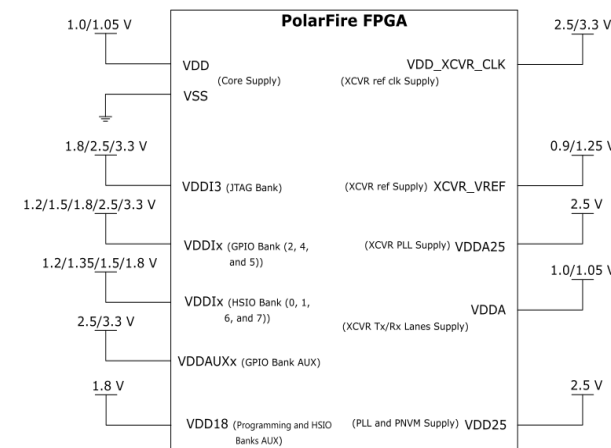


Table 12 • Power-Supply Decoupling Capacitors—MPF100T - FCG484 (1 mm)

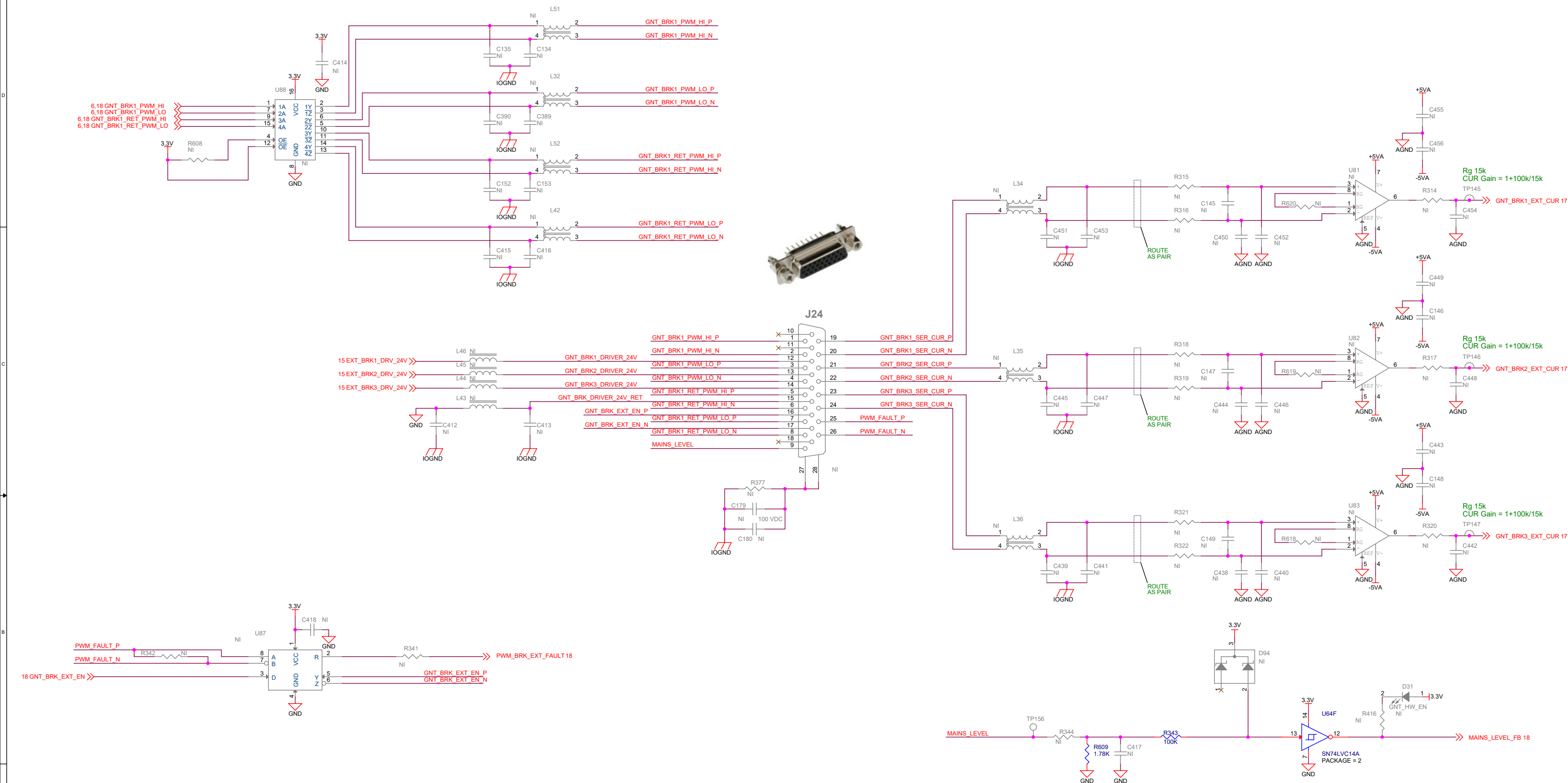
Pin Name	Ceramic							Tantalum
	4.7 nF	10 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	
V _{DD}		2	2					1
V _{DD18}			2				2	
V _{DD25}			5			1		
V _{DDA}	3	1	6				1	
V _{DDA25}			4				1	
V _{DDIO3}			2			1		
V _{DDAUXx} ¹			2				1	
GPIO Bank ²			2				1	
HSIO Bank ³			2				1	
V _{DD_XCVR_CLK}			2			1		
XCVR_VREF			2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

MPF100T-FCG484E

<p>SCALE</p> <p>NONE</p>	
<p>SHEET</p> <p>20 OF 21</p>	
<p>DUAL MOTOR DRIVER</p>	
<p>DWG NO</p> <p>P1060973</p>	<p>REV</p> <p>B</p>

**ALL CIRCUITS ON THIS PAGE NOT INSTALLED.
FOR POSSIBLE FUTURE USE.**



EXTERNAL BRAKE DRIVER IF

varian	SCALE	NONE
	SHEET	21 OF 21
DUAL MOTOR DRIVER		
DWG NO		REV
P1060973		B

CM# 000060020609

Released

Ver: 01

Rev: B

23. January 2024

Signature File



Document: P1060973/SCH/000/01
Description: SCH, DUAL MOTOR DRIVER

Change Master Number: 60020609
ECN Number: 200109363
ECN Description:

Signature list

Date	Time	User	Status
23, January 2024	18:57:04	Gary Yen	Released
23, January 2024	18:56:01	Rami Abdelmotalib	Approved
23, January 2024	03:36:52	Kevin Greenberg	In Eng Approval
09, December 2023	00:06:21	Gary Yen	In Checking
08, December 2023	15:53:01	Gary Yen	In Drafting
17, November 2023	21:16:05	Gary Yen	In Works