VARIANTS

DASH NO.	TYPE OR MODEL	NEXT ASSEMBLY
		P1060966

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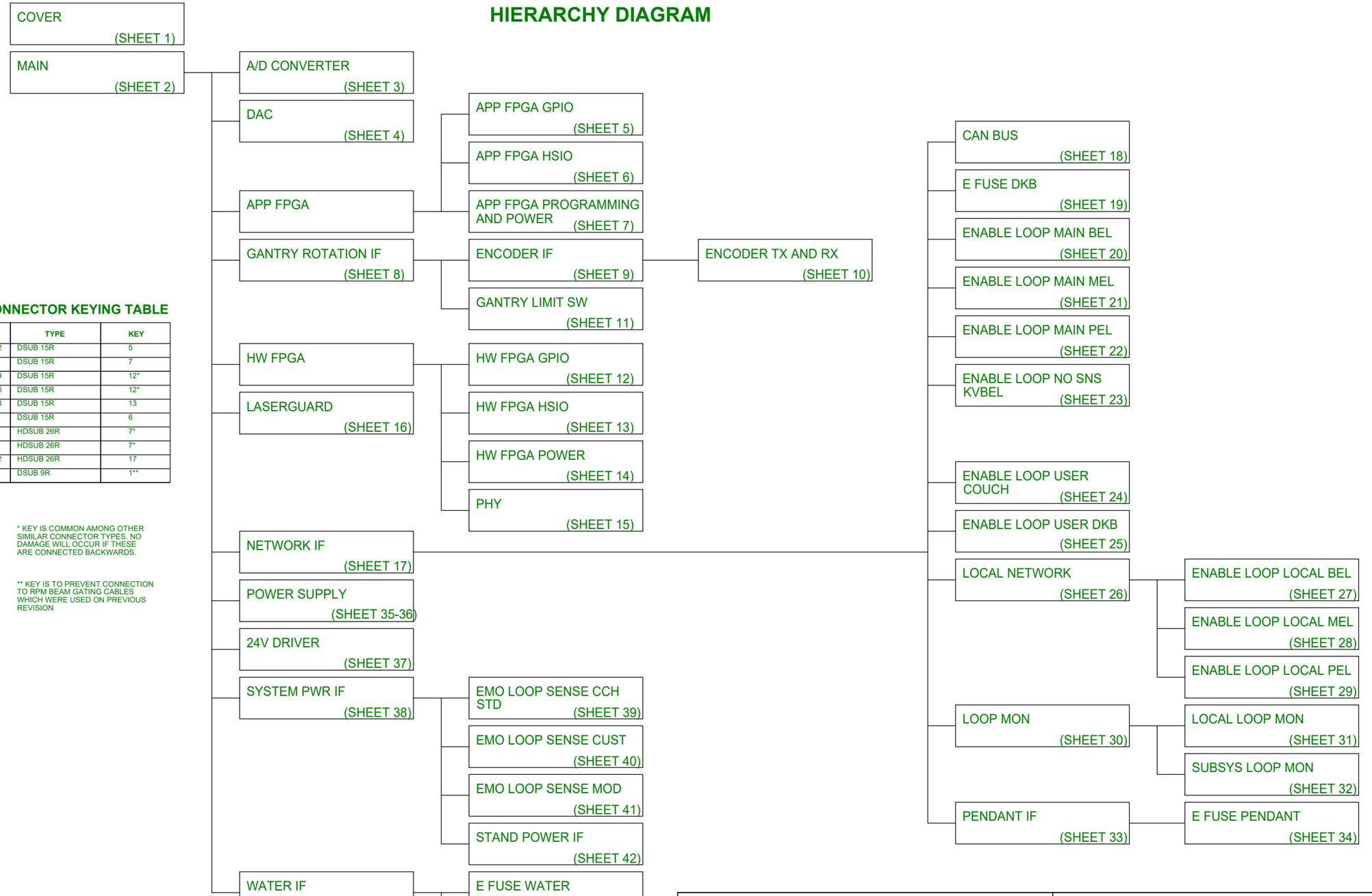
HIERARCHY DIAGRAM



CONNECTOR KEYING TABLE

Jx	TYPE	KEY
J22	DSUB 15R	5
J9	DSUB 15R	7
J29	DSUB 15R	12*
J30	DSUB 15R	12*
J28	DSUB 15R	13
J7	DSUB 15R	6
J3	HDSUB 26R	7*
J4	HDSUB 26R	7*
J12	HDSUB 26R	17
J6	DSUB 9R	1**

* KEY IS COMMON AMONG OTHER SIMILAR CONNECTOR TYPES. NO DAMAGE WILL OCCUR IF THESE ARE CONNECTED BACKWARDS.

** KEY IS TO PREVENT CONNECTION TO RPM BEAM GATING CABLES WHICH WERE USED ON PREVIOUS REVISION

SCHEMATIC DESIGN NOTES

1. ALL RESISTANCE VALUES ARE IN OHMS.

2. PARTIAL REF DES ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. & SUBASSY DESIGNATION.

3. TERMINAL NO. ARE SHOWN FOR REFERENCE ONLY & MAY NOT APPEAR ON THE COMPONENT.

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DESCRIPTION OF CHANGE

- RENUMBERED REFDES
- INCORPORATED REWORK FOR 5VISO CONTROL
- ADDED VOLTAGE MONITOR CIRCUIT FOR PEND_CURR (NO STUFFED)
- ADDED VOLTAGE MONITOR CIRCUIT FOR GANTRY_BU_24V (NO STUFFED)
- CHANGED CHOKES DLW44SM851SK2L -> PE-1210CCMC102STS
- CHANGED JTAG CONNECTORS TO SMT
- CHANGED GND TEST POINTS TO SMT

ECO	
REV	D

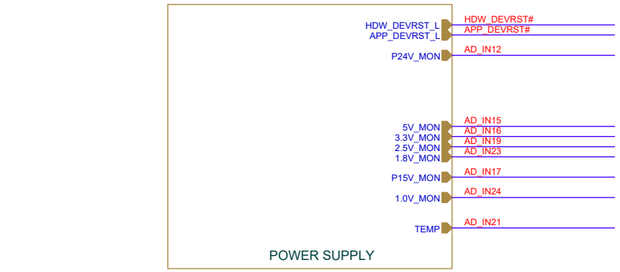
varian

TITLE:

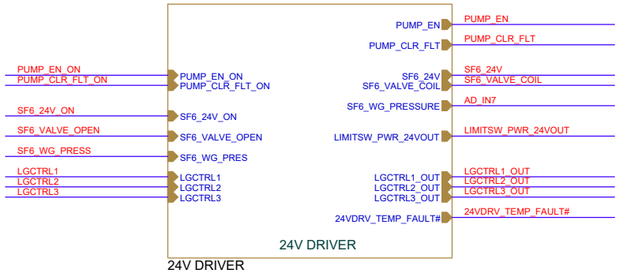
SCH, STN CONTROLLER

DRAWN: V. MANIKONDA	SHEET 1 OF 47	D	P1060967	D
DATE: 2023-05-24		ORCAD CAPTURE	SIZE	DWG NO	REV

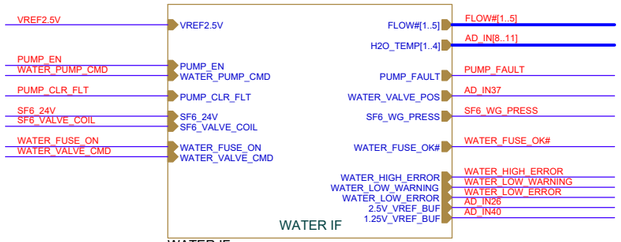
CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024



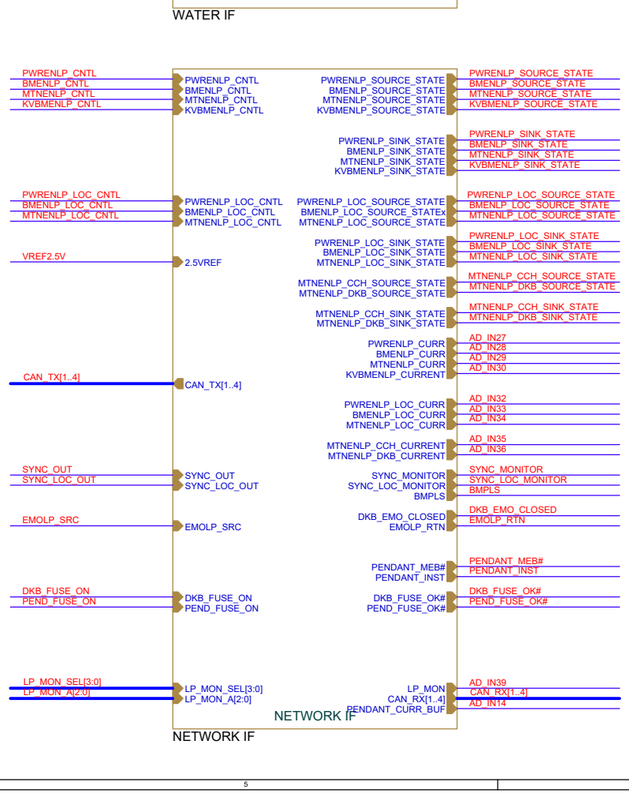
POWER SUPPLY



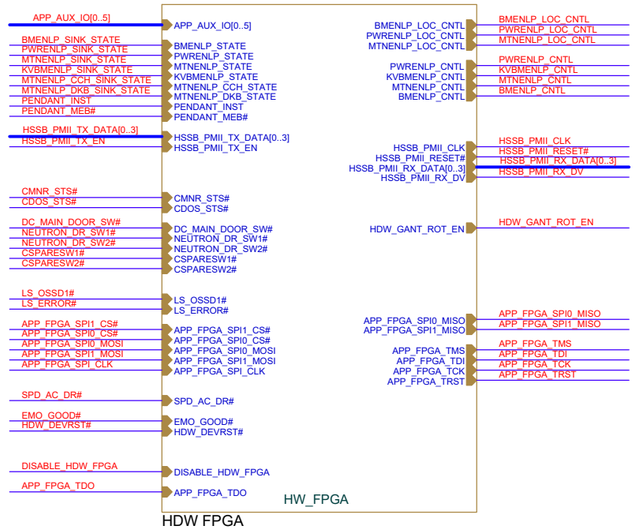
24V DRIVER



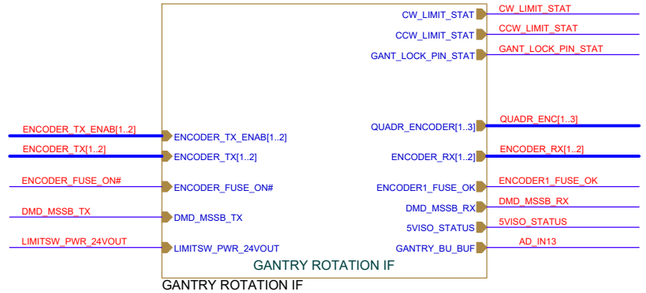
WATER IF



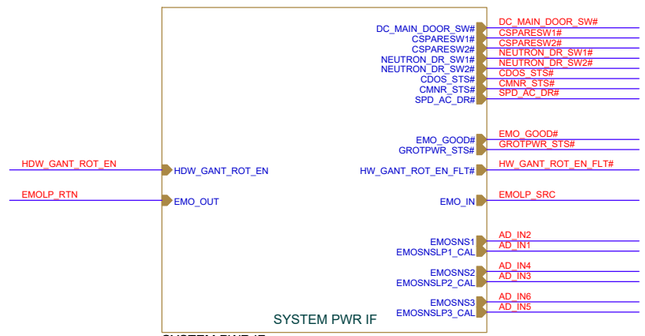
NETWORK IF



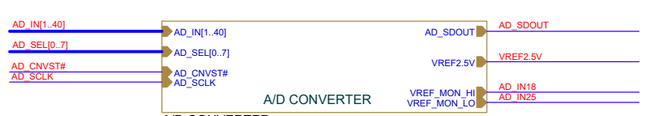
HDW FPGA



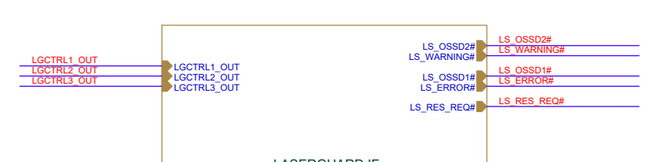
GANTRY ROTATION IF



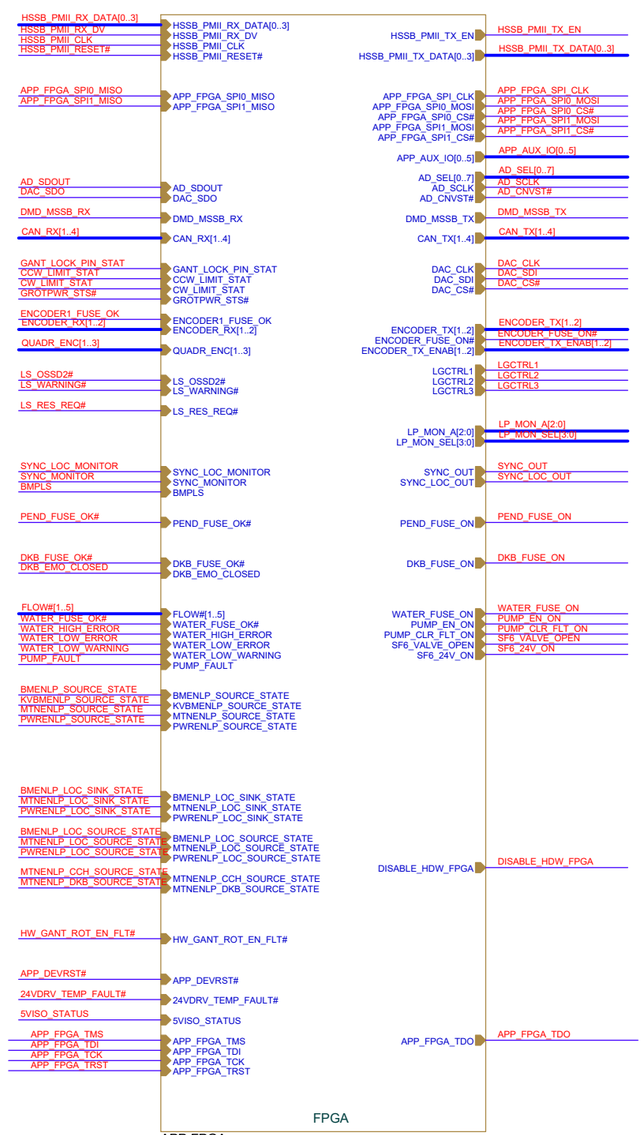
SYSTEM PWR IF



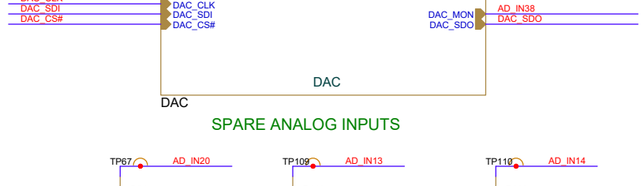
A/D CONVERTER



LASERGUARD IF

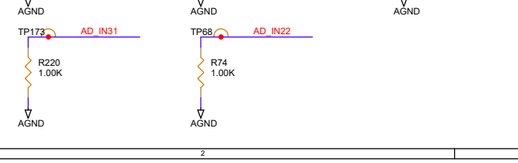


APP FPGA



DAC

SPARE ANALOG INPUTS



VARIANT01

varian

SCALE	NONE
SHEET	2 OF 47

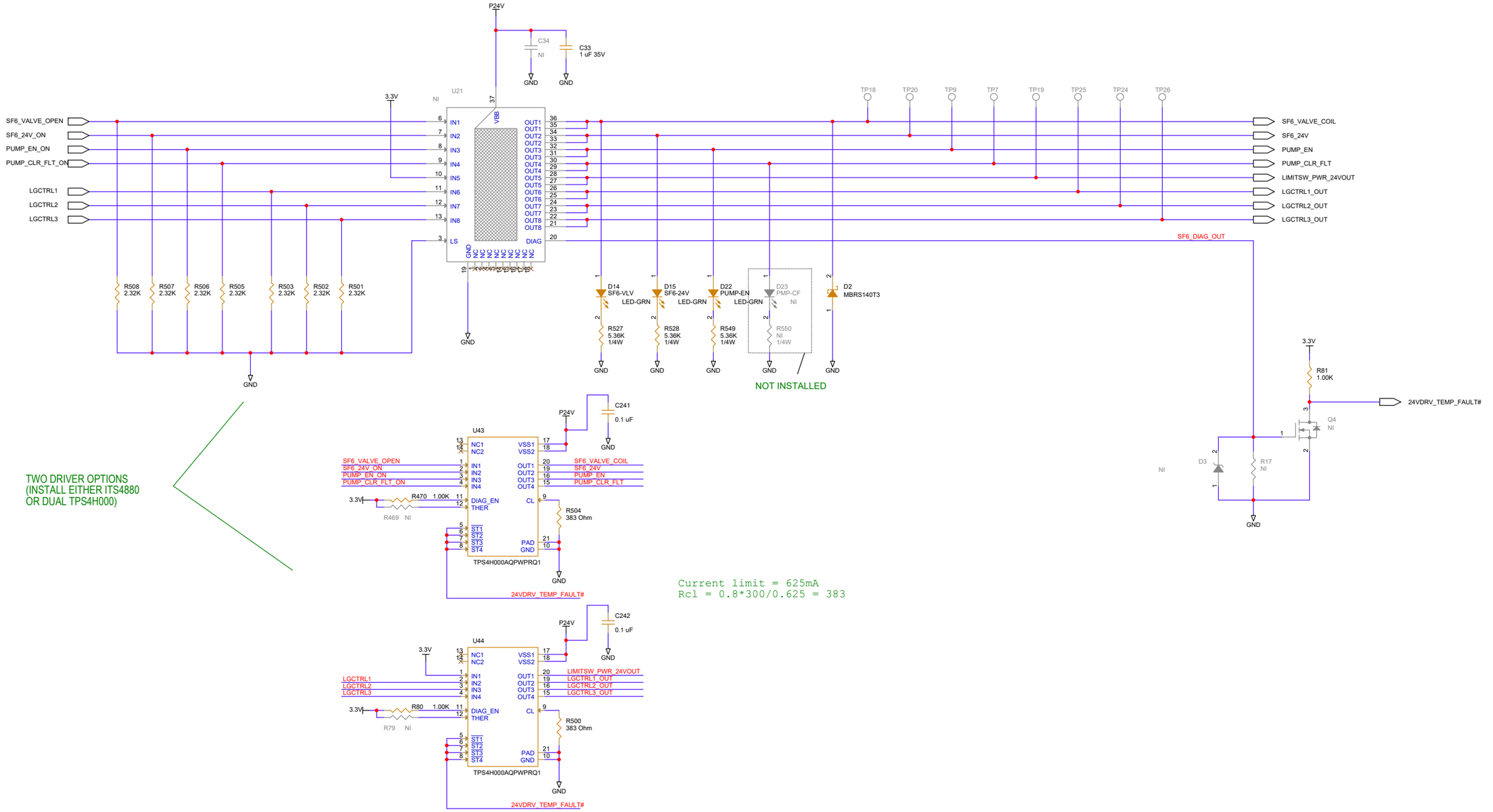
SCH, STN CONTROLLER

/ MAIN

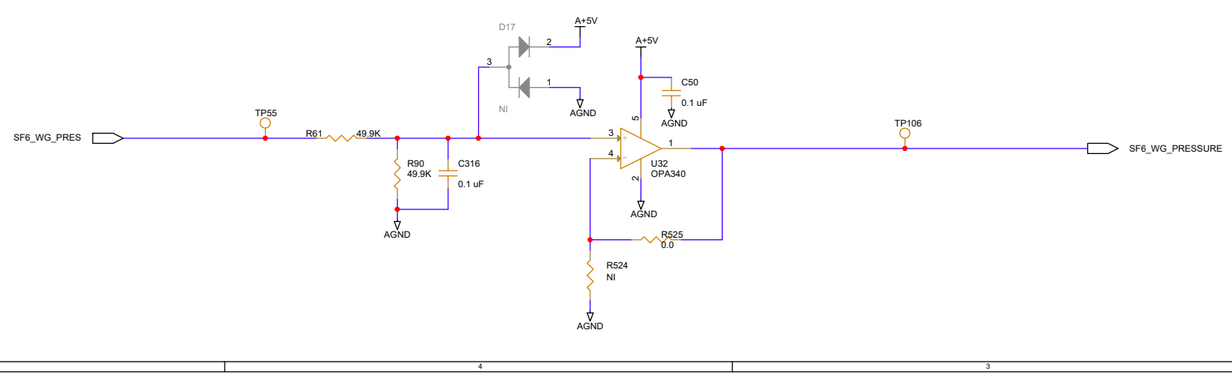
DWG NO	REV
P1060967	D

CW# 000060021312

Released Ver: 03 Rev: D 11. November 2024



SF6 Waveguide Pressure Sensor



CM# 000060021312
Released
Ver: 03
Rev: D
11. November 2024

VARIANT01

varian

SCALE	NONE
SHEET	3 OF 47

SCH, STN CONTROLLER

24V DRIVER

DWG NO	REV
P1060967	D

AD_IN[1..40]

AD_SEL[0..7]

A+5V C397 0.1 uF AGND

U80 ADG708CRU
AD_IN1 AD_IN2 AD_IN3 AD_IN4 AD_IN5 AD_IN6 AD_IN7 AD_IN8 → S1 S2 S3 S4 S5 S6 S7 S8
AD_SEL0 AD_SEL1 AD_SEL2 → A0 A1 A2
AD_SEL3 → EN
D → R221 100 Ohm
VDD 13, VSS 3, GND 14, AGND

1ST MUX ALWAYS ENABLED BEFORE FPGA IS CONFIGURED

A+5V C295 0.1 uF AGND

U42 ADG708CRU
AD_IN9 AD_IN10 AD_IN11 AD_IN12 AD_IN13 AD_IN14 AD_IN15 AD_IN16 → S1 S2 S3 S4 S5 S6 S7 S8
AD_SEL0 AD_SEL1 AD_SEL2 → A0 A1 A2
AD_SEL4 → EN
D → R115 100 Ohm
R122 2.32K GND

A+5V C243 0.1 uF AGND

U20 ADG708CRU
AD_IN17 AD_IN18 AD_IN19 AD_IN20 AD_IN21 AD_IN22 AD_IN23 AD_IN24 → S1 S2 S3 S4 S5 S6 S7 S8
AD_SEL0 AD_SEL1 AD_SEL2 → A0 A1 A2
AD_SEL5 → EN
D → R72 100 Ohm
R78 2.32K GND

A+5V C361 0.1 uF AGND

U57 ADG708CRU
AD_IN25 AD_IN26 AD_IN27 AD_IN28 AD_IN29 AD_IN30 AD_IN31 AD_IN32 → S1 S2 S3 S4 S5 S6 S7 S8
AD_SEL0 AD_SEL1 AD_SEL2 → A0 A1 A2
AD_SEL6 → EN
D → R158 100 Ohm
R164 2.32K GND

A+5V C360 0.1 uF AGND

U56 ADG708CRU
AD_IN33 AD_IN34 AD_IN35 AD_IN36 AD_IN37 AD_IN38 AD_IN39 AD_IN40 → S1 S2 S3 S4 S5 S6 S7 S8
AD_SEL0 AD_SEL1 AD_SEL2 → A0 A1 A2
AD_SEL7 → EN
D → R155 100 Ohm
R163 2.32K GND

PINS 1,2, 14-16 ON GND SIDE, OTHERS ON AGND SIDE, ALL 5 DEVICES

ADC_MUX

A+15V R476 2.00K
A+5V R65 NI
TP63

U15 LM4050AEM3-5.0/NOPB
NC
C26 10 uF
C25 10 uF AGND

R63 1.000K 0.1%
VREF_DIV
R62 1.000K 0.1% AGND

A+5V C24 NI AGND
U11 NI
TP10 VREF2.5V

R73 100.0 Ohm
VREF_MON_HI
R162 4.990K
VREF_MON_LO
R544 200.0 Ohm
C68 0.1 uF
C362 0.1 uF AGND

A+5V C23 0.1 uF AGND
U12 OPA365AIDR
DIFFERENT PACKAGE. ONLY STUFF ONE.

A+5V
R474 NI
3.3V
5V for compatibility with ADS8339
ADC_AVDD
R473 10.0 Ohm
C30 10 uF AGND
C247 0.01 uF AGND
ADC_DVDD
C3 0.01 uF GND
C197 10 uF GND
L17 HZ0805E601R

DEVICE SHOULD BE PLACED OVER SPLIT BETWEEN GND AND AGND PLANES.

A+5V C28 NI AGND
U13 NI
C29 0.01 uF AGND
ADC_REF

<0..5V>
U16
ADC_VIN
TP62
R66 60.4 Ohm
R67 60.4 Ohm
AIN_P AIN_N
C31 1000 pF
REF AVDD DVDD GND
DIN SCLK DOUT CONVST
TP65 AD_SCLK
TP66 AD_SDOUT
TP64 AD_CNVST#
NI

R64 NI
C251 NI-CAP

A+5V C27 0.1 uF AGND
U14 OPA365AIDR
DIFFERENT PACKAGE. ONLY STUFF ONE.

TWO OPTIONS FOR ADC (INSTALL ONE PART)

ADC_AVDD
ADC_REF
ADC_DVDD
U17
0..2.5V
AIN_P AIN_N
REF AVDD DVDD GND EPAD
DIN SCLK DOUT CONVST
AD_SCLK AD_SDOUT AD_CNVST#
ADS8864IDRCR

Note: Keep AD_* signals inside GND plane region. Do not route into AGND region.

VARIANT01

varian

SCALE	NONE
SHEET	4 OF 47

SCH, STN CONTROLLER
/A/D CONVERTER

DWG NO	REV
P1060967	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

INPUT SIGNALS

AD_SDOUT
BMPLS
CCW_LIMIT_STAT
CW_LIMIT_STAT
GANT_LOCK_PIN_STAT
LS_OSSD2#
LS_WARNING#
LS_RES_REQ#

APP_DEVRST#
SYNC_LOC_MONITOR
SYNC_MONITOR
DAC_SDO
DMD_MSSB_RX
GROTPWR_STS#

FLOW#[1..5]
CAN_RX[1..4]
QUADR_ENC[1..3]
ENCODER_RX[1..2]

BMENLP_LOC_SINK_STATE
BMENLP_LOC_SOURCE_STATE
BMENLP_SOURCE_STATE
KVBMENLP_SOURCE_STATE
MTNENLP_CCH_SOURCE_STATE
MTNENLP_DKB_SOURCE_STATE
MTNENLP_LOC_SINK_STATE
MTNENLP_LOC_SOURCE_STATE
MTNENLP_SOURCE_STATE
PWRENLP_LOC_SINK_STATE
PWRENLP_LOC_SOURCE_STATE
PWRENLP_SOURCE_STATE
DKB_EMO_CLOSED
DKB_FUSE_OK#
ENCODER1_FUSE_OK
HW_GANT_ROT_EN_FLT#
PEND_FUSE_OK#

24VDRV_TEMP_FAULT#

PUMP_FAULT
WATER_FUSE_OK#
WATER_HIGH_ERROR
WATER_LOW_ERROR
WATER_LOW_WARNING

5VISO_STATUS

OUTPUT SIGNALS

AD_SCLK
AD_CNVST#
PUMP_CLR_FLT_ON
SYNC_LOC_OUT
SYNC_OUT
DAC_CLK
DAC_SDI

DAC_CS#

LGCTRL1
LGCTRL2
LGCTRL3

DMD_MSSB_TX

CAN_TX[1..4]

LP_MON_A[2:0]

LP_MON_SEL[3:0]

ENCODER_TX[1..2]

ENCODER_TX_ENAB[1..2]

AD_SEL[0..7]

DKB_FUSE_ON
ENCODER_FUSE_ON#
PEND_FUSE_ON
PUMP_EN_ON
SF6_24V_ON
SF6_VALVE_OPEN
WATER_FUSE_ON
APP_DEVRST#

100MHz OSCILLATOR

3.3V
U58
VCC
OE OUT
GND
100.000MHz
ASDMB-100.000MHZ-LY-T
C70 0.1uF
GND
ST_APP_FPGA_100M_CLK
R165 33.2 Ohm
APP_FPGA_100M_CLK

LED DRIVER

3.3V
C333 0.1uF
GND
U60
SN74LVC245A/TSSOP
CAN1_LED# CAN2_LED# CAN3_LED# CAN4_LED# STAT_LED1# STAT_LED2# STAT_LED3# HEARTBEAT_LED#
CAN1_LED_BUF# CAN2_LED_BUF# CAN3_LED_BUF# CAN4_LED_BUF# STAT_LED1_BUF# STAT_LED2_BUF# STAT_LED3_BUF# HEARTBEAT_LED_BUF#
R170 4.99K

CAN1_LED_BUF# R537 392 Ohm D28 CAN SUB LED-GRN
CAN2_LED_BUF# R538 392 Ohm D29 CAN DKB LED-GRN
CAN3_LED_BUF# R539 392 Ohm D30 CAN LOC LED-GRN
CAN4_LED_BUF# R540 392 Ohm D31 CAN PEND LED-GRN
CAN LEDS

STAT_LED1_BUF# R541 392 Ohm D32 FPGA1 LED-GRN
STAT_LED2_BUF# R561 392 Ohm D40 FPGA2 LED-GRN
STAT_LED3_BUF# R562 392 Ohm D41 FPGA3 LED-GRN
FPGA STATUS LEDS

HEARTBEAT_LED_BUF# R563 392 Ohm D42 HRTBT LED-GRN

3.3V BANK

U59-9
BANK-2
MPF100T-FCG484E

AD_SCLK R227 49.9 Ohm ST_AD_SCLK
AD_CNVST# R226 49.9 Ohm ST_AD_CNVST#
AD_SDOUT
AD_SEL[0..7]
AD_SEL0 AD_SEL1 AD_SEL2 AD_SEL3 AD_SEL4 AD_SEL5 AD_SEL6 AD_SEL7
BMPLS CCW_LIMIT_STAT CW_LIMIT_STAT LS_OSSD2# LS_WARNING# GANT_LOCK_PIN_STAT LS_RES_REQ# APP_DEVRST# PUMP_CLR_FLT_ON
SYNC_LOC_MONITOR SYNC_LOC_OUT R169 49.9 Ohm ST_SYNC_LOC_OUT
SYNC_MONITOR SYNC_OUT R167 49.9 Ohm ST_SYNC_OUT
GROTPWR_STS#
BMENLP_LOC_SINK_STATE BMENLP_LOC_SOURCE_STATE BMENLP_SOURCE_STATE KVBMENLP_SOURCE_STATE MTNENLP_CCH_SOURCE_STATE MTNENLP_DKB_SOURCE_STATE MTNENLP_LOC_SINK_STATE MTNENLP_LOC_SOURCE_STATE MTNENLP_SOURCE_STATE PWRENLP_LOC_SINK_STATE PWRENLP_LOC_SOURCE_STATE PWRENLP_SOURCE_STATE
TP134 TP133

F5 E5 D4 C4 F3 E4 B4 A5 E6 D6 C5 B5 D7 C7 C6 B7 E8 D8 A6 A7 E9 D9 B8 A8 B12 B13 C9 C10 B9 B10 C11 C12 A10 A11 A12 A13 G12 G13 F10 E10 D11 D12

GPIO00PB2 GPIO00NB2
GPIO01PB2 GPIO01NB2
GPIO02PB2/DQS GPIO02NB2/DQS
GPIO03PB2 GPIO03NB2
GPIO04PB2 GPIO04NB2
GPIO05PB2 GPIO05NB2
GPIO06PB2 GPIO06NB2
GPIO07PB2 GPIO07NB2
GPIO08PB2/DQS GPIO08NB2/DQS
GPIO09PB2 GPIO09NB2
GPIO10PB2 GPIO10NB2
GPIO11PB2 GPIO11NB2
GPIO12PB2/CLKIN_S_4 GPIO12NB2
GPIO13PB2/CLKIN_S_5 GPIO13NB2
GPIO14PB2/DQS GPIO14NB2/DQS
GPIO15PB2/CLKIN_S_6 GPIO15NB2
GPIO16PB2/LPRB_A GPIO16NB2/LPRB_B
GPIO17PB2/CLKIN_S_7 GPIO17NB2
GPIO24PB2 GPIO24NB2
GPIO25PB2 GPIO25NB2
GPIO26PB2/DQS GPIO26NB2/DQS

F13 ST_DAC_CLK R166 49.9 Ohm DAC_CLK
F12 DAC_SDI
E11 DAC_CS#
F11 DAC_SDO
E13 D13 FLOW#1
E14 FLOW#2
D14 FLOW#3
C14 FLOW#4
C15 FLOW#5
A17 LGCTRL1
B17 LGCTRL2
B14 LGCTRL3
B15 24VDRV_TEMP_FAULT#
C16 C17
A15 LP_MON_A0
A16 LP_MON_A1
G14 LP_MON_A2
H13 LP_MON_SEL0
H15 LP_MON_SEL1
G15 LP_MON_SEL2
D16 LP_MON_SEL3
D17
E15 APP_FPGA_100M_CLK
E16
G17 DKB_EMO_CLOSED
F17 DKB_FUSE_OK#
F15 ENCODER1_FUSE_OK
F16 HW_GANT_ROT_EN_FLT#
E1 PEND_FUSE_OK#
D1
D2
C2 PUMP_FAULT
C1 WATER_HIGH_ERROR
B1 WATER_FUSE_OK#
A2 WATER_LOW_ERROR
A3 WATER_LOW_WARNING
E3 TP183
D3 TP182
B2 TP181
B3 TP180

FLOW#[1..5]
LP_MON_A[2:0]
LP_MON_SEL[3:0]

GPIO27PB2 GPIO27NB2
GPIO28PB2 GPIO28NB2
GPIO29NB2 GPIO29PB2
GPIO30NB2 GPIO30PB2
GPIO31PB2 GPIO31NB2
GPIO32PB2/DQS/CCC_SE_PLL0_OUT0 GPIO32NB2/DQS
GPIO33PB2/CLKIN_S_8/CCC_SE_CLKIN_S_8/CCC_SE_PLL0_OUT0 GPIO33NB2
GPIO34PB2/CCC_SE_PLL0_OUT1 GPIO34NB2
GPIO35PB2/CLKIN_S_9/CCC_SE_CLKIN_S_9 GPIO35NB2
GPIO36PB2 GPIO36NB2
GPIO37PB2 GPIO37NB2
GPIO38PB2/DQS/CCC_SE_PLL1_OUT0 GPIO38NB2/DQS
GPIO39PB2/CCC_SE_CLKIN_S_10/CCC_SE_PLL1_OUT0 GPIO39NB2
GPIO40PB2/CCC_SE_PLL1_OUT1 GPIO40NB2
GPIO41PB2/CCC_SE_CLKIN_S_11 GPIO41NB2
GPIO142PB2/CCC_SW_CLKIN_S_0 GPIO142NB2
GPIO143PB2/CCC_SW_CLKIN_S_1 GPIO143NB2
GPIO144PB2/DQS/CCC_SW_PLL1_OUT0 GPIO144NB2/DQS
GPIO145PB2/CLKIN_S_2/CCC_SW_CLKIN_S_2/CCC_SW_PLL1_OUT0 GPIO145NB2
GPIO146PB2/CCC_SW_PLL1_OUT1 GPIO146NB2
GPIO147PB2/CLKIN_S_3/CCC_SW_CLKIN_S_3 GPIO147NB2

3.3V BANK

U59-10
BANK-4
MPF100T-FCG484E

CAN_TX[1..4]
CAN_TX1 CAN_TX2 CAN_TX3 CAN_TX4
CAN_RX[1..4]
CAN_RX1 CAN_RX2 CAN_RX3 CAN_RX4
QUADR_ENC[1..3]
QUADR_ENC1 PRI_QUADR_A QUADR_ENC2 PRI_QUADR_B QUADR_ENC3 PRI_QUADR_I
STAT_LED1# STAT_LED2# STAT_LED3# HEARTBEAT_LED# ENCODER_FUSE_ON# FPGA_DONE PUMP_EN_ON SF6_24V_ON SF6_VALVE_OPEN WATER_FUSE_ON DKB_FUSE_ON PEND_FUSE_ON 5VISO_STATUS
TP198 TP199 TP202 TP196

R1 T1 N1 P1 N2 P2 T5 T6 P4 R3 T2 T3 N4 P3 R5 R4 P9 R8 P6 R6 P7 P8 N7 N8 N6 N5 M8 M9 M3 M2 L7 L8

GPIO108PB4/CLKIN_W_7/CCC_NW_CLKIN_W_7/CCC_NW_PLL0_OUT0 GPIO108NB4
GPIO109PB4/DQS GPIO109NB4/DQS
GPIO112PB4 GPIO112NB4
GPIO113PB4 GPIO113NB4
GPIO114PB4/CLKIN_W_6/CCC_NW_CLKIN_W_6/CCC_NW_PLL0_OUT1 GPIO114NB4
GPIO115PB4/DQS/CCC_NW_PLL0_OUT0 GPIO115NB4/DQS
GPIO116PB4 GPIO116NB4
GPIO117PB4 GPIO117NB4
GPIO118PB4 GPIO118NB4
GPIO119PB4 GPIO119NB4
GPIO120PB4 GPIO120NB4
GPIO121PB4/DQS GPIO121NB4/DQS
GPIO122PB4 GPIO122NB4
GPIO123PB4 GPIO123NB4
GPIO124PB4 GPIO124NB4
GPIO125PB4 GPIO125NB4

L6 ST_DMD_MSSB_TX
M7 DMD_MSSB_RX
R230 33.2 Ohm DMD_MSSB_TX
K5 TP190
K4 TP192
L3 TP203
M4 TP201
L5 TP189
M5 TP199
K1 TP193
L1 TP200
J3 ENCODER_RX1
J2 SEC_ENDAT_RX ENCODER_RX2
K3 SEC_ENDAT_CLK ENCODER_TX1
L2 SEC_ENDAT_TX ENCODER_TX2
H1 ENCODER_TX_ENAB1
J1 SEC_ENDAT_TXEN ENCODER_TX_ENAB2
F2
F1
G2
H2
J6 CAN1_LED#
K6 CAN2_LED#
H7 CAN3_LED#
J7 CAN4_LED#
J8 TP184
K8 TP197
H4 TP191
J4 TP194
H6 TP187
H5 TP186
J9 TP185
K9 TP188

ENCODER_RX[1..2]
ENCODER_TX[1..2]
ENCODER_TX_ENAB[1..2]

GPIO126PB4 GPIO126NB4
GPIO127PB4/DQS GPIO127NB4/DQS
GPIO128PB4 GPIO128NB4
GPIO129PB4 GPIO129NB4
GPIO130PB4 GPIO130NB4
GPIO131PB4/CLKIN_W_5/CCC_NW_CLKIN_W_5 GPIO131NB4
GPIO132PB4/CLKIN_W_4/CCC_NW_CLKIN_W_4 GPIO132NB4
GPIO133PB4/DQS GPIO133NB4/DQS
GPIO134PB4 GPIO134NB4
GPIO135PB4/CLKIN_W_3/CCC_SW_CLKIN_W_3 GPIO135NB4
GPIO136PB4/CCC_SW_PLL0_OUT1 GPIO136NB4
GPIO137PB4/CLKIN_W_2/CCC_SW_CLKIN_W_2/CCC_SW_PLL0_OUT0 GPIO137NB4
GPIO138PB4/CLKIN_W_1/CCC_SW_CLKIN_W_1 GPIO138NB4
GPIO139PB4/DQS/CCC_SW_PLL0_OUT0 GPIO139NB4/DQS
GPIO140PB4 GPIO140NB4
GPIO141PB4/CLKIN_W_0/CCC_SW_CLKIN_W_0 GPIO141NB4

R564 392 Ohm D43 FPGA DONE LED-GRN
GND

VARIANT01

varian	SCALE NONE
	SHEET 5 OF 47
SCH, STN CONTROLLER	
/FPGA APP FPGA GPIO	
DWG NO P1060967	REV D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

INPUT SIGNALS

HSSB_PMII_RX_DATA[0..3] → HSSB_PMII_RX_DATA[0..3]
APP_FPGA_SPI0_MISO → APP_FPGA_SPI0_MISO
APP_FPGA_SPI1_MISO → APP_FPGA_SPI1_MISO
HSSB_PMII_RX_DV → HSSB_PMII_RX_DV
HSSB_PMII_CLK → HSSB_PMII_CLK
HSSB_PMII_RESET# → HSSB_PMII_RESET#

OUTPUT SIGNALS

HSSB_PMII_TX_DATA[0..3] → HSSB_PMII_TX_DATA[0..3]
APP_AUX_IO[0..5] → APP_AUX_IO[0..5]
HSSB_PMII_TX_EN → HSSB_PMII_TX_EN
APP_FPGA_SPI_CLK → APP_FPGA_SPI_CLK
APP_FPGA_SPI0_CS# → APP_FPGA_SPI0_CS#
APP_FPGA_SPI0_MOSI → APP_FPGA_SPI0_MOSI
APP_FPGA_SPI1_CS# → APP_FPGA_SPI1_CS#
APP_FPGA_SPI1_MOSI → APP_FPGA_SPI1_MOSI
DISABLE_HDW_FPGA → DISABLE_HDW_FPGA

DEBUG CONNECTOR

1.8V
R232 2.32K
J40
APP_DBUG_HEADER2 2 | 1 APP_DBUG_SCLK
APP_DBUG_HEADER4 4 | 3 APP_DBUG_MISO
APP_DBUG_HEADER6 6 | 5 APP_DBUG_MOSI
APP_DBUG_HEADER8 8 | 7 APP_DBUG_CS#
APP_DBUG_HEADER10 10 | 9 APP_DBUG_ACTIVE
12 | 11
GND GND
HEADER 6x2/SM
R231 2.32K
GND

1.8V BANK

U59-7
BANK-0
MPF100T-FCG484E

HSSB_PMII_TX_DATA[0..3]
HSSB_PMII_RX_DATA[0..3]

W9 HSIO78PB0/CLKIN_N_5 — HSSB_PMII_CLK
Y9 HSIO78NB0 — HSSB_PMII_RESET#
V9 HSIO79PB0 — HSSB_PMII_TX_DATA0
V10 HSIO79NB0 — HSSB_PMII_TX_DATA1
R9 HSIO80PB0/CLKIN_N_4 — HSSB_PMII_TX_DATA2
R10 HSIO80NB0 — HSSB_PMII_TX_DATA3
T10 HSIO81PB0/DQS — HSSB_PMII_TX_EN
U10 HSIO81NB0/DQS — HSSB_PMII_RX_DV
U8 HSIO82PB0 — HSSB_PMII_RX_DATA0
U9 HSIO82NB0 — HSSB_PMII_RX_DATA1
T7 HSIO83PB0 — HSSB_PMII_RX_DATA2
T8 HSIO83NB0 — HSSB_PMII_RX_DATA3
AA8 HSIO90PB0
Y8 HSIO90NB0
AA7 HSIO91PB0
AB7 HSIO91NB0
W7 HSIO92PB0
W8 HSIO92NB0
AA5 HSIO93PB0/DQS
AB5 HSIO93NB0/DQS
Y6 HSIO94PB0 — TP138 TP138
AA6 HSIO94NB0
U7 HSIO95PB0 — TP139 TP137
V7 HSIO95NB0

AB3 HSIO96PB0
AB4 HSIO96NB0
V6 HSIO97PB0
W6 HSIO97NB0 — APP_DBUG_HEADER2
AA2 HSIO98PB0 — APP_DBUG_HEADER4
AB2 HSIO98NB0 — APP_DBUG_HEADER6
Y4 HSIO99PB0/DQS — APP_DBUG_HEADER8
Y5 HSIO99NB0/DQS — APP_DBUG_HEADER10
Y3 HSIO100PB0 — APP_DBUG_CS#
AA3 HSIO100NB0 — APP_DBUG_ACTIVE
V5 HSIO101PB0 — APP_DBUG_MOSI
W4 HSIO101NB0 — APP_DBUG_MISO
Y1 HSIO102PB0/CLKIN_N_3/CCC_NW_CLKIN_N_3 — APP_DBUG_SCLK
AA1 HSIO102NB0
V4 HSIO103PB0/CCC_NW_PLL1_OUT1
W3 HSIO103NB0
V1 HSIO104PB0/CLKIN_N_2/CCC_NW_CLKIN_N_2/CCC_NW_PLL1_OUT0
W1 HSIO104NB0
V2 HSIO105PB0/DQS/CCC_NW_PLL1_OUT0
W2 HSIO105NB0/DQS
U3 HSIO106PB0/CCC_NW_CLKIN_N_1 — TP207 TP207
U2 HSIO106NB0 — TP208 TP208
U5 HSIO107PB0/CCC_NW_CLKIN_N_0 — TP206 TP204
U4 HSIO107NB0

1.8V BANK

U59-8
BANK-1
MPF100T-FCG484E

APP_FPGA_SPI_CLK T17 — HSIO42PB1/CCC_NE_CLKIN_N_11
APP_FPGA_SPI0_CS# U17 — HSIO42NB1
APP_FPGA_SPI0_MOSI V16 — HSIO43PB1/CCC_NE_PLL0_OUT1
APP_FPGA_SPI0_MISO W16 — HSIO43NB1
APP_FPGA_SPI1_CS# W17 — HSIO44PB1/CCC_NE_CLKIN_N_10/CCC_NE_PLL0_OUT0
APP_FPGA_SPI1_MOSI V17 — HSIO44NB1
APP_FPGA_SPI1_MISO AB17 — HSIO45PB1/DQS/CCC_NE_PLL0_OUT0
AA17 HSIO45NB1/DQS
AA16 HSIO46PB1
Y16 HSIO46NB1
T16 HSIO47PB1
R16 HSIO47NB1
Y15 HSIO48PB1/CLKIN_N_9/CCC_NE_CLKIN_N_9
AA15 HSIO48NB1
W14 HSIO49PB1/CCC_NE_PLL1_OUT1
Y14 HSIO49NB1
AB14 HSIO50PB1/CLKIN_N_8/CCC_NE_CLKIN_N_8/CCC_NE_PLL1_OUT0
AB15 HSIO50NB1
AA12 HSIO51PB1/DQS/CCC_NE_PLL1_OUT0
AB12 HSIO51NB1/DQS
TP120 AA13 HSIO52PB1 — TP120
TP121 AB13 HSIO52NB1 — TP121
TP119 W13 HSIO53PB1 — TP119
TP118 Y13 HSIO53NB1 — TP118

AA10 HSIO54PB1 — APP_AUX_IO0
AB10 HSIO54NB1 — APP_AUX_IO1
Y11 HSIO55PB1 — APP_AUX_IO2
AA11 HSIO55NB1 — APP_AUX_IO3
V12 HSIO56PB1 — APP_AUX_IO4
W12 HSIO56NB1 — APP_AUX_IO5
AB8 HSIO57PB1/DQS — DISABLE_HDW_FPGA
AB9 HSIO57NB1/DQS
W11 HSIO58PB1
Y10 HSIO58NB1
U12 HSIO59PB1
V11 HSIO59NB1
T15 HSIO66PB1/CLKIN_N_7
R15 HSIO66NB1
T13 HSIO67PB1
U13 HSIO67NB1
V15 HSIO68PB1/CLKIN_N_6
U15 HSIO68NB1
R13 HSIO69PB1/DQS
T12 HSIO69NB1/DQS
R12 HSIO70PB1 — TP113 TP113
T11 HSIO70NB1 — TP114 TP114
V14 HSIO71PB1 — TP117 TP117
U14 HSIO71NB1 — TP116 TP116

XCVR-0

U59-1
MPF100T-FCG484E

M22 M21 XCVR_0_RX0_P XCVR_0_RX0_N
T22 T21 XCVR_0_RX1_P XCVR_0_RX1_N
W20 W19 XCVR_0_RX2_P XCVR_0_RX2_N
AA20 AA19 XCVR_0_RX3_P XCVR_0_RX3_N
R19 R20 XCVR_0A_REFCLK_P XCVR_0A_REFCLK_N
XCVR_0_TX0_P P22 XCVR_0_TX0_N P21
XCVR_0_TX1_P V22 XCVR_0_TX1_N V21
XCVR_0_TX2_P Y22 XCVR_0_TX2_N Y21
XCVR_0_TX3_P AB22 XCVR_0_TX3_N AB21

XCVR-1

U59-2
MPF100T-FCG484E

A20 A19 XCVR_1_RX0_P XCVR_1_RX0_N
C20 C19 XCVR_1_RX1_P XCVR_1_RX1_N
F22 F21 XCVR_1_RX2_P XCVR_1_RX2_N
L20 L19 XCVR_1_RX3_P XCVR_1_RX3_N
G19 G20 XCVR_1A_REFCLK_P XCVR_1A_REFCLK_N
XCVR_1_TX0_P B22 XCVR_1_TX0_N B21
XCVR_1_TX1_P D22 XCVR_1_TX1_N D21
XCVR_1_TX2_P H22 XCVR_1_TX2_N H21
XCVR_1_TX3_P K22 XCVR_1_TX3_N K21

XCVR EXTERNAL REF CLOCKS

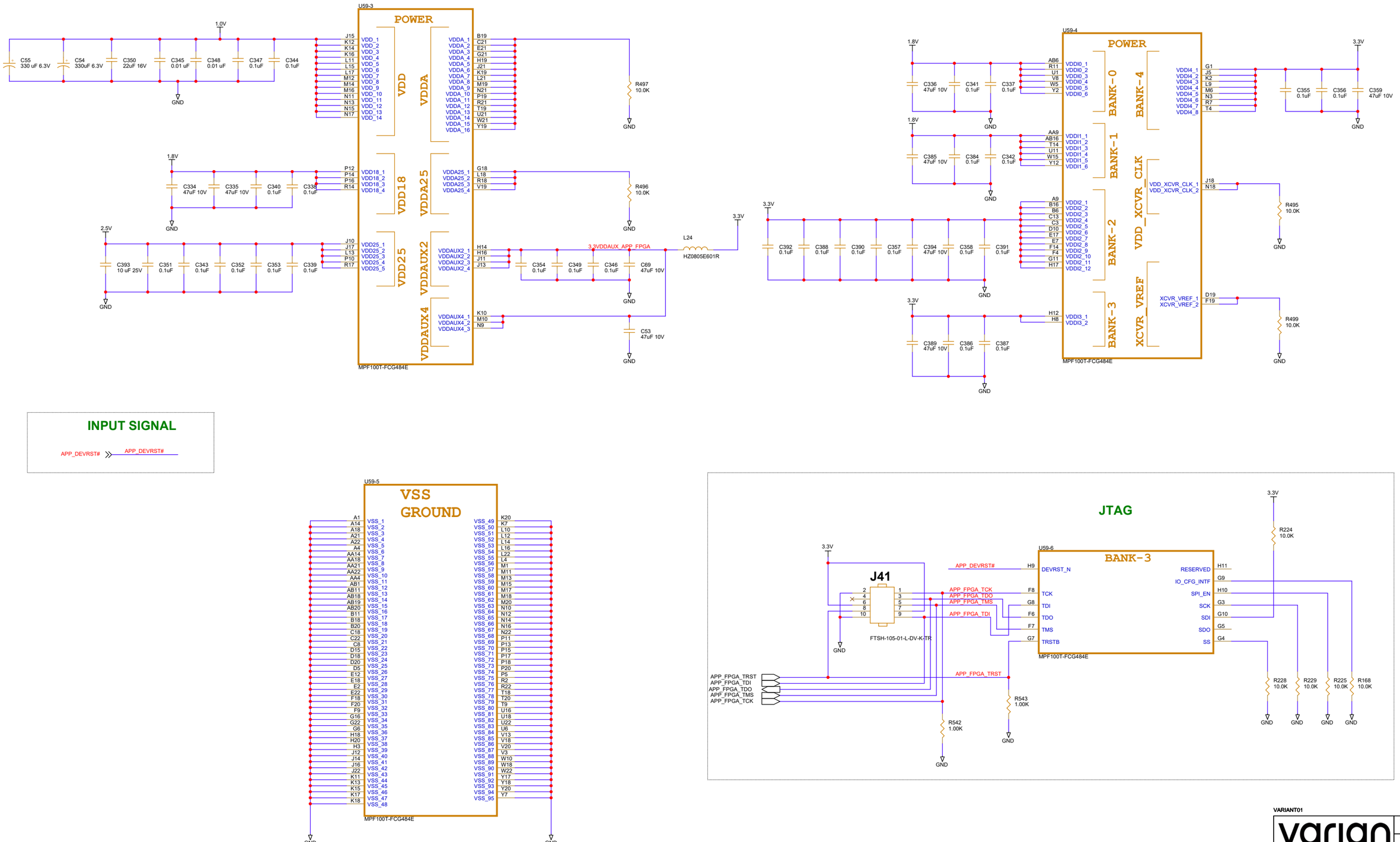
U59-11
MPF100T-FCG484E

U19 U20 XCVR_0B_REFCLK_P XCVR_0B_REFCLK_N
N19 N20 XCVR_0C_REFCLK_P XCVR_0C_REFCLK_N
XCVR_1B_REFCLK_P J19 XCVR_1B_REFCLK_N J20
XCVR_1C_REFCLK_P E19 XCVR_1C_REFCLK_N E20

VARIANT01

varian	SCALE NONE
	SHEET 6 OF 47
SCH, STN CONTROLLER	
/FPGA APP FPGA HSIO	
DWG NO P1060967	REV D

CM# 000060021312
Released
Ver: 03
Rev: D
11. November 2024



INPUT SIGNAL

APP_DEVRST# >> APP_DEVRST#

VARIANT01

varian

SCALE	NONE
SHEET	7 OF 47

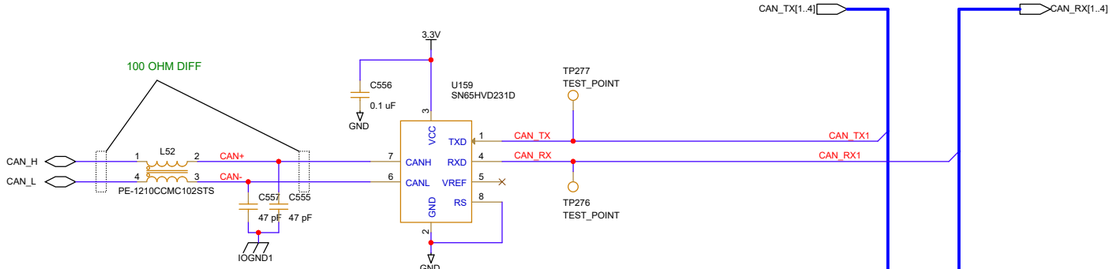
SCH, STN CONTROLLER

/FPGA APP FPGA PROGRAMMING AND POWER

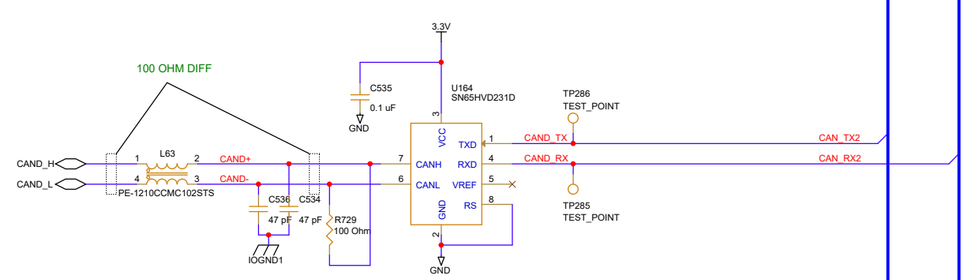
DWG NO	REV
P1060967	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

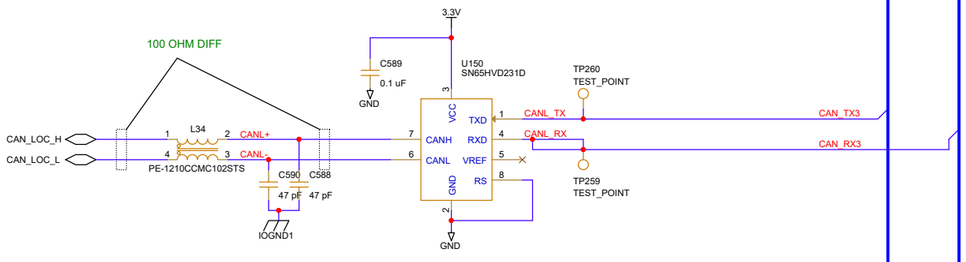
Subsystem CAN Controller



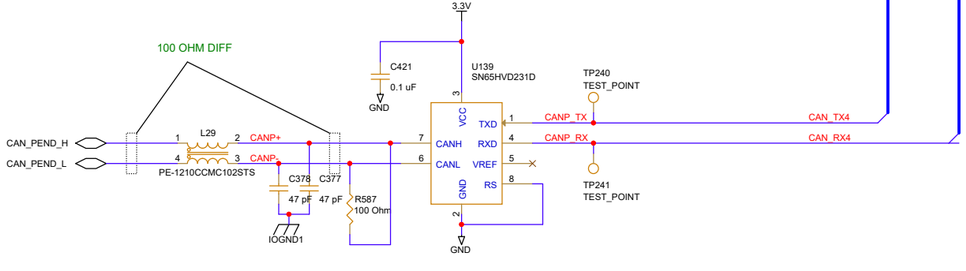
DKB Network CAN Controller



Local CAN Controller



Pendant CAN Controller

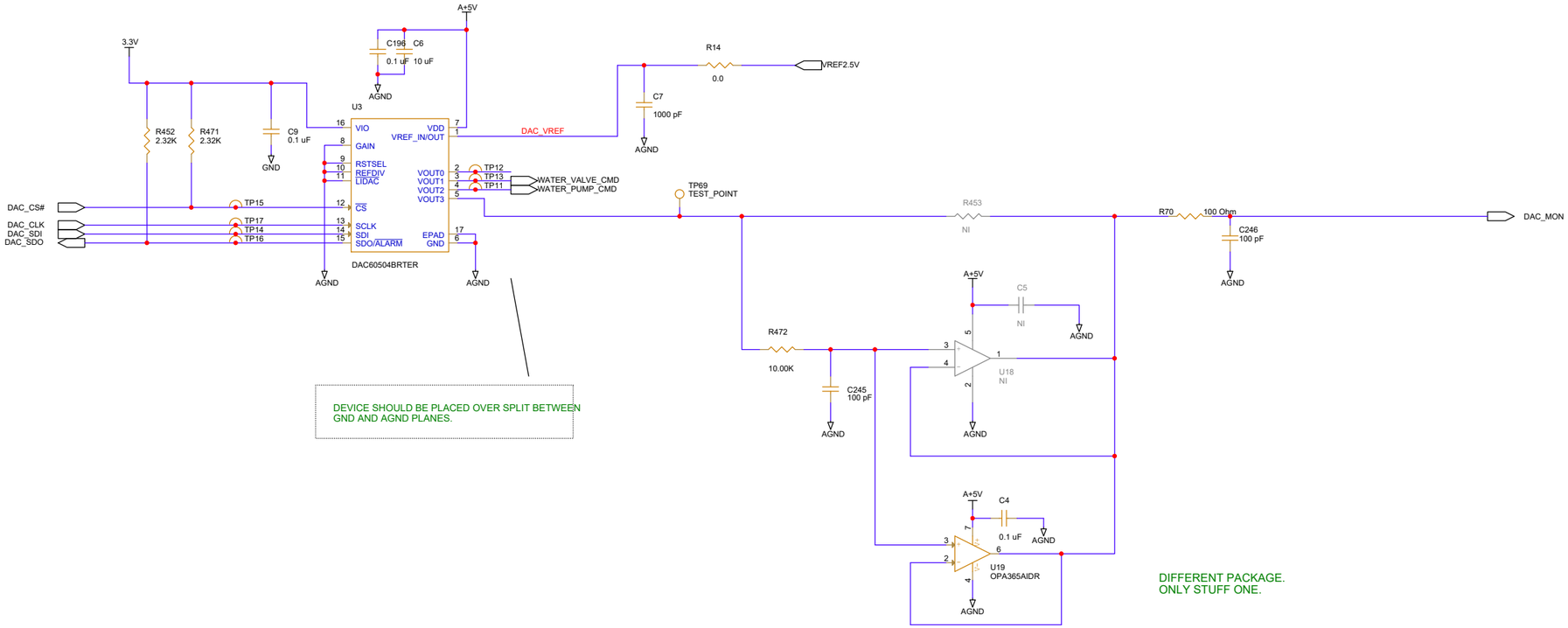


VARIANT01

varian	SCALE NONE
	SHEET 8 OF 47
SCH, STN CONTROLLER /NETWORK IF/CAN BUS	
DWG NO P1060967	REV D

CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

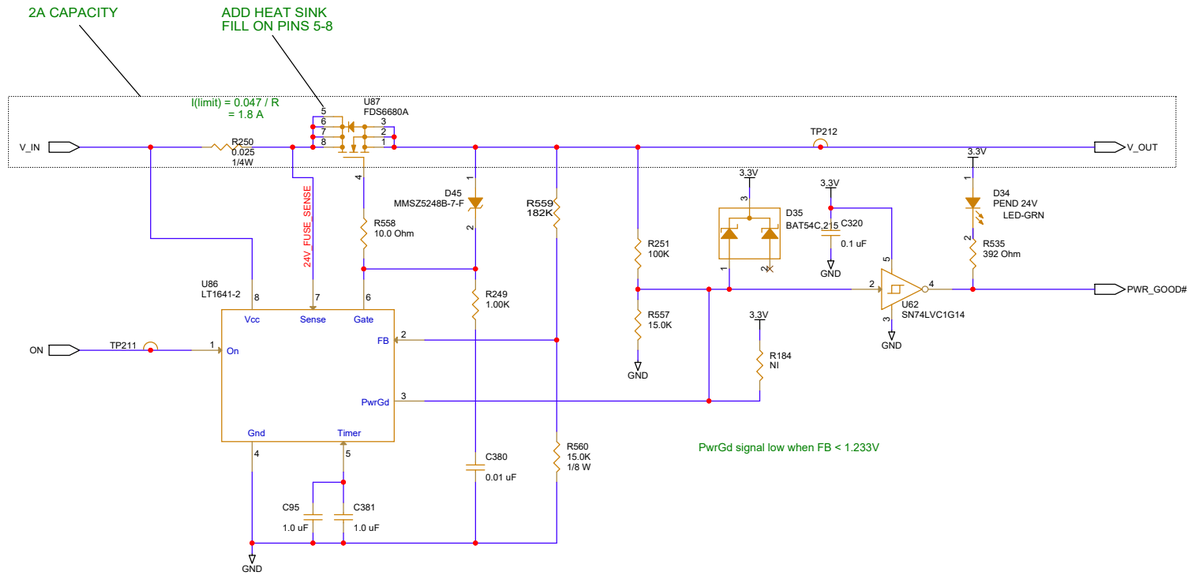
DAC



VARIANT01

varian	SCALE NONE
	SHEET 9 OF 47
SCH, STN CONTROLLER /DAC	
DWG NO P1060967	REV D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024



VARIANT01

varian

SCALE	NONE
SHEET	10 OF 47

SCH, STN CONTROLLER

/NETWORK IF/PENDANT IF/E FUSE PENDANT

DWG NO	REV
P1060967	D

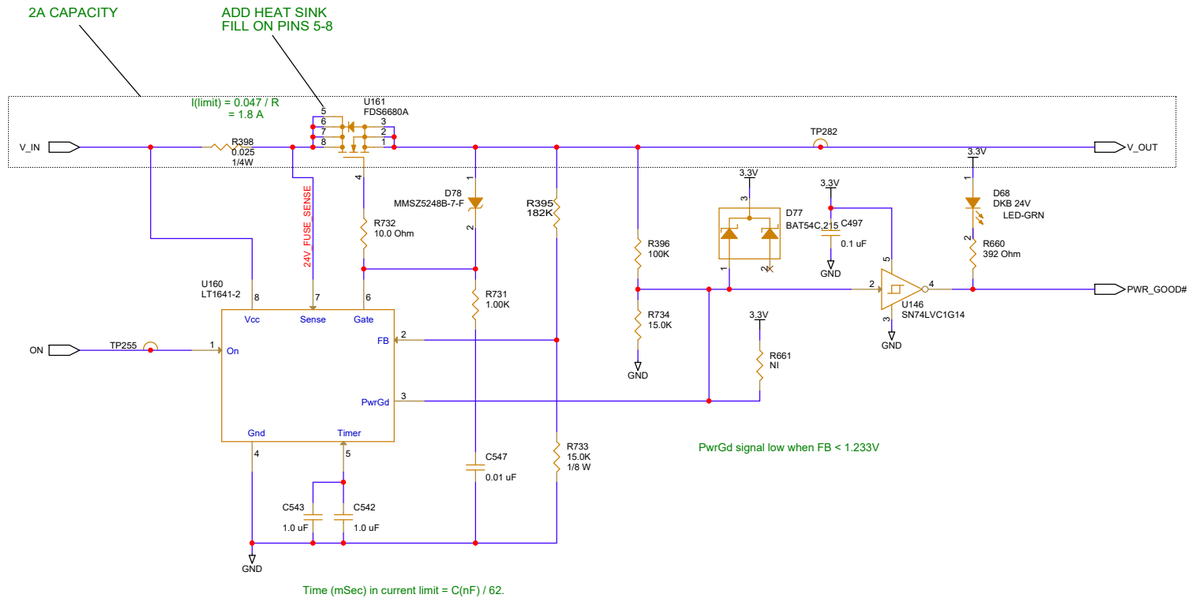
CM# 0000600021312

Released

Ver: 03

Rev: D

11. November 2024



CM# 0000600021312

Released

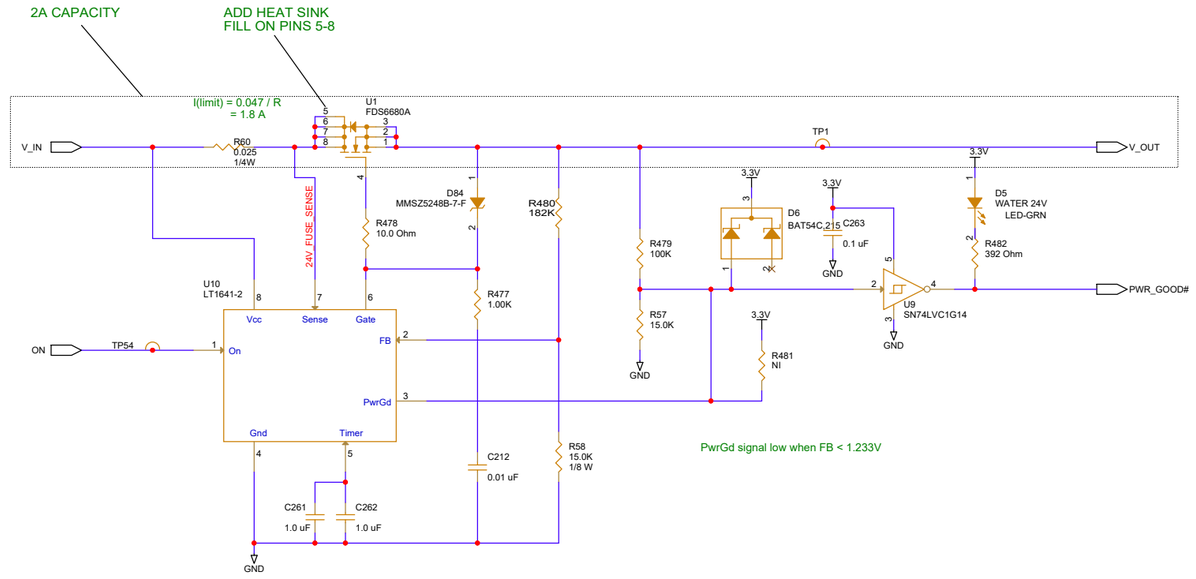
Ver: 03

Rev: D

11. November 2024

VARIANT01

varian	SCALE NONE
	SHEET 11 OF 47
SCH, STN CONTROLLER	
/NETWORK IF/E FUSE DKB	
DWG NO P1060967	REV D



VARIANT01

varian

SCALE	NONE
SHEET	12 OF 47

SCH, STN CONTROLLER

/WATER IF/E FUSE WATER

DWG NO	REV
P1060967	D

CM# 0000600021312

Released

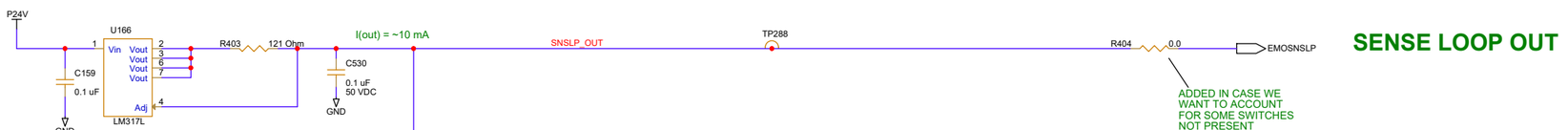
Ver: 03

Rev: D

11. November 2024

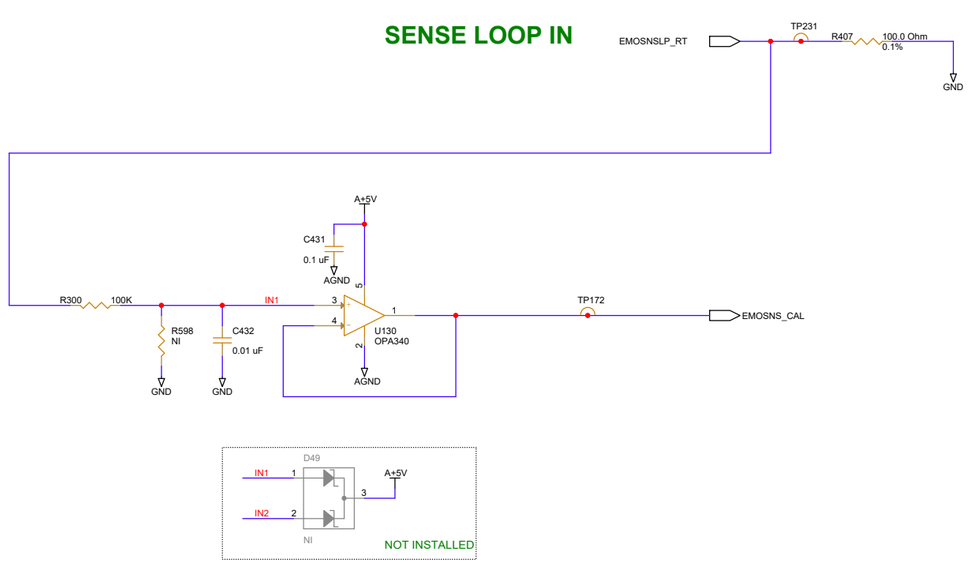
EMO Sense Loop:
Up to 4 EMO buttons in series.
Activated button shorts resistor in EMOSNSLP line.

Circuit is configured for external resistor values: 42.2, 84.5, 169, 340



SENSE LOOP OUT

SENSE LOOP IN



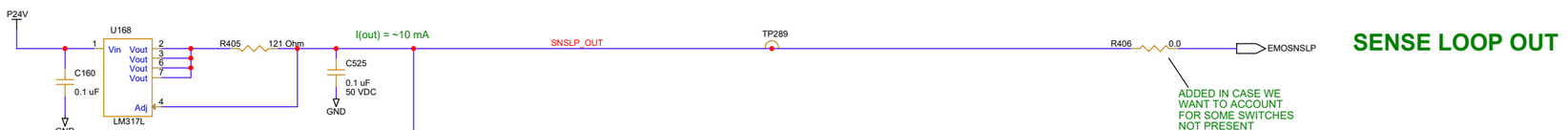
VARIANT01

varian	SCALE NONE
	SHEET 13 OF 47
SCH, STN CONTROLLER	
/SYSTEM PWR IF/EMO LOOP SENSE CCH STD	
DWG NO P1060967	REV D

CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

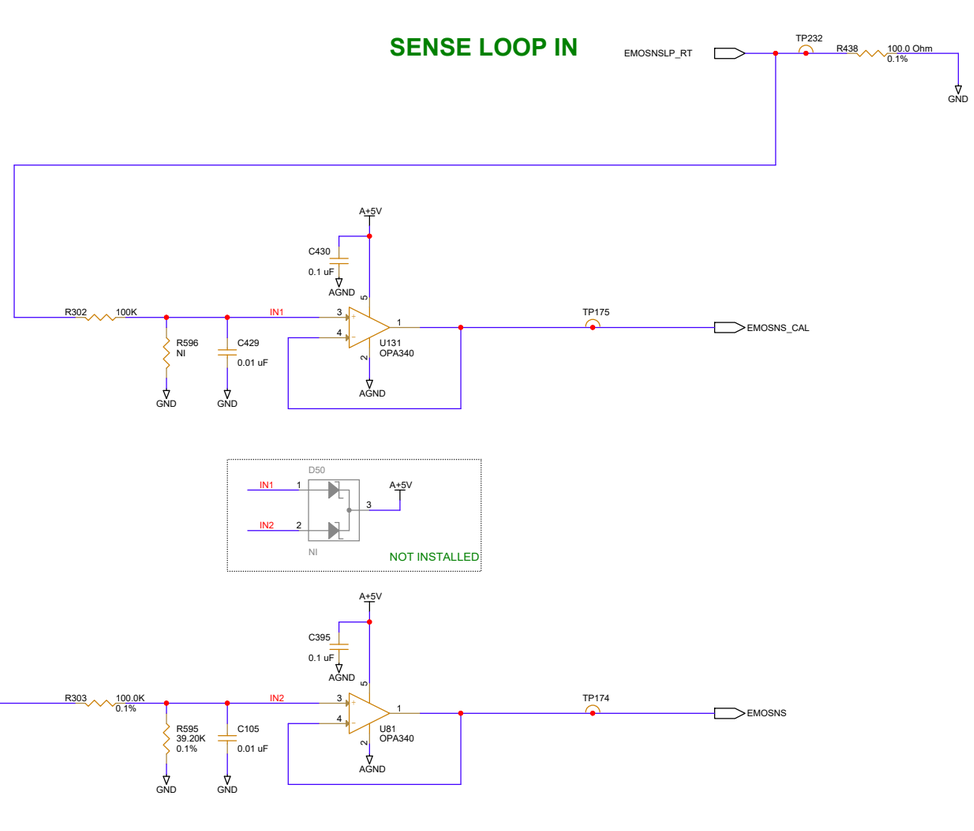
EMO Sense Loop:
Up to 4 EMO buttons in series.
Activated button shorts resistor in EMOSNSLP line.

Circuit is configured for external resistor values: 42.2, 84.5, 169, 340



SENSE LOOP OUT

SENSE LOOP IN



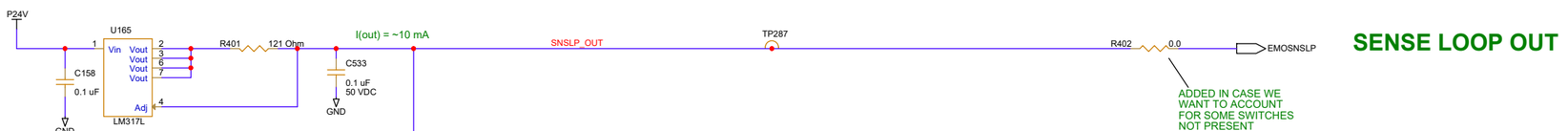
VARIANT01

varian	SCALE NONE
	SHEET 14 OF 47
SCH, STN CONTROLLER	
/SYSTEM PWR IF/EMO LOOP SENSE CUST	
DWG NO P1060967	REV D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

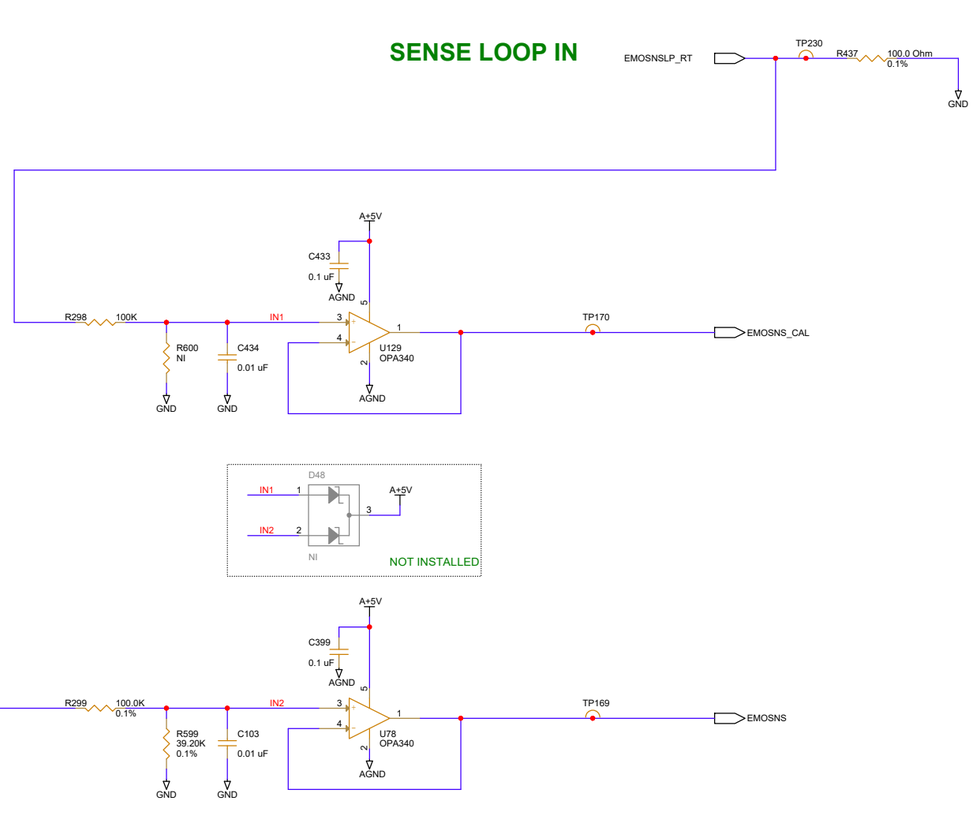
EMO Sense Loop:
Up to 4 EMO buttons in series.
Activated button shorts resistor in EMOSNSLP line.

Circuit is configured for external resistor values: 42.2, 84.5, 169, 340



SENSE LOOP OUT

SENSE LOOP IN



VARIANT01

varian	SCALE NONE
	SHEET 15 OF 47
SCH, STN CONTROLLER /SYSTEM PWR IF/EMO LOOP SENSE MOD	
DWG NO P1060967	REV D

CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

10mA CURRENT SOURCE

P24V
C129 0.1 uF
GND
U151 LM317L (Vin, Vout, Vout, Vout, Vout, Adj)
R369 121 Ohm
R765 10.0 Ohm

LOOP CONTROL SWITCH

R767 NI
TP262
TP261
Q23 FDN5618P
R764 200K
R766 200K
Q42 BSS138
ENLP_CNTL
R679 392 Ohm
R690 4.99K
D54 LOC BEL CMD LED-GRN
GND
ENLP_OUT

ENABLE LOOP OUT

ROUTE TOGETHER

SOURCE SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

A+5V
U93 INA193AIDBVT
SRC+
SRC-
AGND
C478 0.1 uF
TP215
R645 37.4K
ENLP_SOURCE_REF
R266 1.1M
U94 LMV331
R643 4.99K
3.3V
C479 0.1 uF
ENLP_SOURCE_STATE

LOOP CURRENT MEASUREMENT CIRCUIT

CHOOSE SOURCE OF CURRENT MEASUREMENT (CURRENTLY SOURCE SIDE TO REDUCE EFFECT OF LEAKAGE ON MIRRORING)

C408 0.1 uF
R265 1.00K
R573 NI
R644 NI
C477 0.01 uF
U66 OPA340
V = 2.0V AT 10MA
TP157
ENLP_CURRENT
R192 0.0
R267 NI

ENABLE LOOP IN

ENLP_IN
R370 10.0 Ohm
TP245
C470 0.1 uF
R333 806 Ohm
R334 NI 1/4W
REMOTE_SNS
2.5VREF
R196 1.00K
R195 24.3K
U99 OPA340
R636 0.0
Q12 BSS138
R688 200 Ohm

ROUTE TOGETHER

SINK SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

U100 INA193AIDBVT
SNK-
C468 0.1 uF
TP218
R635 37.4K
ENLP_SINK_REF
R274 1.1M
U101 LMV331
R634 4.99K
C469 0.1 uF
R676 392 Ohm
D57 LOC BEL ACT LED-GRN
Q39 BSS138
ENLP_SINK_STATE

VARIANT01

varian

SCALE	NONE
SHEET	16 OF 47

SCH, STN CONTROLLER
/NETWORK IF/LOCAL NETWORK/ENABLE LOOP LOCAL BE

DWG NO	REV
P1060967	D

CM# 0000600021312
Released
Ver: 03
Rev: D
11. November 2024

10mA CURRENT SOURCE

P24V
C131
0.1 uF
GND
U152
Vin
Vout
Vout
Vout
Vout
Adj
LM317L
R371
121 Ohm
R762
10.0 Ohm

LOOP CONTROL SWITCH

TP264
R763
NI
Q24
FDN5618P
TP263
ENLP_OUT
R760
200K
R761
200K
Q41
BSS138
ENLP_CNTL
R680
392 Ohm
D53
LOC MEL CMD
LED-GRN
R689
4.99K
GND
GND

ENABLE LOOP OUT

ROUTE TOGETHER

SOURCE SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

A+5V
U95
SRC+
SRC-
INA193AIDBVT
AGND
C475
0.1 uF
AGND
TP218
R642
37.4K
ENLP_SOURCE_REF
R269
1.1M
3.3V
U96
VCC
EN+
EN-
GND
LMV331
R640
4.99K
3.3V
C476
0.1 uF
GND
ENLP_SOURCE_STATE

LOOP CURRENT MEASUREMENT CIRCUIT

CHOOSE SOURCE OF CURRENT MEASUREMENT (CURRENTLY SOURCE SIDE TO REDUCE EFFECT OF LEAKAGE ON MIRRORING)

A+5V
C407
0.1 uF
AGND
R268
1.00K
R572
NI
R641
NI
C474
0.01 uF
AGND
AGND
A+5V
U67
OPA340
AGND
V = 2.0V AT 10MA
TP158
ENLP_CURRENT
R193
0.0
R270
NI
AGND

ENABLE LOOP IN

ENLP_IN
R372
10.0 Ohm
TP246
A+5V
C467
0.1 uF
AGND
R335
806 Ohm
R336
NI
1/4W
GND
REMOTE_SNS
R199
1.00K
2.5VREF
R198
24.3K
U102
OPA340
AGND
R633
0.0
Q13
BSS138
R687
200 Ohm
GND

ROUTE TOGETHER

SINK SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

A+5V
U103
SNK-
INA193AIDBVT
AGND
C465
0.1 uF
AGND
TP219
R632
37.4K
ENLP_SINK_REF
R275
1.1M
3.3V
U104
VCC
EN+
EN-
GND
LMV331
R631
4.99K
3.3V
C466
0.1 uF
GND
3.3V
R677
392 Ohm
D56
LOC MEL ACT
LED-GRN
Q38
BSS138
GND
ENLP_SINK_STATE

VARIANT01

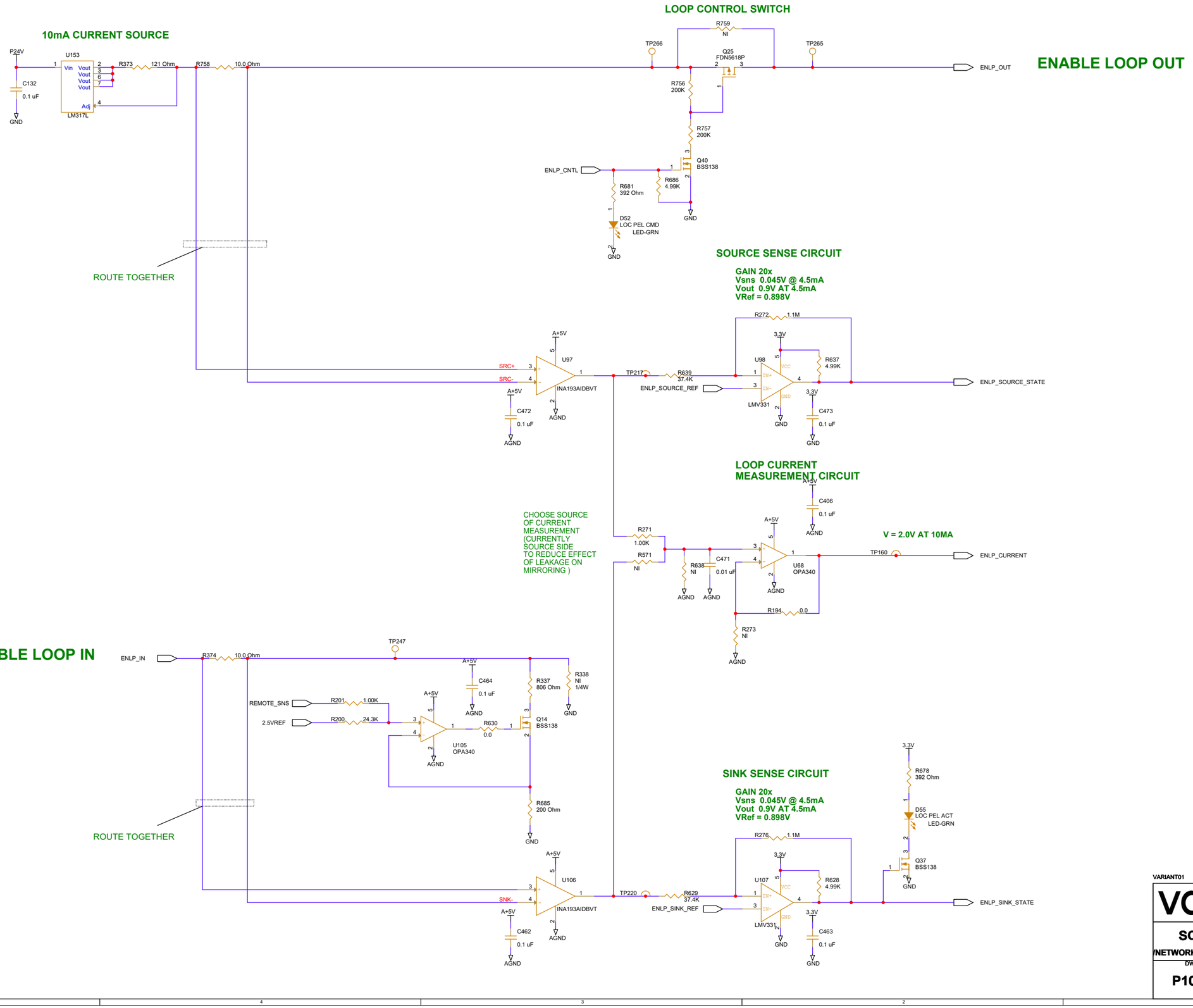
varian

SCALE	NONE
SHEET	17 OF 47

SCH, STN CONTROLLER
/NETWORK IF/LOCAL NETWORK/ENABLE LOOP LOCAL MEL

DWG NO	REV
P1060967	D

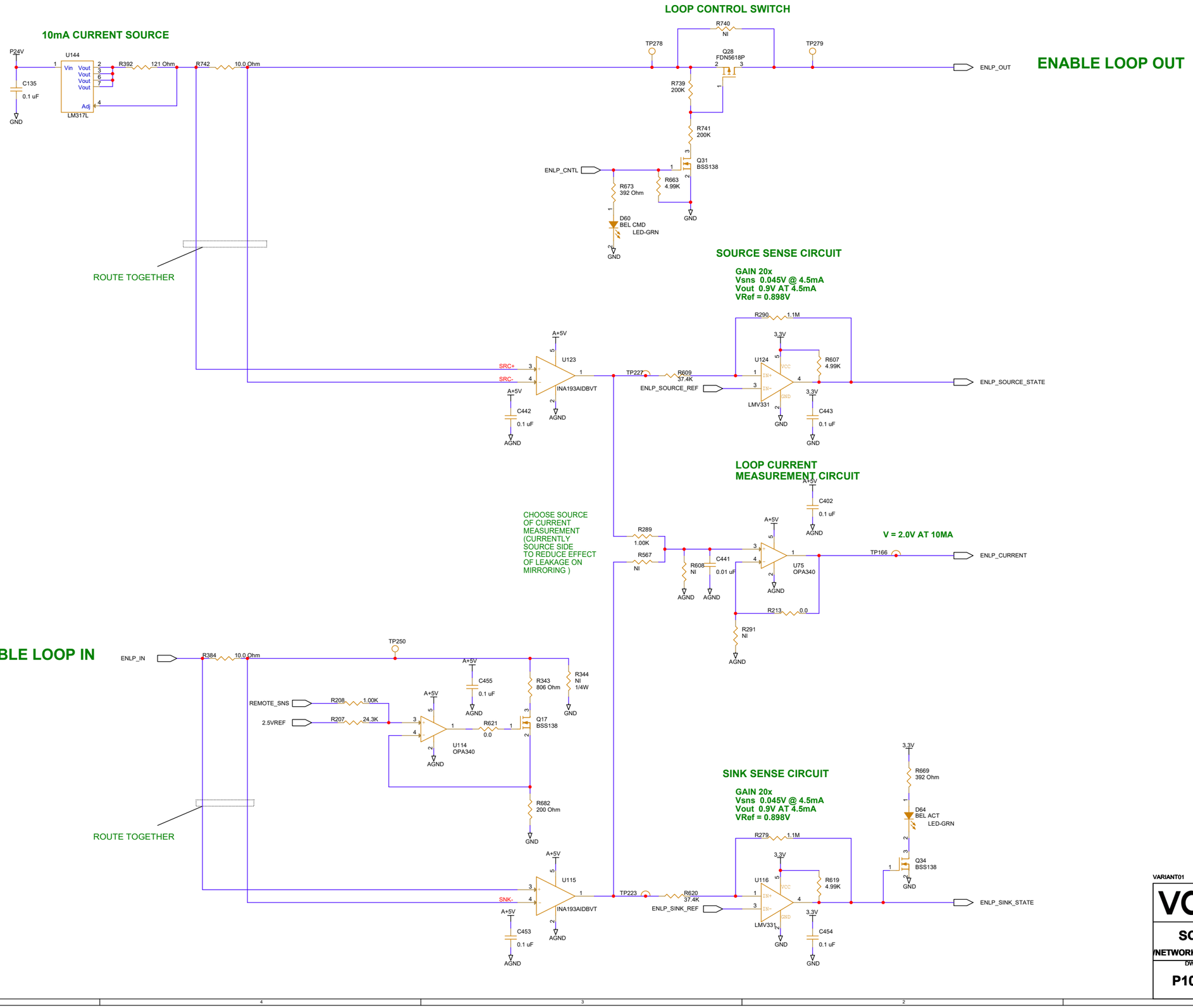
CM# 000060021312
Released
Ver: 03
Rev: D
11. November 2024



VARIANT01

varian	SCALE NONE
	SHEET 18 OF 47
SCH, STN CONTROLLER	
/NETWORK IF/LOCAL NETWORK/ENABLE LOOP LOCAL PEL	
DWG NO P1060967	REV D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024



VARIANT01

varian

SCALE	NONE
SHEET	19 OF 47

SCH, STN CONTROLLER

/NETWORK IF/ENABLE LOOP MAIN BEL

DWG NO	REV
P1060967	D

CM# 0000600021312

Released

Ver: 03

Rev: D

11. November 2024

10mA CURRENT SOURCE

P24V
C133
0.1 uF
GND
U155
Vin
Vout
Vout
Vout
Vout
Adj
LM317L
R389 121 Ohm
R750 10.0 Ohm

LOOP CONTROL SWITCH

R751
NI
TP270
TP271
Q26
FDN5618P
R748
200K
R749
200K
ENLP_OUT
ENLP_CNTL
Q33
BSS138
R674
392 Ohm
R665
4.99K
D59
MEL CMD
LED-GRN
GND

ENABLE LOOP OUT

ROUTE TOGETHER

SOURCE SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

A+5V
U119
SRC+
SRC-
INA193AIDBVT
AGND
C447
0.1 uF
TP225
R614
37.4K
ENLP_SOURCE_REF
R284 1.1M
3.3V
U120
VCC
IN+
IN-
GND
LMV331
R613
4.99K
C449
0.1 uF
ENLP_SOURCE_STATE

LOOP CURRENT MEASUREMENT CIRCUIT

CHOOSE SOURCE OF CURRENT MEASUREMENT (CURRENTLY SOURCE SIDE TO REDUCE EFFECT OF LEAKAGE ON MIRRORING)

A+5V
C404
0.1 uF
AGND
R283
1.00K
R569
NI
R615
NI
C448
0.01 uF
U73
OPA340
V = 2.0V AT 10MA
TP164
ENLP_CURRENT
R210 0.0
R285
NI

ENABLE LOOP IN

ENLP_IN
R380 10.0 Ohm
TP248
A+5V
C461
0.1 uF
R339
806 Ohm
R340
NI
1/4W
GND
REMOTE_SNS
2.5VREF
R203 1.00K
R202 24.3K
U108
OPA340
R627
0.0
Q15
BSS138
R684
200 Ohm

ROUTE TOGETHER

SINK SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

U109
SNK-
INA193AIDBVT
C459
0.1 uF
TP221
R626
37.4K
ENLP_SINK_REF
R277 1.1M
U110
LMV331
R625
4.99K
C460
0.1 uF
ENLP_SINK_STATE
R670
392 Ohm
D63
MEL ACT
LED-GRN
Q36
BSS138

VARIANT01

varian

SCALE	NONE
SHEET	20 OF 47

SCH, STN CONTROLLER
/NETWORK IF/ENABLE LOOP MAIN MEL

DWG NO	REV
P1060967	D

CM# 000060021312
Released
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Rev: D
11. November 2024

10mA CURRENT SOURCE

P24V
C134
0.1 uF
GND
U156
Vin
Vout
Vout
Vout
Vout
Adj
LM317L
R390 121 Ohm
R746 10.0 Ohm

LOOP CONTROL SWITCH

R747
NI
TP272
TP273
Q27
FDN5618P
ENLP_OUT
R744
200K
R745
200K
ENLP_CNTL
Q32
BSS138
R664
4.99K
R675
392 Ohm
D58
PEL CMD
LED-GRN
GND

ENABLE LOOP OUT

ROUTE TOGETHER

SOURCE SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

R287 1.1M
A+5V
U121
SRC+
SRC-
INA193AIDBVT
AGND
C445
0.1 uF
TP226
R612
37.4K
ENLP_SOURCE_REF
3.3V
U122
VCC
IN+
IN-
GND
LMV331
R610
4.99K
C446
0.1 uF
ENLP_SOURCE_STATE

LOOP CURRENT MEASUREMENT CIRCUIT

CHOOSE SOURCE OF CURRENT MEASUREMENT (CURRENTLY SOURCE SIDE TO REDUCE EFFECT OF LEAKAGE ON MIRRORING)

C403
0.1 uF
R286
1.00K
R568
NI
R611
NI
C444
0.01 uF
U74
OPA340
V = 2.0V AT 10MA
TP165
ENLP_CURRENT
R212 0.0
R288
NI

ENABLE LOOP IN

ENLP_IN
R376 10.0 Ohm
TP249
C458
0.1 uF
R341
806 Ohm
R342
NI
1/4W
REMOTE_SNS
2.5VREF
R206 1.00K
R205 24.3K
U111
OPA340
R624
0.0
Q16
BSS138
R683
200 Ohm

ROUTE TOGETHER

SINK SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

R278 1.1M
U112
SNK-
INA193AIDBVT
C456
0.1 uF
TP222
R623
37.4K
ENLP_SINK_REF
U113
LMV331
R622
4.99K
C457
0.1 uF
R671
392 Ohm
D62
PEL ACT
LED-GRN
Q35
BSS138
ENLP_SINK_STATE

VARIANT01

varian

SCALE	NONE
SHEET	21 OF 47

SCH, STN CONTROLLER
/NETWORK IF/ENABLE LOOP MAIN PEL

DWG NO	REV
P1060967	D

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LOOP CONTROL SWITCH

10mA CURRENT SOURCE

P24V
C136 0.1 uF
GND
U145 LM317L (Vin, Vout, Vout, Vout, Vout, Adj)
R393 121 Ohm
R737 10.0 Ohm
TP280
R738 NI
Q29 FDN5618P
TP281
ENLP_OUT

ENABLE LOOP OUT

R735 200K
R736 200K
Q30 BSS138
ENLP_CNTL
R672 392 Ohm
R662 4.99K
GND
D61 KBVEL CMD LED-GRN
GND

ROUTE TOGETHER

SOURCE SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

A+5V
U125 INA193AIDBVT
SRC+
SRC-
C439 0.1 uF
AGND
TP228
R606 37.4K
ENLP_SOURCE_REF
R293 1.1M
3.3V
U126 LMV331
R604 4.99K
C440 0.1 uF
GND
ENLP_SOURCE_STATE

LOOP CURRENT MEASUREMENT CIRCUIT

CHOOSE SOURCE OF CURRENT MEASUREMENT (CURRENTLY SINK SIDE)

R292 NI
R566 1.00K
R605 NI
C438 0.01 uF
AGND
A+5V
C401 0.1 uF
U76 OPA340
TP167
ENLP_CURRENT
R215 0.0
R294 NI

ENABLE LOOP IN

ENLP_IN
TP252
R394 10.0 Ohm
R346 1.0K Ohm 0.25W
GND

ROUTE TOGETHER

SINK SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

A+5V
U134 INA193AIDBVT
SNK-
C425 0.1 uF
AGND
TP234
R592 37.4K
ENLP_SINK_REF
R305 1.1M
3.3V
U135 LMV331
R591 4.99K
C426 0.1 uF
GND
R668 392 Ohm
D65 KVBEL ACT LED-GRN
Q19 BSS138
ENLP_SINK_STATE

VARIANT01

varian

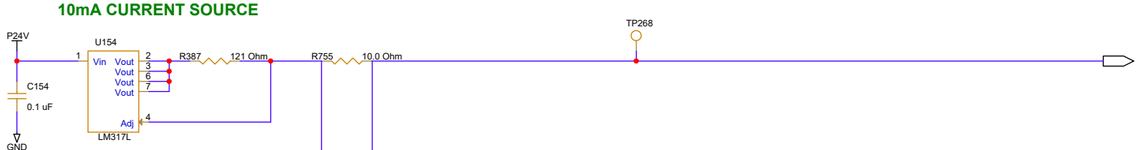
SCALE	NONE
SHEET	22 OF 47

SCH, STN CONTROLLER
/NETWORK IF/ENABLE LOOP NO SNS KVBEL

DWG NO	REV
P1060967	D

CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

10mA CURRENT SOURCE

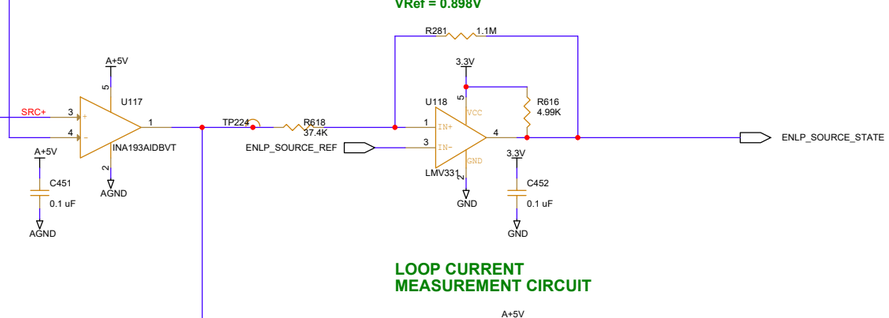


MEB LOOP OUT

ROUTE TOGETHER

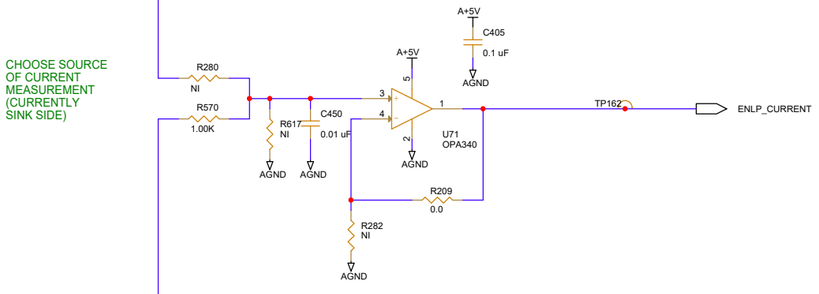
SOURCE SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V



LOOP CURRENT MEASUREMENT CIRCUIT

CHOOSE SOURCE OF CURRENT MEASUREMENT (CURRENTLY SINK SIDE)

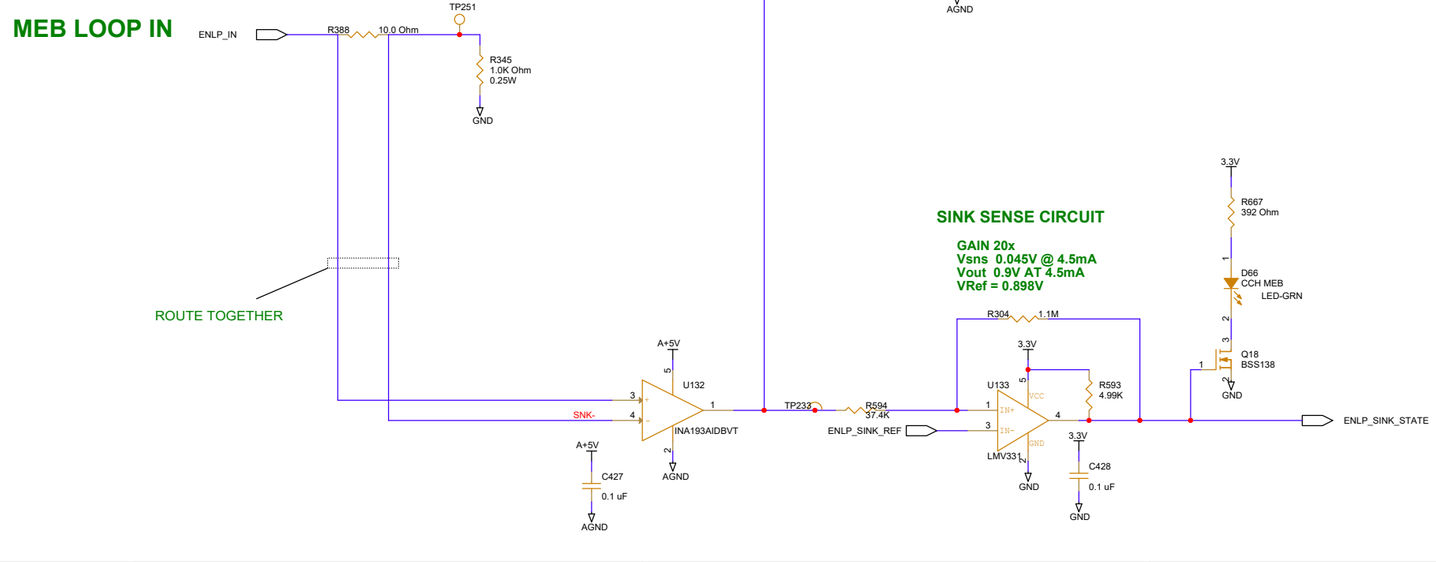


MEB LOOP IN

ROUTE TOGETHER

SINK SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V

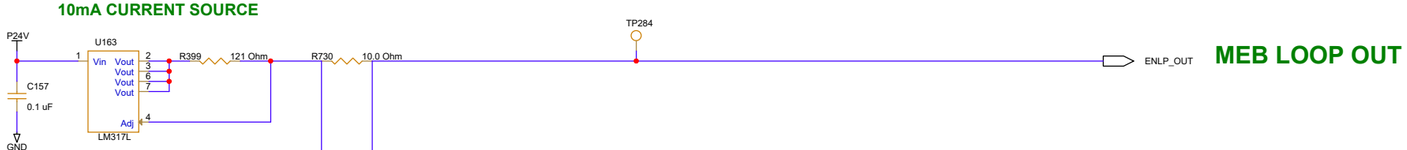


VARIANT01

varian	SCALE	NONE
	SHEET	23 OF 47
SCH, STN CONTROLLER /NETWORK IF/ENABLE LOOP USER COUCH		
DWG NO P1060967	REV	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

10mA CURRENT SOURCE

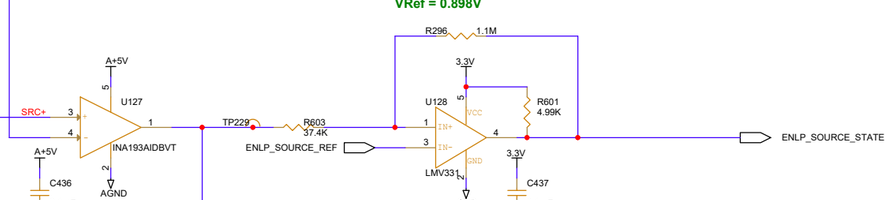


MEB LOOP OUT

ROUTE TOGETHER

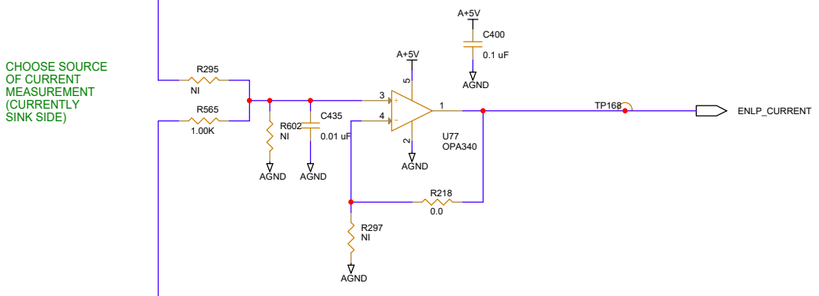
SOURCE SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V



LOOP CURRENT MEASUREMENT CIRCUIT

CHOOSE SOURCE OF CURRENT MEASUREMENT (CURRENTLY SINK SIDE)

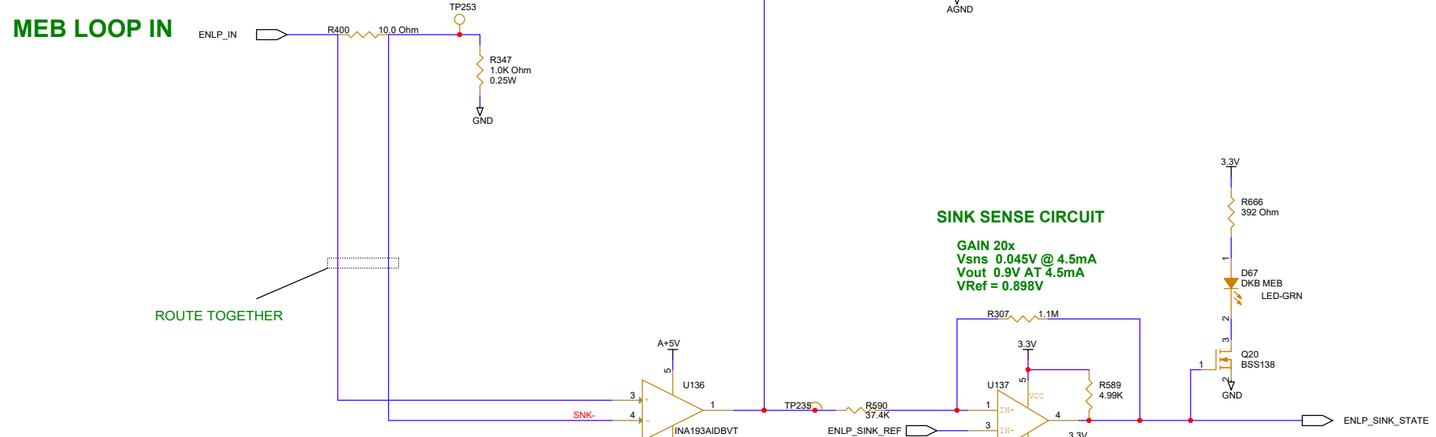


MEB LOOP IN

ROUTE TOGETHER

SINK SENSE CIRCUIT

GAIN 20x
Vsns 0.045V @ 4.5mA
Vout 0.9V AT 4.5mA
VRef = 0.898V



VARIANT01

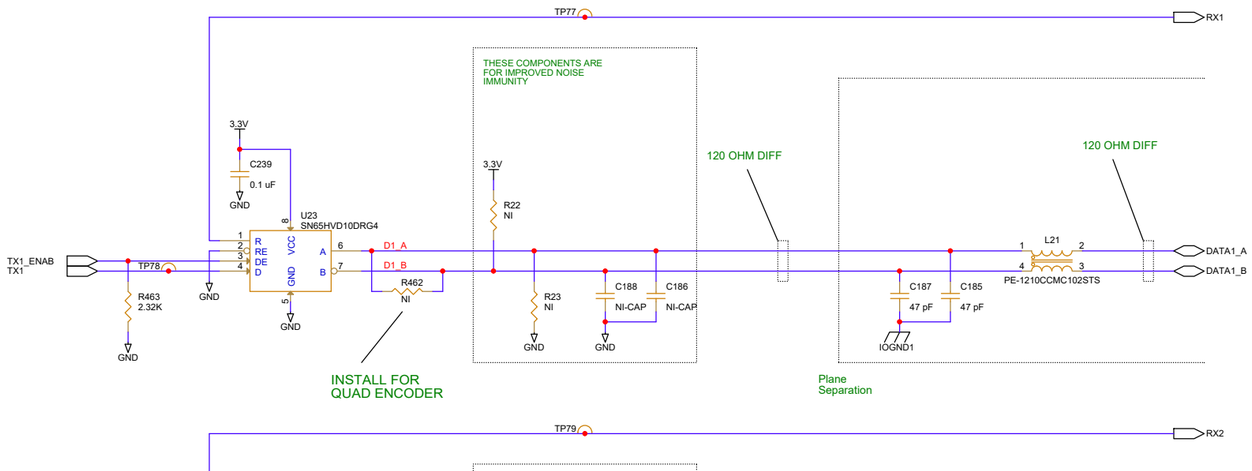
varian	SCALE	NONE
	SHEET	24 OF 47
SCH, STN CONTROLLER /NETWORK IF/ENABLE LOOP USER DKB		
DWG NO P1060967	REV	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

ENDAT ENCODER INTERFACE

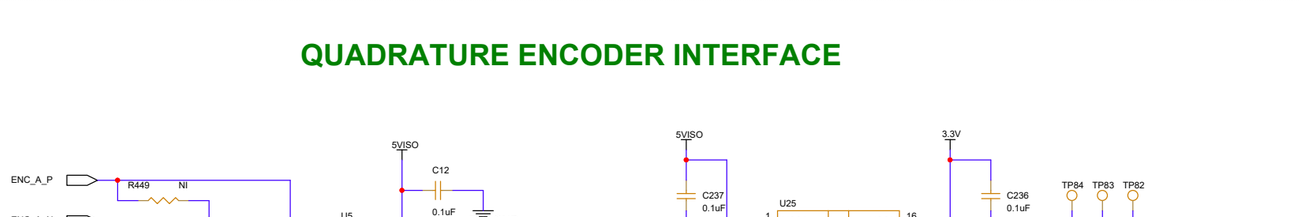
CHANNEL USE

ENCODER	DATA1	DATA2
ENDAT	CLK (OUT)	DATA (BI)



QUADRATURE ENCODER INTERFACE

FROM ENCODER



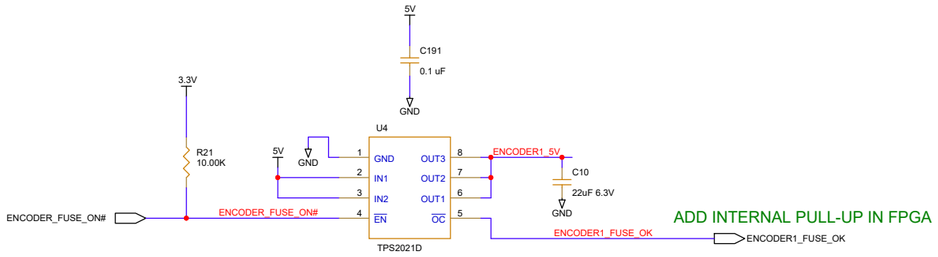
TO FPGA

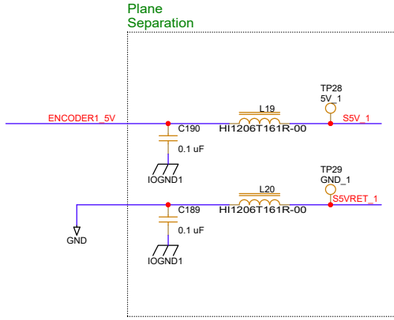
VARIANT01

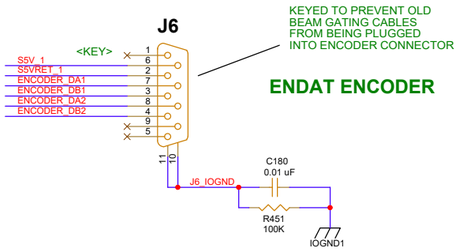
varian	SCALE: NONE
	SHEET: 25 OF 47
SCH, STN CONTROLLER	
/GANTRY ROTATION IF/ENCODER IF/ENCODER 1	
DWG NO: P1060967	REV: D

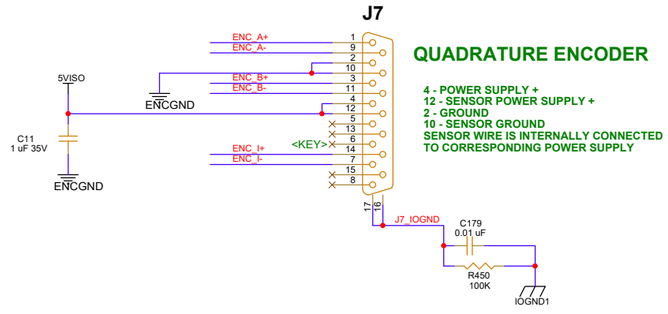
CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

ENDAT AND QUADRATURE ENCODER INTERFACE

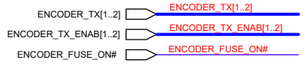




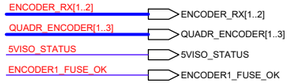




INPUT SIGNALS

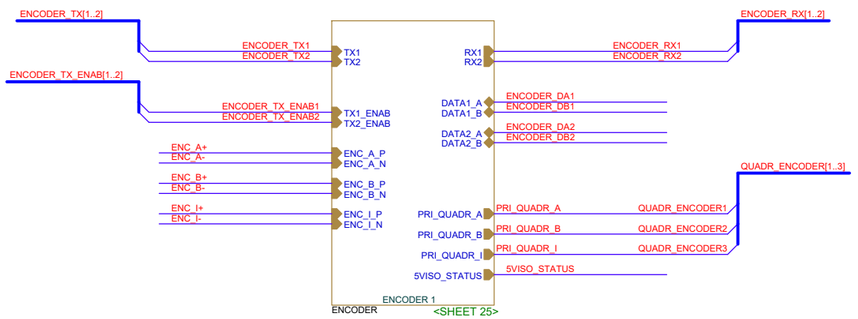


OUTPUT SIGNALS



ENCODER CHANNEL ASSIGNMENT

1	ENDAT CLK
2	ENDAT DATA



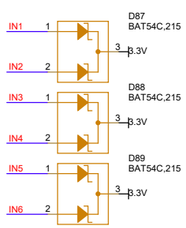
BOM COMPONENTS (CONNECTOR KEYS)

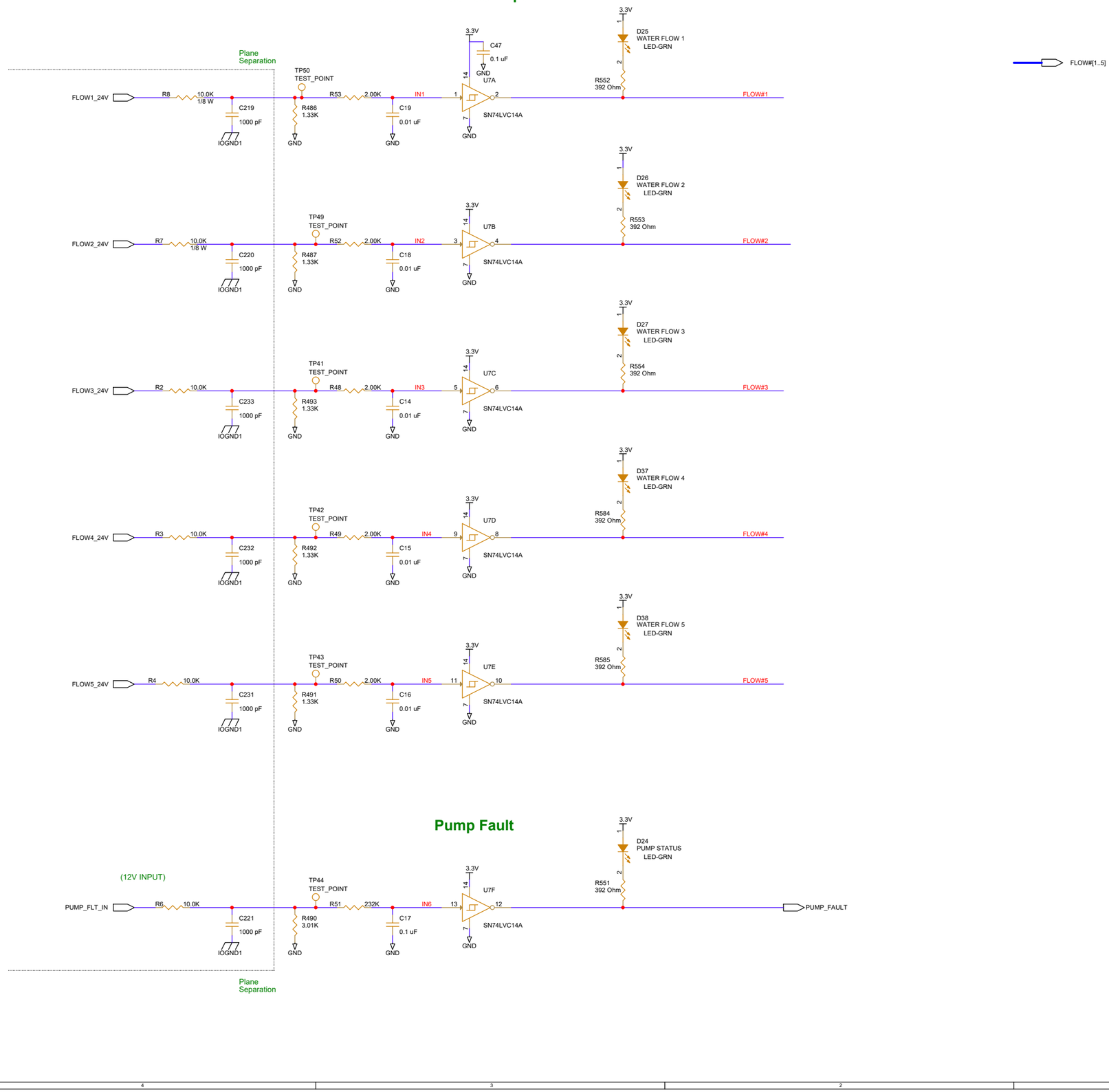
VARIANT01

varian	SCALE NONE
	SHEET 26 OF 47
SCH, STN CONTROLLER /GANTRY ROTATION IF/ENCODER IF	
DWG NO P1060967	REV D

CM# 0000600213112 Released Ver: 03 Rev: D 11. November 2024

Water Flow Sensor Inputs





Pump Fault

VARIANT01

varian

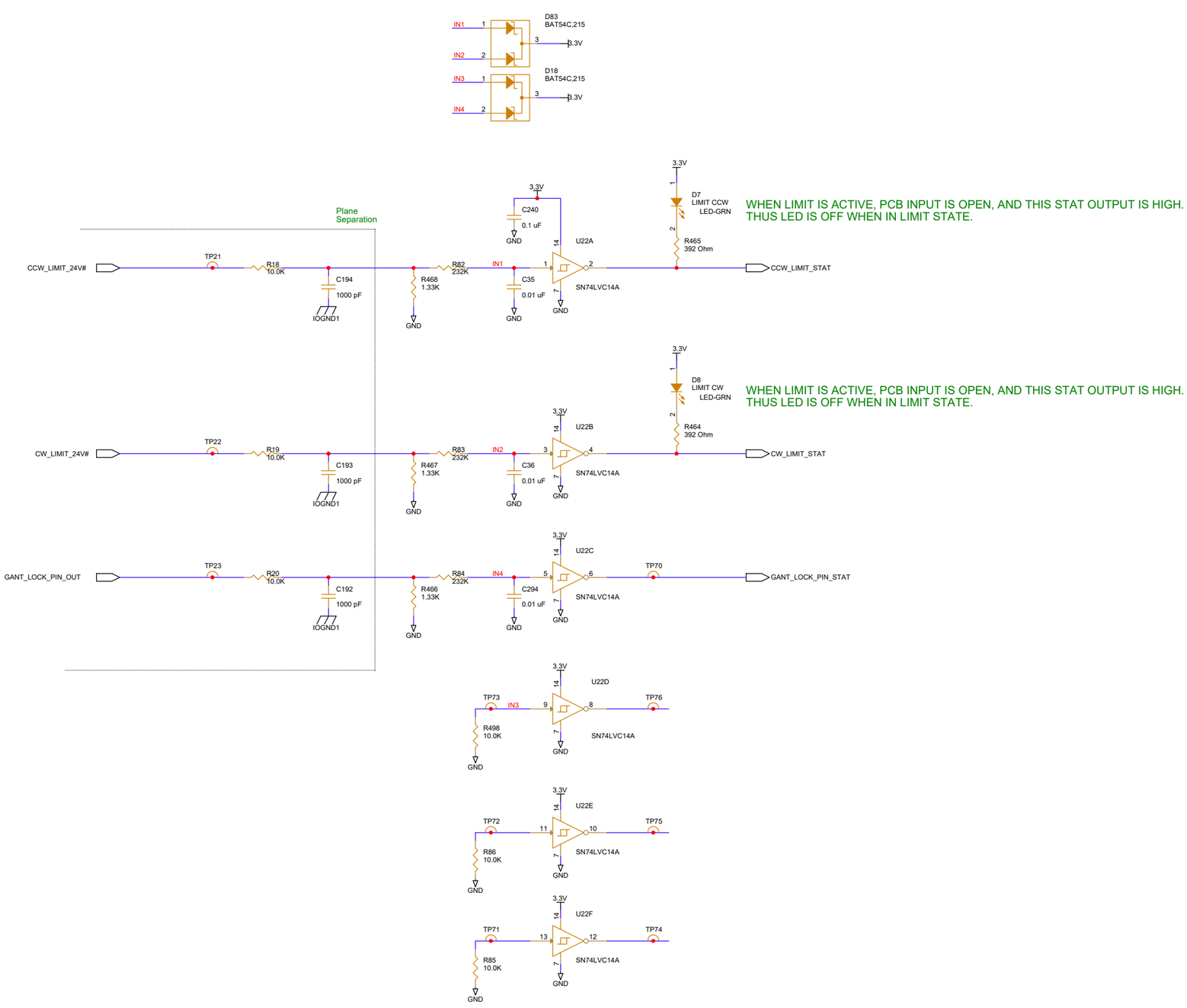
SCALE	NONE
SHEET	27 OF 47

SCH, STN CONTROLLER

/WATER IF/FLOW SENSORS

DWG NO	REV
P1060967	D

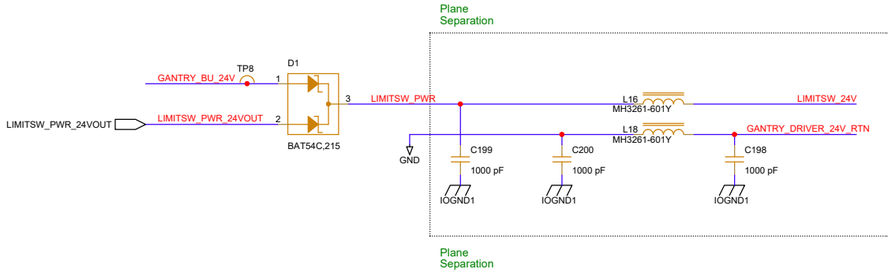
CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

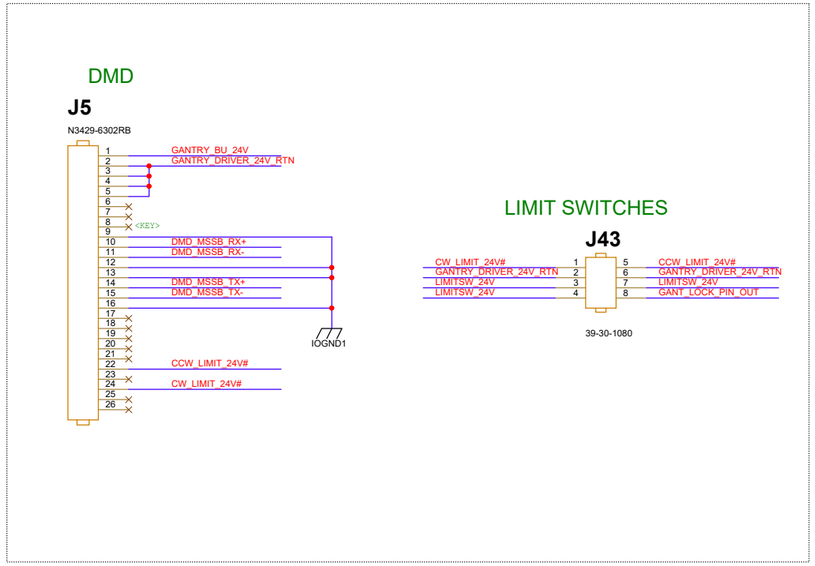


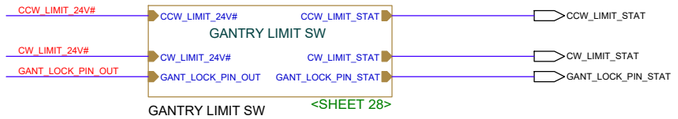
VARIANT01

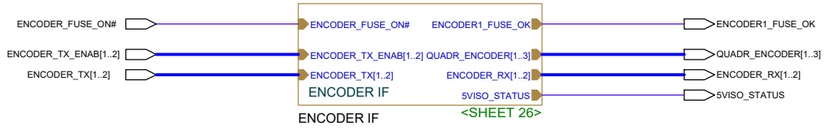
varian	SCALE NONE
	SHEET 28 OF 47
SCH, STN CONTROLLER /GANTRY ROTATION IF/GANTRY LIMIT SW	
DWG NO P1060967	REV D

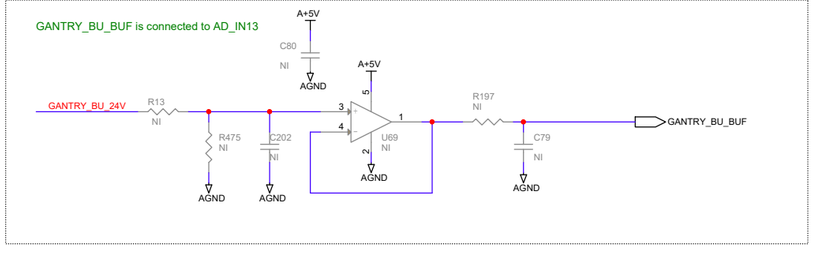
CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

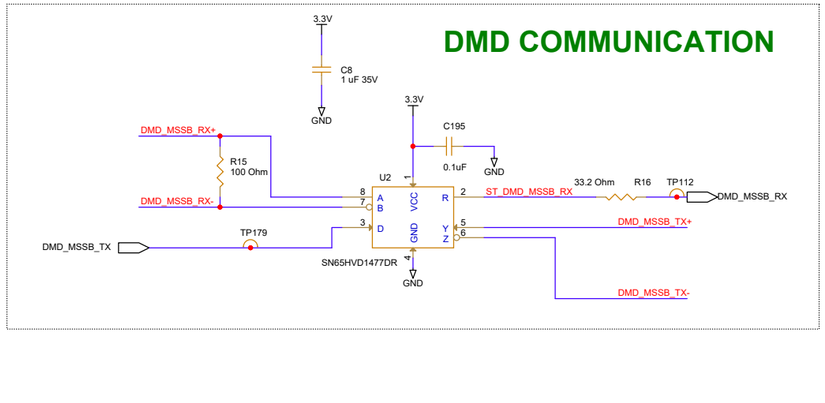












VARIANT01

varian

SCALE	NONE
SHEET	29 OF 47

SCH, STN CONTROLLER

/GANTRY ROTATION IF

DWG NO	REV
P1060967	D

CM# 0000600021312

Released

Ver: 03

Rev: D

11. November 2024

INPUT SIGNALS

SPD_AC_DR# → SPD_AC_DR#
BMENLP_STATE → BMENLP_STATE
CDOS_STS# → CDOS_STS#
CMNR_STS# → CMNR_STS#
EMO_GOOD# → EMO_GOOD#
KVBMENLP_STATE → KVBMENLP_STATE
PENDANT_INST → PENDANT_INST
PENDANT_MEB# → PENDANT_MEB#
PWRENLP_STATE → PWRENLP_STATE

MTNENLP_CCH_STATE → MTNENLP_CCH_STATE
MTNENLP_DKB_STATE → MTNENLP_DKB_STATE
MTNENLP_STATE → MTNENLP_STATE
DC_MAIN_DOOR_SW# → DC_MAIN_DOOR_SW#
NEUTRON_DR_SW1# → NEUTRON_DR_SW1#
NEUTRON_DR_SW2# → NEUTRON_DR_SW2#
LS_OSSD1# → LS_OSSD1#
LS_ERROR# → LS_ERROR#
CSPARESW1# → CSPARESW1#
CSPARESW2# → CSPARESW2#
HDW_DEVRST# → HDW_DEVRST#
APP_FPGA_TDO → APP_FPGA_TDO

OUTPUT SIGNALS

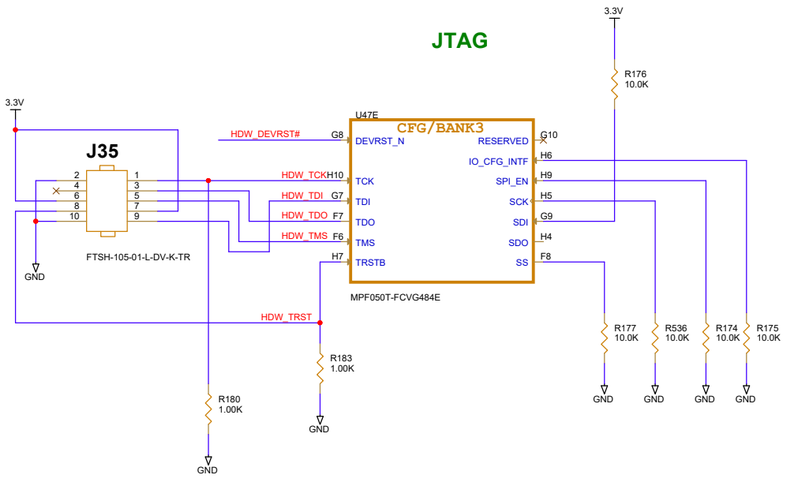
BMENLP_LOC_CNTL, MTNENLP_LOC_CNTL, PWRENLP_LOC_CNTL → BMENLP_LOC_CNTL, MTNENLP_LOC_CNTL, PWRENLP_LOC_CNTL

BMENLP_CNTL, KVBMENLP_CNTL, MTNENLP_CNTL, PWRENLP_CNTL → BMENLP_CNTL, KVBMENLP_CNTL, MTNENLP_CNTL, PWRENLP_CNTL

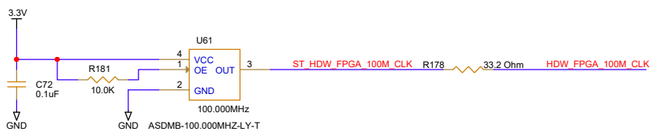
HDW_GANT_ROT_EN → HDW_GANT_ROT_EN

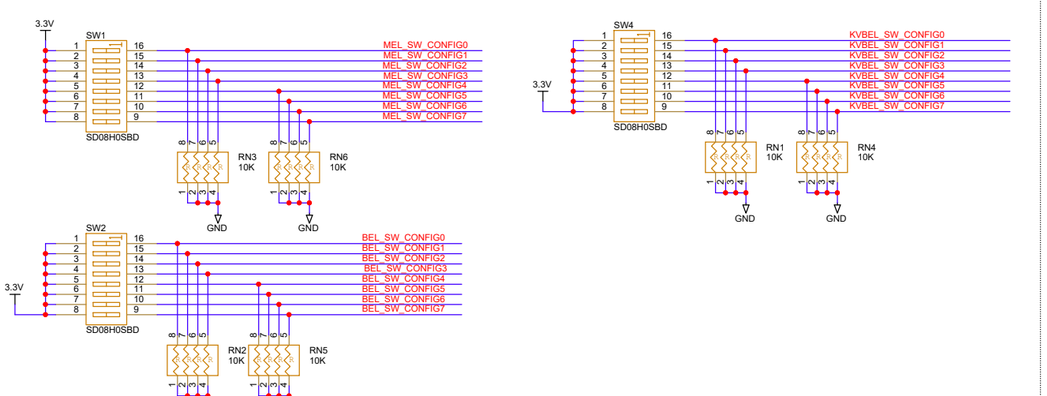
APP_FPGA_TRST, APP_FPGA_TDI, APP_FPGA_TMS, APP_FPGA_TCK → APP_FPGA_TRST, APP_FPGA_TDI, APP_FPGA_TMS, APP_FPGA_TCK

JTAG

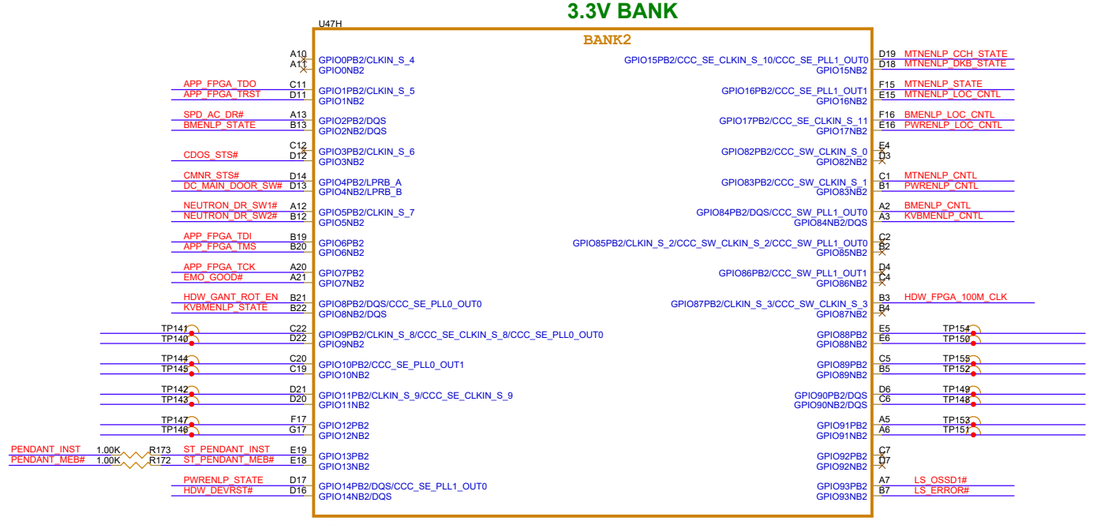


100MHz OSCILLATOR



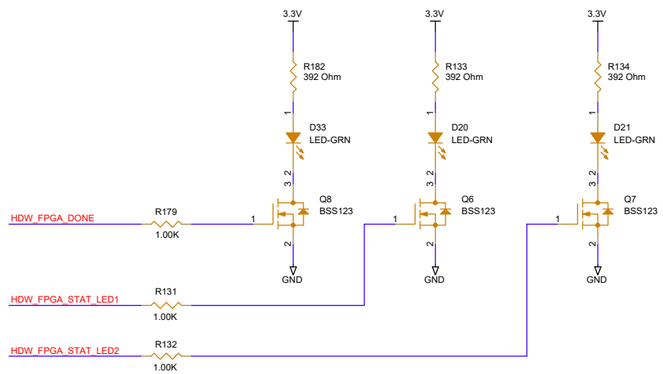


3.3V BANK



3.3V BANK

HW FPGA STATUS LEDS



VARIANT01

varian

SCALE	NONE
SHEET	30 OF 47

SCH, STN CONTROLLER

/HW_FPGA HDW_FPGA_GPIO

DWG NO	REV
P1060967	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

INPUT SIGNALS

APP_FPGA_SPI0_CS#
APP_FPGA_SPI_CLK
APP_FPGA_SPI0_MOSI
APP_FPGA_SPI1_CS#
APP_FPGA_SPI1_MOSI

HSSB_PMII_TX_EN
DISABLE_HDW_FPGA
HSSB_PMII_TX_DATA[0..3]
APP_AUX_IO[0..5]

PHY_RMII_RX_DATA1
PHY_RMII_RX_DATA0
PHY_RMII_RX_DV

OUTPUT SIGNALS

APP_FPGA_SPI0_MISO
APP_FPGA_SPI1_MISO
HSSB_PMII_RX_DV
HSSB_PMII_RESET#
HSSB_PMII_CLK

HSSB_PMII_RX_DATA[0..3]

PHY_RMII_TX_EN
PHY_RMII_TX_DATA1
PHY_RMII_TX_DATA0
PHY_RST#
PHY_50M_CLK
PHY_MDIO
PHY_MDC
ETH_LED1
ETH_LED2

1.8V BANK

U47F — BANK0 — MPF050T-FCVG484E

TP97	R11	HSIO42NB0	
TP95	R12	HSIO42PB0/CLKIN_N_5	
TP98	V10	HSIO43NB0	
TP96	V11	HSIO43PB0	
	U9	HSIO44NB0	
	V9	HSIO44PB0/CLKIN_N_4	
APP_AUX_IO[0..5]	R10		
DISABLE_HDW_FPGA	T10	HSIO45NB0/DQS	
		HSIO45PB0/DQS	
APP_AUX_IO0	U10	HSIO46NB0	
APP_AUX_IO1	T11	HSIO46PB0	
APP_AUX_IO2	T8	HSIO47NB0	
APP_AUX_IO3	U8	HSIO47PB0	
APP_AUX_IO4	AB8	HSIO48NB0	
APP_AUX_IO5	AB7	HSIO48PB0	
TP100	AA7	HSIO49NB0	
TP99	AA6	HSIO49PB0	
TP102	AA5	HSIO50NB0	
TP101	Y4	HSIO50PB0	
	AB5	HSIO51NB0/DQS	
	AB4	HSIO51PB0/DQS	
	AB3	HSIO52NB0	
	AA3	HSIO52PB0	
	Y6	HSIO53NB0	
	Y5	HSIO53PB0	

	W7	HSIO54NB0	
	W6	HSIO54PB0	
ETH_LED1	T7	HSIO55NB0	
ETH_LED2	T6	HSIO55PB0	
HDW_DBUG_HEADER2	V6	HSIO56NB0	
HDW_DBUG_HEADER4	V5	HSIO56PB0	
HDW_DBUG_HEADER6	V7	HSIO57NB0/DQS	
HDW_DBUG_HEADER8	U7	HSIO57PB0/DQS	
HDW_DBUG_HEADER10	V4	HSIO58NB0	
HDW_DBUG_CS#	W4	HSIO58PB0	
HDW_DBUG_ACTIVE	U5	HSIO59NB0	
HDW_DBUG_MOSI	U4	HSIO59PB0	
HDW_DBUG_MISO	W1	HSIO60NB0	
HDW_DBUG_SCLK	W2	HSIO60PB0/CLKIN_N_3/CCC_NW_CLKIN_N_3	
PHY_MDIO	Y3	HSIO61NB0	
PHY_MDC	W3	HSIO61PB0/CCC_NW_PLL1_OUT1	
PHY_RST#	AB2	HSIO62NB0	
PHY_RMII_TX_EN	AA2	HSIO62PB0/CLKIN_N_2/CCC_NW_CLKIN_N_2/CCC_NW_PLL1_OUT0	
PHY_RMII_TX_DATA1	V1	HSIO63NB0/DQS	
PHY_RMII_TX_DATA0	V2	HSIO63PB0/DQS/CCC_NW_PLL1_OUT0	
PHY_RMII_RX_DATA1	U2	HSIO64NB0	
PHY_RMII_RX_DATA0	U3	HSIO64PB0/CCC_NW_CLKIN_N_1	
PHY_RMII_RX_DV	AA1	HSIO65NB0	
HDW_FPGA_50M_CLK	Y1	HSIO65PB0/CCC_NW_CLKIN_N_0	

1.8V BANK

U47G — BANK1 — MPF050T-FCVG484E

HSSB_PMII_RESET#	V20	HSIO18NB1	
HSSB_PMII_CLK	V21	HSIO18PB1/CCC_NE_CLKIN_N_11	
HSSB_PMII_TX_DATA0	V22	HSIO19NB1	
HSSB_PMII_TX_DATA1	W22	HSIO19PB1/CCC_NE_PLL0_OUT1	
HSSB_PMII_TX_DATA2	AA22	HSIO20NB1	
HSSB_PMII_TX_DATA3	AA21	HSIO20PB1/CCC_NE_CLKIN_N_10/CCC_NE_PLL0_OUT0	
HSSB_PMII_TX_EN	W21	HSIO21NB1/DQS	
HSSB_PMII_RX_DV	Y21	HSIO21PB1/DQS/CCC_NE_PLL0_OUT0	
HSSB_PMII_RX_DATA0	V20	HSIO22NB1	
HSSB_PMII_RX_DATA1	AA20	HSIO22PB1	
HSSB_PMII_RX_DATA2	AB21	HSIO23NB1	
HSSB_PMII_RX_DATA3	AB20	HSIO23PB1	
APP_FPGA_SPI0_CS#	W19	HSIO24NB1	
APP_FPGA_SPI_CLK	Y19	HSIO24PB1/CLKIN_N_9/CCC_NE_CLKIN_N_9	
APP_FPGA_SPI0_MOSI	W18	HSIO25NB1	
APP_FPGA_SPI0_MISO	W17	HSIO25PB1/CCC_NE_PLL1_OUT1	
APP_FPGA_SPI1_CS#	Y18	HSIO26NB1	
APP_FPGA_SPI1_MOSI	AA18	HSIO26PB1/CLKIN_N_8/CCC_NE_CLKIN_N_8/CCC_NE_PLL1_OUT0	
APP_FPGA_SPI1_MISO	AB19	HSIO27NB1/DQS	
	AB18	HSIO27PB1/DQS/CCC_NE_PLL1_OUT0	
	AA17	HSIO28NB1	
	AB17	HSIO28PB1	
	Y16	HSIO29NB1	
	W16	HSIO29PB1	

	V19	HSIO30NB1	
HDW_EEP_SCLK	U19	HSIO30PB1	
	V17	HSIO31NB1	
HDW_EEP_CS#	V16	HSIO31PB1	
HDW_EEP_SDI	U17		
HDW_EEP_SDO	U18	HSIO32NB1	
		HSIO32PB1	
TP85	T17	HSIO33NB1/DQS	
TP89	T16	HSIO33PB1/DQS	
TP91	U15	HSIO34NB1	
TP92	T15	HSIO34PB1	
TP88	R15	HSIO35NB1	
TP86	R16	HSIO35PB1	
TP94	V12	HSIO36NB1	
TP93	U12	HSIO36PB1/CLKIN_N_7	
	W12	HSIO37NB1	
	W13	HSIO37PB1	
	U14	HSIO38NB1	
	U13	HSIO38PB1/CLKIN_N_6	
	V14	HSIO39NB1/DQS	
	V15	HSIO39PB1/DQS	
	T12	HSIO40NB1	
	T13	HSIO40PB1	
	R13	HSIO41NB1	
	R14	HSIO41PB1	

U47J — NO CONNECT — MPF050T-FCVG484E

E8	NC	NC	Y9
D8	NC	NC	Y10
B8	NC	NC	W11
A8	NC	NC	Y11
E9	NC	NC	AA10
D9	NC	NC	AA11
B9	NC	NC	Y8
C9	NC	NC	AA8
F10	NC	NC	AB10
E10	NC	NC	AB9
C10	NC	NC	W8
B10	NC	NC	W9
H12	NC	NC	T2
G12	NC	NC	T3
F13	NC	NC	T5
F12	NC	NC	R5
F11	NC	NC	M3
E11	NC	NC	N2
G15	NC	NC	P1
H15	NC	NC	N1
E12	NC	NC	N5
E13	NC	NC	N4
G14	NC	NC	P3
G13	NC	NC	P4
C17	NC	NC	P8
C16	NC	NC	P7
A15	NC	NC	M7
A16	NC	NC	M8
A17	NC	NC	P9
B17	NC	NC	R8
C15	NC	NC	N6
C14	NC	NC	N7
A18	NC	NC	P6
B18	NC	NC	R6
B15	NC	NC	N8
B14	NC	NC	M9
AB13	NC	NC	L5
AB14	NC	NC	L6
AA16	NC	NC	K5
AA15	NC	NC	K6
AB15	NC	NC	J6
AA13	NC	NC	J7
Y15	NC	NC	K8
Y14	NC	NC	K9
AB12	NC	NC	L7
AA12	NC	NC	L8
Y13	NC	NC	J9
W14	NC	NC	J8

U47A — XCVR-0 — MPF050T-FCVG484E

G19	XCVR_0_RX0_P	XCVR_0_TX0_P	F22
G20	XCVR_0_RX0_N	XCVR_0_TX0_N	F21
K21	XCVR_0_RX1_P	XCVR_0_TX1_P	H22
K22	XCVR_0_RX1_N	XCVR_0_TX1_N	H21
M21	XCVR_0_RX2_P	XCVR_0_TX2_P	P22
M22	XCVR_0_RX2_N	XCVR_0_TX2_N	P21
R20	XCVR_0_RX3_P	XCVR_0_TX3_P	T22
R19	XCVR_0_RX3_N	XCVR_0_TX3_N	T21
L19	XCVR_0A_REFCLK_P		
L20	XCVR_0A_REFCLK_N		
N19	XCVR_0B_REFCLK_P		
N20	XCVR_0B_REFCLK_N		
J19	XCVR_0C_REFCLK_P		
J20	XCVR_0C_REFCLK_N		

DEBUG CONNECTOR

1.8V — R458 2.32K

J36 — HEADER 6x2/SM

HDW_DBUG_HEADER2	2	1	HDW_DBUG_SCLK
HDW_DBUG_HEADER4	4	3	HDW_DBUG_MISO
HDW_DBUG_HEADER6	6	5	HDW_DBUG_MOSI
HDW_DBUG_HEADER8	8	7	HDW_DBUG_CS#
HDW_DBUG_HEADER10	10	9	HDW_DBUG_ACTIVE
	12	11	

GND — GND — R457 2.32K — GND

1.8V

R127 2.32K — C58 0.1uF — GND — R126 2.32K

U46 — 25AA640A-I/SN

HDW_EEP_CS#	1	CS	
	3	WP	
HDW_EEP_SDI	5	SI	
HDW_EEP_SCLK	6	SCK	
	8	VCC	
	7	HOLD	
	4	VSS	
	2	SO	HDW_EEP_SDO

GND

50MHz OSCILLATOR

3.3V — C61 0.1uF — GND

R135 10.0K — GND

U48 — SG-210STF 50.0000ML — 50.0000MHz

	4	VCC
	1	OE
	2	GND
50M_CLK_OUT	3	OUT

1.8V — C266 0.1uF — GND

U49 — 74FCT3807SSDCGI

	2	VDD			
	3	ICLK			
	4	GND			
ST_HDW_FPGA_50M_CLK	1	Q4	R87	33.2 Ohm	HDW_FPGA_50M_CLK
ST_PHY_50M_CLK	8	Q3	R136	33.2 Ohm	PHY_50M_CLK
	7	Q2			
	6	Q1			
	5	Q0			

GND

MATCHED LENGTH

VARIANT01

varian

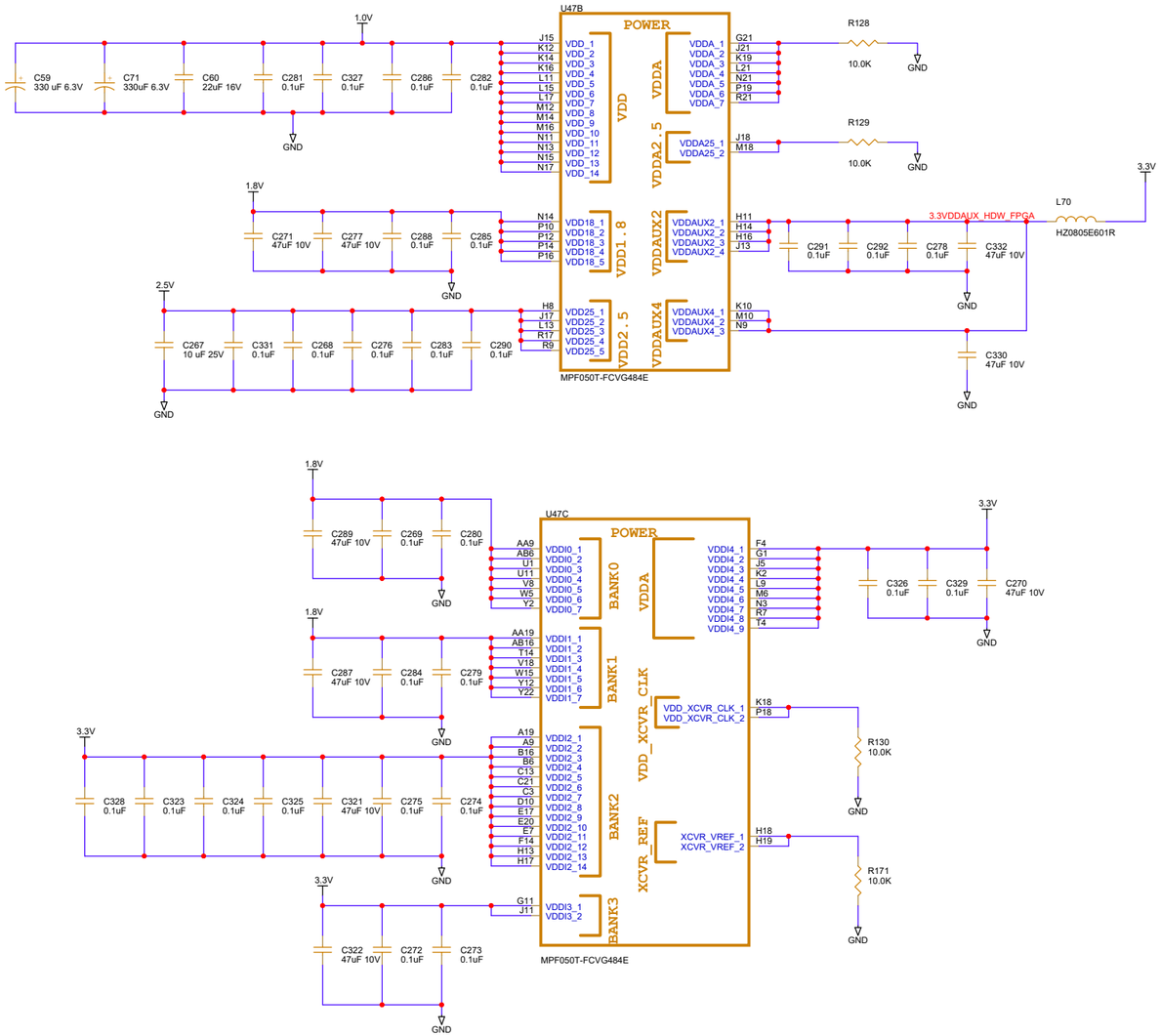
SCALE	NONE
SHEET	31 OF 47

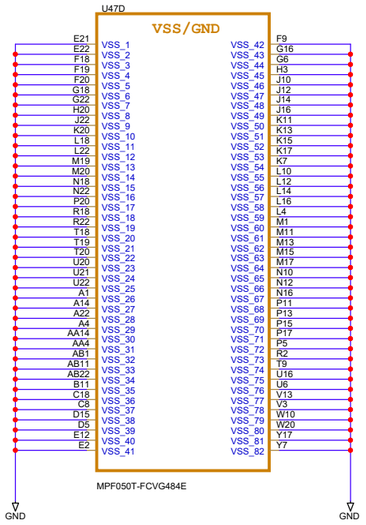
SCH, STN CONTROLLER

/HW_FPGA — HDW_FPGA_HSIO

DWG NO	REV
P1060967	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024





VARIANT01

varian	SCALE NONE
	SHEET 32 OF 47
SCH, STN CONTROLLER	
/HW_FPGA HDW_FPGA_POWER	
DWG NO P1060967	REV D

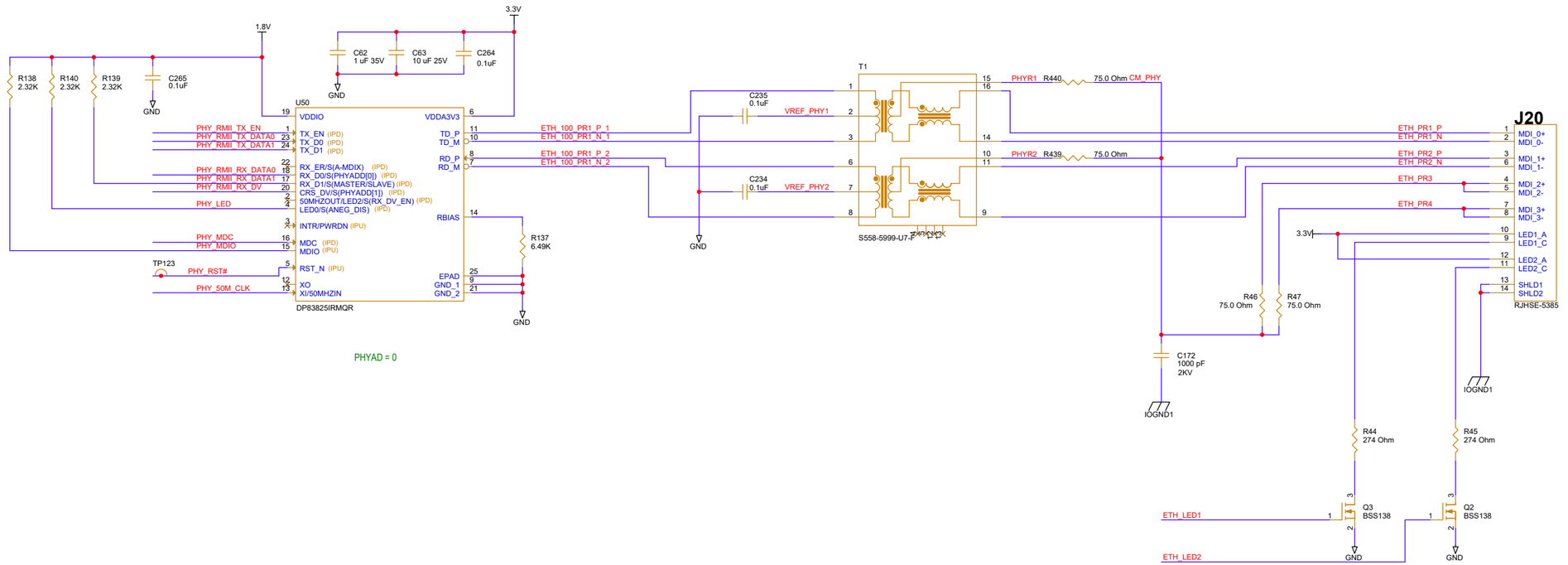
CM# 0000600021312
Released
Ver: 03
Rev: D
11. November 2024

INPUT SIGNALS

PHY_MDIO
PHY_MDC
PHY_RMII_TX_EN
PHY_RMII_TX_DATA1
PHY_RMII_TX_DATA0
PHY_50M_CLK
ETH_LED1
ETH_LED2
PHY_RST#

OUTPUT SIGNALS

PHY_RMII_RX_DATA1
PHY_RMII_RX_DATA0
PHY_RMII_RX_DV



PHYAD = 0

VARIANT01

varian

SCALE	NONE
SHEET	33 OF 47

SCH, STN CONTROLLER

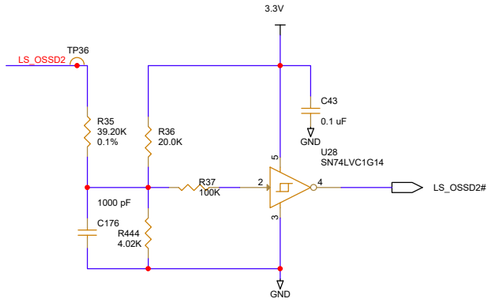
/HW_FPGA PHY

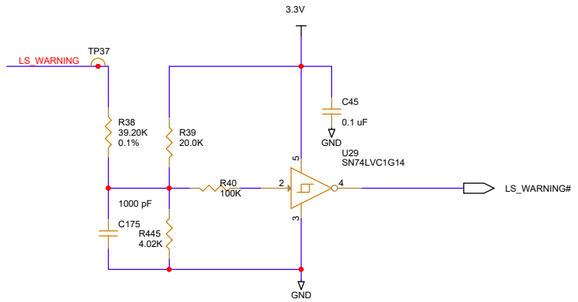
DWG NO	REV
P1060967	D

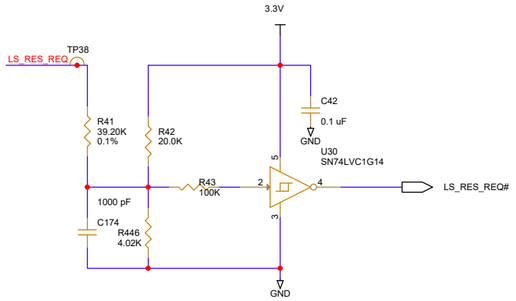
CM# 0000600213112 Released Ver: 03 Rev: D 11. November 2024

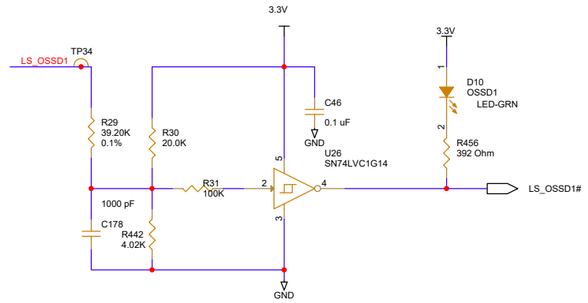
INPUT SIGNALS

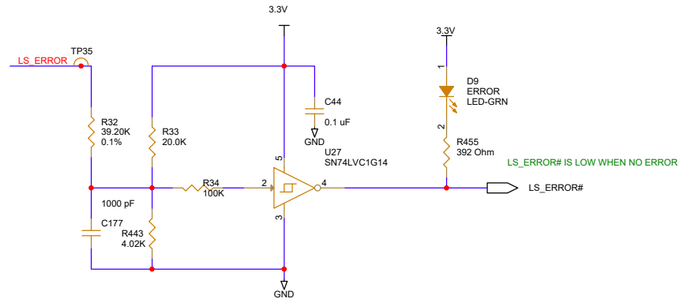
LGCTRL1_OUT → LGCTRL1_OUT
LGCTRL2_OUT → LGCTRL2_OUT
LGCTRL3_OUT → LGCTRL3_OUT





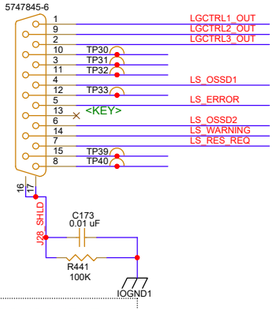






J28

5747845-6



BOM COMPONENT
(CONNECTOR KEY)

XJ28_13
206509-1

VARIANT01

varian

SCALE	NONE
SHEET	34 OF 47

SCH, STN CONTROLLER
/LASERGUARD IF

DWG NO	REV
P1060967	D

CM# 000060021312
Released
Ver: 03
Rev: D
11. November 2024

LOOP VOLTAGE MONITOR
FOR LOCAL LOOP DEBUG

GND/AGND
PLANE SEP

PEL_LOC_OUT — R258 1.1M — R579 100.0K — C76 1000 pF — U63A OPA4340EA/2K5G4 (3, 2, 1, 4, 13) — 100 Ohm — C414 0.01 uF — PEL_LOC_OUT_MON
A+5V — C410 0.1 uF — AGND

PEL_LOC_IN — R257 1.1M — R583 100.0K — C74 1000 pF — U63B OPA4340EA/2K5G4 (5, 6, 7, 4, 13) — 100 Ohm — C418 0.01 uF — PEL_LOC_IN_MON

BEL_LOC_OUT — R313 1.1M — R653 100.0K — C97 1000 pF — U63C OPA4340EA/2K5G4 (12, 11, 10, 4, 13) — 100 Ohm — C485 0.01 uF — BEL_LOC_OUT_MON

BEL_LOC_IN — R261 1.1M — R649 100.0K — C99 1000 pF — U63D OPA4340EA/2K5G4 (14, 15, 16, 4, 13) — 100 Ohm — C417 0.01 uF — BEL_LOC_IN_MON

MEL_LOC_OUT — R260 1.1M — R576 100.0K — C78 1000 pF — U65A OPA4340EA/2K5G4 (3, 2, 1, 4, 13) — 100 Ohm — C409 0.01 uF — MEL_LOC_OUT_MON
A+5V — C416 0.1 uF — AGND

MEL_LOC_IN — R259 1.1M — R578 100.0K — C77 1000 pF — U65B OPA4340EA/2K5G4 (5, 6, 7, 4, 13) — 100 Ohm — C412 0.01 uF — MEL_LOC_IN_MON

THE LOOP INPUTS MONITORED IN THIS COLUMN
DO NOT HAVE FILTERS OR REVERSE PROTECTION,
SO IT IS INCLUDED HERE.

IOGND/AGND
PLANE SEP

PEL_LOC_MID — L41 HZ0805E601R — D109 SMAJ33A-13 — C578 100 pF — IOGND1
R256 1.1M — R648 100.0K — C101 1000 pF — AGND
U65C OPA4340EA/2K5G4 (12, 11, 10, 4, 13) — 100 Ohm — C481 0.01 uF — PEL_LOC_MID_MON

BEL_LOC_MID — L39 HZ0805E601R — D111 SMAJ33A-13 — C580 100 pF — IOGND1
R188 1.1M — R647 100.0K — C102 1000 pF — AGND
U65D OPA4340EA/2K5G4 (14, 15, 16, 4, 13) — 100 Ohm — C411 0.01 uF — BEL_LOC_MID_MON

GATE A ON
SUBSYS_LP_MON
SHEET

MEL_LOC_MID — L40 HZ0805E601R — D110 SMAJ33A-13 — C579 100 pF — IOGND1
R187 1.1M — R582 100.0K — C75 1000 pF — AGND
U64B OPA4340EA/2K5G4 (5, 6, 7, 4, 13) — 100 Ohm — C415 0.01 uF — MEL_LOC_MID_MON

R577 0.0 — AGND
U64C OPA4340EA/2K5G4 (12, 11, 10, 4, 13) — XTRA1_MON

R548 0.0 — AGND
U64D OPA4340EA/2K5G4 (14, 15, 16, 4, 13) — XTRA2_MON

VARIANT01

varian	SCALE NONE
	SHEET 35 OF 47
SCH, STN CONTROLLER	
/NETWORK IF/LOOP MON/LOCAL LOOP MON	
DWG NO P1060967	REV D

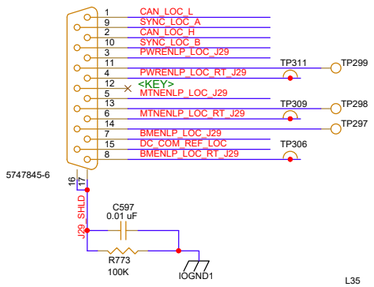
CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

CAN_LOC_H
CAN_LOC_L

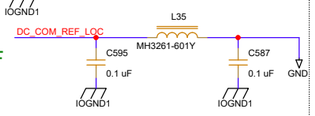
ENLP_SOURCE_REF
ENLP_SINK_REF

Local Network IF (Input)

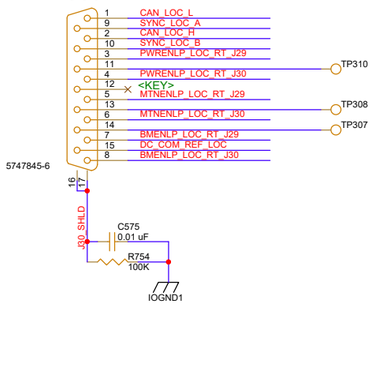
J29

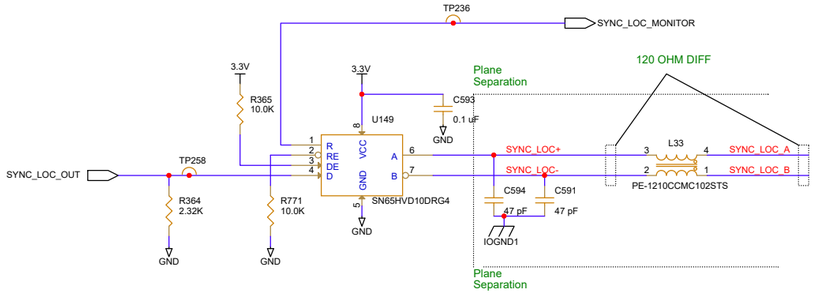


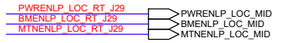
Local Network IF (Output)

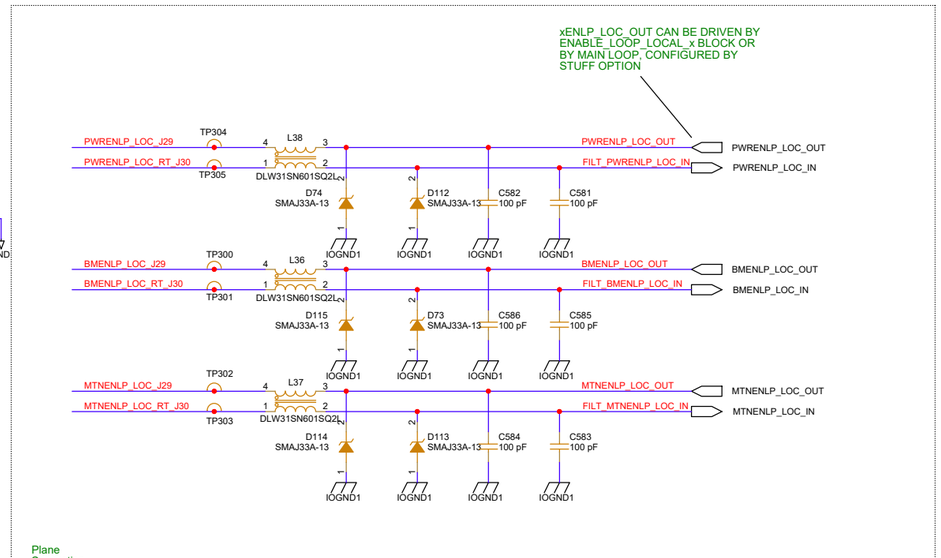


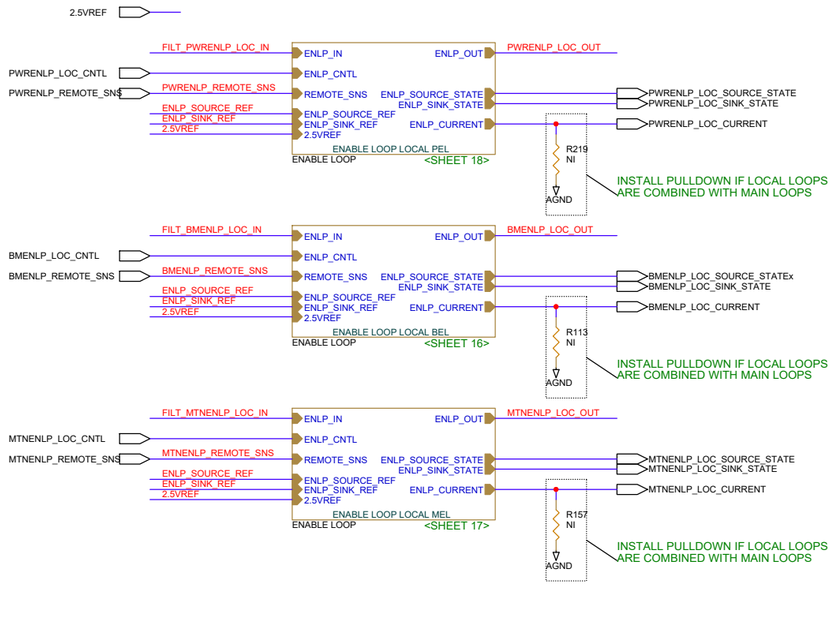
J30









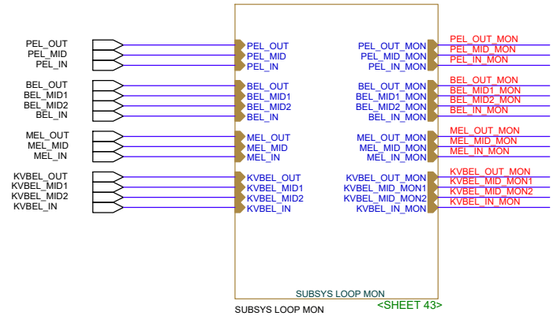


BOM COMPONENTS (CONNECTOR KEYS)

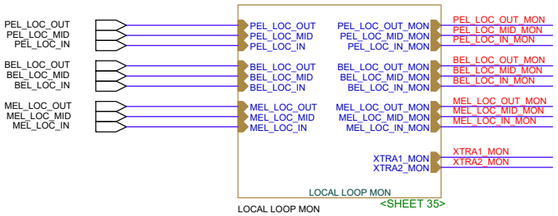
VARIANT01

varian	SCALE NONE
	SHEET 36 OF 47
SCH, STN CONTROLLER	
/NETWORK IF/LOCAL NETWORK	
DWG NO P1060967	REV D

CM# 0000600021312
Released
Ver: 03
Rev: D
11. November 2024



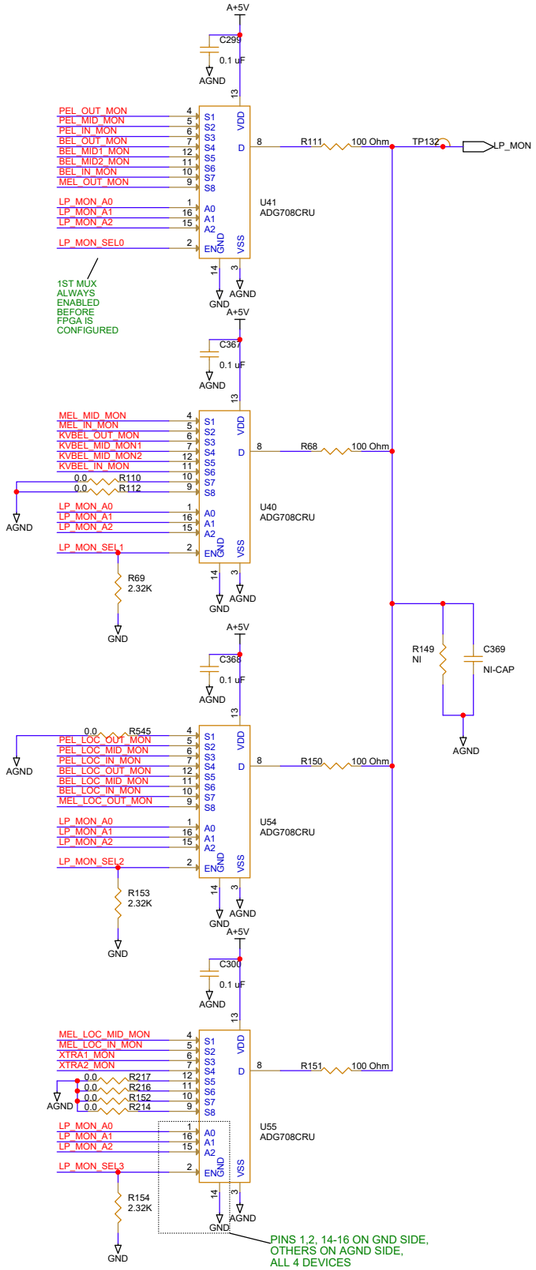
SUBSYS LOOP MON



LOCAL LOOP MON

LP_MON_SEL[3:0]

LP_MON_A[2:0]



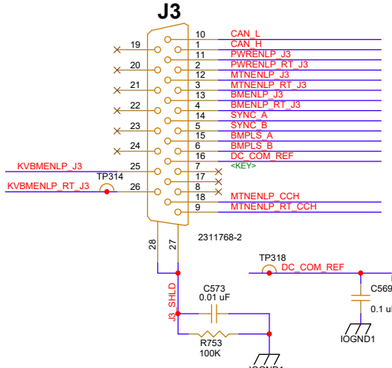
VARIANT01

varian	SCALE NONE
	SHEET 37 OF 47
SCH, STN CONTROLLER /NETWORK IF/LOOP MON	
DWG NO P1060967	REV D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

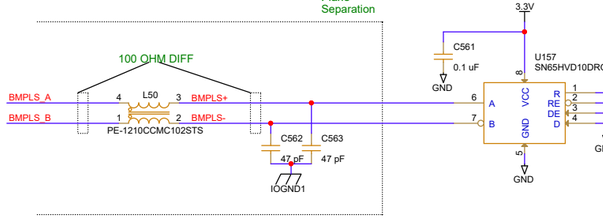
Subsystem Network IF (Output A)

J3



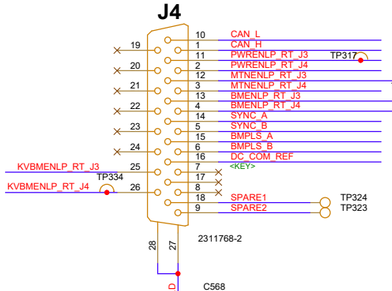
Plane Separation

100 OHM DIFF

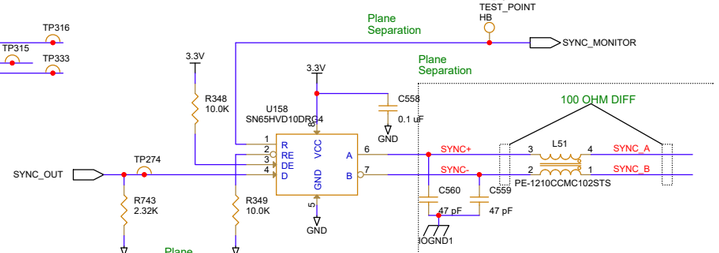


Subsystem Network IF (Output B)

J4



Plane Separation

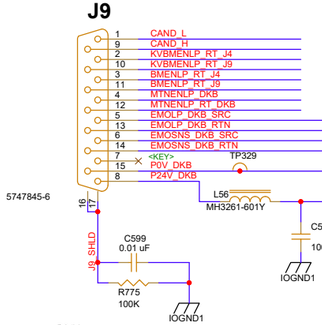


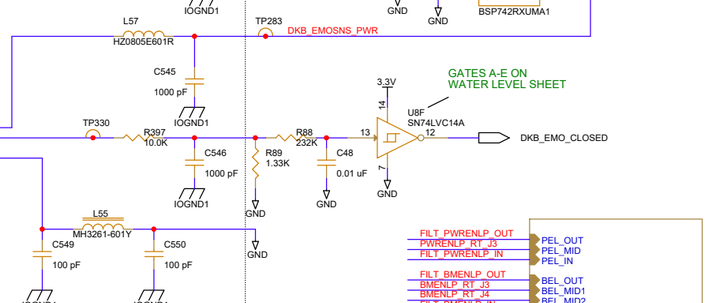
Plane Separation

PROVIDE INDEPENDENT POWER FOR DKB'S EMO SENSE LOOP

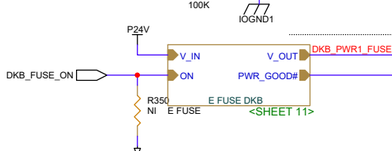
DKB Network IF

J9





GATES A-E ON WATER LEVEL SHEET



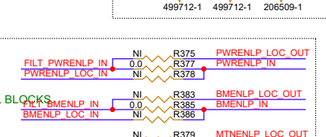
Plane Separation

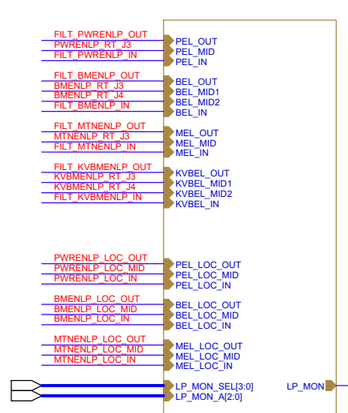
BOM COMPONENTS (CONNECTOR KEYS)

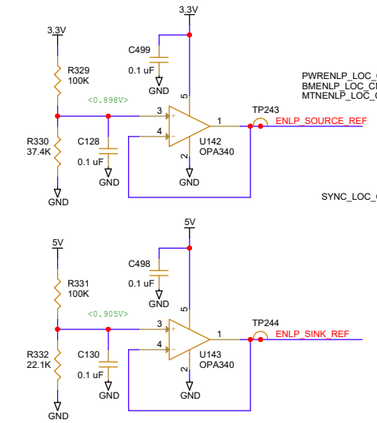
XJ3_7	XJ4_7	XJ9_7
499712-1	499712-1	206509-1

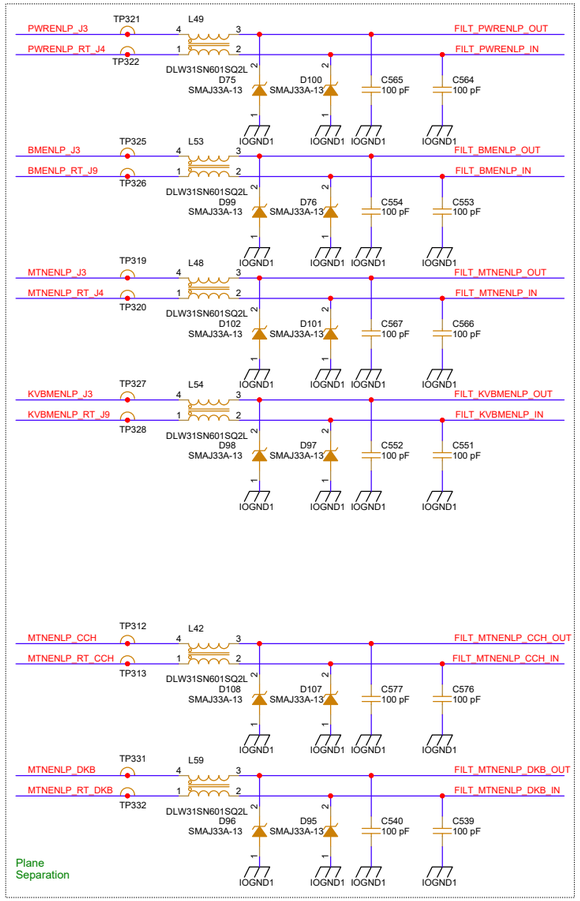
TO COMBINE MAIN LOOPS WITH LOCAL LOOPS:
1) REMOVE 0 OHM RESISTORS
2) INSTALL 0 OHM IN NI POSITIONS
3) REMOVE ALL CIRCUITRY IN ENABLE_LOOP_LOCAL_PEL/BEL/MEL BLOCKS
4) INSTALL 10K IN 3 NI POSITIONS OF LOCAL_NETWORK BLOCK

*** CURRENTLY CONFIGURED FOR SEPARATE LOOPS ***

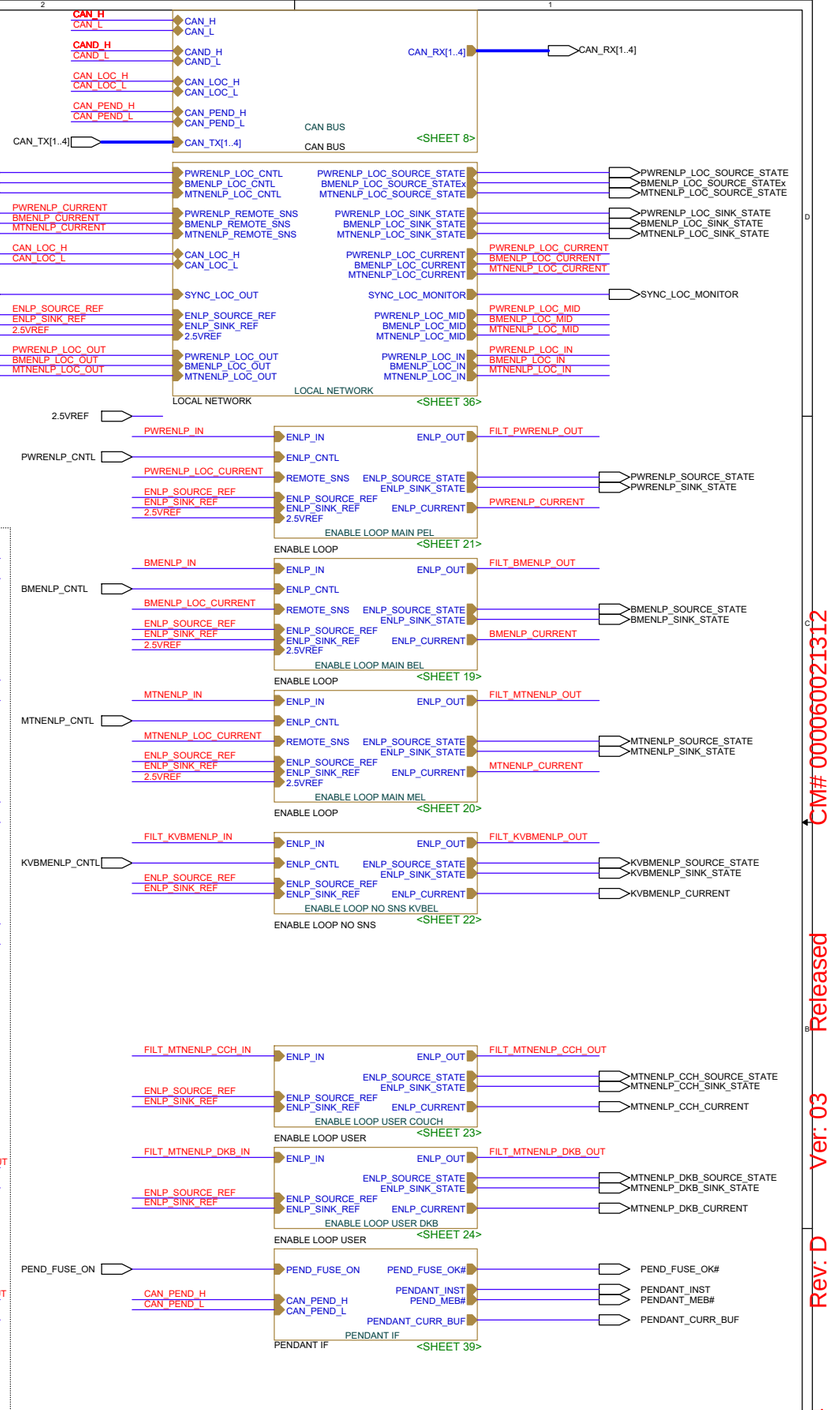


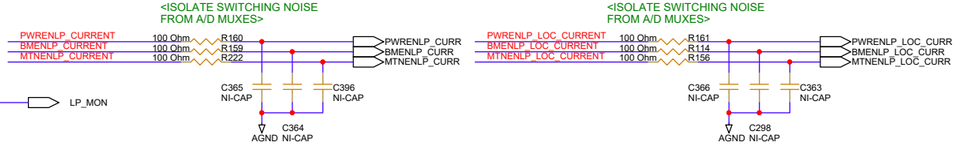






Plane Separation





VARIANT01

varian	SCALE: NONE
	SHEET: 38 OF 47
SCH, STN CONTROLLER /NETWORK IF	
DWG NO: P1060967	REV: D

CM# 0000600213L2

Released Ver: 03 Rev: D 11. November 2024

CAN_PEND_H
CAN_PEND_L

Plane Separation

PENDANT CONNECTOR

J25

1 PEND_ID
2 PENDANT_GND
3 CAN_PEND_H
4 CAN_PEND_L
5 PENDANT_24V
6 PENDANT_MEB_24V

5555154-1

R312 10.0K

GND

PEND_CURR_BUF is connected to AD_IN14

A+5V
C82 NI
AGND
A+5V
PEND_CURR
R223 NI
R306 NI
C106 NI
U70 NI
R204 NI
C81 NI
PENDANT_CURR_BUF

P24V
E FUSE PENDANT
V_IN
ON
V_OUT
PWR_GOOD#
E FUSE
<SHEET 10>
PEND_FUSE_ON
R248 2.32K
PEND_FUSE_OK#
R252 0.5 1W
PEND_V_SHUNT
C376 1000 pF
L27 MH3261-601Y
TP214
PENDANT_24V
L32 MH3261-601Y
C420 1000 pF
C419 1000 pF
PENDANT_GND
IOGND1

PENDANT MONITOR

ROUTE TOGETHER
SVC_PEND_IMON_P
SVC_PEND_IMON_N
U89 INA193AIDBVT
TP177
PEND_CURR
R253 37.4K
R185 1.1M
U88 LMV331
R534 4.99K
C73 NI-CAP
C379 0.1 uF
R533 100K
R186 13.7K
C319 0.1 uF
(41mA TRIP)
PENDANT_INST

PENDANT LED INDICATOR

R532 392 Ohm
D36 PEND_INST LED-GRN
Q9 BSS138

HET PENDANT IS DRIVEN BY 24V AND HAS 10K OUTPUT RESISTANCE

PENDANT_MEB_24V
L28 HZ0805E601R
TP213
C375 1000 pF
R254 10.0K
R556 4.02K
C374 1000 pF
R255 100K
D46 BAT54C,215
U90 SN74LVC1G14
R555 392 Ohm
D47 PEND ME LED-GRN
PEND_MEB#
C373 0.1 uF

VARIANT01

varian

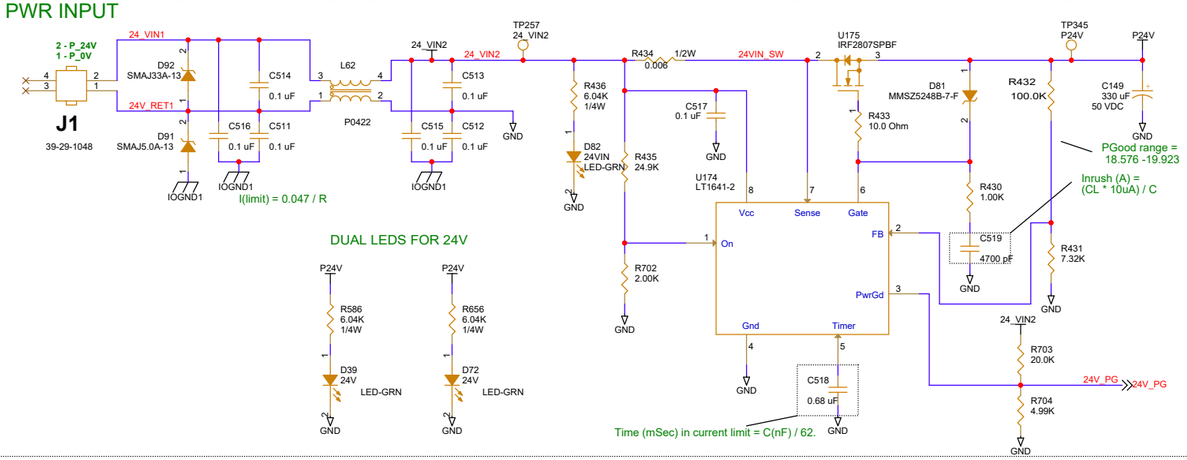
SCALE	NONE
SHEET	39 OF 47

SCH, STN CONTROLLER
/NETWORK IF/PENDANT IF

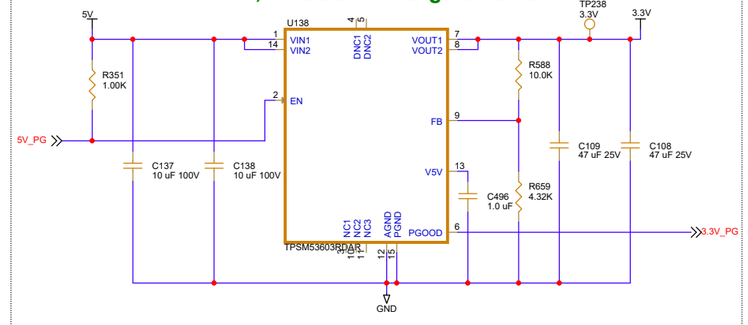
DWG NO P1060967
REV D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

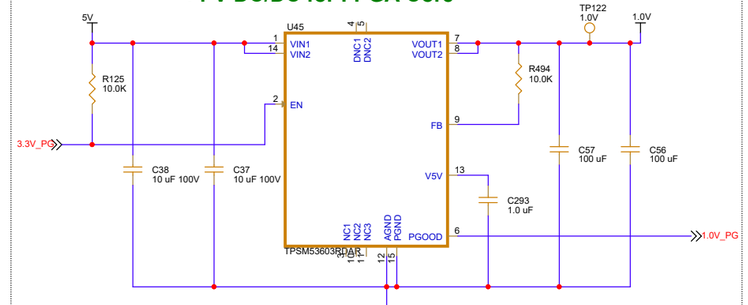
PWR INPUT



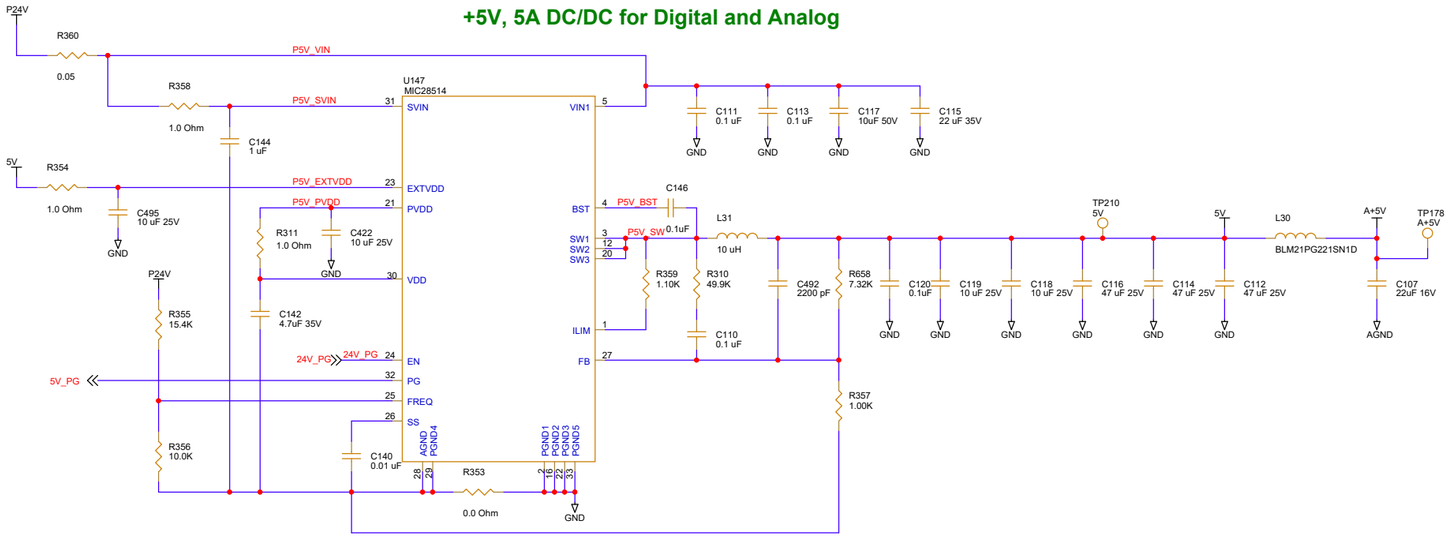
+3.3 V, 3A DC/DC for Digital Circuits



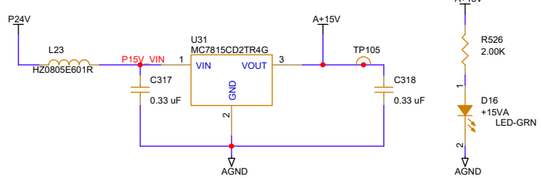
+1 V DC/DC for FPGA Core



+5V, 5A DC/DC for Digital and Analog

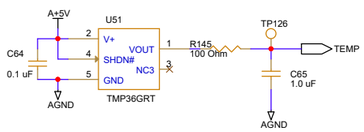


Analog +15V DC/DC

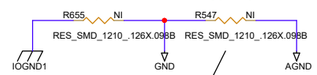


Added Positive 15V DC-DC Converter to support new water valve with higher resistance

Temperature Sensor

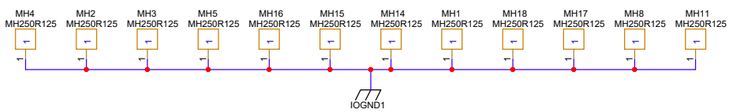


Single Point Connection (close to Power Supplies)

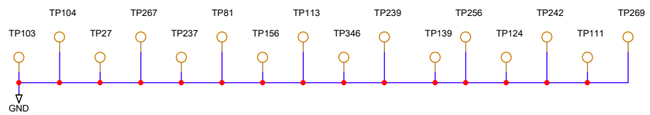


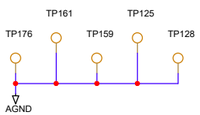
Note: The connection between GND and AGND must be an internal fill (~1" wide) in addition to resistor.

Mounting Holes (connected to Chassis GND through standoffs)



Distribute Test Points Evenly Around Board





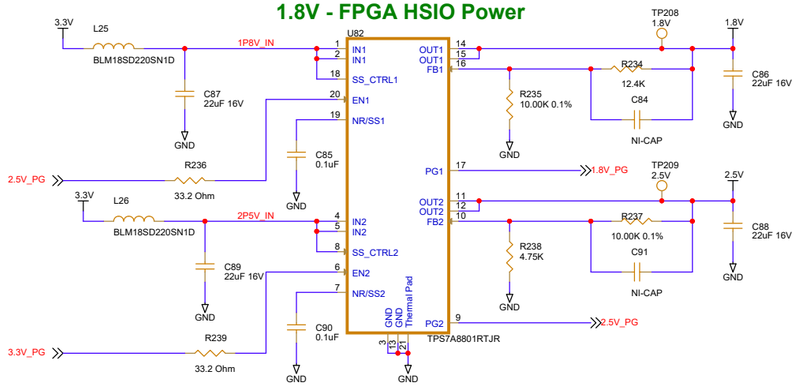
(TEST PTS LOADED)

VARIANT01

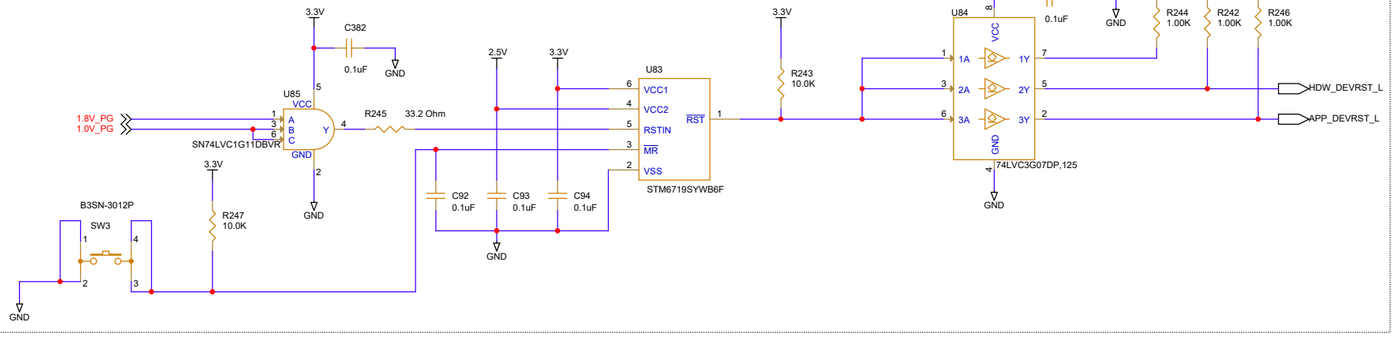
varian	SCALE NONE
	SHEET 40 OF 47
SCH, STN CONTROLLER	
/POWER SUPPLY DC DC CONVERTERS	
DWG NO P1060967	REV D

CM# 0000600021312 Released Ver: 03 Rev: D 11. November 2024

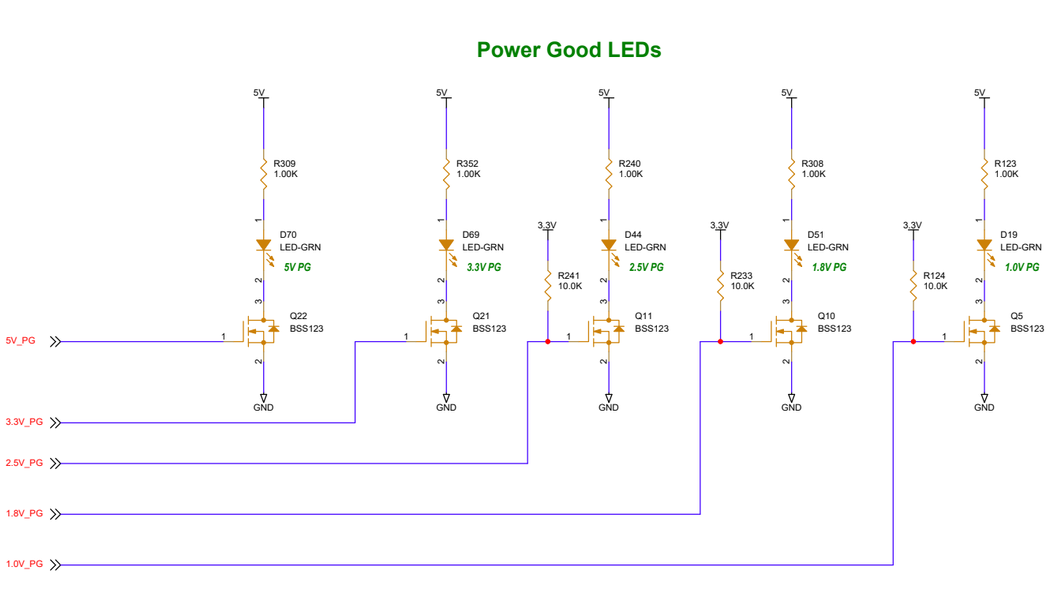
2.5V - FPGA PLL and Clocks
1.8V - FPGA HSIO Power

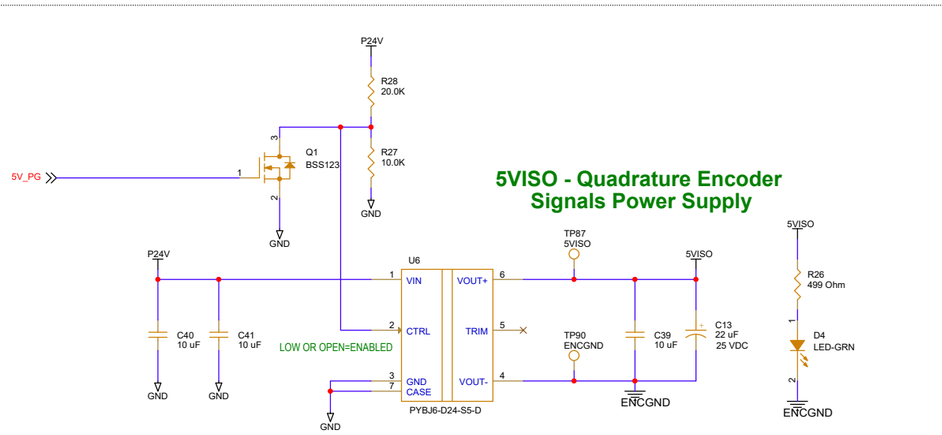


VOLTAGE SUPERVISOR AND PUSH-BUTTON RESET

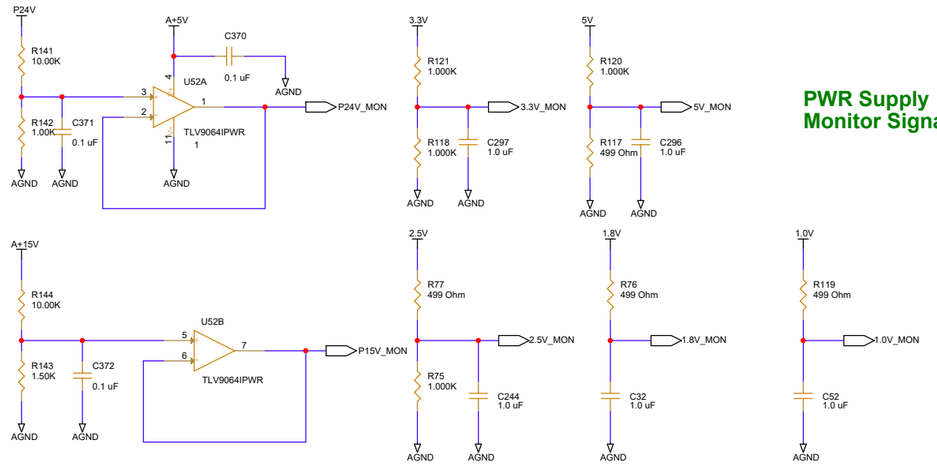


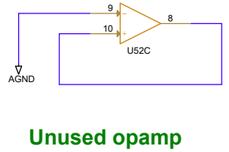
Power Good LEDs



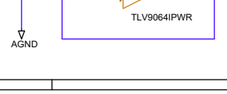


PWR Supply Monitor Signals





Unused opamp



VARIANT01

varian

SCALE	NONE
SHEET	41 OF 47

SCH, STN CONTROLLER

/POWER SUPPLY LDO ISOLATED AND RESET

DWG NO	REV
P1060967	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

EMO_GOOD#
CSPARESW1#
CSPARESW2#
DC_MAIN_DOOR_SW#
NEUTRON_DR_SW1#
NEUTRON_DR_SW2#
CDOS_STS#
CMNR_STS#
GROTPWR_STS#
SPD_AC_DR#

3.3V
C488
0.1 uF
GND
D71
GNT AC STAT
LED-GRN
R657
392 Ohm
U148
SN74LVC1G17DBVR
GROTPWR_STS_N
GROTPWR_STS#
(NON-INVERTING BUFFER)

EMO_GOOD_IN
TP339
R417
39.20K
0.1%
R720
20.0K
C139
0.1 uF
U179
SN74LVC1G14
R416
100K
1000 pF
C165
R719
4.02K

CSPARESW1_IN
TP343
R419
39.20K
0.1%
R718
20.0K
C493
U170
SN74LVC1G14
R418
100K
C166
R717
4.02K

CSPARESW2_IN
TP341
R421
39.20K
0.1%
R716
20.0K
C143
U178
SN74LVC1G14
R420
100K
C167
R715
4.02K

DC_MAIN_DOOR_SW_IN
TP340
R423
39.20K
0.1%
R714
20.0K
C494
U171
SN74LVC1G14
R422
100K
C168
R713
4.02K

NEUTRON_DR_SW1_IN
TP290
R409
39.20K
0.1%
R728
20.0K
C148
U181
SN74LVC1G14
R408
100K
C161
R727
4.02K

NEUTRON_DR_SW2_IN
TP337
R411
39.20K
0.1%
R726
20.0K
C489
U167
SN74LVC1G14
R410
100K
C162
R725
4.02K

CDOS_STS_IN
TP336
R413
39.20K
0.1%
R724
20.0K
C490
U180
SN74LVC1G14
R412
100K
C163
R723
4.02K

CMNR_STS_IN
TP335
R415
39.20K
0.1%
R722
20.0K
C141
U169
SN74LVC1G14
R414
100K
C164
R721
4.02K

GROTPWR_STS_IN
TP344
R425
39.20K
0.1%
R711
20.0K
C491
U177
SN74LVC1G14
R424
100K
C169
R710
4.02K

SPD_AC_DR_IN
TP342
R427
39.20K
0.1%
R709
20.0K
C145
U172
SN74LVC1G14
R426
100K
C170
R708
4.02K

TP292
R429
39.20K
0.1%
R707
20.0K
C147
U176
SN74LVC1G14
R428
100K
XTRA3#
TP291
C171
R706
4.02K

GND

VARIANT01

varian

SCALE	NONE
SHEET	42 OF 47

SCH, STN CONTROLLER
/SYSTEM PWR IF/STAND POWER IF

DWG NO	REV
P1060967	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

LOOP VOLTAGE MONITOR FOR SYSTEM LOOP DEBUG

THE LOOP INPUTS MONITORED IN THIS COLUMN
DO NOT HAVE FILTERS OR REVERSE PROTECTION,
SO IT IS INCLUDED HERE.

GND/AGND
PLANE SEP

PEL_OUT — R315 1.1M — R650 100.0K — C100 1000 pF — U91A OPA4340EA/2K5G4 — R651 100 Ohm — PEL_OUT_MON
C482 0.01 uF, C483 0.1 uF

PEL_IN — R314 1.1M — R654 100.0K — C98 1000 pF — U91B OPA4340EA/2K5G4 — R653 100 Ohm — PEL_IN_MON
C486 0.01 uF

BEL_OUT — R361 1.1M — R701 100.0K — C121 1000 pF — U91C OPA4340EA/2K5G4 — R321 100 Ohm — BEL_OUT_MON
C510 0.01 uF

BEL_IN — R362 1.1M — R699 100.0K — C123 1000 pF — U91D OPA4340EA/2K5G4 — R652 100 Ohm — BEL_IN_MON
C484 0.01 uF

MEL_OUT — R326 1.1M — R693 100.0K — C127 1000 pF — U141A OPA4340EA/2K5G4 — R491 100 Ohm — MEL_OUT_MON
C500 0.01 uF, C502 0.1 uF

MEL_IN — R327 1.1M — R695 100.0K — C125 1000 pF — U141B OPA4340EA/2K5G4 — R324 100 Ohm — MEL_IN_MON
C504 0.01 uF

KVBEL_OUT — R368 1.1M — R769 100.0K — C152 1000 pF — U141C OPA4340EA/2K5G4 — R366 100 Ohm — KVBEL_OUT_MON
C592 0.01 uF

KVBEL_IN — R367 1.1M — R768 100.0K — C153 1000 pF — U141D OPA4340EA/2K5G4 — R492 100 Ohm — KVBEL_IN_MON
C503 0.01 uF, C413 0.1 uF

U92A OPA4340EA/2K5G4 — AGND

U92B OPA4340EA/2K5G4 — AGND

IOGND/AGND
PLANE SEP

PEL_MID — L46 HZ0805E601R — D103 SMAJ33A-13 — C570 100 pF — R328 1.1M — R325 100K — C501 1000 pF — U92C OPA4340EA/2K5G4 — R323 100 Ohm — PEL_MID_MON
C505 0.01 uF

BEL_MID1 — L44 HZ0805E601R — D105 SMAJ33A-13 — C572 100 pF — R318 1.1M — R694 100.0K — C126 1000 pF — U92D OPA4340EA/2K5G4 — R646 100 Ohm — BEL_MID1_MON
C480 0.01 uF

BEL_MID2 — L60 HZ0805E601R — D94 SMAJ33A-13 — C538 100 pF — R316 1.1M — R696 100.0K — C124 1000 pF — U140A OPA4340EA/2K5G4 — R497 100 Ohm — BEL_MID2_MON
C507 0.1 uF, C506 0.01 uF

MEL_MID — L45 HZ0805E601R — D104 SMAJ33A-13 — C571 100 pF — R317 1.1M — R700 100.0K — C122 1000 pF — U140B OPA4340EA/2K5G4 — R322 100 Ohm — MEL_MID_MON
C509 0.01 uF

KVBEL_MID1 — L43 HZ0805E601R — D106 SMAJ33A-13 — C574 100 pF — R319 1.1M — R772 100.0K — C150 1000 pF — U140C OPA4340EA/2K5G4 — R363 100 Ohm — KVBEL_MID_MON1
C596 0.01 uF

KVBEL_MID2 — L61 HZ0805E601R — D93 SMAJ33A-13 — C537 100 pF — R320 1.1M — R770 100.0K — C151 1000 pF — U140D OPA4340EA/2K5G4 — R498 100 Ohm — KVBEL_MID_MON2
C508 0.01 uF

U64A OPA4340EA/2K5G4 — AGND

GATES B-D ON
LOC_LP_MON
SHEET

VARIANT01

varian

SCALE	NONE
SHEET	43 OF 47

SCH, STN CONTROLLER
/NETWORK IF/LOOP MON/SUBSYS LOOP MON

DWG NO	REV
P1060967	D

CM# 0000600021312
Released
Ver: 03
Rev: D
11. November 2024

EMO_OUT

EMO Sense Paths:
1) Modulator
2) Couch and Stand
3) Customer IF

(EMO button on DKB sensed separately)

EMO_IN

DC_MAIN_DOOR_SW#
CSPARESW1#
CSPARESW2#
EMO_GOOD#
GROTPWR_STS#
NEUTRON_DR_SW1#
NEUTRON_DR_SW2#
CDOS_STS#
CMNR_STS#
SPD_AC_DR#

Plane
Separation

EMO LOOP

EMO_IN — 1 — L69 — 4 — EMO_IN_C
EMO_OUT — 2 — L69 — 3 — EMO_OUT_C
CPFC74NP-P503H2A25
C521 22 pF, C520 22 pF
IOGND1

MODULATOR

EMOSNSLP1 — 2 — L64 — 1 — EMOSNSLP1_C
EMOSNSLP1_RT — 3 — L64 — 4 — EMOSNSLP1_RT_C
DLW31SN601SQ2L
C532 22 pF, C531 22 pF
IOGND1

COUCH AND STAND

EMOSNSLP2 — 2 — L65 — 1 — EMOSNSLP2_C
EMOSNSLP2_RT — 3 — L65 — 4 — EMOSNSLP2_RT_C
DLW31SN601SQ2L
C529 22 pF, C528 22 pF
IOGND1

CUSTOMER IF

EMOSNSLP3 — 2 — L66 — 1 — EMOSNSLP3_C
EMOSNSLP3_RT — 3 — L66 — 4 — EMOSNSLP3_RT_C
DLW31SN601SQ2L
C527 22 pF, C526 22 pF
IOGND1

GANTRY ROTATION ENABLE

L68 MH3261-601Y: HW_GANT_ROT_EN_C
C524 100 pF → IOGND1
L67 MH3261-601Y: HW_GANT_ROT_EN_RTN_C
GND — C523 100 pF → IOGND1
C522 100 pF → IOGND1

HDW_GANT_ROT_EN
P24V
U173 BSP742RXUMA1: IN, VBB, VBB, VBB, VBB, GND, OUT, ST
C487 0.1 uF → GND
GND
D80 MBRS140T3
HW_GANT_ROT_EN_PWR
TP294
3.3V
R705 4.99K
HW_GANT_ROT_EN_FLT#
R712 6.04K 1/4W
D79 GNT AC CTRL LED-GRN
GND

EMOSNSLP1_RT → EMOSNSLP_RT; EMOSNSLP → EMOSNSLP1; EMOSNS_CAL, EMOSNS → EMOSNSLP1_CAL, EMOSNS1
EMO LOOP SENSE MOD
EMO LOOP SENSE <SHEET 15>

EMOSNSLP2_RT → EMOSNSLP_RT; EMOSNSLP → EMOSNSLP2; EMOSNS_CAL, EMOSNS → EMOSNSLP2_CAL, EMOSNS2
EMO LOOP SENSE CCH STD
EMO LOOP SENSE <SHEET 13>

EMOSNSLP3_RT → EMOSNSLP_RT; EMOSNSLP → EMOSNSLP3; EMOSNS_CAL, EMOSNS → EMOSNSLP3_CAL, EMOSNS3
EMO LOOP SENSE CUST
EMO LOOP SENSE <SHEET 14>

DC_MAIN_DOOR_SW_C → DC_MAIN_DOOR_SW_IN → DC_MAIN_DOOR_SW#
CSPARESW1_C → CSPARESW1_IN → CSPARESW1#
CSPARESW2_C → CSPARESW2_IN → CSPARESW2#
NEUTRON_DR_SW1_C → NEUTRON_DR_SW1_IN → NEUTRON_DR_SW1#
NEUTRON_DR_SW2_C → NEUTRON_DR_SW2_IN → NEUTRON_DR_SW2#
CDOS_STS_C → CDOS_STS_IN → CDOS_STS#
CMNR_STS_C → CMNR_STS_IN → CMNR_STS#
SPD_AC_DR_C → SPD_AC_DR_IN → SPD_AC_DR#
EMO_GOOD_C → EMO_GOOD_IN → EMO_GOOD#
GROTPWR_STS_C → GROTPWR_STS_IN → GROTPWR_STS#
STAND POWER IF
<SHEET 42>
STAND POWER IF

STAND POWER DISTRIBUTION

J13

TP293
TEST_POINT
TP338
TEST_POINT

HW_GANT_ROT_EN_C	1		
DC_MAIN_DOOR_SW_C	14		
HW_GANT_ROT_EN_RTN_C	2		
	15		
EMO_IN_C	3		
CSPARESW1_C	16		
EMO_OUT_C	4		
CSPARESW2_C	17		
EMOSNSLP3_C	5		
EMO_GOOD_C	18		
EMOSNSLP3_RT_C	6		
SPD_RTN	19		
EMOSNSLP2_C	7		
SPD_AC_DR_C	20		
EMOSNSLP2_RT_C	8		
	21		
EMOSNSLP1_C	9		
	22		
EMOSNSLP1_RT_C	10		
GROTPWR_STS_C	23		
NEUTRON_DR_SW1_C	11		
SPD_RTN	24		
NEUTRON_DR_SW2_C	12		
CDOS_STS_C	25		
CMNR_STS_C	13		

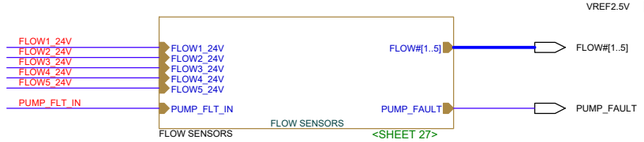
5747846-6

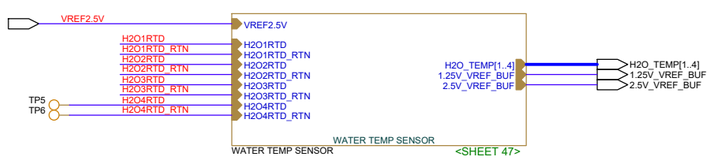
26 — 27 — J13_SHLD
R77 100K
C598 0.01 uF → IOGND1

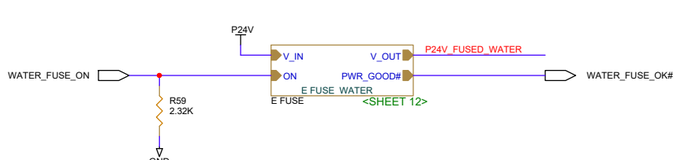
VARIANT01

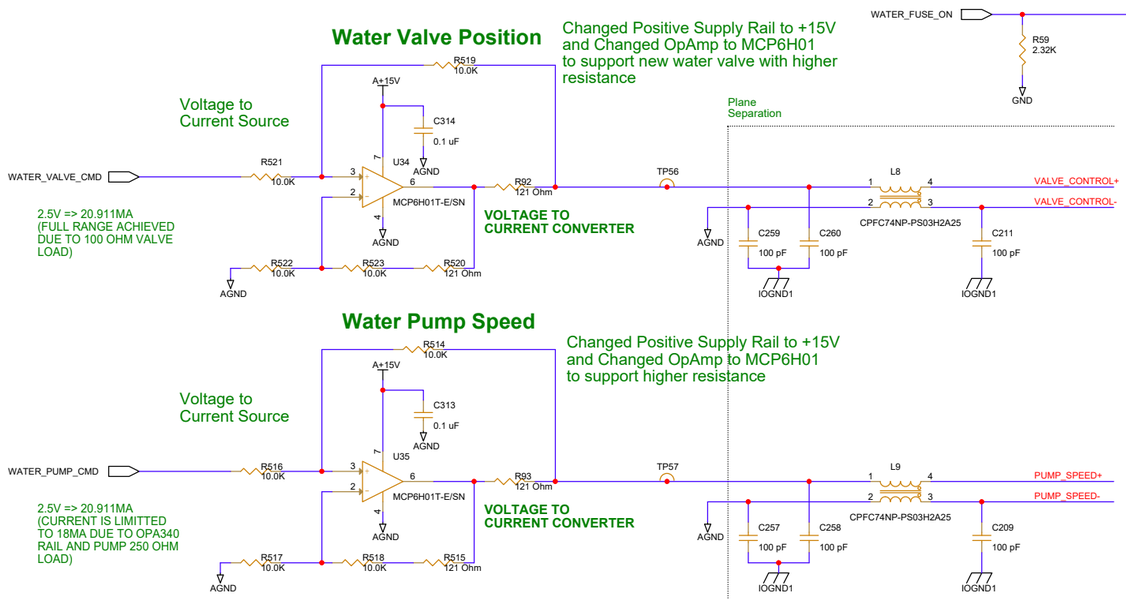
varian	SCALE: NONE
	SHEET: 44 OF 47
SCH, STN CONTROLLER	
/SYSTEM PWR IF SYSTEM PWR IF	
DWG NO: P1060967	REV: D

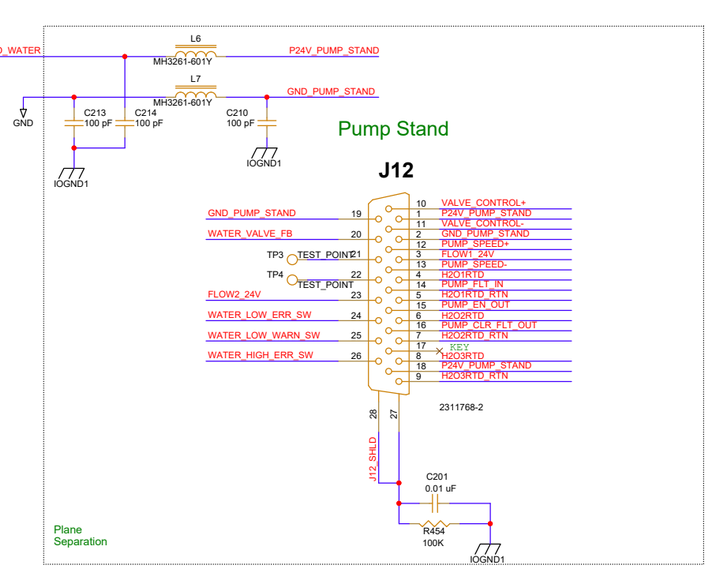
CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

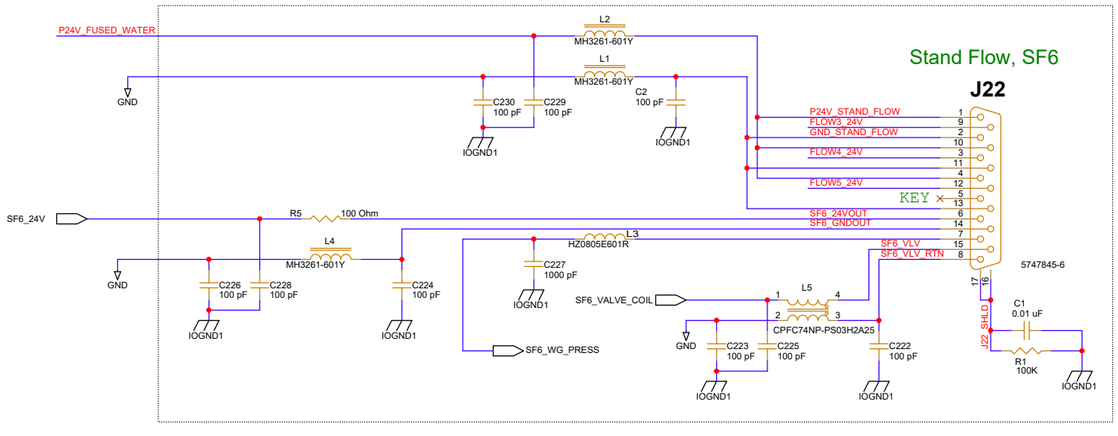


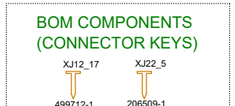












VARIANT01

varian

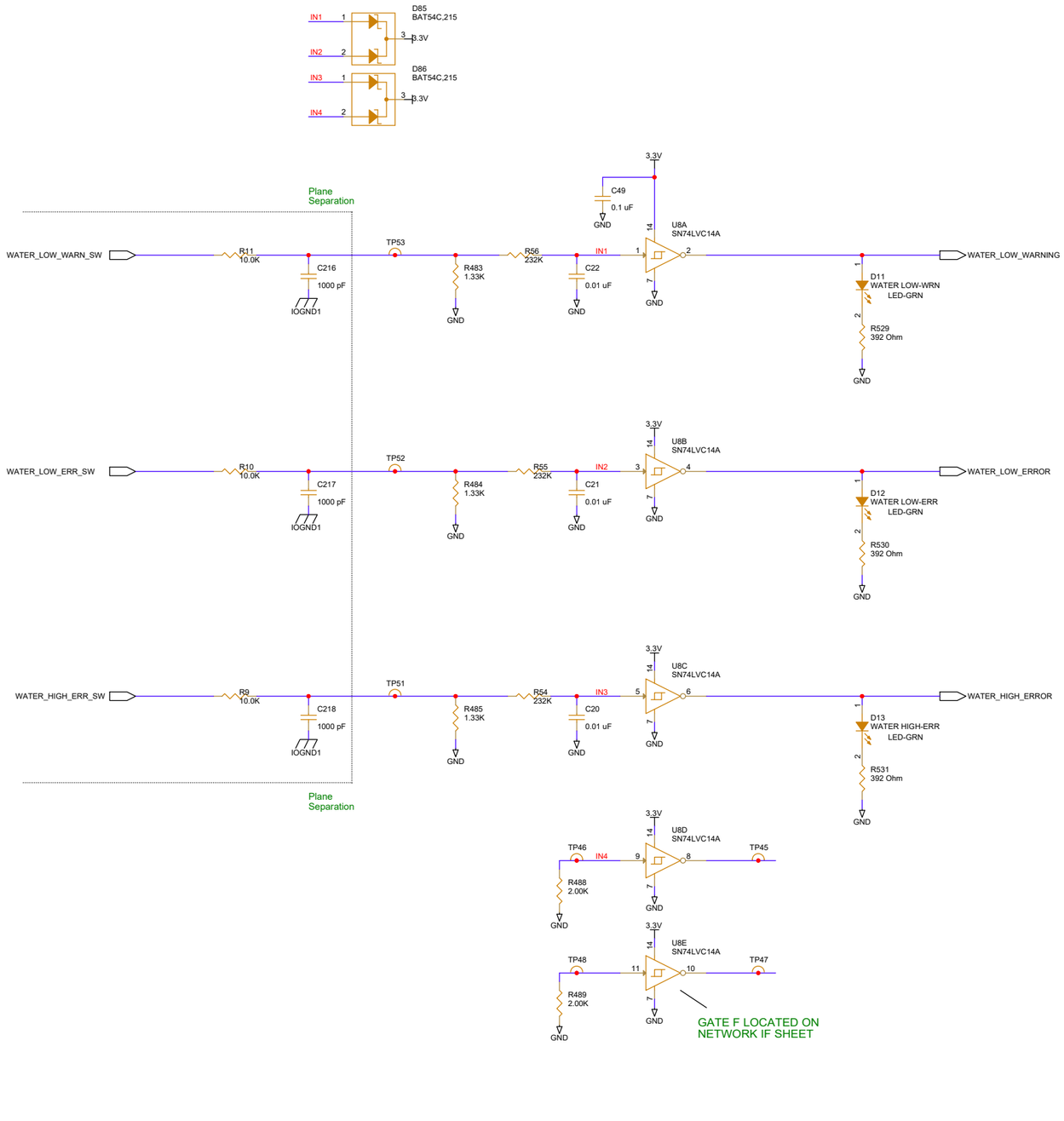
SCALE	NONE
SHEET	45 OF 47

SCH, STN CONTROLLER

/WATER IF

DWG NO	REV
P1060967	D

CM# 000060021312 Released Rev: D Ver: 03 11. November 2024



VARIANT01

varian

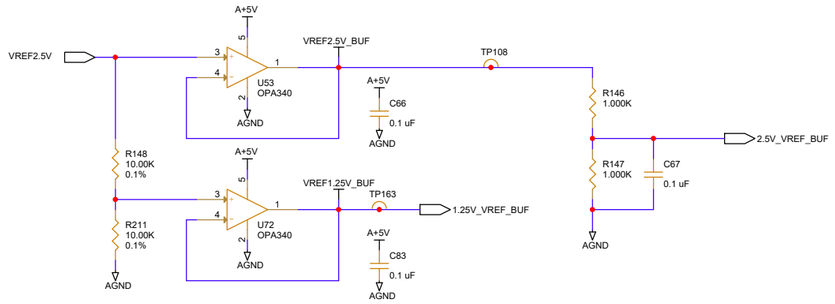
SCALE	NONE
SHEET	46 OF 47

SCH, STN CONTROLLER

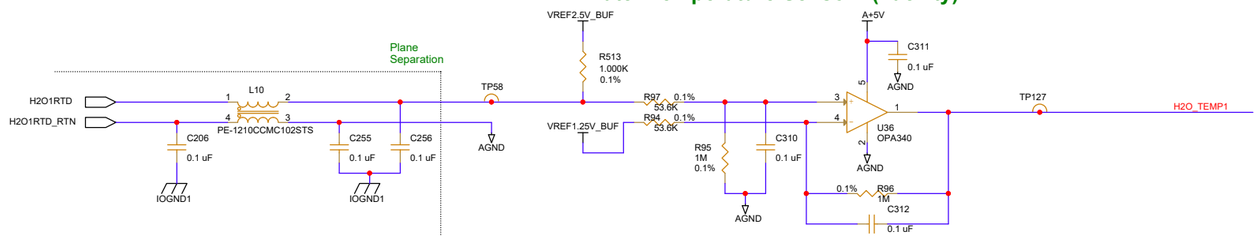
/WATER IF/WATER LEVEL

DWG NO	REV
P1060967	D

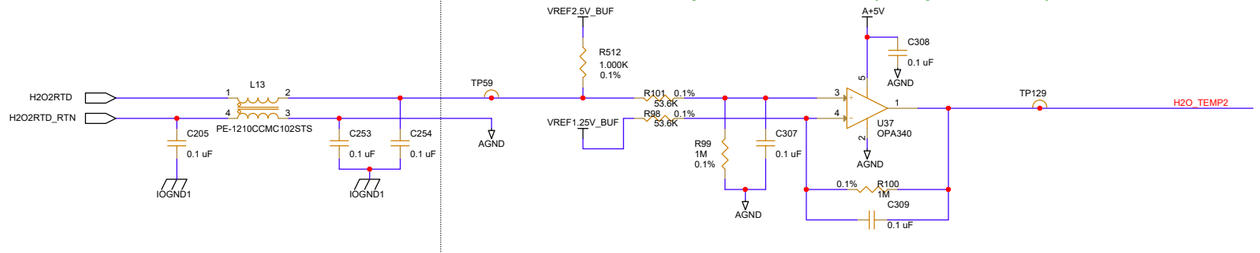
CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024



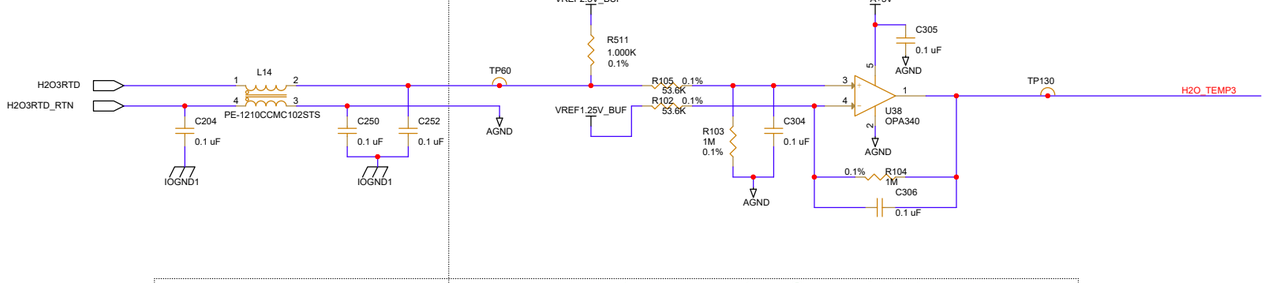
Water Temperature Sensor1 (Facility)



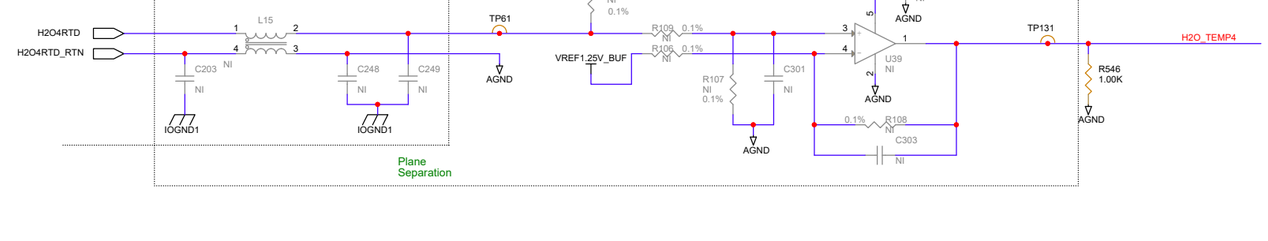
Water Temperature Sensor2 (Pump Stand Out)



Water Temperature Sensor3 (Pump Stand Return)



Water Temperature Sensor4 (Not Used)



H2O_TEMP[1..4]

CIRCUIT BEHAVIOR WITH 1K RTD (AT 0C)

TEMP (C)	RTD RESISTANCE (OHMS)	AMPLIFIER OUT (V)
0	1000	0
10	1038	0.44
20	1077	0.865
30	1115	1.273
40	1154	1.667
50	1192	2.048
60	1231	2.415

VARIANT01

varian

SCALE	NONE
SHEET	47 OF 47

SCH, STN CONTROLLER

/WATER IF/WATER TEMP SENSOR

DWG NO	REV
P1060967	D

CM# 000060021312 Released Ver: 03 Rev: D 11. November 2024

Signature File

varian
A Siemens Healthineers Company

Document: P1060967/SCH/000/03
Description: SCH, STAND CONTROLLER

Change Master Number: 60021312
ECN Number: 200109931
ECN Description:

Signature list

Date	Time	User	Status
11, November 2024	18:43:58	Gary Yen	Verification Rel
06, November 2024	00:56:16	Ge Song	Approved
06, November 2024	00:28:31	Kevin Greenberg	In Eng Approval
06, November 2024	00:03:24	Gary Yen	In Checking
05, November 2024	18:44:22	Gary Yen	In Drafting
04, November 2024	19:28:01	Gary Yen	In Works

Signature File

varian
A Siemens Healthineers Company

Document: P1060967/SCH/000/03
Description: SCH, STAND CONTROLLER

Change Master Number: 60021312
ECN Number: 200109931
ECN Description:

Signature list

Date	Time	User	Status
11, November 2024	18:45:05	Gary Yen	Released
11, November 2024	18:43:58	Gary Yen	Verification Rel
06, November 2024	00:56:16	Ge Song	Approved
06, November 2024	00:28:31	Kevin Greenberg	In Eng Approval
06, November 2024	00:03:24	Gary Yen	In Checking
05, November 2024	18:44:22	Gary Yen	In Drafting
04, November 2024	19:28:01	Gary Yen	In Works