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*Content: This document describes the procedure for functional testing of the Stand Controller Assy., P/N P1060966xxx.*

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# PURPOSE

This document provides step-by-step functional testing methods for automatic testing of the Stand Controller Assembly at Jabil’s Tempe, Arizona plant.

# SCOPE

This document constitutes the functional test plan for the Stand Controller Assy., P/N 100014296-03. This document describes the testing procedures in a high level format without making detailed references to the test software, instrument configuration or ATE stimulus and response signal routing. Units that meet all of the requirements of this document shall be accepted as functional.

# REFERENCE DOCUMENTS

* Stand Controller Board 1060967-P Schematics P/N 1060967 Rev. D
* Beam Enable Loop Test Procedure (Stand Controller) Doc No. 100014296-BEL Test Procedure Rev. A

# DEFINITIONS and CONVENTIONS

## Definitions

* **ADC** – Analog-to-Digital Converter
* **ATE** – Automatic Test Equipment
* **ESD** – Electro-Static Discharge
* **FFT** – Fast Fourier Transform
* **GND** – Ground/UUT 0V Reference
* **GPIO** – General Purpose Input/output
* **IF** – Interface
* **LVPECL** – Low Voltage Positive Emitter Coupled Logic
* **nC** – 10-9 Coulombs
* **P/N** – Part number
* **PWB** – Printed Wiring Board
* **Sps** – Samples-per-second (1kSps = 1000 Samples-per-second)
* **STN** – Stand Controller  **UUT** – Unit Under Test
* **VDC** – Volts Direct Current
* **Vpp** – Volts Peak-to-Peak

## Conventions

### A reference to setting the state of a control signal to a specific logic level refers to a write operation to the UUT’s FPGA to set the state of a register for signals connected to the UUT’s FPGA.

### A reference to reading the state of a status signal for a specific logic level refers to a read operation from the UUT’s FPGA to get the state of input signals connected to the UUT’s FPGA.

# EQUIPMENT REQUIRED

The following list contains the required test equipment for functional testing of the BGM Controller assembly on the SOCRATES ATE System.

## Test Equipment

5.1.1 Agilent N6702A Power Supply Main Frame

5.1.2 Agilent N6743B Power Supply Module; 20V @ 5.0A

5.1.3 Agilent N6744B Power Supply Module; 35V @ 3.0A

5.1.4 Agilent N6745B Power Supply Module; 60V @ 1.6A

5.1.5 Agilent 6674A Power Supply Module; 60V @ 35A

5.1.6 Agilent 34401A DMM

5.1.7 National Instrument PXI-6509 96-Channel DIO Module

5.1.8 National Instrument PXI-2527 Multiplexer Module

5.1.9 National Instrument PXI-2529 Switch Matrix Module

5.1.10 National Instrument PXI-2568 Relay Module

5.1.11 National Instruments PXI-6704 DAC Module

## Test Software/Firmware

5.2.1 Stand Controller Test Software, P1060966-TSW.

5.2.2 Stand Controller Test Actel Firmware, P1060966-TFW.

5.2.3 Actel Test Firmware programmed with FlashPro.

# PRE-TEST PROCEDURES

***Warning: ESD Sensitive devices present* -** Ensure proper grounding procedures are followed while handling/testing this and all ESD sensitive assemblies as defined in IPC-A-610.

## Visual Inspection

6.1.1 Visually inspect the Stand Controller to be tested for obvious signs of wrong, missing or improperly oriented parts (Refer to Assembly Drawing).

6.1.2 Also inspect for signs of contamination and poor workmanship including soldering defects (bridges, splashes, balls, unsoldered pins, flux build-up, etc.) and improper mounting of parts. Pay specific attention to ensure that through-hole parts and sockets are mounted flush to the board.

6.1.3 Any discrepancies must be corrected before proceeding.

# TEST SETUP

## ATE/Fixture Connections and Software Loading - Performed once for each lot.

7.1.1 Ensure that all instruments on the SOCRATES ATE System have been reset.

7.1.2 Ensure that the engaging handle on the ATE Interface is in the up (disengaged) position.

7.1.3 Place the Stand Controller Test Fixture, P/N 100014296-FX, on to the interface with the fixture hinges facing the machine.

7.1.4 Once the fixture is properly seated on the interface, then push the interface handle down to engage the fixture.

# TEST PROCEDURE

The following procedure contains step by step instructions for testing the UUT. Although this test was developed exclusively to be performed on a specific ATE, it does not detail the specific ATE related operations such as signal routing. This information could be gathered by inspection of the test software and fixture drawing.

## Initial Power On

DESCRIPTION:

The Power Input at J1 consists of a hot swap controller (U174), which will enable power to the UUT when the input voltage is greater than +17.65V ± 0.35V by turning on the U174. The hot swap controller will also limit the inrush current by ramping the gate voltage of U174 to control the slew rate of the input voltage to the internal power circuitry of the board. The slew rate of the gate is determined by the gate capacitor C519 and is calculated by the equation dV/dt = 10uA/ C519 = 2.13V/ms.

The input supply voltage will first be set to +24V and the inrush current amplitude and slope will be measured to be within the allowable tolerance. The input supply voltage will then be set to +16.5V and the initial supply current will be measured for less than 100mA to verify that the hot swap controller has not enabled power to the UUT. The input supply voltage will then be increased in increments of 0.1V, not to be greater than 24V, and for each step, the current will be measured. When the supply current measures greater than 0.16A, the power has been enabled to the UUT and the supply voltage will be verified to be within the turn on window. The input supply voltage will be set to the normal operating voltage of +24V, and the supply voltage and current will be measured to be within tolerance. If any failures occur during the above tests, then the test will be aborted and the UUT must be repaired before continuing.

PROCEDURE:

### Before power up, test continuity between J3\_16 to J4\_16, between J29\_15 to J30\_15, verify they’re 0ohm to 10ohm.

### Power on UUT.

### The Power Input voltage at J1 will be set to +16.5V and the supply current will be measured for less than 50mA.

### The supply voltage will be increased in increments of 0.1V until the supply current is greater than 0.16A. The supply voltage will be measured for (17.40VDC, 18.00VDC).

### Turn on all power supply

### Check voltage rails LEDs. A prompt will be displayed to the user querying whether D82, D39, D72, D16, D4, D19, D70, D69, D44 and D51 are illuminated green. A response of “Yes” is expected.

## FPGA Firmware Load

DESCRIPTION:

The UUT has two FPGAs U47 for the HDW FPGA and U59 for the APP FPGA. The part number of U47 is MPF050T-FCVG484E and the part number of U59 is MPF100T-FCG484E. FPGAs’ ID code are read via USB to JTAG interface (J40 for the APP FPGA and J35 for the HDW FPGA). A FPGA programming pod connected to J40 is used to perform downloading the special build test firmware for the APP FPGA via the JTAG interface. Once the firmware downloading is completed, the FPGA \_DONE signal is driven high.

After finishing all ATE tests, the special build test firmware of APP FPGA is erased.

If the loading of the test firmware into the APP FPGA fails, then the test will be aborted and the UUT must be repaired before continuing.

A FPGA programming pod connected to J35 is used to perform downloading the hardwired firmware into HDW FPGA via the JTAG interface. Once the firmware downloading is completed, the FPGA \_DONE signal is driven high.

If the loading of the test firmware into the HDW FPGA fails, then the test will be aborted and the UUT must be repaired before continuing.

PROCEDURE:

### Visual check the APP FPGA and HDW FPGA part number.

### APP FPGA Test firmware is loaded automatically using FPGA programming pod Actel FlashPro 4 present in the following folder: TBD to the configuration flash of the APP FPGA.

### When complete, the FPGA\_DONE is HIGH, A prompt will be displayed to the user querying whether LED D43 is on. A response of “Yes” is expected.

### HDW FPGA firmware is loaded automatically using FPGA using FPGA programming pod Actel FlashPro 4 present in the following folder: TBD to the configuration flash of the HDW FPGA.

## Reset Test

The reset function is tested by pushing the reset button (SW3), it resets the APP FPGA and HDW FPGA.

PROCEDURE:

### Power on UTT.

### Check FPGA DONE LEDs. A prompt will be displayed to the user querying whether D43 is illuminated green and D33 is off. A response of “Yes” is expected.

### Push Reset switch SW3 for ~1 second.

### Check FPGA DONE LEDs. A prompt will be displayed to the user querying whether D43 is off and D33 is illuminated green. A response of “Yes” is expected.

### Release the switch.

### Check FPGA DONE LEDs. A prompt will be displayed to the user querying whether D43 is illuminated green and D33 is off, and D21 (HDW\_FPGA\_STAT\_LED2) blind once. A response of “Yes” is expected.

## ADC Test

The interface to the ADC (U16/U17) will be tested by reading the measurements of the voltage rail monitors. The remaining channels will be verified during their corresponding test sections. The following channels will be read from the A/D Converter:

PROCEDURE:

### The P24V\_MON Monitor (AD\_IN12) will be read for +24VDC ± 10%.

### The 5V\_MON Monitor (AD\_IN15) will be read for +5VDC ± 10%.

### The 3.3V\_MON Monitor (AD\_IN16) will be read for +3.3VDC ± 10%.

### The P15V\_MON Monitor (AD\_IN17) will be read for +1.363VDC ± 10%.

### The 2.5V\_MON Monitor (AD\_IN19) will be read for +2.5VDC ± 10%.

### The 1.0V\_MON Monitor (AD\_IN24) will be read for +1.0VDC ± 10%.

### 8.3.12 The scale factor for the temperature sensor is 10mV/C. The TEMP Monitor (AD\_IN21) will be read for +0.75VDC ± 0.1V (for 25C ± 10C).

### The 1.8V\_MON Monitor (AD\_IN23) will be read for +1.8VDC ± 5%.

## Serial EEPROM

DESCRIPTION:

It’s programed by system commands, and it should be programmed by APP FPGA for ATE test purpose. Need APP FPGA test firmware and ATP test flow.The Serial EEPROM(U46) will be tested by programming all 8kB and reading back the data to verify that the contents are correct. The EEPROM will then be erased (all bytes set to 0xFF) and read back to verify the device is blank. The SPI interface to the EEPROM will be configured for a bit rate of 2Mbps.

For testing purposes, access to the EEPROM will be performed as word (16-bit) transfers, resulting in 4k word memory locations. The data used to fill the EEPROM is specified by **Equation 8-2**.

*W*=1+16*n*

#### Equation 8-1: EEPROM Data

Where W is the data word and n is the word index (0 to 4095).

When programming the EEPROM, a sequential page write operation will be used for the 256 pages, which will allow for writing 16 words per write cycle per page. **Figure 8-1** illustrates the algorithm used for programming the EEPROM. When reading back the data from the EEPROM, a sequential page read operation will be used to read each page per read cycle.

Send the WREN

Command

Write

Page Data

(16

Words

)

Read Status

Register

WIP = 0?

NO

All Pages

Programmed?

Send the WRDI

Command

Programming

Complete

Successfully

YES

NO

YES

Has more

than 10ms

passed?

Terminate Programming:

FAILED!

NO

YES

#### Figure 8-1: Page Write Sequence

PROCEDURE:

### The Serial EEPROM will be programmed with the 4k words of test data and will be verified to complete successfully.

### The 4k words of the Serial EEPROM will be read and verified to be equal to the test data written to the device.

### 8.5.3 The Serial EEPROM will be erased and will be verified to complete successfully.

### 8.5.4 The 4k words of the Serial EEPROM will be read and each word will be verified to equal 0xFFFF.

## DAC Tests

DESCRIPTION

DAC (U3) is tested by setting the DAC voltage from APP FPGA debug port SPI interface to varying voltage values between 0 to +4.5V and reading the DAC\_MON voltage at AD\_IN38 of A/D converter.

PROCEDURE:

### With DAC voltage Set to 0.5V, the DAC\_MON shall be read for 0.5V ± 0.2V.

### With DAC voltage Set to 2.5V, the DAC\_MON shall be read for 2.5V ± 0.2V.

### With DAC voltage Set to 4.5V, the DAC\_MON shall be read for 4.5V ± 0.2V.

## Electronic Fuse Test

DESCRIPTION

The power supply for the DKB, PEND and Water Interface is provided by a hot swap controller which is enabled by DKB\_FUSE\_ON, PEND\_FUSE\_ON and WATER\_FUSE\_ON respectively provided by the FPGA. The FPGA will enable these signals and report the status of DKB\_FUSE\_OK#, PEND\_FUSE\_OK# and WATER\_FUSE\_OK# status signal. The tester checks the voltage P24V\_DKB, PENDANT\_24V and P24V\_FUSED\_WATER to verify that the hot swap controller and power switch are functioning as expected.

PROCEDURE:

### DKB\_FUSE\_ON, PEND\_FUSE\_ON and WATER\_FUSE\_ON are set to logic 0.

### A prompt is displayed to the user querying whether LEDs D68, D34, and D5 are OFF. A response of “yes” is expected.

### DKB\_FUSE\_OK# is read for logic 1.

### PEND\_FUSE\_OK# is read for logic 1.

### WATER\_FUSE\_OK# is read for logic 1.

### P24V\_DKB at J9-8 shall be measured for a value between ±0.5V.

### PENDANT\_24V at J25-5 shall be measured for a value between ±0.5V.

### P24V\_PUMP\_STAND at J12-1 shall be measured for a value between ±0.5V.

### P24V\_PUMP\_STAND at J12-18 shall be measured for a value between ±0.5V.

### P24V \_STAND\_FLOW at J22-1 shall be measured for a value between ±0.5V.

### DKB\_FUSE\_ON shall be set for logic 1.

### DKB\_FUSE\_OK# shall be read for logic 0.

### P24V\_DKB at J9-8 shall be measured to be between 23.0V and 25.0V.

### PEND\_FUSE\_ON shall be set to logic 1.

### PEND\_FUSE\_OK# shall be read for logic 0.

### PENDANT\_24V at J25-5 shall be measured to be between 23.0V and 25.0V.

### WATER\_FUSE\_ON shall be set for logic 1.

### A prompt is displayed to the user querying whether LEDs D34, D68 and D5 are ON. A response of “yes” is expected.

### WATER\_FUSE\_OK# shall be read for logic 0.

### P24V\_PUMP\_STAND at J12-1 shall be measured to be between 23.0V and 25.0V.

### P24V\_PUMP\_STAND at J12-18 shall be measured to be between 23.0V and 25.0V.

### P24V \_STAND\_FLOW at J22-1 shall be measured to be between 23.0V and 25.0V.

### DKB\_FUSE\_ON, PEND\_FUSE\_ON and WATER\_FUSE\_ON shall be set to logic 0.

## System Power Interface: EMO Loop Sense

DESCRIPTION

There are 3 EMO loop sense circuits in the Stand Controller which detect the engagement of switches. These are the Couch and Stand EMO Sense Loop, the Customer EMO Sense Loop and the Modulator & DKB EMO Sense Loop. When engaged, the switches in each of these loops short scaled resistors in order to change the voltage read across the output of the loops. The source current through each loop is constant and set by the combination of LM317L 1.25V regulators and 121ohm series resistors to produce 10mA. The resistance of the switch resistors is integer multiples of each other (R, 2R, 4R and 8R) and are placed in series with the current source. The change in resistance is sensed when each switch shorts these resistances out and alters the voltage seen across the current source. A voltage follower circuit detects this change and the A/D converter reads the corresponding voltages through inputs AD\_IN2, AD\_IN4, and AD\_IN6, for each respective loop. A similar voltage follower circuit for calibration sense at the return line of each EMO loop circuit can also be checked by the A/D converter through channels AD\_IN1, AD\_IN3, AD\_IN5, respectively, to verify the constant current on the primary EMO sense. The current through the loop at the return is measured across 100ohm resistors to ground and this voltage will always correspond to a value of approximately 1V.

The Stand Controller EMO loop sense circuits are configured for resistance values of 42.2ohm, 84.5ohm, 169ohm and 340ohm. The tester will utilize the same switches and resistor configuration and toggle the switches in different combinations to simulate the actuation of the EMO switches. The voltage at the EMO sense loops will be measured for the combinations and the A/D converter will be checked that it measures the correct corresponding voltages to verify.

Nominal source current = 10.3mA

#### Table 8.7.23-1: EMO Sense Loop Expected Sense Voltage

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| EMO Sense Loop Tester Switch Resistors | | | |  |  |
| R1 | R2 | R3 | R4 | 100ohm | EMOSNS  Voltage |
| 42.2 | 84.5 | 169 | 340 | 100 | 2.129 |
|  | 84.5 | 169 | 340 | 100 | 2.007 |
|  |  | 169 | 340 | 100 | 1.762 |
|  |  |  | 340 | 100 | 1.273 |
|  |  |  |  | 100 | 0.289 |

**Table 8.7.23-2: EMO Sense Loop Expected Calibration Sense Voltage**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| R1 | R2 |  | R3 | R4 | 100ohm | EMOSNS\_CAL  Voltage |
| 42.2 |  | 84.5 | 169 | 340 | 100 | 1.022 |
|  |  | 84.5 | 169 | 340 | 100 | 1.023 |
|  |  |  | 169 | 340 | 100 | 1.023 |
|  |  |  |  | 340 | 100 | 1.024 |
|  |  |  |  |  | 100 | 1.027 |

The high-side output voltage and return loop sensing calibration voltage is tested by measuring the expected output voltages at current sources (U165, U151 and U152) and calibration resistors (R407, R437 and R438).

PROCEDURE:

### Connect switch load resistor of 500ohm EMOSNSLP2\_C at J13-7 and EMOSNSLP2\_RT\_C at J13-8

### Read the voltage at EMOSNSLP2\_CAL with the A/D converter at channel AD\_IN3. The voltage should read 1V +/-10%

### Read the voltage at EMOSNS2 with the A/D converter at channel AD\_IN4. The voltage should read 1.75V +/-0.1V

### Connect switch load resistor of 500ohm across EMOSNSLP3\_C at J13-5 and EMOSNSLP3\_RT\_C at J13-6

### Read the voltage at EMOSNSLP3\_CAL with the A/D converter at channel AD\_IN5. The voltage should read 1V +/-10%

### Read the voltage at EMOSNS3 with the A/D converter at channel AD\_IN6. The voltage should read 1.75V +/-0.1V

### Connect switch load resistor of 500ohm across EMOSNSLP1\_C at J13-9 and EMOSNSLP1\_RT\_C at J13-10

### Read the voltage at EMOSNSLP1\_CAL with the A/D converter at channel AD\_IN1. The voltage should read 1V +/-10%

### Read the voltage at EMOSNS1 with the A/D converter at channel AD\_IN2. The voltage should read 1.75V +/-0.1V

### Set tester’s DAC4 to output 5V voltage across J13\_3 (EMO\_IN\_C) and J13\_4 (EMO\_OUT\_C).

### Measure voltage across J9\_5 (EMOLP\_DKB\_SRC) and J9\_13 (EMOLP\_DKB\_RTN), verify the voltage is 5V +/- 0.5V.

### Reset tester’s DAC4 to output 0V.

## Network Interface: Enable Loops and Loop Monitors

DESCRIPTION

There are 3 types of enable loops within the Stand Controller. These loop types and their differences are outlined in the table below.

#### Table 8.8.12-1: Enable Loop Types

|  |  |  |  |
| --- | --- | --- | --- |
| **Type** | **Loop Control Switch** | **Remote Sensing** | **Loops Used** |
| ENABLE LOOP USER | No | No | DKB, Couch (loop segment for pendant and side panels only) |
| ENABLE\_LOOP | Yes | Yes | BEL, MEL, PEL |
| ENABLE\_LOOP\_NO\_SNS | Yes | No | KVBEL |

There are several main elements of the enable loops: A loop control switch, source and sink status, remote sense input, and current monitor. The ENABLE LOOP USER and ENABLE\_LOOP\_NO\_SNS have subsets of these elements. The ENABLE LOOP USER does not contain the loop control switch or remote sense circuitry. The ENABLE\_LOOP\_NO\_SNS circuit does not contain the remote sense circuitry.

The Beam Enable Loop (BEL), Motion Enable Loop (MEL), Power Enable Loop (PEL) have all of the full ENABLE\_LOOP circuitry. They are also duplicated in the Local Network Interface and the information from both the Network and Local Network interfaces must match at all times. The Remote Sense allows the current from the Network loop to be conveyed to the Local Network loop and vice versa.

To test each ENABLE\_LOOP, the switch control will be toggled and the voltage of each 1.25V reference will be measured. The A/D converter will be used to verify the measured voltage. The tester will then connect a low impedance switch or relay that allows the enable loop to be closed, each loop’s ENLP\_OUT will be connected to ENLP\_IN with a series switch. The detected source and sink states will be checked by the FPGA and the measured enable loop current will be checked by measuring the voltage at ENLP\_CURRENT for each loop through the A/D converter inputs.

|  |  |  |
| --- | --- | --- |
| Specially, for the Beam Enable Loop, ENLP\_OUT will be toggled connecting to and disconnecting from ENLP\_IN at different points, and test makes the above measurements | | |
| under all conditions. |  | |
| **Please refer to the separate procedure (Doc No. 100014296-BEL Test Procedure Rev. A)** | | |
| **for details of Beam Enable Loop test.** | |  |

The A/D converter will be used to also read the state of the switch voltages to verify the state of the enable loops.

PROCEDURE:

### Before test BEL loop, ENLP\_OUT will be connected to ENLP\_IN by connecting the J3\_13 to J3\_4, J4\_13 to J4\_4, J9\_3 to J9\_11, J29\_7 to J29\_8, and J30\_7 to J30\_8 with relays to make the loop close.

### Before test PEL loop, ENLP\_OUT will be connected to ENLP\_IN by connecting the J3\_11 to J3\_2, J4\_11 to J4\_2, J29\_3 to J29\_4, and J30\_3 to J30\_4 with relays to make the loop close.

### Before test MEL loop, ENLP\_OUT will be connected to ENLP\_IN by connecting the J3\_12 to J3\_3, J4\_12 to J4\_3, J29\_5 to J29\_6, and J30\_5 to J30\_6 by relays to make the loop close.

### Before test KVBEL loop, ENLP\_OUT will be connected to ENLP\_IN by connecting the J3\_25 to J3\_26, and J4\_25 to J4\_26 by relays to make the loop close.

### Before test COUCH loop, ENLP\_OUT will be connected to ENLP\_IN by connecting the J3\_18 to J3\_9 by relays to make the loop close.

### Before test DKB loop, ENLP\_OUT will be connected to ENLP\_IN by connecting the J4\_6 to J4\_14 by relays to make the loop close.

### A prompt will be displayed to the user to Configure switches SW2 to OFF position.

### A prompt will be displayed to the user to Configure switches SW3 to OFF position.

### A prompt will be displayed to the user to Configure switches SW1 to OFF position.

### Signals at J13 EMO\_GOOD\_IN, CSPARESW1\_IN, CSPARESW2\_IN, DC\_MAIN\_DOOR\_IN, NEUTRON\_DR\_SW1\_IN, NEUTRON\_DR\_SW2\_IN, CDOS\_STS\_IN, CMNR\_STS\_IN, GROTPWR\_STS\_IN, SPD\_AC\_DR\_IN shall be set to 0V through relay.

### FPGA\_LOOP\_CTRL shall be read for a value of 0x00.

### A prompt will be displayed to the user querying whether LEDs D52 through D67 are OFF. A response of “Yes” is expected.

### An input voltage of 24V shall be applied to EMO\_GOOD\_IN at J13-18.

### A 250Ω resistor shall be connected to J25-5 PENDANT\_24V to J25-2 PENDANT\_GND by switch/relay.

### CONN\_INPUTS register bits EMO\_GOOD from FPGA shall be read for logic 1.

### Signals FPGA\_BMENLP\_CTRL, FPGA\_HW\_BMENLP\_CNTL, FPGA\_KVBMENLP\_CTRL, FPGA\_MTNENLP\_CTRL, FPGA\_PWRENLP\_LOC\_CTRL, FPGA\_BMENLP\_LOC\_CTRL, FPGA\_MTNENLP\_LOC\_CNTL shall be set to logic 0.

### FPGA ENCODER\_FUSE ON bit shall be set to logic 1 (FPGA CONN\_OUTPUTS register sets to 0x40)

### FPGA INTERNAL\_STAT register bit PENDANT\_INST shall be read for logic 1.

### ATE switches/relays shall close the PEL, BEL, MEL, PEL\_LOC, BEL\_LOC and MEL\_LOC enable loops.

### FPGA PWRENLP\_CTRL shall be read for logic 0.

### FPGA BMENLP\_CTRL shall be read for logic 0.

### FPGA MTNENLP\_CTRL shall be read for logic 0.

### FPGA KVBMENLP\_CTRL shall be read for logic 0.

### PEL\_OUT\_MON thru ADC from U41 shall be measured to be less than 0.1V.

### PEL\_MID\_MON thru ADC from U41 shall be measured to be less than 0.1V.

### PEL\_IN\_MON thru ADC from U41 shall be measured to be less than 0.1V.

### The combination of BMENLP\_CURR through ADC(AD\_IN28) and BMENLP\_LOC\_CURR through ADC(AD\_IN33) shall be measured to be less than 0.02V.

### BEL\_OUT\_MON thru ADC from U41 shall be measured to be less than 0.1V.

### BEL\_MID1\_MON thru ADC from U41 shall be measured to be less than 0.1V.

### BEL\_MID2\_MON thru ADC from U41 shall be measured to be less than 0.1V.

### BEL\_IN\_MON thru ADC from U41 shall be measured to be less than 0.1V.

### MEL\_OUT\_MON thru ADC from U41shall be measured to be less than 0.1V.

### MEL\_MID\_MON thru ADC from U40 shall be measured to be less than 0.1V.

### MEL\_IN\_MON thru ADC from U40 shall be measured to be less than 0.1V.

### KVBEL\_OUT\_MON thru ADC from U40 shall be measured to be less than 0.1V.

### KVBEL\_MID1\_MON thru ADC from U40 shall be measured to be less than 0.1V.

### KVBEL\_MID2\_MON thru ADC from U40 shall be measured to be less than 0.1V.

### KVBEL\_IN\_MON thru ADC from U40 shall be measured to be less than 0.1V.

### PEL\_LOC\_OUT\_MON thru ADC from U54 shall be measured to be less than 0.1V.

### PEL\_LOC\_MID\_MON thru ADC from U54 shall be measured to be less than 0.1V.

### PEL\_LOC\_ IN\_MON thru ADC from U54shall be measured to be less than 0.1V.

### BEL\_LOC\_OUT\_MON thru ADC from U54 shall be measured to be less than 0.1V.

### BEL\_LOC\_MID\_MON thru ADC from U54 shall be measured to be less than 0.1V.

### BEL\_LOC\_ IN\_MON thru ADC from U54 shall be measured to be less than 0.1V.

### MEL\_LOC\_OUT\_MON thru ADC from U54 shall be measured to be less than 0.1V.

### MEL\_LOC\_MID\_MON thru ADC from U55 shall be measured to be less than 0.1V.

### MEL\_LOC\_ IN\_MON thru ADC from U55 shall be measured to be less than 0.1V.

### FPGA\_PWRENLP\_CTRL and FPGA\_PWRENLP\_LOC\_CTRL shall be set to logic 1.

### FPGA\_PWRENLP\_CTRL and FPGA\_PWRENLP\_LOC\_CTRL shall be read for logic 1.

### Verify LOC\_PEL\_CMD, LOC\_PEL\_ACT, PEL\_CMD, and PEL\_ACT LEDs are on. Verify BEL, MEL loop LEDs are off.

### A prompt will be displayed to the user querying whether LEDs PEL(D52, D55, D58 and D62) are ON, and MEL (D53, D56, D59 and D63), BEL (D54, D57, D60, D64), and KVBEL(D61 and D65) are OFF. A response of “Yes” is expected.

### FPGA\_BMENLP\_CTRL and FPGA\_BMENLP\_LOC\_CTRL shall be set to logic 1.

### FPGA\_BMENLP\_CTRL and FPGA\_BMENLP\_LOC\_CTRL shall be read for logic 1.

### Verify LOC\_BEL\_CMD, LOC\_BEL\_ACT, BEL\_CMD, and BEL\_ACT LEDs are on.

### A prompt will be displayed to the user querying whether LEDs D54, D57, D60, and D64 have turned ON. A response of “Yes” is expected.

### FPGA\_MTNENLP\_CTRL and FPGA\_MTNENLP\_LOC\_CTRL shall be set to logic 1.

### FPGA\_MTNENLP\_CTRL and FPGA\_MTNENLP\_LOC\_CTRL shall be read for logic 1.

### Verify LOC\_MEL\_CMD, LOC\_MEL\_ACT, MEL\_CMD, and MEL\_ACT LEDs are on.

### A prompt will be displayed to the user querying whether LEDs D53, D56, D59 and D63 have turned ON. A response of “Yes” is expected.

### FPGA\_KVBMENLP\_CTRL shall be set to logic 1.

### FPGA\_KVBMENLP\_CTRL shall be read to logic 1.

### Verify KBVEL\_CMD, and KBVEL\_ACT LEDs are on.

### A prompt will be displayed to the user querying whether LEDs D61 and D65 have turned ON. A response of “Yes” is expected.

### PEL\_OUT\_MON thru ADC from U41 shall be measured to be between 1.63V and 2.33V.

### BEL\_OUT\_MON thru ADC from U41 shall be measured to be between 1.63V and 2.33V.

### MEL\_OUT\_MON thru ADC from U41 shall be measured to be between 1.63V and 2.33V.

### KVBEL\_OUT\_MON thru ADC from U40 shall be measured to be between 1.63V and 2.33V.

### PEL\_LOC\_OUT\_MON thru ADC from U54 shall be measured to be between 1.63V and 2.33V.

### BEL\_LOC\_OUT\_MON thru ADC from U54 shall be measured to be between 1.63V and 2.33V.

### MEL\_LOC\_OUT\_MON thru ADC from U54 shall be measured to be between 1.63V and 2.33V.

### PEL\_MID\_MON thru ADC from U41 shall be measured to be between 1.63V and 2.33V.

### BEL\_MID1\_MON thru ADC from U41 shall be measured to be between 1.63V and 2.33V.

### MEL\_MID\_MON thru ADC from U40 shall be measured to be between 1.63V and 2.33V.

### KVBEL\_MID1\_MON thru ADC from U40 shall be measured to be between 1.63V and 2.33V.

### PEL\_LOC\_MID\_MON thru ADC from U54 shall be measured to be between 1.63V and 2.33V.

### BEL\_LOC\_MID1\_MON thru ADC from U54 shall be measured to be between 1.63V and 2.33V.

### MEL\_LOC\_MID\_MON thru ADC from U55 shall be measured to be between 1.63V and 2.33V.

### BEL\_MID2\_MON thru ADC from U41 shall be measured to be between 1.63V and 2.33V.

### KVBEL\_MID2\_MON thru ADC from U40 shall be measured to be between 1.63V and 2.33V.

### ATE close the CCH and DKB enable loop by proper switches/relays.

### MTNELP\_CCH\_CURRENT (AD\_IN35) thru ADC from U56 shall be measured to be between 1.63V and 2.33V.

### MTNELP\_DKB\_CURRENT (AD\_IN36) thru ADC from U56 shall be measured to be between 1.63V and 2.33V.

### Signals EMO\_GOOD\_IN shall be disconnected and PEND\_FUSE\_ON shall be turned OFF.

|  |  |
| --- | --- |
| **For the special test of Beam Enable Loop test, please refer to the separate procedure (Doc No.** | |
| **100014296-BEL Test Procedure Rev. A).** |  |

## Gantry Rotation Interface: Gantry IO and Gantry Limit Switch

DESCRIPTION

The interface has a full-duplex RS485 interface, the detailed test description is in the RS422/485 test section.

A dual common cathode diode D1 is added to the LIMITSW\_PWR\_24VOUT, so, LIMITSW\_24V will be affected by GANTRY\_BU\_24V from J5.

Gantry Limit Switch is also tested in this section. There are two switch circuits for the Gantry: clockwise and counterclockwise. Each of these circuits consists of a Schmitt trigger inverter which drives 3.3V logic to the FPGA. The inputs to the Schmitt triggers are 24V signals, voltage divided by resistors. The inputs will be tested by toggling the 24V inputs between 0 and 24V and sensing the state through the FPGA.

LEDs D7 (CCW) and D8(CW) will light to reflect the state of the input signals. The operator will be asked to verify the state of these LEDs.

PROCEDURE:

### LIMITSW\_24V between J43-3/4/7 and J42-2/6 will be measured to be between 21.0 and 24.5V.

### Apply 25VDC to GANTRY\_BU\_24V at J5-1.

### Measure LIMITSW\_24V between J43-3 and J42-2 is between 24V ~ 26V.

### Remove 25VDC from GANTRY\_BU\_24V at J5-1.

### Input voltage 0V +/-2% shall be applied to CW\_LIMIT\_24V# at J43-1.

### Input voltage 0V +/-2% shall be applied to CCW\_LIMIT\_24V# at J43-5.

### Input voltage 24V +/-2% shall be applied to GANT\_LOCK\_PIN\_OUT at J43-8.

### CCW\_LIMIT\_STAT will be measured for logic 1.

### CW\_LIMIT\_STAT will be measured for logic 1.

### GANT\_LOCK\_PIN\_STAT will be measured for logic 0.

### A prompt will be displayed to the user querying whether LEDs D7 is OFF and D8 is OFF. A response of “Yes” is expected.

### Input voltage 24V +/-2% shall be applied to CW\_LIMIT\_24V# at J43-1.

### Input voltage 24V +/-2% shall be applied to CCW\_LIMIT\_24V# at J43-5.

### Input voltage 0V +/-2% shall be applied to GANT\_LOCK\_PIN\_OUT at J43-8.

### CCW\_LIMIT\_STAT will be measured for logic 0.

### CW\_LIMIT\_STAT will be measured for logic 0.

### GANT\_LOCK\_PIN\_STAT will be measured for logic 1.

### Signal CCW\_LIMIT\_24V on J5-22 will be measured to be between 22.0V and 24.5V.

### Signal CW\_LIMIT\_24V on J5-24 will be measured between 22.0V and 24.5V.

### A prompt will be displayed to the user querying whether LEDs D7 is ON and D0 is ON. A response of “Yes” is expected.

## Gantry Rotation Interface: Encoder Interfaces

DESCRIPTION

Encoder1 has 2 transmit and 2 receive channels. They are tested in RS422/RS485 test section.

In the new design, besides encoder1 at J6, it has 3 quadrature encoders at J7, with an isolated DC/DC converter for 5VISO (U6). The 3 quadrature encoders are RS422 communication ports, the test steps are listed in RS422/RS485 test section.

The ENCODER\_FUSE\_ON# signal is driven by the FPGA to enable the TI TPS2021D power distribution switches providing 5V power to J6. To test the enable, the FPGA will toggle this signal and check ENCODER\_FUSE\_OK.

S5V\_1 is measured to detect that the switch is operating correctly. 5VISO will also be measured.

PROCEDURE

### Set ENCODER\_FUSE\_ON# to high

### Measure S5V\_1 on J6\_6, verify it’s ± 0.1V

### Set ENCODER\_FUSE\_ON# to low

### Measure S5V\_1 on J6\_6, verify it’s 5V ± 0.2V

### Measure 5VISO between J7\_4/12 and J7\_2/10, verify it’s 5V ± 0.2V

### Measure S5V\_1 on J6\_6, verify it’s 5V ± 0.2V

### Verify that the ENCODER1\_FUSE\_OK is high

### Use the high current relay to add 2 ohm resistors parallel with the 1K ohm resistors. It will trip the over current condition at U4 and U6.

### Set ENCODER\_FUSE\_ON# to high

### Close relay K0

### Set ENCODER\_FUSE\_ON# to low

### Verify that the ENCODER1\_FUSE\_OK is low

### Set ENCODER\_FUSE\_ON# to high

### Open relay K0

## Laserguard Controller Interface

DESCRIPTION

The Laserguard controller consists of 5 digital status inputs (LS\_OSSD2, LS\_WARNING, LS\_RES\_REQ, LS\_OSSD1 and LS\_ERROR), and three 24V outputs (LGCTRL1\_OUT, LGCTRL2\_OUT and LGCTRL3\_OUT). The FPGA is used to read the status of these signals..

24V power supplies are by setting the load switch (U44) to ON from FPGA to set the 24V outputs. The tester will toggle the status inputs LS\_OSSD1, LS\_ERROR, LS\_OSSD2, LS\_WARNING and LS\_RES\_REQ and the FPGA will confirm the state of those lines.

The FPGA will toggle the LGCTRL1\_OUT, LGCTRL2\_OUT, LGCTRL3\_OUT lines low and high to the tester for verification. The tester will use a 10kohm pull-down for these inputs.

Refer to schematic page 34 and page 3 for details.

PROCEDURE:

### Tester set signals J28-6 (LS\_OSSD2) low, J28-14 (LS\_WARNING) high, J28-7 (LS\_RES\_REQ) low, J28-4 (LS\_OSSD1) high, and J28-5 (LS\_ERROR) low.

### A prompt will be displayed to the user querying whether the green LED D10 is ON and D9 is OFF. A response of “Yes” is expected.

### Read the APP FPGA status bits (LS\_OSSD2#, LS\_WARNING#, LS\_RES\_REQ#, LS\_OSSD1# and LS\_ERROR# in Register) and verify them matched sets.

### Tester set signals J28-6 (LS\_OSSD2) high, J28-14 (LS\_WARNING) low, J28-7 (LS\_RES\_REQ) high, J28-4 (LS\_OSSD1) low, and J28-5 (LS\_ERROR) high.

### A prompt will be displayed to the user querying whether the green LED D10 is OFF and D9 is ON. A response of “Yes” is expected.

### Read the APP FPGA status bits (LS\_OSSD2#, LS\_WARNING#, LS\_RES\_REQ#, LS\_OSSD1# and LS\_ERROR# in Register) and verify them matched sets.

### FPGA sets signals LGCTRL1, LGCTRL2 and LGCTRL3 high.

### Measure the voltage on J28-1 (LGCTRL1\_OUT), J28-9 (LGCTRL2\_OUT) and J28-2 (LGCTRL3\_OUT) are between 22.0V and 24.5V.

### FPGA sets signals LGCTRL1, LGCTRL2 and LGCTRL3 low.

### Measure the voltage on J28-1 (LGCTRL1\_OUT), J28-9 (LGCTRL2\_OUT) and J28-2 (LGCTRL3\_OUT) are ± 0.1V.

## SF6 Gas Controller

DESCRIPTION:

The SF6 Gas controller consists of a pressure sensor and valve driver circuit. The pressure sensor consists of a voltage divider and an analog voltage follower circuit which feeds the A/D converter. The input signal is in the range 0-5V and is divided by 2 and the output is in the range 0-2.5V. The pressure sensor circuit will be tested by applying voltages of 0, 2.5V, 5V and 6V. The A/D converter will report the voltage sensed at input AD\_IN7.

The valve driver circuit consists of digital signals driven by the FPGA. U43 is a high side switch that connects 24V power supply to valve driver controlled by FPGA. The FPGA will toggle these signals and the resulting 24V state will be read by the test system.

PROCEDURE:

### Set the signals SF6\_VALVE\_OPEN, PUMP\_EN\_ON to logic 1 and SF6\_24V\_ON, PUMP\_CLR\_FLT\_ON to logic 0.

### Connect a load resistor of 1Kohm 1% across SF6\_VALVE\_COIL at J22-15 (SF6\_VLV) relative to J22-8 (SF6\_VLV\_RTN)

### Connect a load resistor of 1Kohm 1% across SF6\_24V at J22-6 (SF6\_24VOUT) relative to J22-14 (SF6\_GNDOUT)

### Connect a load resistor of 1Kohm 1% across PUMP\_EN at J12-15 (PUMP\_EN\_OUT) relative to J12-19 (GND\_PUMP\_STAND)

### Connect a load resistor of 1Kohm 1% across PUMP\_CLR\_FLT at J12-16 PUMP\_CLR\_FLT\_OUT) relative to J12-19 (GND\_PUMP\_STAND)

### A prompt will be displayed querying if LEDs D14 and ~~D36~~ D22 are ON and D15 is OFF. A response of “Yes” is expected.

### SF6\_VALVE\_COIL on J22-15 will be measured to be between 22.0V and 25.0V.

### SF6\_24V on J22-6 will be measured for ±0.3V.

### PUMP\_EN on J12-15 will be measured to be between 22.0V and 25.0V.

### PUMP\_CLR\_FLT on J12-16 will be measured for ±0.3V.

### Set the signals SF6\_VALVE\_OPEN, PUMP\_EN\_ON to logic 0 and SF6\_24V\_ON, PUMP\_CLR\_FLT\_ON to logic 1.

### A prompt will be displayed querying if LEDs D15 is ON, D14 and ~~D36~~ D22 are OFF and. A response of “Yes” is expected.

### SF6\_VALVE\_COIL on J22-15 will be measured to be between ±0.3V.

### SF6\_24V on J22-6 will be measured to be between 22.0V and 25.0V.

### PUMP\_EN on J12-15 will be measured to be between ±0.3V.

### PUMP\_CLR\_FLT on J12-16 will be measured to be between 22.0V and 25.0V.

### Set all signals SF6\_VALVE\_OPEN, PUMP\_EN\_ON, SF6\_24V\_ON and PUMP\_CLR\_FLT\_ON to logic 0.

### A voltage of 0V +20mV will be applied to signal SF6\_WG\_PRESS at J22-7

### The voltage of SF6\_WG\_PRESSURE at AD\_IN7 will be read for 0V +/-100mV

### A voltage of 1.0V +/-2% will be applied to signal SF6\_WG\_PRESS at J22-7

### The voltage of SF6\_WG\_PRESSURE at AD\_IN7 will be read for (0.45V, 0.51V)

### A voltage of 2.0V +/-2% will be applied to signal SF6\_WG\_PRESS at J22-7

### The voltage of SF6\_WG\_PRESSURE at AD\_IN7 will be read for (0.9V, 1.02V)

### A voltage of 3.0V +/-2% will be applied to signal SF6\_WG\_PRESS at J22-7

### The voltage of SF6\_WG\_PRESSURE at AD\_IN7 will be read for (1.35V, 1.53V)

### A voltage of 4.0V +/-2% will be applied to signal SF6\_WG\_PRESS at J22-7

### The voltage of SF6\_WG\_PRESSURE at AD\_IN7 will be read for (1.8V, 2.04V)

## System Power IF: Stand Power Interface

DESCRIPTION

Status from the Stand Power Distribution Board is relayed to the Stand Controller through opto-coupled 24V digital inputs. These signals will be toggled by the test system and the FPGA will be used to report their state for verification.

PROCEDURE:

### Signal CSPARESW1\_C at J13-16 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal CSPARESW2\_C at J13-17 shall be set to 24V with respect to SPD\_RTN at J13-24

### Signal DC\_MAIN\_DOOR\_SW\_C at J13-14 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal NEUTRON\_DR\_SW1\_C at J13-11 shall be set to 24V with respect to SPD\_RTN at J13-24

### Signal NEUTRON\_DR\_SW2\_C at J13-12 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal CDOS\_STS\_C at J13-25 shall be set to 24V with respect to SPD\_RTN at J13-24

### Signal CMNR\_STS\_C at J13-13 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal GROTPWR\_STS\_C at J13-23 shall be set to 24V with respect to SPD\_RTN at J13-24

### Signal SPD\_AC\_DR\_C at J13-20 shall be set to 0V with respect to SPD\_RTN at J13-24

### A prompt will be displayed to the user querying whether LED ~~D90~~ D71 is ON. A response of “yes” is expected.

### Read APP FPGA register bits and verify them matched with sets.

### GROTPWR\_STS\_IN shall be read for logic 0.

### Signal CSPARESW1\_C at J13-16 shall be set to 24V with respect to SPD\_RTN at J13-24

### Signal CSPARESW2\_C at J13-17 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal DC\_MAIN\_DOOR\_SW\_C at J13-14 shall be set to 24V with respect to SPD\_RTN at J13-24.

### Signal NEUTRON\_DR\_SW1\_C at J13-11 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal NEUTRON\_DR\_SW2\_C at J13-12 shall be set to 24V with respect to SPD\_RTN at J13-24

### Signal CDOS\_STS\_C at J13-25 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal CMNR\_STS\_C at J13-13 shall be set to 24V with respect to SPD\_RTN at J13-24

### Signal GROTPWR\_STS\_C at J13-23 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal SPD\_AC\_DR\_C at J13-20 shall be set to 24V with respect to SPD\_RTN at J13-24

### A prompt will be displayed to the user querying whether LED D71 is OFF. A response of “yes” is expected.

### Read APP FPGA register bits and verify them matched with sets.

### GROTPWR\_STS\_IN shall be read for logic 1.

### Signal CSPARESW1\_C at J13-16 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal CSPARESW2\_C at J13-17 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal DC\_MAIN\_DOOR\_SW\_C at J13-14 shall be set to 0V with respect to SPD\_RTN at J13-24.

### Signal NEUTRON\_DR\_SW1\_C at J13-11 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal NEUTRON\_DR\_SW2\_C at J13-12 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal CDOS\_STS\_C at J13-25 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal CMNR\_STS\_C at J13-13 shall be set to 0V with respect to SPD\_RTN at J13-24

### Signal GROTPWR\_STS\_C at J13-23 shall be set to 0V with respect to SPD\_RTN at J13-24.

### Signal SPD\_AC\_DR\_C at J13-20 shall be set to 0V with respect to SPD\_RTN at J13-24.

## System Power Interface

DESCRIPTION

The System Power Interface provides an interface to the Stand Power Distribution Board. The Gantry Rotation Power Control driver is a switch, enabled by the FPGA through the signal HDW\_GANT\_ROT\_EN. The test system will measure the output 24V supply HW\_GANT\_ROT\_EN\_C at J13-1 when enabled and the FPGA will verify the switch status output HW\_GANT\_ROT\_EN\_FLT# to correspond with the controlled state. According to datasheet of BSP742R, protection function is not designed for continuous and repetitive operation. The short current protection will not be tested here.

LED D79 will light to reflect the state of the Gantry Rotation Switch. The operator will be asked to verify the state of this LED.

PROCEDURE

### Signals BMENLP\_CNTL, HDW\_GANT\_ROT\_EN, KVBMENLP\_CNTL, MTNENLP\_CNTL, PWRENLP\_CNTL, BMENLP\_LOC\_CNTL, PWRENLP\_LOC\_CNTL, MTNENLP\_LOC\_CNTL shall be set to 0.

### Status of MEL\_SW\_CONFIG\_ADDR shall be read by HDW FPGA, a prompt will be displayed to the user to configure all switches on SW1 to OFF position if has not.

### Status of BEL\_SW\_CONFIG\_ADDR shall be read by HDW FPGA, a prompt will be displayed to the user to configure all switches on SW2 to OFF position if has not.

### Status of KVBEL\_SW\_CONFIG\_ADDR shall be read by HDW FPGA, a prompt will be displayed to the user to configure all switches on SW4 to OFF position if has not.

### Input voltage of 24V shall be applied to signal PENDANT\_MEB\_24V.

### Signal PEND\_FUSE\_ON shall be set to logic 1.

### Input voltage of 24V shall be applied to signals LS\_OSSD1 and LS\_ERROR.

### HDW\_GANT\_ROT\_EN shall be read to logic 0.

### A prompt will be displayed to the user querying whether LED D79 is OFF. A response of “yes” is expected.

### HW\_GANT\_ROT\_EN\_C on J13-1 is measured for ±0.5V.

### Input voltage of 24V shall be applied to signal EMO\_GOOD\_IN at J13-18 to set EMO\_GOOD to logic 1.

### Input voltage of 24V shall be applied to signal PENDANT\_MEB \_24V at J25-6 to set PEND\_MEB# to logic 0.

### Connect e-load or 50 Ω 1W resistor to J6-6 S5V\_1, set DUT register CONN\_OUTPUTS bit ENCDER\_FUSE\_ON to logic 1.

### DUT register INTERNAL\_STAT bit PENDANT\_INST, shall be read to logic 1.

### HDW\_GANT\_ROT\_EN shall be set to logic 1.

### A prompt will be displayed to the user querying whether LED D79 is ON. A response of “yes” is expected.

### HW\_GANT\_ROT\_EN\_C on J13-1 shall be measured to be between 22.0V and 25.0V.

### HW\_GANT\_ROT\_EN\_FLT# shall be read for logic 1.

### HDW\_GANT\_ROT\_EN shall be set to logic 0.

### All the signals where 24V was applied (LS\_OSSD1, LS\_ERROR, EMO\_GOOD\_IN, PENDANT\_MEB\_24V) and load on J6-6 S5V\_1 shall be removed.

## Water Interface: Flow Sensors Test

DESCRIPTION

The flow sensor inputs are also 3.3V referenced Schmitt trigger inverters to the FPGA. The 24V input voltages are voltage divided to reduce their level before input to the Schmitt triggers. To test the flow sensors, the test system will generate voltages causing the Schmitt triggers to toggle and the FPGA will detect the change of state. Similarly, the PUMP\_FAULT signal will have 12V applied at its input and a Schmitt trigger inverter relays the data to the FPGA.

To test, each sensor, FLOW# [1:5] and PUMP\_FAULT, will be toggled and the resulting state detected by the FPGA.

PROCEDURE:

### Input voltage of 24V shall be applied to FLOW1\_24V at J12-3.

### Input voltage of 0V shall be applied to FLOW2\_24V at J12-23

### Input voltage of 24V shall be applied to FLOW3\_24V at J22-9.

### Input voltage of 0V shall be applied to FLOW4\_24V at J22-3.

### Input voltage of 24V shall be applied to FLOW5\_24V at J22-12.

### Input voltage of 0V shall be applied to PUMP\_FLT\_IN at J12-14.

### A prompt will be displayed to the user querying whether the LEDs D25, D27, and D38 are ON and D24, D26, and D37 are OFF. A response of “Yes” is expected.

### Signal FLOW [5:1] shall be read for a value of 0xA.

### Signal PUMP\_FAULT shall be read for logic 1.

### Input voltage of 0V shall be applied to FLOW1\_24V at J12-3.

### Input voltage of 24V shall be applied to FLOW2\_24V at J12-23

### Input voltage of 0V shall be applied to FLOW3\_24V at J22-9.

### Input voltage of 24V shall be applied to FLOW4\_24V at J22-3.

### Input voltage of 0V shall be applied to FLOW5\_24V at J22-12.

### Input voltage of 12V shall be applied to PUMP\_FLT\_IN at J12-14.

### A prompt will be displayed to the user querying whether the LEDs D24, D26, and D37 are ON and D25, D27, and D38 are OFF. A response of “Yes” is expected.

### Signal FLOW [5:1] shall be read for a value of 0x15.

### Signal PUMP\_FAULT shall be read for logic 1.

### FLOW2\_24V at J12-23 shall be disconnected.

### FLOW4\_24V at J22-3 shall be disconnected.

### PUMP\_FLT\_IN at J12-14 shall be disconnected.

## Water Interface: Water IF Tests

DESCRIPTION

**Water IF:**

The Water Valve Position and Water Pump Speed signals are controlled by the Stand Controller DAC, U3. The DAC is controlled by the FPGA through a Serial Peripheral Interface (SPI) bus. To test the interface, the FPGA will use the SPI bus to generate output voltages of varying voltages between 0V and +2.5V. to generate 20.91mA current by Voltage to Current converter circuits through op-amps ensures a current through the load that is independent of the load and dependent only on the variation of the input voltages from the DAC, WATER\_VALVE\_CMD and WATER\_PUMP\_CMD. 100ohm and 250 ohms load resistors in the tester will be connected across VALVE\_CONTROL+ and VALVE\_CONTROL- and across PUMP\_SPEED+ and PUMP\_SPEED-. The resulting voltages will be read by the test system to measure the output value of the DAC on both the Valve and Pump control circuits.

The Water Valve Feedback circuit is a voltage follower which feeds the AD\_IN37 input of the A/D converter. The tester will generate voltages between 2V and 10V and the A/D converter will read and verify the voltage generated by the tester.

**Water Level Sensors:**

Three water level sensors, low warning, low error, high error, are sensed by the FPGA through Schmitt trigger inverters. The input voltages to the Schmitt triggers are voltage divided to reduce their magnitude. To test the level sensors, the test system will generate voltages causing the Schmitt triggers to toggle and the FPGA will detect the change of state.

Each sensor generates inputs to toggle LEDs. LEDs D11, D13 and D12 will light to reflect the state of the input signals. The operator will be asked to verify the state of these LEDs.

**Water Temperature Sensors:**

There are 4 temperature sensor circuits on the Stand Controller. They work by detecting the variation of voltage resulting from the changes in resistance on RTDs (resistor temperature devices). The voltages are amplified through comparator op-amps (U36, U37, U38) and read by the Stand Controller A/D via channels AD\_IN8, AD\_IN9 and AD\_IN10. At 0 degrees C, the input voltage will result in an output voltage read by the A/D converter as 0V. The RTD resistance is 1kohm at this temperature and the nominal input voltage is 1.25V, a result of a voltage divider between the RTD and 1kohm resistors R511, R512 and R513. To test the sensor interface, 1.2KΩ resistors will be connected to the H2OxRTD and H2OxRTD\_RTN. Read and verified by the A/D converter of the Stand Controller.

|  |  |  |  |
| --- | --- | --- | --- |
| Vrtd (V) | Amplifier Out (V) | Equivalent  Temp  (degC) | Equivalent RTD  Resistance (ohms) |
| 1.25 | 0 | 0 | 1000 |
| 1.273584 | 0.44 | 10 | 1038 |
| 1.296364 | 0.865 | 20 | 1077 |
| 1.3182328 | 1.273 | 30 | 1115 |
| 1.3393512 | 1.667 | 40 | 1154 |
| 1.3597728 | 2.048 | 50 | 1192 |
| 1.379444 | 2.415 | 60 | 1231 |

Added 2.5V\_VREF\_BUF and 1.25V\_VREF\_BUF to ADC as AD\_IN26 and AD\_IN40.

PROCEDURE:

**Water IF:**

### With DAC voltage set to 0V through the SPI bus, an output voltage at VALVE\_CONTROL J12-10 shall be measured for 0V +/-100mV.

### With DAC voltage set to 0.5V through the SPI bus, an output voltage at VALVE\_CONTROL J12-10 shall be measured for (0.313V, 0.513V)

### With DAC voltage set to 1.0V through the SPI bus, an output voltage at VALVE\_CONTROL J12-10 shall be measured for (0.726V, 0.926V)

### With DAC voltage set to 1.5V through the SPI bus, an output voltage at VALVE\_CONTROL J12-10 shall be measured for (1.14V, 1.34V)

### With DAC voltage set to 2.0V through the SPI bus, an output voltage at VALVE\_CONTROL J12-10 shall be measured for (1.553V, 1.753V)

### With DAC voltage set to 2.5V through the SPI bus, an output voltage at VALVE\_CONTROL J12-10 shall be measured for (1.966V, 2.166V)

### With DAC voltage set to 0V through the SPI bus, an output voltage at PUMP\_SPEED J12-12 shall be measured for 0V +/-100mV.

### With DAC voltage set to 0.5V through the SPI bus, an output voltage at PUMP\_SPEED J12-12 shall be measured for (0.933V, 1.133V)

### With DAC voltage set to 1.0V through the SPI bus, an output voltage at PUMP\_SPEED J12-12 shall be measured for (1.966V, 2.166V)

### With DAC voltage set to 1.5V through the SPI bus, an output voltage at PUMP\_SPEED J12-12 shall be measured for (2.999V, 3.199V)

### With DAC voltage set to 2.0V through the SPI bus, an output voltage at PUMP\_SPEED J12-12 shall be measured for (4.032V, 4.232V)

### With DAC voltage set to 2.5V through the SPI bus, an output voltage at PUMP\_SPEED J12-12 shall be measured for (5.065V, 5.265V)

### With DAC voltage at J12-20 (WATER\_VALVE\_FB) set to 2.0V, WATER\_VALVE\_POS shall be read for (0.375V, 0.414V) through A/D converter channel AD\_IN37.

### With DAC voltage at J12-20 (WATER\_VALVE\_FB) set to 10.0V, WATER\_VALVE\_POS shall be read for (1.873V, 2.072V) through A/D converter channel AD\_IN37.

**Water Level Sensors:**

### An Input voltage of 24V shall be applied to WATER\_LOW\_WARN\_SW at J12-25.

### An Input voltage of 0V shall be applied to WATER\_LOW\_ERR\_SW at J12-24.

### An Input voltage of 24V shall be applied to WATER\_HIGH\_ERR\_SW at J12-26.

### A prompt will be displayed to the user querying whether the LED D12 is ON and D11 and D13 is OFF. A response of “Yes” is expected.

### Signal WATER\_LOW\_WARNING shall be read for logic 0.

### Signal WATER\_LOW\_ERROR shall be read for logic 1.

### Signal WATER\_HIGH\_ERROR shall be read for logic 0.

### An Input voltage of 0V shall be applied to WATER\_LOW\_WARN\_SW at J12-25.

### An Input voltage of 24V shall be applied to WATER\_LOW\_ERR\_SW at J12-24.

### An Input voltage of 0V shall be applied to WATER\_HIGH\_ERR\_SW at J12-26.

### A prompt will be displayed to the user querying whether the LED D11 and D13 are ON and D12 is OFF. A response of “Yes” is expected.

### Signal WATER\_LOW\_WARNING shall be read for logic 1.

### Signal WATER\_LOW\_ERROR shall be read for logic 0.

### Signal WATER\_HIGH\_ERROR shall be read for logic 1.

### An Input voltage of 0V shall be applied to WATER\_LOW\_ERR\_SW at J12-24.

**Water Temperature Sensors:**

### Read 2.5V\_REF\_BUF at AD\_IN26 and verify it’s 1.25V ±0.1V

### Read 1.25V\_REF\_BUF at AD\_IN40 and verify it’s 1.25V ±0.1V

### H2O\_TEMP1 shall be measured to be between 0.958V and 1.164V through the A/D converter at channel AD\_IN8.

### H2O\_TEMP2 shall be measured to be between 0.958V and 1.164V through the A/D converter at channel AD\_IN9.

### H2O\_TEMP3 shall be measured to be between 0.958V and 1.164V through the A/D converter at channel AD\_IN10.

## Network Interface: SP485

The Stand Controller includes several RS422/RS485 interfaces. RS485 is half-duplex, and RS422 is point-to-point in one direction only.

To test, RS422 outputs can be looped-back to RS422 inputs, and RS485 outputs can be connected to each other. Connections are as shown in Table 1. Directions are shown as input, output, or bidirectional.

Table : RS422/485 Loopback

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | BMPLS | DMD\_MSSB\_RX | ENC\_A | ENC\_B | ENC\_I | ENCODER\_D2 |
|  |  | I | I | I | I | I | B |
| SYNC\_LOC | O | X |  |  | X |  |  |
| SYNC | O |  |  | X |  | X |  |
| DMD\_MSSB\_TX | O |  | X |  |  |  |  |
| ENCODER\_D1 | B |  |  |  |  |  | X |

SYNC\_LOC\_A/B(U149) in Local Network IF and SYNC\_A/B (U158) in the Network IF are RS485 transceiver with Tx and Rx ports enabled; and BMPLS\_A/B (U157) in the Network IF RS485 transceiver with Rx port only; ENCODER\_D1\_A/B (U23) and ENCODER\_D2\_A/B (U24) in the ENDAT Encoder IF are RS485 transceiver with Tx and Rx ports controlled by enable signals; and ENC\_A\_P/N, ENCB\_P/N and ENC\_I\_P/N (U5) in the Quadrature Encoder IF are RS422 line receiver with Rx ports only. DMD\_MSSB\_TX+/- and DMD\_MSSB\_RX+/- in the DMD communication IF are RS485 transceivers with Tx and Rx port enabled. A loop back configure ration is shown Figure 1.

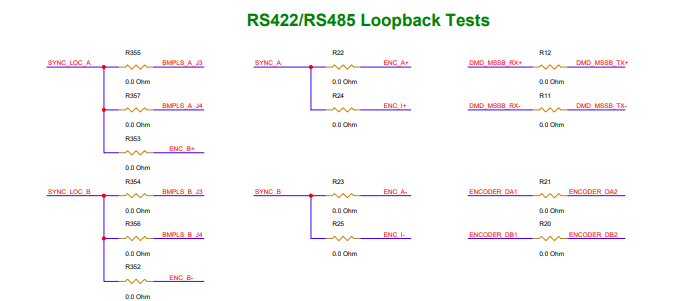


Figure . RS422/RS485 Loopback Tests

PROCEDURE:

### Configure the RS422/RS485 loopback tests as shown in Figure 1.

### ATE enables the RS422/RS485 test case from APP\_FPGA special build test firmware via SPI interface.

### ATE check the RS422/RS485 test results via SPI interface for every 10 seconds, the test results shall be set to 1.

### Repeat test for 10 times, ATE shall report no errors.

## Network IF: Pendant IF Test

DESCRIPTION

The Pendant Interface at J25 consists of a CAN bus driver (U) and controller, a +24V output with hot-swap controller and overload protection (U86), a current monitor circuit (U89 and U88) sensed through R252, and a Pendant motion enable control input. The current monitor output, PENDANT\_INST, will be logic 0 when the 24V output current is greater than 41mA, and it is set to logic 1 when the current is less than 41mA.

The Pendant interface source is provided through a 24V supply controlled by a hot swap controller U86. The controller will be tested for control and status by enabling and disabling the controller via the FPGA and checking the output Pendant interface supply voltage and hot swap controller status signal.

A motion enable input is part of the Pendant interface. It is a 24V digital input which is voltage divided and fed into a Schmitt trigger input. The FPGA is used to detect the state of the input.

The CAN interface is tested via the other tests related to the CAN bus.

PROCEDURE:

### Input voltage of 24V shall be applied to PENDANT\_MEB\_24V through a relay.

### A prompt will be displayed to the user querying whether LED D47 is ON.

### PEND\_MEB# shall be read for logic 0.

### Disconnect the PENDANT\_MEB\_24V relay.

### A prompt will be displayed to the user querying whether LED D47 is OFF.

### PEND\_MEB# shall be read for logic 1.

### PEND\_FUSE\_ON shall be set to logic 1.

### The PENDANT\_INST will be read for logic 1.

### A prompt will be displayed to the user querying whether the green LED D36 is ON. A response of “Yes” is expected.

### PEND\_FUSE\_ON shall be set to logic 0.

### PENDANT\_INST shall be read for logic 0.

### Measure PEND\_ID at J25\_1, verify the resistance to ground is 10KΩ ±10%.

## Network Interface: CAN Bus

DESCRIPTION:

There are four CAN bus interfaces on the Stand Controller that are IPs integrated into FPGAs. Each controller interfaces through standard ISO 11898-2 CAN PHY transceivers, U159, U164, U150 and U139 respectively. The Subsystem Network interface is via connectors J3 and J4. The DKB Network interface is via J9; The Local Network interface is via J29 and J30; and the Pendant CAN Network is accessed via modular connector J25.

These CAN bus interfaces will be tested by connecting the Subsystem CAN differential pair to the Local Network CAN differential pair, and connecting the DKB Network differential pair to the Pendant Network differential pair as shown in Figure 2.



Figure . CAN Bus Test

For the first CAN bus test, the Subsystem CAN will control the bus first and transmit the test messages to others. The test data will then be read from the receive FIFO, and the bytes will be verified to match the test data transmitted by the Subsystem CAN controller. This will be repeated with the Local Network CAN controller as the transmitter, the DKB CAN controller as transmitter and Pendant Network CAN as transmitter, the others receive data and the data will be verified to match the test messages.

J9 – CAN2, J3/4 – CAN1, J29/30 – CAN3, J25 – CAN4

1. Each CAN controller has an unique ID
2. CAN2 sends test pattern (1 frame, 8 bytes) to CAN1
3. CAN1 receives and resend test pattern to CAN3
4. CAN3 receives and resend test pattern to CAN4
5. CAN4 receives and resend test pattern to CAN3
6. CAN2 receives data and verify it matches with test pattern

PROCEDURE:

### Configure the CAN Bus loopback tests as shown in Figure 2.

### ATE enables the CAN Bus test case from APP\_FPGA special build test firmware via SPI interface.

### ATE check the CAN Bus test results via SPI interface for every 10 seconds, the test results shall be set to 1, repeat reading test results for 10 times.

## Ethernet test

DESCRIPTION:

Loop back test needs to be conducted for testing DUT ethernet functionality. The test fixture which provides loop back connection should be connected to DUT RJ45 connector J20.

J20-1 is connected to J20-3, J20-2 is connected to J20-6, J20-4 is connected to J20-7, J20-5 is connected to J20-8.

PROCEDURE:

### A CAT5e cable is connected from DUT to Test PCBA

### The FPGA sets up the PHY appropriately using the MDIO interface (100Mbps, Auto negotiation, Auto-MDIX).

### The FPGA transmits data to the PHY.

### The FPGA monitors data from the PHY and evaluates (e.g. good packet counters increasing, bad packet counters steady).

### The results of the test are displayed and recorded.

## FPGA Erase

The APP FPGA on the UUT shall be manually erased after completion of automated functional test.

PROCEDURE:

### APP FPGA Test firmware is erased using FPGA programming pod Actel FlashPro 4. The FPGA shall be verified to be blank.

## Shut Down

### Ensure that power is removed from the UUT.

### Reset all instruments on the ATE.

### Remove all fixture connectors from the UUT.

### Remove the UUT from the test fixture.

### Functional Test is Complete.

Summary of changes to design P1060967:

* This board is a respin and, due to number of changes REFDES were renumbered. Most REFDES have changed (except most connectors have stayed the same).
* Connectors that have physically changed are: J39 (removed), J40 was renamed to J5. J8 is renamed J43 and uses a new connector.
* There is no longer a mezzanine board feature. All former mezzanine board functions have been incorporated into the main-board (Ethernet PHY and RJ45 connector, controlling logic moved to hardwired FPGA). This also affects EEPROM access and FPGA programming.
* The 2 FPGAs have changed from ProASIC3 to PolarFire. All hardwired FPGA programming will be from JTAG connector. The application FPGA can be either from the JTAG connector, or from the hardwired FPGA.
* The DC/DC power tree has changed, including new power supplies for the new FPGAs. There is no -5VA anymore (entire design is now unipolar).
* ADC (ADS8864IDRCR) has changed, and scaling will change as input range of ADC is 0-5V but only 0-2.5V is used (i.e. ADC converted values will be half of former values).
* DAC (DAC60504BRTER) has changed. It is also now unipolar. Scaling will change. Also, DAC output 0 is no longer used.
* 24V multi-channel high side drivers (TPS4H000AQPWPRQ1) are different.
* CANbus controllers are no longer separate ICs. Design uses IP in the FPGA which emulates former SJA1000 controller ICs.
* J3/J4 have less features supported (all "spare" connections are removed).
* J28 has 3 new controlled 24V high-side outputs
* J40 has been renamed J5. The interface has changed (simplified). It now includes a full duplex RS422 link and has less signals.
* J7 has changed. It includes a fully isolated interface, including isolated RS422 inputs and an isolated 5V power output.
* Pendant switch (formerly SW3) is removed.