SET - 1

VAAGDEVI ENGINEERING COLLEGE

P.O.BOLLIKUNTA, KHILA WARANGAL (M) WARANGAL - 506 005 (AUTONOMOUS)

II YEAR B.TECH I SEM R23 REG. I - MID TERM EXAMINATIONS SEP - 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

Computer Science and Engineering(AI&ML)

Time:10.00 AM - 12.00 noon Max.Marks:30

Date: 21.09.2024

Session: F N Dort A & R

| Session: x 1 | Note: This question Paper Contains two parts. Part A & B |
|--|--|
| Cos | Course Outcomes for Assessment in this Test: |
| The state of the s | Understand the basics of instructions sets and their impact on processor design. |
| | Demonstrate an understanding of the design of the functional units of a digital computer system |
| 3 | Evaluate cost performance and design trade-offs in designing and constructing a computer processor including memory. |
| 4 | Design a pipeline for consistent execution of instructions with minimum hazards |

| | I MINI TE | $\mathbf{X} \ 1 = 1$ | 0 Mar | ks) |
|--------|--|----------------------|-------|-----|
| 0 N | CHOOSE THE CORRECT ANSWER Questions | Marks | СО | BL |
| Q. No. | A microprogram sequencer (a) Generates the address of next micro instruction to be executed. (b) Generates the control signals to execute a microinstruction. (c) Sequentially averages all microinstructions in the control memory. (d) Enables the efficient handling of a micro program subroutine. | 1 | 1 | 1 |
| 2 | In STACK structure both addition and removal are called as () (a) PUSH and POP (b) POP and PUSH c) PUSH and PUSH (d) POP and POP | 1 | 1 | 2 |
| 3 | The control unit controls other units by generating ((a) Control signals (b) Timing signals (c) Transfer signals (d) Both A&B | 1 | 1 | 4 |
| 4 | 8bit registers includes () (a) AR,PC (b)INPR,OUTR (c)AC,IR (d)A& C | 1 | 2 | 1 |
| 5 6 | The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called () (a) Data transfer instructions. (b) Program control instructions. (c) Input-output instructions. (d) Logical instructions. | 1 | 2 | 1 |
| | FILL IN THE BLANKS | | | |
| 6 | holds the address of the location to be accessed | 1 | 2 | 1 |
| | ogram counter consists of bits | | 1 | 1 |
| 8 | Y=(p+q)*(r+s) is example of instruction | 1 | 1 | 1 |
| | Description for instruction CLA is | 1 | 2 | 1 |
| 0 | A control word is represented with and | 1 | 1 | |

| | PART – B | $(4 \times 5 = 2$ | 20 Marl | ks) |
|--------|---|-------------------|---------|-----|
| | ANSWER ANY FOUR OF THE FOLLOWIN | G | | |
| Q. No. | Questions | Marks | co | BL |
| 1 | Design a 4 bit binary Adder and Subtractor for A=1010 and B=0100 | 5 | 2 | 3 |
| 2 | Explain instruction formats for arithmetic micro operation of $Y = (A+B) \cdot (C+D)$ in detail | 5 | 2 | 3 |
| 3 | Explain data transfer and data manipulation instruction with | 5 | 1 | 2 |
| 4 | With a neat sketch explain the block diagram of a Digital Computer | 5 | 1 | 2 |
| 5 | Identify the function of a address sequencer in mixed programmed control unit and explain | 5 | 2 | 2 |
| 6 | Explain general register organization | 5 | 1 | 2 |

| | Assessment | Summary : | | | 28 | | | - |
|---|------------|-----------|------------|-------|---------|----------|--------|-------|
| | Cos | Remember | Understand | Apply | Analyze | Evaluate | Ĉreate | Total |
| Γ | | , | 20 | 10 | | | | 30 |