# CprE 381, Computer Organization and Assembly Level Programming

# Team Contract – Project Part 2

Project Teams Group #: _Section 7 Group 1_

Team Members: ____Ian Johnson_____

___Yohan Bopearatchy_____

___Bailey Gorlewski_____

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*Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.*

**Course Goals:** *List and acknowledge the goals of your individual team members.*

- *learn everything about computer architecture*
- *get an A*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *be able to explain the workings of a stored-program computer from gates to C*

**Team Expectations:**

- **Conduct:**
  - *Keep up the pace of work*
  - *Be respectful and inclusive*
- **Communication:**
  - *Text communication*
  - *Expect a response within the hour*
  - *At least twice a week meeting*
- **Group conventions:**
  - *Testbench: tb_*
  - *Naming convention: "name abv"_design&number (mux_2t1)*
  - *do files not necessary*

    - *gitlab*
    - *comments: Short description of file, name of creator, when created, last updated, last person to update*

- **Meetings:**
    - *Wednesdays*
    - *discord if needed*
    - *Work separately on responsibilities, yes*
- **Peer Evaluation Criteria:**
    - *Work on your own time as much as possible*
    - *Complete responsibilities on time/Don't fall behind*

**Role Responsibilities:** *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

| **Lab Part** | | **Estimated Time** | **Design** | | **Test** | |
|---|---|---|---|---|---|---|
| | | | **Lead** | **Deadline** | **Lead** | **Deadline** |
| Software-Scheduled Pipeline | Control Signals | 0.5 hr | Ian | 11/15 | Yohan | 11/18 |
| | Datapath | 3 hr | Yohan | 11/22 | Ian | 11/29 |
| | Testing | 3 hr | Bailey | 11/22 | Ian | 11/29 |
| | Synthesis (human effort) | 0.5 hr | Bailey | 11/29 | Yohan | 11/29 |
| Hardware-Scheduled Pipeline | Pipeline Register Update | 1 hr | Bailey | 11/18 | Ian | 11/21 |
| | Data Hazard Avoidance | 4 hr | Ian | 11/22 | Bailey | 11/29 |
| | Control Hazard Avoidance | 2-6 hr based on group size | Ian | 11/29 | Bailey | 12/2 |
| | Integration (Hardware-Schedule Pipeline) | 3 hr | Yohan | 12/2 | Ian | 12/6 |
| | Testing | 3 hr | Yohan | 12/6 | Bailey | 12/6 |
| | Synthesis | 0.5 hr | Bailey | 12/6 | Yohan | 12/6 |

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Please note that to be done properly, the test programs will require significant time investment, but will result in a much stronger final design.*

**Integrity of Work:** *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code

ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

**Student Signature** ___Ian Johnson_____ **Date** ___11/11/2021___

**Student Signature** ____Yohan Bopearatchy_____ **Date** __11/11/2021____

**Student Signature** ____Bailey Gorlewski_____ **Date** _____11/11/2021_____

**Student Signature** _____ **Date** _____

**Student Signature** _____ **Date** _____

**Student Signature** _____ **Date** _____