lab1mem Project Status (01/21/2018 - 14:36:00)			
Project File:	Lab1.xise	**Parser Errors:**	No Errors
Module Name:	TopLevel	**Implementation State:**	Synthesized
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.6	• **Warnings:**	3 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	55	18224	0%
Number of Slice LUTs	107	9112	1%
Number of fully used LUT-FF pairs	39	123	31%
Number of bonded IOBs	12	232	5%
Number of Block RAM/FIFO	1	32	3%
Number of BUFG/BUFGCTRLs	1	16	6%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun Jan 21 14:35:53 2018	0	3 Warnings (0 new)	13 Infos (0 new)
Translation Report	Out of Date	Sun Jan 21 14:28:15 2018	0	0	0
Map Report	Out of Date	Sun Jan 21 14:28:31 2018	0	1 Warning (0 new)	6 Infos (0 new)
Place and Route Report	Out of Date	Sun Jan 21 14:29:02 2018	0	0	3 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Out of Date	Sun Jan 21 14:29:09 2018	0	0	4 Infos (0 new)
Bitgen Report	Out of Date	Sun Jan 21 14:29:24 2018	0	1 Warning (0 new)	1 Info (0 new)

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Sun Jan 21 14:32:52 2018	
WebTalk Report	Out of Date	Sun Jan 21 14:29:25 2018	
WebTalk Log File	Out of Date	Sun Jan 21 14:29:28 2018	

Date Generated: 01/21/2018 - 14:36:01