

# VLSI Mini-Project 3

## Folded-Cascode Differential Amplifier

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### 1 Circuit Analysis

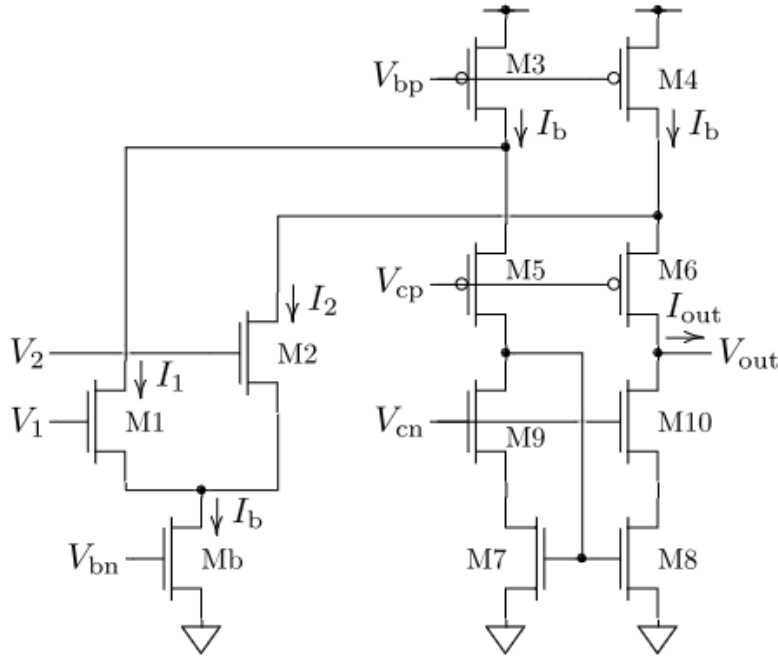


Figure 1: Folded-cascode differential amplifier from MP3 handout.

#### 1. Circuit Analysis

- (a) The circuit makes use of the diff pair  $M_1$ ,  $M_2$  to draw a variable amount of current out of the drains of  $M_3$  and  $M_4$ . When  $I_1 \neq I_2$ , then the currents in the lower branches  $M_5$  through  $M_{10}$  become unequal. Because the pull-down transistors  $M_7$  through  $M_{10}$  are in a current mirror configuration driven by the left hand side, the currents can only be solved for if  $V_{out}$  slams to less than  $2V_{DS,sat}$  away from the rails to put  $M_6$  and  $M_4$  or  $M_{10}$  and  $M_8$  into the ohmic region.

$V_1$  is the non-inverting input, because when  $I_1 > I_2$ , then the pull-down transistors on the left draw less current, which is mirrored to the pull-down transistors on the right, and so  $M_6$  is passing more current than  $M_{10}$  and  $M_8$  are able to, and  $V_{out}$  rises to put  $M_6$  and  $M_4$  into the ohmic region.

$V_2$  is the inverting input, because when  $I_1 < I_2$ , then the pull-down transistors on the left draw more current, which is mirrored to the pull-down transistors on the right, and  $M_6$  cannot pass as much current as  $M_{10}$  and  $M_8$  are trying to, and so  $V_{out}$  falls to put  $M_{10}$  and  $M_8$  into the ohmic region.

- (b)  $M_1$  or  $M_2$  must be capable of passing at least  $I_b$ . For this, one of their gate voltages  $V_1$  and  $V_2$  must be at least  $V_{bn}$  higher than the common-source voltage  $V_{node}$ , such that  $V_{GS}$  for  $M_1$  or  $M_2$  is around  $V_{GS}$  for  $M_b$ . For the circuit to work correctly,  $M_b$  must be in saturation, so  $V_{node} \geq V_{DS,sat}$ . Therefore, we have that  $V_{CM} \geq V_{bn} + V_{DS,sat}$ .
- $M_3$  and  $M_4$  should also be capable of passing  $I_b$ , which means they should remain in saturation. This provides an upper bound in the form of  $V_{node} \leq V_{DD} - V_{DS,sat}$ . We already established that  $V_1$  or  $V_2$  is  $V_{bn}$  higher than  $V_{node}$ , so  $V_{CM} - V_{bn} \leq V_{DD} - V_{DS,sat}$ , or  $V_{CM} \leq V_{DD} - V_{DS,sat} + V_{bn}$ . Since  $V_{bn} > V_{DS,sat}$ , the upper limit of  $V_{CM}$  is only given by  $V_{DD}$ . Therefore, we have  $V_{bn} + V_{DS,sat} \leq V_{CM} \leq V_{DD}$ .
- (c) Let the current through  $M_3$  and  $M_4$  be  $I_b$  based on the bias voltage  $V_{bp}$ , where  $I_b \geq I_1, I_2$ . The current through  $M_7, M_9$  is  $I_b - I_1$ , and it is mirrored over to  $M_8, M_{10}$  if all transistors are in saturation. The current through  $M_6$  is  $I_b - I_2$ . By Kirchoff's Current Law, the current into the output node is  $I_b - I_2 - (I_b - I_1) = I_1 - I_2$ .
- (d) The current through  $M_3$  and  $M_4$  must be at least  $I_b$ , because when  $V_1 \neq V_2$ , then either  $I_1 = I_b$  or  $I_2 = I_b$ . If  $M_3$  or  $M_4$  could not source this current, then  $M_1$  or  $M_2$  would have to fall out of saturation, and the behavior of the circuit would be compromised. You might be able to make an argument that in this case, one of the currents is still larger than the other, and the imbalance in current still forces the output voltage to swing in the same way albeit with a slower slew rate. The circuit would still operate more or less like a diff amp at DC when the current through  $M_3$  and  $M_4$  is greater than  $\frac{1}{2}I_b$ , but really, it is best to keep it above or equal to  $I_b$ . Having a larger current would not hinder the circuit's operation, but it would be superfluous, as the maximum current into the output node's parasitic capacitance is still  $I_1 - I_2$ .
- (e) I used the cascode bias voltage generator that we went over in class and described in Brad's [paper on the subject](#), shown in Figure 3.

## 2. Xschem Simulations

The folded-cascode differential amplifier is shown in Figure 2, and the bias voltage generator is shown in Figure 3.

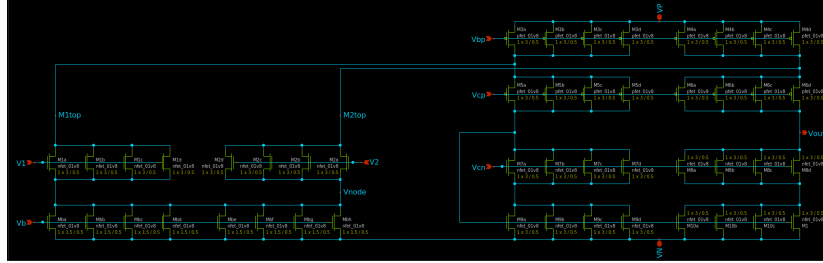


Figure 2: Xschem schematic for folded-cascode differential amplifier.

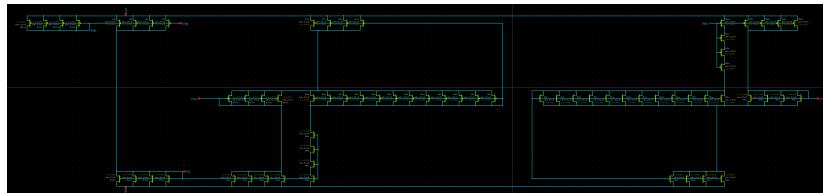


Figure 3: Xschem schematic for bias voltage generator circuit.

- (a) Figure 4 shows the test harness used to analyze the voltage transfer characteristics with  $V_2$  set at various constant voltages over the entire common-mode input range in increments of  $0.2V$ . At  $V_2 = 800mV$  and above, the output has a gain of over 800 and approaches the rails asymptotically (but more quickly on the pull-down side, probably due to better

mobility of electrons than holes). For  $V_2 = 600mV$  and below, the output does not reach the lower rails. This makes sense, because the common-mode input voltage is below the acceptable range of  $V_{CM} \geq V_{bn} + V_{DS,sat}$ , where  $V_{bn} \approx 670mV$  and  $V_{DS,sat} \approx 100mV$ .

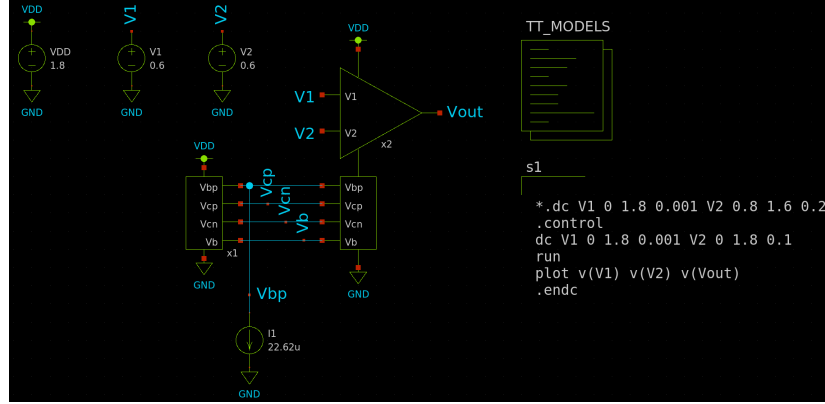


Figure 4: Test harness for diff amp VTCs.

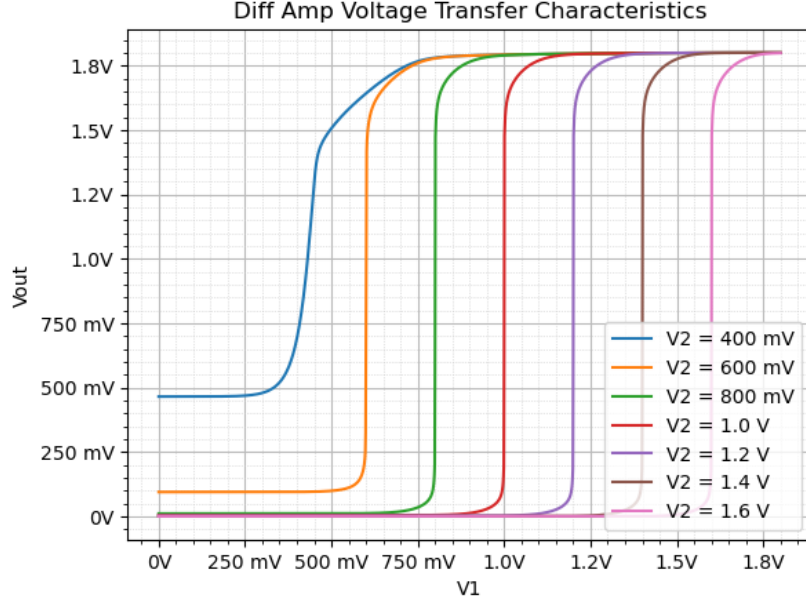


Figure 5: Diff amp voltage transfer characteristics for  $0.4V \leq V_2 \leq 1.6V$ .

- (b) Figure 6 shows the test harness used to analyze the IV characteristic with  $V_2 = 0.8V$  and the output node held at  $0.8V$ . When  $V_1 = V_2$ , the output current is zero. The incremental transconductance gain  $\frac{\delta I_{sat}}{\delta V_G}$  is around  $176\mu A/V$ . Given that the intrinsic gain is given by the product of the incremental transconductance gain and the early effect resistance  $g_m \cdot r_o$ , this implies that  $r_o \approx 4.66M\Omega$ , which is a reasonable value. The current approaches  $+20\mu A / -17\mu A$ , which is nearly  $\pm I_b$ , where  $I_b \approx 22.62\mu A$ .

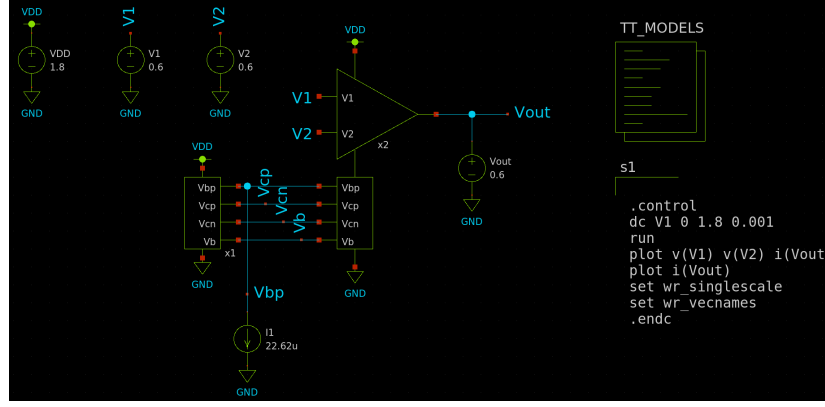


Figure 6: Test harness for IV characteristic.

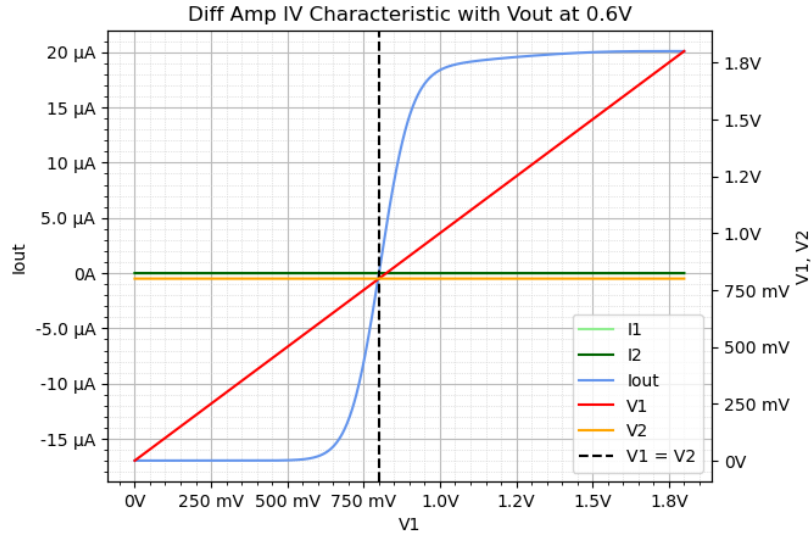


Figure 7: Diff amp IV characteristic for  $V_{out} = 0.6V$ .

- (c) Figure 8 shows the test harness used to analyzed the loopgain of the diff amp, which is plotted in Figure 7. The DC gain at DC is  $+53dB \approx 468$ , which is on the same order of magnitude as the DC intrinsic gain obtained from the VTC. The unity-gain crossover frequency is at  $798kHz$ , which is close to the  $1MHz$  expected given the bias current value. The phase margin is  $89^\circ$ , and the gain margin is  $42dB$ , which is very stable. The loopgain magnitude falls off at a very consistent  $20dB/decade$  with a cutoff frequency of around  $1kHz$ ; the phase reveals two poles centered around the unity-gain bandwidth at roughly  $1kHz$  and  $90MHz$ .

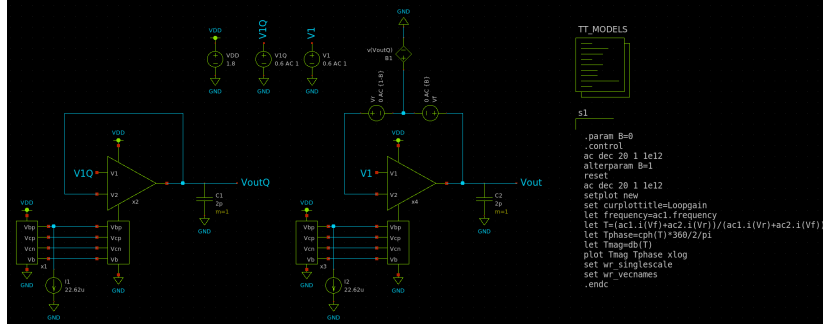


Figure 8: Test harness for loopgain characteristic.

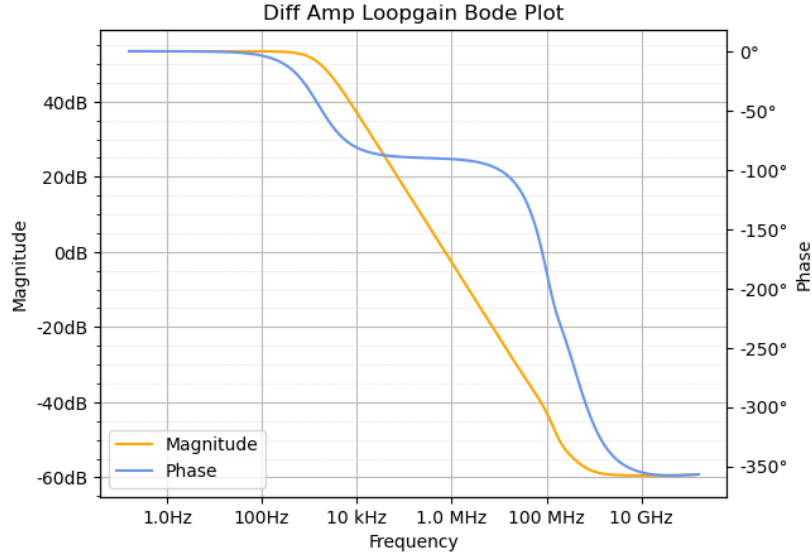


Figure 9: Diff amp loopgain characteristic.

- (d) Figure 10 shows the test harness used to analyze the unity-gain closed-loop frequency response. The  $-3dB$  cutoff frequency is exactly  $798kHz$ , which is the same as the unity-gain crossover frequency from the loopgain analysis. At this frequency, the phase shift is  $-48.3^\circ$ , which is close to the  $-45^\circ$  expected from a first-order low-pass filter.

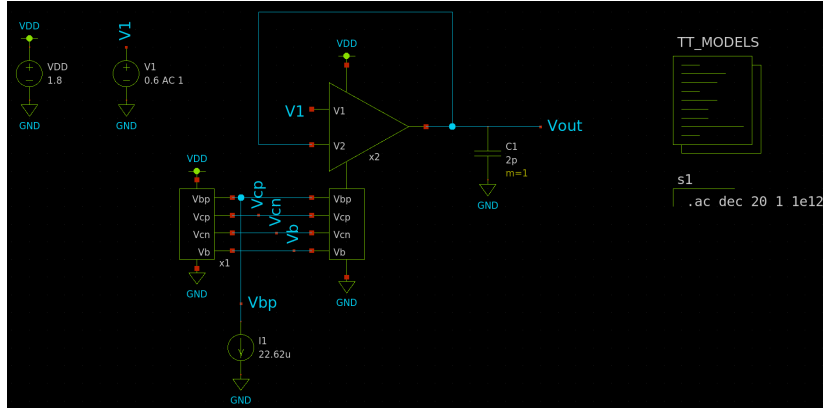


Figure 10: Test harness for AC closed loop analysis.

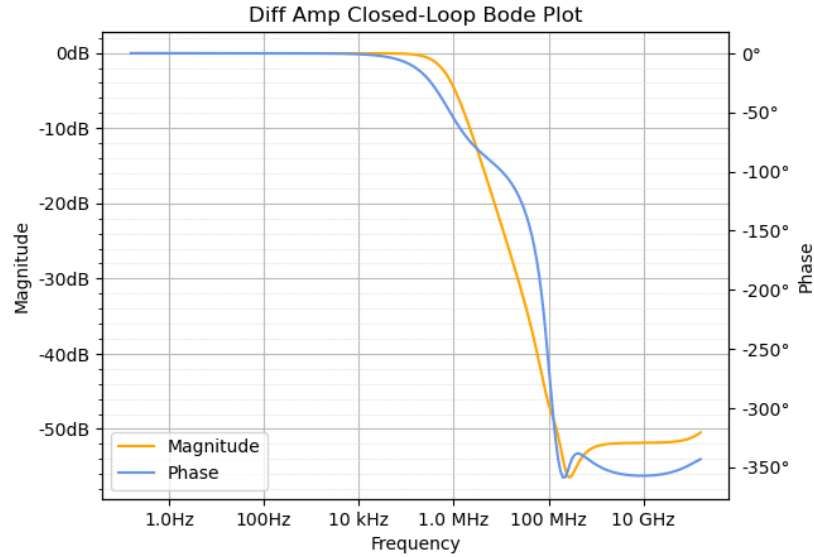


Figure 11: Diff amp AC closed loop analysis.

## 2 Xschem Layout-Driven Schematic

## 3 Magic Layout

## 4 Netgen LVS

The circuits match uniquely between the Xschem schematic and the Magic layout. See the contents of the 'comp.log' file from Netgen below.

Circuit 1 cell sky130\_fd\_pr\_\_nfet\_01v8 and Circuit 2 cell sky130\_fd\_pr\_\_nfet\_01v8 are black boxes.  
Equate elements: no current cell.  
Device classes sky130\_fd\_pr\_\_nfet\_01v8 and sky130\_fd\_pr\_\_nfet\_01v8 are equivalent.

Circuit 1 cell sky130\_fd\_pr\_\_pfet\_01v8 and Circuit 2 cell sky130\_fd\_pr\_\_pfet\_01v8 are black boxes.  
Equate elements: no current cell.  
Device classes sky130\_fd\_pr\_\_pfet\_01v8 and sky130\_fd\_pr\_\_pfet\_01v8 are equivalent.

Flattening unmatched subcell flipflop\_layout in circuit shift\_register\_lvs.spice (0)(4 instances)  
Flattening unmatched subcell shift\_register\_inverter\_2 in circuit shift\_register\_lvs.spice (0)(1 instance)  
Flattening unmatched subcell shiftregister\_inverter in circuit shiftregister.spice (1)(1 instance)  
Flattening unmatched subcell flipflop in circuit shiftregister.spice (1)(4 instances)

Subcircuit summary:

Circuit 1: shift_register_lvs.spice	Circuit 2: shiftregister.spice
sky130_fd_pr__nfet_01v8 (30)	sky130_fd_pr__nfet_01v8 (30)
sky130_fd_pr__pfet_01v8 (30)	sky130_fd_pr__pfet_01v8 (30)
Number of devices: 60	Number of devices: 60
Number of nets: 30	Number of nets: 30

Netlists match uniquely with property errors.

shift\_register\_inverter\_2/7/sky130\_fd\_pr\_\_pfet\_01v8:M4 vs. shiftregister\_inverter\_0/sky130\_fd\_pr\_\_pfet\_01v8:M4  
W circuit1: 1 circuit2: 2 (delta=66.7%, cutoff=1%)  
shift\_register\_inverter\_2/7/sky130\_fd\_pr\_\_pfet\_01v8:M3 vs. shiftregister\_inverter\_0/sky130\_fd\_pr\_\_pfet\_01v8:M3  
W circuit1: 1 circuit2: 2 (delta=66.7%, cutoff=1%)

Cells have no pins; pin matching not needed.

Device classes `shift_register_lvs.spice` and `shiftregister.spice` are equivalent.

Final result: Circuits match uniquely.  
Property errors were found.

The following cells had property errors:  
`shift_register_lvs.spice`