VLSI Mini-Project 3

Folded-Cascode Differential Amplifier

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1 Circuit Analysis

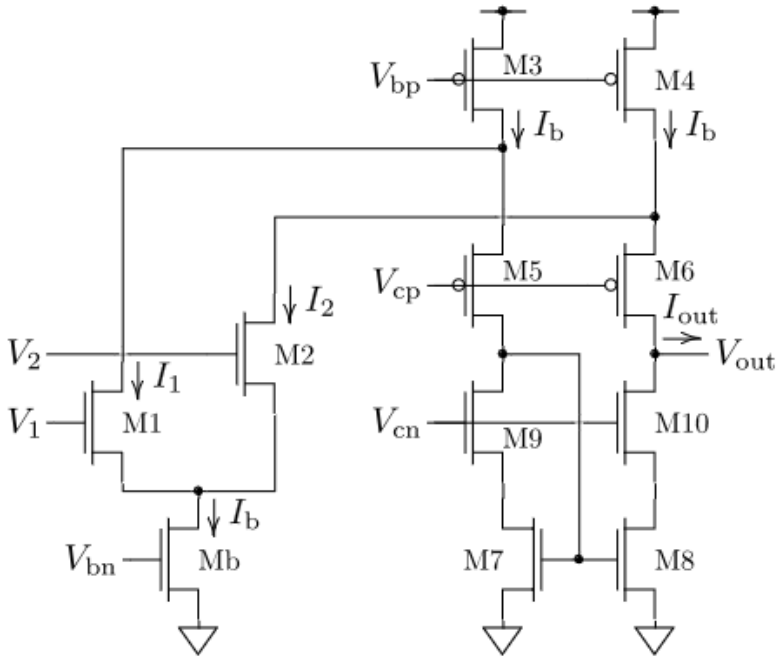

Figure 1: Folded-cascode differential amplifier from MP3 handout.

1. Circuit Analysis

   (a) The circuit makes use of the diff pair M_1, M_2 to draw a variable amount of current out of the drains of M_3 and M_4. When $I_1 \neq I_2$, then the currents in the lower branches M_5 through M_{10} become unequal. Because the pull-down transistors M_7 through M_{10} are in a current mirror configuration driven by the left hand side, the currents can only be solved for if V_{out} slams to less than $2V_{DS,sat}$ away from the rails to put M_6 and M_4 or M_{10} and M_8 into the ohmic region.

   V_1 is the non-inverting input, because when $I_1 > I_2$, then the pull-down transistors on the left draw less current, which is mirrored to the pull-down transitors on the right, and so M_6 is passing more current than M_{10} and M_8 are able to, and V_{out} rises to put M_6 and M_4 into the ohmic region.

   V_2 is the inverting input, because when $I_1 < I_2$, then the pull-down transistors on the left draw more current, which is mirrored to the pull-down transitors on the right, and M_6

cannot pass as much current as M_{10} and M_8 are trying to, and so V_{out} falls to put M_{10} and M_8 into the ohmic region.

(b) M_1 or M_2 must be capable of passing at least I_b. For this, one of their gate voltages V_1 and V_2 must be at least V_{bn} higher than the conmmon-source voltage V_{node}, such that V_{GS} for M_1 or M_2 is around V_{GS} for M_b. For the circuit to work correctly, M_b must be in saturation, so $V_{node} \geq V_{DS,sat}$. Therefore, we have that $V_{CM} \geq V_{bn} + V_{DS,sat}$.

M_3 and M_4 should also be capable of passing I_b, which means they should remain in saturation. This provides an upper bound in the form of $V_{node} \leq V_{DD} - V_{DS,sat}$. We already established that V_1 or V_2 is V_{bn} higher than V_{node}, so $V_{CM} - V_{bn} \leq V_{DD} - V_{DS,sat}$, or $V_{CM} \leq V_{DD} - V_{DS,sat} + V_{bn}$. Since $V_{bn} > V_{DS,sat}$, the upper limit of V_{CM} is only given by V_{DD}. Therefore, we have $V_{bn} + V_{DS,sat} \leq V_{CM} \leq V_{DD}$.

(c) Let the current through M_3 and M_4 be I_b based on the bias voltage V_{bp}, where $I_b \geq I_1, I_2$. The current through M_7, M_9 is $I_b - I_1$, and it is mirrored over to M_8, M_{10} if all transistors are in saturation. The current through M_6 is $I_b - I_2$. By Kirchoff's Current Law, the current into the output node is $I_b - I_2 - (I_b - I_1) = I_1 - I_2$.

(d) The current through M_3 and M_4 must be at least I_b, because when $V_1 \neq V_2$, then either $I_1 = I_b$ or $I_2 = I_b$. If M_3 or M_4 could not source this current, then M_1 or M_2 would have to fall out of saturation, and the behavior of the ciruit would be compromised. You might be able to make an argument that in this case, one of the currents is still larger than the other, and the imbalance in current still forces the ouput voltage to swing in the same way albeit with a slower slew rate. The circuit would still operate more or less like a diff amp at DC when the current through M_3 and M_4 is greater than $\frac{1}{2}I_b$, but really, it is best to keep it above or equal to I_b. Having a larger current would not hinder the circuit's operation, but it would be superfluous, as the maximum current into the output node's parasitic capacitance is still $I_1 - I_2$.

(e) I used the cascode bias voltage generator that we went over in class and described in Brad's paper on the subject, shown in Figure 3. Because the example in the paper only produces a voltage for an nMOS cascode configuration, I created a second copy of the circuit and flipped it by switching nMOS with pMOS and switching V_{DD} and GND. Finally, to accept a bias current for both the nMOS and pMOS circuits, I created a pMOS current mirror linked to an nMOS current mirror to produce the same current through both circuits.

2. Xschem Simulations

The folded-cascode differential amplifier is shown in Figure 2, and the bias voltage generator is shown in Figure 3.

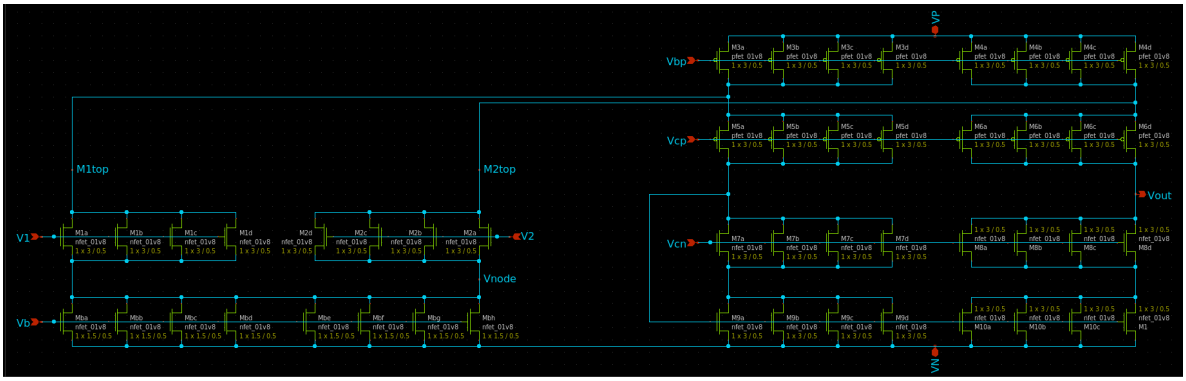

Figure 2: Xschem schematic for folded-cascode differential amplifier.

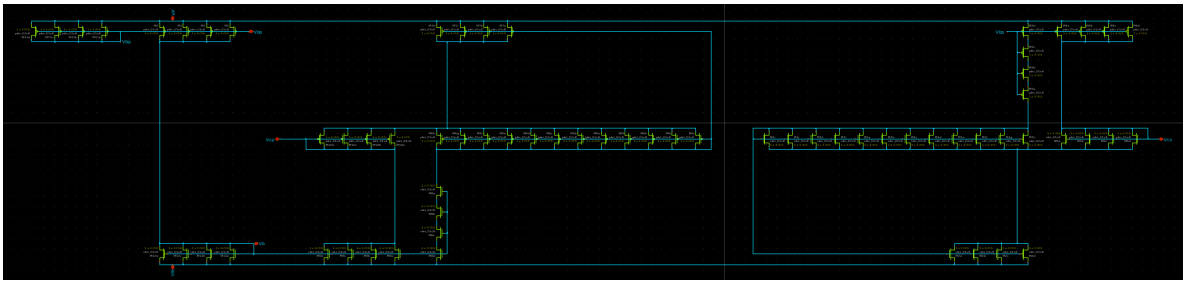

Figure 3: Xschem schematic for bias voltage generator circuit.

(a) Figure 4 shows the test harness used to analyze the voltage transfer characteristics with V_2 set at various constant voltages over the entire common-mode input range in increments of $0.2V$. At $V_2 = 800mV$ and above, the output has a gain of over 800 and approaches the rails asymptotically (but more quickly on the pull-down side, probably due to better mobility of electrons than holes). For $V_2 = 600mV$ and below, the output does not reach the lower rails. This makes sense, because the common-mode input voltage is below the acceptable range of $V_{CM} \geq V_{bn} + V_{DS,sat}$, where $V_{bn} \approx 670mV$ and $V_{DS,sat} \approx 100mV$.

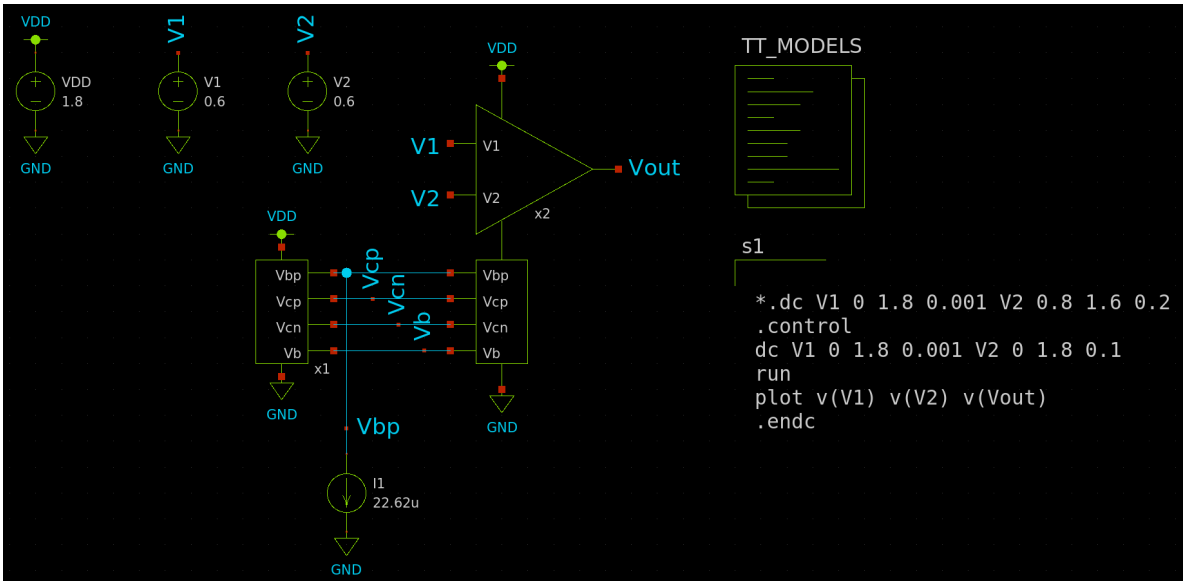

Figure 4: Test harness for diff amp VTCs.

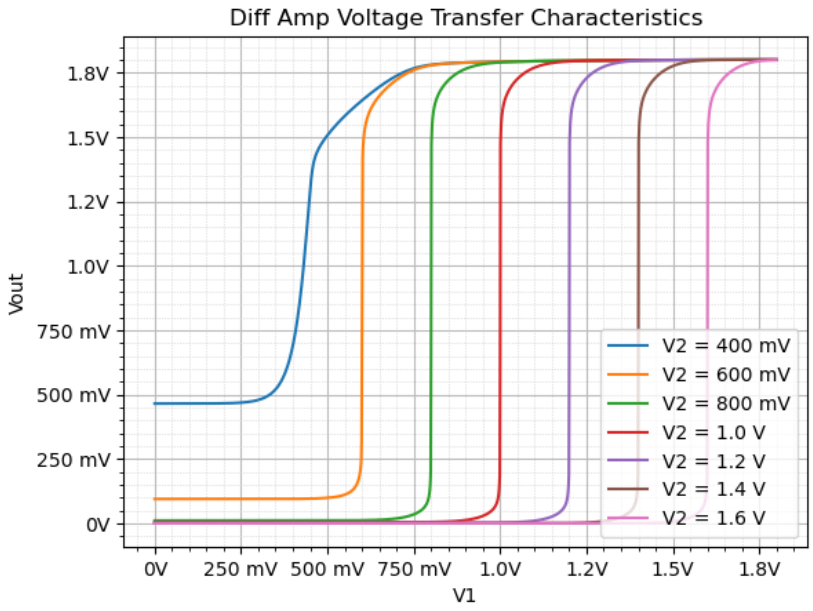

Figure 5: Diff amp voltage transfer characteristics for $0.4V \leq V_2 \leq 1.6V$.

(b) Figure 6 shows the test harness used to analyze the IV characteristic with $V_2 = 0.8V$ and the output node held at 0.8V. When $V_1 = V_2$, the output current is zero. The incremental transconductance gain $\frac{\delta I_{sat}}{\delta V_G}$ is around $176\mu A/V$. Given that the intrinsic gain is given by the product of the incremental transconductance gain and the early effect resistance $g_m \cdot r_o$, this implies that $r_o \approx 4.66M\Omega$, which is a reasonable value. The current approaches $+20\mu A/-17\mu A$, which is nearly $\pm I_b$, where $I_b \approx 22.62\mu A$.

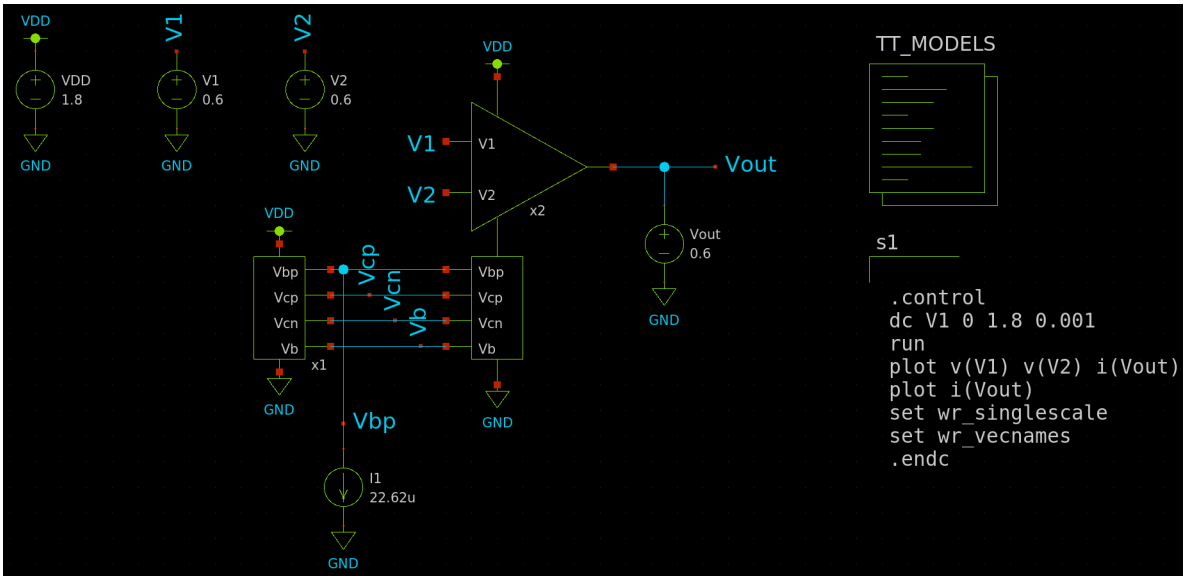

Figure 6: Test harness for IV characteristic.

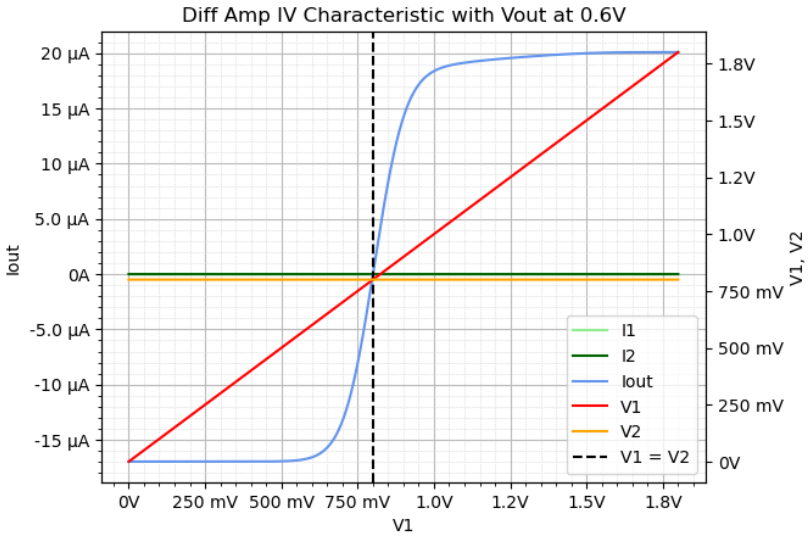

Figure 7: Diff amp IV characteristic for $V_{out} = 0.6V$.

(c) Figure 8 shows the test harness used to analyzed the loopgain of the diff amp, which is plotted in Figure 7. The DC gain at DC is $+53dB \approx 468$, which is on the same order of magnitude as the DC intrinsic gain obtained from the VTC. The unity-gain crossover frequency is at $798kHz$, which is close to the $1MHz$ expected given the bias current value. The phase margin is 89°, and the gain margin is $42dB$, which is very stable. The loopgain magnitude falls off at a very consistent $20dB$/decade with a cutoff frequency of around $1kHz$; the phase reveals two poles centered around the unity-gain bandwidth at roughly $1kHz$ and $90MHz$.

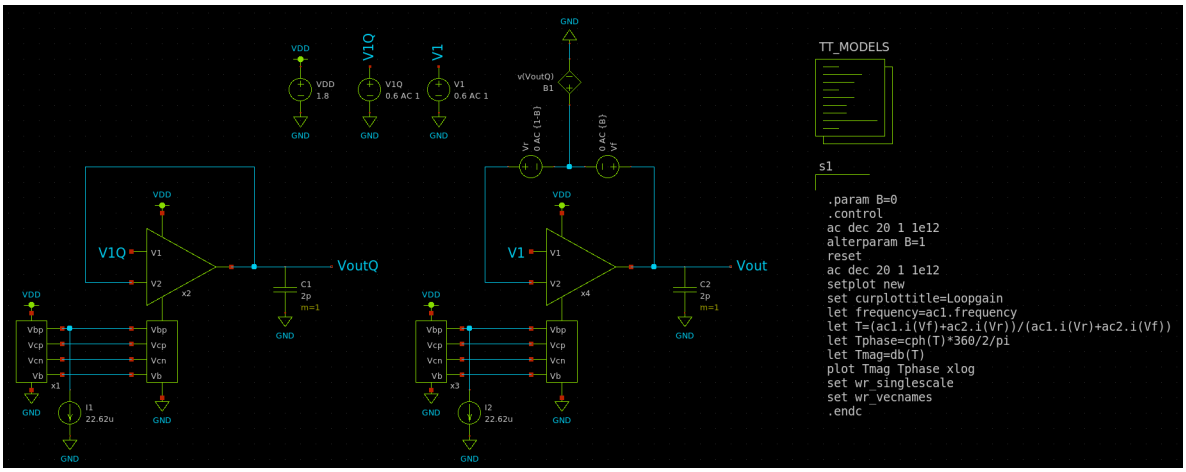

Figure 8: Test harness for loopgain characteristic.

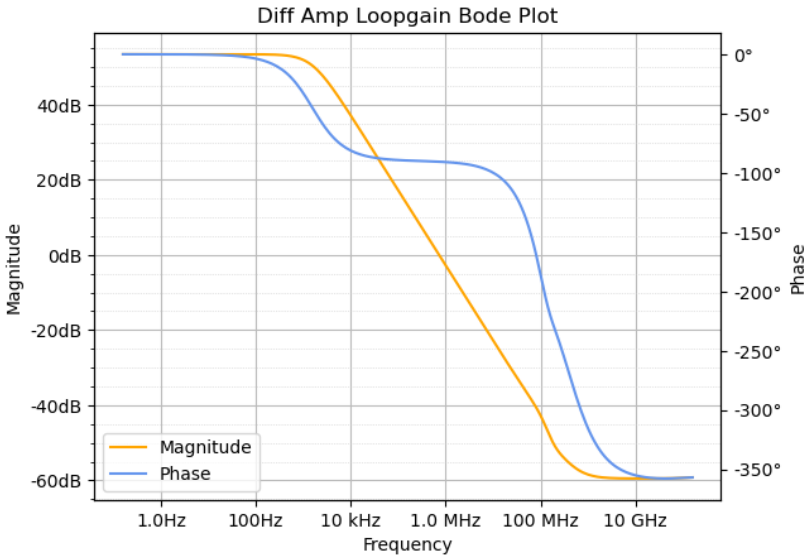

Figure 9: Diff amp loopgain characteristic.

(d) Figure 10 shows the test harness used to analyze the unity-gain closed-loop frequency response. The $-3dB$ cutoff frequency is exactly $798kHz$, which is the same as the unity-gain crossover frequency from the loopgain analysis. At this frequency, the phase shift is $-48.3°$, which is close to the $-45°$ expected from a first-order low-pass filter.

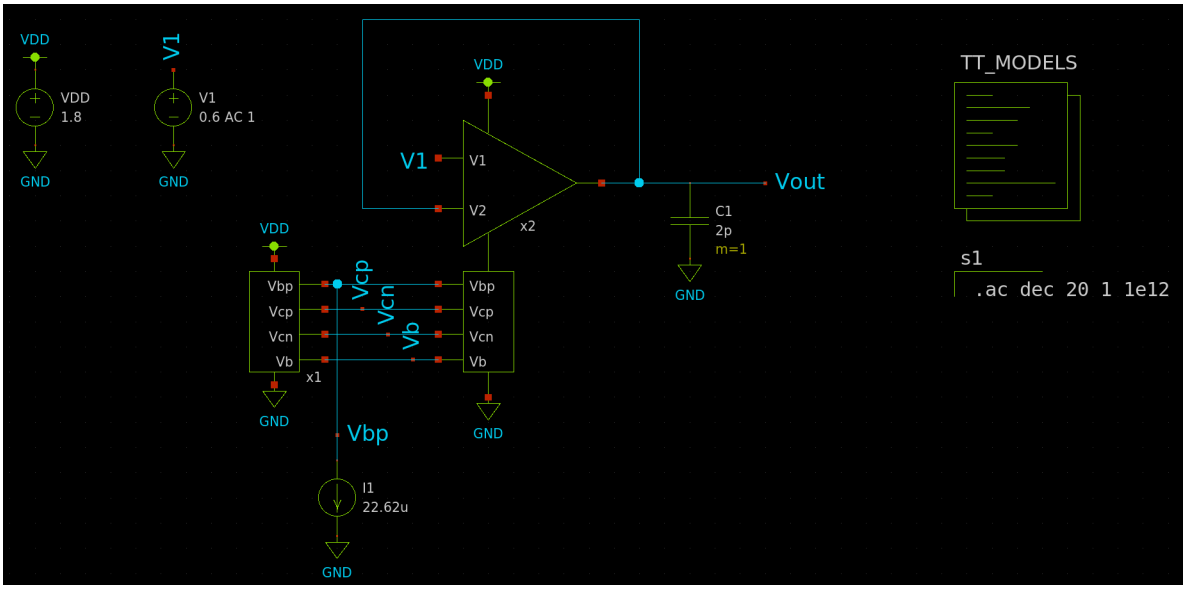

Figure 10: Test harness for AC closed loop analysis.

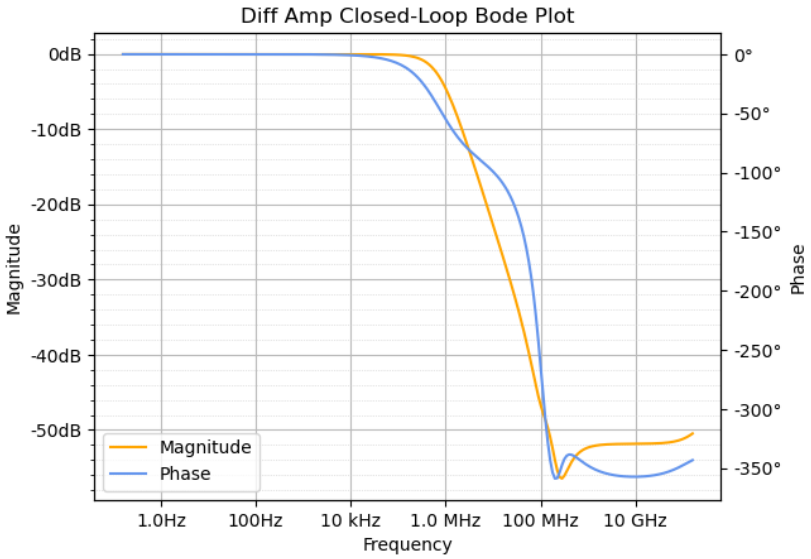

Figure 11: Diff amp AC closed loop analysis.

2 Xschem Layout-Driven Schematic

Figures 12 and 13 show the layout-driven schematics for the diff amp and bias voltage generator, respectively. I used at least four units for each transistor with transistors requiring matching having their units interleaved in a common-centroid configuration. For the diff amp, I found it most convenient to place the diff pair transistors at the top of the layout so that the drains would be close to the topmost pMOS transistors.

I performed LVS comparisons for both circuits with their corresponding schematics in Figures 2 and 3, respectively, after adding dummy transistors to the original schematics.

Lastly, I created symbols for the circuits containing dummy devices and connected them as shown in Figure 14 to perform LVS on the entire circuit in Magic.

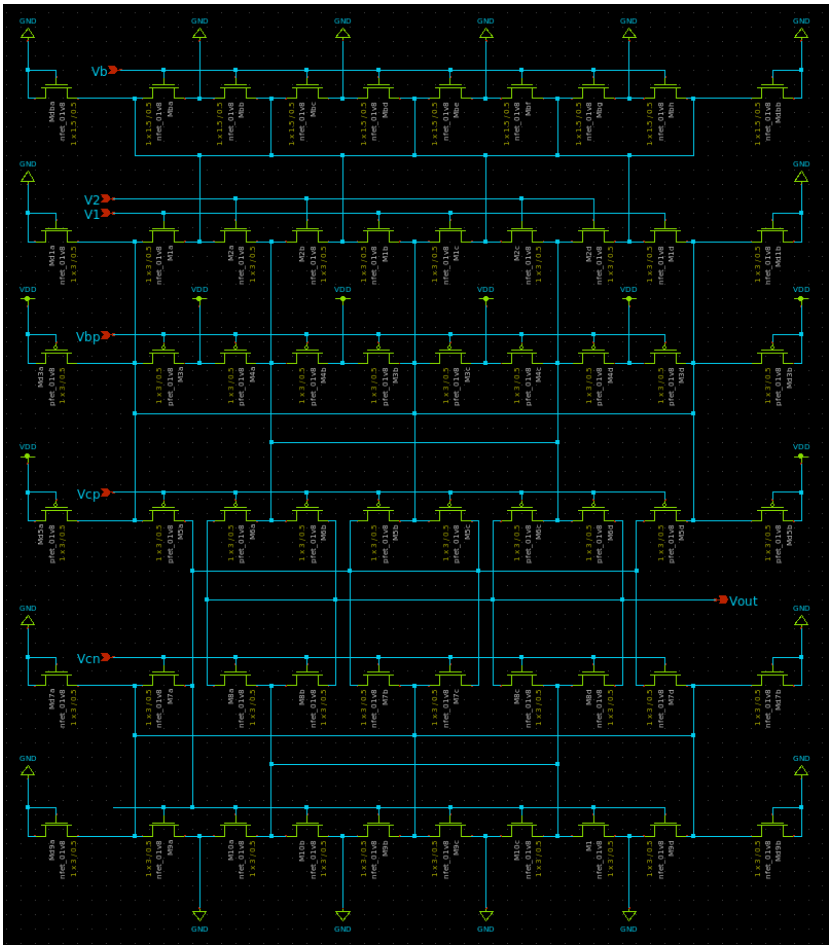

Figure 12: Layout-driven schematic for diff amp in Xschem.

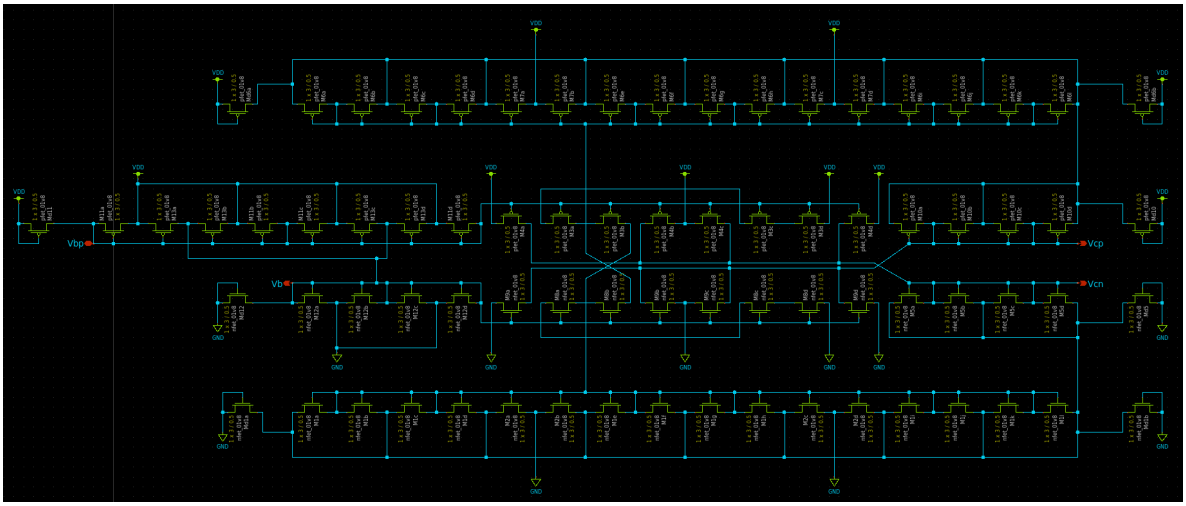

Figure 13: Layout-driven schematic for bias voltage generator in Xschem.

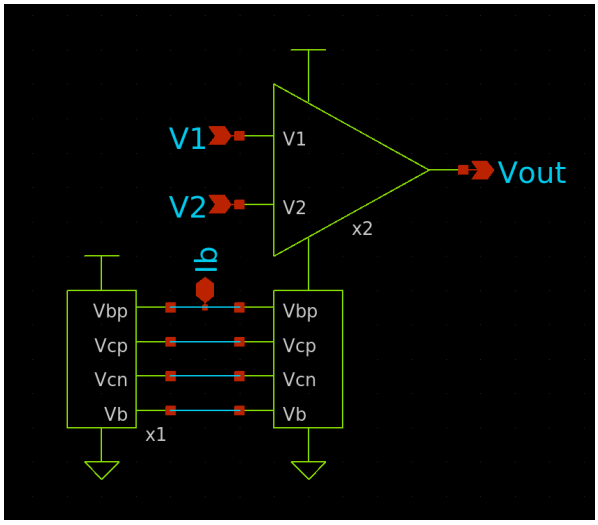

Figure 14: Symbols used for diff amp and bias voltage generator circuit in Xschem for top-level LVS comparison.

3 Magic Layout

Figures 15, 16, and 17 show the layout of the diff amp, the bias voltage generation circuit, and the combination of the two cells in Magic. The diff amp contains substrate diffusion regions on the outside edges of each row of transistors (except for the two rows near the bottom which are wider). The bias voltage generator contains diffusion regions in the corners as well as four smaller regions closer to the center. The inputs V_1 and V_2 to the combined layout are the two metal prongs along the top left edge of the diff amp. The bias current connection is on the left side of the bias voltage generator, just below the power plane. The output of the diff amp is a thin metal wire on the lower right.

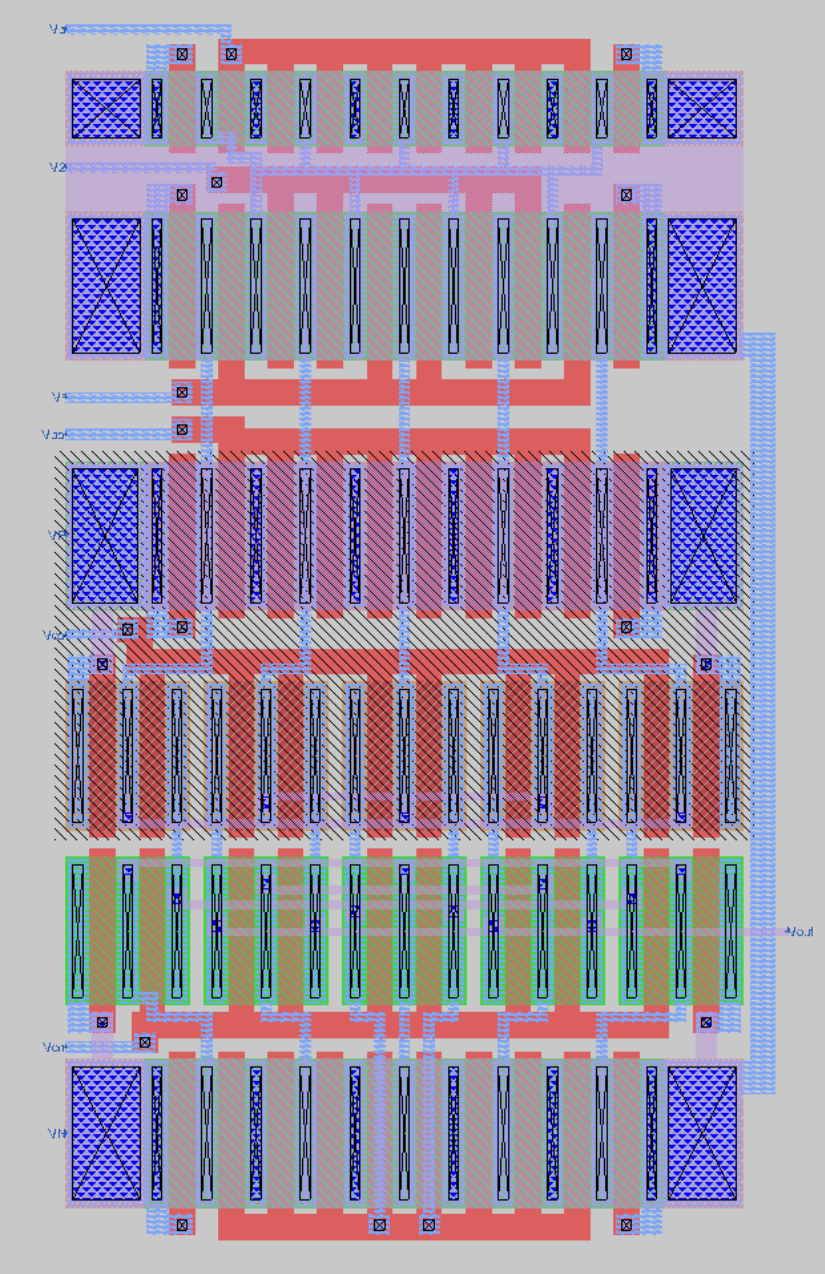

Figure 15: Layout of diff amp in Magic.

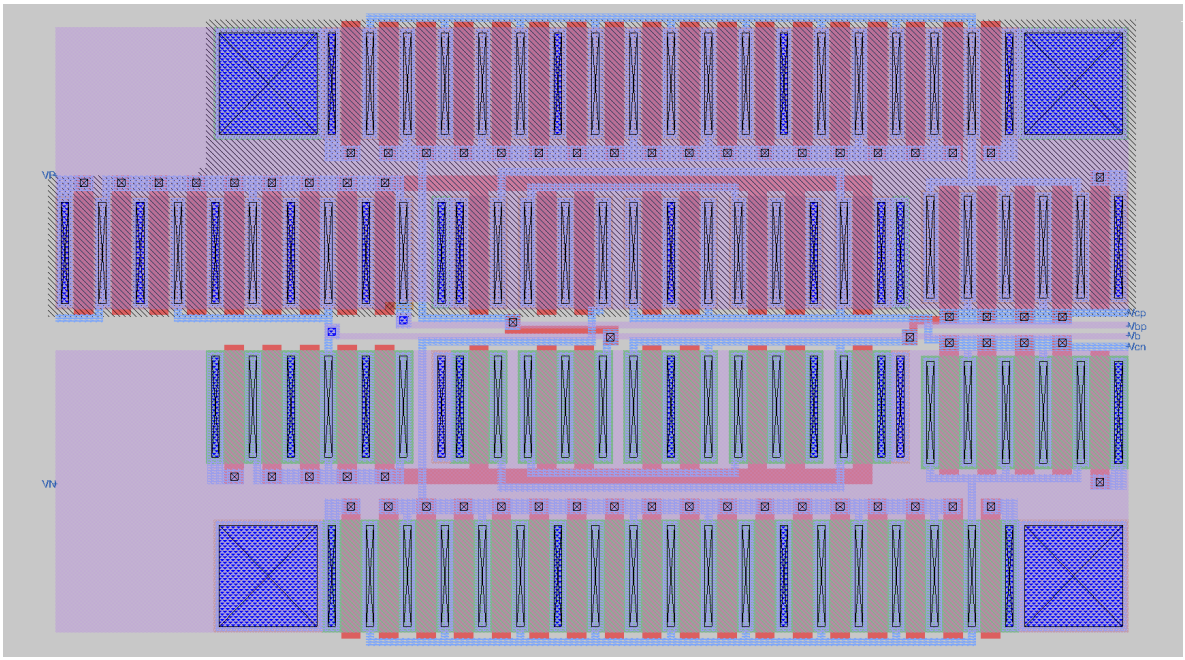

Figure 16: Layout of bias voltage generator circuit in Magic.

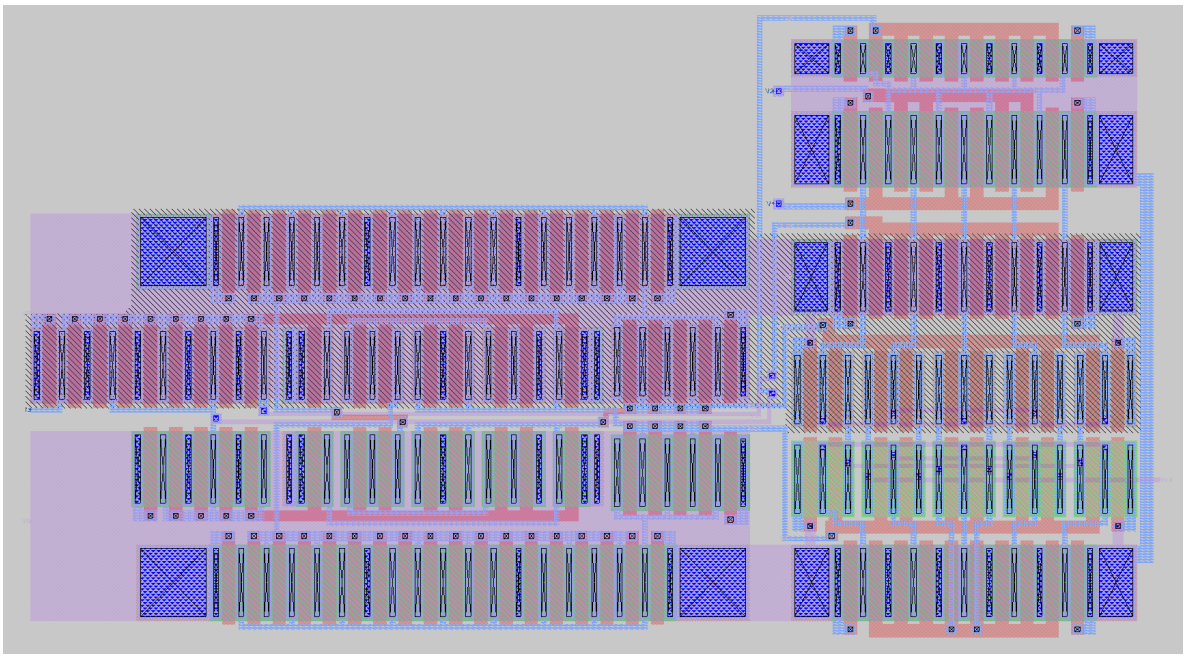

Figure 17: Combined layout of diff amp and bias voltage generator as subcells in Magic.

4 Netgen LVS

The circuits match uniquely between the Xschem schematic and the Magic layout. See the contents of the 'comp.log' file from Netgen below.

```
Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are black boxes.
```

```
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.

Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.
Flattening unmatched subcell nmos_test in circuit mp1/magic/buffer_test.spice (0)(2 instances)
Flattening unmatched subcell inverter in circuit mp1/magic/buffer_xschem.spice (1)(2 instances)

Subcircuit summary:
Circuit 1: mp1/magic/buffer_test.spice     |Circuit 2: mp1/magic/buffer_xschem.spice
-------------------------------------------|-------------------------------------------
sky130_fd_pr__pfet_01v8 (2)                |sky130_fd_pr__pfet_01v8 (2)
sky130_fd_pr__nfet_01v8 (2)                |sky130_fd_pr__nfet_01v8 (2)
Number of devices: 4                       |Number of devices: 4
Number of nets: 5                          |Number of nets: 5
-----------------------------------------------------------------------------------------
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes mp1/magic/buffer_test.spice and mp1/magic/buffer_xschem.spice are equivalent.

Final result: Circuits match uniquely.
```

5 GitHub Files

All of my files for Mini-Project 3 are in my GitHub repository (currently under the branch *temp*).

I tried to copy all final design files for Mini-Project 3 into the folder entitled mp3/submission).