VLSI Mini-Project 2

4-bit CSRL Shift Register

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1 Introduction

I fully intended to do two complete versions of the layout: first using a conservative analysis of the circuit and a straightforward layout, and then reducing transistor sizes and optimizing for the flip-flop pitch. I figured the former would be easy to accomplish as a minimum viable product, and doing the layout twice would give me insight into an efficient routing scheme. However, I promptly mismanaged my time and did not do a second revision. Hence, the design presented here is functional but not optimized.

2 Xschem Schematic

2.1 Conservative Analysis

Figure 1 shows my layout-driven schematic for the CSRL flip-flop. It is based on the paper and patent application by Massimo Sivilotti, and I checked the netlist of my layout-driven schematic against the schematic copied verbatim from those resources.

The crucial strength ratio requirement occurs when the clock changes from low to high. Since the nMOS transistors will turn on before the pMOS transistors turn off, we have a pull-up network and a pull-down network activated at the same time. On the rising edge, the pull-down network must be stronger, such that a potential high bit from the right-side flip-flop does not propagate backwards into the left-side flip-flop.

The pull-down network consists of the one of the bottoms of the cross-coupled inverters of the $\bar{\phi}$ latch and the clock-gated pull down transistor. The pull-up network consists of one of the clock-gated nMOS pass through transistors of the ϕ latch and one of the tops of the cross-coupled inverters of the ϕ latch. A simple way to guarantee that the pull-down network will win is by assigning a strength of 4 to the nMOS pull-down resistors and a strength of 1 to the nMOS pass through transistors. Thus, treating two of the pull-down transistors as acting in series and ignoring the pMOS transistors which are not easy to compare, we still obtain a 2:1 strength ratio in favor of the pull-down network.

In Figure 1, this means M12, M8, and M9 should have a strength of 4, while all other nMOS transistors should have a strength of 1. A similar argument for the other latch prescribes a strength of 4 for M7, M5, and M6, while all other pMOS transistors should have a strength of 1.

2.2 Next-Level Analysis

It can be readily shown that during the clock transition from low to high that creates the critical case, the gate of the critical inverter is already high. Because the gate voltage is not the limiting factor in the (at first negligible) current through the inverter nMOS, that transistor must be in the ohmic region (cut off due to a small drain-to-source voltage). As the current through the clock-gated nMOS transistors increases, the current through the inverter nMOS will rise as needed. *It does not constrain the strength of the pull-down network*, as defined by the amount of current it is able to sink at a certain instant of the clock voltage. Thus, the strength of the pull-down network for our intents and purposes is equal to the strength of the clock-gated nMOS pull-down transistor.

This analysis allows us to greatly reduce the area of our layout. Not only can we reduce the strength of the clock-gated nMOS pull-down transistor from 4 to 2 by virtue of ignoring the series effects of the inverter nMOS transistors, but the inverter transistors also do not need to be bigger! We end up with the simple requirement that the clock-gated nMOS pull-down transistor have a strength of 2 where all other nMOS transistors have a strength of 1. A similar argument prescribes a strength of 2 for the clock-gated pMOS pull-up transistor in the ϕ latch and a strength of 1 for all other pMOS transistors.

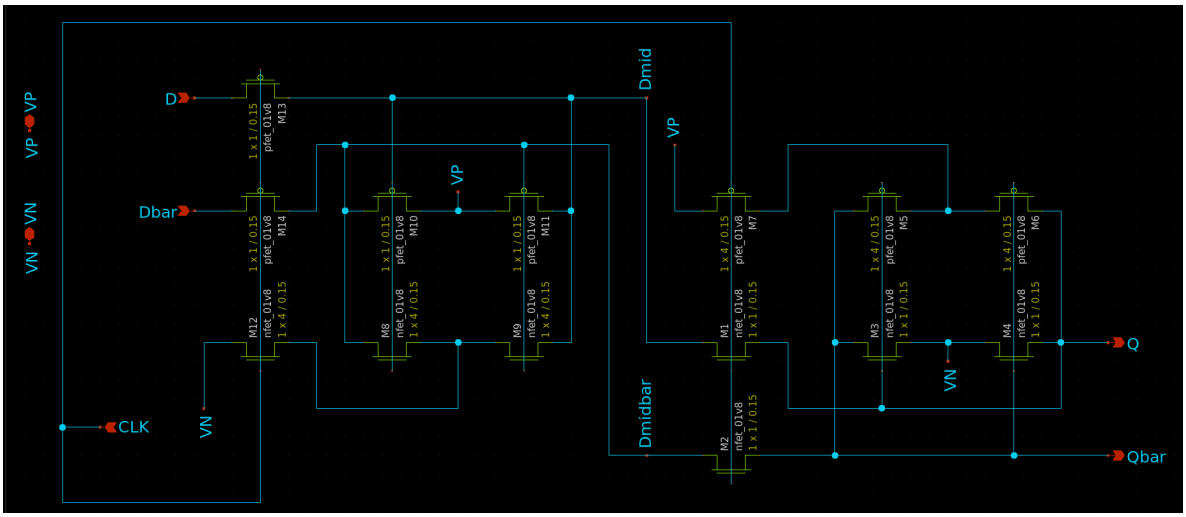

Figure 1: Layout-driven schematic for CSRL rising edge flip-flop.

2.3 Double Inverter

The CSRL latch requires two buffered inputs, D and $\bar{D}$, to effectively drive its state. In a shift register, the buffered signals are provided by the cross-coupled inverters of the opaque latch to the left. However, the first flip-flop in the shift register needs an additional component to provide the appropriate inputs. I used two inverters in series to produce the buffered complementary signals. The first inverter thresholds and buffers the input signal A to become $\bar{D}$, and the second inverter re-creates the signal A at D. Figure 2 shows the schematic for the double inverter, which is represented as one symbol in Figure 3.

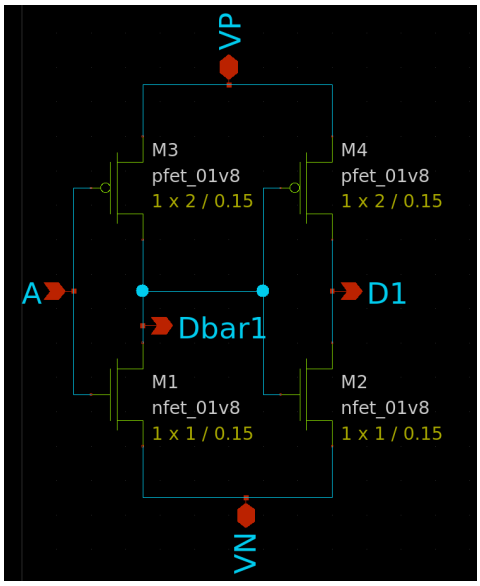

Figure 2: Double CMOS inverter schematic to generate the input signal for the 4-bit shift register.

Figure 3 shows the schematic I used to test the 4-bit CSRL shift register. I tested it first using a ratioless flip-flop design. The output was as desired for the tt, ff, and fs models and failed for the sf and ss models. With the conservative design (three nMOS transistors and three pMOS transistors having strength 4), it works using all corner models.

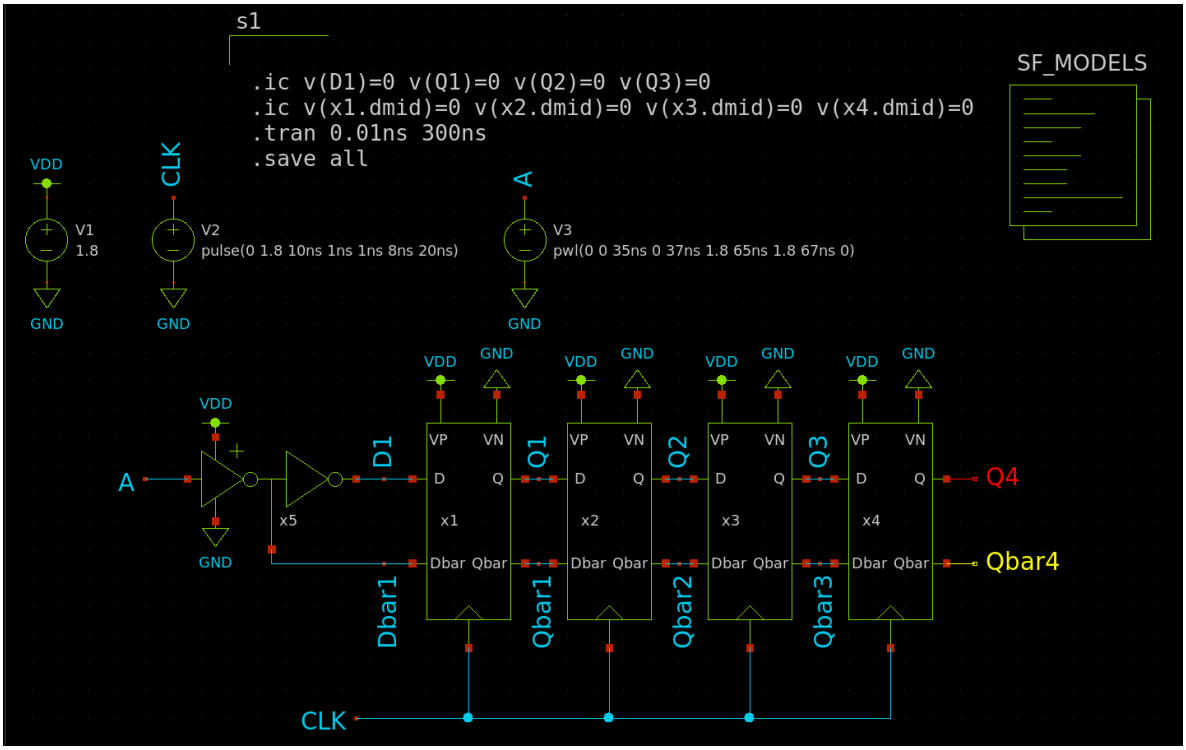

Figure 3: 4-bit CSRL shift register testing setup. Notice that in this test I am using the sf model, which is one of the corner models that failed with the ratioless design.

Figure 4 shows the output of the simulation using the sf corner model. The input A is turned on for just under two clock cycles. As expected, the first flip-flop flips high on the rising edge of the clock. It stays at a weak 1 due to the pass-through nMOS transistor being used as a pull-up during the transparent phase. Then, when the clock falls low, the ϕ latch become opaque and pulls the logic level to the rail. The 1 bit propagates through the shift register on each rising edge of the clock as expected.

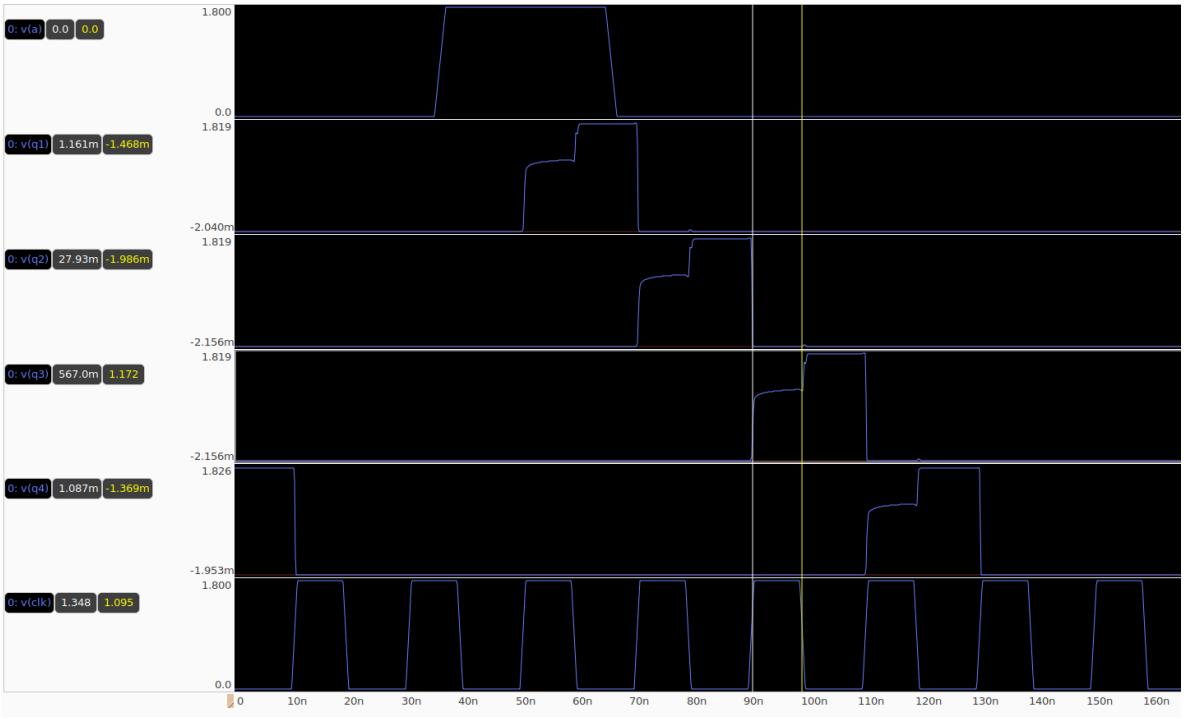

Figure 4: Simulation results for 4-bit CSRL shift register. The bits are stable even for the sf model.

3 Magic Layout

As stated, for my first design, I did not try very hard to optimize the layout, shown in Figure 5. I had three transistors in each latch with strength 4, so I placed them all next to each other because I didn't want to create a very tall stack and have to run long wires. I lined up transistors that shared a gate so that all the gates were perfectly vertical. I am proud of how I routed the cross-coupled inverters along the horizontal centerline. The Q and $\bar{Q}$ outputs on the right hand side line up with the D and $\bar{D}$ inputs on the left so they can easily be composed into a shift register. The clock input is along the bottom.

I had a lot of unused space in my layout, so I created some oversized p-substrate and n-well contacts. I made clever use of the *upsidedown* function in Magic and the fact that painting over a region with nwell or pwell inverts the doping to copy the $\bar{\phi}$ latch to create the ϕ latch. A single CSRL flip-flop cell is 7.15 microns wide by 9.7 microns tall.

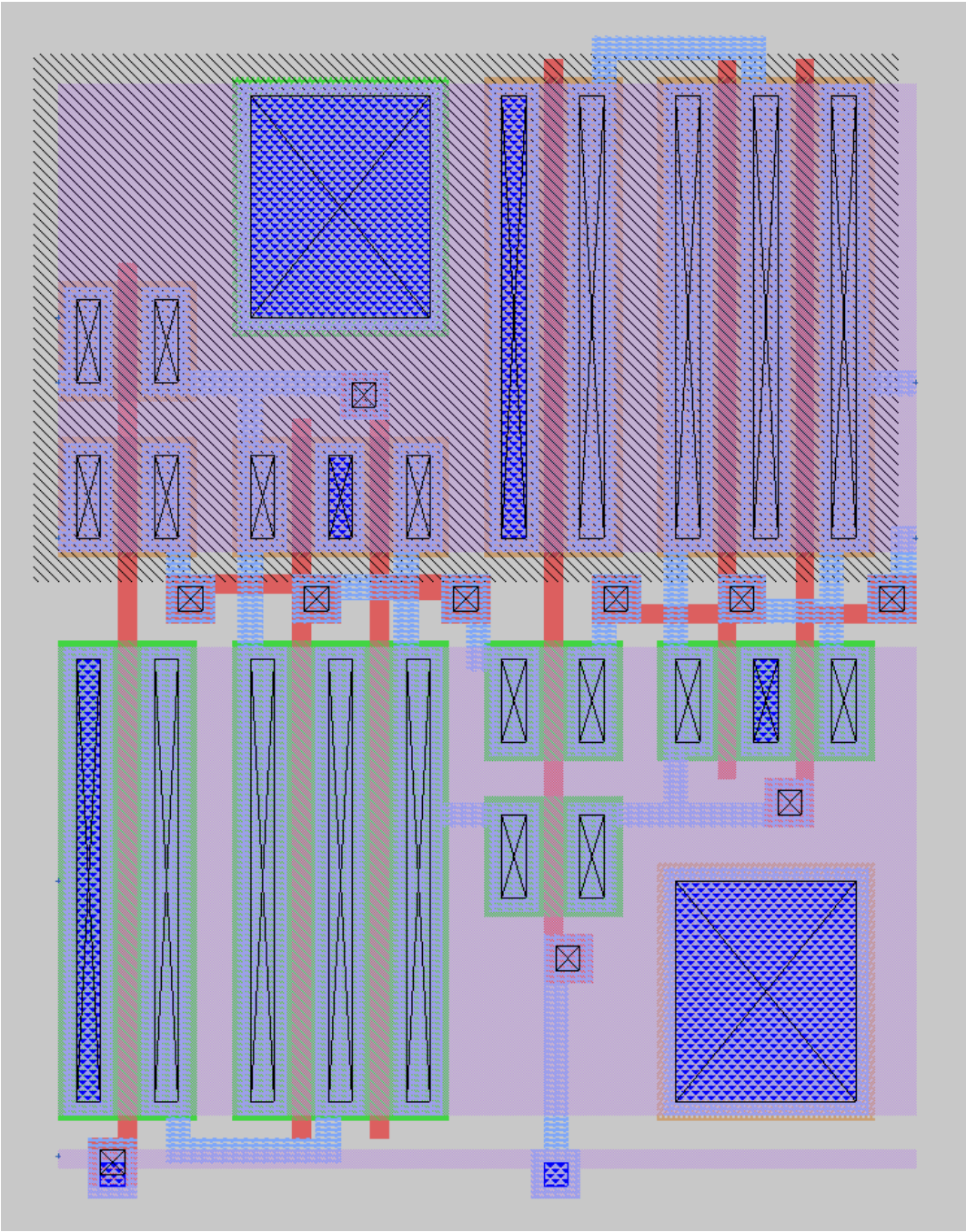

Figure 5: Magic layout of CSRL flip-flop. It was not particularly optimized for pitch. The bounding box is 7.15 microns wide by 9.7 microns tall.

Figure 6 shows the layout of the double inverter which feeds the D and $\bar{D}$ inputs of the first flip-flop. This double inverter was custom designed to interface with the CSRL flip-flop layout.

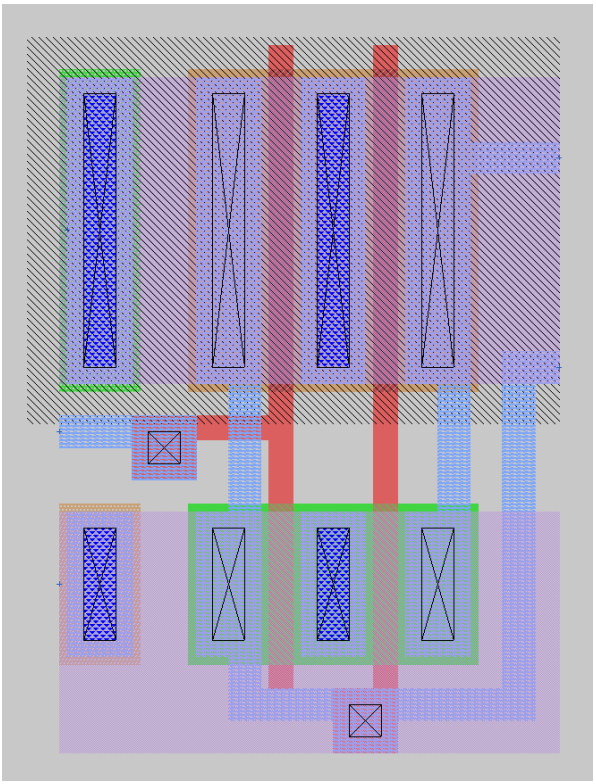

Figure 6: Double CMOS inverter layout.

Figure 7 shows how I composed the double inverter cell with four CSRL flip-flop cells to create a four-bit shift register.

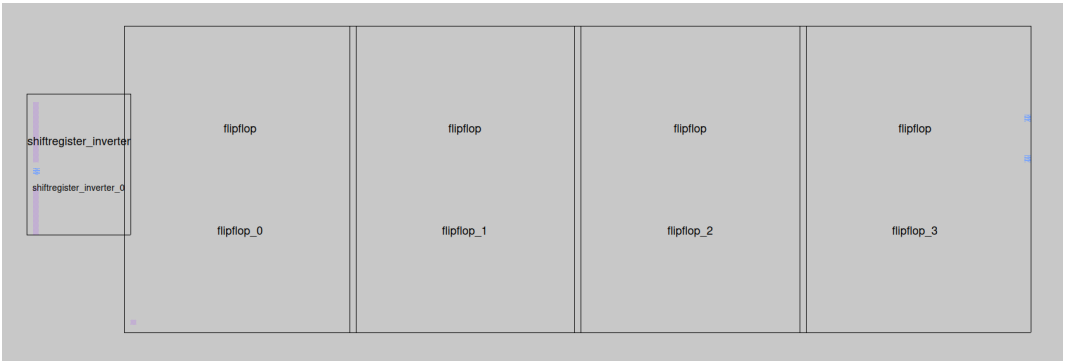

Figure 7: Magic layout showing hierarchical shift register design.

Figure 8 shows the final layout of the 4-bit shift register with the contents of the cells revealed.

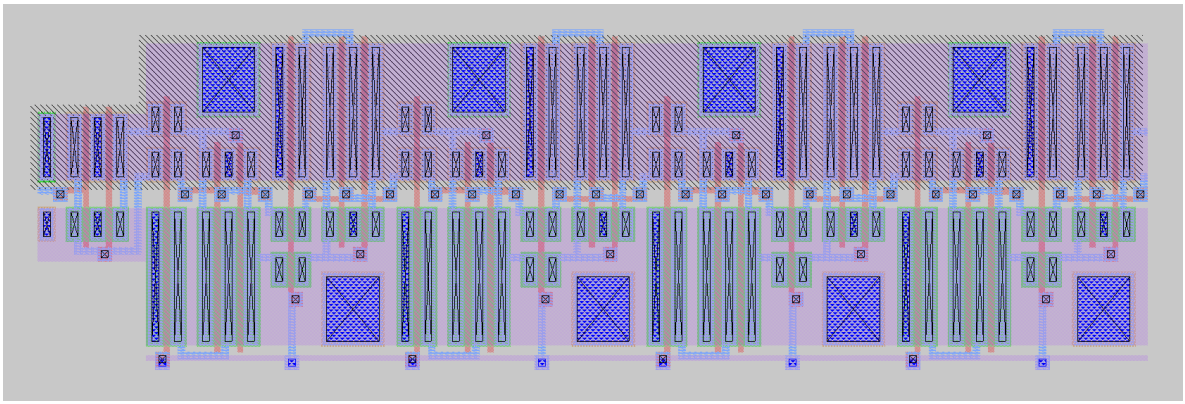

Figure 8: Magic layout showing final 4-bit shift register and input inverters. The bounding box of the entire layout is 31.9 microns wide by 9.7 microns tall.

4 Netgen LVS

The circuits match uniquely between the Xschem schematic and the Magic layout. See the contents of the 'comp.log' file from Netgen below.

```
Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.

Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.
Flattening unmatched subcell flipflop_layout in circuit shift_register_lvs.spice (0)(4 instances)
Flattening unmatched subcell shift_register_inverter_2 in circuit shift_register_lvs.spice (0)(1 inst
Flattening unmatched subcell shiftregister_inverter in circuit shiftregister.spice (1)(1 instance)
Flattening unmatched subcell flipflop in circuit shiftregister.spice (1)(4 instances)

Subcircuit summary:
Circuit 1: shift_register_lvs.spice        |Circuit 2: shiftregister.spice
-------------------------------------------|-------------------------------------------
sky130_fd_pr__nfet_01v8 (30)               |sky130_fd_pr__nfet_01v8 (30)
sky130_fd_pr__pfet_01v8 (30)               |sky130_fd_pr__pfet_01v8 (30)
Number of devices: 60                      |Number of devices: 60
Number of nets: 30                         |Number of nets: 30
-------------------------------------------------------------------------------------
Netlists match uniquely with property errors.
shift_register_inverter_2:7/sky130_fd_pr__pfet_01v8:M4 vs. shiftregister_inverter_0/sky130_fd_pr__pfe
 W circuit1: 1   circuit2: 2   (delta=66.7%, cutoff=1%)
shift_register_inverter_2:7/sky130_fd_pr__pfet_01v8:M3 vs. shiftregister_inverter_0/sky130_fd_pr__pfe
 W circuit1: 1   circuit2: 2   (delta=66.7%, cutoff=1%)
Cells have no pins;  pin matching not needed.
Device classes shift_register_lvs.spice and shiftregister.spice are equivalent.

Final result: Circuits match uniquely.
Property errors were found.

The following cells had property errors:
 shift_register_lvs.spice
```