VLSI Mini-Project 1

CMOS AND Gate Schematic and Layout

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September 12, 2023

1 Xschem Schematic

I implemented a CMOS inverter (Figure 1) and CMOS nand gate (Figure 2) using standard transistor configurations. I chose the widths of the inversion regions to standardize the equivalent strengths of the gates in the worst case scenario. For the inverter, the PMOS transistor had a width of $2\mu m$, and the NMOS transitor had a width of $1\mu m$. For the nand gate, all transistors had a width of $2\mu m$.

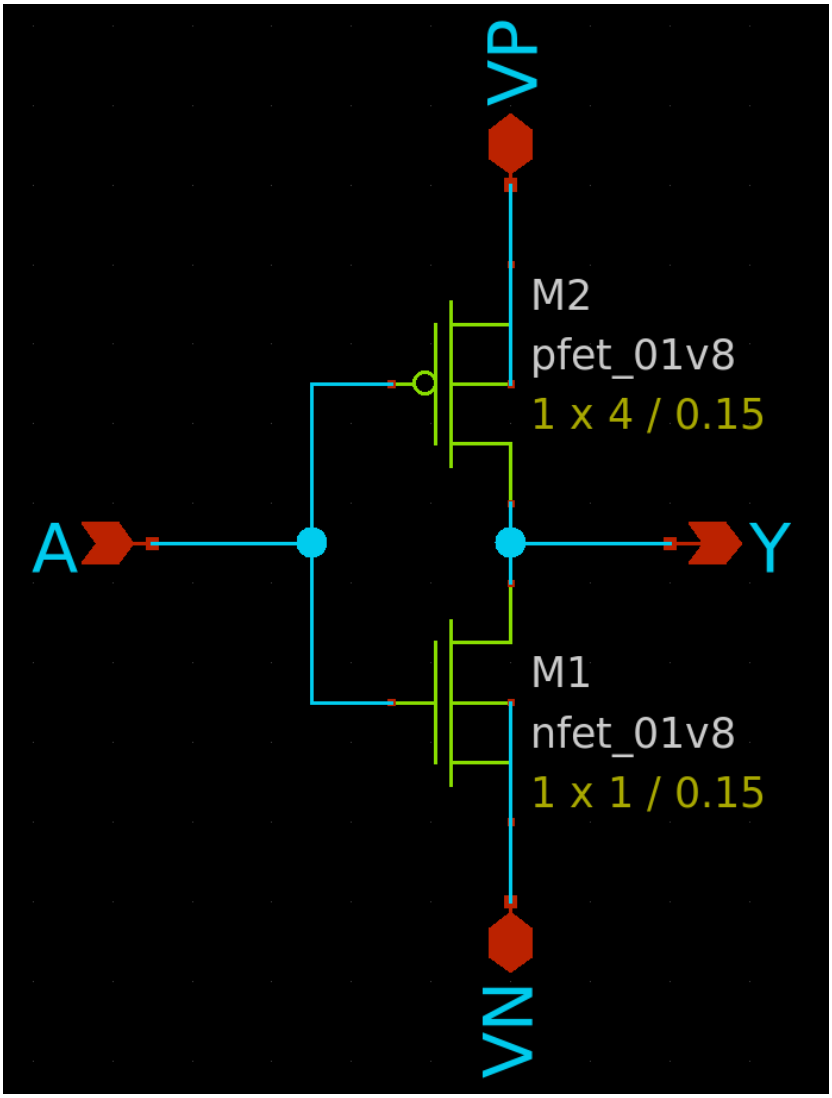

Figure 1: Inverter schematic.

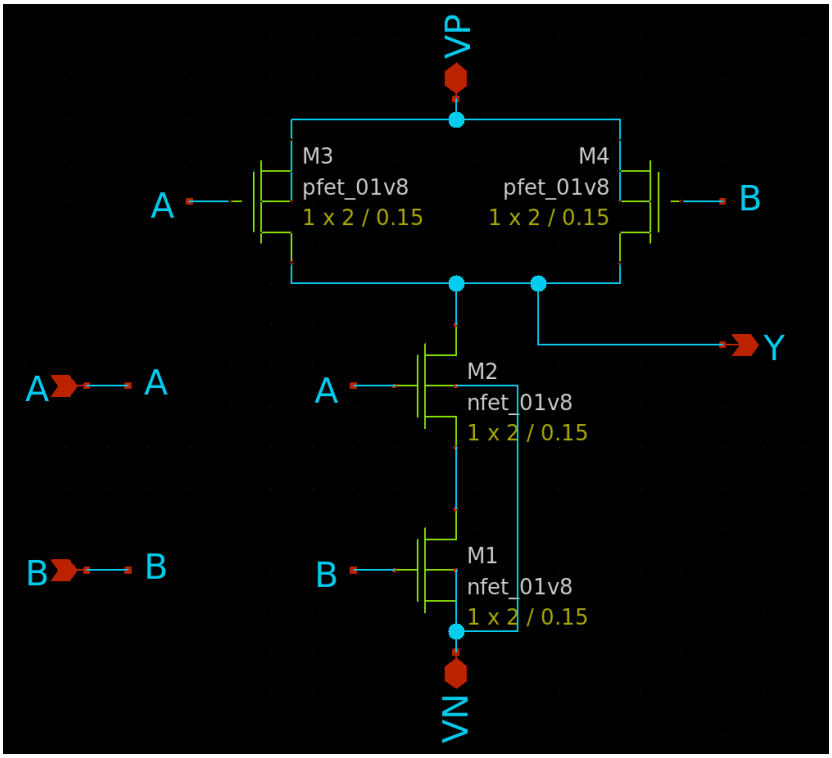

Figure 2: Nand gate schematic.

I created symbols for the schematics and created a hierarchical schematic for the and gate, which consists of a nand gate and an inverter in series, as shown in Figure 3.

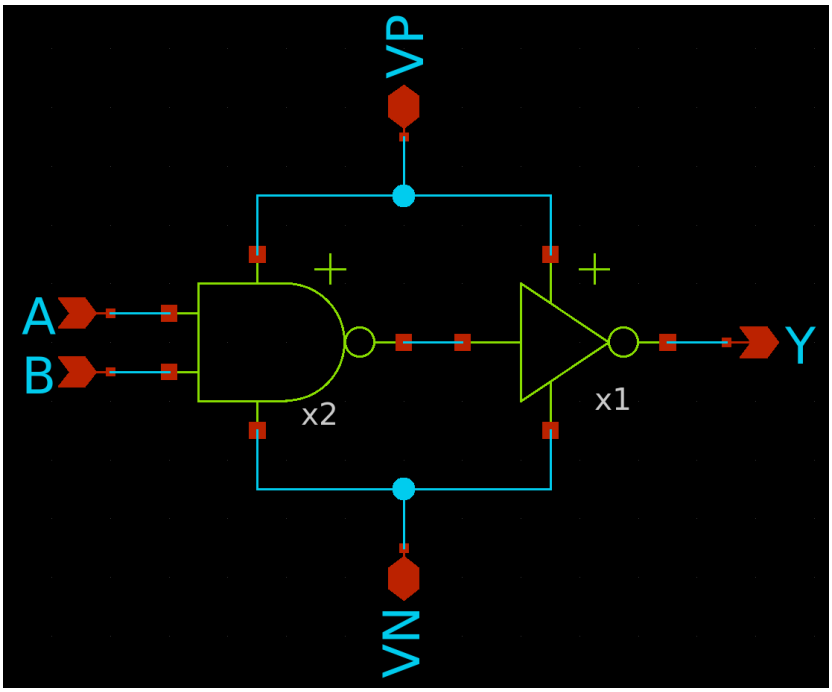

Figure 3: Hierarchical and gate schematic.

Finally, I connected my and gate up to the simulation circuit shown in Figure 4. The output of the and gate is loaded with a $200fF$ capacitor. The inputs are supplied with two voltage sources which

follow a square wave offset by 90 degrees from each other. Therefore, the inputs to the and gate go through all four states ('00', '01', '10', and '11') for about $4ns$ each.

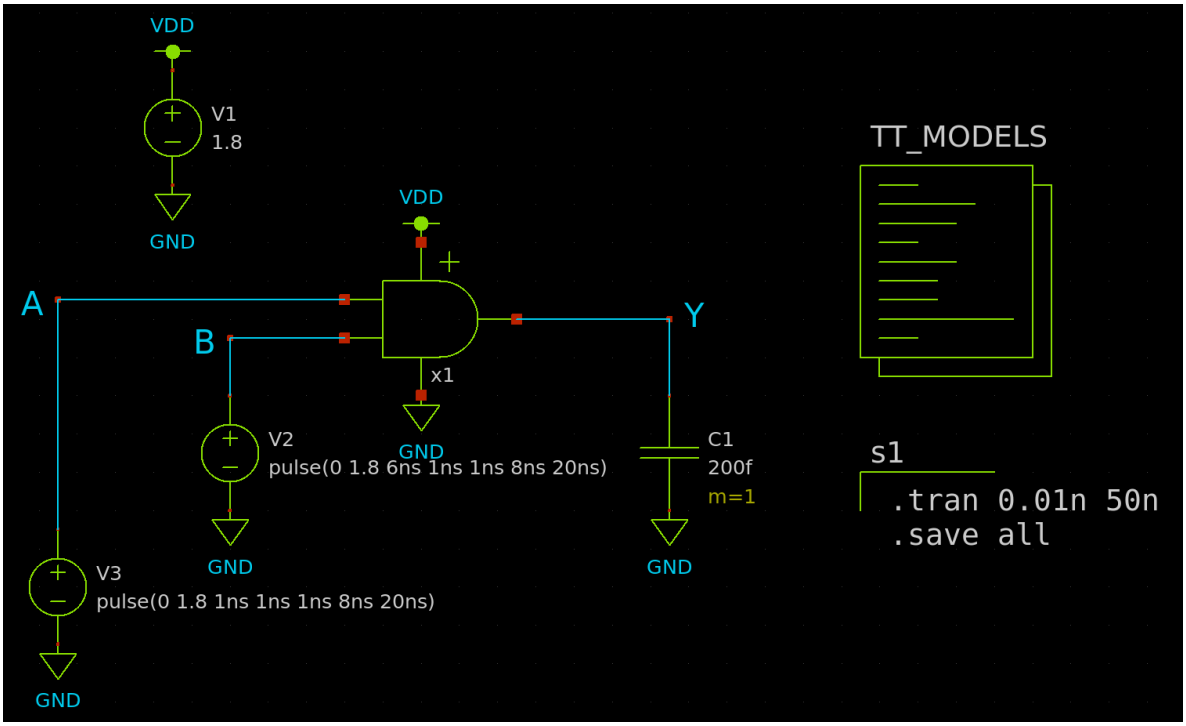

Figure 4: And gate testing setup with a 200fF output capacitor.

The results are shown in Figure 5, and a zoomed in version is shown in Figure 6. As expected, the output Y is only high when the inputs A and B exceed a threshold of around half of V_{DD}. The slew rate of the and gate is faster than that of the voltage sources. The zoomed in figure shows that the output starts to rise when both inputs are above $1.0V$ and begins to fall when both inputs are below $0.6V$.

The output exponentially approaches the expected value, with a time constant roughly double on the rising edge ($\tau \approx 1ns$) than on the falling edge ($\tau \approx 0.5ns$). The time constant is mainly driven by the characteristics of the inverter transistors. I believe the difference in time constant is due to the value for hole mobility used by NGspice. I designed using the ratio $\mu_{electrons} \approx 2 \cdot \mu_{holes}$, but it seems that NGspice estimate is $\mu_{electrons} \approx 4 \cdot \mu_{holes}$. When I tried making the width of the PMOS transistors four microns instead of two, then the time constants on the rising and falling edges matched much more closely. For the layout, I used a width of 2 microns for the PMOS transistors.

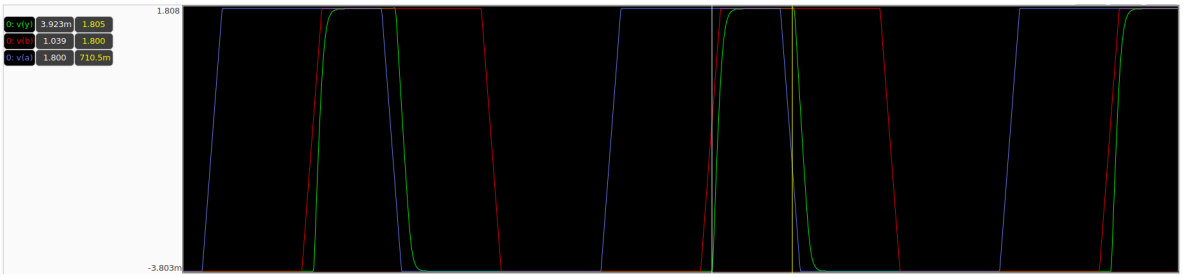

Figure 5: Results of simulation with a 200fF output capacitor (shown over a $50ns$ domain).

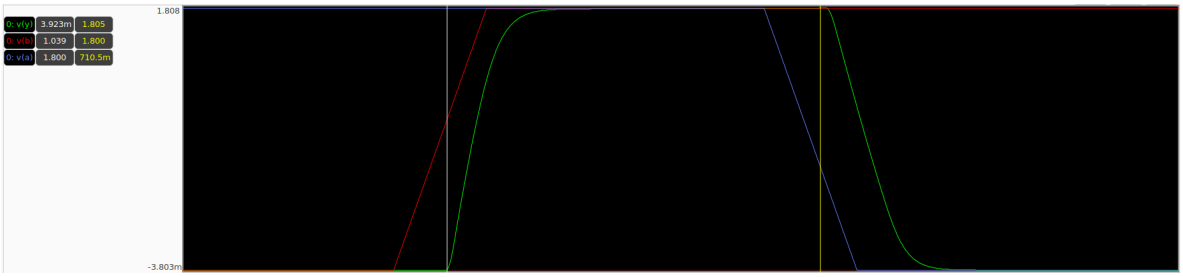

Figure 6: Results of simulation with a 200fF output capacitor (shown over a $10ns$ domain).

2 Magic Layout

My magic layout is shown in Figures 7 and 8. The inputs to the nand gate are on the lower left hand side, and the output of the inverter is on the right. To accommodate the wider NMOS transistors, the nand gate is taller than the inverter. The positive rail runs continuously across the top of the cell, and the negative rail is narrower over the inverter section because the NMOS transistor is narrower. This necessitated a circuitious signal connection between the nand gate output and the inverter input.

When connecting the cells together, I had to leave 150nm of space between them to avoid design rule violations due to the local interconnect of the inverter input (which abuts the left hand side of its cell) being too close to the p-substrate diffusion contact (which nearly abuts the right hand side of the nand gate). If I had designed the nand and inverter together instead of as separate cells, I could have made use of the side-by-side n-substrate diffusion regions and side-by-side p-substrate diffusion regions at the boundary between the nand gate and the inverter. However, since I designed the two cells independently for general use, I cannot take advantage of this potential optimization. I specifically chose for the inverter's input to abut the side of its cell to facilitate placing multiple of them in series to make a buffer, even though this might mean inefficient integration between different types of cells.

The final area of my and gate is $5.4\mu m$ by $5.7\mu m$. This means you could fit 30,000 of my and gates on a square millimeter of silicon (not accounting for interconnects between cells).

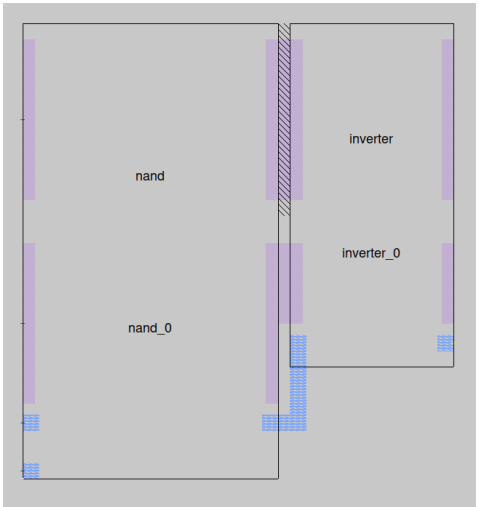

Figure 7: Magic layout showing how the nand and inverter cells interact.

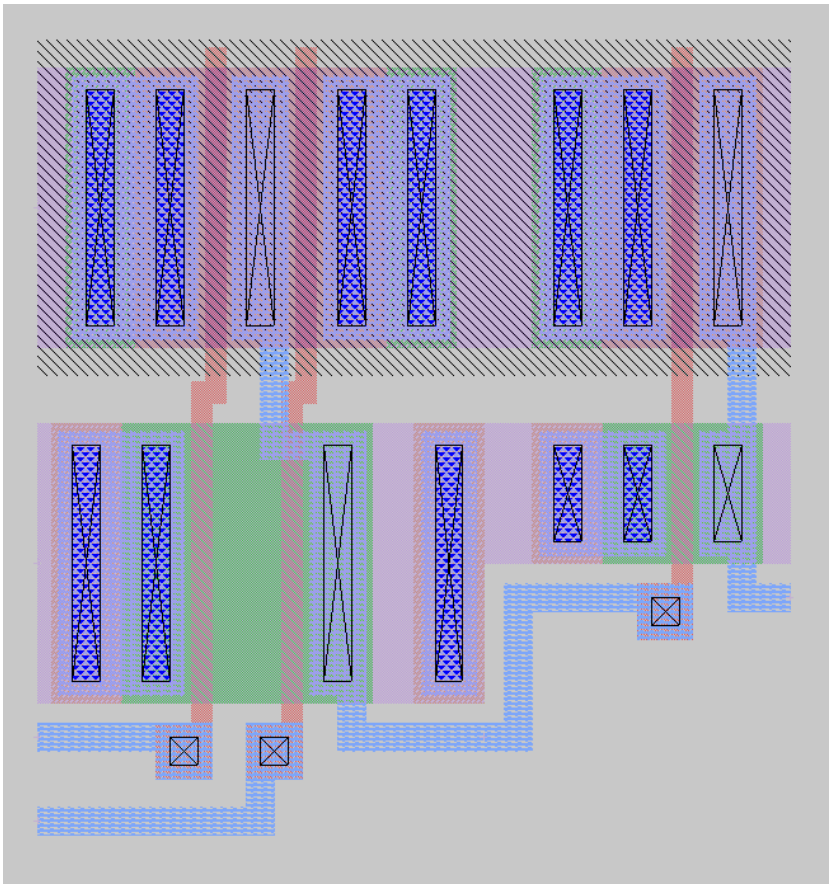

Figure 8: Magic layout showing the complete and gate. The total area is 5.4 by 5.7 microns.

3 Netgen LVS

The circuits match uniquely between the Xschem schematic and the Magic layout. See the contents of the 'comp.log' file from Netgen below.

```
Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.

Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.

Subcircuit summary:
Circuit 1: nand                            |Circuit 2: nand
-------------------------------------------|-------------------------------------------
sky130_fd_pr__nfet_01v8 (2)                |sky130_fd_pr__nfet_01v8 (2)
sky130_fd_pr__pfet_01v8 (2)                |sky130_fd_pr__pfet_01v8 (2)
Number of devices: 4                       |Number of devices: 4
Number of nets: 6                          |Number of nets: 6
-----------------------------------------------------------------------------------------
Netlists match uniquely with property errors.
sky130_fd_pr__pfet_01v8:M4 vs. sky130_fd_pr__pfet_01v8:1:
 W circuit1: 1   circuit2: 2   (delta=66.7%, cutoff=1%)
sky130_fd_pr__pfet_01v8:M3 vs. sky130_fd_pr__pfet_01v8:3:
```

```
 W circuit1: 1   circuit2: 2   (delta=66.7%, cutoff=1%)
sky130_fd_pr__nfet_01v8:M2 vs. sky130_fd_pr__nfet_01v8:0:
 W circuit1: 1   circuit2: 2   (delta=66.7%, cutoff=1%)
sky130_fd_pr__nfet_01v8:M1 vs. sky130_fd_pr__nfet_01v8:2:
 W circuit1: 1   circuit2: 2   (delta=66.7%, cutoff=1%)

Subcircuit pins:
Circuit 1: nand                          |Circuit 2: nand
-----------------------------------------|-----------------------------------------
VP                                       |VP
Y                                        |Y
VN                                       |VN
A                                        |B **Mismatch**
B                                        |A **Mismatch**
-------------------------------------------------------------------------------------
Cell pin lists for nand and nand altered to match.
Device classes nand and nand are equivalent.

Subcircuit summary:
Circuit 1: inverter                      |Circuit 2: inverter
-----------------------------------------|-----------------------------------------
sky130_fd_pr__nfet_01v8 (1)              |sky130_fd_pr__nfet_01v8 (1)
sky130_fd_pr__pfet_01v8 (1)              |sky130_fd_pr__pfet_01v8 (1)
Number of devices: 2                     |Number of devices: 2
Number of nets: 4                        |Number of nets: 4
-------------------------------------------------------------------------------------
Netlists match uniquely with property errors.
sky130_fd_pr__pfet_01v8:M2 vs. sky130_fd_pr__pfet_01v8:0:
 W circuit1: 1   circuit2: 2   (delta=66.7%, cutoff=1%)

Subcircuit pins:
Circuit 1: inverter                      |Circuit 2: inverter
-----------------------------------------|-----------------------------------------
Y                                        |Y
A                                        |a_n50_n110# **Mismatch**
VP                                       |w_n240_270# **Mismatch**
VN                                       |a_n200_0# **Mismatch**
-------------------------------------------------------------------------------------
Cell pin lists for inverter and inverter altered to match.
Device classes inverter and inverter are equivalent.

Subcircuit summary:
Circuit 1: and_xschem.spice              |Circuit 2: and.spice
-----------------------------------------|-----------------------------------------
nand (1)                                 |nand (1)
inverter (1)                             |inverter (1)
Number of devices: 2                     |Number of devices: 2
Number of nets: 6                        |Number of nets: 6
-------------------------------------------------------------------------------------
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes and_xschem.spice and and.spice are equivalent.

Final result: Circuits match uniquely.
.
```

```
The following cells had property errors:
 nand
 inverter
```