BIFURCATIONS AND SYNCHRONIZATION USING AN INTEGRATED PROGRAMMABLE CHAOTIC CIRCUIT

M. DELGADO-RESTITUTO, M. LIÑÁN, J. CEBALLOS and A. RODRÍGUEZ-VÁZQUEZ

Centro Nacional de Microelectrónica (CNM)
Ed. CICA, Avda. Reina Mercedes s/n
41012 - Seville, SPAIN.

This paper presents a CMOS chip which can act as an autonomous stand-alone unit to generate different real-time chaotic behaviors by changing a few external bias currents. In particular, by changing one of these bias currents, the chip provides different examples of a period-doubling route to chaos. We present experimental orbits and attractors, time waveforms and power spectra measured from the chip. By using two chip units, experiments on synchronization can be carried out as well in real-time. Measurements are presented for the following synchronization schemes: linear coupling, drive-response and inverse system. Experimental statistical characterizations associated to these schemes are also presented. We also outline the possible use of the chip for chaotic encryption of audio signals. Finally, for completeness, the paper includes also a brief description of the chip design procedure and its internal circuitry.

Running Title:

A Chip for Real-Time Generation of Chaotic Behaviors

Contact Author:

Angel Rodríguez-Vázquez

Centro Nacional de Microelectrónica (CNM)
Ed. CICA, Avda. Reina Mercedes s/n
41012 Sevilla, SPAIN
Phone: +34 5 423 99 23 Fax: +34 5 423 18 32 E-Mail: angel@cnm.us.es

BIFURCATIONS AND SYNCHRONIZATION USING AN INTEGRATED PROGRAMMABLE CHAOTIC CIRCUIT

M. DELGADO-RESTITUTO, M. LIÑÁN, J. CEBALLOS and A. RODRÍGUEZ-VÁZQUEZ

Centro Nacional de Microelectrónica (CNM)
Ed. CICA, Avda. Reina Mercedes s/n
41012 - Seville, SPAIN.

This paper presents a CMOS chip which can act as an autonomous stand-alone unit to generate different real-time chaotic behaviors by changing a few external bias currents. In particular, by changing one of these bias currents, the chip provides different examples of a period-doubling route to chaos. We present experimental orbits and attractors, time waveforms and power spectra measured from the chip. By using two chip units, experiments on synchronization can be carried out as well in real-time. Measurements are presented for the following synchronization schemes: linear coupling, drive-response and inverse system. Experimental statistical characterizations associated to these schemes are also presented. We also outline the possible use of the chip for chaotic encryption of audio signals. Finally, for completeness, the paper includes also a brief description of the chip design procedure and its internal circuitry.

1. Introduction

Chaos in electrical circuits has drawn strong attention during the last decade [Chua, 1987; Chua & Hasler, 1993]. This topic is of evident theoretical interest since circuits provide very simple vehicles for the experimental observation of chaotic phenomena (instead of only through computer simulation). Chaos is also of practical engineering interest. For instance, the inherent unpredictability of deterministic chaos has been used to design improved white and colored noise generators [McGonigal & Elmasry,1987; Rodríguez-Vázquez *et al.*, 1991; Murch & Bates, 1990; Delgado-Restituto *et al.*, 1992], as well as for the generation of secure random number time-series [Bernstein & Lieberman, 1990; Rodríguez-Vázquez *et al.*, 1991]. The random-like appearance of chaos has also proven

useful to improve the noise performance of switched-capacitor ΣΔ modulators, making these circuits operate in chaotic regimes [Schreier, 1991; Hein, 1993]. Chaotic circuits also exhibit potential applications in nonlinear signal processing and neural computation. On one hand, the possibility of two or more chaotic systems oscillating in a coherent, synchronized way can be exploited for signal encryption and secure communications [Carroll & Pecora, 1991; Oppenheim *et al.*, 1992; Kocarev *et al.*, 1992]. On the other, the fact that chaos has been identified to be behind the sensory information processing performed by natural nervous systems [Matsumoto *et al.*, 1987; Freeman, 1992], motivates looking for artificial neural network paradigms based upon chaotic neurons, in an attempt to better emulate living beings [Aihara *et al.*, 1990, Nozawa, 1992].

In today's electronic systems, economic reasons dictate the convenience of having all component parts integrated on common silicon substrates, instead of breadboarded using off-the-shelf components. In this scenario, and before the potentials of chaotic circuits can be exploited into future marketable instrumentation, communication, or computing systems, it must be demonstrated that chaos can be generated in a controllable and robust form using monolithic circuits, preferably in *standard* VLSI technologies.

Up to date, only few of the previously reported chaotic circuits have been realized as monolithic[†1] integrated circuits. In 1987 [Rodríguez-Vázquez *et al.*, 1987], the authors started a research line in this direction which has resulted in a number of CMOS chips. Some of them are described by *finite-difference* equations (FDE's), while others are described by *ordinary differential* equations (ODE's). In 1991 a programmable integrated noise source was presented based on the Bernoulli shift [Rodríguez-Vázquez *et al.*, 1991]. It uses *switched-capacitor* techniques, the same as in the flicker noise generator presented in 1992 [Delgado-Restituto *et al.*, 1992]. In 1993, an integrated circuit for white noise generation was presented [Delgado-Restituto *et al.*, 1993] which uses nonlinear *switched-current* techniques [Rodríguez-Vázquez & Delgado-Restituto, 1994]. Although all these ICs are simple and robust, their sampled-data nature restricts the maximum frequency attainable. In 1993 an integrated chaotic generator was presented which overcomes this problem through the use of continuous-time circuitry to realize ODE's [Rodríguez-Vázquez & Delgado-Restituto, 1993]. Other working[†2] ICs intended to be used as parts (together with off-chip components) of chaotic electronic systems are found in [Cruz & Chua, 1993], [Delgado-Restituto & Rodríguez-Vázquez, 1994] and [Horio & Suyama, 1995]. However, they are basically intended to be used as modules of larger breadboarded chaotic circuits.

1. By monolithic we mean all the needed components are fabricated on the same silicon substrate.
2. Chips demonstrated only through simulation results are not included.

The chip presented here is an updated version of that in [Rodríguez-Vázquez & Delgado-Restituto, 1993]. The original one was basically aimed to prove the possibility to build an ODE-based chaotic generator in a fully monolithic manner. Although this goal was achieved, the circuit suffered from the problems of such demonstration IC units: rather tricky controllability and difficult to use by others except the designers. The new chip overcomes these problems. It is easy to use and control, and its robustness has been significantly enhanced through system-level and circuit-level optimization. It has been fabricated in a 2.4μm double-poly double-metal CMOS technology, and occupies 5mm^2 with a power consumption of 1.8mW for a 5V voltage supply. A remarkable feature of the new prototype is its versatility for the observation of bifurcation and synchronization phenomena by just controlling a few external bias currents.

The outline of the paper is as follows. Section 2 introduces the state equations of the oscillator, details the output pins description of the chip as well as their electrical characteristics, and identifies which terminals serve as programming variables of the dynamic behavior. Sections 3 and 4 are tailored to illustrate the performance of the prototype through experimental measurements of bifurcation and synchronization phenomena, respectively. Finally, Sec. 5 gives a theoretical basis for the functional description introduced in Sec. 2 and presents the internal block diagram of the chaotic oscillator, ignoring as much as possible microelectronic-related details.

2. Chip Terminals and Interconnections

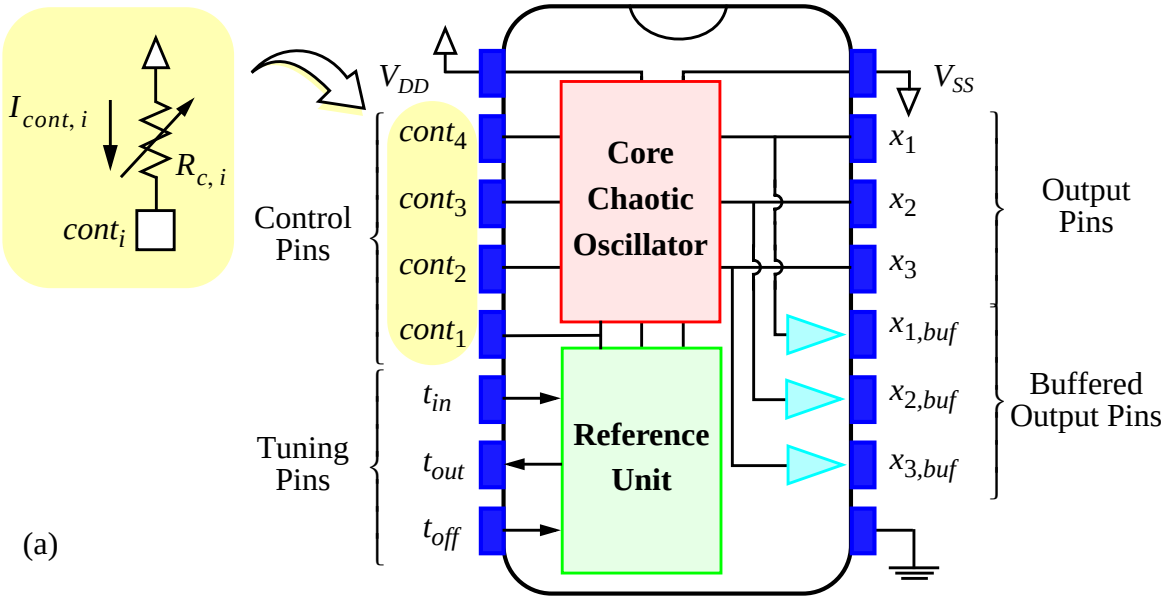
Fig.1(a) shows the pin connections and internal structure of the integrated chaotic generator and Fig.1(b) shows the experimental setup. The chip architecture comprises a *core chaotic oscillator* and some auxiliary circuitry (three voltage *buffers* and a time constant *reference unit*) to increase the versatility of the prototype. The chip has 16 external pins.

The most important block in the architecture of Fig.1 is the core chaotic oscillator. It implements a third order autonomous continuous-time system, which includes an odd-symmetric, three-region *piecewise-linear* (PWL) nonlinearity,

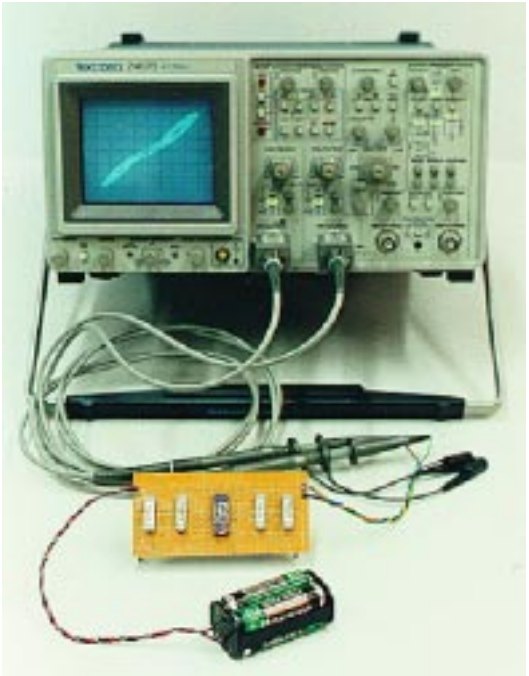
$$\tau\frac{dx_1}{dt} = h(x_1) + \alpha x_2 \qquad \tau\frac{dx_2}{dt} = \alpha(x_1 - x_3) - \gamma\, x_2 \qquad \tau\frac{dx_3}{dt} = \beta x_2 \tag{8}$$

where $h(\,)$ (see Fig.2) is given by,

$$h(x_1) = m_1 x_1 + \frac{m_0 - m_1}{2}\{|x_1 + B_p| - |x_1 - B_p|\} \tag{9}$$



(a)



(b)

Fig. 1. (a) Chip architecture; (b) Experimental setup showing oscilloscope, chip with four tuning resistors, and the battery pack.

The behavior is determined by seven parameters. Four of them, τ, m_0, m_1 and B_p, are externally programmable. The other three, α, β and γ, have fixed values.

The programmable parameters are controlled through the low impedance inputs $cont_1$, $cont_2$, $cont_3$ and $cont_4$. They have DC levels around –0.5V, and the controlling

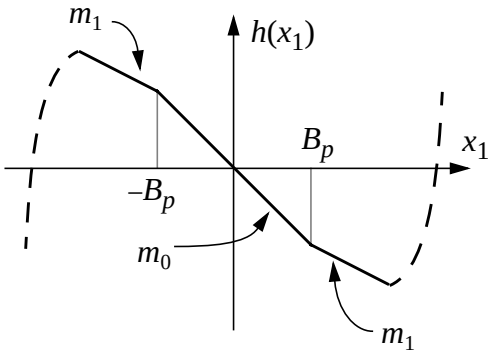


Fig. 2. Nonlinearity of the chaotic oscillator.

Characteristic	Symbol	Min	Typ	Max	Unit
Positive Power Supply Voltage	V_{DD}	2.0	3.0	5.0	Vdc
Negative Power Supply Voltage	V_{SS}	-2.0	-3.0	-5.0	Vdc
Tuning Parameter, τ ($V_{DD} = -V_{SS} = 3.0$ V)	I_{cont1}	1.0	1.5	5.0	μA
Bifurcation Parameter, m_0 ($V_{DD} = -V_{SS} = 3.0$ V)	I_{cont2}	0.0	1.5	10.5	μA
Bifurcation Parameter, m_1 ($V_{DD} = -V_{SS} = 3.0$ V)	I_{cont3}	1.0	2.5	4.5	μA
Amplitude Parameter, B_p ($V_{DD} = -V_{SS} = 3.0$ V)	I_{cont4}	0.2	0.3	0.7	μA

Table I: Electrical characteristics (typical conditions are for reproducing the Chua's double-scroll attractor)**.**

variables are the currents entering the terminals. Because of the low-impedance feature, each current can be generated using a simple resistance (see inset of Fig.1). I_{cont1} sets the time constant τ of the chaotic oscillator ($\tau \sim (I_{cont1})^{-1/2}$) which thus can vary approximately between $12\mu s$ and $60\mu s$. I_{cont2} and I_{cont3} set respectively the central m_0 and outer m_1 slopes of the nonlinearity. Achievable ranges are between 0 and 5 for m_0, and between -1 and -3 for m_1. Finally, I_{cont4}, together with I_{cont1}, controls the breakpoints B_p of the nonlinearity ($B_p \sim I_{cont4}(I_{cont1})^{-1/2}$). Table I shows the electrical characteristics of

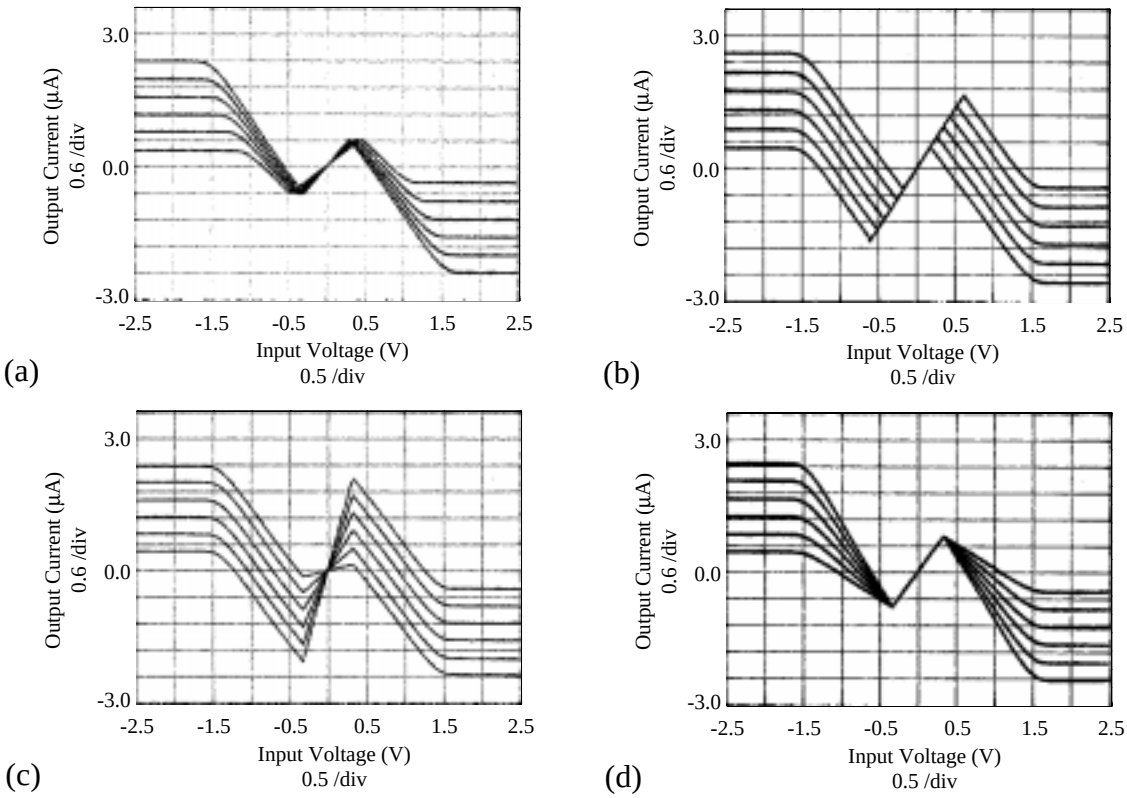


Fig. 3. Variation of the PWL characteristics of the nonlinearity with: (a) I_{cont1}; (b) I_{cont4}; (c) the central slope, m_0 (control variable I_{cont2}); and (d) the outer slopes, m_1 (control variable I_{cont3}).

the control pins at room temperature, as well as the range of biasing conditions of the chip, assuming that power supply is symmetrical with respect to ground ($V_{DD} = -V_{SS}$).

Fig.3 shows the variation of the realized nonlinear characteristic for different parameter configurations. They have been obtained by varying quasi-statically from rail to rail the voltage at pin x_1 of Fig.1, while fixing the output pins x_2 and x_3 to ground. Fig.3(a) illustrates the effect of changing the biasing current I_{cont1}, while keeping the rest of control variables constant ($I_{cont2} = 1.12\mu A$, $I_{cont3} = 2.7\mu A$ and $I_{cont4} = 0.3\mu A$). Note that as the τ value is increased by the effect of lowering I_{cont1}, the nonlinear characteristics suffers from a breakpoint displacement towards the power rails, which may preclude the existence of chaotic regime. This problem can be overridden by forcing a proper reduction on the current I_{cont4}. Fig.3(b) illustrates the effect of varying I_{cont4} while keeping the rest of control inputs fixed ($I_{cont1} = 1.4\mu A$ and the biasing currents I_{cont2} and I_{cont3} as before). Finally, Fig.3(c) and (d) show the variation of the nonlinear characteristic for different slopes m_0 and m_1 of the central and outer pieces, respectively. As previously stated, they can be externally controlled through biasing currents I_{cont2} and I_{cont3} applied to pins

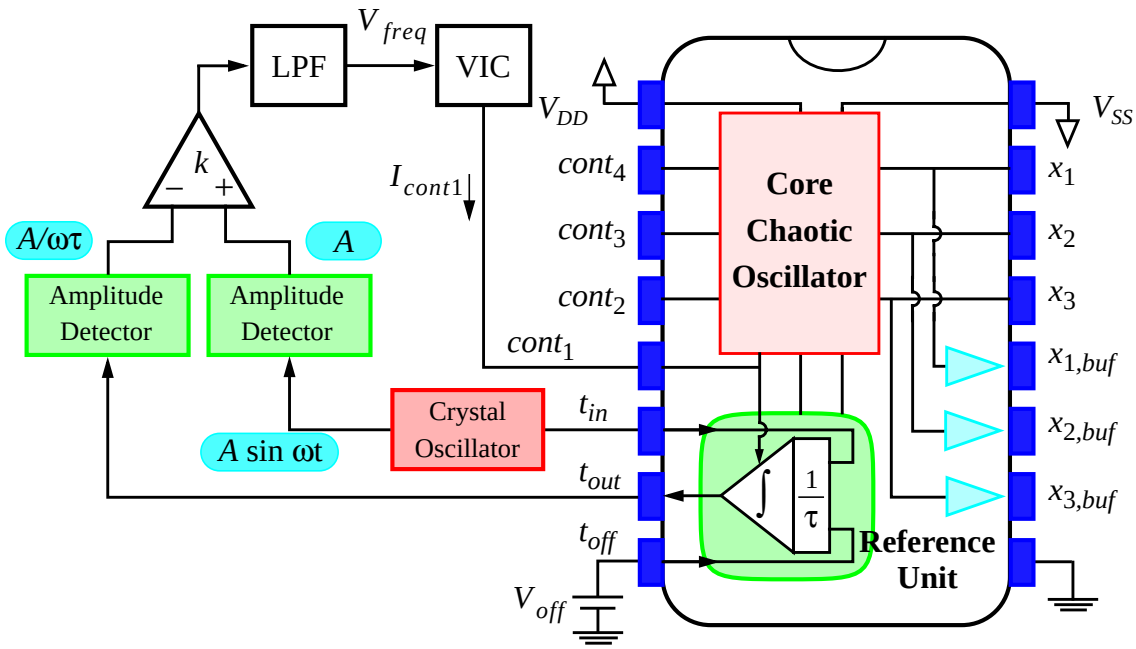


Fig. 4. Automatic Tuning Mechanism.

$cont_2$ and $cont_3$, respectively.

Output pins x_1, x_2 and x_3 are high impedance nodes which correspond to the state variables of the core chaotic oscillator. Since these state variables are voltages, and because of the high-impedance feature (about 1.5MΩ under usual operation conditions), significant loading errors may appear when measuring at these output terminals. These loading problems are alleviated by using the low-impedance buffered output pins $x_{1,\,buf}$, $x_{2,\,buf}$ and $x_{3,\,buf}$ (their output impedances are below 200Ω under usual operation conditions).

A time-constant reference unit has been also included (see Fig.1) to guarantee proper parameter matching among synchronizing chips. For synchronization to occur, it is necessary not only to have good relative parameter matching inside each chip (guaranteed by our adopted design strategies), but also good relative matching among the same parameter at different chip instances. This is difficult to achieve without tuning because of uncontrollable random fluctuations, as well as variations with temperature and aging. Due to this, designers have to face a scenario where parameters have around 20% errors -- intolerable to guarantee the asymptotic synchronization of the oscillators.

Fig.4 shows the block diagram of the automatic tuning circuitry. The on-chip reference unit simply consists of an integrator matched with those in the core chaotic oscillator. The time constant of this integrator (master system) is tuned to an accurately defined external reference frequency. If all the integrators included on-chip are simultaneously tuned, the

time constant of the oscillator (slave system) is related to the reference frequency as well. The accuracy of the tuning mechanism is determined by the matching of on-chip component values (absolute errors of about 1-2% can be obtained). Note that tuning is based on amplitude detection. Pins t_{in} and t_{out} in Fig.1 represent respectively the input and output nodes of the integrator. A voltage-mode crystal oscillator is applied to t_{in} and the changes in the output amplitude (measured at pin t_{out}) with the frequency of the reference signal, are detected and used to tune the system. The control signal V_{freq} generated by the system in closed loop is converted to a current and then applied to pin $cont_1$ so that the time constant of the circuit becomes locked to that of the external crystal oscillator. Proper operation of the proposed tuning mechanism relies on the integrator be offset-free. Otherwise, the output amplitude will change linearly with time regardless of the signal provided by the crystal oscillator. To avoid this situation, an offset correction terminal (pin t_{off} in Fig.1) is added to the scheme, so that any deviation can be externally compensated.

3. Experimental Bifurcations

Next, we present a picture book of bifurcation sequences, chaotic attractors and periodic windows which has been measured on the silicon prototype by changing the bias currents I_{cont2} and I_{cont3}. The other programmable parameters were set to $I_{cont1} = 1.4\mu A$ and $I_{cont4} = 0.3\mu A$. The book comprises Fig.5 through Fig.21. Among them, the first seven figures illustrate corresponding instances of a typical period-doubling route to chaos which have been obtained by only varying the biasing current I_{cont2} while fixing $I_{cont3} = 2.35\ \mu A$.

For each value of I_{cont2} and I_{cont3} (indicated in the associated figure captions) along the picture book we show the phase portraits of the attractor, the power spectrum of the voltage at pin x_1, and the time waveforms of the three state variables. In both the Lissajous figures and time waveforms, the representation scale for the x_1 state variable is set to $350mV/div$. Corresponding oscilloscope scales for the x_2 and x_3 variables are $200mV/div$ and $400mV/div$, respectively. The waveform temporal basis is $0.2ms/div$ for Figs.5-8, and $0.5ms/div$ for Figs.9-21. Finally, for the horizontal scale of the spectrum, the left side of the display is nearly DC, with $2kHz/div$, while the vertical scale is $10dB/div$.

The experimental results obtained from the prototype are in full accordance with measurements previously reported from discrete component realizations [Chua *et al.*, 1993].

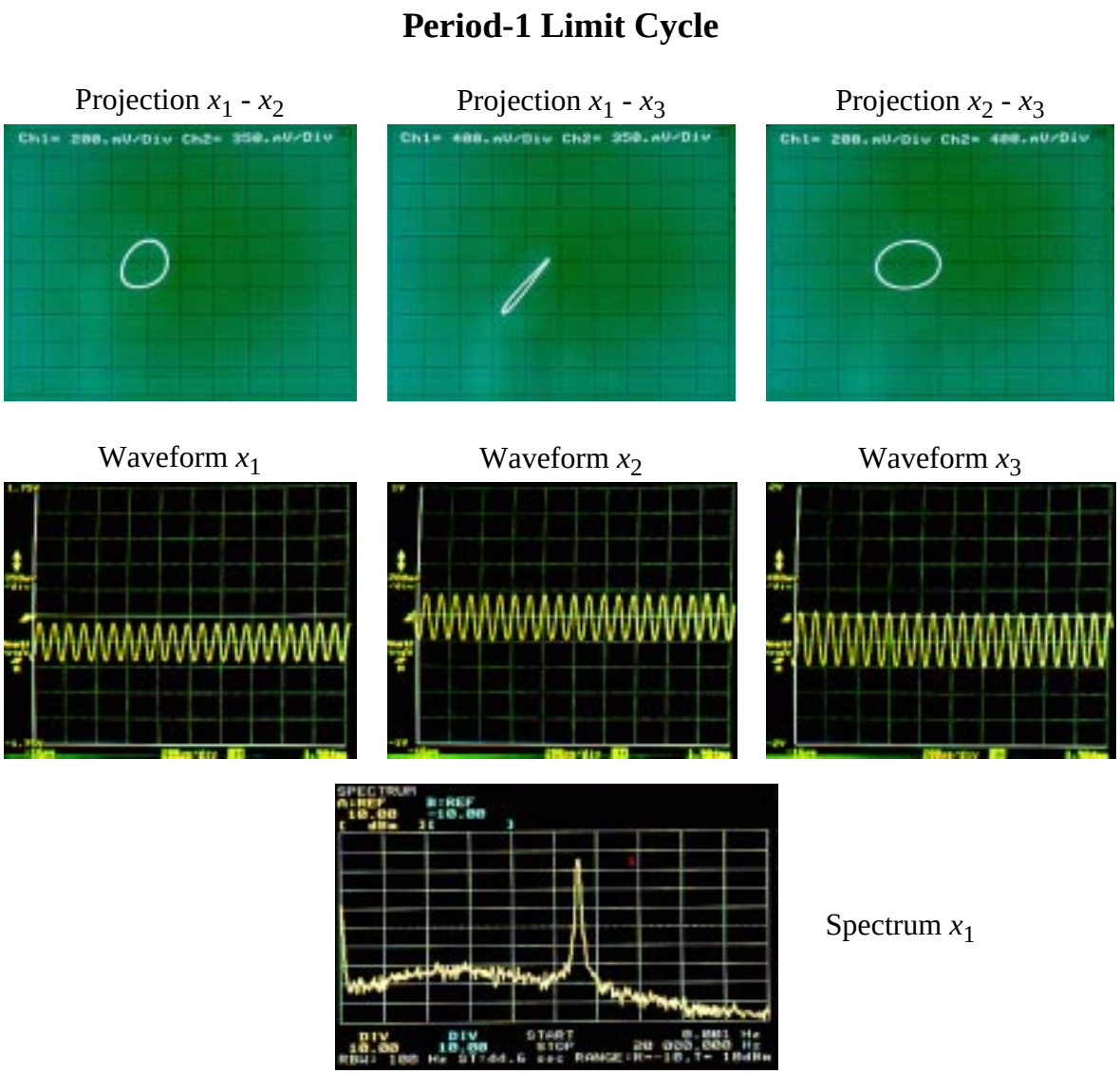


Fig. 5. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.0 μA, I_{cont3} = 2.35 μA.

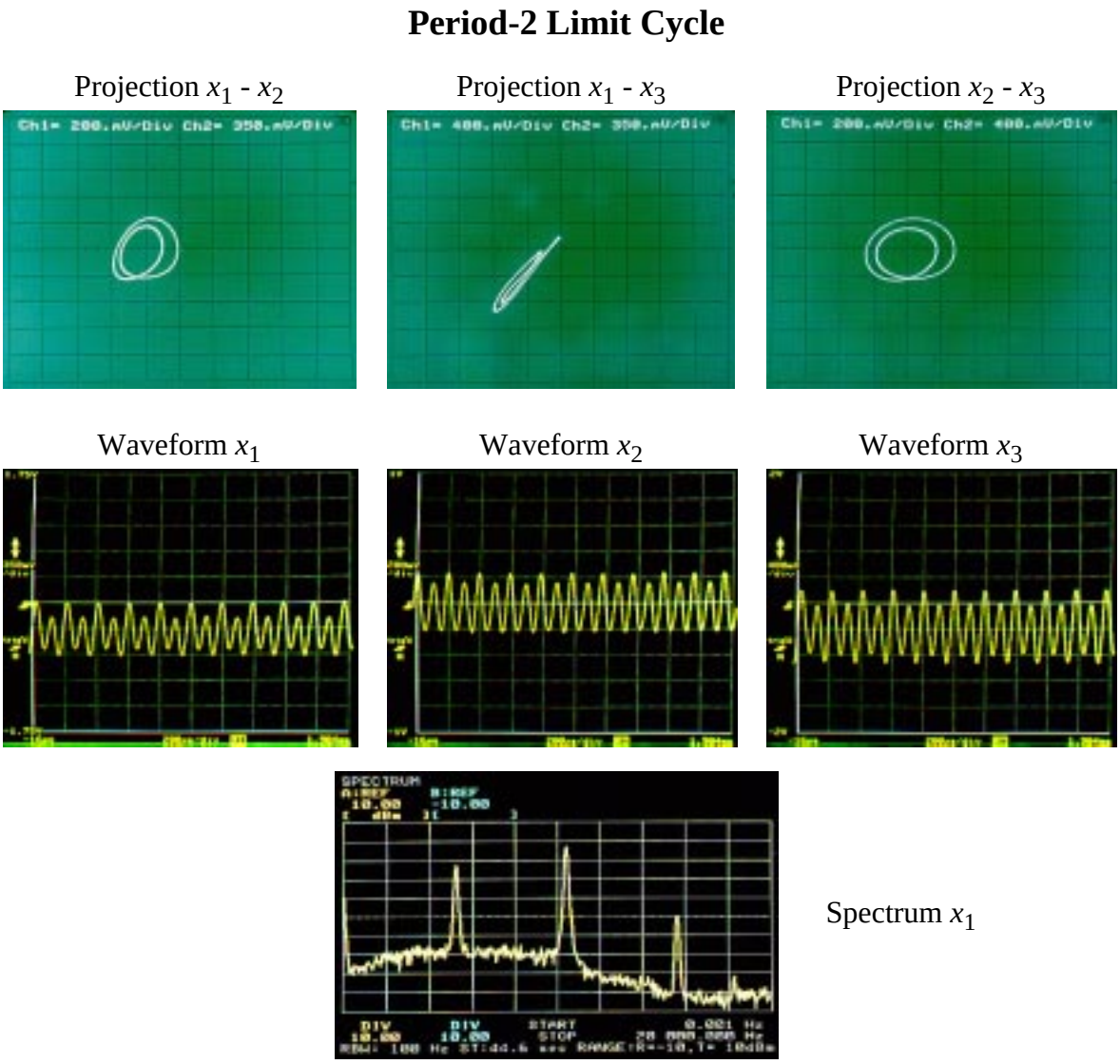


Fig. 6. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.04 μA, I_{cont3} = 2.35 μA.

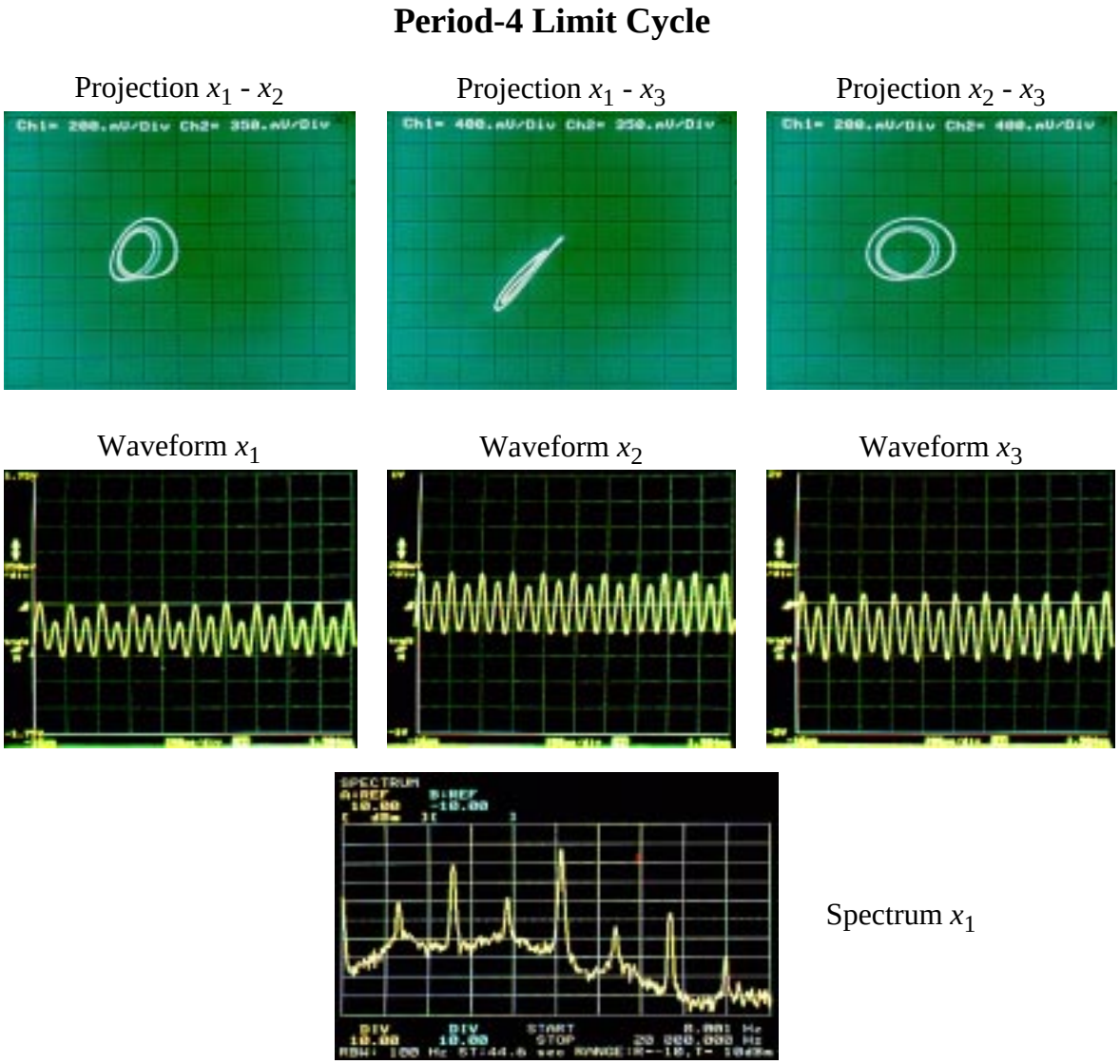


Fig. 7. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.065 μA, I_{cont3} = 2.35 μA.

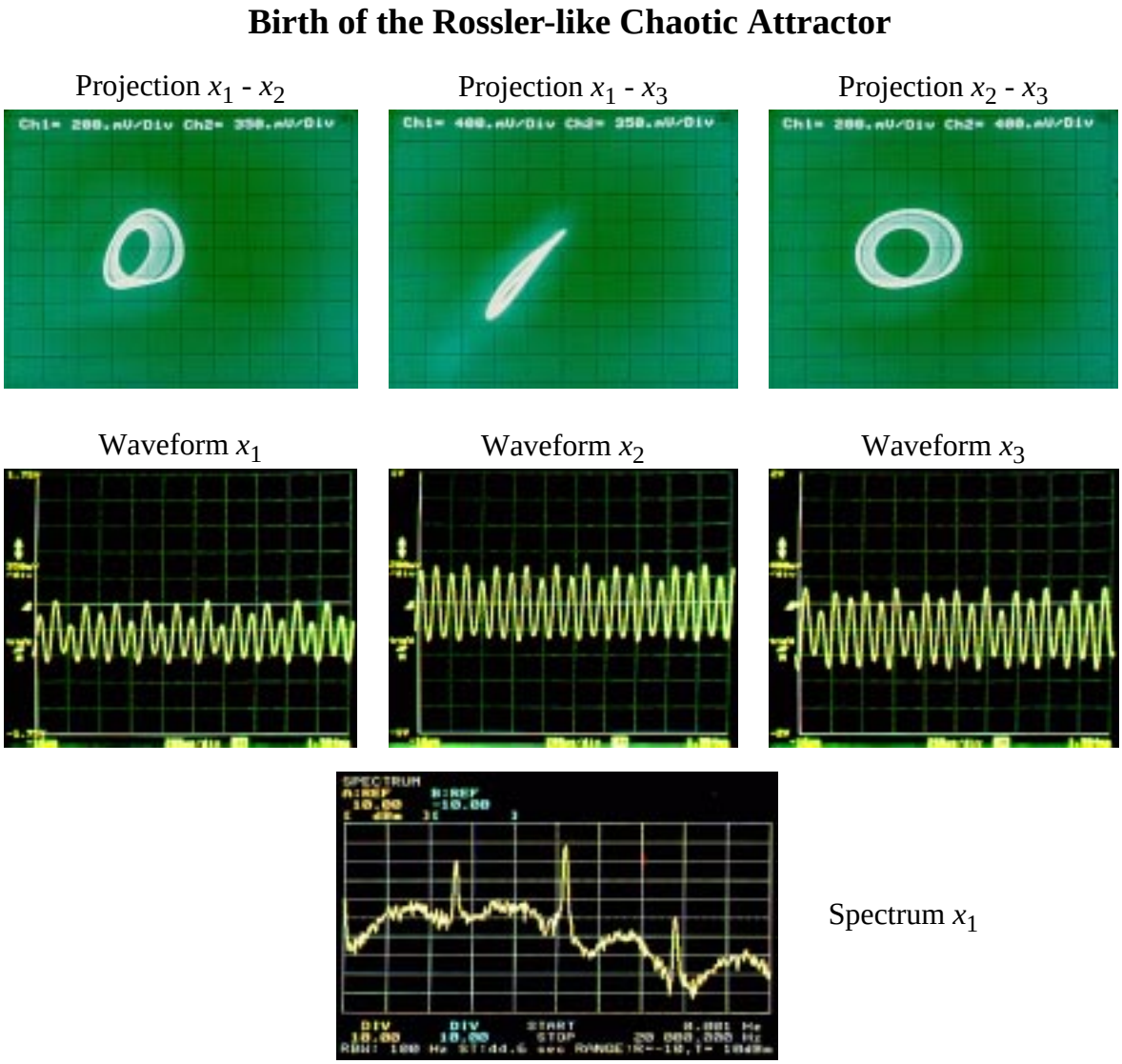


Fig. 8. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.07 μA, I_{cont3} = 2.35 μA.

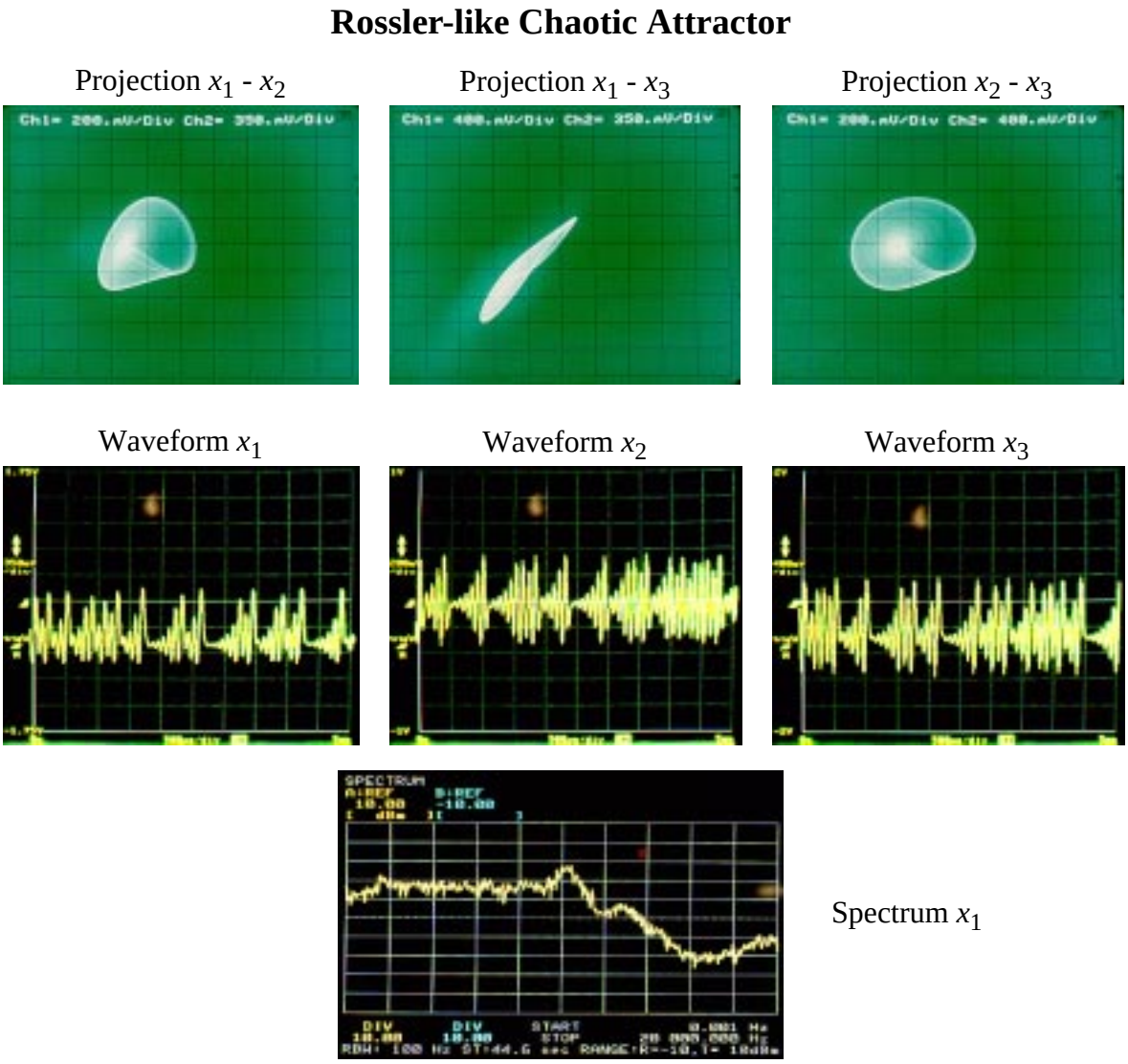


Fig. 9. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.12 μA, I_{cont3} = 2.35 μA.

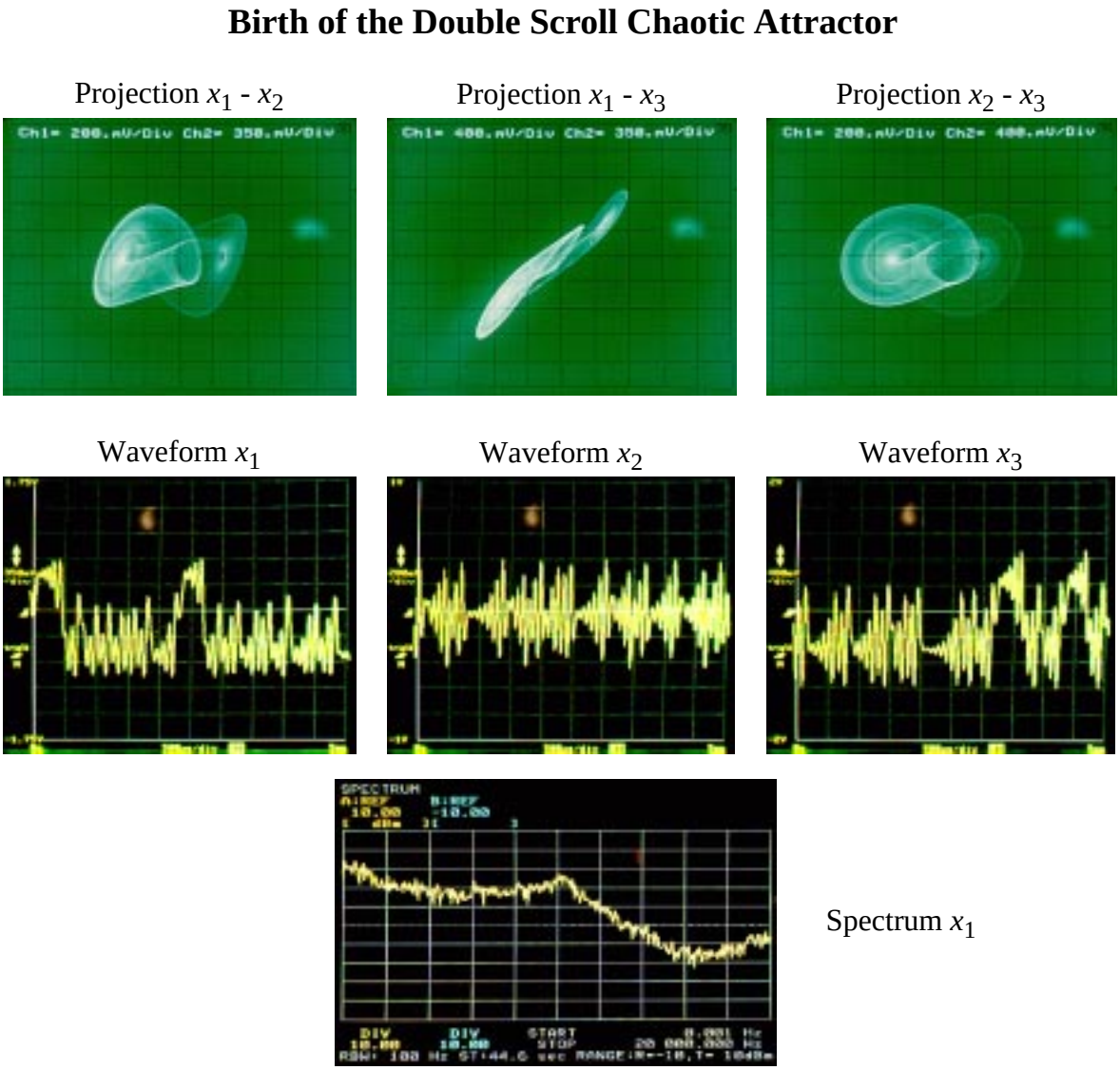
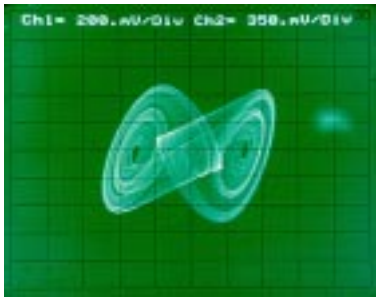


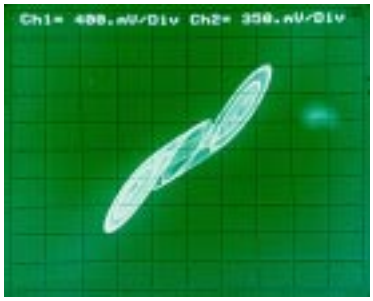
Fig. 10. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.135 μA, I_{cont3} = 2.35 μA.

Double Scroll Chaotic Attractor

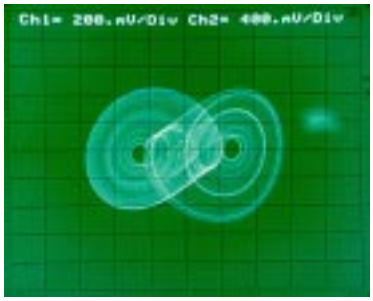
Projection x_1 - x_2



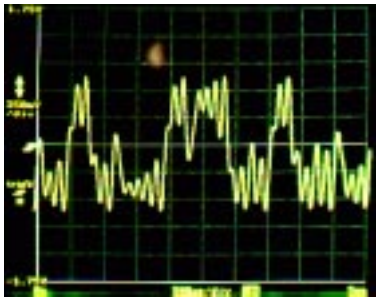
Projection x_1 - x_3



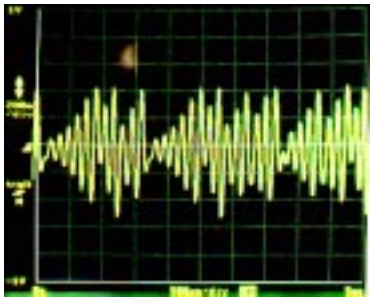
Projection x_2 - x_3



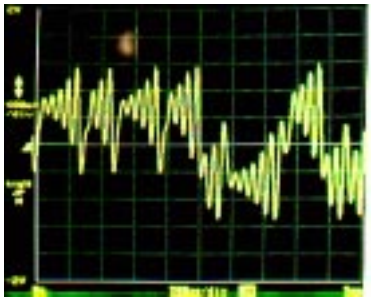
Waveform x_1

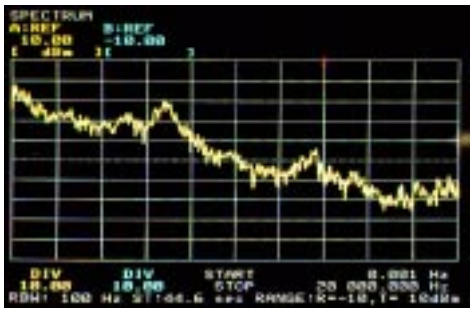


Waveform x_2



Waveform x_3





Spectrum x_1

Fig. 11. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.15 μA, I_{cont3} = 2.35 μA.

3-3 Periodic Window

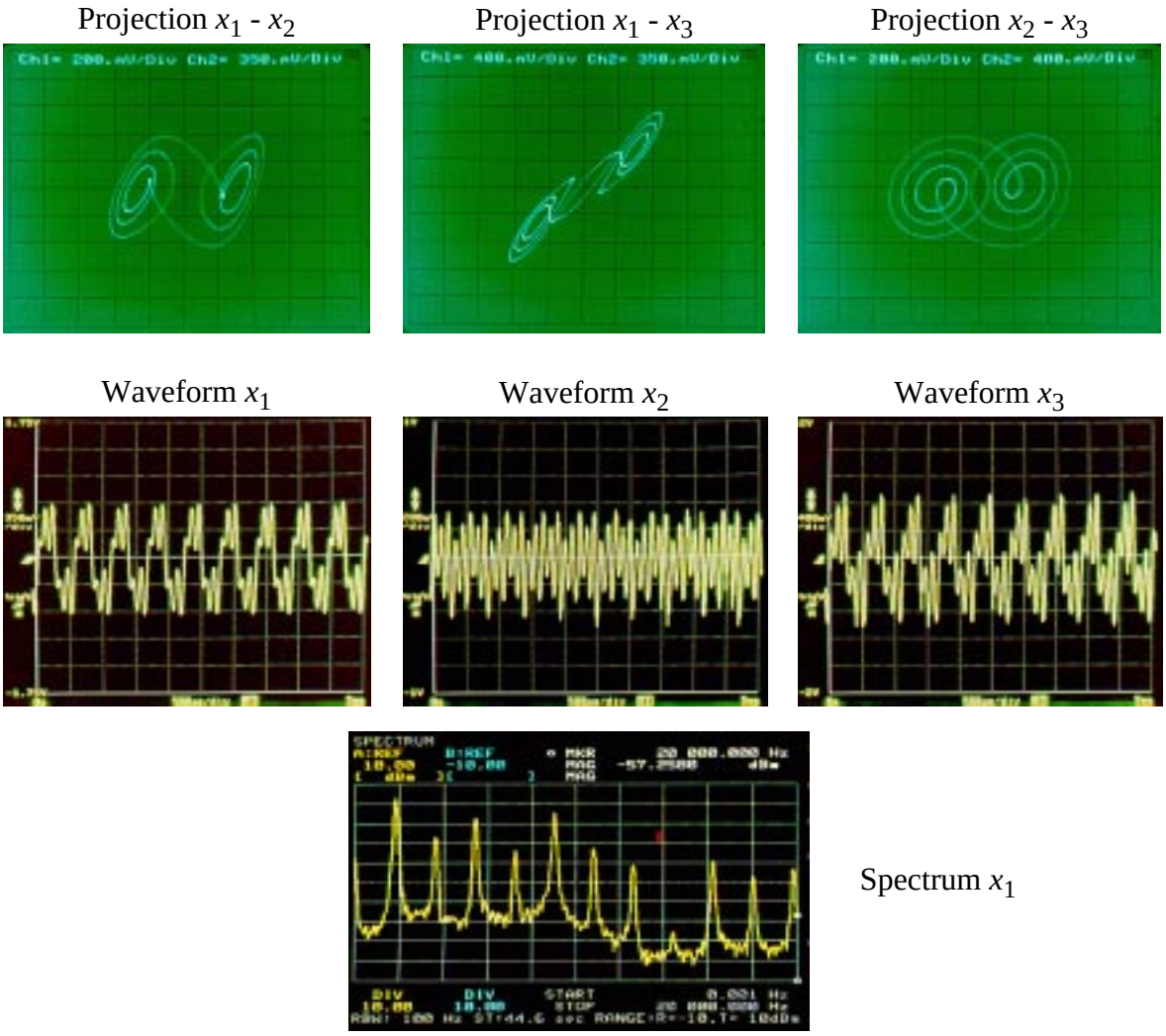


Fig. 12. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.24 μA, I_{cont3} = 2.47 μA.

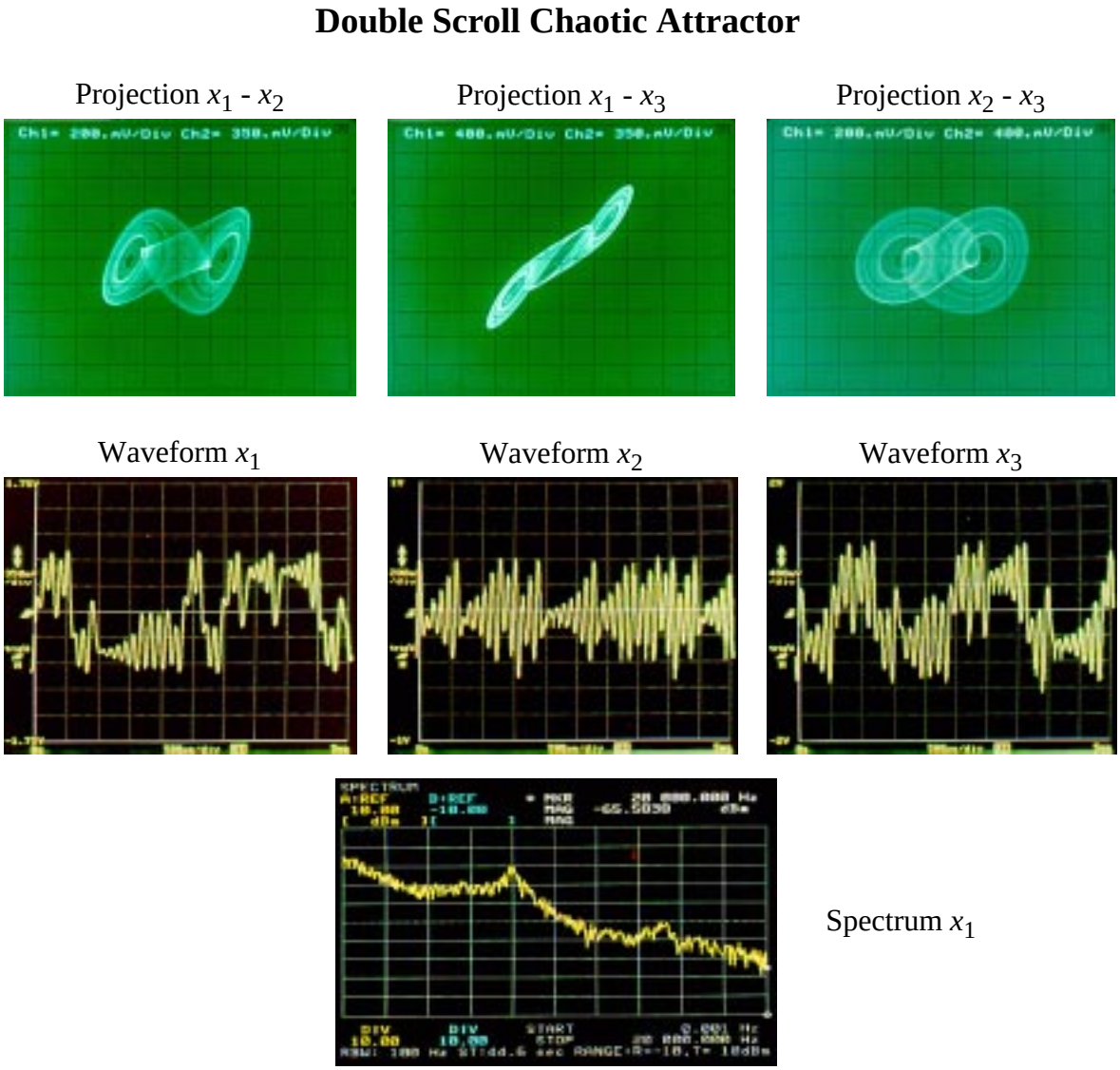


Fig. 13. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.47 μA, I_{cont3} = 2.56 μA.

4-4 Periodic Window

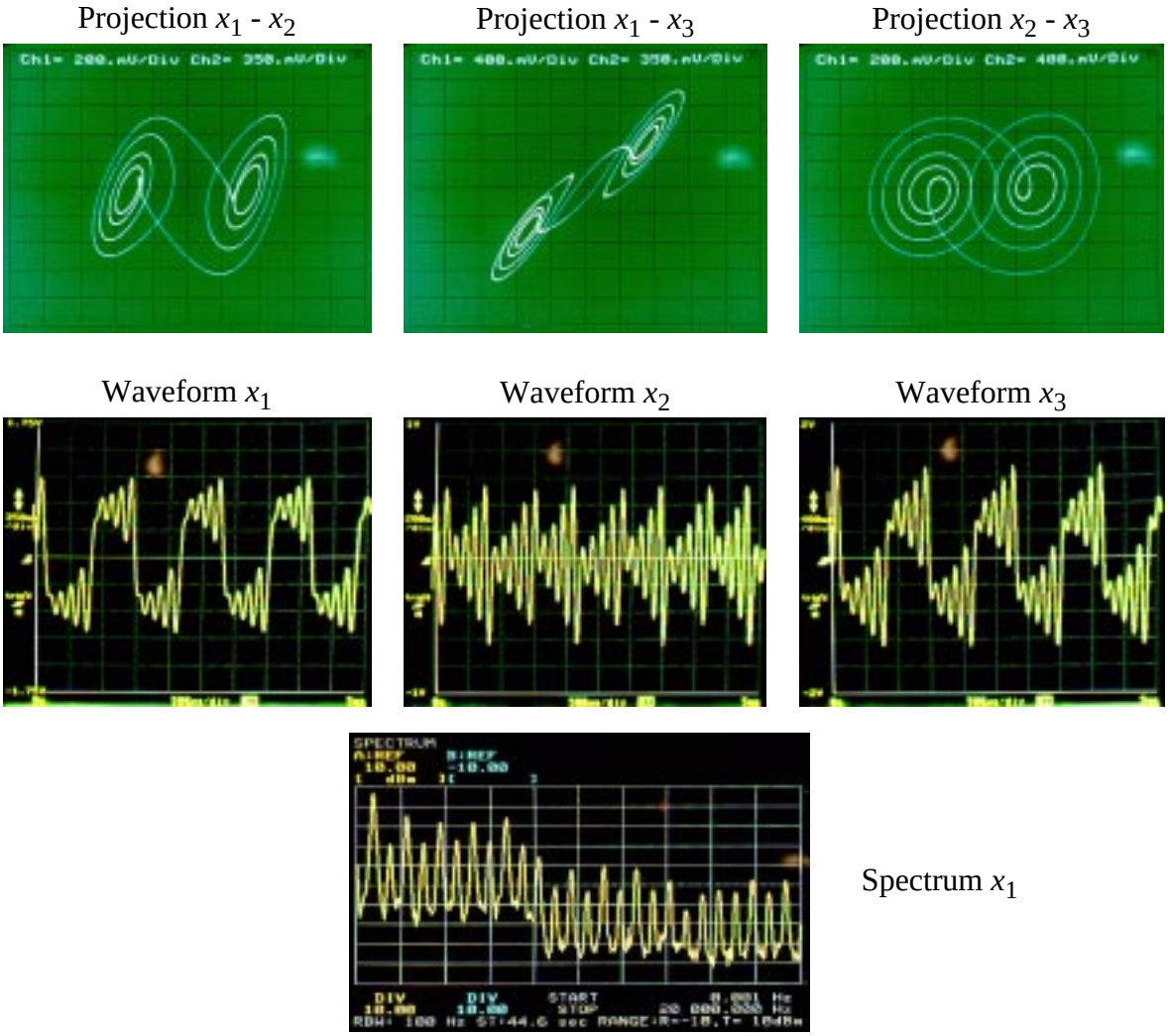


Fig. 14. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.62\ \mu A$, $I_{cont3} = 2.56\ \mu A$.

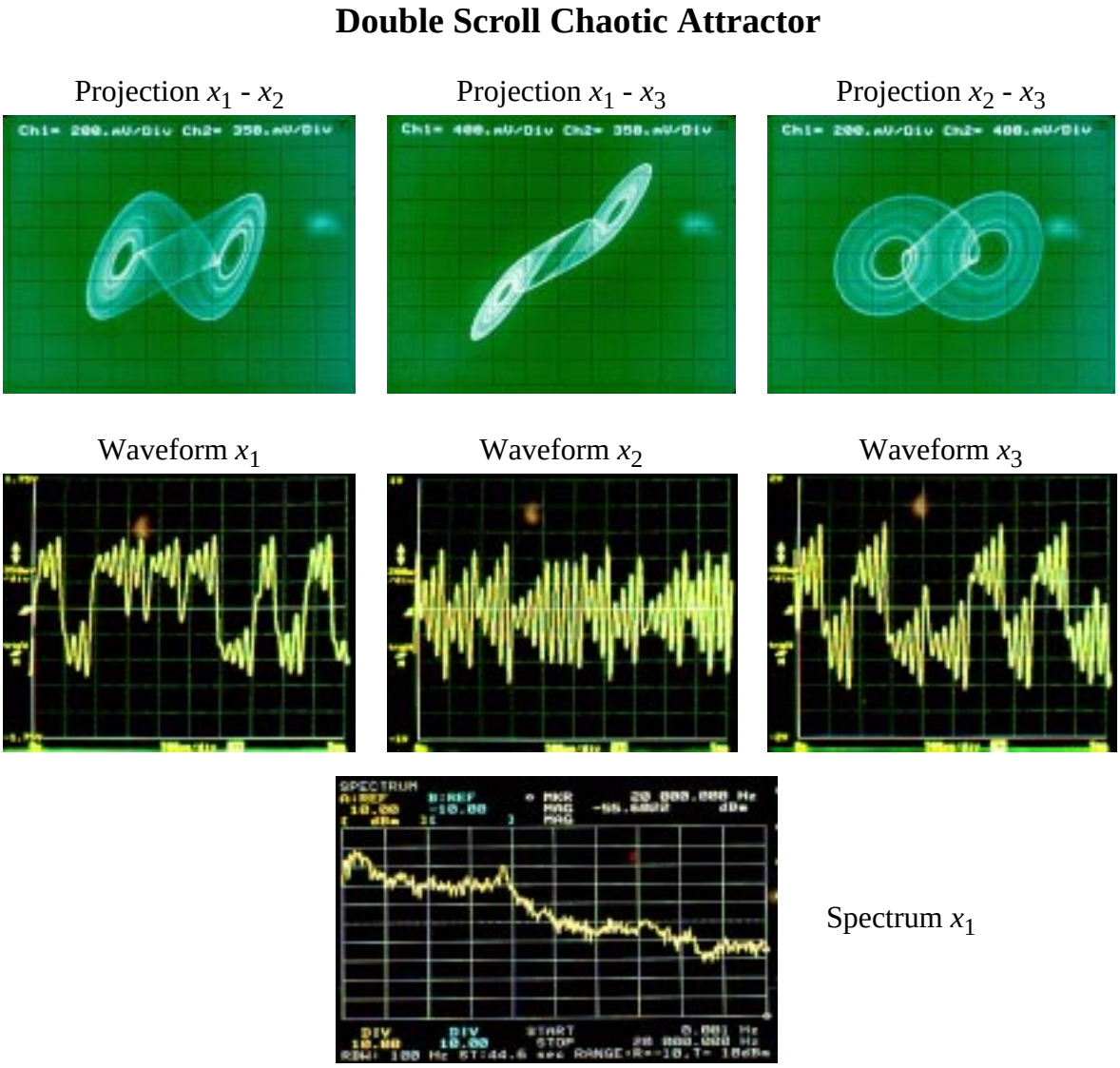


Fig. 15. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.60 μA, I_{cont3} = 2.58 μA.

5-5 Periodic Window

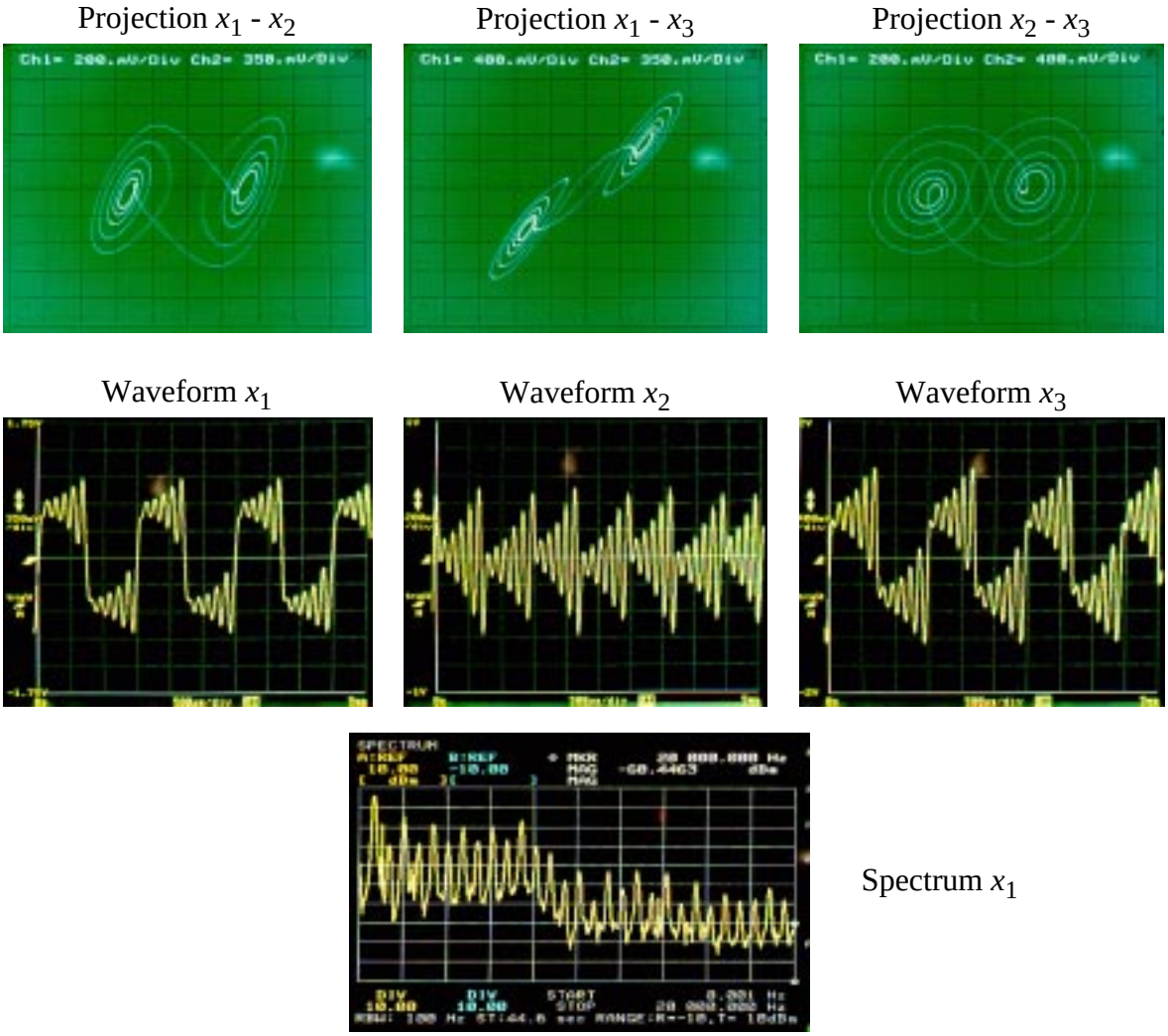


Fig. 16. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.65\ \mu A$, $I_{cont3} = 2.61\ \mu A$.

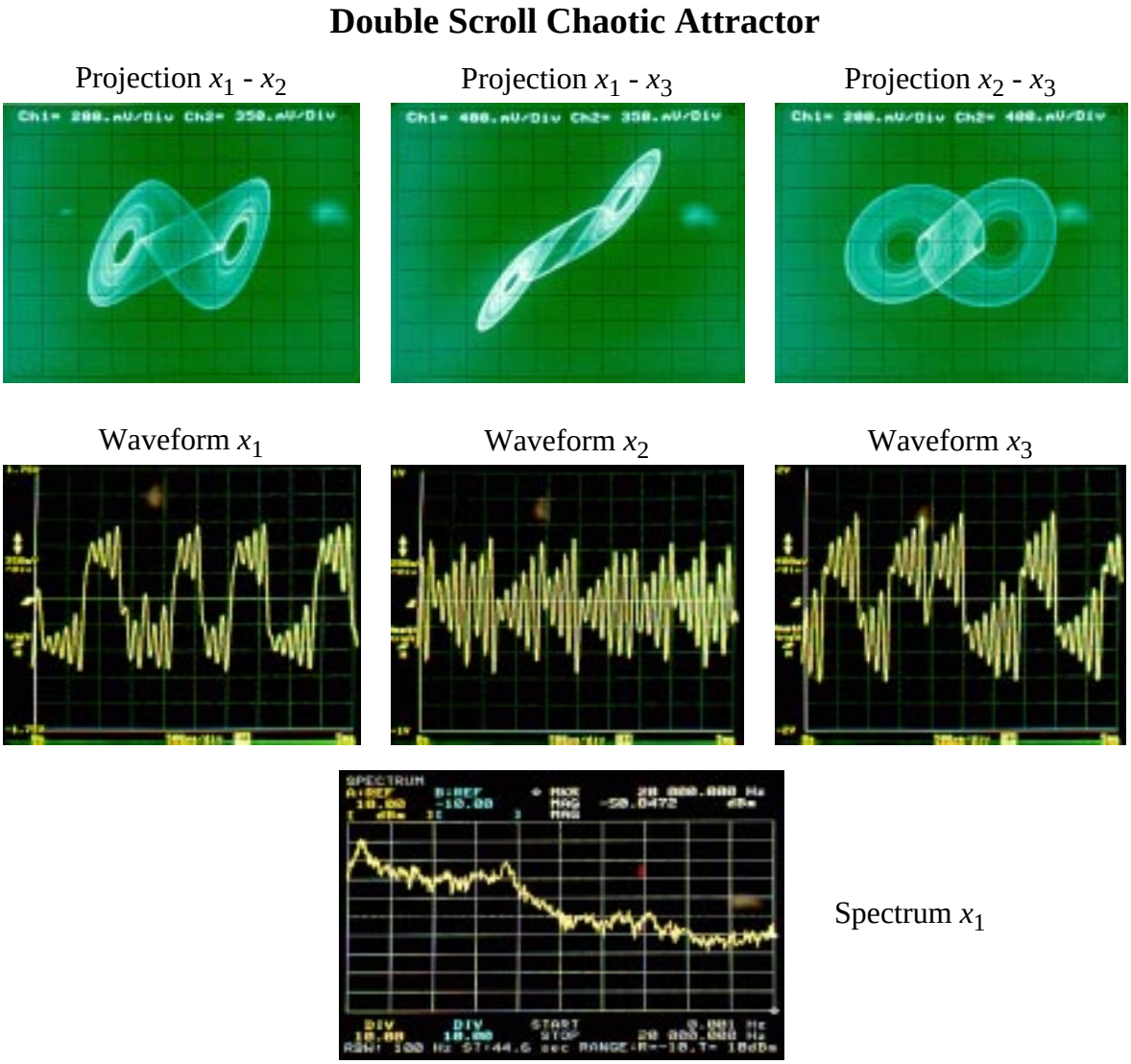


Fig. 17. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.70 μA, I_{cont3} = 2.61 μA.

6-6 Periodic Window

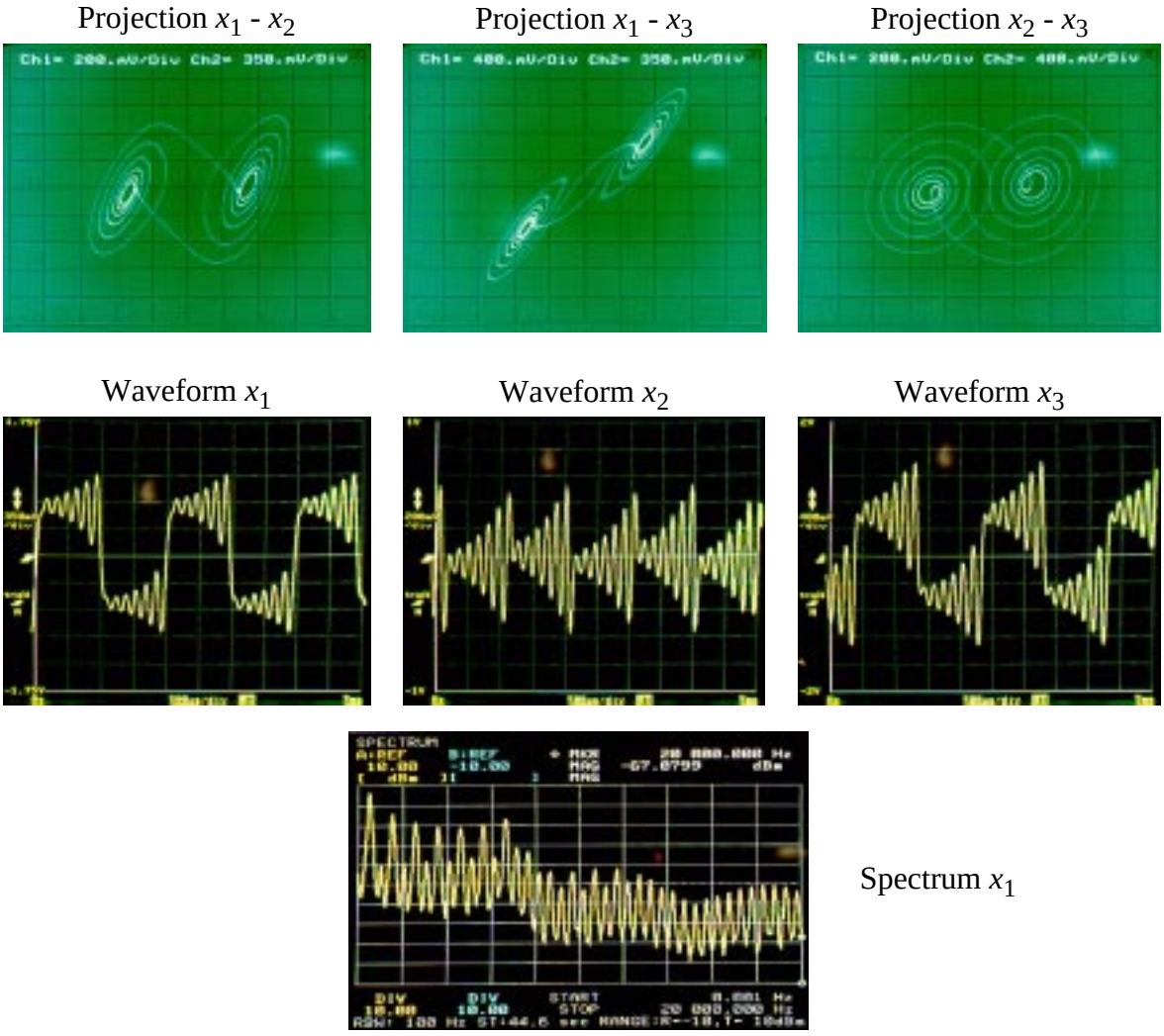


Fig. 18. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.72\ \mu A$, $I_{cont3} = 2.63\ \mu A$.

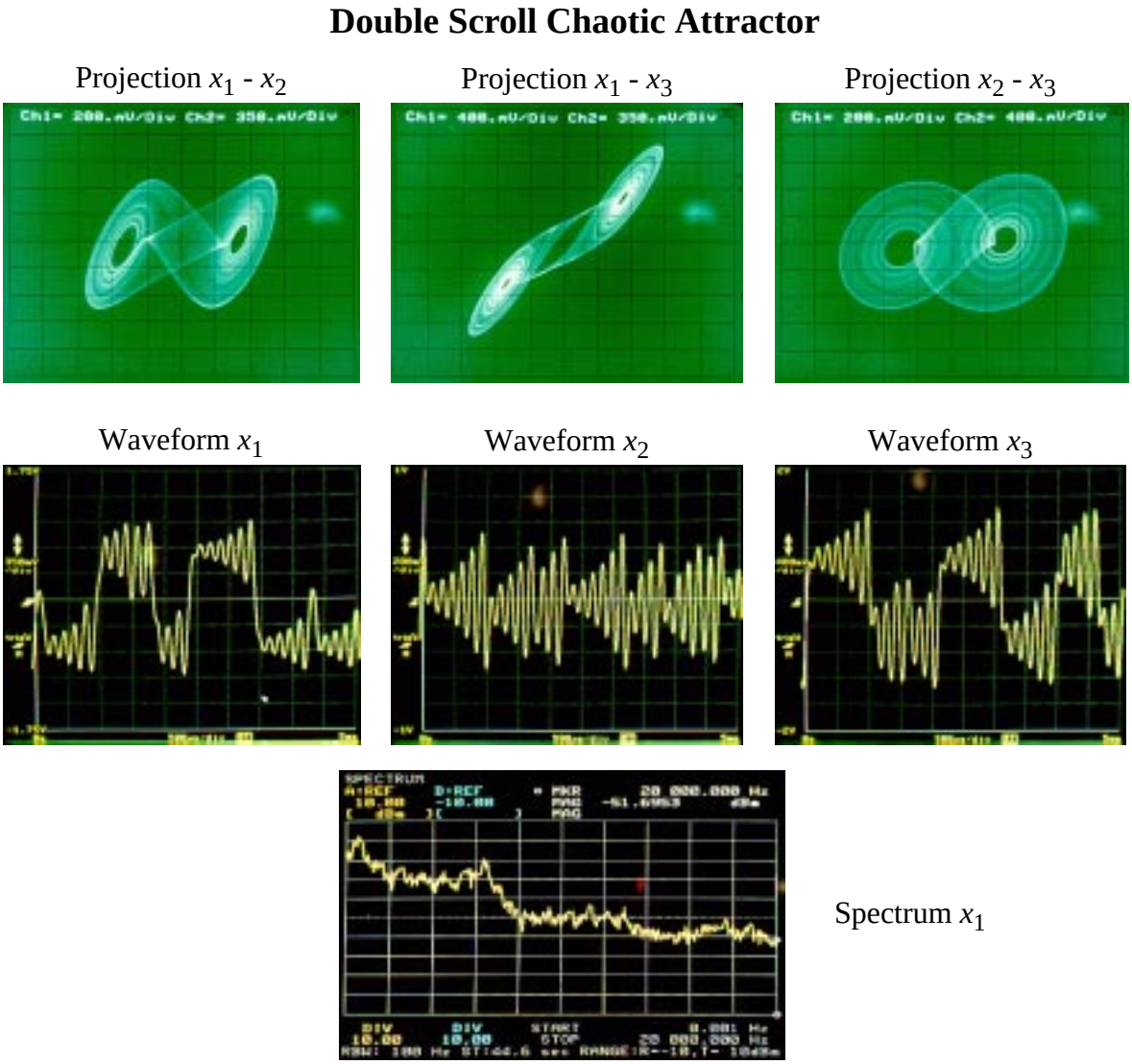


Fig. 19. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.79 μA, I_{cont3} = 2.66 μA.

7-7 Periodic Window

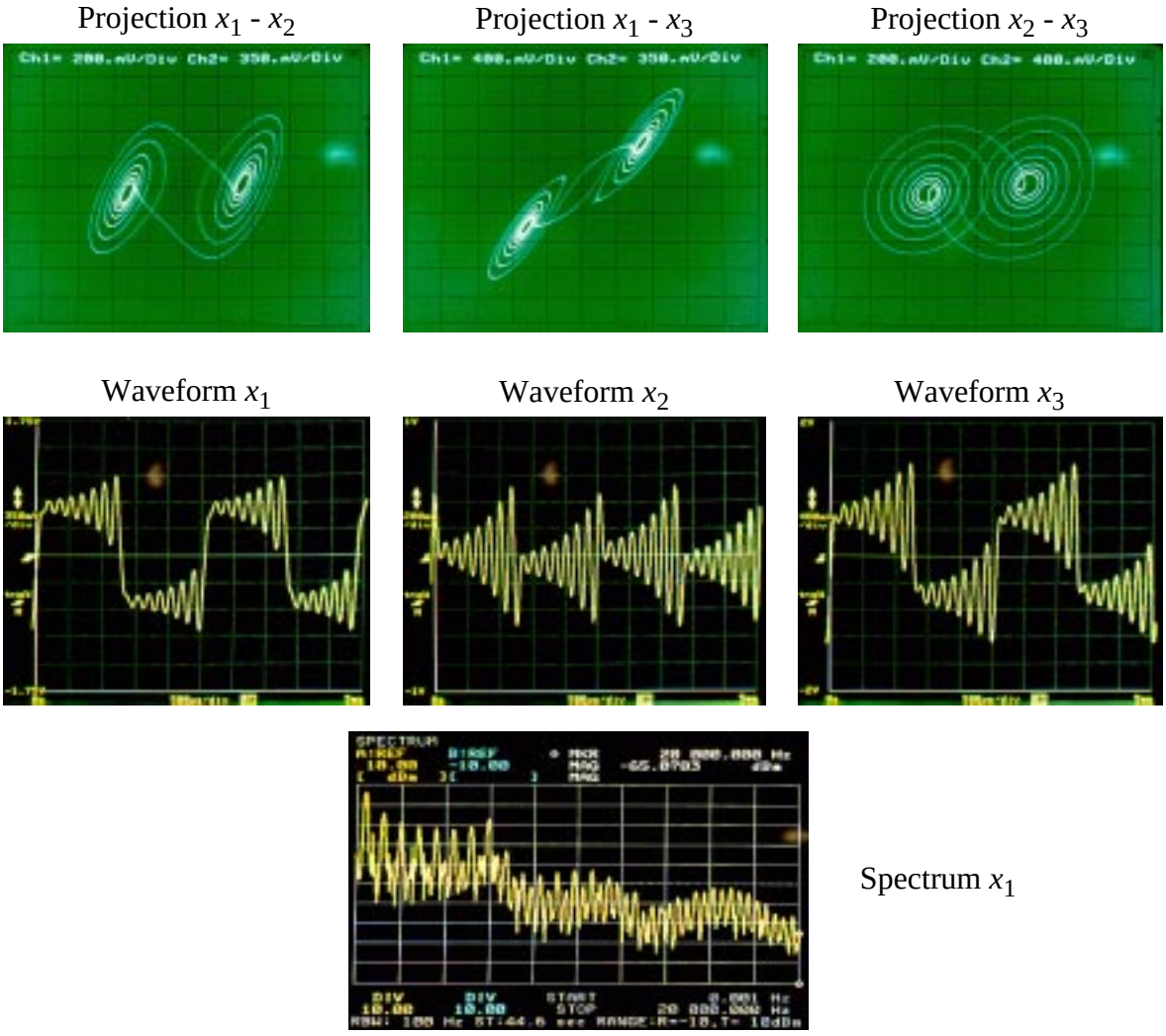


Fig. 20. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.81 μA, I_{cont3} = 2.66 μA.

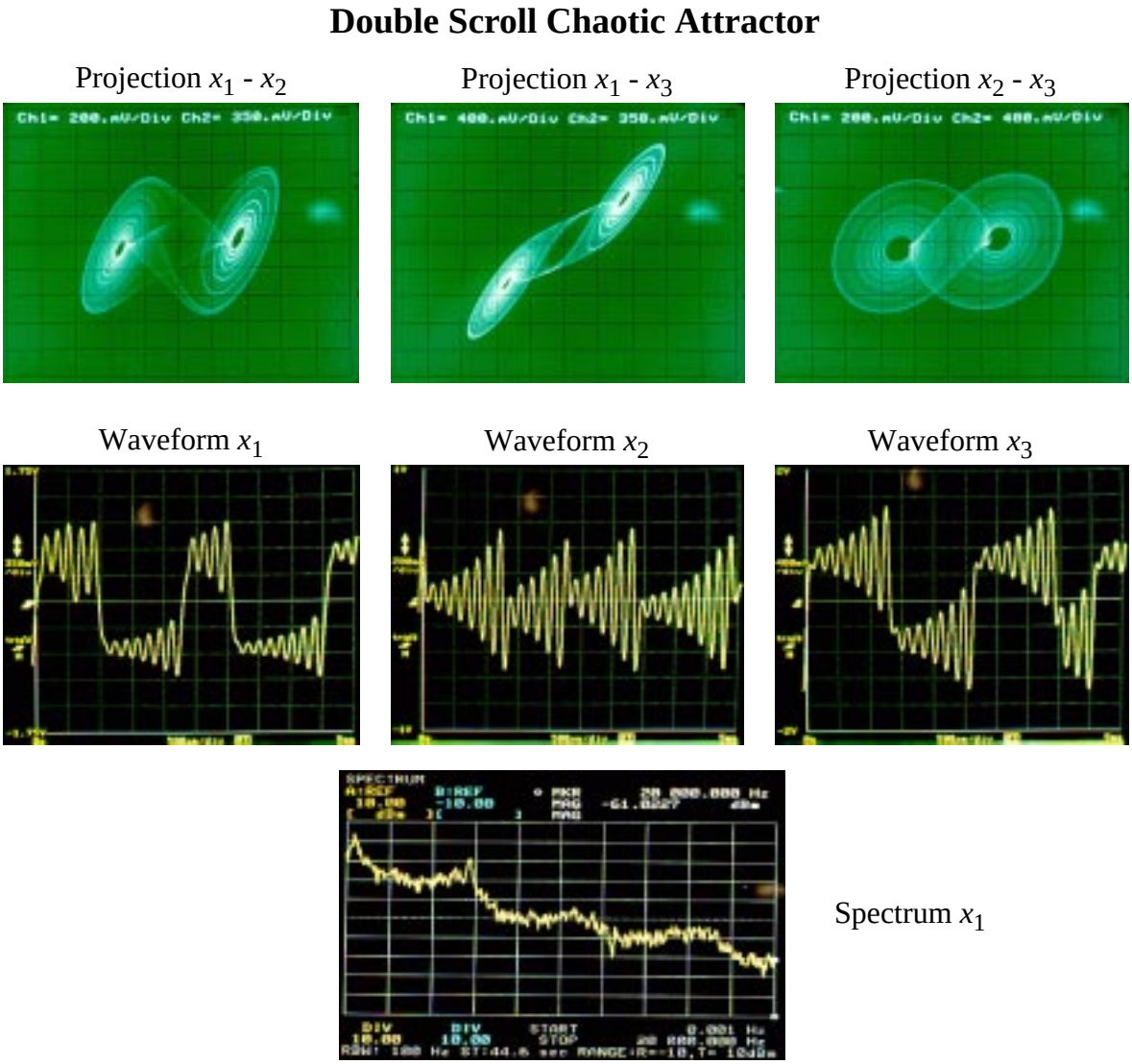


Fig. 21. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for I_{cont2} = 1.85 μA, I_{cont3} = 2.66 μA.

4. Experimental Chaotic Synchronization

Several experiments have been carried out to demonstrate the feasibility of chaotic synchronization between two of the manufactured IC prototypes. They have been grouped according to the interaction mechanism employed into *mutual coupling*, *drive-response* and *inverse system* experiments. An in-depth revision of these synchronization schemes can be found in [Hasler, 1994].

4.1 Mutual Coupling Scheme

Fig.22(a) shows the experimental setup used for the x_1-linear coupling between two of the manufactured chips. It is built by simply inserting a linear resistor R_1 between the x_1 terminals of the prototypes [†3]. Adjustable parameters in both chips were set to $I_{cont1} = 1.4\mu\text{A}$, $I_{cont2} = 1.20\mu\text{A}$, $I_{cont3} = 2.35\mu\text{A}$ and $I_{cont4} = 0.3\mu\text{A}$.

Fig.22(b) displays the correlation index between signals $x_{12,\,buf} - x_{22,\,buf}$, for different values of the coupling resistance R_1. This plot has been obtained by keeping track of the signals at 10,240 instants during an arbitrary time interval of length 20ms. A similar plot for signals $x_{13,\,buf} - x_{23,\,buf}$ is shown in Fig.22(c). It is interesting to note that synchronization of signals $x_{12,\,buf} - x_{22,\,buf}$ tends to deteriorate at lower resistance values than signals $x_{13,\,buf} - x_{23,\,buf}$. Also observe that both correlation indexes maintain above 0.95 for approximately $R_1 < 750\text{k}\Omega$, thus confirming synchronization in spite of the chaotic behavior exhibited by the oscillators. This is illustrated in Fig.23(a)-(b) which show that the $x_{12,\,buf} - x_{22,\,buf}$ and $x_{13,\,buf} - x_{23,\,buf}$ phase plots follow nearly perfect straight lines, even if circuits evolve in a typical double scroll attractor. In order to test the robustness of the synchronization against parameter mismatch, we introduced a 10% error on the central slopes of the nonlinearity of the chips, while keeping unaltered the rest of parameters. In this situation, synchronization by x_1-linear coupling was also possible, but for a stronger interaction between the oscillators (lower values of the coupling resistance R_1). Namely, it was found that synchronization with a correlation index larger than 0.95 in the variables x_2 and x_3 is only possible for $R_1 < 480\text{k}\Omega$.

A similar setup was built by inserting a linear resistor R_2 between the x_2 terminals of the oscillators, thus leading to an x_2-coupled system. Fig.24(a)-(b) show the correlation

3. In the sequel, we adopt the following nomenclature to distinguish the output terminals of the chips: Output variables from unbuffered terminals are denoted as x_{ij}. For buffered terminals, output signals are denoted as $x_{ij,\,buf}$. In both cases, the first subindex, i, indicates the chip ($i = 1, 2$), and the second subindex, j, the state variable of the oscillator ($j = 1, 2, 3$).

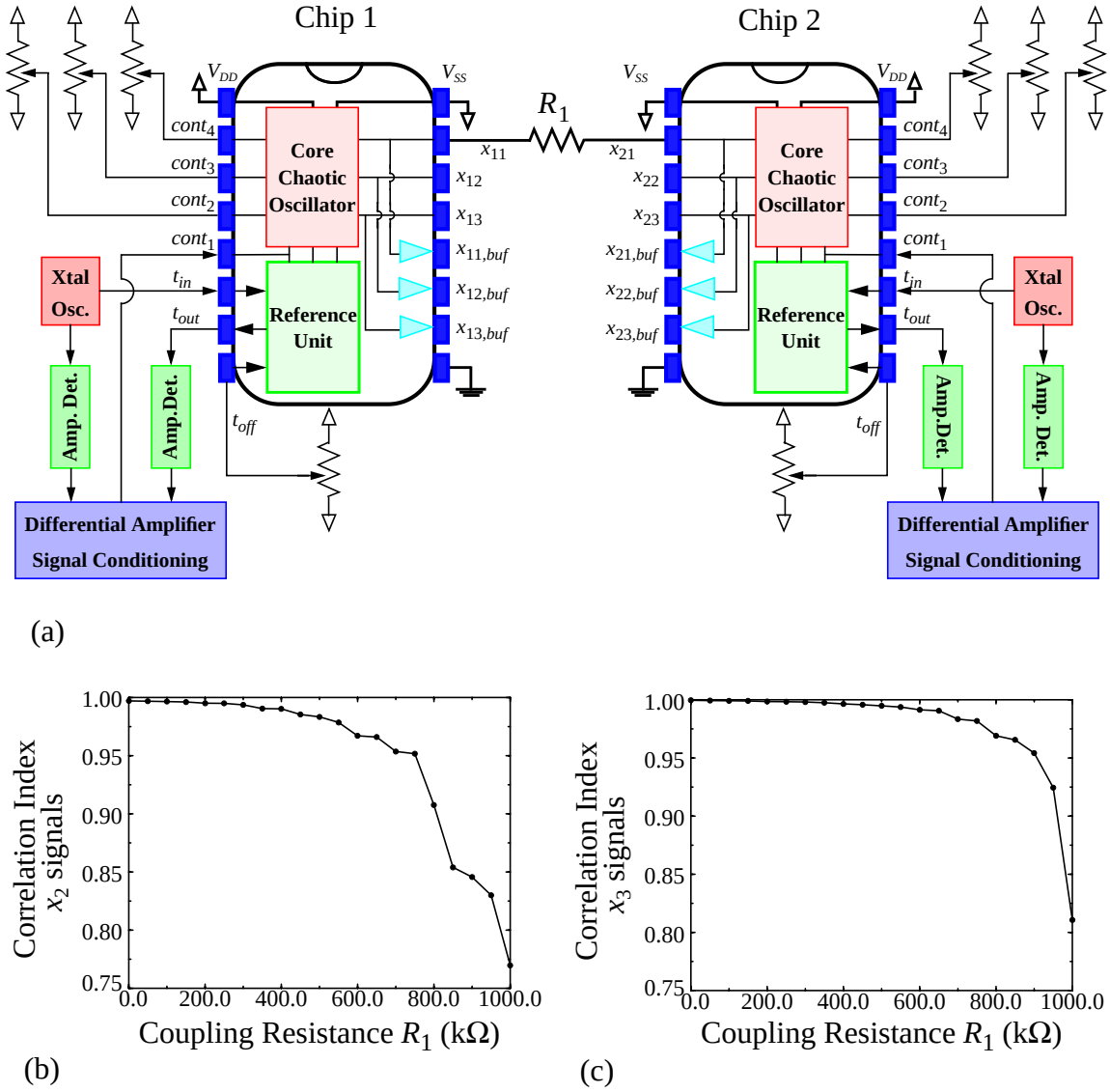


Fig. 22. (a) Experimental setup for an x_1-linear coupling synchronization scheme; (b)-(c) Correlation indexes between $x_{12,\,buf} - x_{22,\,buf}$ and $x_{13,\,buf} - x_{23,\,buf}$, respectively.

indexes of signals $x_{11,\,buf} - x_{21,\,buf}$ and $x_{13,\,buf} - x_{23,\,buf}$, respectively, for different values of the coupling resistance R_2. Observe that synchronization performance of this scheme worsens with respect to the x_1-linear coupling system. In fact, the correlation index of signals $x_{11,\,buf} - x_{21,\,buf}$ is always below 0.75 even if the resistance is replaced by a short (maximum interaction strength). As an illustration, Fig.24(c)-(d) show the $x_{11,\,buf} - x_{21,\,buf}$ and $x_{13,\,buf} - x_{23,\,buf}$ phase plots for $R_2 = 25\text{k}\Omega$. Note that the system exhibits sporadic

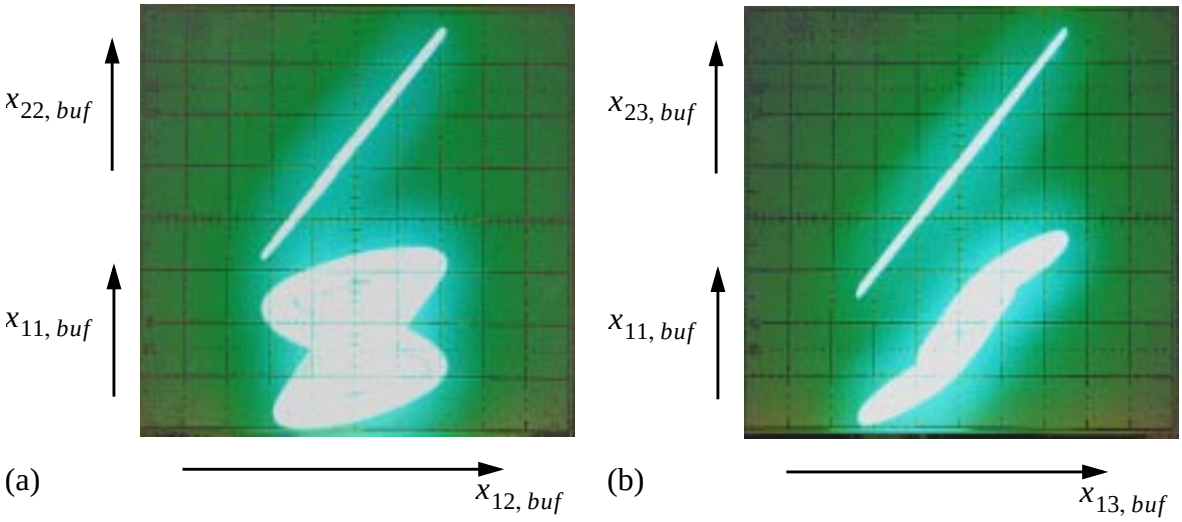


Fig. 23. Synchronization performance of the x_1-linear coupling system for $R_1 = 200\text{k}\Omega$.

losses of synchronization as indicated by the "wings" at both sides of the $x_{11,\,buf} - x_{21,\,buf}$ bisectrix.

An x_3-coupled system was also probed in the laboratory, but synchronization was not possible in this case.

4.2 Drive-Response Scheme

Fig.25 considers a drive-response scheme as originally proposed in [Carroll & Pecora, 1991]. Fig.25(b)-(c) show the phase plots obtained from the x_1-drive experimental setup depicted in Fig.25(a). Adjustable parameters were set as in the previous section. As can be seen from the $x_{12,\,buf} - x_{22,\,buf}$ and $x_{13,\,buf} - x_{23,\,buf}$ phase plot, nearly ideal synchronization (correlation indexes above 0.99 in the x_2 and x_3 variables) is obtained in spite of the chaotic behavior exhibited by the circuits.

With regard to the x_2-drive scheme, it was found that synchronization depends on the dynamic behavior of the oscillators. Namely, it was found that synchronization worsens as the biasing current I_{cont2} increases, i. e., as the circuits evolve through the period-doubling sequence. As an example, Fig.26(a)-(b) show the phase plots obtained from the x_2-drive experimental setup for $I_{cont2} = 1.20\mu\text{A}$. Correlation indexes are 0.83 for the x_1 signals and 0.95 for the x_3 signals.

Synchronization was not possible for a x_3-drive configuration as predicted by theory [Madan, 1993].

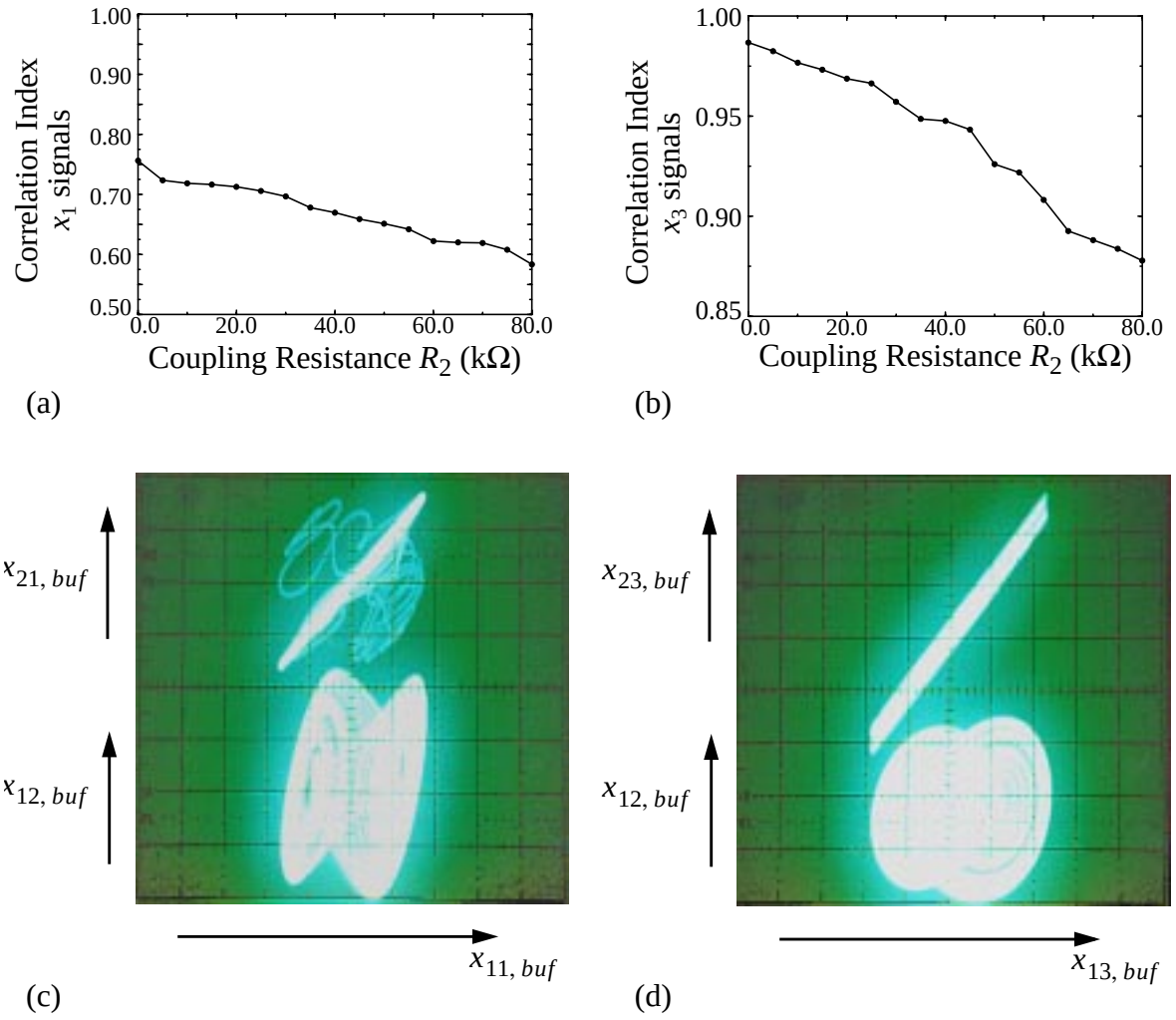


Fig. 24. Measurements from an x_2-linear coupling synchronization scheme. (a)-(b) Correlation indexes between $x_{11,\,buf} - x_{21,\,buf}$ and $x_{13,\,buf} - x_{23,\,buf}$, respectively. (c)-(d) Synchronization performance for $R_2 = 25\text{k}\Omega$.

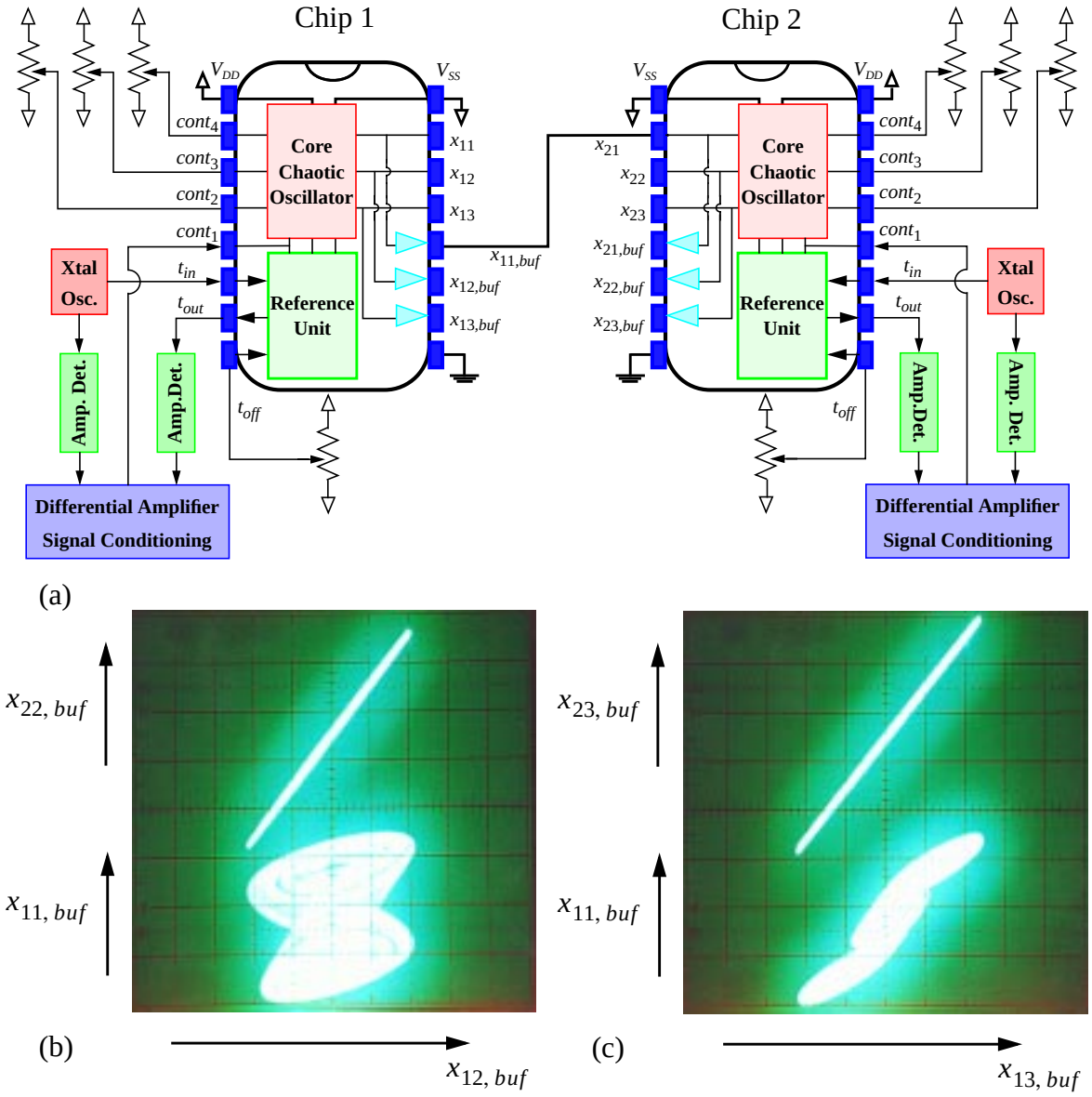


Fig. 25. (a) Master-Slave simplified experimental setup; (b)-(c) Measured performance.

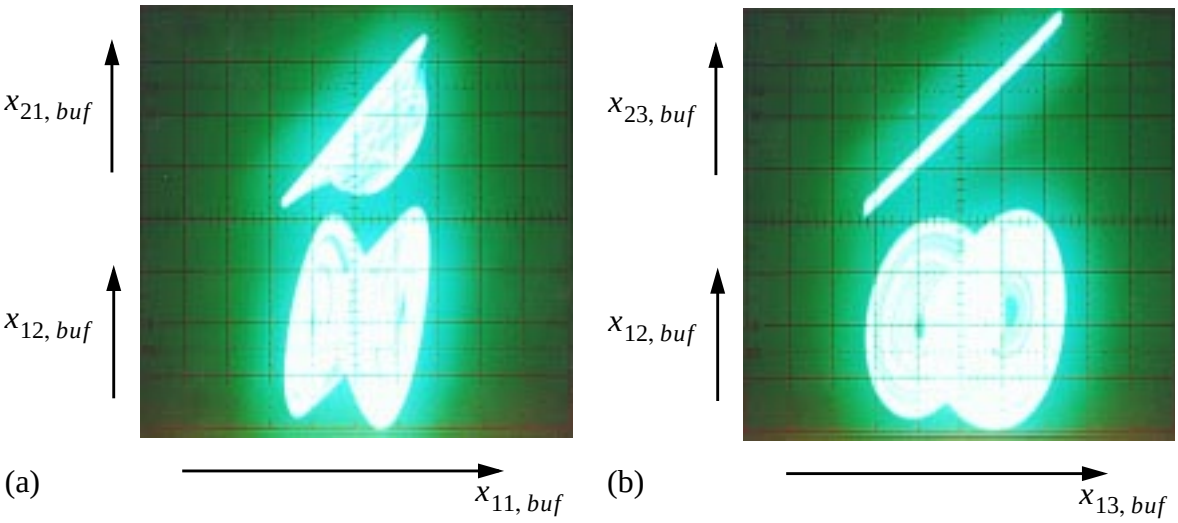


Fig. 26. Synchronization performance of the x_2-drive system.

4.3 Inverse System Scheme

Fig.27(a) shows the experimental setup used to demonstrate synchronization by the inverse system approach between two of the manufactured chips. A voltage signal $s(t)$ is linearly converted to a current and injected in the x_{11} terminal of the first chip. The voltage $\Phi(t) = x_{11,\,buf}$ generated by this prototype is then transmitted to a receiving system which consists of a current detector, a voltage amplifier and a chaotic oscillator matched with that of the transmitter. In the receiver, the signal $\Phi(t)$ drives the current detector which is a device with one input- and two output-ports. One of the output terminals acts as a voltage buffer from the input port, and it is connected to the x_{21} terminal of the second chaotic oscillator prototype. The other terminal provides a voltage proportional to the current flowing through the first output port, and it is connected to a programmable voltage amplifier. This amplifier, in turn, controls the amplitude of the voltage generated by the current detector and obtains the recovered signal $r(t)$. In practice, the current detector and the voltage amplifier can be funded in a single block formed by an opamp and an instrumentation amplifier.

Fig.27(b) illustrates the performance of the setup. The picture on the left shows the input signal $s(t)$ (a sine wave of 10kHz and $350\mathrm{mV_{p-p}}$) and the recovered signal $r(t)$. As can be seen a nearly perfect synchronization is achieved. On the other hand, the picture on

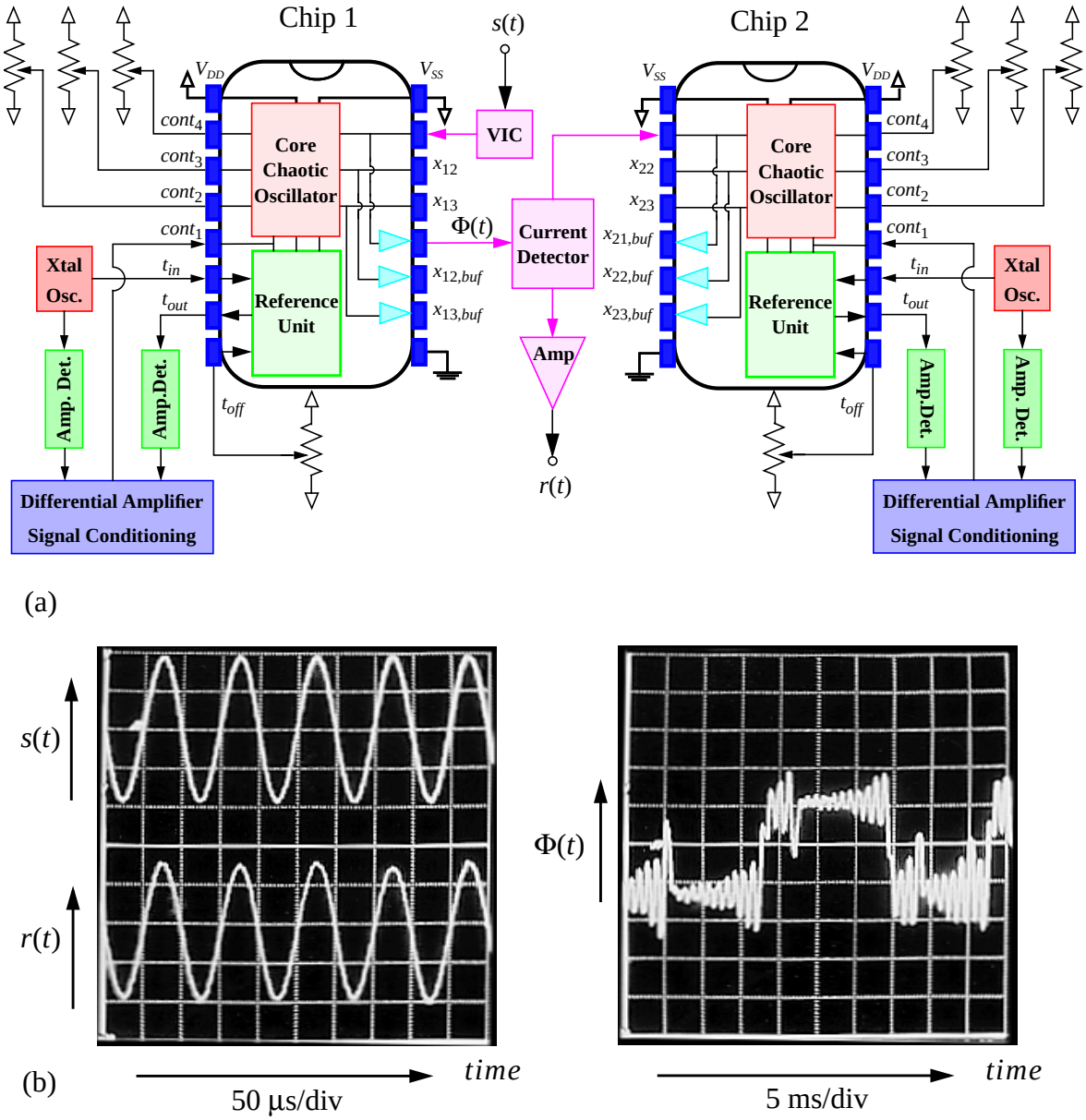
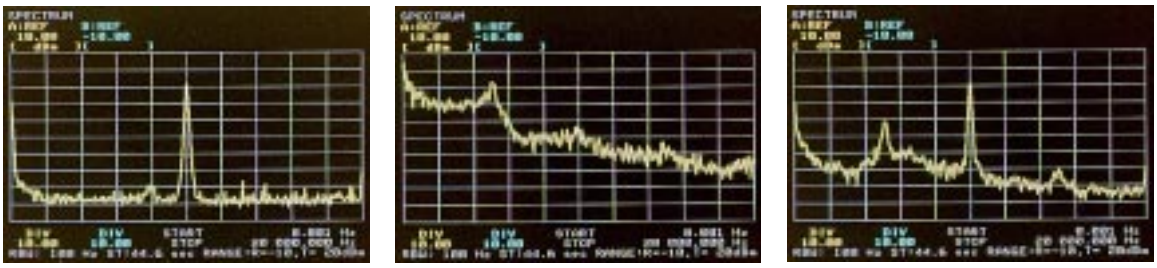


Fig. 27. (a) Simplified experimental setup for the inverse system approach; (b) Measured performance.

the right of Fig.27(b) shows the waveform of the chaotic modulated transmitted signal, which clearly keeps no resemblance with the injected tone.

Fig.28 shows the power spectra of the signals in Fig.27(b)-(c). Note that the signal to noise ratio of the recovered signal (Fig.28(c)) is greater than +55dB with less than -0.2dB loss of the input signal power (Fig.28(a)) [†4]. Also note that the spectrum of the transmitted

4. For input frequencies around 15kHz, the signal-to-noise ratio rises up to +60dB.



(a) (b) (c)

Fig. 28. Power spectra of the (a) input signal; (b) transmitted signal; and (c) recovered signal.

signal does not present a peak at the input frequency, thus confirming that $s(t)$ is completely hidden on the chaotic waveform $\Phi(t)$. At lower tone frequencies, masking property still holds, but the signal-to-noise ratio of the recovered signal notably worsens. In fact, for input frequencies below 1kHz, it has been found that the signal-to-noise ratio drops down to +40dB, while retaining similar losses at the receiver.

The performance of the inverse system setup in Fig.27(a) has been also statistically characterized in time domain by comparing the input signal $s(t)$ with the recovered signal $r(t)$. We have assumed that $s(t)$ consists of a single tone and have varied its amplitude and frequency. By keeping track of the recovered signal $r(t)$, we can identify which are the better conditions for signal transmission. Fig.29 shows the offset, variance and maximal deviation of the recovered signal with respect to the input signal. Special mention deserves the evolution of the variance with the tone amplitude, shown in Fig.29(b). Observe that for low tone amplitudes (below 350mV), the variance maintains small (less than 1.5mV^2) for input frequencies between 1 and 25kHz. As the amplitude raises from this value, the variance abruptly increases, specially at the bounds of the input frequency range. This means that for amplitudes larger than about 350mV, synchronization is lost. We have identified two main causes for desynchronization:

- The receiver is unable to keep track of the transmitted signal.
- The transmitter becomes locked at a stable limit cycle regardless of $\Phi(t)$.

The first cause fundamentally appears at high input frequencies, while the second occurs for low input frequencies. For amplitudes lower than 350mV, the system may exhibit sporadic losses of synchronization as indicated by the maximal deviation between the input and recovered signals, shown in Fig.29(c). However, after a short transient, synchronization is again restored.

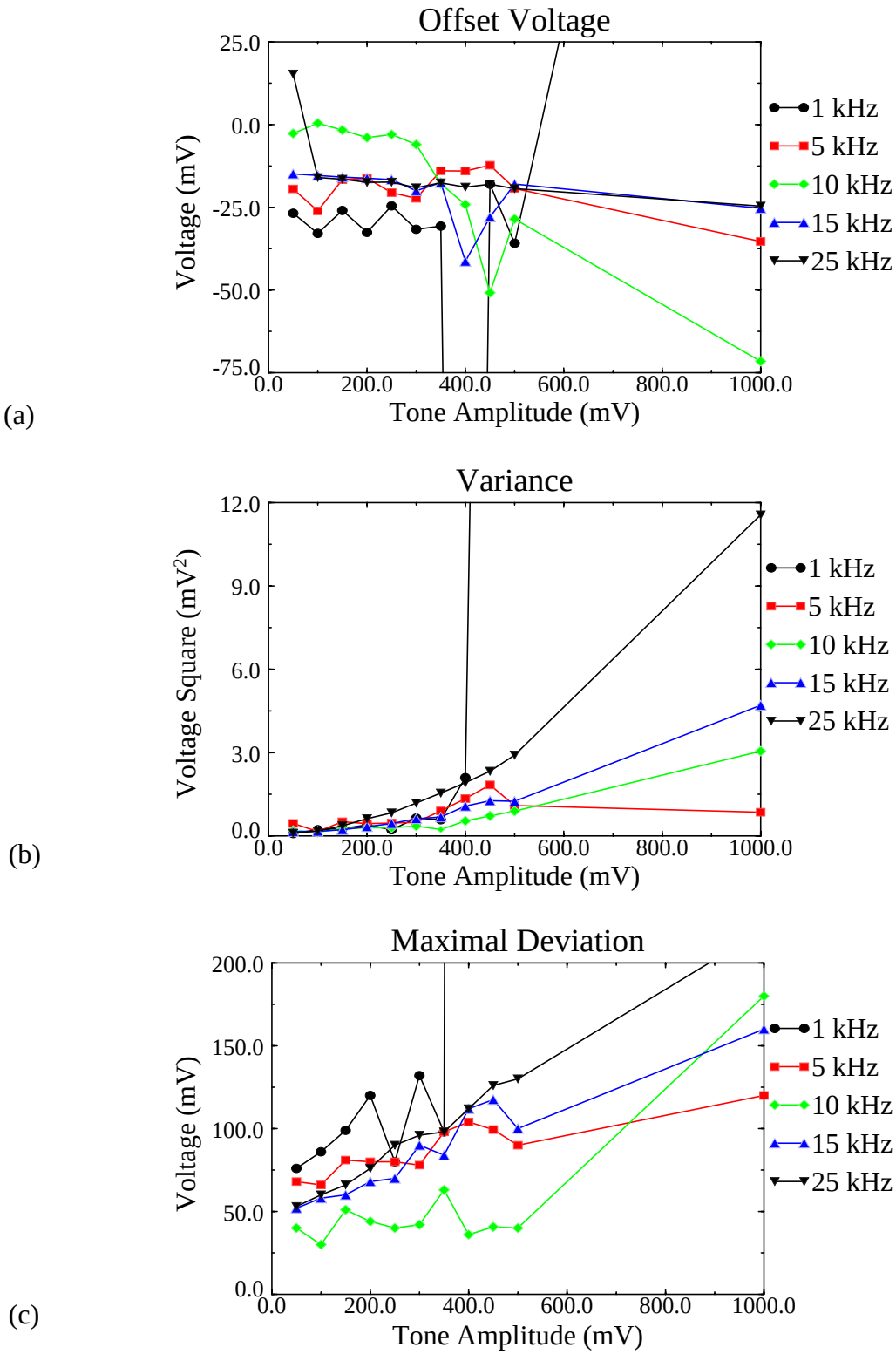


Fig. 29. Time-domain performance of the chaotic modulation synchronization scheme using two integrated prototypes.

We have also experimentally evaluated the correlation index between the input and

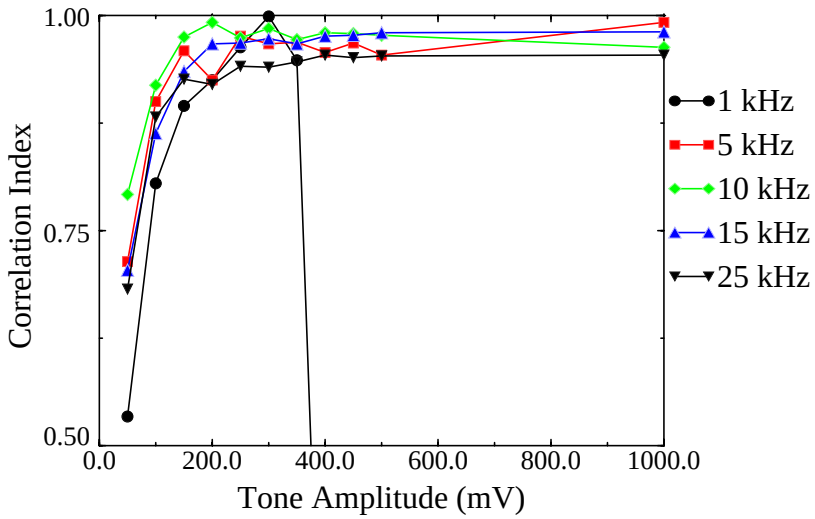


Fig. 30. Correlation index between the input and the recovered signals.

the recovered signals. This is illustrated in Fig.30. Observe that, for tone amplitudes above 150mV, correlation index is always larger than 0.9 regardless of the input frequency. Taking this into account as well as the previous results on the variance, we conclude that the amplitude of the input signal must be comprised between 150mV and 350mV, for input frequencies between 1 and 25kHz, in order to guarantee synchronization.

Taking into account the range of frequencies used for $s(t)$ and the noise-like appearance of the transmitted signal $\Phi(t)$, the synchronization scheme in Fig.27(a) could be readily exploited for audio signal encryption. To evaluate the security of the transmission, we have measured the correlation index between the input and the transmitted signal, assuming again that $s(t)$ consists of a single tone. The results are shown in Fig.31. Note that the index is close to zero for every input frequency, excepting at 1kHz. In this last case, since the transmitter evolves into a stable limit cycle for input amplitudes above 350mV, the correlation index tends to increase.

5. Chip Function and Block Diagram

This section contains the functional description and circuit realization of the core chaotic oscillator. For those readers with scarce knowledge of integrated circuit design, some fundamental concepts will be given at the front-end of this description.

Fig.32 illustrates a systematic procedure for the monolithic realization of arbitrary

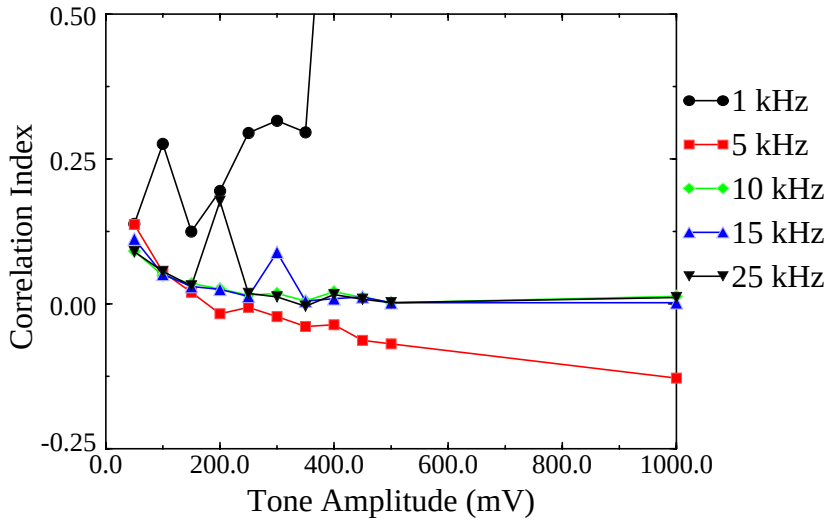


Fig. 31. Correlation index between the input and the transmitted signals.

nonlinear dynamical systems. This procedure strongly relies upon proper *hierarchical* problem decomposition as shown in Fig.32, which particularizes for the well-known double-scroll attractor. The first step in the methodology is to identify the set of equations describing the dynamics. This corresponds to the *behavioral* level at the top of the hierarchy. The obtained description maps down to the *block level*, which defines a network synthesis architecture for the problem. At the block level, the different operators, or *functional* building blocks, required for physical realization, as well as their interconnection, are clearly identified. Each of these blocks must be subsequently mapped down to a collection of interconnected circuit elements, thus defining a *circuit level*. Two different sublevels can be identified; one containing only idealized elements (for instance VCCS's), and another where these idealized elements are realized using available circuit primitives of the technology. Fig.32 illustrates both sublevels. Observe that the circuit level infers choosing the physical nature of the variables which support information flow (usually voltages, currents or both). Bottom level in the VLSI design hierarchy define the *layout* phase, where circuit primitives are codified into geometrical objects required for processing and fabrication.

In this paper, we will be mainly interested in the two first steps of the hierarchy, i.e., in the behavioral and block level design aspects of the chaotic oscillator. Technical details at the circuit and layout levels will be published elsewhere.

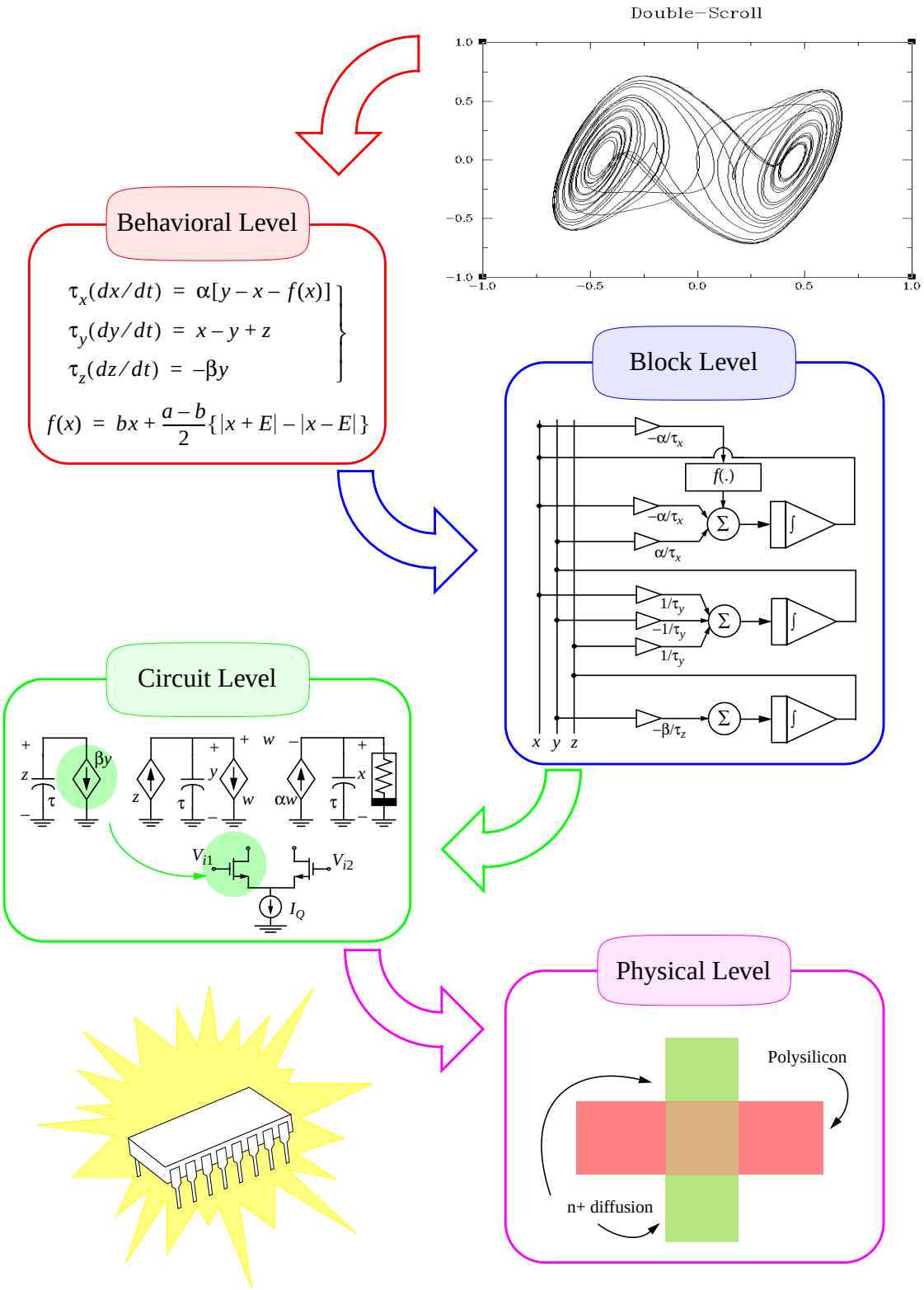


Fig. 32. Synthesis route towards monolithic nonlinear circuits.

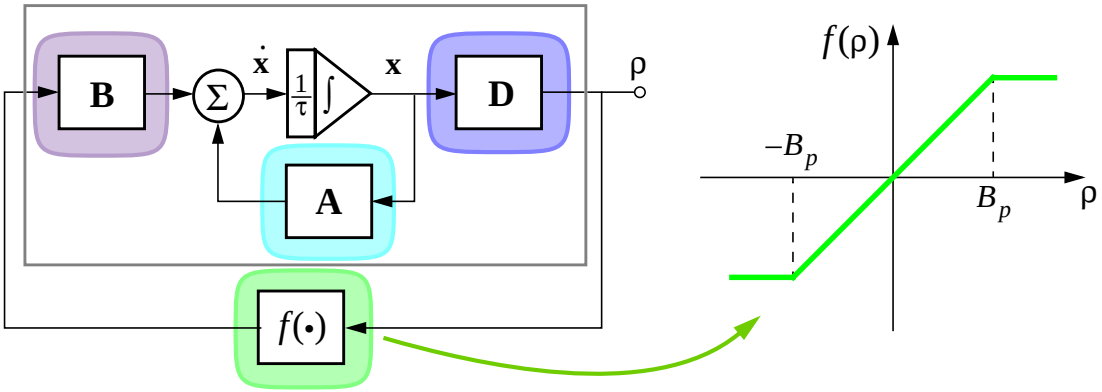


Fig. 33. Block diagram for the members of the family L_3.

5.1 Behavioral Level Description

The mathematical model of the designed chaotic oscillator is a *canonical* system (which will be defined below) of the family of continuous, odd-symmetric, three-region piecewise-linear (PWL) vector fields in $\Re^3$. Members of this family, denoted hereafter by L_3, are generally represented by the following third order continuous-time nonlinear state equation [Chua *et al.*, 1986],

$$\tau \frac{d}{dt}\mathbf{x}(t) = \mathbf{F}[\mathbf{x}(t)] = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\, f[\mathbf{D}^\dagger \mathbf{x}(t)] \tag{10}$$

which can be mapped onto the analog computer concept shown in Fig.33. In the above equation, τ represents the time-integration constant; $\mathbf{x}(t) = [x_1(t), x_2(t), x_3(t)]^\dagger$ is the state-space vector; $\mathbf{A} = [a_{ij}]$ is a real invertible square matrix defining the linear part of the system; $\mathbf{B} = [b_i]$ and $\mathbf{D} = [d_i]$ are real 3-dimensional vectors; and the nonlinear map $f(\,)$ is a real-valued continuous PWL function given by

$$f[\mathbf{D}^\dagger \mathbf{x}(t)] = \frac{1}{2}\{\left|\mathbf{D}^\dagger \mathbf{x}(t) + B_p\right| - \left|\mathbf{D}^\dagger \mathbf{x}(t) - B_p\right|\} \tag{11}$$

where B_p is a real scale factor, with no influence on the qualitative dynamic behavior of the system. The function $f(\,)$ thus defined, divides $\Re^3$ into an inner region D_0 containing the origin, and two outer regions D_{+1} and D_{-1}, in such a way that, $\mathbf{F}(\mathbf{x}) = -\mathbf{F}(-\mathbf{x})$. According to Eq. (11), the two parallel boundary planes separating D_0 from the outer regions D_{+1} and D_{-1}, are given respectively by,

$$\begin{aligned} U_{+1} &= \{\mathbf{x} \in \Re^3 \mid \mathbf{D}^\dagger \mathbf{x} = B_p\} \\ U_{-1} &= \{\mathbf{x} \in \Re^3 \mid \mathbf{D}^\dagger \mathbf{x} = -B_p\} \end{aligned} \tag{12}$$

It is worth noting that the qualitative behavior of any member of the family L_3 is solely determined by the three eigenvalues μ_1, μ_2 and μ_3 associated to the inner region of the vector field $\mathbf{F}(\ )$, and the three eigenvalues ν_1, ν_2 and ν_3 associated to the outer regions [Chua *et al.*, 1986].

By *canonical systems* of L_3 we mean those vector fields in L_3 such that, with only 7 nonzero parameters, are able to synthesize almost every prescribed set of eigenvalue patterns, and hence, to reproduce almost every possible qualitative dynamics in L_3 [5] [Chua & Lin, 1990; Chua, 1993]. A well-known example of canonical system in L_3 is the *Chua´s oscillator* which is endowed with a rich repertoire of nonlinear dynamical phenomena, including all kinds of bifurcations and routes to chaos (period-doubling, intermittency and torus breakdown). Actually the number of strange attractors which can be generated with Chua´s oscillator form a zoo with more than 30 different exemplars (see [Chua *et al.*, 1993] for a nice collection of color plates corresponding to all these attractors).

From an integrated design perspective, canonical systems deserves special attention: Since system parameters must be mapped into physical devices, those models with a minimum number of nonzero parameters will be a priori the most advantageous in terms of system complexity and area consumption.

In our design, we have taken advantage of the topological conjugacy property of canonical systems in L_3, not to reproduce as much as possible dynamic behaviors, but to identify which of these systems is the best suited for the monolithic implementation of a particular chaotic attractor. Accordingly, the behavioral level description of our prototype have been obtained after applying the following algorithm:

- Calculate the eigenvalues associated with the system candidate in L_3 whose attractor is to be reproduced by canonical systems, up to topological conjugacy.
- Identify the parameter values which must take every canonical system in L_3 so that corresponding eigenvalues coincide with those obtained in the previous step.
- Select that canonical system of those previously identified which satisfies as close as possible a set of optimization criteria derived from microelectronic experience.

5. Properly speaking, canonical systems are said to be *topologically conjugate* to the class $\tilde{L}_3 = L_3 - \varepsilon_0$, where ε_0 is a set of zero measure.

Let us examine each step of the algorithm.

The first step begins with the selection of the particular chaotic attractor to be synthesized. Among the wide number of candidates offered by the family L_3, we have considered the so-called *double-scroll* attractor, shown in Fig.34, which arises from the well-known *Chua´s circuit* [Chua, 1992]. The reasons behind this election is threefold. First, and most important, because there are several experimental evidences using discrete components that the model allows the observation of chaos synchronization phenomena. Second, because there is an extense theoretical background concerning its dynamic behavior [Madan, 1993], what supposes an invaluable help during the synthesis root towards an integrated prototype. Finally, because it is one of the simplest models proposed so far for the generation of chaotic signals, and a priori, will result in a easier silicon implementation.

It is worth noting that the double-scroll attractor has been previously synthesized by microelectronic circuits (in fully monolithic form in [Rodríguez-Vázquez & Delgado-Restituto, 1993] and in partial monolithic form in [Cruz & Chua, 1993]). A common feature of both chips is that their behavioral level description were derived directly from Chua´s circuit, and hence, no attempt of performance optimization from an IC design viewpoint was done.

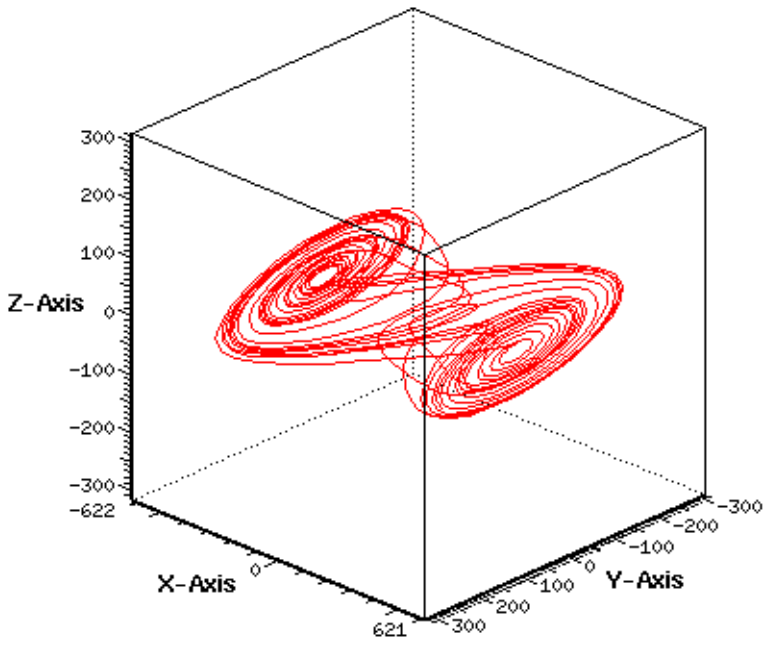


Fig. 34. The Chua's double-scroll chaotic attractor.

The double scroll attractor is not an isolated chaotic phenomenon but it can be visualized for different eigenvalues patterns in L_3. To fit the requirements of the first step in our algorithm, we will adopt the following set of eigenvalues,

$$\mu_1 = 2.22 \qquad \mu_{2,3} = -0.97 \pm j2.71 \tag{13}$$

for the inner region, and

$$\nu_1 = -3.94 \qquad \nu_{2,3} = 0.19 \pm j3.05 \tag{14}$$

for the outer regions, as it is customarily defined in many references (see for instance, [Madan, 1993]).

Now we are in position to deal with the second step of the algorithm. Since the number of canonical systems in L_3 is extremely huge [Chua *et al.*, 1993], calculation of the parameters associated with Eqs. (13)-(14) for each one of these systems would result in a rather time-consuming task even with computer aid. Thus we are enforced to reduce the scope of our design space, or in other words, to impose some values among the 15 parameters defining the family L_3. To this end, we have made the following assumptions:

$$\mathbf{D} = \mathbf{e}_1 = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}^{\dagger} \tag{15}$$

and

$$\mathbf{B} = b_1\mathbf{e}_1 = \begin{bmatrix} b_1 & 0 & 0 \end{bmatrix}^{\dagger} \tag{16}$$

Equation (15) only fixes the orientation of the boundary planes in the state space (see Eq. (12)) and, consequently, it does not impose any constraint on the number of canonical systems. On the contrary, Eq. (16) reduces the number of canonical numbers to a tractable quantity, yet sufficient to make a representative comparison basis. Equation (16) presents also the added benefit of limiting the influence of the nonlinearity $f(\,)$ to only one differential equation of the system (10). Since implementation of nonlinear transfer elements require in general more circuitry than linear ones, the restriction results advantageous in terms of system complexity and area consumption.

The last step of the algorithm refers to the selection of the canonical system best suited for monolithic implementation. We have adopted the following selection criteria in order of relevance:

- *Asymptotic synchronization*. We must select those configurations which guarantee asymptotic synchronization of two chaotic systems when they interact in a proper way. This point only can be verified after realistic behavioral simulations including montecarlo analysis and assuming nonideal transmission channels.
- *Low sensitivity to parameter variations*. We must select those canonical systems which minimize the influence of parameter deviations on the dynamic performance. At the circuit level, this means that the chaotic behavior must be robust enough against the statistical deviations of technological properties.
- *Parameters must have integer ratios*. This criterium arises because most analog circuit techniques are based on the matching properties of similar components. In general, matching is largely favored if circuit elements are built by replicating a given unitary component. Since system parameters are mapped into electronic devices, it is clear that by keeping integer relationships among parameters, the final circuit realization will gain in accuracy. Also, at the layout level, application of this criterium leads to very modular, high integration density implementations.
- *Low spread of parameter values*. This rule derives directly from the above. If the quotient between the magnitude of the largest and smallest nonzero parameters were very high, the number of unitary elements required to implement the chaotic oscillator would increase, consequently increasing area and power consumption.

After applying the last two steps of the algorithm to the eigenvalue pattern defined in Eqs. (13)-(14), we have obtained the following state equation for the double-scroll attractor

$$\tau\frac{dx_1}{dt} = h(x_1) + \alpha x_2 \qquad \tau\frac{dx_2}{dt} = \alpha(x_1 - x_3) - \gamma\, x_2 \qquad \tau\frac{dx_3}{dt} = \beta x_2 \tag{17}$$

where $h(\,)$ is given by,

$$h(x_1) = m_1 x_1 + \frac{m_0 - m_1}{2}\{|x_1 + B_p| - |x_1 - B_p|\} \tag{18}$$

and the parameter values are defined as,

$$(\alpha, \beta, \gamma, m_0, m_1) = (3, 4, 1, 1, -2) \tag{19}$$

Equations (17)-(18) are equivalent to the representation Eq. (10) with matrices **A**, **B** and **D** defined as

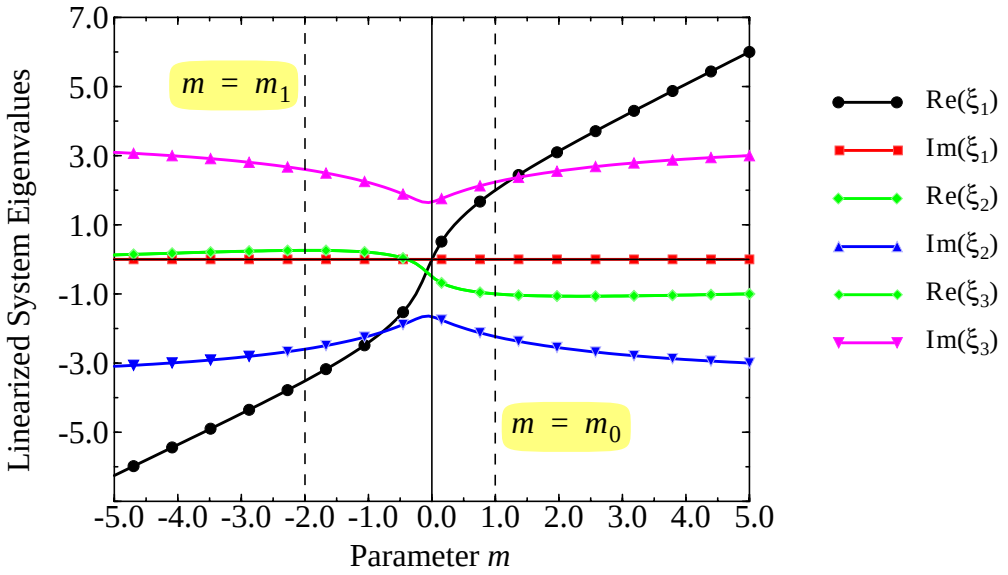


Fig. 35. Evolution of the linearized system eigenvalues with parameter m.

$$\mathbf{A} = \begin{bmatrix} m_1 & \alpha & 0 \\ \alpha & -\gamma & -\alpha \\ 0 & \beta & 0 \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} m_0 - m_1 \\ 0 \\ 0 \end{bmatrix} \qquad \mathbf{D} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{20}$$

where it is worth noting that parameters a_{21} and a_{23} have the same magnitude but opposite signs. As will be shown, this fact may lead to further simplifications at the circuit-level.

Fig.35 shows a representation of the eigenvalues (ξ_1, ξ_2, ξ_3) calculated from the linearized system associated to Eq. (17), i. e., that system with $h(x_1)$ defined as $h(x_1) = mx_1$ instead of Eq. (18), as a function of the equivalent slope m. Since the nonlinearity Eq. (18) is piecewise-linear, the set of eigenvalues (μ_1, μ_2, μ_3) and (ν_1, ν_2, ν_3) corresponding to the inner and outer regions of the Chua´s model, will be given by the values of (ξ_1, ξ_2, ξ_3) at the intersections of the plots in Fig.35 with the lines $m = m_0$ and $m = m_1$, respectively.

The dynamical model defined by Eqs. (17)-(18) clearly meets all the assumed optimization targets: all the parameters have integer values, and their spread is very low (the maximum ratio among parameters is four). Additionally, the resulted configuration is found to exhibit the best possible performance regarding sensitivities against parameter deviations, and also satisfy the asymptotic synchronization condition. Thus, we can conclude that the system formed by Eqs. (17)-(18) is a good candidate for integration purposes.

5.2 Block Level Description

The state-variable approach has been adopted for the block level design of the chaotic system defined by Eqs. (17)-(18). This approach is similar to that followed in classical *analog computation* (see Fig.33) and reduces implementation of PWL dynamic systems to the realization of a number of mathematical operations: *integration*, *summation*, *signal scaling* and *rectification*. However, compared to circuit strategies in classical analog computers where operators are built around operational amplifiers, our approach will be based in transconductors where both voltage and current play a significant role, thus yielding much more compact realizations.

Fig.36(a) shows the block diagram of the core chaotic oscillator obtained state-variable principles. In this diagram, state variables are translated into capacitor voltages, linear transconductors are assumed to perform as ideal voltage controlled current sources (see Fig.36(b)), and the PWL function is determined by the nonlinear transfer characteristics of the transconductor at the upper right corner of the diagram, whose output current is proportional to $h(V_{in})$, where function $h(\ )$ is defined in Eq. (18) (see Fig.36(c)). Taking into account the input-output relationships of all transconductors, Eq. (17) can be easily derived.

Special mention deserves the different alternatives exploited for the realization of system parameters in Eqs. (17)-(18). Taking advantage from the fact that parameters α, β and γ are integer numbers, they have been implemented by first defining a *unitary transconductance block* with gain g_{mu}, and then connecting in parallel as many of such units as indicated in Eq. (19) (their combined contribution is obtained by KCL at the common output node). With this arrangement we are tacitly renouncing to use parameters α, β and γ as external controllable variables of the oscillator, since their absolute values are completely defined once the unit transconductance g_{mu} has been set. For this reason, α, β and γ can be regarded as *fixed* parameters. On the contrary, the global time constant of the system, τ, which, for the block diagram in Fig.36(a) is easily shown to be

$$\tau = C/g_{mu} \tag{21}$$

can be externally controlled by adjusting the value of g_{mu}. This, in turn, can be done by conveniently setting the common *tuning variable* T_v of the transconductors in Fig.36(a) (tuning terminals and their interconnection to a common node have been suppressed for the sake of clarity in the schematic). Parameter τ has no influence on the qualitative dynamic behavior of the oscillator, but only modifies its frequency response. In the chip architecture of Fig.1, tuning variable T_v is provided by the biasing current I_{cont1} applied to pin $cont_1$.

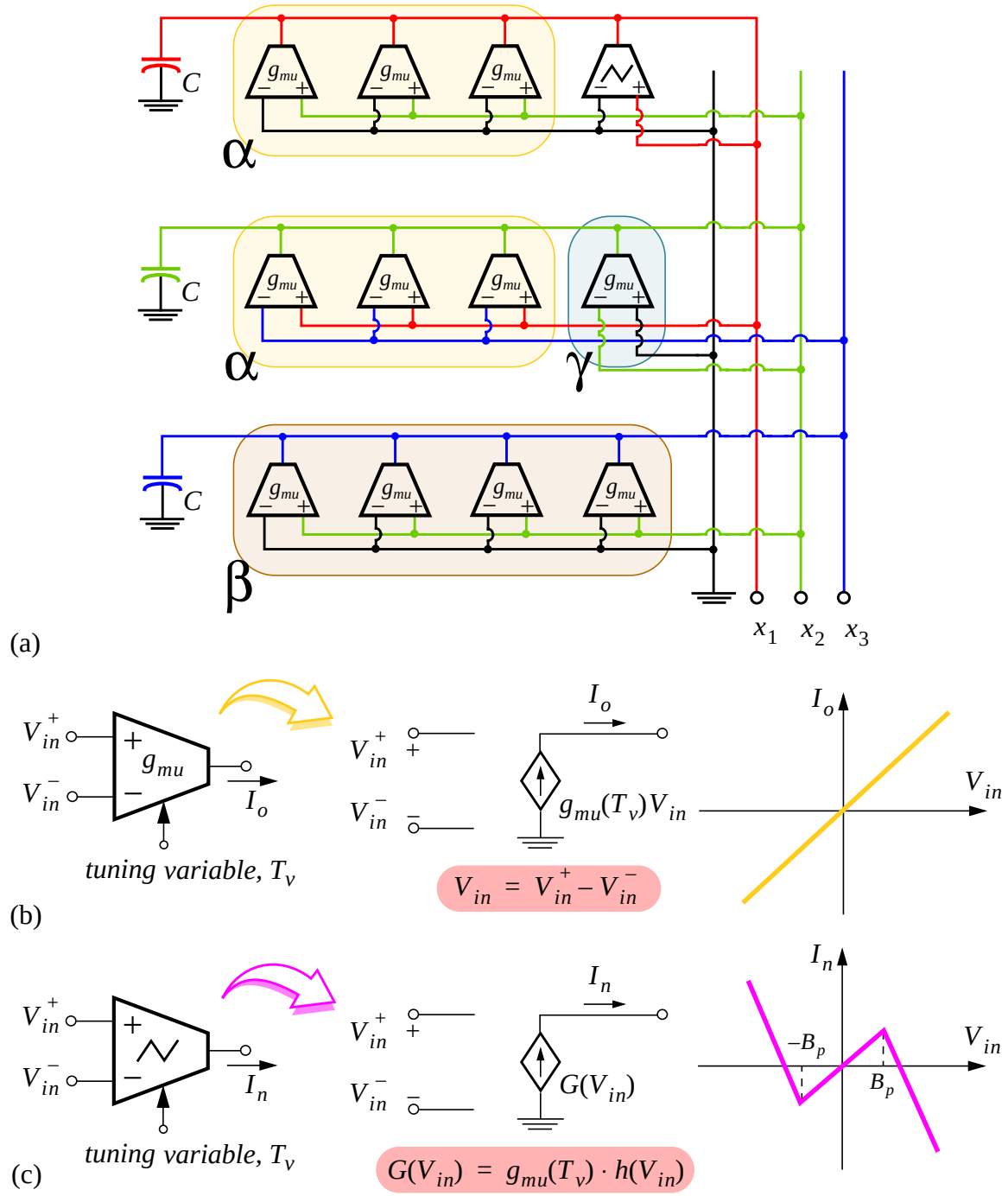


Fig. 36. (a) $G_m - C$ block diagram of the core chaotic oscillator; (b) Ideal model for the linear transconductors; (c) Ideal model for the PWL blocks.

The rest of parameters of the oscillator, , are associated to the nonlin-

ear transconductor of Fig.36(a). In the same way as the tuning variable, all of them have been made externally programmable through appropriate current-mode circuit techniques (details will be provided elsewhere). Parameter B_p, which defines the breakpoints of the PWL characteristic, controls the size of the chaotic attractor in the state space but it has no influence on the qualitative dynamic behavior. Hence, it can be considered as an *amplitude* parameter. It is controlled by the biasing current I_{cont4} applied to pin $cont_4$ in Fig.1. On the other hand, parameters m_0 and m_1 which define the central and outer slopes of the PWL function, respectively, have a large influence on the qualitative time evolution of the oscillator. In fact, m_0 and m_1 (controlled by biasing currents I_{cont2} and I_{cont3}, respectively) can be regarded as *bifurcation* parameters, because their continuous variation over well defined ranges allows observation of the different dynamic states around the double-scroll attractor (nominal point of our oscillator at the behavioral design space).

B_p, m_0 and m_1

6. References

Aihara, K., Takabe, T. & Toyoda, M. [1990] "Chaotic Neural Networks," *Phys. Lett.* **A144**, 333-340.

Bernstein, G. M. & Lieberman, M. A. [1990] "Secure Random Number Generation Using Chaotic Circuits," *IEEE Trans. on Circuits and Systems* **37**(9), 1157-1164.

Carroll, T. L. & Pecora, L. M. [1991] "Synchronizing Chaotic Signals," *IEEE Trans. on Circuits and Systems* **38**(4), 453-456.

Chua, L. O., Komuro, M. and Matsumoto, T. [1986] "The Double Scroll Family -- Part I: Rigorous Proof of Chaos, and Part II: Rigorous Analysis of Bifurcation Phenomena," *IEEE Trans. on Circuits and Systems* **33**(11), 1072-1118.

Chua, L. O. (Guest Editor) [1987] "Special Issue on Chaotic Systems," *Proceedings of the IEEE* **75**(8).

Chua, L. O. & Lin, G. N. [1990] "Canonical Realization of Chua's Circuit Family," *IEEE Trans. on Circuits and Systems* **37**(7), 885-902.

Chua, L. O. [1992] "The Genesis of Chua's Circuit," *Int. J. Electronics Communications* **46**(4), 250-257.

Chua, L. O. [1993] "Global Unfolding of Chua´s Circuit," *IEICE Trans. on Fundamentals* **E76-A**(5), 704-734.

Chua, L. O. & Hasler, M. (Guest Editors) [1993] "Special Issue on Chaos in Nonlinear Elec-

tronic Circuits," Part A: Tutorials and Reviews, *IEEE Trans. on Circuits and Systems*-I **40**(10); Part B: Bifurcation and Chaos, *IEEE Trans. on Circuits and Systems*-I **40**(11); Part C: Applications, *IEEE Trans. on Circuits and Systems*-II **40**(10).

Chua, L. O., Wu, C. W., Huang, A. & Zhong, G.-Q. [1993] "A Universal Circuit for Studying and Generating Chaos -- Part I: Routes to Chaos, and Part II: Strange Attractors," *IEEE Trans. on Circuits and Systems*-I **40**(10), 732-761.

Cruz, J. M. & Chua, L. O. [1993] "An IC Chip of Chua's Circuit," *IEEE Trans. on Circuits and Systems*-II **40**(10), 614-625.

Delgado-Restituto, M., Rodríguez-Vázquez, A., Espejo, S. & Huertas, J. L. [1992] "A Chaotic Switched-Capacitor Circuit for $1/f^{\gamma}$ Generation," *IEEE Trans. on Circuits and Systems* **39**(4), 325-328.

Delgado-Restituto, M., Medeiro, F. & Rodríguez-Vázquez, A., [1993] "Nonlinear Switched-Current CMOS IC for Random Signal Generation," *Electronic Letters* **29**(25), 2190-2191.

Delgado-Restituto, M. & Rodríguez-Vázquez, A., [1994] "Switched-Current Chaotic Neurons," *Electronic Letters* **30**(5), 429-430.

Freeman, W. J. [1992] "Tutorial on Neurobiology: From Single Neurons to Brain Chaos," *Int. J. Bifurcation and Chaos* **2**(3), 451-482.

Hasler, M. [1994] "Synchronization Principles and Applications". *Proc. of the* 1994 *IEEE Int. Symp. on Circuits and Systems (Tutorials)*, Chapter **6.2**, 314-327.

Hein, S. [1993] "Exploiting Chaos to Suppress Spurious Tones in General Double-Loop SD Modulators," *IEEE Trans. on Circuits and Systems*-II **40**(10), 651-659.

Horio, H. & Suyama, K. [1995] "Experimental Verification of Signal Transmission Using Synchronized SC Chaotic Neural Networks," *IEEE Trans. on Circuits and Systems*-I **42**(7), 393-395.

Kocarev, L. J., Halle, K. S., Eckert, K., Parlitz, U. & Chua, L. O. [1992] "Experimental Demonstration of Secure Communications via Chaotic Synchronization," *Int. J. Bifurcation and Chaos* **2**(4), 709-713.

Madan, R. N. (editor) [1993] *Chua's Circuit: A Paradigm for Chaos* (World Scientific, Singapore).

Matsumoto, G., Aihara, K., Hanyu, Y., Takahashi, N., Yoshizawa, S. & Nagumo, J. [1987] "Chaos and Phase Locking in Normal Squid Axons," *Phys. Lett.* **A123**, 162-166.

McGonigal, G. C. & Elmasry, M. I. [1987] "Generation of Noise by Electronic Iteration of the Logistic Map," *IEEE Trans. on Circuits and Systems* **34**(8), 981-983.

Murch, A. R. & Bates, R. H. T. [1990] "Colored Noise Generation through Deterministic Chaos," *IEEE Trans. on Circuits and Systems* **37**(5), 608-613.

Nozawa, H. [1992] "A Neural Network Model as a Globally Coupled Map and Applications based on Chaos," *Chaos* **2**(3), 377-386.

Oppenheim, A. V., Wornell, G. W., Isabelle, S. H. & Cuomo, K. M. [1992] "Signal Processing in the Context of Chaotic Signals," *Proc. IEEE Int. Conf. on Acoustics, Speech and Signal Processing* IV, 117-120.

Rodríguez-Vázquez, A., Huertas, J. L., Rueda, A., Pérez-Verdú, B. & Chua, L. O., [1987] "Chaos from Switched-Capacitor Circuits: Discrete Maps". *Proceedings of the IEEE* **75**(8), 1090-1106.

Rodríguez-Vázquez, A., Espejo, S., Huertas, J. L. & Martin, J. D. [1990] "Analog Building Blocks for Noise and Truly Random Number Generation in CMOS VLSI," *Proc. European Conf. on Solid-State Circuits*, 225-228.

Rodríguez-Vázquez, A., Delgado-Restituto, M., Espejo, S. & Huertas, J. L. [1991] "Switched Capacitor Broadband Noise Generator for CMOS VLSI," *Electronic Letters* **27**(21), 1913-1915.

Rodríguez-Vázquez, A. & Delgado-Restituto, M. [1993] "CMOS Design of Chaotic Oscillators Using State Variables: A Monolithic Chua's Circuit," *IEEE Trans. on Circuits and Systems*-II **40**(10), 596-613.

Rodríguez-Vázquez, A. & Delgado-Restituto, M. [1994] "Generation of Chaotic Signals using Current-Mode Techniques," *J. of Intelligent and Fuzzy Systems* **2**(1), 15-37.

Schreier, R. [1991] "*Noise-Shaped Coding*," Ph. D. Thesis, University of Toronto.

FIGURE CAPTIONS

Fig. 1. (a) Chip architecture; (b) Experimental setup showing oscilloscope, chip with four tuning resistors, and the battery pack.

Fig. 2. Nonlinearity of the chaotic oscillator.

Fig. 3. Variation of the PWL characteristics of the nonlinearity with: (a) I_{cont1}; (b) I_{cont4}; (c) the central slope, m_0 (control variable I_{cont2}); and (d) the outer slopes, m_1 (control variable I_{cont3}).

Fig. 4. Automatic Tuning Mechanism.

Fig. 5. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.0\ \mu A$, $I_{cont3} = 2.35\ \mu A$.

Fig. 6. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.04\ \mu A$, $I_{cont3} = 2.35\ \mu A$.

Fig. 7. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.065\ \mu A$, $I_{cont3} = 2.35\ \mu A$.

Fig. 8. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.07\ \mu A$, $I_{cont3} = 2.35\ \mu A$.

Fig. 9. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.12\ \mu A$, $I_{cont3} = 2.35\ \mu A$.

Fig. 10. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.135\ \mu A$, $I_{cont3} = 2.35\ \mu A$.

Fig. 11. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.15\ \mu A$, $I_{cont3} = 2.35\ \mu A$.

Fig. 12. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.24\ \mu A$, $I_{cont3} = 2.47\ \mu A$.

Fig. 13. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.47\ \mu A$, $I_{cont3} = 2.56\ \mu A$.

Fig. 14. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.62\ \mu A$, $I_{cont3} = 2.56\ \mu A$.

Fig. 15. Experimental Lissajous figures, state waveforms, and power spectrum of the

x_1 variable for $I_{cont2} = 1.60\ \mu A$, $I_{cont3} = 2.58\ \mu A$.

Fig. 16. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.65\ \mu A$, $I_{cont3} = 2.61\ \mu A$.

Fig. 17. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.70\ \mu A$, $I_{cont3} = 2.61\ \mu A$.

Fig. 18. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.72\ \mu A$, $I_{cont3} = 2.63\ \mu A$.

Fig. 19. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.79\ \mu A$, $I_{cont3} = 2.66\ \mu A$.

Fig. 20. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.81\ \mu A$, $I_{cont3} = 2.66\ \mu A$.

Fig. 21. Experimental Lissajous figures, state waveforms, and power spectrum of the x_1 variable for $I_{cont2} = 1.85\ \mu A$, $I_{cont3} = 2.66\ \mu A$.

Fig. 22. (a) Experimental setup for an x_1-linear coupling synchronization scheme; (b)-(c) Correlation indexes between $x_{12,\,buf} - x_{22,\,buf}$ and $x_{13,\,buf} - x_{23,\,buf}$, respectively.

Fig. 23. Synchronization performance of the x_1-linear coupling system for $R_1 = 200\text{k}\Omega$.

Fig. 24. Measurements from an x_2-linear coupling synchronization scheme. (a)-(b) Correlation indexes between $x_{11,\,buf} - x_{21,\,buf}$ and $x_{13,\,buf} - x_{23,\,buf}$, respectively. (c)-(d) Synchronization performance for $R_2 = 25\text{k}\Omega$.

Fig. 25. (a) Master-Slave simplified experimental setup; (b)-(c) Measured performance.

Fig. 26. Synchronization performance of the x_2-drive system.

Fig. 27. (a) Simplified experimental setup for the inverse system approach; (b) Measured performance.

Fig. 28. Power spectra of the (a) input signal; (b) transmitted signal; and (c) recovered signal.

Fig. 29. Time-domain performance of the chaotic modulation synchronization scheme using two integrated prototypes.

Fig. 30. Correlation index between the input and the recovered signals.