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Dual feedback IRC ring for chaotic waveform generation

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Abstract

The authors have proposed an inverter resistor capacitor (IRC)-based simple chaotic ring oscillator with dual feedback for the generation of the chaotic waveform. The proposed chaotic system uses three coupled autonomous first-order differential equations and it can be electrically demonstrated using the complementary metal oxide semiconductor (CMOS) inverters with few passive RC elements for the generation of the high-frequency strange attractor. The basic dynamical characteristics and multistability property with complex bifurcation pattern in a wide range of parameters are well observed through theoretical as well as numerical simulation analysis using scaled inverse tangent function. In addition, a simple IRC chaotic model design is investigated using 0.18μm MOS transistor parameters with grounded capacitors and an equivalent CMOS-based scaled inverse tangent function. Moreover, the Cadence post layout simulation gives useful information about the circuit sustainability for IC design with high frequency (MHz), low power dissipation (940 μW) and small chip area (826.3 μm^2).

1 | INTRODUCTION

A simple electronic circuit implementation of an autonomous chaotic system has been an active research area in the field of chaos theory since its inception. A system with complex behaviour in the three-dimensional phase space has been illustrated by a set of ordinary differential equations which contains at least one nonlinear function. Over the past few decades, many chaotic systems specifically, the Lorenz and Rossler system [1, 2], the Chua's circuit [3, 4], the hysteresis chaotic oscillator [5, 6], chaotic jerk [7–10] and many more are reported in scientific study. The current scenario of electronics world uses unpredictable nature of chaotic waveform which is suitable for secure communication [11, 12] in VLSI integration.

An electrical implementation of most of the scientific study comes with conventional operational amplifier (Op-Amp) with excess number of passive components with large chip area, high power dissipation in comparison to advance analogue building block in chaotic circuits [13–26]. However, a monolithic implementation of canonical mathematical model for generation of chaotic waveform using commercially available components as well as complementary metal oxide semiconductor (CMOS)-based operational transconductance amplifier (OTA) with comparator [13] and inverter [14] are well depicted. Also, a circuit implementation with two CMOS ring oscillator with a pair of diode is reported in [15, 16]. After the advent of Chua's system, a large number of scientific studies have been reported on different methods for the realisation of chaotic circuit using current feedback operational amplifier (CFOA) in the study [17, 18]. However, some other available designs for chaotic circuitry based on CMOS active blocks are OTA [19], current conveyor (CCII) [20], dual output second generation current conveyor (DO-CCII) [21] and differential voltage current conveyor transconductance amplifier (DVCCTA) [22] and few more. These low-frequency chaotic oscillator circuits consist of numerous electronic components and transistors to realise the active inductor and nonlinear element. Moreover, some attractive implementation approaches of chaotic system are also available as bipolar junction transistor (BJT) based R-C chaotic oscillator [23, 24], CMOS chaotic jerk circuit [25], simple implementation of high frequency hyperchaotic circuit [26, 27] and bistable nonvolatile elastic-membrane memcapacitor exhibiting a chaotic behaviour [28] with less number of components.

The dissipative chaotic flow with multistability property is an exceptional case in the chaos theory. Such systems are very limited in study [29–31] and found unwanted in some

situations. Any sudden change in the states with parameters or external disturbance produces a new stable situation from the desired state and useful in chaos based secure communication systems. On the other side, the availability of such new low-frequency system uses more number of quadratic nonlinearity function and multiplying terms [29, 30], that make the system equation more complex and difficult to implement for monolithic design. However, a simple implementation of chaotic oscillator utilised hysteresis property of Op-Amp with only few passive components in [31].

The major challenge for the design of high frequency low power chaotic system with multistable property must have a simple implementation without passive inductor and multiplier. Thus, the main aim of this research article is to bring a new design for the implementation of chaotic circuit with minimum number of active and passive components count using fundamental IRC element. The major advantage of CMOS inverter based chaotic circuit provides an ease of integration for both analogue and digital perspective. A process parameter with 0.18 μm CMOS technology is used for CMOS inverter. The workability test of the proposed chaotic system is well verified using numerical analysis (MATLAB) as well as post layout simulation using a Cadence's Virtuoso tool.

2 | CIRCUIT DESCRIPTION

The proposed dual feedback loop ring oscillator based on third-order chaotic system can be demonstrated as a block diagram in Figure 1(a). Here, (x_1, x_2, x_3) represents the consecutive output of the first-order low pass RC filter with adjustable nonlinear element $f(x)$. An IRC based simple CMOS chaotic wave generator is shown in Figure 1(b) and mathematically characterised by following a set of voltage differential equations as:

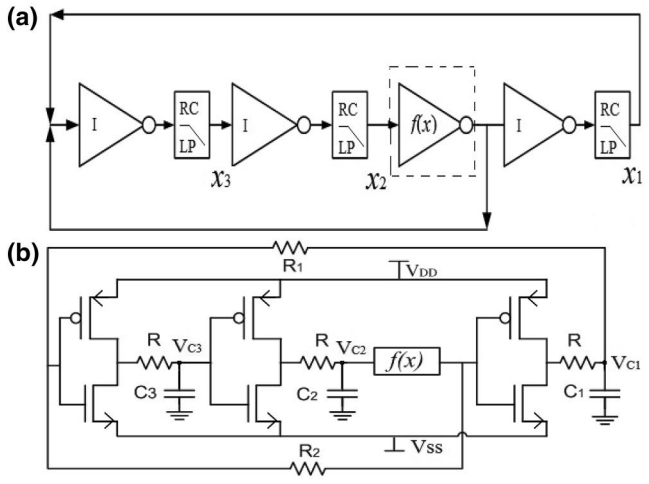

FIGURE 1 Proposed chaotic system: (a) block diagram and (b) CMOS IRC chaotic system with grounded capacitor

$$\left.\begin{aligned} RC_1\frac{dV_{C1}}{dt} &= -aV_{C1} + bf(x) \\ RC_2\frac{dV_{C2}}{dt} &= -V_{C3} - V_{C2} \\ RC_3\frac{dV_{C3}}{dt} &= -cV_{C1} - df(x) - V_{C3} \end{aligned}\right\} \quad (1)$$

where constant terms are $a = (\frac{R+R_1}{R_1} \quad -\frac{RR_2}{R_1(R_1+R_2)})$, $b = (\frac{R}{(R_1+R_2)} - 1), c = \frac{R_2}{R_1+R_2}, d = \frac{R_1}{R_1+R_2}$.

The proposed circuit topology uses an IRC based ring oscillator with dual feedback in which one is used to establish the regular periodic oscillations using inverted phase while the other one provides in-phase feedback. Here, the charging and the discharging phenomena of capacitors with the CMOS inverter exhibit very interesting dynamical phenomena that will cause an incremental and decremental change in voltage and current. The implementation of proposed circuit using few resistor, CMOS inverter and RC pair makes a simple design in comparison to available study of chaotic circuit [3–29]. In order to exhibit chaos, an autonomous circuit requires at least one nonlinear element. The proposed design uses an inverter as a simple nonlinear circuit which is equivalent to scaled inverse tangent function ($0.5 - 0.5tanh(10 * V - 5)$) and provides nonlinear behaviour with parameter variation. This proposes a scaled realisation of basic inverter (Figure 2(a)) as a nonlinear element $f(x)$ and Figure 2(b) is examined where the bistable operation of a modified CMOS inverter works as a nonlinear function. It fulfils the requirement of chaotic oscillation without using more number of external components for nonlinear element as compared to Chua's circuit [3, 4], hysteresis chaotic oscillator [5, 6] and chaotic jerk [7–10], CMOS ring oscillator [15, 16].

In general, output of basic inverter switched from high bias voltage (V_{DD}) to low bias voltage (V_{SS}) by appropriate input that contributes the transition of inverter output. The switching threshold voltage (V_{th}) is also known as midpoint voltage (V_{mid}) where output voltage of inverter approaches for same input voltage. Thus, if the switching threshold voltage (V_{th}) is not equal to the V_{mid} then one of the transistors will be in triode region which causes the nonlinearity in the proposed chaotic system. In order to calculate the V_{th} as a function of electrical parameter of MOS by assuming transistor in saturation region and short circuit power dissipation condition ($V_{th} < V_{in} < V_{DD} - |V_{thp}|$) given $I_{Dn} = I_{Dp}$ as:

$$k_n(V_{th} - V_{thn})^2 = k_p(V_{DD} - V_{th} - |V_{thp}|)^2 \quad (2)$$

where $k_n = \frac{\mu_n C_{ox}}{2}(\frac{W}{L})_n$ and $k_p = \frac{\mu_p C_{ox}}{2}(\frac{W}{L})_p$. By assuming a common input voltage ($V_{in} = V_{th}$) yields the common voltage as a midpoint voltage V_{th} as:

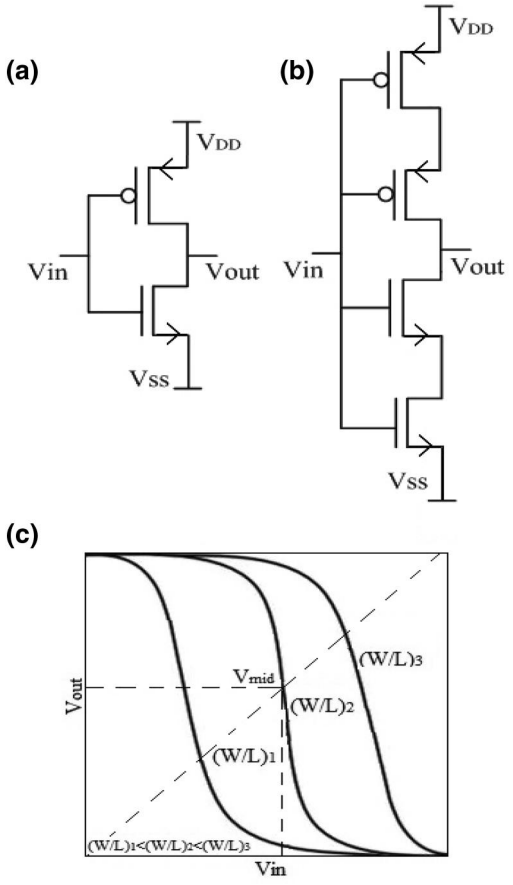

FIGURE 2 Nonlinear element: (a) basic CMOS inverter, (b) proposed nonlinear element and (c) input-output characteristic for different aspect ratio (W/L)

$$V_{th} = \frac{V_{DD} - V_{tp} + V_{tn}\left(\frac{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_n}{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_p}\right)^{-1/2}}{1 + \left(\frac{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_n}{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_p}\right)^{-1/2}} \tag{3}$$

Moreover, for a matched transistor and a typical assumption for ideal symmetric inverter by using $\mu_n = \mu_p$ and $V_{tn} = |V_{tp}|$ give the midpoint voltage (V_{tn}) as $V_{DD}/2$. In practical terms, mobility and threshold voltages are important as they vary due to the fabrication process imperfections. So, it is almost impossible to set the V_{th} to $V_{dd}/2$ with infinite precision and always some nonlinearity exists which may cause the chaotic behaviour. Furthermore, the nonlinear characteristic of the nonlinear function $f(x)$ can be adjusted with the input voltage and the aspect ratio. By utilising input voltage without any load in the inverter $f(x)$, yields transconductance of N-channel metal oxide semiconductor (NMOS) and P-channel metal oxide semiconductor (PMOS) as: $g_{mn} = \delta I_{ds}/\delta V_{gs}$, and $g_{mp} = \delta I_{sd}/\delta V_{sg}$. Then, the output of $f(x)$ as a current output I_{out} was observed as I_{Dp}–I_{Dn}. By differentiating current output w.r.t. voltage gives the transconductance terms g_m as:

$$g_m = -\frac{\delta I_{Dp}}{\delta V_{sg_p}} - \frac{\delta I_{Dn}}{\delta V_{gs_n}} = -g_{mp} - g_{mn} \tag{4}$$

It should be noted that g_{mn} increases when input increase ($V_{gs_n} = V_{in}$) and g_{mp} decreases when input increase ($V_{sg_p} = V_{dd} - V_{in}$). So the overall characteristic of the inverter will change w.r.t the capacitor voltage (V_C) and is accomplished by the charging and discharging of the capacitor. Moreover, tuning of aspect ratio (W/L) will cause a significant change in resistance value. Here, the inverter $f(x)$ contributes a variable resistance termed as drain-to-source resistance (r_{ds}) and can be formulated in linear mode as:

$$r_{ds} = \frac{-1}{k_n(V_{gs} - V_{th} - V_{ds})_n + k_p(V_{gs} - V_{th} - V_{ds})_p} \tag{5}$$

In the linear mode, r_{ds} depends on the gate voltage as V_{in} that allocates control over r_{ds}. According to the proposed concept, r_{ds} has to vary with respect to V_{in}. Channel length (L) and width (W) are also an important parameter which also affects the inverter characteristics and needs to be scaled according to the output swing in order to convert the single attractor to a strange attractor. A modified inverter, as shown in Figure 2(b), uses a nonlinear element. However, strange attractor may be achieved by using transistor sizing. The device sizing may increase $f(x)$ which will give more complex chaotic behaviour. Figure 2(c) shows input output characteristics of modified inverter with variation of aspect ratio, as the W/L increases or decreases the V_{mid} shifted towards the high bias voltage (V_{DD}) or low bias voltage (V_{SS}).

3 | MATHEMATICAL MODEL AND STABILITY ANALYSIS

The set of three differential equations of the proposed design in Equation (1) is modelled in terms of three state variables (x_1, x_2 and x_3) for basic dynamical analysis. The state space analysis of the proposed model can be approximated by the following scale variable and control parameters as $x_1 = Vc_1/V_T, x_2 = Vc_2/V_T, \quad x_3 = RI_L/V_T, \alpha = aC_2/C_1$, $\beta = bC_2/C_1, \gamma = cC_2/C_3, \ \kappa = dC_2/C_3), \ \tau = t/RC_2$. The mathematical model in terms of the state variables for numerical analysis of the proposed chaotic system brings the following set of equation as:

$$\left.\begin{aligned} \dot{x_1} &= -\alpha x_1 + \beta f(x) \\ \dot{x_2} &= -x_3 - x_2 \\ \dot{x_3} &= -\gamma x_1 - \kappa f(x) - x_3 \end{aligned}\right\} \tag{6}$$

where control parameter values (α, β, γ, κ) are always positive. Here, the nonlinear function $f(x)$ represented by a scaled inverse tangent function as $0.5 - 0.5tanh(10 * x_2 - 5)$.

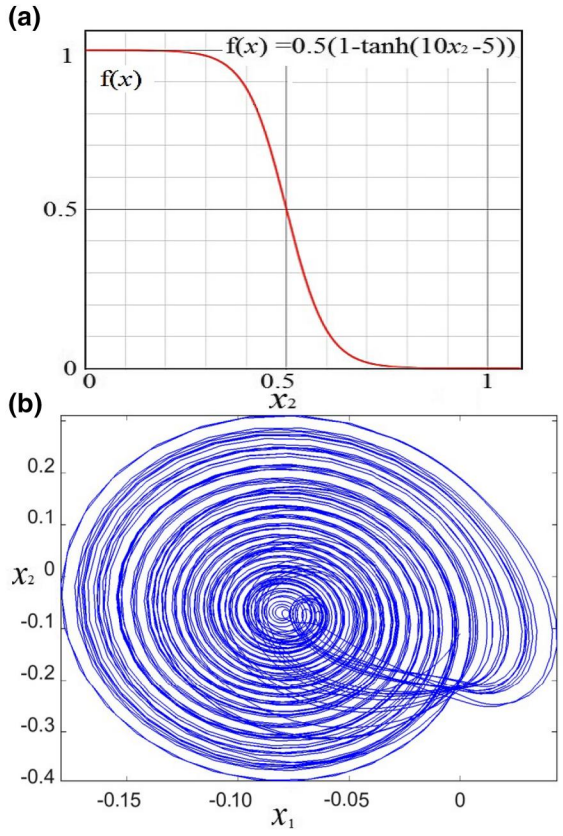

FIGURE 3 Numerical simulation result: (a) equivalent nonlinear function $f(x_2)$ plot and (b) a phase orbit in $x-y$ plane

Figure 3(a) shows an equivalent plot ($f(x_2)$w.r.t. x_2) for inverter input output characteristics (as in Figure 2(c)). To examine the chaotic behaviour, basic dynamic characteristics analysis of the proposed system will exhibit invariance properties for transformation of coordinate (x_1, x_2, x_3) to $(-x_1, -x_2, -x_3)$. One of the important properties termed as dissipativity can be characterised as:

$$\nabla V = \frac{\partial \dot{x_1}}{\partial x_1} + \frac{\partial \dot{x_2}}{\partial x_2} + \frac{\partial \dot{x_3}}{\partial x_3} = -(\alpha + 2) < 0 \tag{7}$$

Therefore, for all positive values of the α bring the system dissipative. Furthermore, by putting condition $(\dot{x_1} = \dot{x_2} = \dot{x_3} = 0)$ in Equation (7) gives the equilibrium point of the chaotic system. We have found that system enables multiple equilibrium point $E_{f(x)}$ $((\beta/\alpha)f(x), (\beta\gamma/\alpha + \kappa)f(x), -(\beta\gamma/\alpha + \kappa)f(x))$ which depends on the control parameter and nonlinear function. A stability analysis at $E_{f(x)}$ can be carried out using the corresponding Jacobian matrix as:

$$[J] = \begin{bmatrix} -\alpha & \beta f'(x) & 0 \\ 0 & -1 & -1 \\ -\gamma & -\kappa f'(x) & -1 \end{bmatrix} \tag{8}$$

Moreover, the eigenvalues of the Jacobian matrix yields the characteristic equation $|J - \lambda I|$ at $E_{0,1}$ as:

$$\lambda^3 + (2+\alpha)\lambda^2 + (1 + 2\alpha - \kappa c')\lambda + (\alpha - c'(\kappa\alpha + \gamma\beta)) = 0 \tag{9}$$

where, $c' = f'(x)$. For example, let $f(x)$ equal to -1 and 1 gives the solution for the characteristic polynomial Equation (11) as $(-2.53, -0.231 \pm 0.932i)$ and $(-1, -1, -0.7)$ with instance control parameter ($\alpha = 1$, $\beta = 2.5$, $\gamma = 0.9$, $\kappa = 0.9$) which supports both stable equilibrium. It gives the proof of multistability property at different equilibriums of the proposed system as [29, 30]. On the other hand, an alternative proof of chaoticity with parametric values ($\alpha = 1$, $\beta = 2.5$, $\gamma = 0.9$, $\kappa = 0.09$) and initial condition (0.1031, 0.3556, -0.356) generates the Lyapunov exponents (0.025, 0, -2.05) with the Kaplan-Yorke dimension 2.018. A numerical simulation for phase orbit of single scroll in x_1-x_2 plane is shown in Figure 3(b). A series of investigation of the proposed chaotic system in Equation (7) by tuning individually α, β, κ or γ value by keeping other parameter constant produces bifurcation diagram as shown in Figure 4. In addition to the observed behaviour of the attractor w.r.t the initial condition, a plot of basin of attraction for the chaotic system with ($\alpha = 0.7, \beta = 2.5, \gamma = 0.9, \kappa = 0.09$) is shown in Figure 5 using numerical simulation in MATLAB. It informs different attraction regions for the initial condition in the $x_1(0)$ vs $x_2(0)$ initial plan with $x_3(0)$ equal to 0.1. Here, different colours in local basins of attraction represent the different chaotic states in two initial plane viz. *blue* region leads to periodic behaviour and *yellow* region leads to chaotic behaviour. Local basin of attraction in Figure 5 indicates the absence of strange attractors of the system with initial conditions near the origin. Therefore, strange attractor of the system is hidden.

4 | WORKABILITY TEST

An implementation of the theoretical chaotic model is validated for the practical feasibility using post layout simulation. The circuit of a continuous-time MOS IRC chaotic system is integrated with 0.18 μm CMOS technology parameter and well simulated in Cadence Virtuoso platform. Figure 6 shows the chaotic system which involves only active MOS resistor for ease of integration and the appropriate value of the resistance can be achieved by adjusting the value of V_{R1}, V_{R2} and V_R. To justify the theoretical investigation post layout simulation is performed with standard component values as $C_1 = 10$ nF, $C_2 = C_3 = 1$ nF, $R = 10\text{k}\Omega$, $R_2 = 2.5\text{k}\Omega$ and R_1 as a potentiometer of 1 kΩ as a dominant parameter. By tuning the value of R_1 from 100 Ω to 300 Ω, system nature changes from a period doubling to a chaos.

To justify the numerical simulation results more precisely, we have performed the advance simulation using Cadence Virtuoso tool comprising a post layout simulation. Figure 6 shows the post layout high frequency (up to MHz) time series waveform (V_{C1}, V_{C2} and V_{C2}) with R_1=190 Ω. Figure 7 is the post layout trajectories for single and double scroll (V_{C1} vs

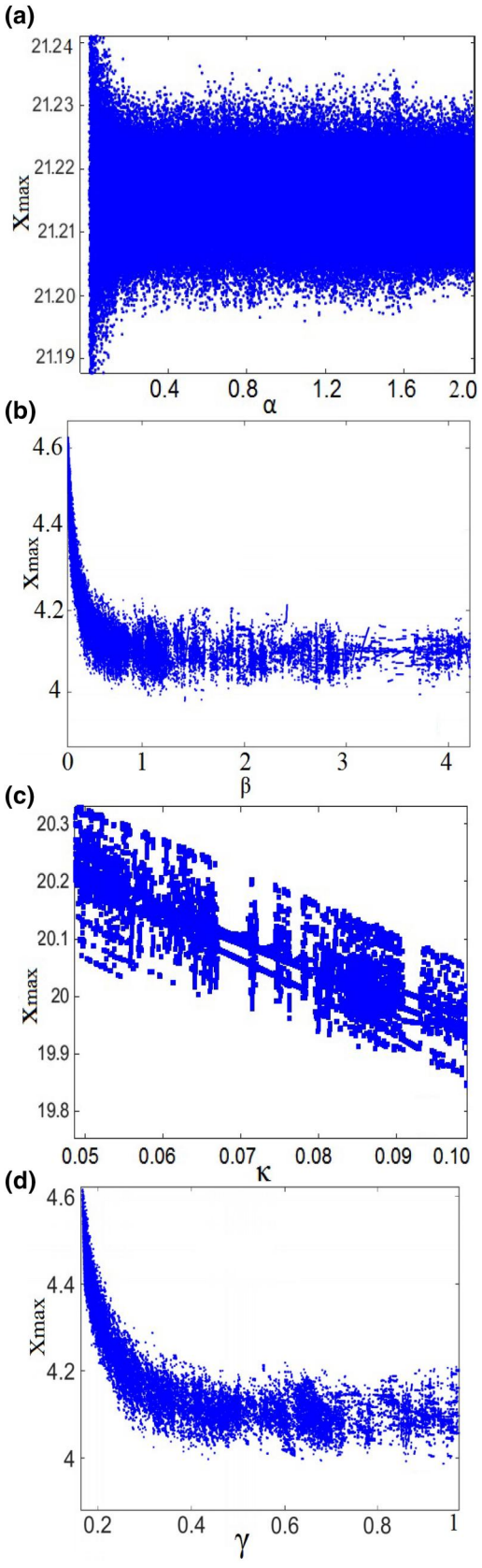

FIGURE 4 Bifurcation diagram of x_{max}: (a) α value by keeping the other parameter constant ($\beta = 2.5$, $\gamma = 0.9$, $\kappa = 0.09$), (b) β value by keeping other parameter ($\alpha = 0.7$, $\gamma = 0.9$, $\kappa = 0.09$) constant, (c) κ value by keeping other parameter ($\alpha = 0.7$, $\beta = 2.5$, $\gamma = 0.9$) constant and (d) γ value by keeping other parameter ($\alpha = 0.7$, $\beta = 2.5$, $\kappa = 0.09$) constant

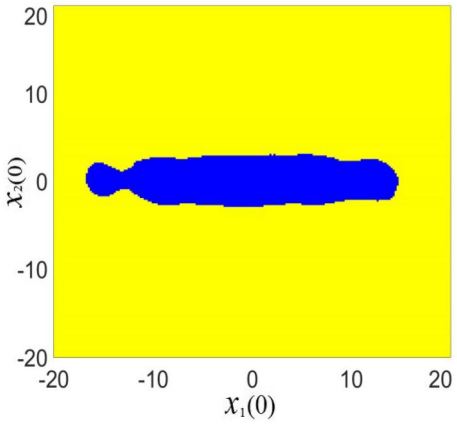

FIGURE 5 Local basins of attraction in two initial plane $x(0)$ vs $y(0)$ with ($\alpha = 0.7$, $\beta = 2.5$, $\gamma = 0.9$, $\kappa = 0.09$) and $x_3(0)$ equal to 0.1

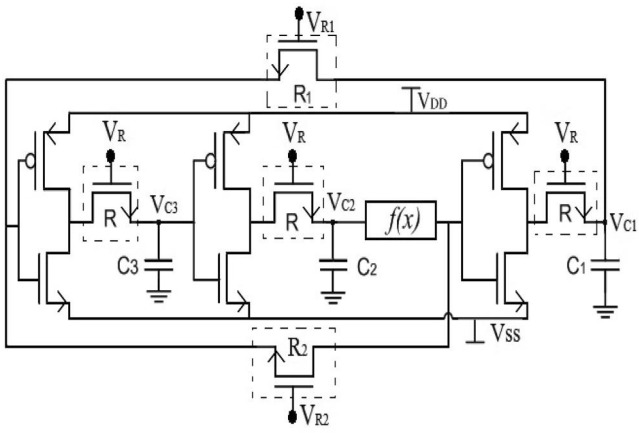

FIGURE 6 Proposed complete CMOS IRC chaotic system with grounded capacitor

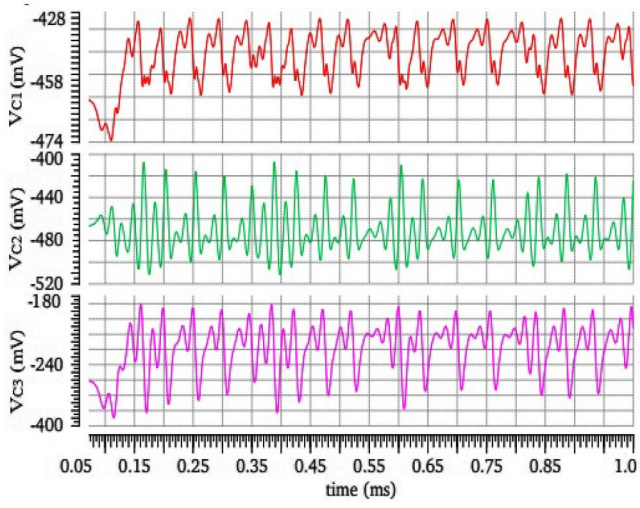

FIGURE 7 Post layout time series response (V_{C1}, V_{C2} and V_{C2}) with component value ($C_1 = 10$nF, $C_2 = C_3 = 1$ nF, $R_1 = 190\ \Omega$, $R_2 = 2.5$kΩ)

Reference	Components (active and passive)	Tech.	PC	Frequency	NF
[9] Figure 1	Op-Amp, 4A, 6R, 3C, 1D	4 μm	NA	Hz	exp()
[17] Figure 2	CFOA, 5A, 7R, 3C, T-NA	NA	NA	KHz	PWL
[19] Figure 1	OTA, 2A, 1R, 2C, 1LT78	2 μm	NA	KHz	PWL
[20] Figure 1	CCII, 1A, 3R, 3C, T-NA	BJT	NA	KHz	JFET
[21] Figure 2	DO-CCII, 4A, 7R, 3C, T56	BJT	120 mW	KHz	PWL
[22] Figure 10	DVCCTA, 3A, 6R,3C, T60	0.5 μm	17.7 mW	KHz	PWL
[23] Figure 1	BJT, 7R, 4C, T2	BJT	3.1 mW	KHz	bistable
[24] Figure 1	CMOS, 2R, 3C,1L, T1	0.18 μm	NA	KHz	exp()
[25] Figure 1	CMOS, 1R, 3C, T24	0.18 μm	0.72 mW	MHz	tanh()
[26] Figure 2	OTRA, 1A, 1R, 3C, 1L, 2D, T14	0.25 μm	23 mW	MHz	cubic
Prop. Figure 1	MOS, 3C, 5R, T10	0.18μm	940μW	MHz	tanh()

TABLE 1 Performance comparison with MOS based chaotic circuit

Tech, technology parameter (CMOS); PC, power consumption; A, number of active blocks; R, resistor; C, capacitor; L, inductor; D, diode; T, transistor count; FO, frequency of operation; NF, nonlinear function; PWL, piece-wise linear; NA, not available

V_{C2}) with $R_1 = 300\ \Omega$. The W/L for PMOS and NMOS is 2.4 μm / 0.18 μm and 4.8 μm / 0.36 μm for the generation of single and double scroll, respectively. The total area of the present layout and the power consumption is observed as 826.29 μm^2 and 940 μW for supply voltage of ±1.25V respectively. This post layout simulation result verification validates the proposed theoretical concept and also s follows the numerical simulation.

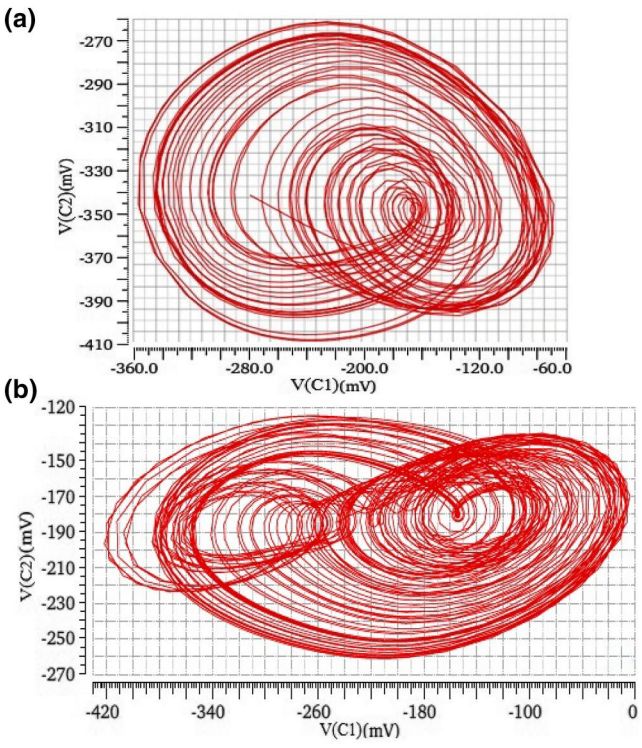

FIGURE 8 Post layout trajectories (V_{C1} vs V_{C3}) with component value (C_1 = 10nF, $C_2 = C_3$ = 1 nF and a R_1 = 190 Ω, R_2 = 2.7kΩb R_1 = 200 Ω, R_2 = 2.5kΩ)

The proposed IRC based chaotic system offers both Rossler and Lorenz like dynamics with minimum number of active and passive components in comparison to available scientific study. Table 1 gives a complete comparative study of the existing chaotic system with the proposed one in terms of active and passive components count, CMOS technology parameter, power dissipation, frequency of operation and nonlinear function. In addition, the proposed chaotic system does not require any external nonlinear element as in [9] and [17–26]. However, the proposed chaotic system utilises minimum number of transistor as compared to [9, 17, 19, 21, 22, 25, 26]. Moreover, a simple IRC chaotic circuitry using MOSFET dissipates very less power (μW) and is suitable for high frequency operation (MHz). In comparison to available hidden attractors with multistable property [29–31], the proposed design is free from multiplier term and passive inductor unlike [17, 19, 24, 26] and suitable for simple chaotic system with multistability property, less chip area and fully CMOS based design with only few grounded capacitors. Hence, the proposed design may be suitable for the monolithic integration.

5 | CONCLUSION

A new design of a simple MOS IRC ring oscillator-based chaotic system is implemented. The discovery of the proposed system with scaled inverse tangent function is striking, because of hidden attractor with a unique multistability property in an autonomous chaotic system. Various bifurcation diagrams are observed resulting in the formation of different types of chaotic attractors. The post layout simulation results follow numerical values and confirm the workability of the proposed chaotic model. It is important to note that proposed circuit provides the following attractive features as (i) simple and

versatile design, (ii) utilisation of CMOS, (iii) compact structure without the involvement of inductor, (iv) high frequency and low power dissipation and (v) fully CMOS chaotic system suitable for IC fabrication as compared to previously suggested chaotic circuits. A major advantage of a fully CMOS-based chaotic circuit is having an integration capability which will be fully applicable for the analogue, digital and mixed-mode design.

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