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Bifurcation and Chaos in CMOS Inverters Ring Oscillator

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ABSTRACT

In this paper, chaotic behavior which occur in CMOS inverters ring is described. A ring having three CMOS inverters operates with discrete time model has been used in this study. The chaotic behavior has been found in the presented inverters ring along with a variation of an external input. A circuit model for the presented inverters ring is proposed and confirmed by employing SPICE circuit simulator as well as by observing a breadboard composed of discrete components.

1. INTRODUCTION

There are many studies on chaotic behavior in nonlinear systems in the recent decade [1]-[6]. The nonlinear feedback system such as a pulsewidth modulated (PWM) system with a difference equation displays chaos if this equation has periodic solution of each period as described in [1]. The chaotic phenomena is also found in a negative resistance LC oscillator as shown in [2] and in a two cells or three cells autonomous system of cellular neural networks which exhibits the Hopf-like bifurcation as shown in [3]. Recently, a neuron model which exhibits chaotic behavior called chaotic neuron [4]-[6] has been investigated and can be implemented with several electronic circuit models. Such kind of chaotic neuron is employed to construct a chaotic neural networks which can be a possible implementation scheme for artificial neural networks [6]. In our study, we focus on a CMOS inverters ring as a target for observing the chaotic behavior. The targeted circuit model is composed of three CMOS inverters operates in discrete time. The chaotic behavior has been found in the presented inverters ring along with a variation of an external input. Due to based on discrete time operation, the model presented here is similar to the chaotic neuron model as described in [4]-[6]. However, the presented circuit structure is pretty simple and just composed of three CMOS inverters, two CMOS switches and a hold condenser. In the circuit, two CMOS switches and the hold condenser are employed to control the inverter ring operates in discrete time. The chaotic behavior in the presented inverters ring has been confirmed by employing SPICE as well as by observing a breadboard composed of discrete components.

2. CIRCUIT MODEL

At first, we would like to focus on the well known transfer characteristics of a CMOS inverter. The switching point of a CMOS inverter's transfer characteristics is typically designed to be a half of magnitude of the supply voltage (e.g. $\approx \frac{V_{DD}}{2}$). In ideal case, gain factors β_p of PMOS and β_n of NMOS transistors of a CMOS inverter are equivalently designed by adjusting a ratio of channel width-to-length ratio (W_p/L_p) of PMOS transistor and channel width-to-length ratio (W_n/L_n) of NMOS transistor. In a word, this ratio should be designed to cancel a difference between the mobilities of PMOS and NMOS transistors. During transition, both of PMOS and NMOS transistors are in saturation (momentarily turn on) and result a short pulse of current drawn from the power supply. A MOS device in saturation behaves like an ideal current source with drain to source current I_{ds} does not depend upon source to drain voltage V_{ds}. At the transition time, the PMOS and NMOS transistors are treated as two current source in series. We utilize this transfer characteristics of a CMOS inverter to generate the chaotic behavior. The circuit model of the presented ring oscillator is shown in Fig. 1. It consists of three CMOS inverters, two CMOS switches and a hold condenser C. An external input is applied to the output of the first CMOS inverter through a resistor R. Two CMOS switches which operate with a single phase $Clock$ and the hold condenser C are employed for controlling the ring oscillator operates with discrete time model. Due to operation with single phrase clock, the presented circuit operates with higher speed than the previous models [4],[6] at least two times.

3. SIMULATION AND OBSERVATION RESULTS

We have simulated the presented inverters ring employing SPICE (Bakerley version) circuit simulator. A 1μm standard CMOS technology process has been assumed for all simulations.

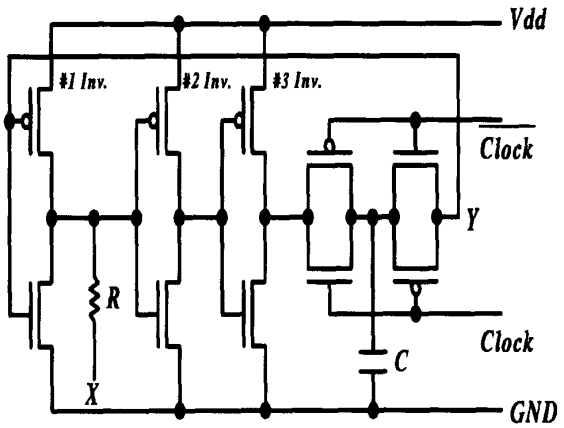

Fig. 1 Circuit model.

For convenient, we define a unit PMOS transistor has W_p=4μm , L_p=2μm and a unit NMOS transistor has W_p=2μm , L_p=2μm. The W_p is defined as twice larger than W_n for canceling the difference between μ_p of PMOS and μ_n NMOS transistors ($\mu_n \simeq 2\mu_p$). The value of hold condenser C is 1pF, resistor R for external input is 1.5KΩ and the frequency of sampling clock is 50MHz. Fig. 2 shows the simulation result of the occurred chaotic behavior through the output voltage Y in the presented inverters ring along with the variation of the external input voltage X (0V$\sim$5V). In this case, the first inverter of the inverters ring has designed having β_n/β_p=1 as a gain factor. Therefore, if we give to this first inverter that having various gain factors, the occurred chaotic area will appear in various areas according to the given gain factor to the first inverter. In a word, we are able to control the occurred chaotic area by controlling the gain factor of the first inverter, artificially. In order to control the gain factor of the first inverter, we employ an Analog-Digital-Balance (ADB) circuit [7] instead of this first inverter. The gain factor is controlled by 2-bit digital control code, that means we can obtain four different gain factors of the ADB circuit. ADB circuit is composed by 3 CMOS inverters connected in parallel as shown in Fig. 3. The channel conductances of PMOS pull-up and NMOS pull-down transistors of each CMOS inverter are equivalently designed and weighted by the channel width-to-length ratio (W/L). In order to utilize the analog portion of the DC transfer characteristic of a CMOS inverter operating in the transition region, the ADB circuit has two types of inputs. One is a digital code input (terminals: D_1,D_2) and the other an analog voltage input (terminal: X). The analog input voltage is translated into a quantized voltage between the supply voltage V_{DD} and the ground. For the PMOS pull-up and NMOS pull-down transistors of the

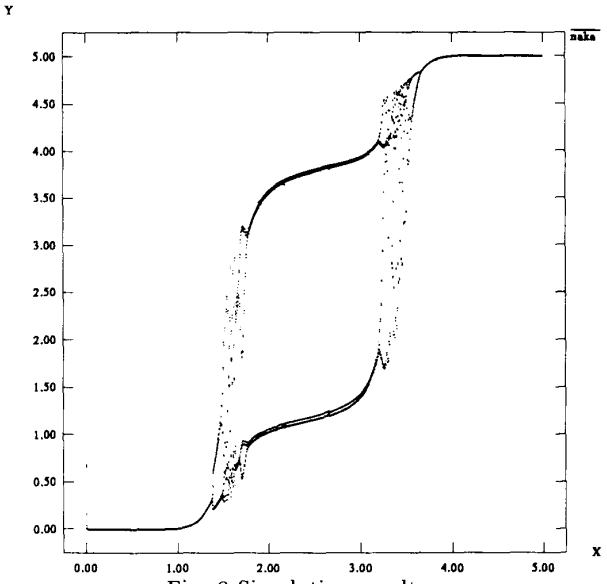

Fig. 2 Simulation result.

inverters having digital inputs, the given weights are non-overlap binary numbers of 1 and 2. For the PMOS pull-up and NMOS pull-down transistor of the inverter having an analog voltage input, the given weight is 4.

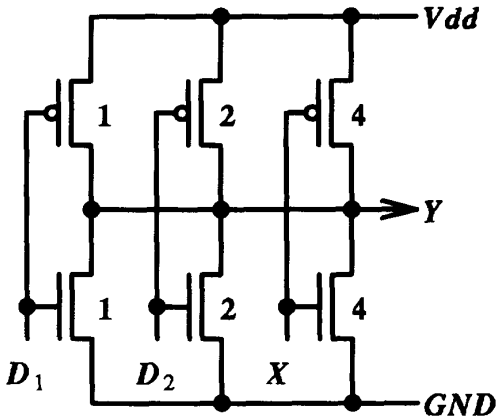

Fig. 3 Analog-Digital-Balance (ADB) circuit.

The ADB circuit can be treated as a CMOS inverter which has a superimposed channel conductance ratio $\frac{\beta_n}{\beta_p}$ as follows:

$$\frac{\beta_n}{\beta_p} = \frac{2^2 + \sum_{i=1}^{1} 2^{i-1} D_i}{2^2 + \sum_{i=1}^{2} 2^{i-1} \overline{D_i}} \quad . \tag{1}$$

Therefore, we can obtain $\frac{4}{7}, \frac{5}{6}, \frac{6}{5}$ and $\frac{7}{4}$ as the gain factors of the ADB circuit corresponding to four value 00, 01, 10 and 11 of digital control code of D_1 and D_2. Fig. 4 shows the simulation results of the occurred chaotic behavior of the presented inverters ring when the ADB circuit employed as the first inverter.

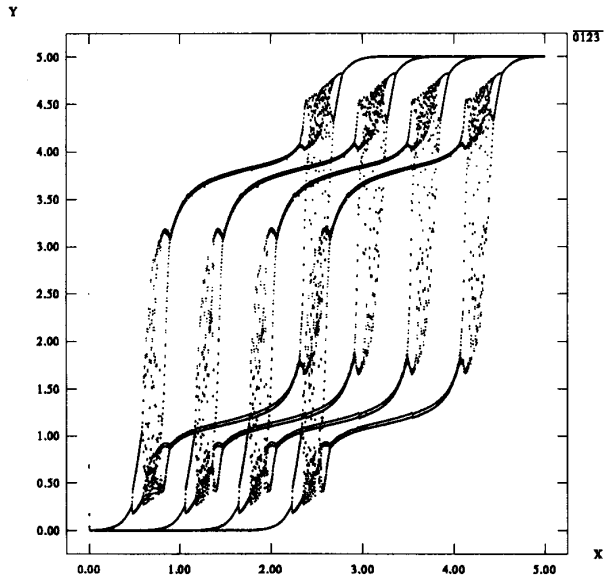

Fig. 4 Simulation results of inverters ring with ADB circuit.

We also have observed the chaotic behavior occurs in the presented inverter ring employing a breadboard composed of discrete components. The used hold condenser C is 200pF, resistor R for external input is 100Ω and the frequency of sampling clock is 2.5MHz. Figs. 5 and 6 show the chaotic behavior of the presented inverters ring along with the variation of external input X (0∼5V) when the gain factor of the first inverter is designed as 1. Figs. 7, 8, 9 and 10 show four chaotic behaviors of the presented inverters ring along with the variation of external input X (0∼5V) and four gain factors of $\frac{4}{7}, \frac{5}{6}, \frac{6}{5}$ and $\frac{7}{4}$ of the ADB circuit controlled by the digital code of D_1 and D_2. Fig. 11 shows the designed physical layout of the proposed inverters ring with the ADB circuit as the first inverter, employing a conventional 1μm double-metal CMOS process. The whole circuit contains only 16 transistors and has an area of 160μm×80μm.

4. CONCLUSION

We have described our CMOS inverters ring which displays the chaotic behavior. Since the circuit model is pretty simple, it is easy to design and define the gain factors of the CMOS inverters which control the occurring chaotic area. The presented circuit model having a simple structure runs with single phase clock makes it operates with over 50 times higher speed than the previous models. Also, the presented circuit model can be realized only with 16 transistors that makes it is possible to integrate a large number of these circuits for implementing the chaotic neural networks.

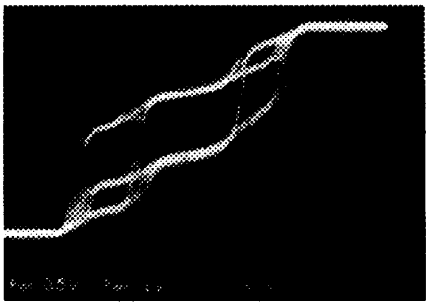

Fig. 5 Measurement result (gain factor: 1).

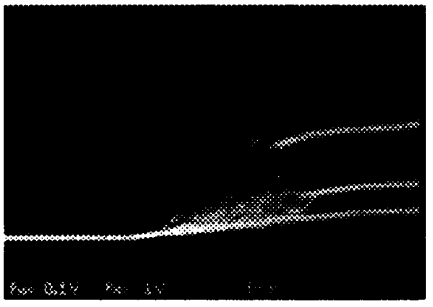

Fig. 6 Magnified.

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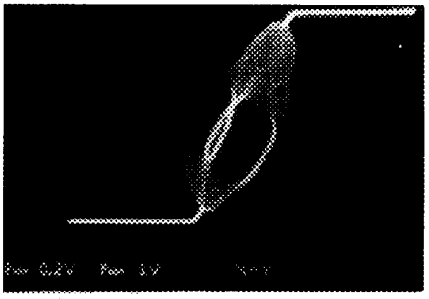

Fig. 7 Measurement result (gain factor: $\frac{4}{7}$).

Fig. 8 Measurement result (gain factor: $\frac{5}{6}$).

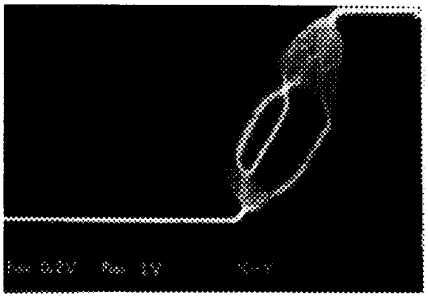

Fig. 9 Measurement result (gain factor: $\frac{6}{5}$).

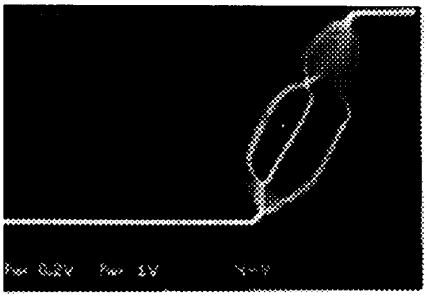

Fig. 10 Measurement result (gain factor: $\frac{7}{4}$).

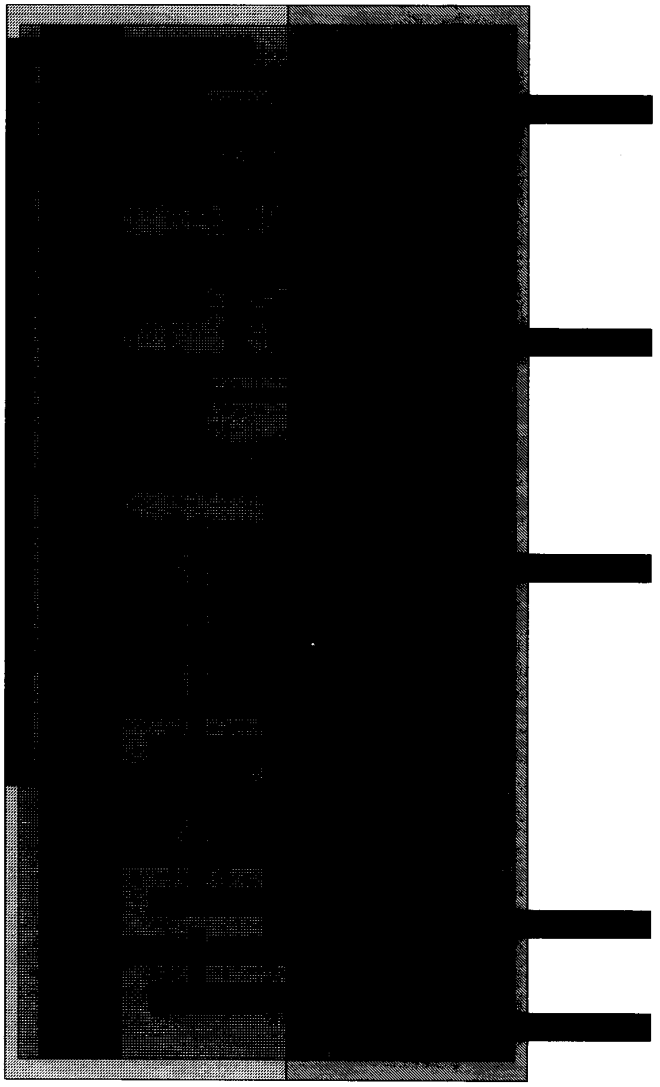

Fig. 11 Physical layout of inverters ring with ADB circuit.