Suzhou Huaxin Microelectronics Co., Ltd.

HuaXin Micro-electronics Co., Ltd

HS2300-P MCU

Reference book

Ver. 2.01F

Directoryrecord

1. Overview

The HS2300-P series is a low power, high speed, high noise margin, EPROM/ROM based on 8-bit CMOS process
The MCU uses the RISC instruction set and has a total of 42 instructions. The branch instruction is a single-cycle instruction except for two-cycle instru
This easy-to-use, easy-to-remember instruction set greatly reduces development time. The HS2300-P series includes a power-on reset (Power-on Reset)
POR), Brown-out Reset BOR, Power-up Reset Timer (WWRT), oscillation start
Oscillator Start-up Timer OST, Watchdog Timer, EPROM/ROM, SRAM,
Bidirectional tri-state I/O port (can be set to pull-up/pull-down, open-drain), power-saving sleep mode, 8-bit timing with 8-bit presetr/
Counter, independent interrupt, sleep wake mode and reliable code protection, there are two oscillator sources for user configuration options, including p
Oscillator source and low power oscillator.
The HS2300-P series can access 1K x 13 program memory space and can access registers directly or indirectly.
And the data memory area, all special function registers are distributed in the data storage area and contain specific program pointers.

2. Features

- 42 RISC instructions
- In addition to the program branch instruction is two cycles, all instructions are single cycle
- 13-bit wide instruction, 8-bit wide data path, 5-level deep hardware stack
- Support GOTO instruction full ROM jump
- Support full ROM subroutine call
- 1K × 13 program memory
- 49 × 8-bit general-purpose registers

◆ Operating speed: DC - 20 MHz clock input; DC - 100 ns instruction cycle
◆ Direct and indirect addressing modes
◆ 8-bit real-time clock/counter with 8-bit programmable prescaler (timer 0)
◆ Internal power-on reset circuit (POR), built-in low voltage detection (LVD) for Brown-out Reset (BOR)
◆ Power-on reset timer (PWRT) and oscillator start timer (OST)
◆ Watchdog Timer (WDT) uses internal crystal oscillator with high reliability and is enabled or disabled by software.
◆ Two groups of I / O ports IOA and IOB are controlled by independent instructions, and can be configured with pull-up, pull-down and open-drain
◆ Wake-up sleep: Input state change of INT pin or port B realizes sleep wake-up
◆ Power-saving sleep mode, programmable code protection
◆ Optional oscillator option: ERC: External RC Oscillator
IRC: Internal RC Oscillator
ERIC: External Resistor Internal Capacitor Oscillator
LF: low speed crystal
HF: high speed crystal
◆ Wide operating voltage range: 2.3V to 5.5V

Feature selection list

CHIP	ROM (Byte)	RAM (Byte)	Stack	I/O	Package
HS2300-P	1K*13	49	5	12	SOP14/DIP14
	1K*13	49	5	6	SOP8/DIP8

3. Pin information

3.1 pin diagram

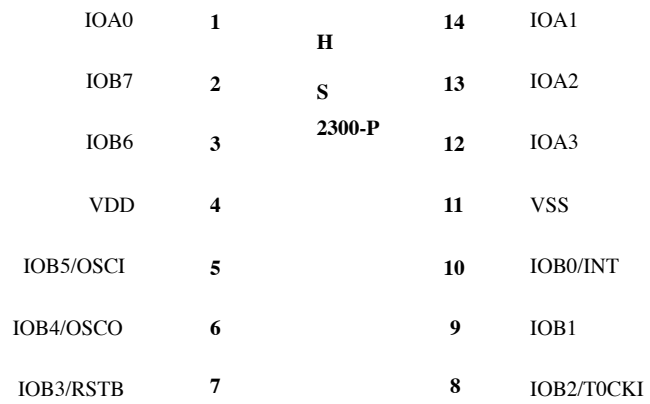


Figure 3.1 Pin Information (14PIN)

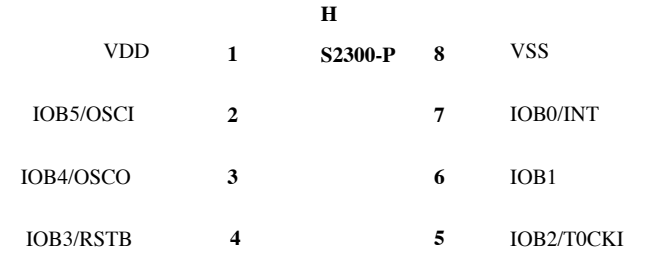


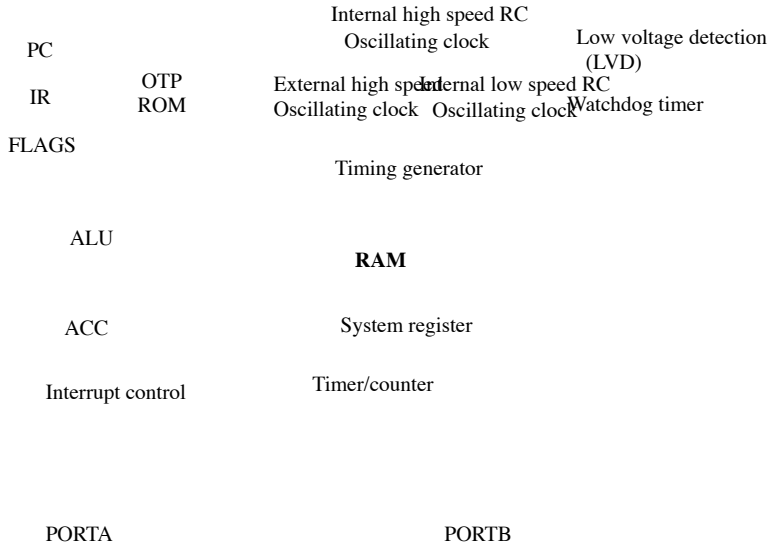
Figure 3.2 Pin Information (8PIN)

3.2 pin description

name	Types of	Description
IOA0~ IOA3	I/O	1. General I/O port 2. Configurable pull-down resistor
IOB0/INT	I/O	1. General I/O port 2. Configurable pull-up/pull-down/open-drain function 3. Pin change causes the chip to wake up from sleep mode 4. Trigger interrupt generation by rising or falling edge Choose)
IOB1	I/O	1. General I/O port 2. Configurable pull-up/pull-down/open-drain function 3. Pin change causes the chip to wake up from sleep mode
IOB2/T0CKI	I/O	1. General I/O port 2. Configurable pull-up/pull-down/open-drain function 3. Pin change causes the chip to wake up from sleep mode 4. Timer input (select)
IOB3/RSTB	I/O	1. Input pin 2. System reset signal (active low) 3. Pin change causes the chip to wake up from sleep mode 4. Configurable as open drain output
IOB4/OSCO	I/O	1. General I/O port 2. Configurable pull-up/drain open function 3. Pin change causes the chip to wake up from sleep mode 4. Oscillator output pin (crystal mode cannot be set to pull up)
IOB5/OSCI	I/O	1. General I/O port 2. Configurable pull-up/drain open function 3. Pin change causes the chip to wake up from sleep mode 4. Oscillator input pin (crystal mode cannot be set to pull up)
IOB6~IOB7	I/O	1. General I/O port 2. Configurable pull-up/drain open function 3. Pin change causes the chip to wake up from sleep mode
VDD	P	System power input
VSS	P	System ground input

Note: I: output; O: input; P: power supply

4. System block diagram



5. Memory structure

The HS2300-P memory is divided into program memory and data memory.

5.1 program memory structure

The HS2300-P has a 10-bit program counter PC that can address 1K*13 program memory. The chip reset vector is 3FFH.
The CALL/GOTO instruction addresses all program memory.
H/W interrupt vector address 008H., S/W interrupt vector address 002H. CALL/GOTO can point to the same program page All storage space (1K for one program page)
The program accessor and stack structure are shown below:

Program Counter PC<9:0>

Stack Stack 1
Stack Stack 2
Stack Stack 3
Stack Stack 4
Stack Stack 5

3FFH Reset vector
.
.

.
008H H/W interrupt vector
.
.
002H S/W interrupt vector

000H

5.2 data memory structure

The data memory of the HS2300-P consists of special function registers SFR and general purpose registers.
Indirect addressing is realized through the FSR register. Direct addressing is realized through the FSR register too

Table 5.1: Data Accessor Structure

address	Functional description	
00H	INDF	
01H	TMR0	
02H	PCL	N/A OPTION
03H	STATUS	
04H	FSR	
05H	PORTA	05H IOSTA
06H	PORTB	06H IOSTB
07H	General purpose register	
08H	PCON	
09H	WUCON	
0AH	PCHBUF	
0BH	PDCON	
0CH	ODCON	
0DH	PHCON	
0EH	INTEN	
0FH	INTFLAG	
10H~3FH	General purpose register	

Table 5.2: Special Function Register Addresses

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
00H(r/w)	INDF	Use the FSR's content addressing data registers (non-physical registers)							
01H(r/w)	TMR0	8-bit real-time timer counter							
02H(r/w)	PCL	The lower 8 bits of the PC							
03H(r/w)	STATUS	RST	GP1	GP0	T0	PD	Z	DC	C
04H(r/w)	FSR	*	*	Indirect addressing pointer					
05H(r/w)	PORTA	-	-			IOA3	IOA2	IOA1	IOA0
06H(r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
08H(r/w)	PCON	WDTE	EIS	LVDTE	*	*	*	*	*
09H(r/w)	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3		WUB2	WUB1 WUB0
0AH(r/w)	PCHBUF	-	-	-	-	-	-		
0BH(r/w)	PDCON		/PDB2	/PDB1	/PDB0	/PDA3		/PDA2	/PDA1 /PDA0
0CH(r/w)	ODCON	ODB7	ODB6	ODB5	ODB4			ODB2	ODB1 ODB0
0DH(r/w)	PHCON	/PHB7	/PHB6	/PHB5	/PHB4			/PHB2	/PHB1 /PHB0
0EH(r/w)	INTEN	GIE	*	*	*	*	INTIE	PBIE	T0IE
0FH(r/w)	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF

Note: "-" is not used, the read operation returns „0 "; “* ” is not used, and the read operation returns „1"

Table 5.3: Registers Controlled by OPTION or IOST Instructions

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
N/A(w)	OPTION	INTEDGE		T0CS	T0SE	PSA	PS2	PS1	PS0
05H(w)	IOSTA	Port A Input Output Control Register							
06H(w)	IOSTB	Port B Input Output Control Register							

6. Functional Description

6.1 working register

6.1.1 INDF (Indirect Addressing Register **)**

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
00H(r/w)	INDF	Use the FSR's content addressing data registers (non-physical registers)							

The INDF register is not a real physical register. Any instruction that uses the INDF register actually accesses the pointer register. The register pointed to by the device (FSR). If the INDF register is read using indirect addressing (FSR = '0'), the read is terminated. If it is 00H; use Indirect Addressing to write to the INDF register, the actual execution is a null operation, but it may affect the flag. Bit. Bits <5:0> of the FSR register can be used to select 64 registers (address: 00H~3FH).

Example 6.1: Indirect Addressing

- The value in register 28 is 10H.
- The value in register 29 is 0AH
- Put 28 into the FSR register
- Reading the INDF register will return 10H
- The value of the FSR register is incremented by 1.
- Reading the INDF register will return 0AH

6.1.2 TMR0 (Timer Counter **)**

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
01H(r/w)	TMR0	8-bit real-time timer counter							

TMR0 is an 8-bit timer counter. The clock source of TMR0 can be the instruction clock or an external clock. How to choose from T0CS (OPTION<5>) control. If an external clock (T0CKI pin) is selected, TMR0 will be on the rising/falling edge of the clock (by T0SE (OPTION<4>) control) plus 1. The prescaler can be assigned to the TMR0 mode by clearing the PSA bit (OPTION<3>). Block, in this case, any write to TMR0 will clear the prescaler register.

6.1.3 PCL (lower byte of the program counter **)** and **Stack**

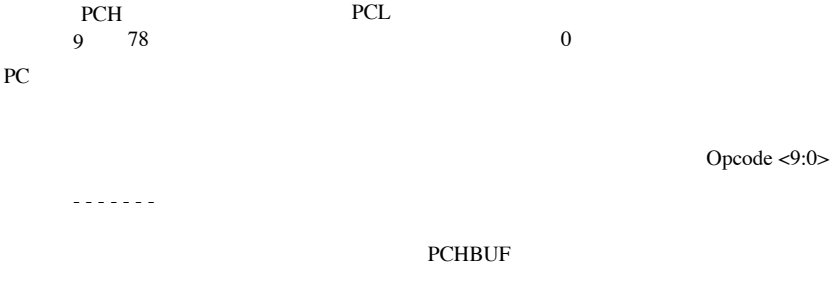
address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
02H(r/w)	PCL	Low byte of the program counter							

The HS2300-P has a 10-bit program counter PC and a 10-bit 5-level deep hardware stack. The lower 8 bits of the PC are PCL (PC<7:0>), it can be read or written; the 8th and 9th bits are PCH (PC<9:8>), which cannot be directly read or written, and the PCH register can be chan The change is implemented by the PCHBUF register.
When the program is executed, the PC is loaded with the next place where the program will be executed.
site. For each instruction cycle, the PC value will increase by 1, unless there is an instruction to change the value of the PC.

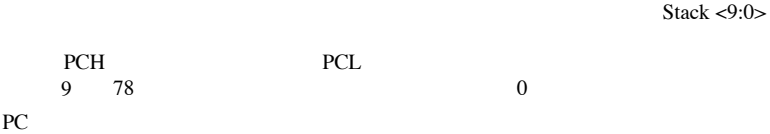
Figure 6.1 shows four cases of loading PC values.

Figure 6.1: Four cases of loading a PC

Case 1: Execute GOTO instruction



Case 2: Execute the CALL instruction



Case 3: Execute RETIA, RETFIE or RETURN instructions

Stack <9:0>

PCH PCL
9 78 0

PC

- - - - - - -

PCHBUF

Case 4: When writing PCL

PCH PCL
9 78 0

PC

ALU results or

PCHBUF<1:0> Opcode <7:0>

- - - - - - -

PCHBUF

Note 1: PCHBUF is valid only when the PCL content is the destination address.

2: PCHBUF does not change with PCH changes

6.1.4 STATUS (Status Register)

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
03H(r/w)	STATUS	RST	GP1	GP0	TO	PD	Z	DC	C

The status register STATUS reflects the state of the operator after the operation and reset. If STATUS is the destination of an instruction, And the instruction will affect the flag bit Z, DC or C, then the write operation for this three bits is forbidden. Bit4 and Bit3 are not writable. Clearing the status register STATUS will result in the following result 000uu1uu (u means unchanged).

C: carry/borrow bit

1 = with or without a borrow

0 = no carry or borrow

Note: The polarity is reversed when borrowing. Performing the subtraction is done by adding the complement of the second operand.

For shift instructions (RRR, RLR), the highest or lowest bit of the source register is in this bit.

DC: Half carry/borrow bit (ADDAR, ADDIA, SUBIA, SUBAR instruction)

1 = There is a 3rd bit to the 4th carry or no 3rd place to the 4th place

0 = no 3rd digit to carry the 4th digit or 3rd digit to the 4th digit

Z: Zero

1 = the result of an arithmetic or logical operation is zero
0 = result of operation or logical result is non-zero

PD : Power-down flag

1= Power up or execute CLRWDT instruction
0= Execute SLEEP instruction

TO : Timer overflow flag

1= Power up or execute CLRWDT or SLEEP instruction
0= watchdog timer overflow

GP1: GP0: General Purpose Register Read and Write Bits

RST: System wake-up type bit
1= PORTB status change wake up
0= other types of wakeup

6.1.5 FSR (Indirect Addressing Pointer)

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
04H(r/w)	FSR	Unused	Unused			Indirect addressing pointer			

Bit: Bit0: Select the indirect addressing register address;
Bit7:6: Not used, read returns 1

6.1.6 PORTA and PORTB (Port Data Register)

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
05H(r/w)	PORTA	Unused	Unused	Unused	Unused	IOA3	IOA2	IOA1	IOA0
06H(r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

The read port operation is the state of the read pin, regardless of the pin mode. IOB3 can be used as an input or as an open-drain output.

6.1.7 CHIPCON (Chip Control Register)

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
08H(r/w)	PCON	WDTE	EIS	LVDTE	Unused	Unused	Unused	Unused	Unused

LVDTE: LVDT (Low Voltage Detection) Enable Bit
1 = enable LVDT
0 = disable LVDT

EIS: IOB0/INT pin definition bit
1 = INT (external interrupt input pin), in this mode, IOB0 must be set to "1". The input function of IOB0 is controlled by the hardware screen Masking, reading the INT pin information is the same as reading PORTB
0 = IOB0 pin is selected, mask INT function

WDTE: WDT (Watchdog Timer) Enable Bit
1 = enable WDT
0 = disable WDT

6.1.8 WUCON (PORB Input Status Change Wakeup Control Register)

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
09H(r/w)	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

1: Enable wake-up function
0: Turn off wake-up function

6.1.9 PCHBUF (PC high buffer)

address	name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0AH(r/w)	PCHBUF	Unused	Unused	Unused	Unused	Unused	Unused		

The lower 2 digits are valid. See 6.1.3 for details.

6.1.10 PDCON (internal pull-down control register)

address	name	B7	B6	B5	B4	B3	B2	B1	B0
0BH(r/w)	PDCON	Unused	/PDB2	/PDB1	/PDB0	/PDA3	/PDA2	/PDA1	/PDA0

1: Disable the internal pull-down of the corresponding pin
0: Enable internal pull-down of corresponding pin

6.1.11 ODCON (Open-Drain Control Register)

address	name	B7	B6	B5	B4	B3	B2	B1	B0
0CH(r/w)	ODCON	ODB7	ODB6	ODB5	ODB4	Unused	ODB2	ODB1	ODB0

1: Corresponding pin open-drain output enable
0: Corresponding pin open-drain output is disabled

6.1.12 PHCON (Internal Pull-Up Control Register)

address	name	B7	B6	B5	B4	B3	B2	B1	B0
0DH(r/w)	PHCON	/PHB7	/PHB6	/PHB5	/PHB4	Unused	/PHB2	/PHB1	/PHB0

1: Disable the internal pull-up of the corresponding pin
0: Enable internal pull-up of the corresponding pin

6.1.13 INTEN (interrupt mask register)

address	name	B7	B6	B5	B4	B3	B2	B1	B0
0E(r/w)	INTEN	GIE	Unused	Unused	Unused	Unused	INTIE	PBIE	T0IE

T0IE: Timer0 overflow interrupt enable bit
1 = Enable Timer0 overflow interrupt
0 = Disable Timer0 overflow interrupt
PBIE: Port B input status change interrupt enable bit
1 = Enable Port B input status change interrupt
0 = Disable Port B input status change interrupt

INTIE: External Interrupt Enable Bit
1 = enable external interrupt
0 = disable external interrupt
GIE: global interrupt enable bit
1 = Enable all interrupts that are masked. For wake-up interrupts in sleep mode, the MCU will jump to interrupt address 008H.
0 = All interrupts are disabled. For sleep mode midpoint interrupt wake-up, the MCU will execute the SLEEP instruction.
Note: When an interrupt event occurs, the GIE is cleared by hardware and all interrupts are disabled.
Execute the RETFIE instruction to exit the interrupt
Order and reset GIE = 1 to allow interrupts.

6.1.14 INTFLAG (Interrupt Status Register)

address	name	B7	B6	B5	B4	B3	B2	B1	B0
0F(r/w)	INTFLAG	Unused	Unused	Unused	Unused	Unused	INTIF	PBIF	T0IF

T0IF: Timer0 overflow interrupt flag, set when Timer0 overflows, software reset
PBIF: Port B input status change interrupt flag, set when Port B input status changes, software reset
INTIF: External interrupt flag, rising/falling edge of INT pin (configured by INTEDG bit OPTION<6>), software complex Bit

6.1.15 ACC (accumulator)

address	name	B7	B6	B5	B4	B3	B2	B1	B0
N/A(r/w)	ACC	accumulator							

An internal data transfer, instruction operand memory location is not addressed when the accumulator is present.

6.1.16 OPTION register

address	name	B7	B6	B5	B4	B3	B2	B1	B0
N/A(w)	OPTION	Not used	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Execute the OPTION instruction and the contents of the accumulator ACC will be transferred to the OPTION register. OPTION register is A writable unreadable register that contains various control bits to set the TMR0/WDT and its prescaler and external interrupt.

PS2: PS0: Prescaler ratio selection bit

PS2: PS0	**TMR0** ratio	**WDT** ratio
0 0 0	1:2	1:1
0 0 1	1:4	1:2
0 1 0	1:8	1:4
0 1 1	1:16	1:8
1 0 0	1:32	1:16
1 0 1	1:64	1:32
1 1 0	1:128	1:64
1 1 1	1:256	1:128

PSA: Prescaler allocation bit

1= Prescaler assigned to WDT

0= Prescaler assigned to TMR0

T0SE: TMR0 clock source edge select bit

1= T0CKI pin falling edge trigger count

0= T0CKI pin rising edge trigger count

T0CS: TMR0 clock source select bit

1= External T0CKI pin. Even if IOST IOB2="0", IOB2/T0CKI will be forced to be input.

0= internal instruction clock

INTEDG: External Interrupt Trigger Mode Select Bit

1 = INT pin rising edge triggers interrupt

0 = INT pin falling edge trigger interrupt

6.1.17 **IOSTA** and **IOSTB** (**I/O** Port Control Register)

address	name	B7	B6	B5	B4	B3	B2	B1	B0
05H(w)	IOSTA				PORTA I/O Control Register				
05H(w)	IOSTB				PORTB I/O Control Register				

Execute the IOST R (05H~06H) instruction to load the contents of the accumulator ACC into this register. When the IOST register is some When the position is "1", the output of the corresponding pin is driven to a high impedance state (in this case, the input mode); when the IOST register is The data in the latch is output from the corresponding pin (in this case, the output mode). The IOST register is only writable and is set to 1 after reset.

6.2 **I/O** port

PORT A and PORT B are bidirectional tri-state input/output ports. PORT A is a 4-pin I/O port; PORT B is an 8-pin I/O port. IOB3 can be used as an input or an open-drain output.

In addition to IOB3 as an input or open-drain output and IOB2 need to pass the T0CS ((OPTION<5>)) bit of the OPTION register In addition to control, all I/O pins have a direct control register (IOSTA and IOSTB) for configuring the port's input and output. state.

When IOB3 is used as an open-drain output, the port must be configured as an output, and the chip programming configuration option must be set to ope

The IOB input state change can wake up the chip and configure the wake-up function of the corresponding pin through the WUCON register.

IOB<7:4> and IOB<2:0> have corresponding pull-up control bits (PHCON register) to enable internal pull-ups, if set For output mode, the internal pull-up function is automatically turned off.

IOA<3:0> and IOB<2:0> have corresponding pull-down control bits (PDCON register) to enable internal pull-down, if set to In the output mode, the internal pull-down function is automatically turned off.

IOB<7:4> and IOB<2:0> have corresponding open-drain control bits (ODCON registers) when these pins are set to output mode The open-drain output can be enabled by the ODCON register.

IOB<7:0> has an input change interrupt/wake function. Whether each of its pins has this function depends on the WUCON registration Corresponding bit

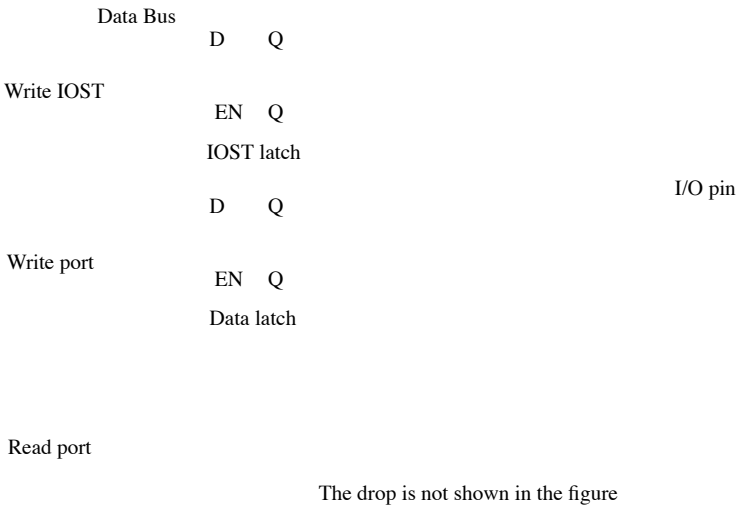
When EIS (PCON<6>) = 1, IOB0 is used as an external interrupt input pin. In this mode, IOB0 input changes interrupt/wake-up function. Can be shielded by hardware, even if the software has been set to use the interrupt/wake function.

The multiplex function of the pin can be set by the configuration word. After the multiplex function is set, the read I/O value is 0.

The I/O port pin diagram is as follows

IOA0~IOA3:

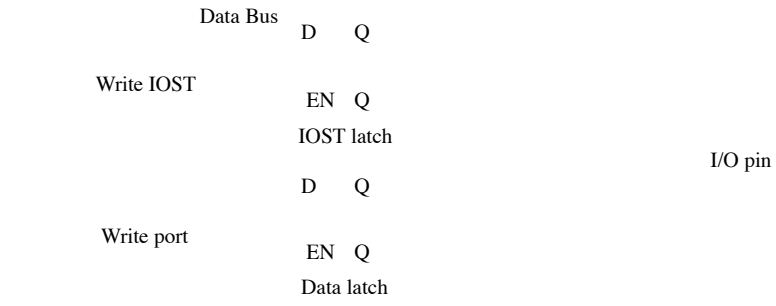
Page 16



The drop is not shown in the figure

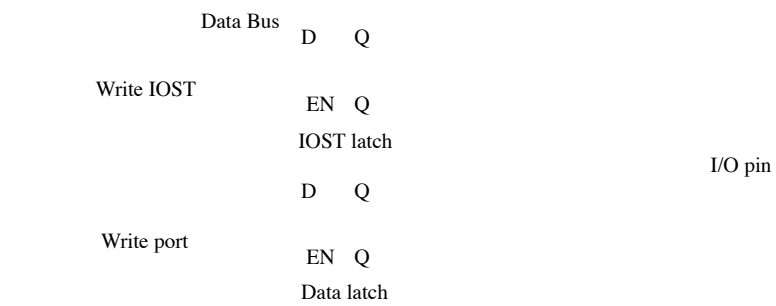
Page 17

IOB1~IOB7:

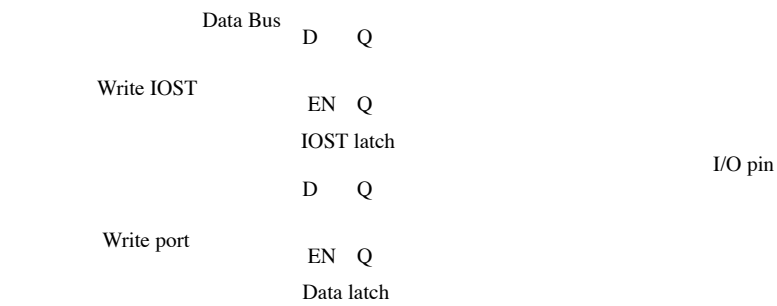


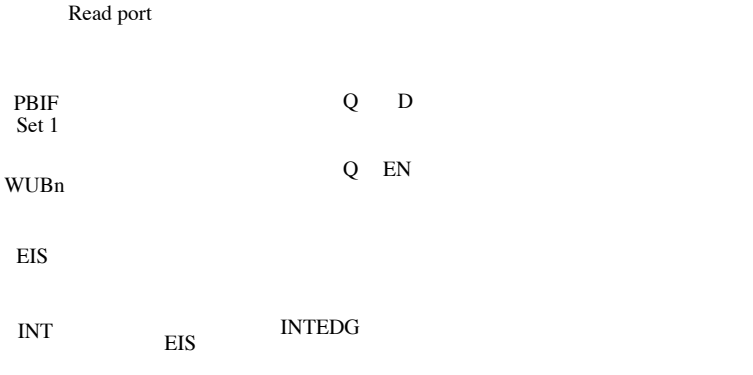
Pull-up/pull-down/open-drain is not shown in the figure

IOB3:



IOB0/INT:





Pull-up/pull-down/open-drain is not shown in the figure

6.3 Timer0/WDT and Prescaler

6.3.1 Timer0

Timer0 is an 8-bit timer counter with an optional internal instruction clock or an external clock source (T0CKI pin).

6.3.1.1 Internal Instruction Clock as Clock Source: Timing Mode

The timing mode is selected by clearing the T0CS bit.

In the timing mode, TMR0 is incremented by 1 for each instruction cycle (without prescaler).

If the TMR0 register is written, TMR0 will not start incrementing after two instruction cycles.

6.3.1.2 External clock source: counting mode

The count mode is selected by setting T0CS. In the counting mode, TMR0 is incremented by 1 on the rising or falling edge of the T0CKI pin.

Whether the rising edge or the falling edge is controlled by T0SE (1: falling edge; 0: rising edge).

When the prescaler is not used, the external clock can also be output as a prescaler.

The synchronization of T0CKI with the internal phase clock is required.

This is done by sampling the output of the prescaler at T2 and T4 of the phase clock. Therefore, the signal of T0CKI is required to be high and low.

Keep at least 2Tosc.

When using prescaler, the external clock signal is first divided by the asynchronous ripple counter prescaler.

In order to make the external clock full

For the full sampling requirement, the pulsation counter must be taken into account.

Therefore, the external clock is required to maintain at least 4Tosc for the prescaler to divide.

6.3.2 WDT (Watchdog Timer)

The Watchdog Timer (WDT) is an on-chip RC oscillator that does not require any external components. The RC vibration

The oscillator is independent of the RC oscillator on the OSCI/OSCO pin. This way, even if the device's OSCI and OSCO pins are clocked off

The vibration (such as sleep mode), the WDT will still work normally.

In normal operation or in sleep mode, a WDT overflow will cause a device Reset.

T0 will be cleared to 0. There is a device configuration bit, WDTE, which controls the enable/disable of the Watchdog Timer (WDT).

In the absence of prescaler, the watchdog overflow time is approximately 18ms, 4.5ms, 288ms or 72ms. This time can pass

SUT<1:0> settings. If a longer overflow time is required, the prescaler can be used, so the maximum time the watchdog overflows is approximately 36.8s.

The CLRWDT instruction is used to clear the WDT and the divider. If the WDT is enabled, this instruction prevents the watchdog from overflowing

Reset the chip.

The SLEEP instruction will reset the WDT and the divider if the WDT is enabled. This will provide the longest before the watchdog resets. sleeping time.

6.3.3 Prescaler

The prescaler (8-bit down count) can be used for Timer0 or WDT, but not both. PSA (OPTION<3>) decision

The fixed prescaler is assigned to Timer0 or WDT, and PS<2:0> (OPTION<2:0>) determines the division ratio.

When the prescaler is assigned to Timer0, a write to TMR0 will clear the prescaler. When the prescaler is assigned to the WDT,

CLRWDT will clear the prescaler and WDT. The prescaler is not readable or writable. After reset, the prescaler content is all ones.

To avoid unnecessary resets, the CLRWDT instruction or the CLRR TMR0 instruction must be used when changing the prescaler.

Need to be executed.

Instruction clock

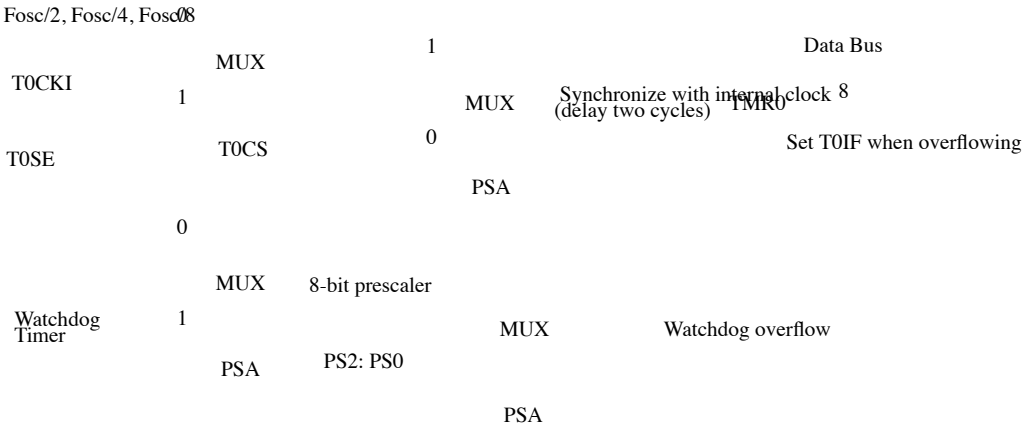


Figure 6.4: Block Diagram of the Prescaler

6.4 interrupt

The HS2300-P has three interrupt modes:

1. External interrupt of INT pin
2, TMR0 overflow interrupt
3, PORT B input status change interrupt

INTFLAG is the interrupt flag register. Global Interrupt Enable bit, GIE (INTEN<7>), enables all unused screens when set.
Blocked interrupts, all interrupts will be turned off when cleared.

When the interrupt occurs, the GIE bit (the GIE bit before the interrupt occurs and the interrupt mask associated with the interrupt is set to 1) is clea
The further interrupt is interrupted, and the next instruction jumps to 008h and begins execution.
The interrupt flag bit is cleared by software before the GIE is reset.
Prevent repeated interruptions.

Executing the RETFIE instruction will exit the interrupt and will reset the GIE

An interrupt flag bit (except PBIF) will be set by its interrupt event, regardless of whether its associated interrupt enable bit is enabled.
use. Reading the INTFLAG register will return the result of INTFLAG and INTEN.

When a soft interrupt occurs through the INT instruction, the next instruction jumps to 002H and begins execution.

6.4.1 External Interruption

Whether the external interrupt INT pin rising edge or falling edge trigger is determined by the INTEDG bit (OPTION<6>), when a valid
The flag bit, INTIF, is set when a transition occurs. If the INTIE bit (INTEN<2>) is cleared, the interrupt is masked.

If the INTIE bit is already set before sleep, the INT interrupt can wake the system from sleep. If the GIE bit has been set,
The interrupt service routine will be executed after the machine wakes up, otherwise the next instruction after sleep will be run.

6.4.2 Timer0 Interrupt

The T0IF flag is set (INTFLAG<0>) when TMR0 overflows (FFH 00H). The T0IE bit (INTEN<0>) is cleared.
The interrupt is blocked.

6.4.3 PORT B Input Change Interrupt

When the IOB<7:0> input changes the interrupt trigger, the PBIF flag is set (INTFLAG<1>). The PBIE bit (INTEN<1>) is cleared.
The interrupt is blocked.

The port B information must be read before the input change interrupt occurs. The WUBn bit corresponding to the port of PortB
(WUCON<7:0>) This function is not available when cleared or set to output or when the IOB0 pin is set to external interrupt input pin INT.

If the PBIE bit is already set before sleep, the PORT B input pin change interrupt can also be used as a sleep wake condition. In sleep
The previous GIE bit has been set, and the interrupt service routine will be executed after the MCU wakes up. Otherwise, the next instruction after sleep

6.5 SLEEP (sleep mode **)**

Execute the SLEEP instruction to enter sleep mode. PD is cleared, T0 is set, watchdog timer is also cleared to 0 but still keeps running
Status, external clock is off; all I/O pins remain in the state before sleep

6.5.1 Sleep awakening

The following events will occur to wake the chip from sleep mode:

1, RSTB pin reset

2, WDT overflow (if WDT is enabled)

3. IOB0/INT pin interrupt, or PORT B input status change

An external RSTB pin and a watchdog overflow can reset the machine.

The PD bit is set at power-on reset or when the SLEEP instruction is executed.

The TO bit is used to clear the watchdog time-out reset.

In order for the machine to wake up by an interrupt, the interrupt enable bit must be set, regardless of whether the GIE is set.

When the GIE bit is cleared, the machine

After the wake-up, the instruction after the SLEEP instruction is executed; when the GIE bit is set to 1, the machine wakes up to the interrupt reset addre

The machine wake-up delay time in high or low frequency mode is 18/4.5/288/72ms (this delay time is set by SUT<1:0>) plus 16 vibrations

Swing cycle.

In IRC, ERIC or ERC mode, the machine wake-up delay time is 640μs.

6.6 reset **RESET**

The following events will cause the HS2300-P to reset:

1, power-on reset (POR)

2. Brown-out reset (BOR)

3, WDT overflow reset

4, RSTB pin reset

Some registers have no effect under some reset conditions, their state is unknown during power-up and other reset situations.

Unchanged. On a power-on reset, the RSTB pin is reset, and most registers return to the reset state after a watchdog WDT overflow reset.

When the Vdd rise signal is detected, the chip will generate a power-on reset pulse signal. To use this feature, users need

Connect the RSTB pin to Vdd.

When Vdd is below a certain fixed value, it will be a chip reset, which ensures that the chip can only operate within the normal voltage range. owe

Voltage reset (BOR) reset is used primarily as an application in AC or heavy duty switching applications.

6.6.1 Power- **up** Delay Timer **PWRT**

After any reset, the Power-up Timer provides a delay time of 18/4.5/288/72ms (this delay time is

SUT<1:0> setting) (or 640μs depending on the source of the oscillation and the reset condition). The chip will remain in reset state here. This

The period of time will vary depending on voltage, temperature, and process.

Table 6.1 PWRT time

Oscillation type	Power-on reset Undervoltage reset	**RSTB** reset **WDT** overflow reset
ERC, IRC, ERIC	18/4.5/288/72ms	640μs
HF, LF	18/4.5/288/72ms	18/4.5/288/72ms

6.6.2 Oscillator Start-up Timer **OST**

In HF or LF mode, the start-up timer (OST) provides a 16 oscillator week when the PWRT delay expires.

Period delay (input from OSCI). This is to ensure that the crystal or ceramic resonator starts to oscillate and establish a stable oscillation. During this tir

As long as the OST is working, the MCU will remain in the reset state.

The start-up timer counts up only when the amplitude of the oscillating signal reaches the input threshold of the oscillator.

6.6.3 Reset sequence

After the POR, BOR or WDT overflow signal is detected, reset in the following order

1. Reset latch is set, clear PWRT and OST;

2. After POR, BOR or WDT overflow reset pulse, PWRT starts counting;

3. After the PWRT overflows, the OST starts counting.

4. After the OST is finished, clear the latch and reset.

In HF or LF mode, the reset delay time is 18/4.5/288/72ms plus 16 oscillation periods; in IRC/ERIC, ERC

In mode, the POR, BOR reset delay time is 18/4.5/288/72ms; the RSTB and WDT overflow reset delay time is 640μs.

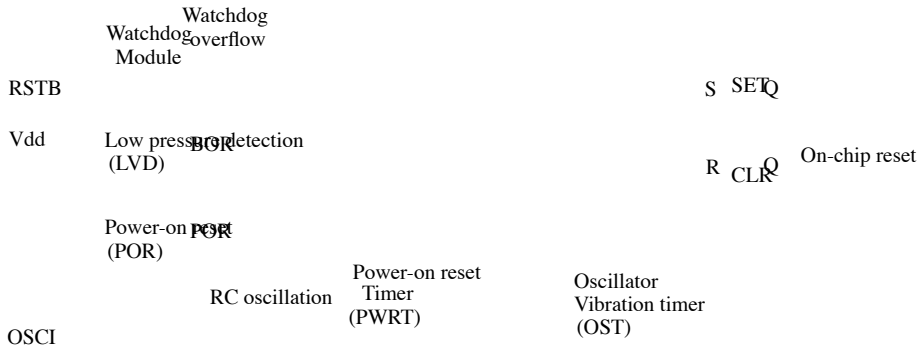


Figure 6.5 Reset circuit diagram

Table 6.2 Register Reset Status

register	address	**POR** or **BOR**	**RSTB** or **WDT** reset
ACC	N/A	Xxxx xxxx	Uuuu uuuu
OPTION	N/A	-011 1111	-011 1111
IOSTA	05H	---- 1111	---- 1111
IOSTB	06H	1111 1111	1111 1111
INDF	00H	Xxxx xxxx	Uuuu uuuu
TMR0	01H	Xxxx xxxx	Uuuu uuuu
PCL	02H	1111 1111	1111 1111
STATUS	03H	0001 1xxx	000# #uuu
FSR	04H	11xx xxxx	11uu uuuu
PORTA	05H	Xxxx xxxx	Uuuu uuuu
PORTB	06H	Xxxx xxxx	Uuuu uuuu
PCON	08H	101- ----	101- ----
WUCON	09H	0000 0000	0000 0000
PCHBUF	0AH	---- --00	---- --00
PDCON	0BH	1111 1111	1111 1111
ODCON	0CH	0000 0000	0000 0000
PHCON	0DH	1111 1111	1111 1111
INTEN	0EH	0--- -000	0--- -000
INTFLAG	0FH	---- -000	---- -000
General purpose register	10H~3FH	Xxxx xxxx	Uuuu uuuu

Description: u = not changed; x = unknown; - = not used; # = reference table

Table 6.3 RST/T0/PD Status After Reset or Wake-up

RST	**T0**	**PD**	condition
0	1	1	Power-on reset POR
0	1	1	Brown-out reset BOR
0	u	u	RSTB reset under normal working conditions
0	1	0	RSTB reset during sleep
0	0	1	WDT reset under normal working conditions
0	0	0	WDT wakes up during sleep
1	1	0	Pin change wake up during sleep

Description: u = not changed

Table 6.4 Events Affecting T0/PD

event	**T0**	**PD**
Power-on	1	1
WDT overflow	0	u
Execute the SLEEP instruction	1	0
Execute the CLRWDT instruction	1	1

Description: u = not changed

6.7 oscillation configuration

The HS2300-P has 6 different oscillation modes. You can select different modes by configuring Fosc:

1. ERC: External R/C Oscillator
2, IRC: internal resistance internal capacitor oscillator
3, ERIC: external resistor internal capacitor oscillator
4, XT: external oscillator
5, LF: low frequency crystal oscillator
6, HF: high frequency crystal oscillator

In XT, LF, or HF mode, a crystal or ceramic is connected to the OSCI and OSCO pins to establish oscillation. For saving
When the cost or accuracy is not high, the ERC mode can be selected. The RC oscillation frequency depends on the R and C values, and the operating te
And other process parameters.

The IRC/ERIC oscillation mode is used for cost saving, and can be applied in places where accuracy is not required. The MCU provides 4 different
RC oscillation frequency: 8MHz, 4MHz, 1MHz and 455KHz, selected by (RCM<1:0>), or the user can also pass
Change the external resistor to achieve. The ERIC oscillator frequency is dependent on resistance and capacitance, operating temperature, and other proc

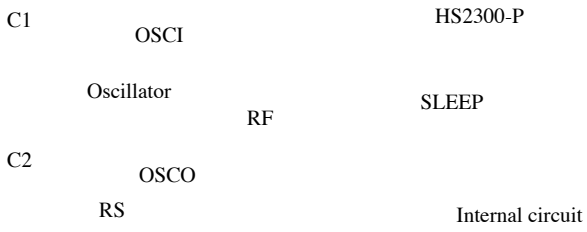


Figure 6.6: HF or LF mode (external oscillation)

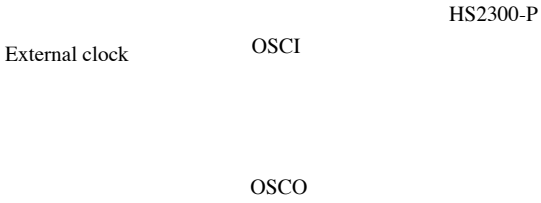


Figure 6.7: HF or LF mode (external clock input)

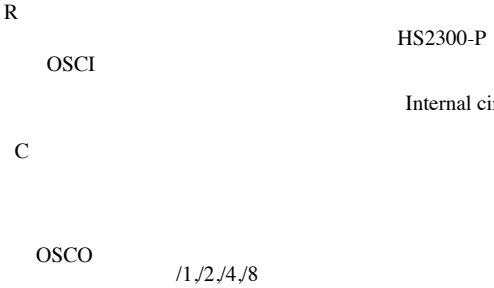


Figure 6.8: ERC Mode

R HS2300-P

OSCI

C Internal circuit

OSCO

/1,/2,/4,/8

Figure 6.9: ERIC mode

Page 25

R HS2300-P

OSCI

C Internal circuit

OSCO

/1,/2,/4,/8

Figure 6.10: IRC mode

7. Electrical characteristics

7.1 absolute maximum rating

Power supply voltage: 0V~ 6.0V
Input voltage: VSS-0.3V~ VDD+0.3V
Storage temperature: -65 ° C ~ 150 ° C
Working temperature: 0 ° C ~ 70 ° C

7.2 Operating conditions

DC supply voltage: +2.3V~5.5V

7.3 DC characteristics **(** unless otherwise specified **WDT** and **LVDT are** prohibited **)**

Working temperature: 0 ° C ~ 70 ° C

symbol	description	condition	Minimum	typical	maximum	unit
F_{HF}	HF mode clock range	Vdd=5V	1		20	MHz
		Vdd=3V	1		15	
F_{LF}	LF mode clock range	Vdd=5V	32		4000	KHz
		Vdd=3V	32		1000	
F_{ERC}	ERC mode clock range	Vdd=5V	DC		15	MHz
		Vdd=3V	DC		7	
$F_{IRC/ERIC}$	IRC/ERIC mode Clock range	ERIC mode, Vdd=5V	DC		15	MHz
		ERIC mode, Vdd=3	DC		7	
		IRC mode, Vdd=5V	0.455		8	
		IRC mode, Vdd=3	0.455		8	
V_{IH}	Input high voltage	I/O port, Vdd=5V	2.0			V
		RSTB, T0CKI pin, Vdd=5V	2.0			
		I/O port, Vdd=3V	1.5			
		RSTB, T0CKI pin, Vdd=3V	1.5			
V_{IL}	Input low voltage	I/O port, Vdd=5V			1.0	V
		RSTB, T0CKI pin, Vdd=5V			1.0	
		I/O port, Vdd=3V			0.6	
		RSTB, T0CKI pin, Vdd=3V			0.6	
V_{OH}	Output high voltage	Vdd=5V, I_{OH} =-5.4mA	3.6			V
V_{OL}	Output low voltage	Vdd=5V, I_{OL} =8.7mA			0.6	V
I_{PH}	Pull-up resistor current	Pin grounding, Vdd=5V		-65		µA
I_{PD}	Pull-down resistor current	Pin connected to Vdd, Vdd=5V		45		µA
I_{WDT}	WDT current	Vdd=5V		9	12	µA
		Vdd=3V		2	4	
T_{WDT}	WDT cycle	Vdd=5V		16.2		Ms
		Vdd=4V		17.9		
		Vdd=3V		20.4		

		Vdd=5V, LVDT=3.6V	30	40	
I_{LVDT}	LVDT current	Vdd=5V, LVDT=2V	twenty three	30	μA
		Vdd=3V, LVDT=2V	6.8	8.0	
		Sleep mode, Vdd=5V, WDT makes can	20		
		Sleep mode, Vdd=5V, WDT ban stop	3		
I_{SB}	Sleep mode current	Sleep mode, Vdd=3V, WDT makes can	2.5		μA
		Sleep mode, Vdd=3V, WDT ban stop	1.1		
		HF mode, Vdd=5V, 4 clock fingers make			
		20MHz	2.04		
I_{DD}	Working current	15MHz	1.68		mA
		10MHz	1.28		
		4MHz	0.78		
		2MHz	0.62		
		HF mode, Vdd=3V, 4 clock fingers make			
		20MHz	0.92		
IDD	Working current	15MHz	0.72		mA
		10MHz	0.54		
		4MHz	0.30		
		2MHz	0.19		
		HF mode, Vdd=5V, 2 clock fingers make			
		20MHz	2.94		
I_{DD}	Working current	15MHz	2.34		mA
		10MHz	1.74		
		4MHz	0.96		
		2MHz	0.68		
		HF mode, Vdd=3V, 2 clock fingers make			
		20MHz	1.38		
I_{DD}	Working current	15MHz	1.07		mA
		10MHz	0.77		
		4MHz	0.38		
		2MHz	0.24		
		LF mode, Vdd=5V, 4 clock fingers make			
		2MHz	290		
I_{DD}	Working current	1MHz	208		μA
		500KHz	167		
		100KHz	118		
		32KHz	101		

		LF mode, Vdd=3V, 4 clock fingers make			
		2MHz	105		
I_{DD}	Working current	1MHz	73		μA
		500KHz	54		
		100KHz	33		
		32KHz	26		
		LF mode, Vdd=5V, 2 clock fingers make			

I_{DD}	Working current	2MHz		371	μA
		1MHz		269	
		500KHz		194	
		100KHz		130	
		32KHz		108	
		LF mode, Vdd=3V, 2 clock fingers make			
		2MHz		158	
I_{DD}	Working current	1MHz		100	μA
		500KHz		67	
		100KHz		38	
		32KHz		29	
		ERC mode, Vdd=5V, 4 clocks instruction			
			R=1K F=14.96M	4.572	
			R=3.3KF=11.06M	1.845	
		C=3P	R=10K F=5.80M	0.761	
			R=100K F=808K	0.170	
			R=300K F=276K	0.119	
			R=1K F=11.7M	4.226	
			R=3.3KF=6.35M	1.519	
		C=20P	R=10K F=2.73M	0.613	
			R=100K F=320K	0.147	
IDD	Working current		R=300K F=108K	0.109	
			R=1K F=5.23M	3.429	
			R=3.3KF=2.05M	1.163	
		C=100P	R=10K F=748K	0.454	mA
			R=100K F=80K	0.126	
			R=300K F=26.4K	0.100	
			R=1K F=2.5M	3.024	
			R=3.3KF=900K	1.021	
		C=300P	R=10K F=316K	0.403	
			R=100K F=32K	0.119	
			R=300K F=10.67K	0.098	
		ERC mode, Vdd=3V, 4 clocks instruction			
IDD	Working current		R=1K F=8.29M	2.280	

		R=3.3KF=7.2M	0.913
		R=10K F=4.58M	0.396
		R=100K F=900K	0.071
		R=300K F=316K	0.040
		R=1K F=7M	2.214
		R=3.3KF=5.1M	0.837
	C=20P	R=10K F=2.71M	0.327
		R=100K F=374K	0.058
		R=300K F=128K	0.035
		R=1K F=4.14M	2.060
		R=3.3KF=2.11M	0.688
	C=100P	R=10K F=848K	0.253
		R=100K F=96K	0.047
		R=300K F=32K	0.030
		R=1K F=2.36M	1.890
		R=3.3KF=972K	0.630
	C=300P	R=10K F=360K	0.226
		R=100K F=38K	0.043
		R=300K F=12.71K	0.028
	ERC mode, Vdd=5V, 2 clocks instruction		
C=3P		R=1K F=15.16M	5.435
		R=3.3KF=11.27M	2.358

			R=10K F=5.77M	0.986	
			R=100K F=826K	0.183	
			R=300K F=274K	0.108	
		C=20P R=1K	F=11.56M	4.835	
			R=3.3KF=6.12M	1.808	
			R=10K F=2.72M	0.701	
			R=100K F=308K	0.138	
I_{DD}	Working current		R=300K F=105K	0.092	mA
		C=100P R=1K	F=5.32M	3.680	
			R=3.3KF=1.99M	1.234	
			R=10K F=722K	0.479	
			R=100K F=77K	0.110	
			R=300K F=25K	0.081	
		C=300P R=1K	F=2.52M	3.107	
			R=3.3KF=892K	1.057	
			R=10K F=312K	0.398	
			R=100K F=32K	0.102	
			R=300K F=11K	0.077	
		ERC mode, Vdd=3V, 2 clocks instruction			
I_{DD}	Working current	C=3P R=1K	F=8.306M	2.552	mA
			R=3.3KF=7.29M	1.130	
			R=10K F=4.81M	0.518	

Page 30

			R=100K F=904K	0.084	
			R=300K F=338K	0.039	
		C=20P R=1K	F=7.08M	2.445	
			R=3.3KF=5.07M	0.986	
			R=10K F=2.68M	0.393	
			R=100K F=362K	0.061	
			R=300K F=123K	0.031	
		C=100P R=1K	F=4.11M	2.197	
			R=3.3KF=2.03M	0.745	
			R=10K F=810K	0.270	
			R=100K F=91K	0.043	
			R=300K F=30K	0.025	
		C=300P R=1K	F=2.37M	1.953	
			R=3.3KF=964K	0.648	
			R=10K F=354K	0.231	
			R=100K F=38K	0.038	
			R=300K F=13K	0.022	
		ERIC mode, Vdd=5V, 4 clocks instruction			
		R=1K	F=15.16M		
I_{DD}	Working current	R=3.3K	F=11.27M		mA
		R=10K	F=5.77M		
		R=100K	F=826K		
		R=300K	F=274K		
		ERIC mode, Vdd=3V, 4 clocks instruction			
		R=1K	F=15.16M		
I_{DD}	Working current	R=3.3K	F=11.27M		mA
		R=10K	F=5.77M		
		R=100K	F=826K		
		R=300K	F=274K		
		ERIC mode, Vdd=5V, 2 clocks instruction			
		R=1K	F=15.16M		
I_{DD}	Working current	R=3.3K	F=11.27M		mA
		R=10K	F=5.77M		
		R=100K	F=826K		

		R=300K	F=274K	
		ERIC mode, Vdd=3V, 2 clocks instruction		
		R=1K	F=15.16M	
I_{DD}	Working current	R=3.3K	F=11.27M	mA
		R=10K	F=5.77M	
		R=100K	F=826K	
		R=300K	F=274K	
I_{DD}	Working current	IRC mode, Vdd=5V, 4 clock fingers		mA

Page 31

		make		
		F=8M		
		F=4M		
		F=1M		
		F=455K		
		IRC mode, Vdd=3V, 4 clock fingers make		
I_{DD}	Working current	F=8M		mA
		F=4M		
		F=1M		
		F=455K		
		IRC mode, Vdd=5V, 2 clock fingers make		
I_{DD}	Working current	F=8M		mA
		F=4M		
		F=1M		
		F=455K		
		IRC mode, Vdd=3V, 2 clock fingers make		
I_{DD}	Working current	F=8M		mA
		F=4M		
		F=1M		
		F=455K		

8. Package and size

8.1 SOP14 package drawing and dimensions

8.1.1 SOP14 package drawing

8.1.2 SOP14 package size

Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.1	-	0.25	0.004	-	0.01
A2	-	1.45	-	-	0.057	-
B	0.33	-	0.51	0.013	-	0.02
C	0.19	-	0.25	0.007	-	0.010
D	8.55	-	8.75	0.337	-	0.344
E	3.8	-	4	0.150	-	0.157
e	-	1.27	-	-	0.05	-
H	5.8	-	6.2	0.228	-	0.244
L	0.4	-	1.27	0.016	-	0.05
Y	-	-	0.10	-	-	0.004

8.2 DIP14 package drawing and dimensions

8.2.1 DIP14 package drawing

8.2.2 DIP14 package size

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.650 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.250 (TYP)		0.01(TYP)	

8.3 SOP8 package drawing and dimensions

8.3.1 SOP8 package drawing

8.3.2 SOP8 package size

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
H	0.250 (TYP)		0.01(TYP)	

8.4 DIP8 package drawings and dimensions

8.4.1 DIP8 package drawing

8.4.2 DIP8 package size

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170

A1	0.510		0.020		
A2	3.200	3.600	0.126	0.142	
B	0.380	0.570	0.015	0.022	
B1	1.524 (BSC)	0.060 (BSC)			
C	0.204	0.360	0.008	0.014	
D	9.000	9.400	0.354	0.370	
E	6.200	6.600	0.244	0.260	
E1	7.32		7.920		
e	2.540 (BSC)	0.100 (BSC)			
θ	0^0	8^0	0^0	8^0	

9. Amend the record

version	time	content	editor
V2.00F	**2016.03.09**	first edition	HLJ
V2.01F	**2016.05.20**	How to configure **IOB3 in the** IO port description	QCH