IAN HILL

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Key Qualifications

- Forefront knowledge in integrated electronics reliability including physics, test methods, and prediction techniques.
- Expertise with probabilistic programming paradigms for generative modelling and Bayesian experimental design.
- Proficient in a breadth of ASIC design and test topics across both analog and digital domains.
- Highly developed technical leadership skills from design team, research group, and teaching assistant roles.

Experience

Capstone Teaching Assistant, University of British Columbia: *Vancouver, BC (Sept. 2020 – Present)*

- Provided technical guidance, mentorship, and evaluation for 25 teams across diverse hardware and software projects.

Silicon Verification Intern, Microsoft Corporation: *Raleigh, NC (Sept. – Dec. 2019)*

- Designed dynamic SystemVerilog generation tooling, accelerating test simulations across four design teams.
- Lead development of on-demand RTL memory generation system, eliminating vendor delays for digital designers.

ASIC Design Intern, NVIDIA Corporation: *Santa Clara, CA (Sept. – Dec. 2018)*

- Developed lightweight PCIe 4.0 clocking architecture model for rapid design feedback and test simulations.
- Implemented and verified critical bug resolutions in ASIC graphics processors using Perl and Verilog.

Silicon Validation Engineering Intern, NVIDIA Corporation: *Santa Clara, CA (Jan. – Apr. 2018)*

- Developed on-demand pre-silicon power estimator, providing rapid chip binning planning capabilities.

Hardware Designer, Tyco Security Products: *Vaughan, ON (May – Aug. 2017)*

- Designed and evaluated circuitry enabling long-range wired communications in intrusion security products.

Tools

Python, Rust
NumPyro, PyMC
KiCAD, Altium
Cadence Virtuoso
Verilog, VHDL
Vim, LaTeX, Office

Interests

Classical guitar
Music composition
Downhill skiing
Scuba diving
Sail racing

Projects

Candidate for Doctor of Philosophy in Electrical and Computer Engineering, University of British Columbia: *Vancouver, BC (Sept. 2020 – Present)*

Thesis – Accelerated test design and live monitoring strategies for silicon wear-out

Supervisor – Professor André Ivanov

Awards – NSERC Postgraduate Doctoral Scholarship (PGS-D) – 2023 – $95 000 CAD

Bachelor of Applied Science, Honours Co-operative Electrical Engineering with Management Sciences Option, University of Waterloo: *Waterloo, ON (Sept. 2015 – Apr. 2020)*

Projects

12nm ASIC for Development of Novel Silicon Wear-Out Sensors: *(Sept. 2021 – Sept. 2023)*

- Designed and implemented novel mixed-signal device aging sensors in a FinFET process.

Automated Accelerated Hardware Stress Testing Platform: *(Mar. 2023 – Jul. 2024)*

- Developed PCB and Rust firmware solution to reliably conduct continuous 1000-hour tests.

Photonics Aging Analysis and Non-Invasive Monitoring: *(Jan. 2021 – Apr. 2022)*

- Developed custom photonics IC for photonics aging sensor development.