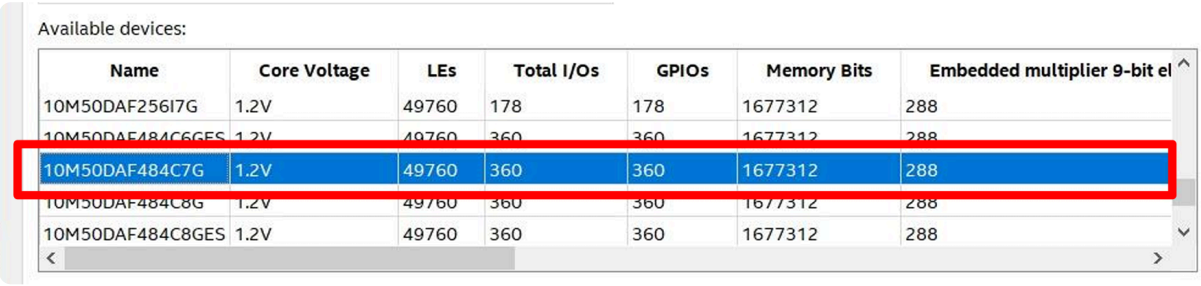
# Week9 Special Multiply

## Basic Setting

1. **Device Family:** MAX 10(DA/DF/DC/SA/SC)
2. **Available Devices:** 10M50DAF484C7G


Available devices:

| Name | Core Voltage | LEs | Total I/Os | GPIOs | Memory Bits | Embedded multiplier 9-bit el |
|---|---|---|---|---|---|---|
| 10M50DAF256I7G | 1.2V | 49760 | 178 | 178 | 1677312 | 288 |
| 10M50DAF484C6GES | 1.2V | 49760 | 360 | 360 | 1677312 | 288 |
| 10M50DAF484C7G | 1.2V | 49760 | 360 | 360 | 1677312 | 288 |
| 10M50DAF484C8G | 1.2V | 49760 | 360 | 360 | 1677312 | 288 |
| 10M50DAF484C8GES | 1.2V | 49760 | 360 | 360 | 1677312 | 288 |

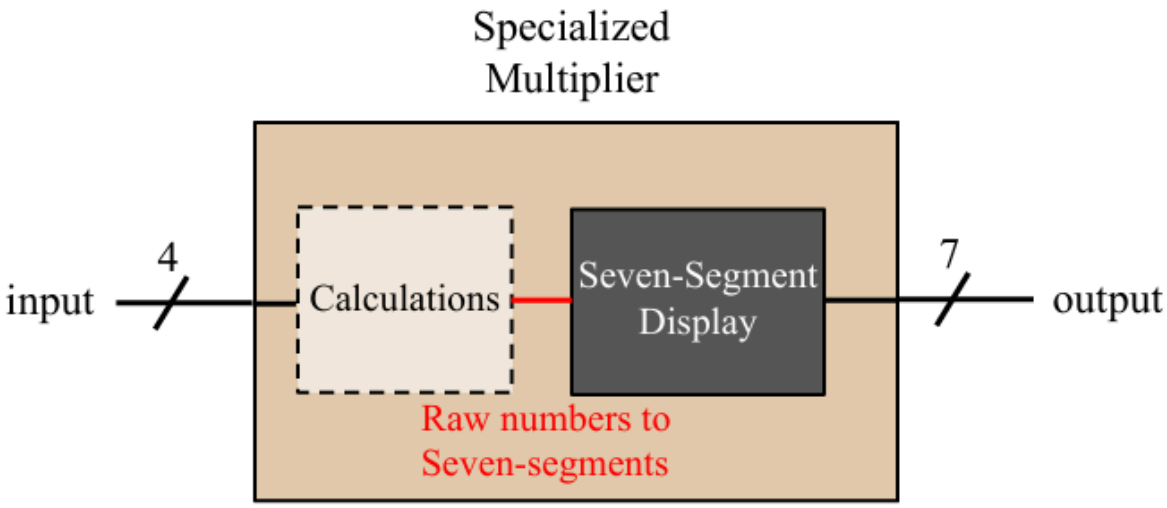
3. **EDA Tool Settings, Simultation:** Modelsim-Altera, Verilog HDL
4. Click 「Assignments > Pin Planner > Location」分配 Pin
5. 到裝置管理員，「其他裝置 > USB-Blaster」，右鍵「更新驅動程式」
6. 瀏覽電腦上的驅動程式
7. 路徑 `C:\intelFPGA_lite\16.1\quartus\drivers\usb-blaster` （16.1 或 18.1）
8. 到裝置管理員，「通用序列匯流排控制器 > Altera USB-Blaster」，有就代表成功
9. Click 「Tools > Programmer」
10. Click 「Hardware Setup > USB Blaster」，然後 Currently selected hardware 選「USB-Blaster [USB0]」
11. Click 「Add file > ~.sof > Open」（注意是在 `outputfiles` 裡面）
12. Click 「Start」顯示 Success 成功

## Special Multiply

### Request

1. 當輸入為 0~2，輸出值=輸入值+1
2. 當輸入為 3~5，輸出值=輸入值乘以 2
3. 當輸入為 6~8，輸出值=輸入值乘以 2 後，再減1
4. 其他輸入，輸出值為 0

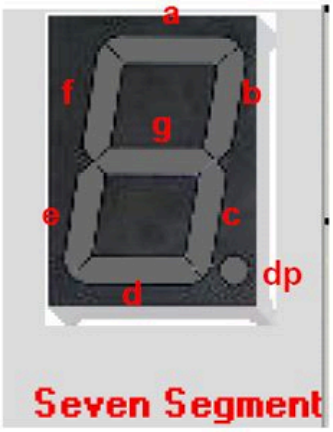
## Logic Gate

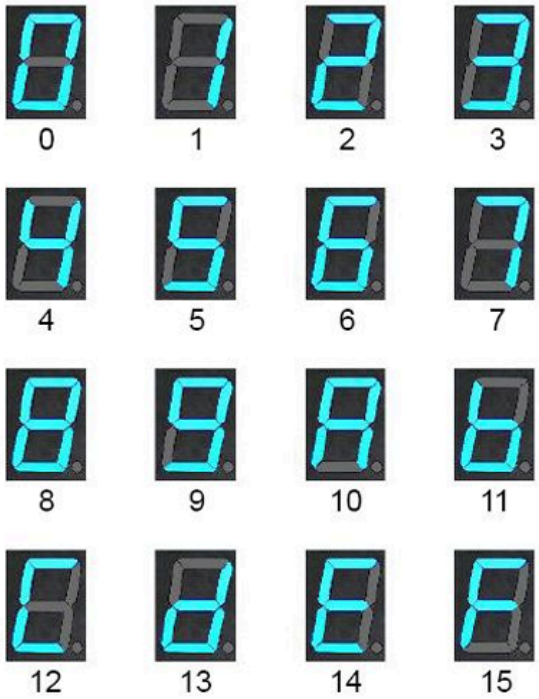



## Seven Display

- 0~15 七段顯示器對應
  - 0: 亮
  - 1: 不亮

```
4'd0: out = 7'b1000000;
4'd1: out = 7'b1111001;
4'd2: out = 7'b0100100;
4'd3: out = 7'b0110000;
4'd4: out = 7'b0011001;
4'd5: out = 7'b0010010;
4'd6: out = 7'b0000010;
4'd7: out = 7'b1111000;
4'd8: out = 7'b0000000;
4'd9: out = 7'b0010000;
4'd10: out = 7'b0001000;
4'd11: out = 7'b0000011;
4'd12: out = 7'b1000110;
4'd13: out = 7'b0100001;
4'd14: out = 7'b0000110;
4'd15: out = 7'b0001110;
```




g a

Ex: 


out=7'b1000000;

g=1

Ex: 


out=7'b0010010;

b=1, e=1

| Signal Name | FPGA Pin No. | Description | Signal Assigned | 對應字母 |
|---|---|---|---|---|
| HEX00 | PIN_C14 | Seven Segment Digit 0[0] | out[0] | a |
| HEX01 | PIN_E15 | Seven Segment Digit 0[1] | out[1] | b |
| HEX02 | PIN_C15 | Seven Segment Digit 0[2] | out[2] | c |
| HEX03 | PIN_C16 | Seven Segment Digit 0[3] | out[3] | d |
| HEX04 | PIN_E16 | Seven Segment Digit 0[4] | out[4] | e |
| HEX05 | PIN_D17 | Seven Segment Digit 0[5] | out[5] | f |
| HEX06 | PIN_C17 | Seven Segment Digit 0[6] | out[6] | g |

# Verilog

```
module main(in, out);
input [3:0] in;
output reg [6:0] out;

always@(*)
begin
        case(in)
                4'b0000: out = 7'b1111001; // out = 0+1
                4'b0001: out = 7'b0100100; // out = 1+1
                4'b0010: out = 7'b0110000; // out = 2+1
                4'b0011: out = 7'b0000010; // out = 3*2
                4'b0100: out = 7'b0000000; // out = 4*2
                4'b0101: out = 7'b0001000; // out = 5*2
                4'b0110: out = 7'b0000011; // out = 6*2-1
                4'b0111: out = 7'b0100001; // out = 7*2-1
                4'b1000: out = 7'b0001110; // out = 8*2-1
                default: out = 7'b1000000;
        endcase
end
endmodule
```