



Department of Computer Science and Information Engineering

National Cheng Kung University

LAB - 05

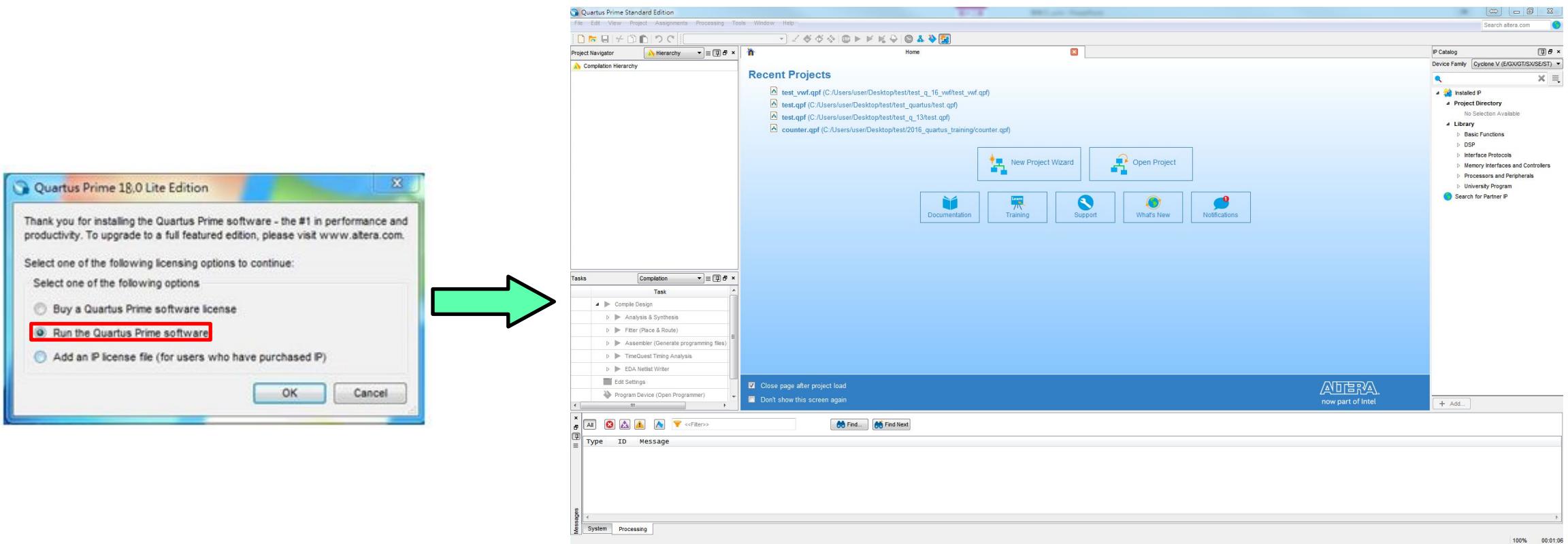
陳培殷老師
國立成功大學 資訊工程系

Digital Integrated Circuit Design Laboratory



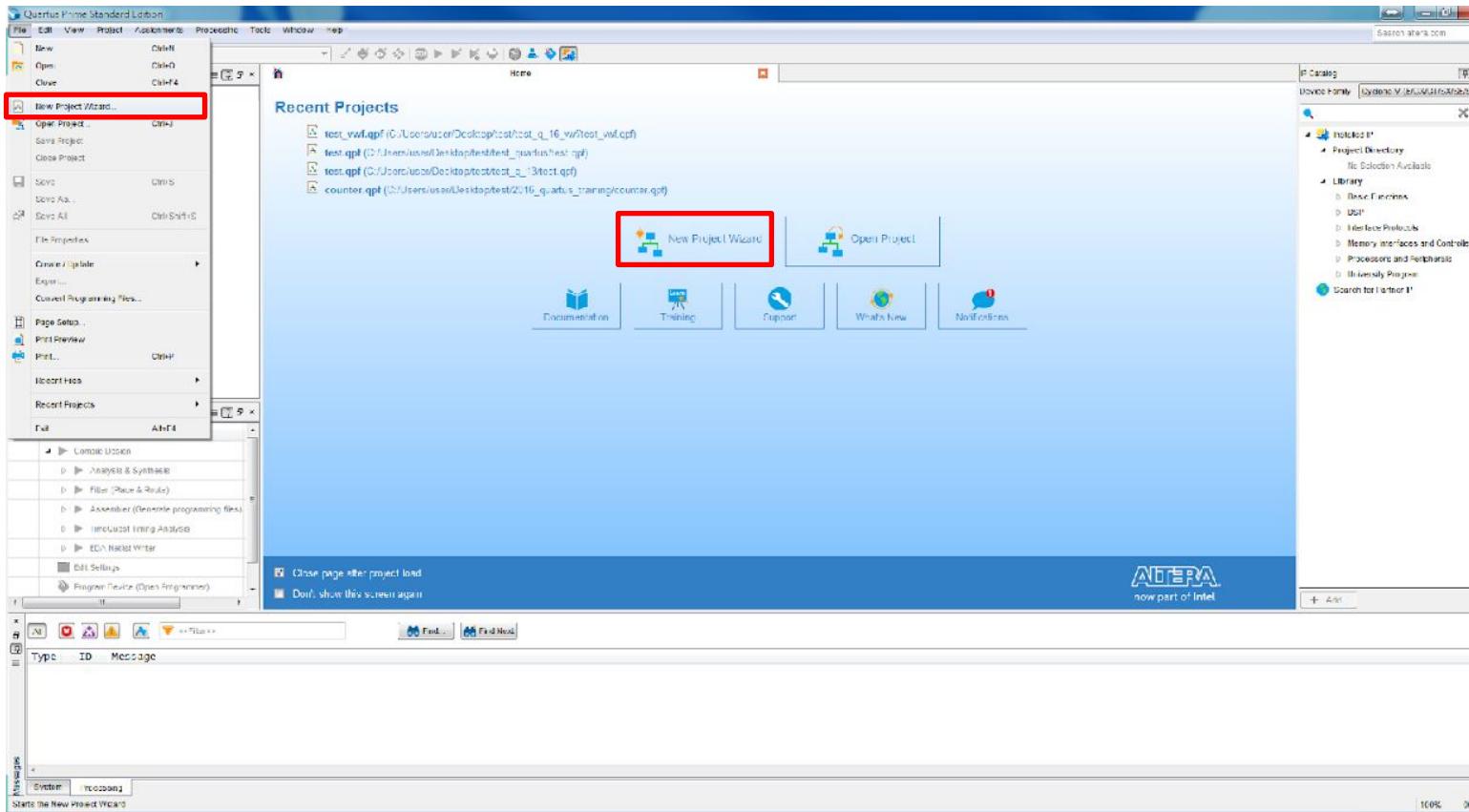
Quartus II Tutorial (1/19)

■ Getting Started – □ Start the Quartus II software



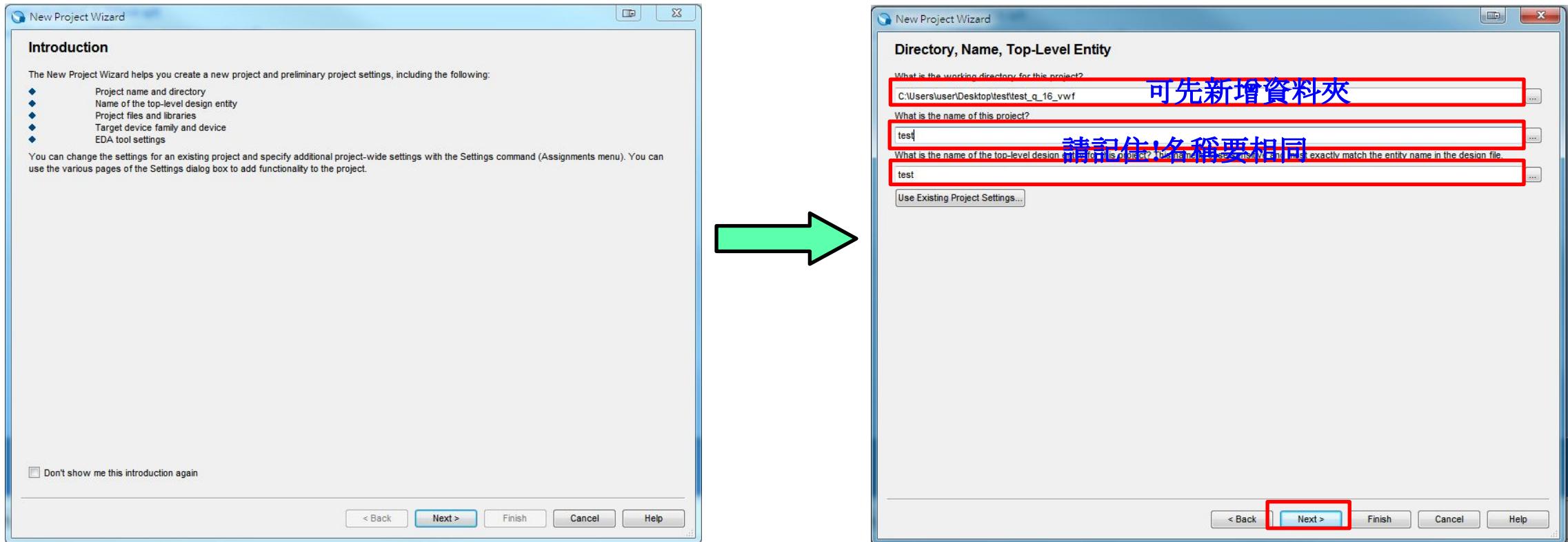
Quartus II Tutorial (2/19)

- Create a New Project –
 - Open New Project Wizard (File → New Project Wizard...)



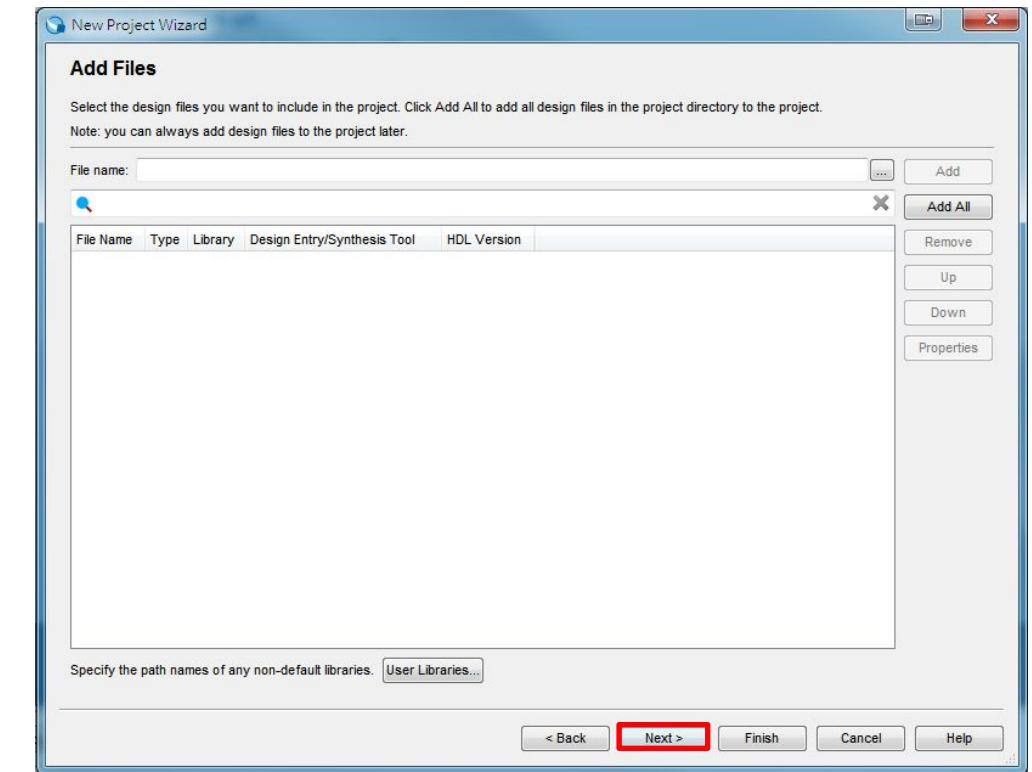
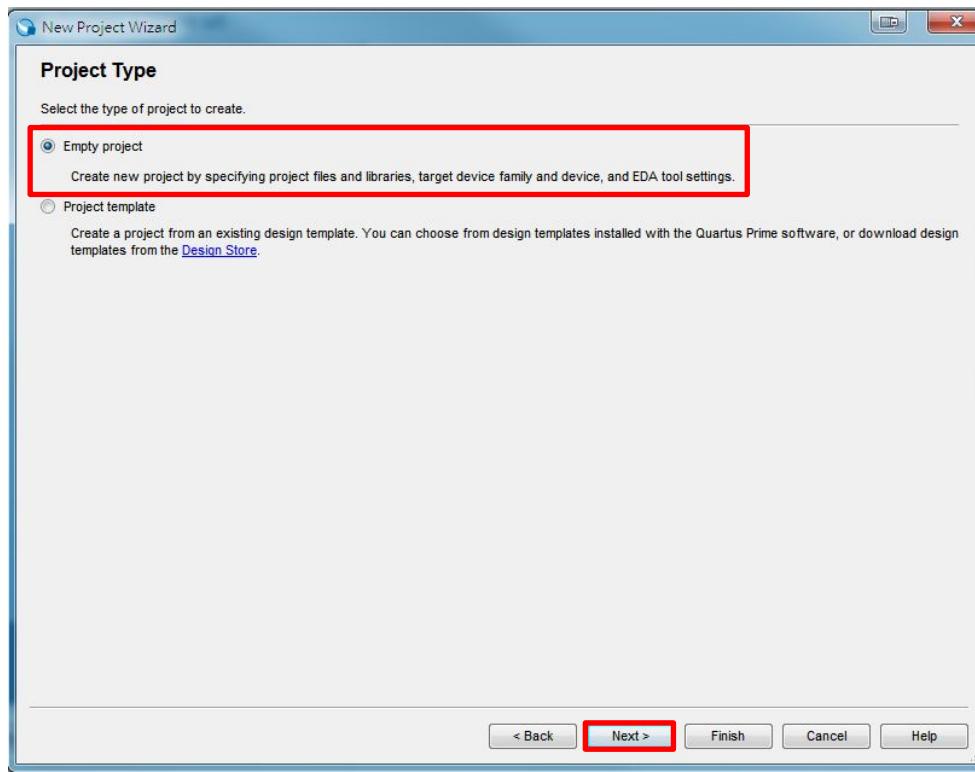
Quartus II Tutorial (3/19)

■ Specify the working directory and the name of the project



Quartus II Tutorial (4/19)

- Select “Empty project”. Then, click “Next”.
- Select design files. Or click “Next” to skip this step.

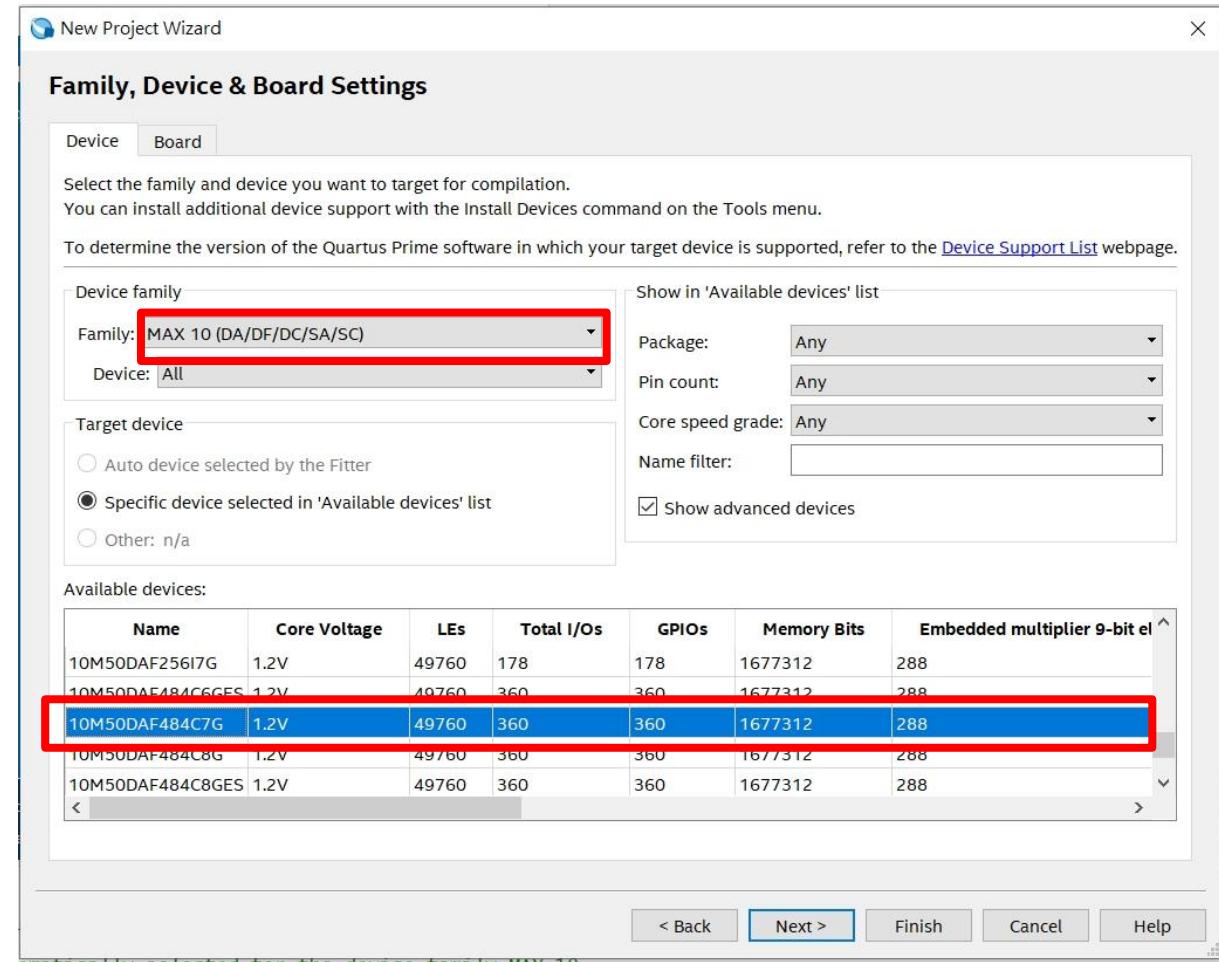


Quartus II Tutorial (5/19)

- Specify device settings - (DE10-Lite Device family are used). Click “Next.”

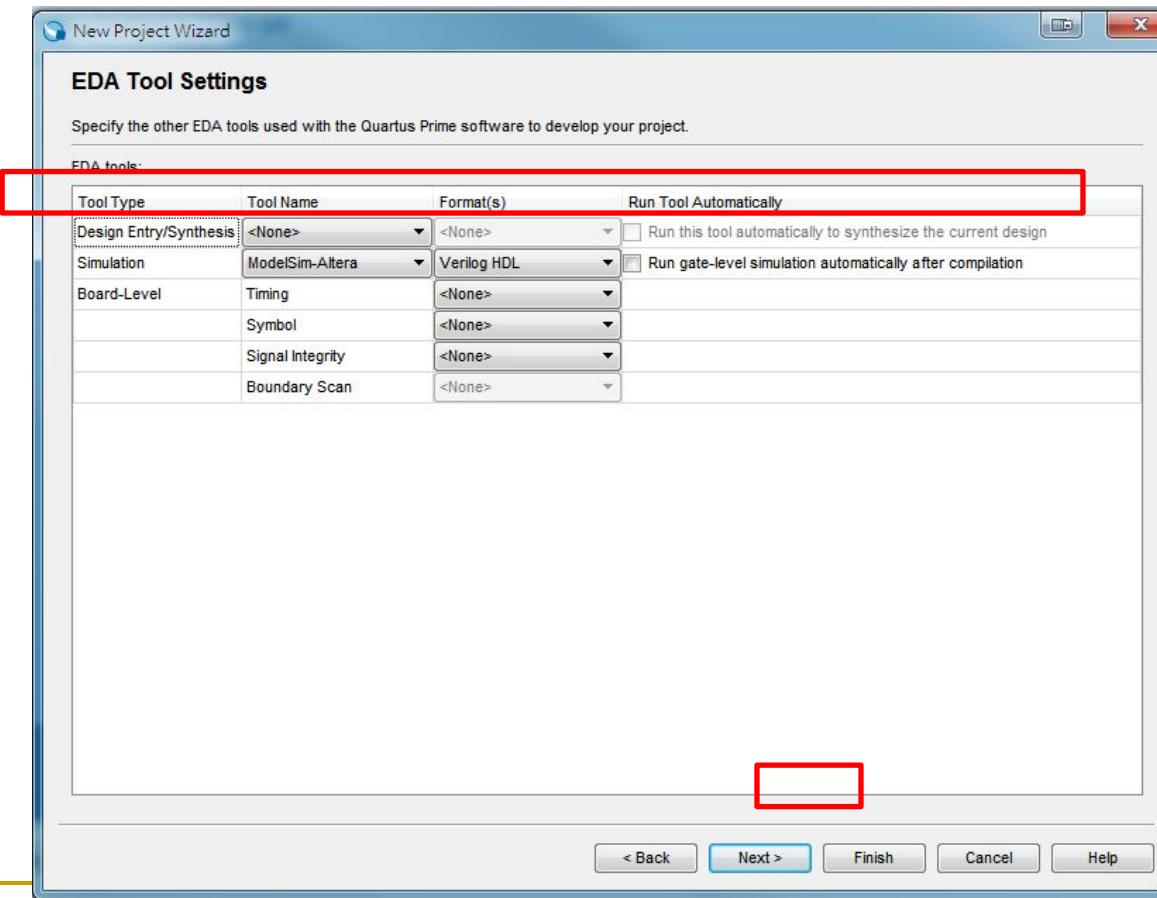
MAX 10(DA/DF/DC/SA/SC)

10M50DAF484C7G



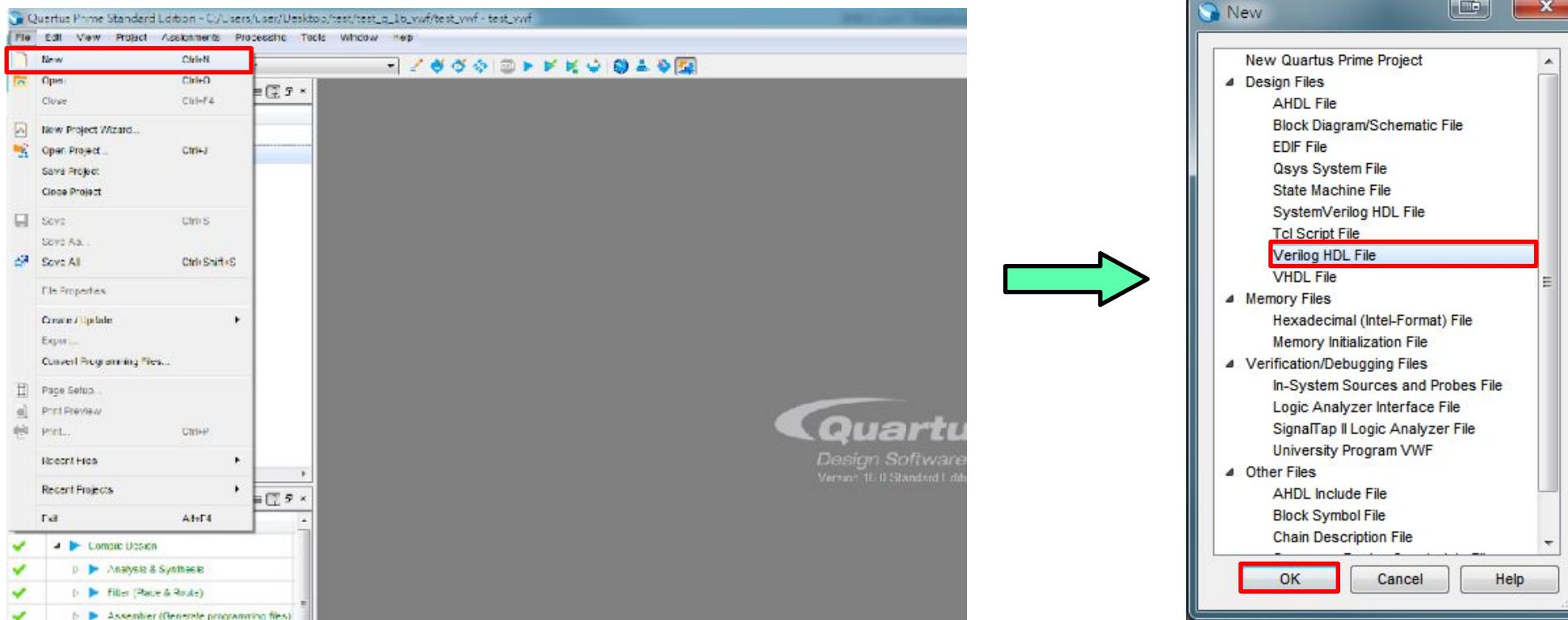
Quartus II Tutorial (6/19)

- Specify EDA Tool – (**Modelsim-Altera** is selected for simulation). Click “Finish.”



Quartus II Tutorial (7/19)

- Edit a new file by opening a Verilog HDL file
 - (File → New → Verilog HDL File → OK)



Quartus II Tutorial (8/19)

■ Write Verilog code

Top module name 一定要跟 Project name 相同 !!

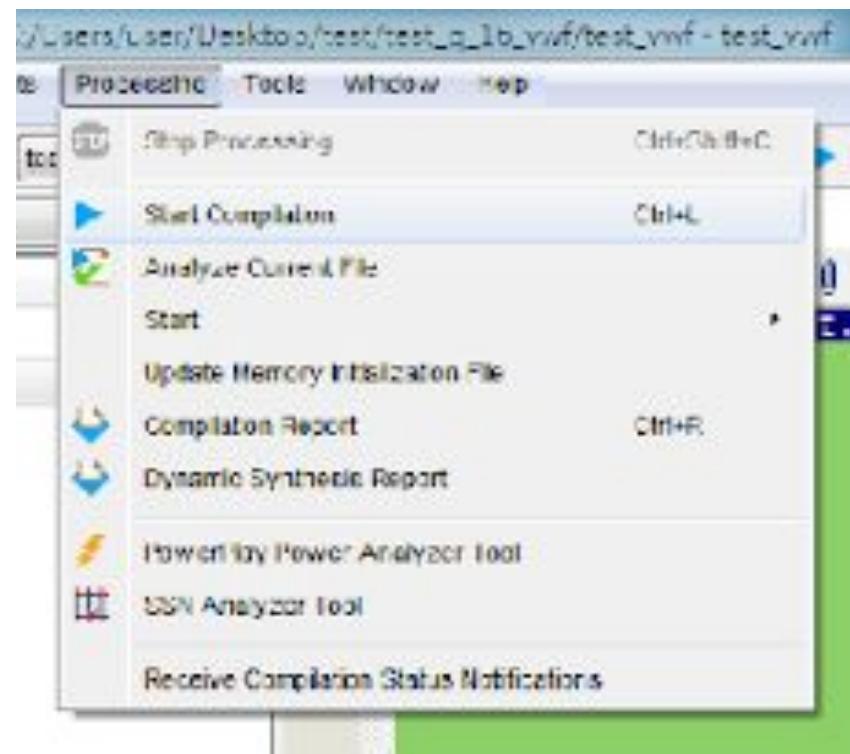
```
1: //File Name : Half_Adder.v
2: module half_adder(a, b, sum, carry);
3: input a, b;
4: output sum, carry;
5:
6: assign sum = a ^ b;
7: assign carry = a & b;
8:
9: endmodule
```

輸入(input)		輸出(output)	
被加數(a)	加數(b)	和(sum)	進位(carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



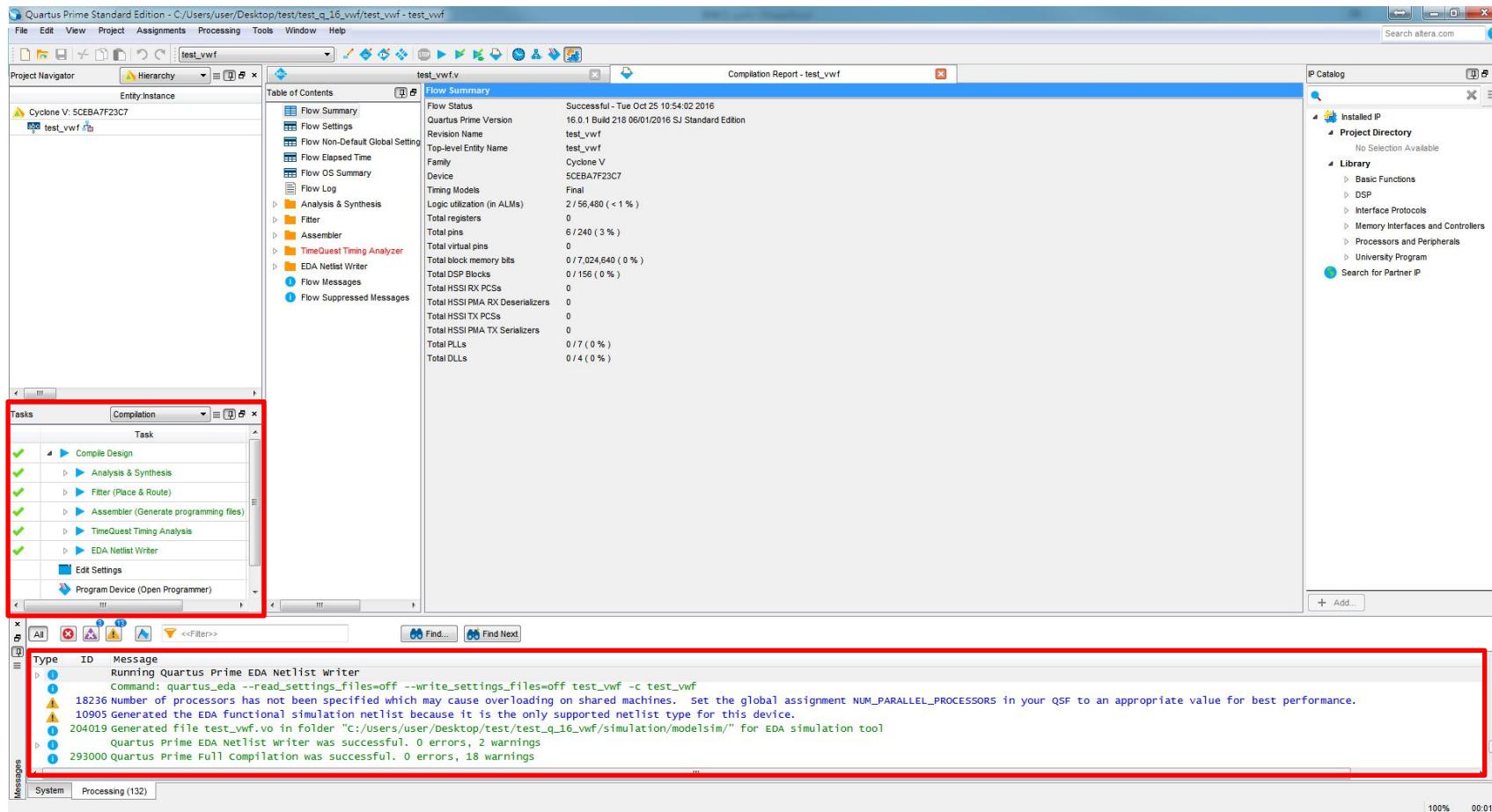
Quartus II Tutorial (9/19)

- Compiling the Designed Circuit (synthesis 合成)
 - (Processing → Start Compilation)



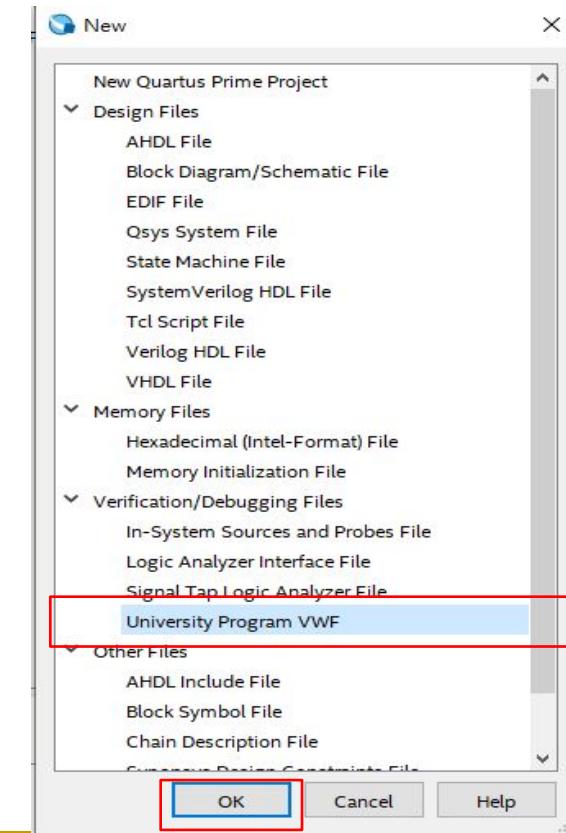
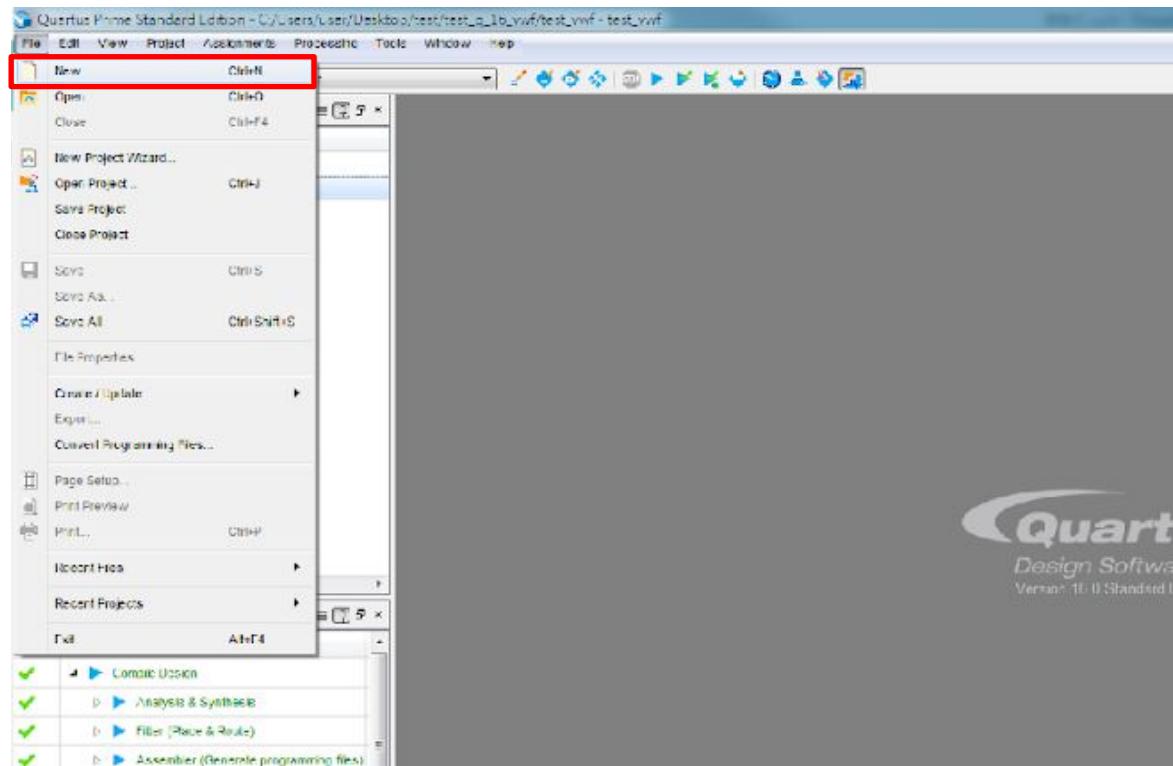
Quartus II Tutorial (10/19)

■ Successful compilation



Quartus II Tutorial (11/19)

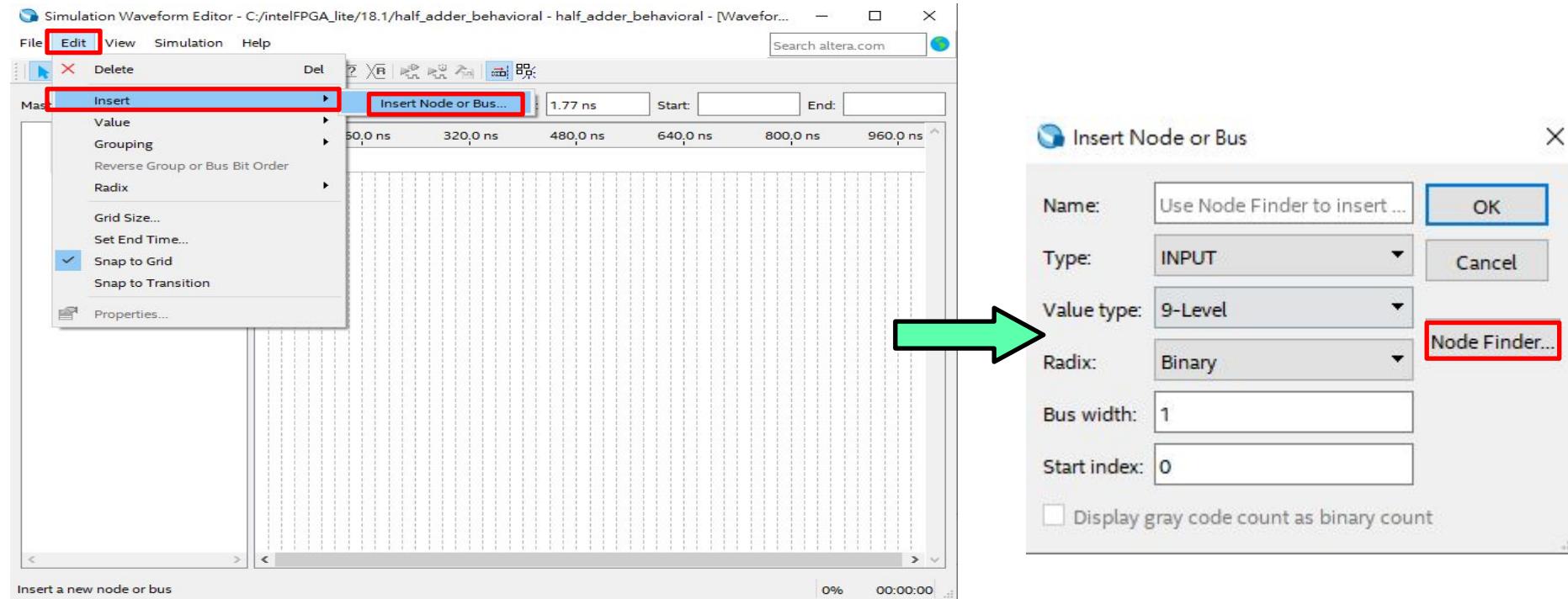
- Edit a new file by opening a Verilog HDL file
 - (File → New → University Program VWF → OK)



Quartus II Simulation (12/19)

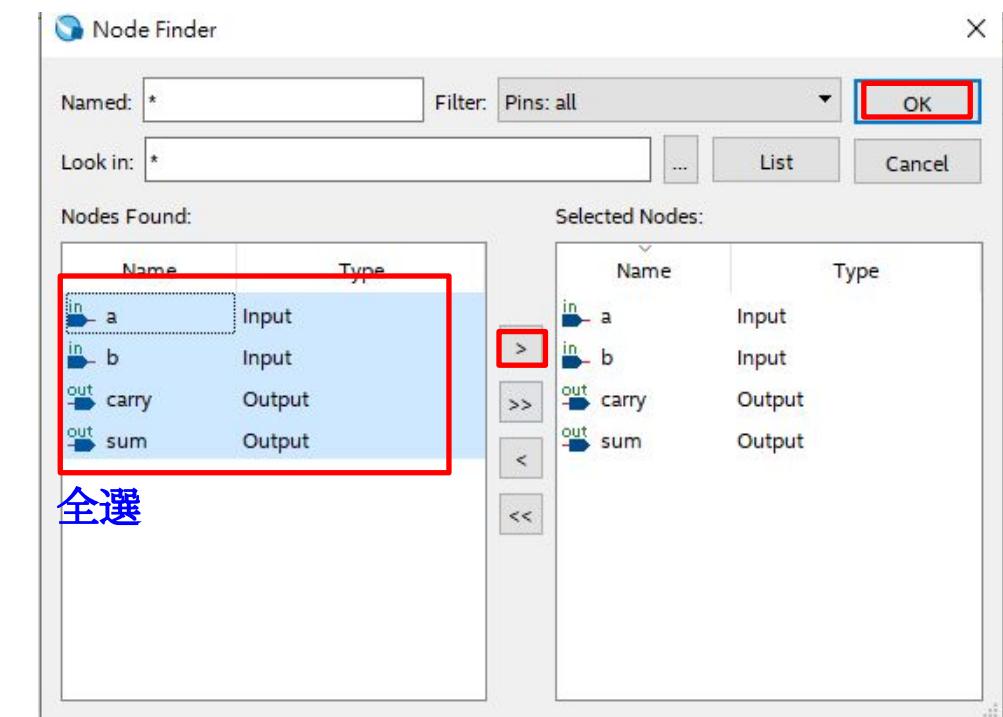
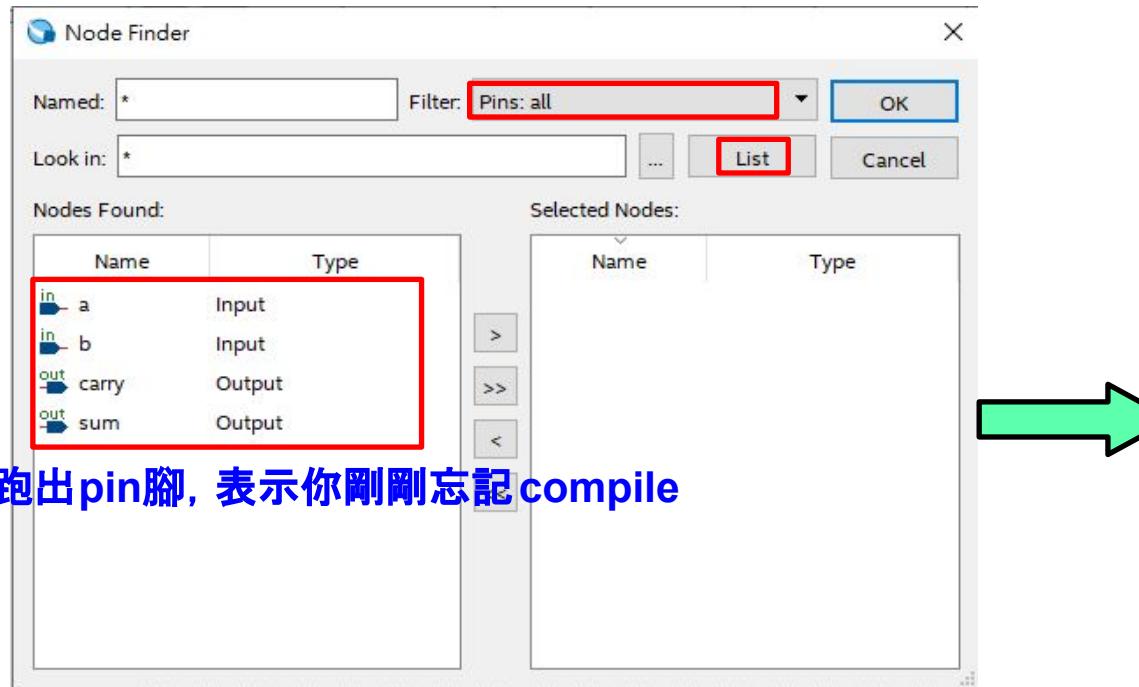
■ Simulating the Designed Circuit

- Use node finder to find all the I/O pins (Edit → Insert → Insert Node or Bus...)



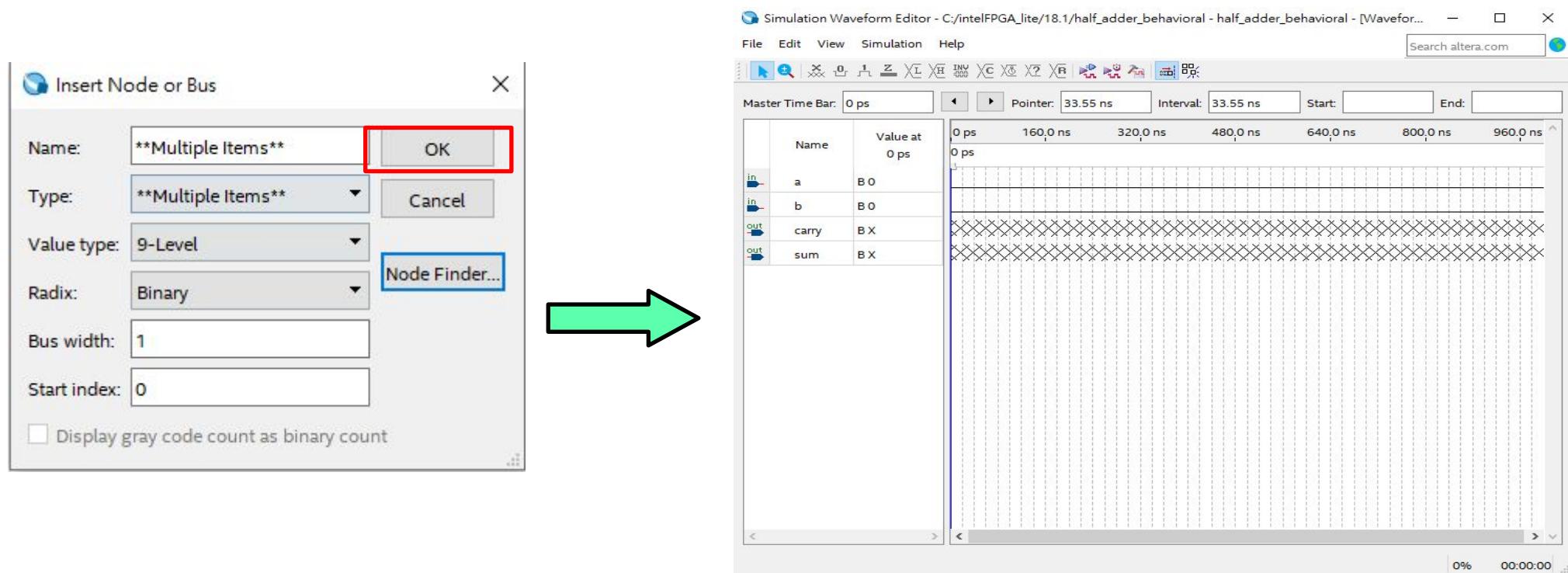
Quartus II Simulation (13/19)

- Simulating the Designed Circuit
 - Selecting nodes to insert into the Waveform Editor



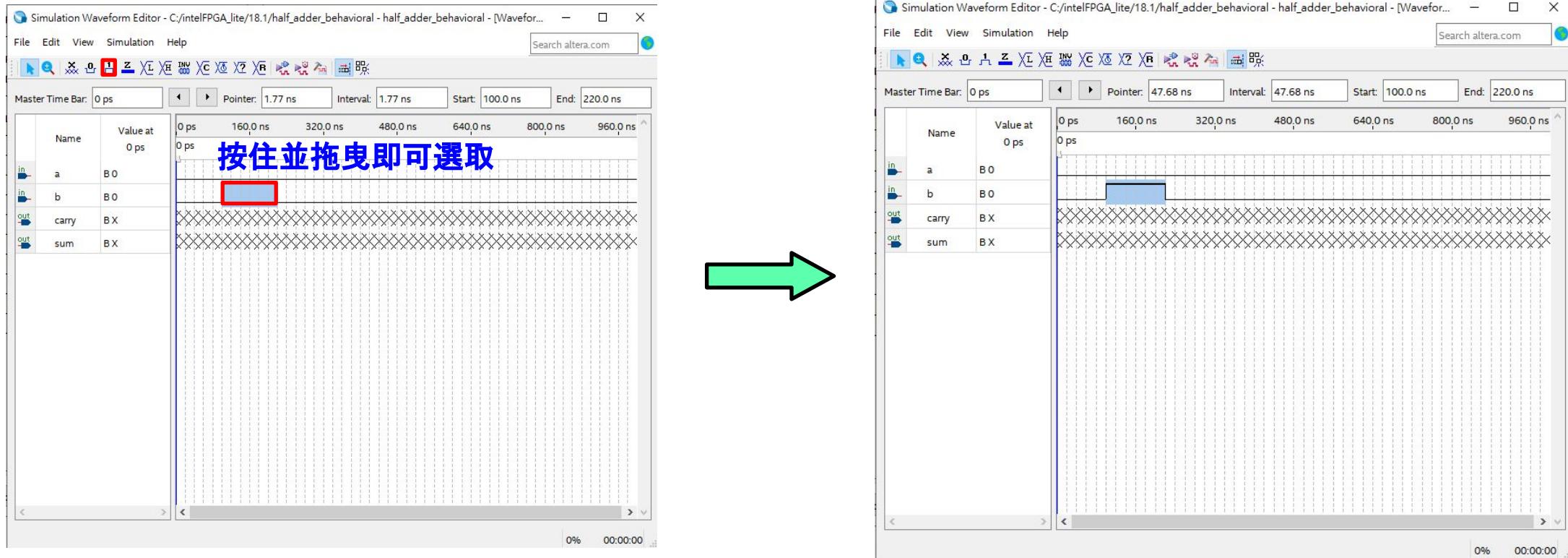
Quartus II Simulation (14/19)

- Simulating the Designed Circuit
 - Selecting nodes to insert into the Waveform Editor



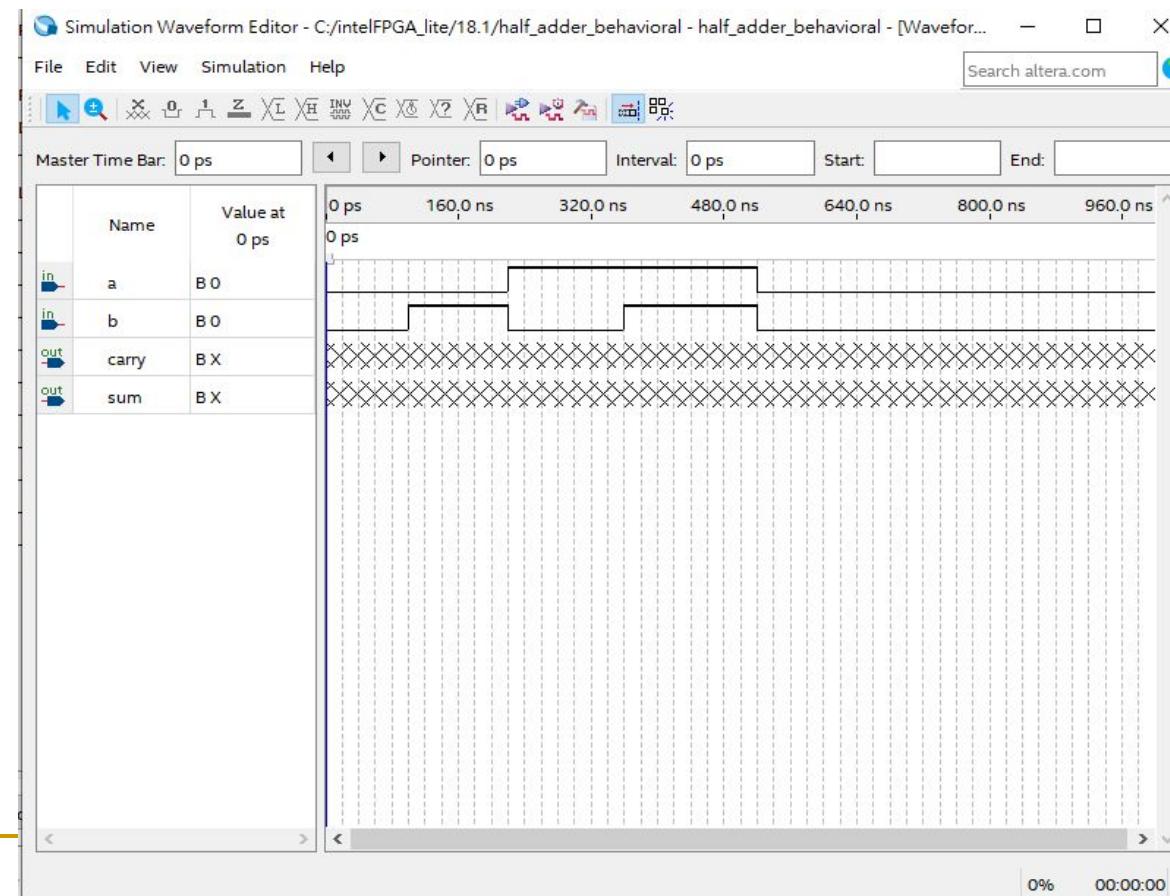
Quartus II Simulation (15/19)

- Simulating the Designed Circuit
 - Select and edit waveform



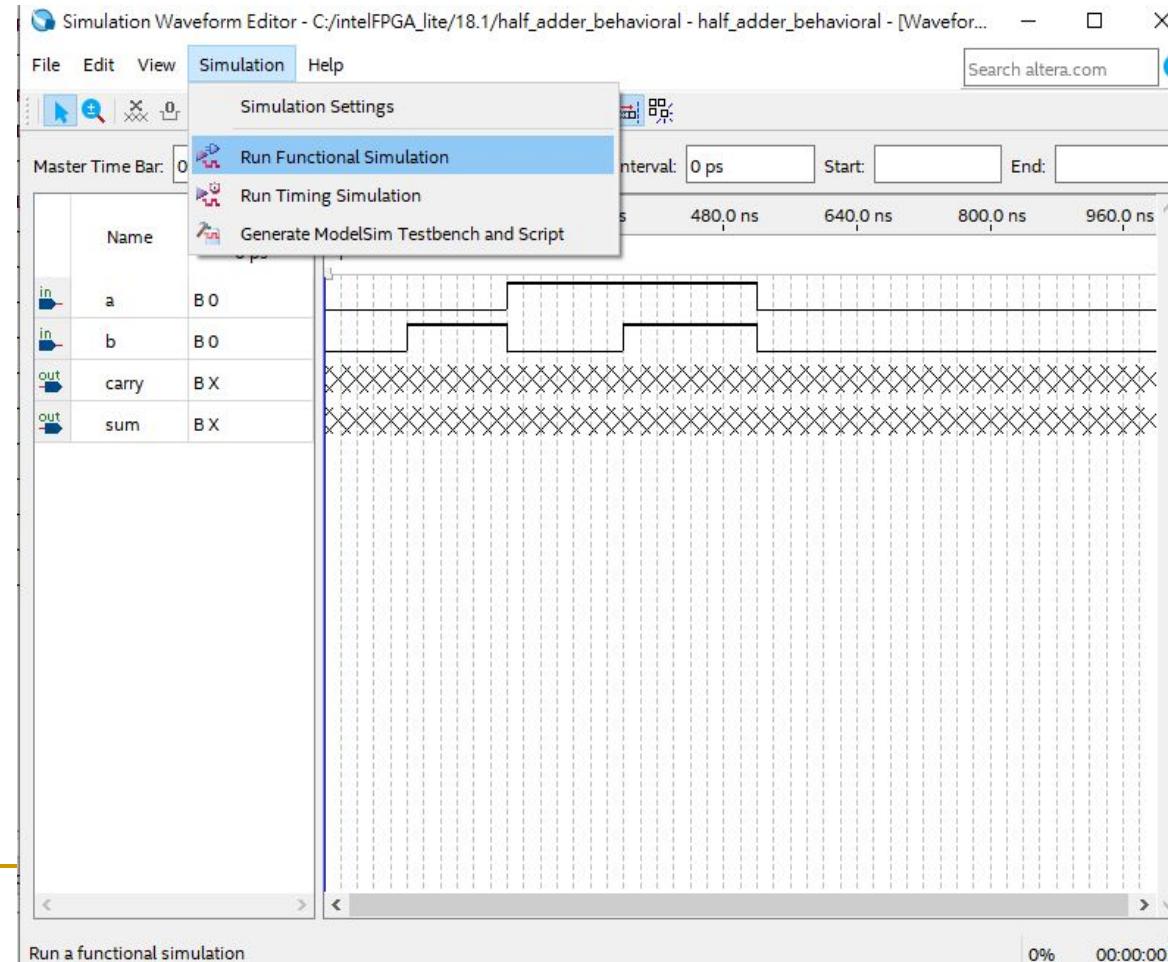
Quartus II Simulation (16/19)

- Simulating the Designed Circuit
 - Setting of test values



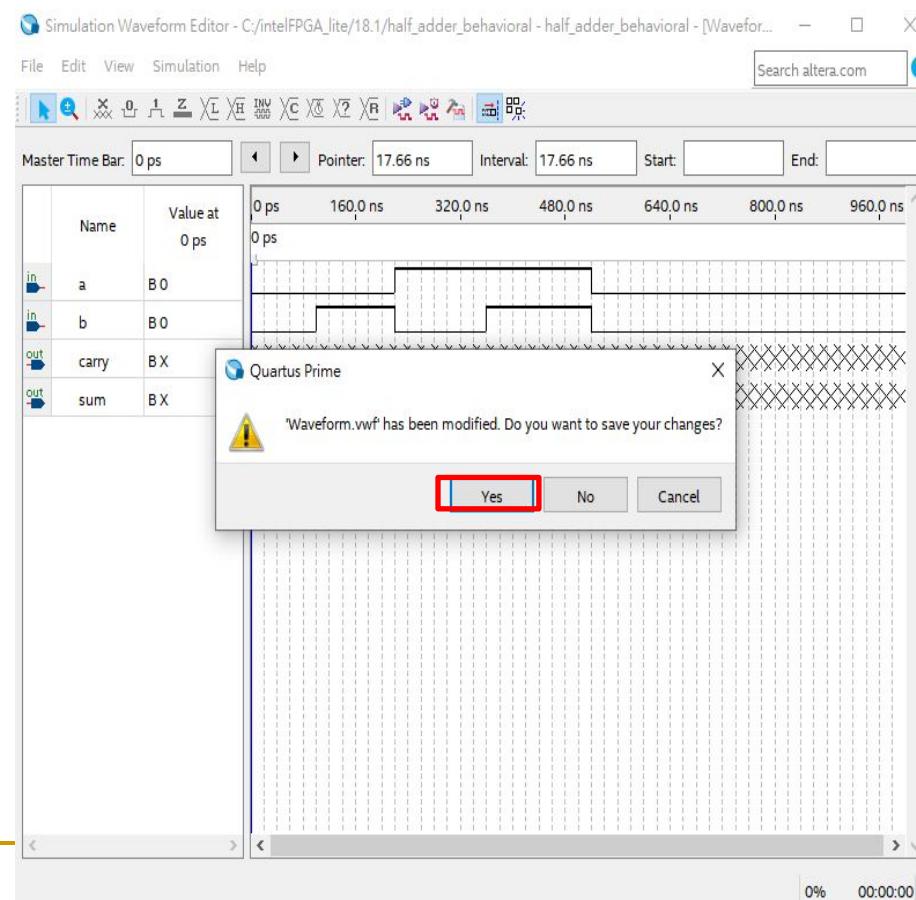
Quartus II Simulation (17/19)

- Simulating the Designed Circuit
 - Run Functional Simulation



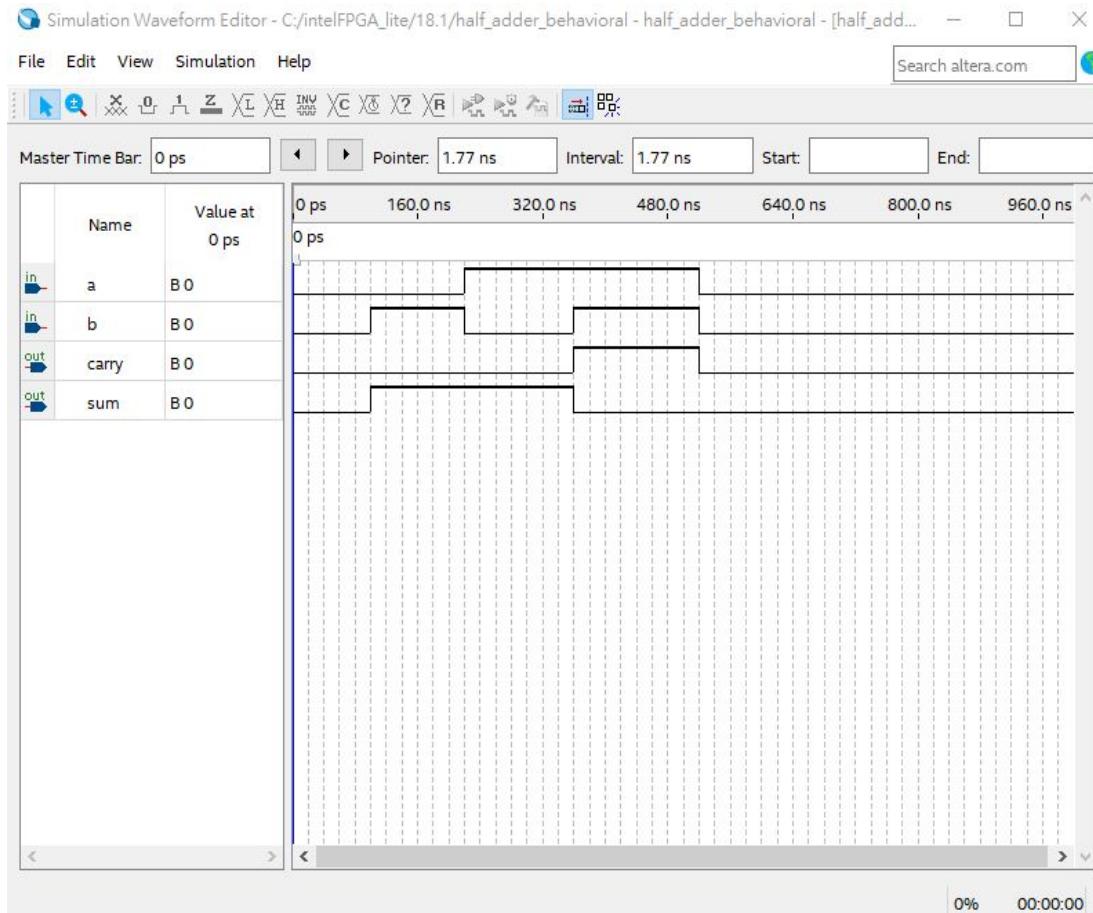
Quartus II Simulation (18/19)

- Simulating the Designed Circuit
 - Save .vwf



Quartus II Simulation (19/19)

The result of functional simulation

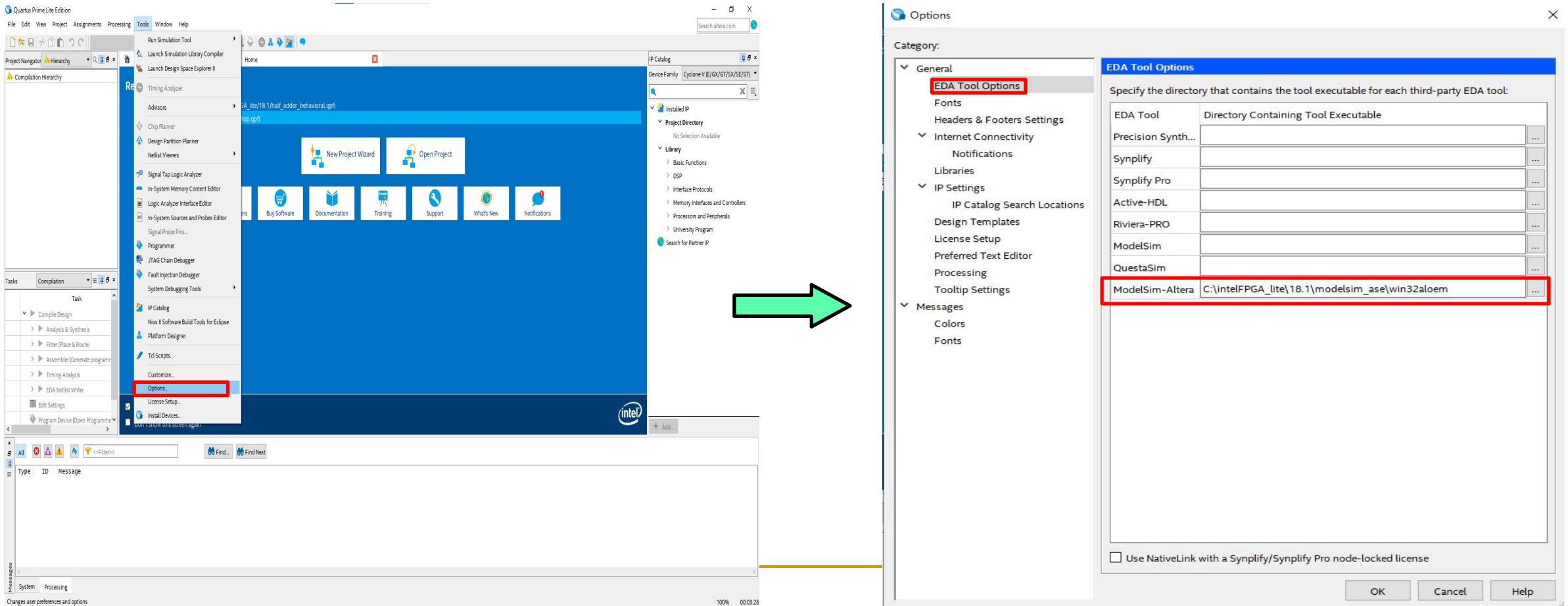


輸入(input) 被加數 (a)	輸入(input) 加數(b) (b)	輸出(output) 和 (sum)	輸出(output) 進位 (carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Quartus II Simulation Notice

■ 如果simulation時出現error, 修改ModelSim-Altera路徑

- 個人電腦 : (Tools → Options → EDA Tool Options → ModelSim-Altera → C:\intelFPGA_lite\18.1\modelsim_ase\win32aloem)
- 實驗室電腦 : (Tools → Options → EDA Tool Options → ModelSim-Altera → C:\intelFPGA\16.1\modelsim_ase\win32aloem)



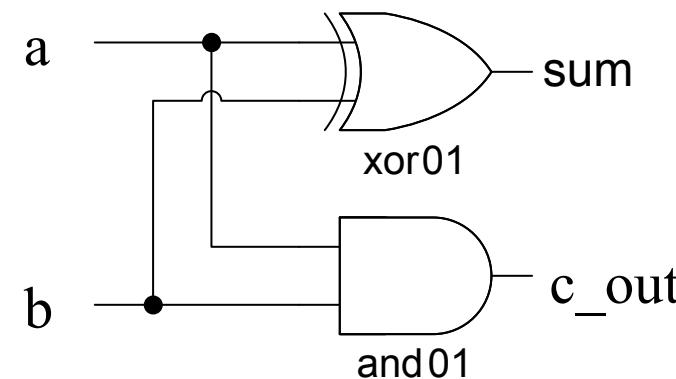
Lab I - Half Adder

a\b\	0	1
0	0	1
1	1	0

$$\text{sum} = a \oplus b$$

a\b\	0	1
0	0	0
1	0	1

$$c_{\text{out}} = ab$$



Lab I - Half Adder

- **(a) Using Verilog to implement a 1-bit Half Adder**

Please implement with 3 methods

- 1) **Structural description**
- 2) **Data flow description**
- 3) **Behavioral description**

- **(b) Simulation with waveform**

Lab I - Hint

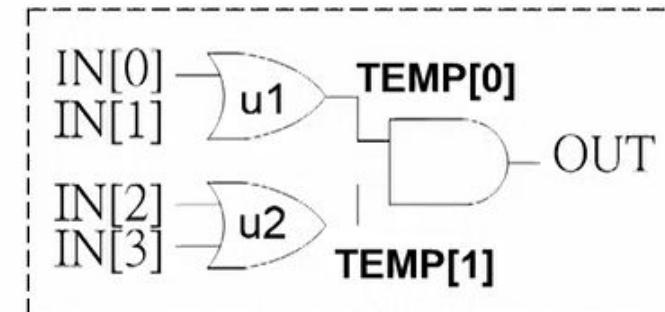
Structural Description

Verilog allows three kinds of descriptions for circuits:

- (1) Structural description (2) Data flow description (3) Behavioral description

Structural description:

```
1. module OR_AND_STRUCTURAL(IN,OUT);  
  
2.     input      [3:0]    IN;  
3.     output      OUT;  
4.     wire       [1:0]    TEMP;  
  
5.     or u1(TEMP[0], IN[0], IN[1]);  
6.     or u2(TEMP[1], IN[2], IN[3]);  
7.     and (OUT, TEMP[0], TEMP[1]);  
8. endmodule
```



***Synthesized (synthesis) +
optimized by tools***

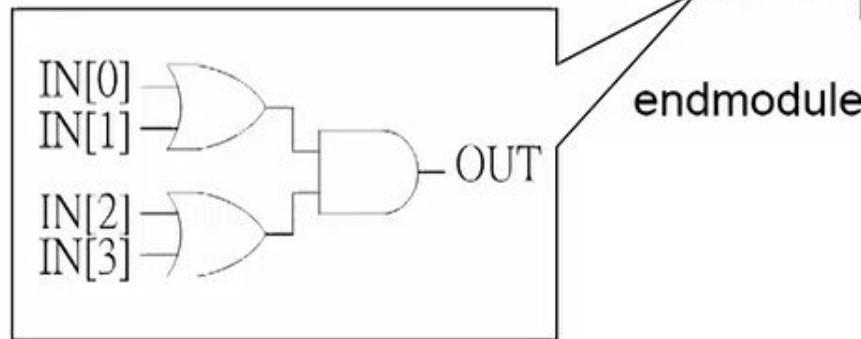
Lab I - Hint

Data Flow Description

Data flow description

1. module OR_AND_DATA_FLOW(IN, OUT);
2. input [3:0] IN;
3. output OUT;
4. assign OUT = (IN[0] | IN[1]) & (IN[2] | IN[3]);

*Synthesized and
optimized by tools*



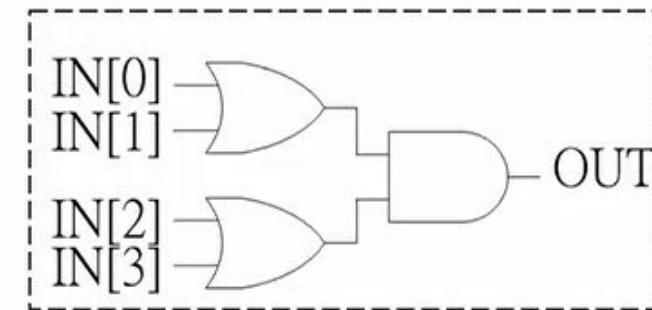
endmodule

Lab I - Hint

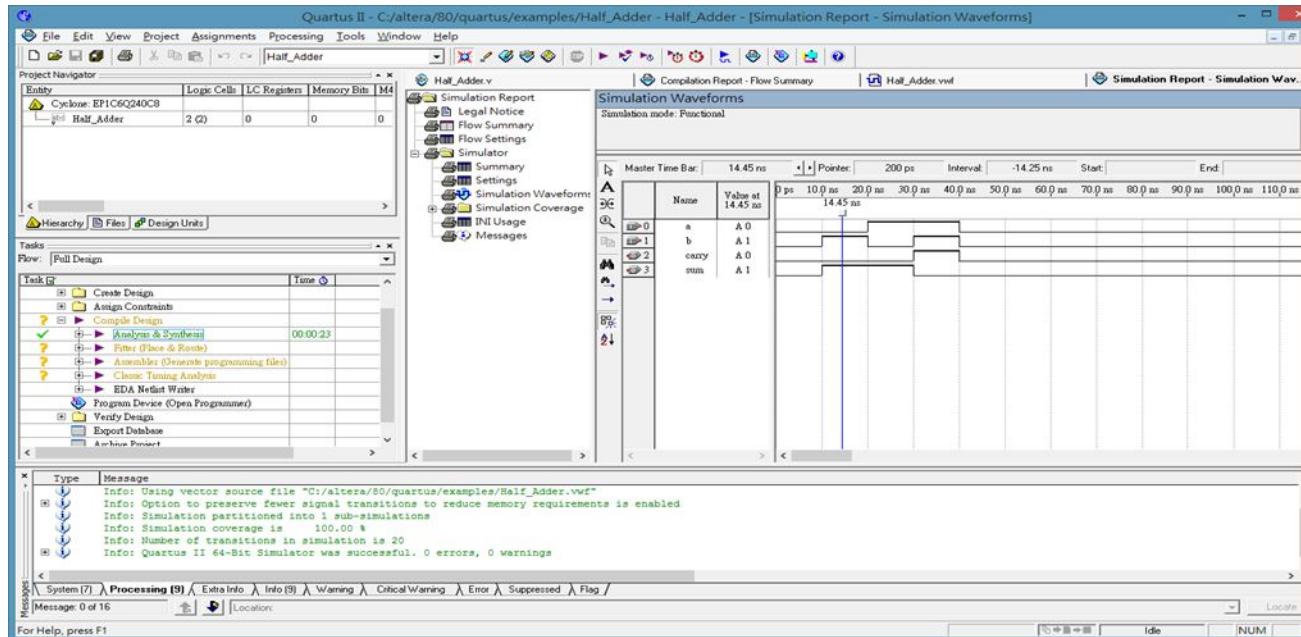
Behavioral (RTL) Description

Behavioral description

```
1. module OR_AND_BEHAVIORAL(IN, OUT);  
2.   input [3:0]  IN;  
3.   output      OUT;  
4.   reg        OUT;  
5.  
6.   always @(IN)  
7.     begin  
8.       OUT = (IN[0] | IN[1]) & (IN[2] | IN[3]);  
9.     end  
10.    endmodule
```



Lab I - Simulation with waveform



a	b	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Lab II - Full Adder (1/2)

ab\c_in	0	1
00	0	1
01	1	0
11	0	1
10	1	0

sum

$$= \underline{\overline{a}} \underline{\overline{b}} \underline{\overline{c}}_{in} + \underline{\overline{a}} \underline{b} \underline{\overline{c}}_{in} + \underline{a} \underline{\overline{b}} \underline{\overline{c}}_{in} + \underline{a} \underline{b} \underline{c}_{in}$$

$$= (\underline{\overline{a}}b + \underline{a}\underline{\overline{b}})c_{in} + (\underline{\overline{a}}b + \underline{a}\underline{b})\underline{c}_{in}$$

$$= (a \oplus b)c_{in} + (a \oplus b)\underline{c}_{in}$$

$$= (a \oplus b) \oplus c_{in}$$

ab\c_in	0	1
00	0	0
01	0	1
11	1	1
10	0	1

c_out

$$= ab + \underline{\overline{a}} \underline{\overline{b}} \underline{\overline{c}}_{in} + \underline{\overline{a}} \underline{b} \underline{\overline{c}}_{in}$$

$$= ab + (\underline{\overline{a}}b + \underline{a}\underline{\overline{b}})c_{in}$$

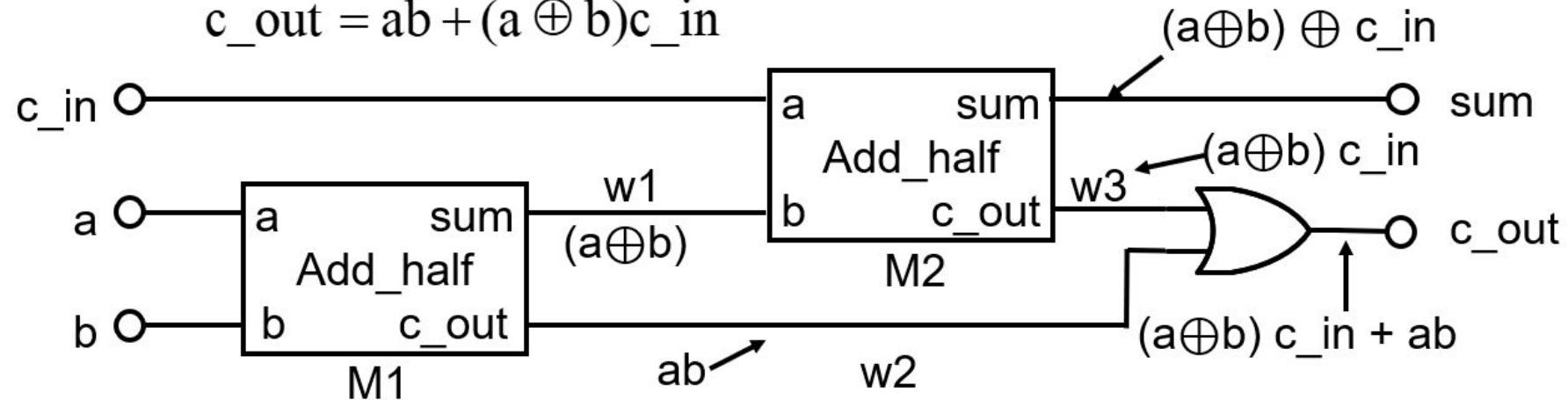
$$= ab + (a \oplus b)c_{in}$$

Lab II - Full Adder (2/2)

You can implement a full adder with (2 half adder and 1 or gate).

$$\text{sum} = (a \oplus b) \oplus c_{\text{in}}$$

$$c_{\text{out}} = ab + (a \oplus b)c_{\text{in}}$$



Lab II - Full Adder

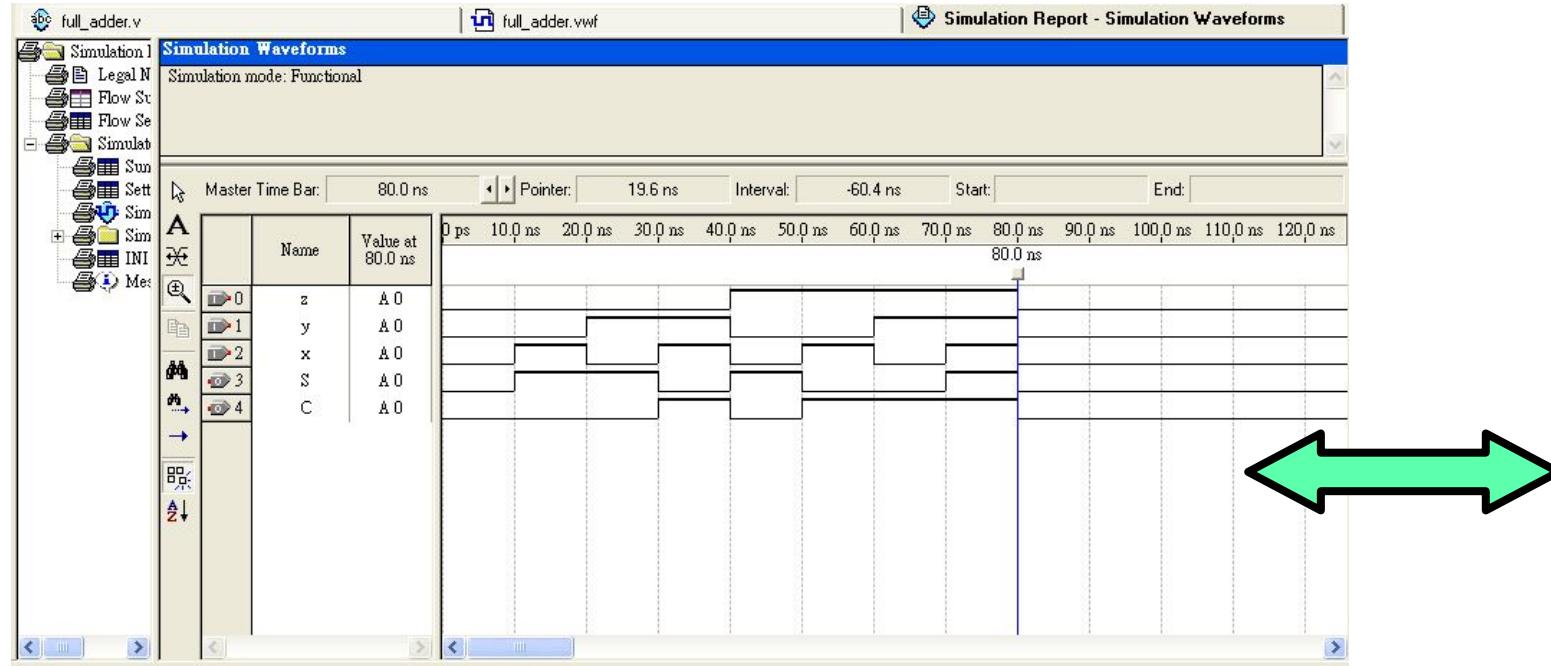
- **(a) Using Verilog to implement a 1-bit Full Adder**

Please implement with 3 methods

- 1) **Structural description**(with 2 half adder + 1 or gate)
- 2) **Data flow description**
- 3) **Behavioral description**

- **(b) Simulation with waveform**

Lab II - Simulation with waveform



z	y	x	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Notice

- 請勿在桌面建立 Project 及請勿命名中文資料夾
- Device family 請確認與 FPGA Chip 符合 (**10M50DAF484C7G**)
- Top module name & Project name 需要一致
- 確認 `module ... endmodule` 為keyword 變成**藍色字體**