



LAB - 07

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新板子

- Specify device settings - (DE10-Lite Device family are used). Click “Next.”

MAX 10(DA/DF/DC/SA/SC)

10M50DAF484C7G

New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: MAX 10 (DA/DF/DC/SA/SC)

Device: All

Target device

☐ Auto device selected by the Filter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter:

☒ Show advanced devices

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-bit el
10M50DAF256I7G	1.2V	49760	178	178	1677312	288
10M50DAF484C6GES	1.2V	49760	360	360	1677312	288
10M50DAF484C7G	1.2V	49760	360	360	1677312	288
10M50DAF484C8G	1.2V	49760	360	360	1677312	288
10M50DAF484C8GES	1.2V	49760	360	360	1677312	288

< Back Next > Finish Cancel Help

舊板子

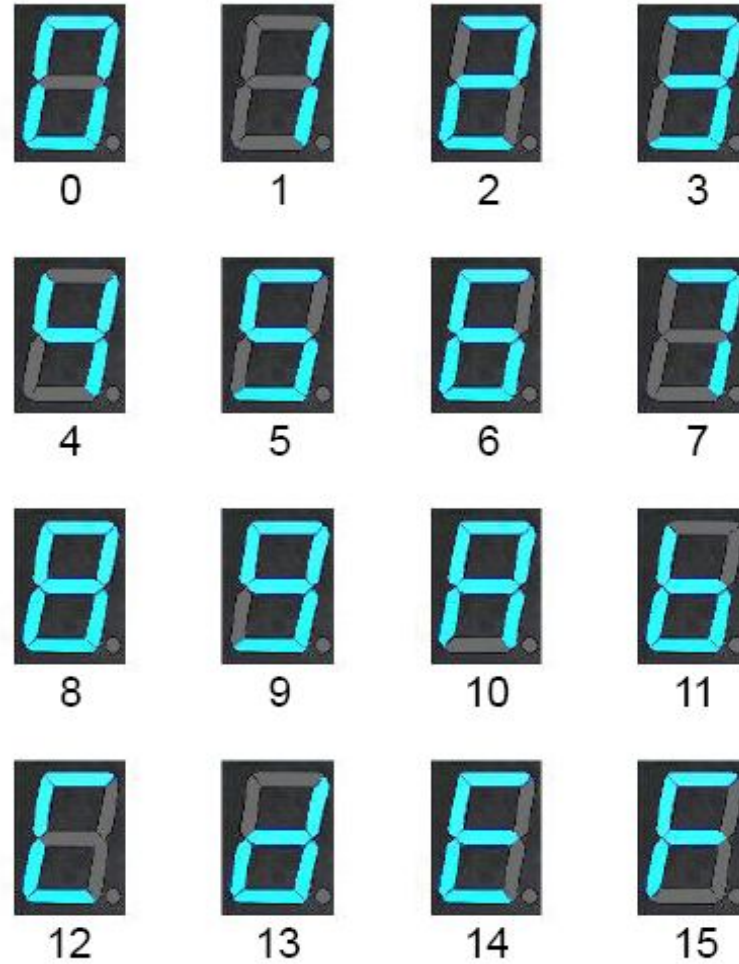
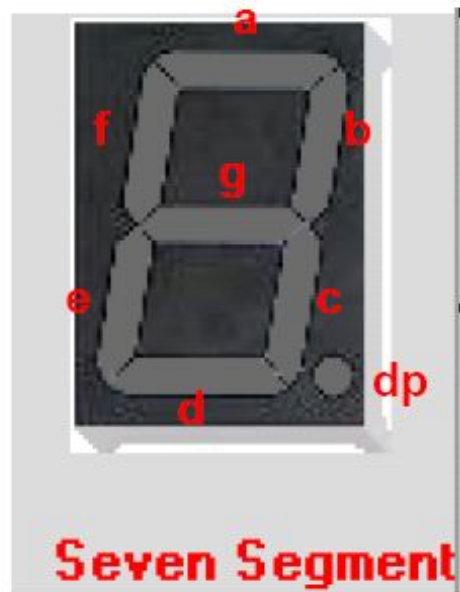
- Specify device settings - (DE0-CV Device family are used). Click “Next.”

5CEFA4F23C7

The screenshot shows the 'New Project Wizard' dialog box, specifically the 'Family, Device & Board Settings' tab. The 'Device' sub-tab is selected. The 'Device family' dropdown is set to 'Cyclone V (E/GX/GT/SX/SE/ST)'. The 'Available devices' table lists several Cyclone V devices, with '5CEFA4F23C7' highlighted. The 'Next >' button is highlighted.

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS	PCIe Hi
SCEFA2F23I7	1.1V	9430	224	224	0	0	0
5CEFA4F23C7	1.1V	18480	224	224	0	0	0
5CEFA4F23I7	1.1V	18480	224	224	0	0	0
5CEFA5F23C7	1.1V	29080	240	240	0	0	0
5CEFA5F23I7	1.1V	29080	240	240	0	0	0

Seven-segment display (1/3)



Seven-segment display (2/3)

- 0 is on, 1 is off
- dp is useless in DE10_Lite board


■ Ex:  0 `out=7'b10000000;`

Diagram illustrating the segment states for displaying '0':

- Segment 'g' (middle horizontal bar) is on (1).
- Segment 'a' (top horizontal bar) is off (0).
- Segments 'b', 'c', 'd', 'e', and 'f' are all off (0).

g ← a

■ Ex:  5 `out=7'b0010010;`

Diagram illustrating the segment states for displaying '5':

- Segment 'b' (top-left vertical bar) is on (1).
- Segment 'e' (bottom-left vertical bar) is on (1).
- Segment 'd' (bottom horizontal bar) is on (1).
- Segments 'a', 'c', 'f', and 'g' are all off (0).

b=1, e=1

Seven-segment display (3/3) 新板子

- Assign out to seven segment digit pin of FPGA
 - Take seven segment digit 0 as example

Signal Name	FPGA Pin No.	Description	Signal Assigned	對應字母
HEX00	PIN_C14	Seven Segment Digit 0[0]	out[0]	a
HEX01	PIN_E15	Seven Segment Digit 0[1]	out[1]	b
HEX02	PIN_C15	Seven Segment Digit 0[2]	out[2]	c
HEX03	PIN_C16	Seven Segment Digit 0[3]	out[3]	d
HEX04	PIN_E16	Seven Segment Digit 0[4]	out[4]	e
HEX05	PIN_D17	Seven Segment Digit 0[5]	out[5]	f
HEX06	PIN_C17	Seven Segment Digit 0[6]	out[6]	g

Seven-segment display (3/3) 舊板子

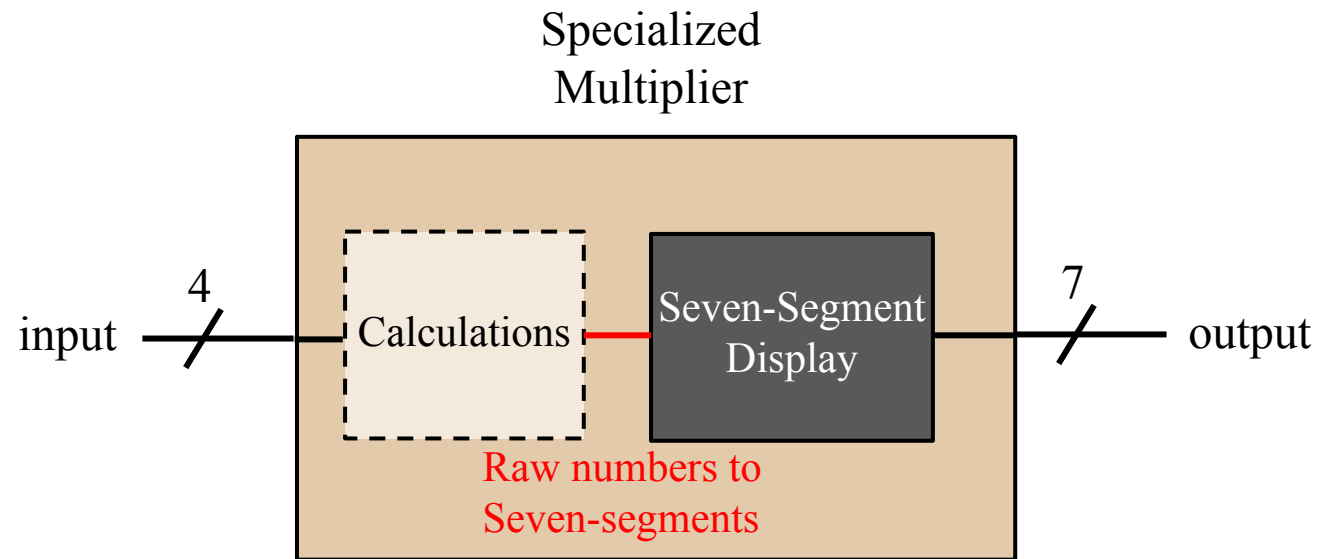
- Assign out to seven segment digit pin of FPGA
 - Take seven segment digit 0 as example

Signal Name	FPGA Pin No.	Description	Signal Assigned	
HEX00	PIN_U21	Seven Segment Digit 0[0]	out[0]	a
HEX01	PIN_V21	Seven Segment Digit 0[1]	out[1]	b
HEX02	PIN_W22	Seven Segment Digit 0[2]	out[2]	c
HEX03	PIN_W21	Seven Segment Digit 0[3]	out[3]	d
HEX04	PIN_Y22	Seven Segment Digit 0[4]	out[4]	e
HEX05	PIN_Y21	Seven Segment Digit 0[5]	out[5]	f
HEX06	PIN_AA22	Seven Segment Digit 0[6]	out[6]	g

Lab I 特殊功能乘法器

- 設計一個特殊功能乘法器並將結果以七段顯示器表示
- 功能說明：
 - 當輸入為 0~2, 輸出值=輸入值+1
 - 當輸入為 3~5, 輸出值=輸入值乘以 2
 - 當輸入為 6~8, 輸出值=輸入值乘以 2 後, 再減1
 - 其他輸入, 輸出值為 0
- 輸入為4 bits SW3~SW0
- 輸出為7 bits HEX06~HEX00

Hint



Notice for Lab I

▣ 輸入為 0~2

- 輸出值=輸入值再加1
- Ex: in=1, out=2;



▣ 當輸入為 3~5

- 輸出值=輸入值乘以 2
- Ex: in=3, out=6;



▣ 輸入為 6~8

- 輸出值=輸入值乘以 2 後, 再減1
- Ex: in=8, out=15 (F);



▣ 其他輸入

- 輸出值為 0
- Ex: in=12, out=0;



Notice

- 請勿命名中文或數字開頭的資料夾
- Device family 請確認與 FPGA Chip 符合 (10M50DAF484C7G)
- Top module name & Project name 需要一致
- 在組合電路中, case、if...else...若沒有寫滿, 合成後會產生latch