CHENGYI ZHANG

+1(341) 766-9131 ◇ Berkeley, CA
iansseijelly@berkeley.edu ◇ Github Page ◇ Personal Site

EDUCATION

University of California, Berkeley, Bachelor of Arts, Computer Science — Expected 2024
GPA: **3.978**/4 (Dean's List)
Selected Coursework: **EECS151** Digital Design and Integrated Circuits, **CS152** Computer Architecture and Engineering, **ELENG105** Microelectronic Devices and Circuits, **EECS251B** Advanced Digital Circuits, **CS61C** Computer Architecture & Machine Structures, **ELENG140** Linear Integrated Circuits

SKILLS

Digital Design	Verilog, Chisel, Vivado, Chipyard, Firesim, VCS, Verilator, Innovus, Genus, Voltus
Analog Design	Cadence Virtuoso, ADE-L Simulation, Spice Simulation
Programming	C, RISC-V Assembly, Python, Scala, Java, MatLab, Javascript, SQL
Data Analysis	Numpy, Pandas, Seaborn, Matplotlib, Sklearn

EXPERIENCE

Student Researcher — Aug 2022 - Present
SLICE Lab @ Berkeley — *Berkeley, CA*

- Advised by Dima Nikiforov and Professor Sophia Shao.
- Research interests include: Design and Simulation Infrastructure, General-Purpose Hardware Architecture, Robotics SoC accelerator, and Hardware-Software Co-design. See research projects for details.

Student Researcher & Developer — Jan 2022 - Present
ACE Lab @ Berkeley — *Berkeley, CA*

- Advised by Professor Dan Garcia.
- Research interests include: randomization, assessment platforms infrastructure and question generators.

Academic Student Employee — Jan 2022 - Present
UC Berkeley — *Berkeley, CA*

- Computer Science Mentor, Junior Mentor, CS61C: Intro to Computer Architecture, Spring 2022
- Course Reader, EECS151: Digital Design, Fall 2022
- Course Teaching Assistance, EECS151: Digital Design, Spring 2023

CPU Design Verification Intern — May 2023 - August 2023
Apple — *Cupertino, CA*

- Detail not disclosed due to NDAs.

RESEARCH PROJECTS

RoSÉ, Hardware Software Cosimulation Pre-Silicon Full-Stack Robotics SoC Evaluation Infrastructure

- Extended the hardware simulator portion, Firesim, to use experimental on-premise FPGA deployment
- Extended the software simulator portion, Airsim, to simulate with autonomous vehicle model
- Conducted experiments across different software and hardware architecture for the optimal design points. Swept over different simulator configurations to profile the accuracy-latency tradeoff of the infrastructure.
- Paper submitted to and published in International Symposium of Computer Architecture (ISCA) 2023.

- Rearchitecting and implementing the hardware peripheral model for sensor inputs in chisel to support multi-tenant, latency and bandwidth aware, fully configurable generation of polling, streaming, interrupt, and Direct Memory Access typed sensor inputs.

FireAxe, partitioned cycle-accurate FPGA accelerated RTL simulation

- Established connection over the QSFP optical port of Alveo U250 Accerlerator Card FPGAs through the Interlaken 150G and Aurora 64B66B Vivado IP core in FireSim.
- Measured the latency-bandwidth tradeoff and characteristics on Alveo U250 with internal logic analyzer.
- Implemented the Meta-simulation extension to support multi-fpga full system visibility debug.

Unique Variant, Prairielearn controlled-randomization architectural support

- Leaded a team 4, managed project progress, organized meetings, and provided necessary training.
- Designed the updated architecture highlighting minimal invasive changes to the front-end, full backward-support capabilities, and without compromising performance.
- Implemented the back-end infrastructural changes.

BaceQG, configurable, randomized, difficulty-balancing Boolean Algebra Circuit & Expression Question Generator.

- Designed the rule-based generator architecture and devised a difficulty balancing algorithm.
- Implemented the generator program in python and integrated it to an online assessment platform, Prairielearn.
- Scripted the generation flow for fully automated, multiple-configurations generation.

COURSE PROJECTS

Verilog CPU, single core in-order RISC-V processor *EECS151*

- Designed and implemented a CPU with RISC-V instruction set architecture and a 3-stage pipeline using Verilog, 7nm ASAP standard cells, and simulated, verified, synthesized, and PARed the design.
- Coded the Arithmetic Logic Unit, Register File, Immediate Generator, Control Signal, and Memories.
- Implemented bypassing paths for data hazards and reordered the PC logic for eliminating control hazards.
- Implemented a direct-mapped, write-back cache, and an Memory controller to improve interface clarity.

LCD Driver, high frequency, low-power analog driver for LCD Display *EE140*

- Designed an analog folded telescopic differential amplifier for driving an RC-modeled LCD Display matrix with an ideal digital input.
- Reached a low power consumption of 0.542mW and a settling error of 0.105% within 180ns delay.
- The design has a full output voltage swing of 1.4V and a stable phase margin of 75 degrees. It has a PSRR of 51.5dB and a CMRR of 73dB, showing good noise rejection ratio

UCIe, high speed chiplets interconnect standard in Chipyard *EECS251B*

- Designed and Implemented the sideband channel and relevant modules.
- Designed and Implemented utilities for parsing sideband messages and factory methods for Chipyard Integration
- The Project received the 2023 Apple-sponsored class Design Award.

NumC, high-performance library for Matrix Operation *CS61C*

- Coded a library for matrix allocation, addition, multiplication, and power using naive C code.
- Accelerated the matrix multiplication operation by 64 times and power operation by 743 times compared to naive C implementation. Achieved the optimization by implementing SIMD using Intel vector Intrinsics, MIMD using OpenMP, fast exponentiation algorithm, matrix transposition, loop unrolling, and cache blocking.