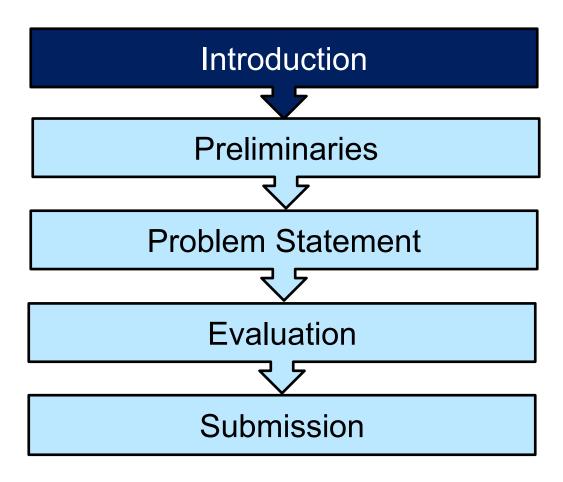


# Programming Assignment #1: Equivalence Checking

Presenter: TA Yuan-Chan Huang

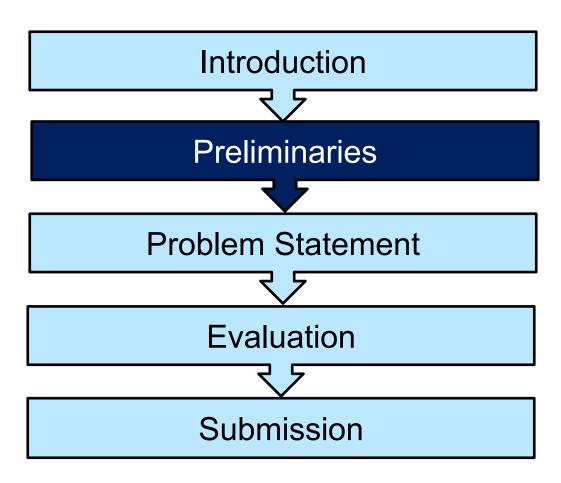
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## **Equivalence checking**

 Prove that two representations of a circuit design exhibit exactly the same behavior.



## **Conjunctive Normal Form**

- Conjunctive Normal Form (CNF)
  - Product of sums (POS)

#### **DIMACS CNF Format**

- The first line starts with p cnf, followed by the number of variables and the number of clauses.
- Each clause is a line of integers terminated by a 0.
  - Positive integers: variables in positive phases
  - Negative integers: variables in negative phases (negations)
- Example

p cnf 12 27  
1 -5 0 
$$\longrightarrow$$
  $(x_1 \lor \neg x_5)$   
7 -5 0  
5 -1 -7 0

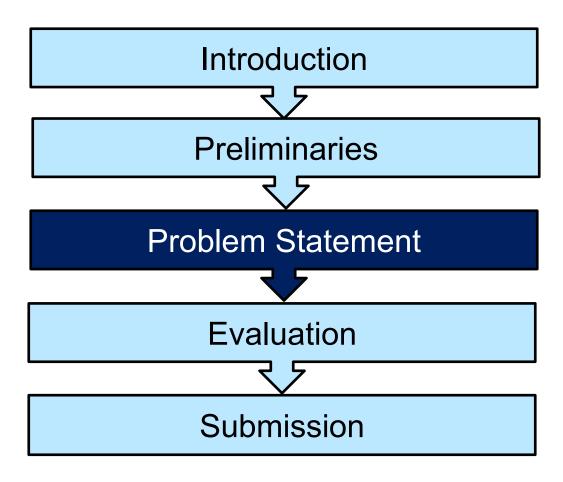
#### **MiniSat**

- A small, yet efficient, SAT solver
- Usage

```
./MiniSat_v1.14_linux [*.dimacs] [*.output]
```

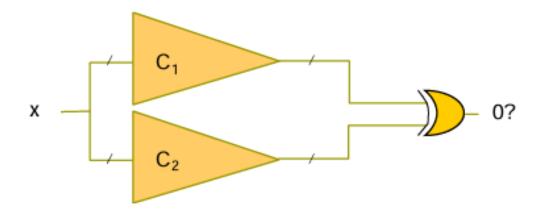
Example

```
IRISLAB-79:~/IntroToEDA/PA1> ./MiniSat v1.14 linux example.dimacs example.output
                                  =[MINISAT]===
 Conflicts |
                 ORIGINAL
                                              LEARNT
                                                                   Progress
              Clauses Literals
                                   Limit Clauses Literals Lit/Cl
                            66
          0 |
                   24
                                               0
                                                        0
                                                              nan
                                                                     0.000 %
restarts
                      : 1
conflicts
                      : 0
                                       (0 /sec)
decisions
                      : 3
                                       (3058 /sec)
propagations
                                       (12232 /sec)
                      : 12
conflict literals
                      : 0
                                       ( nan % deleted)
Memory used
                      : 1.69 MB
CPU time
                      : 0.000981 s
SATISFIABLE
```



#### **Miter Structure**

- A miter structure is introduced to compare circuit outputs.
- Two circuits are equivalent if and only if the miter's output is always constant 0.



#### **Tseitin transformation**

- Combinational gate can be translated into CNF clauses.
- Example: NOT gate  $(C \to \overline{A}) \land (\overline{C} \to A), (\overline{C} \lor \overline{A}) \land (C \lor A)$

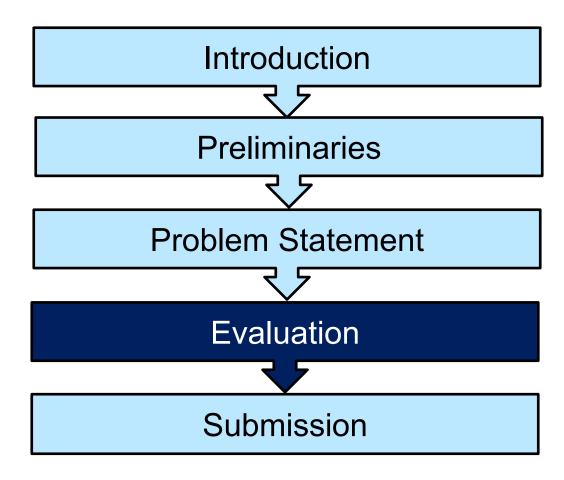
Туре	Operation	CNF sub-expression
AND AND	$C = A \cdot B$	$(\overline{A} ee \overline{B} ee C) \wedge (A ee \overline{C}) \wedge (B ee \overline{C})$
NAND	$C = \overline{A \cdot B}$	$(\overline{A} ee \overline{B} ee \overline{C}) \wedge (A ee C) \wedge (B ee C)$
	C = A + B	$(A \lor B \lor \overline{C}) \land (\overline{A} \lor C) \land (\overline{B} \lor C)$
NOR NOR	$C = \overline{A + B}$	$(A \lor B \lor C) \land (\overline{A} \lor \overline{C}) \land (\overline{B} \lor \overline{C})$
NOT	$C = \overline{A}$	$(\overline{A} ee \overline{C}) \wedge (A ee C)$
XOR	$C = A \oplus B$	$(\overline{A} \vee \overline{B} \vee \overline{C}) \wedge (A \vee B \vee \overline{C}) \wedge (A \vee \overline{B} \vee C) \wedge (\overline{A} \vee B \vee C)$

#### **TODO**

- Write a program that generates the CNF for verifying the equivalence of two combinational circuits.
- The program should be invoked as:

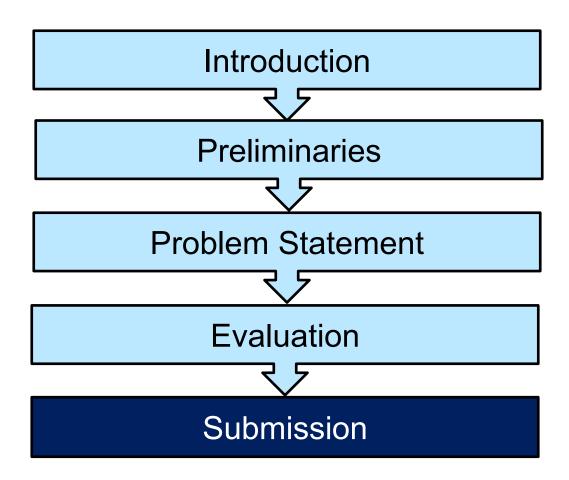
```
./ec [*_A.bench] [*_B.bench] [*.dimacs]
```

- Hint:
  - Construct a miter circuit → Tseitin transformation



#### **Evaluation**

- We will use MiniSat to check the CNF files generated by your program.
- Your program must handle circuits with thousands of gates.
- If your program takes more than 1 minute to generate CNF, the case will be considered failed, even if the result is correct.



#### **Submission**

- Compress your project directory into a zip file named : StudentID\_pa1.zip
- The unzipped directory must follow the structure below:

```
<StudentID_pa1>/
|-- bin/
|-- src/
|-- Makefile
|-- REDAME.md
```

#### **Submission**

- No Plagiarism.
- Penalty for late submission: 20% per day.
- Deadline: October 8, 2025, 23:59.

## If you have any question, ...

- Yuan-Chan Huang
  - E-mail: <u>r14943071@ntu.edu.tw</u>
  - Office Hours: Wed. 12:30~13:20 @ BL-407



## Thank You!