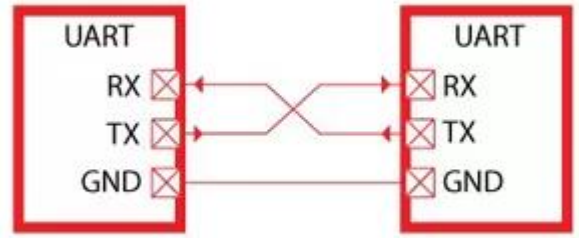
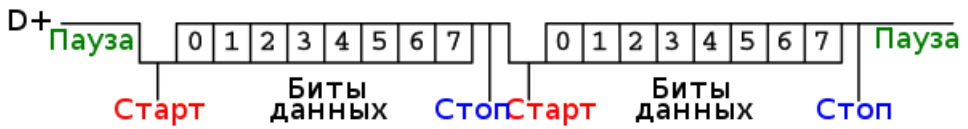
Интерфейсы

UART

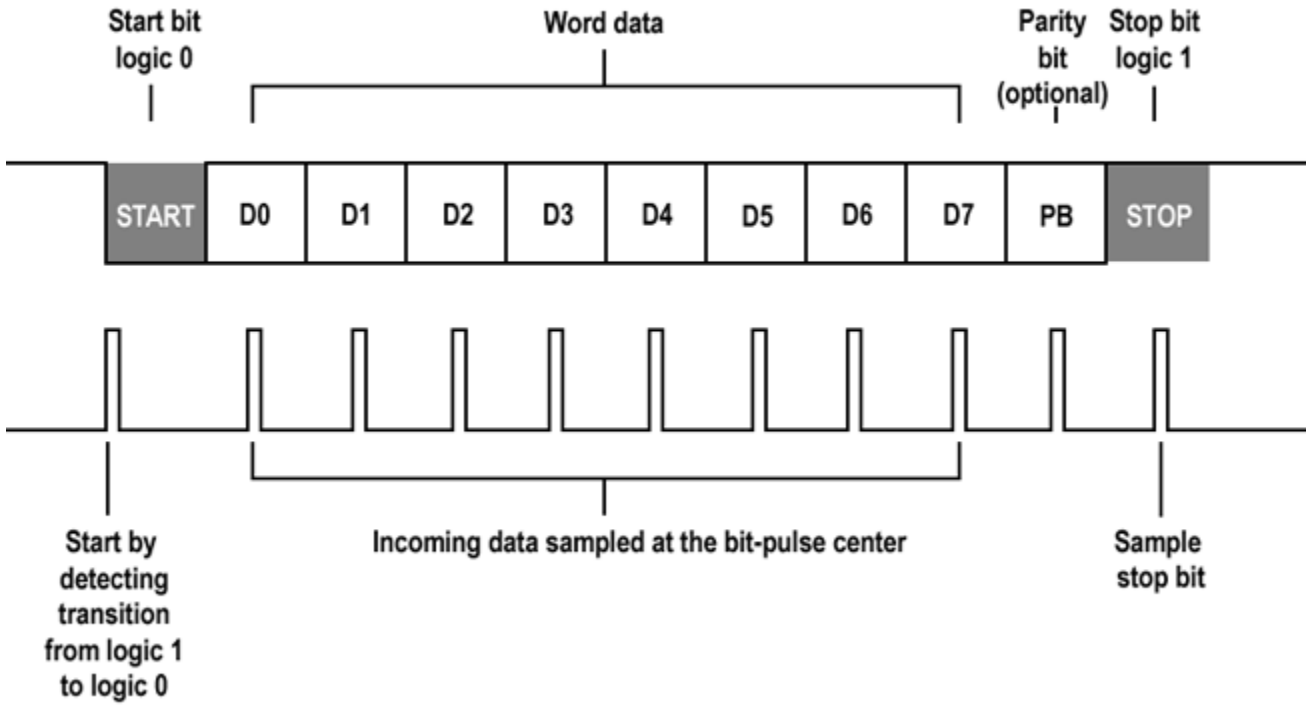
- Часто применяется в embedded системах
- UART – universal asynchronous reciver-transmitter
- Соединение типа точка-точка
- Дуплексная передача
- Нет спецификации





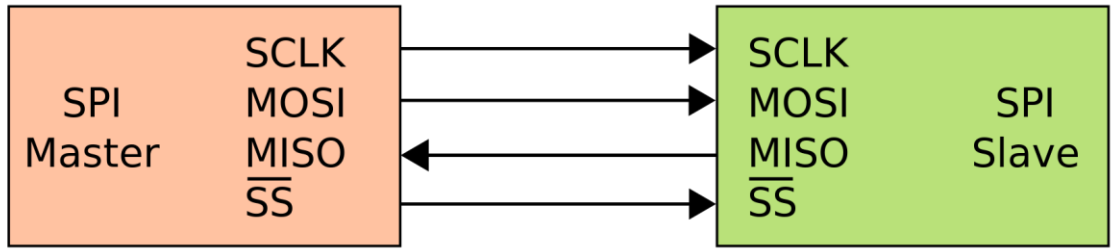
UART

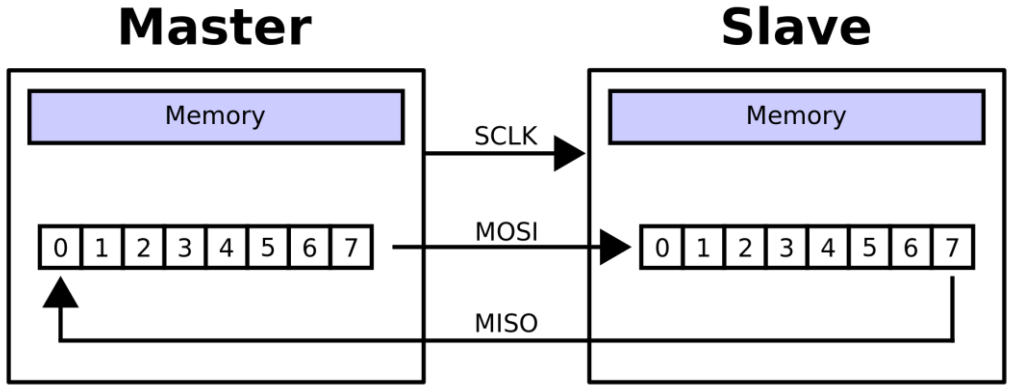
- S = 300; 600; 1200; 2400; 4800; **9600**; 19200; 38400; 57600; 115200; 230400; 460800; 921600
- T = 1/S c



SPI

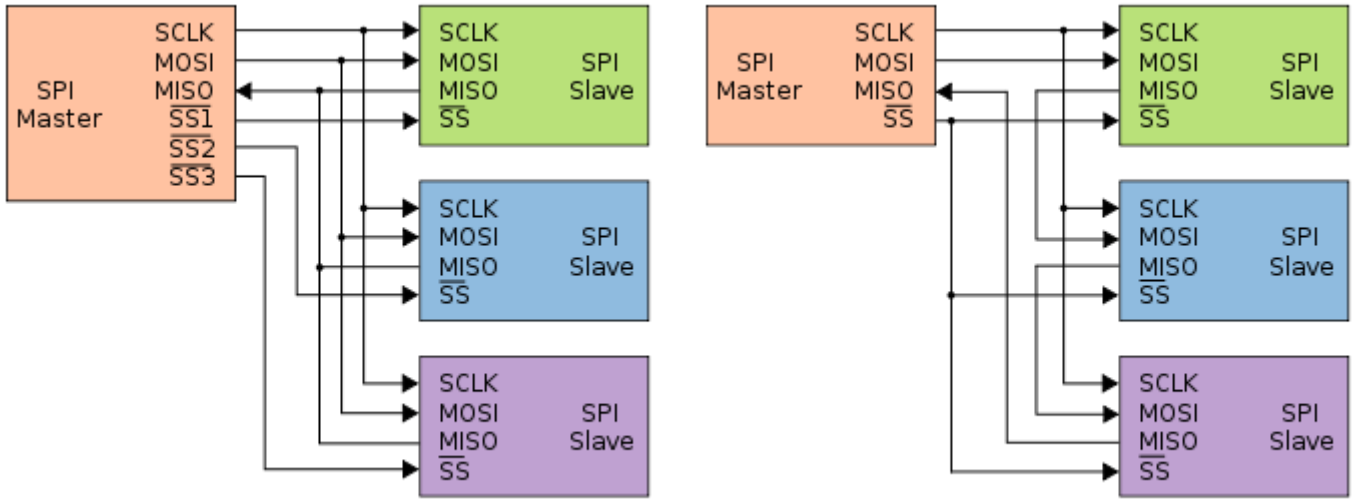
- SPI – serial peripheral interface
- Дуплексная передача
- MOSI —*Master Out Slave In*
- MISO —*Master In Slave Out*
- SCLK — синхросигнал.
- SS —*Slave Select*.
- Отсутствие официального стандарта

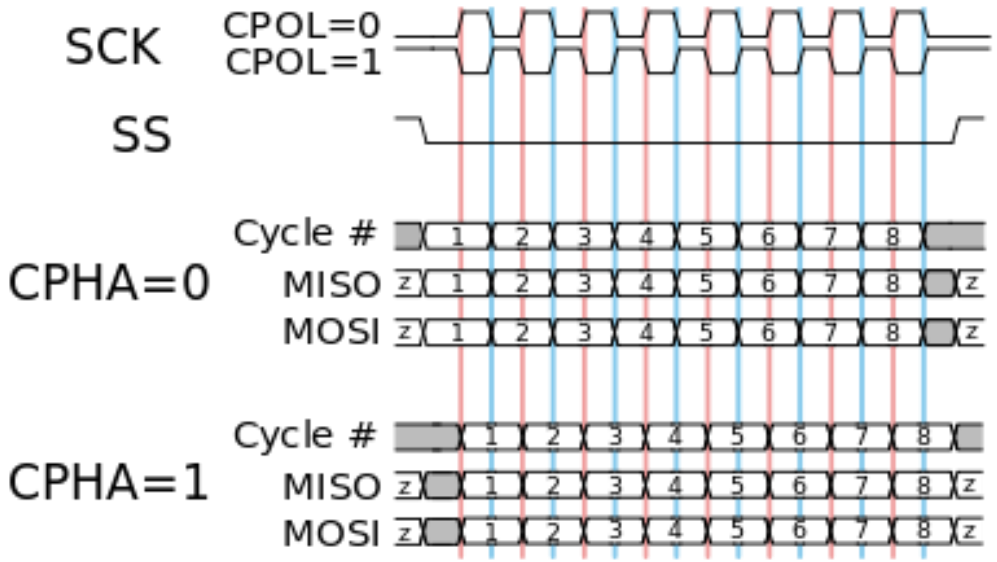




SPI

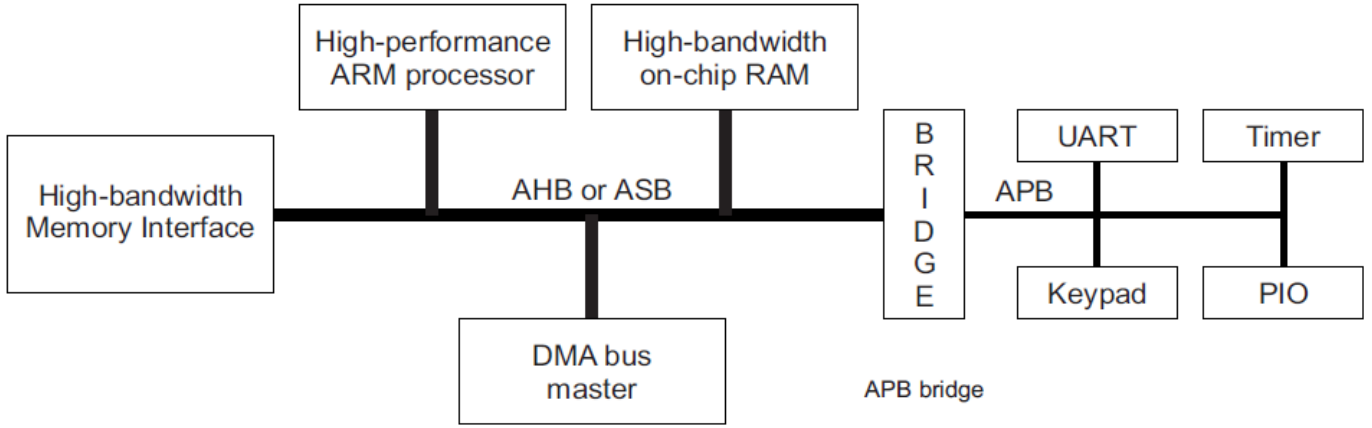
- CPOL = 0 — сигнал синхронизации начинается с низкого уровня;
- CPOL = 1 — сигнал синхронизации начинается с высокого уровня;
- CPHA = 0 — выборка данных производится по переднему фронту сигнала синхронизации;
- CPHA = 1 — выборка данных производится по заднему фронту сигнала синхронизации.

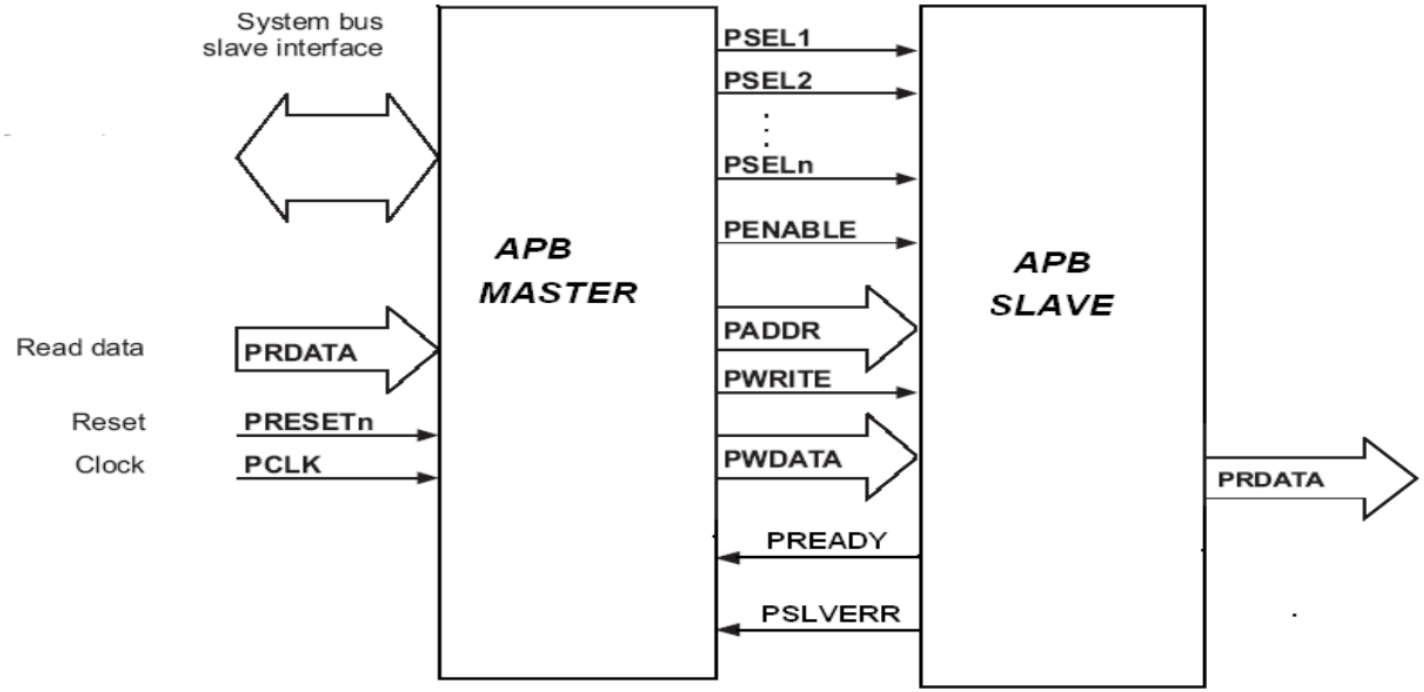




AMBA APB

- AMBA - Advanced Microcontroller Bus Architecture
- APB - Advanced Peripheral Bus
- ARM, специфицирован
- Для работы с простой внутренней периферией

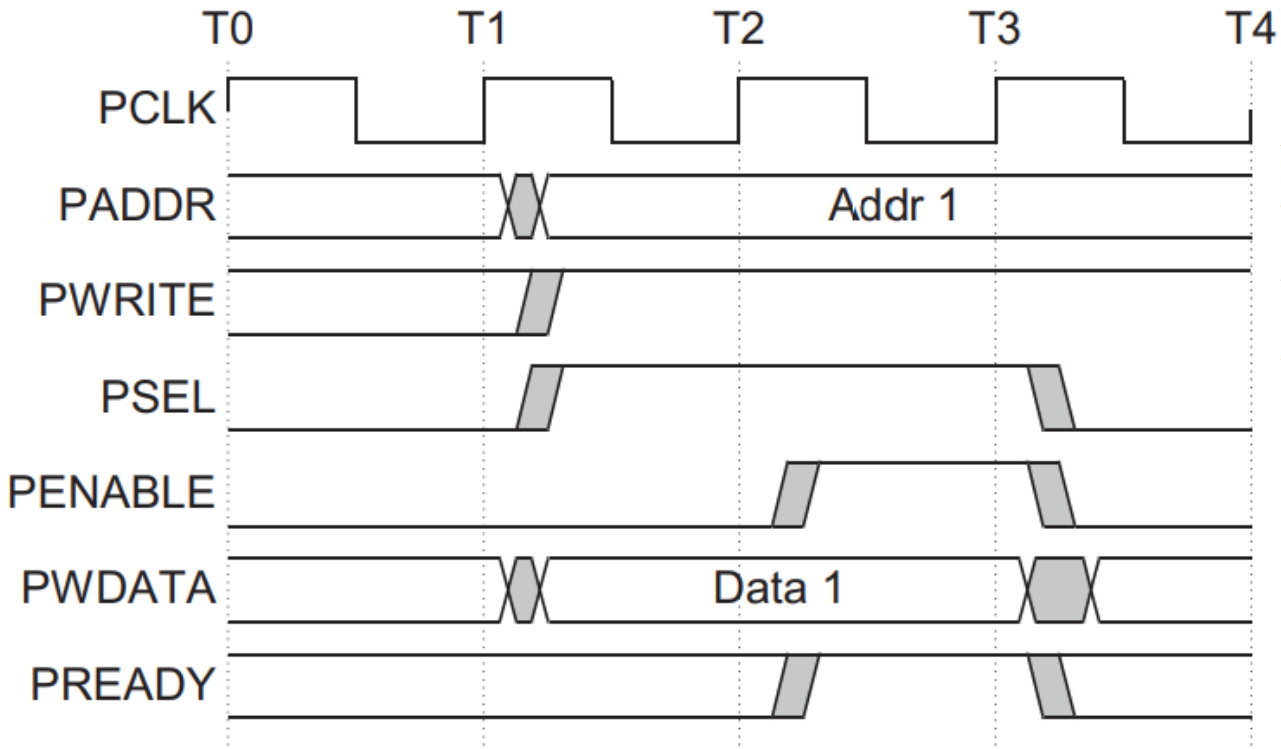




AMBA APB

Signal	Source	Description
PCLK	Clock source	Clock. The rising edge of **PCLK** times all transfers on the APB.
PRESETn	System bus equivalent	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PADDR	APB bridge	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PPROT	APB bridge	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
PSELx	APB bridge	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a **PSELx** signal for each slave.
PENABLE	APB bridge	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	APB bridge	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PWDATA	APB bridge	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when **PWRITE** is HIGH. This bus can be up to 32 bits wide.
PSTRB	APB bridge	Write strobes. This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each eight bits of the write data bus. Therefore, **PSTRB[n]** corresponds to **PWDATA[(8n + 7):(8n)]**. Write strobes must not be active during a read transfer.
PREADY	Slave interface	Ready. The slave uses this signal to extend an APB transfer.
PRDATA	Slave interface	Read Data. The selected slave drives this bus during read cycles when **PWRITE** is LOW. This bus can be up to 32-bits wide.
PSLVERR	Slave interface	This signal indicates a transfer failure. APB peripherals are not required to support the **PSLVERR** pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

AMBA APB write with no waits



At T1, a write transfer starts with address **PADDR**, write data **PWDATA**, write signal **PWRITE**, and select signal **PSEL,** being registered at the rising edge of **PCLK**. This is called the Setup phase of the write transfer.

At T2, enable signal **PENABLE**, and ready signal **PREADY**, are registered at the rising edge of **PCLK**.

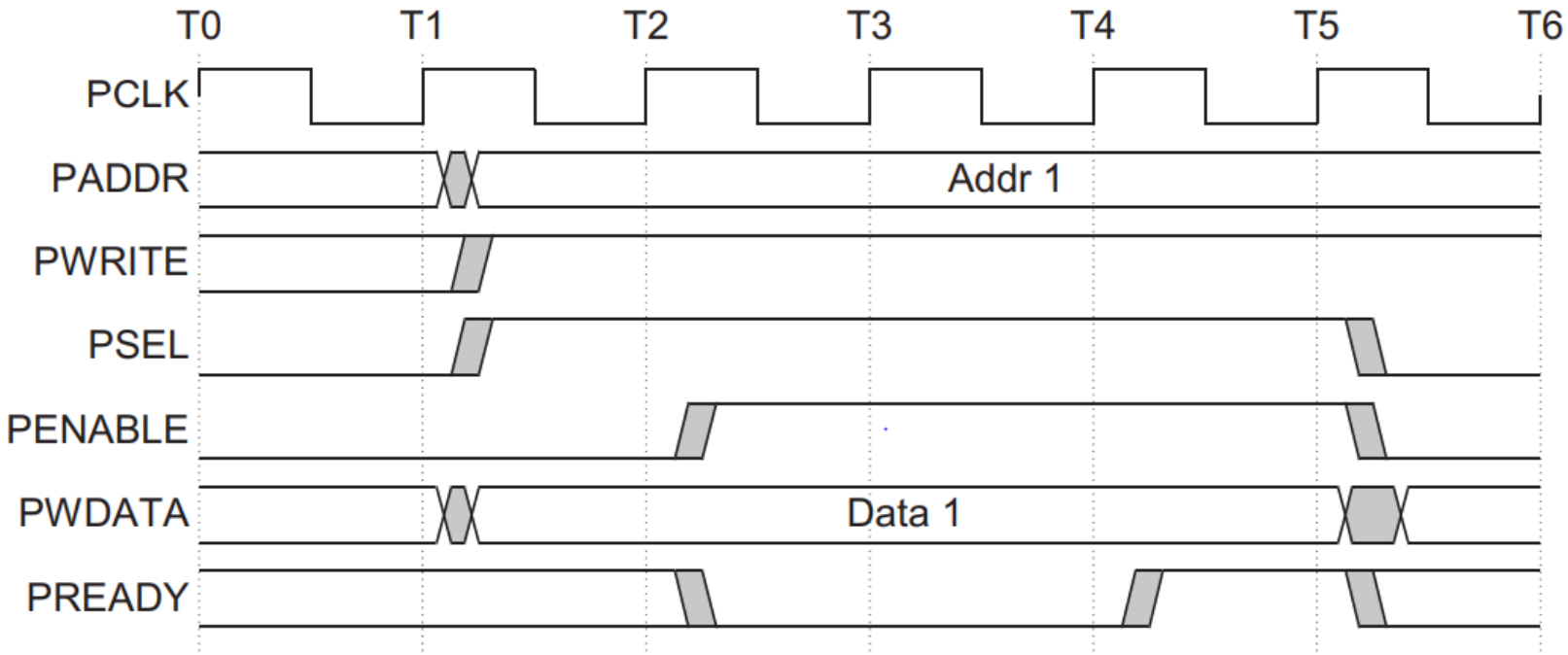
When asserted, **PENABLE** indicates the start of the Access phase of the transfer.

When asserted, **PREADY** indicates that the slave can complete the transfer at the next rising edge of **PCLK**.

The address **PADDR**, write data **PWDATA**, and control signals all remain valid until the transfer completes at T3, the end of the Access phase.

The enable signal **PENABLE**, is deasserted at the end of the transfer. The select signal **PSEL**, is also deasserted unless the transfer is to be followed immediately by another transfer to the same peripheral.

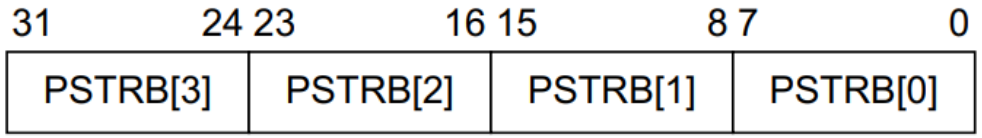
AMBA APB write with waits



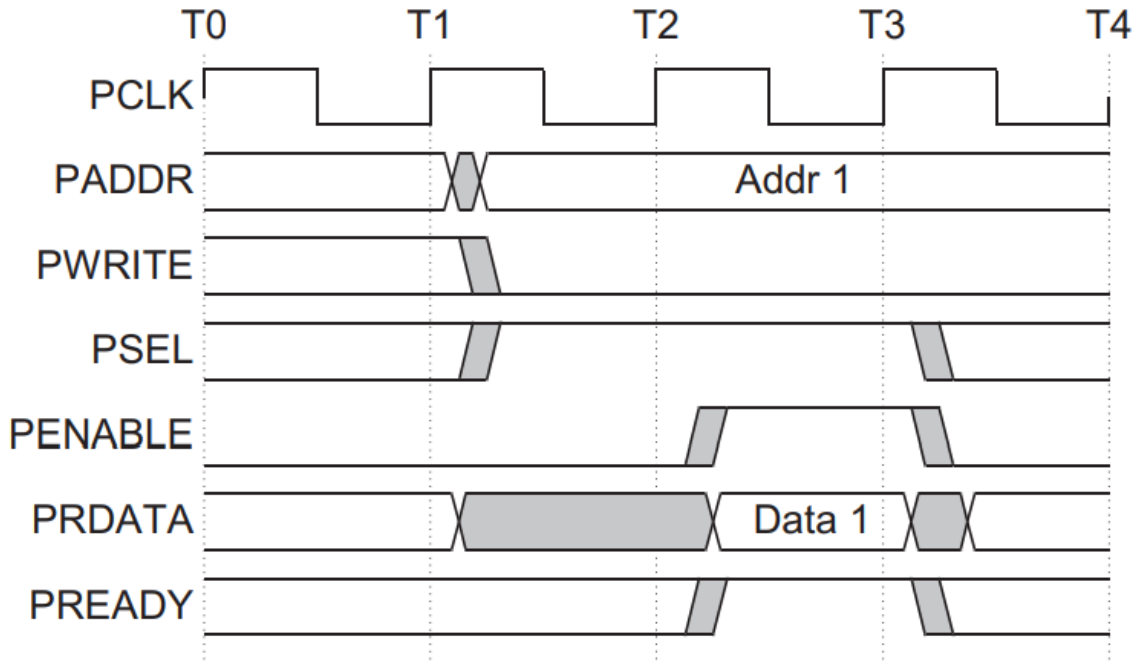
AMBA APB strobes

The write strobe signals, **PSTRB**, enable sparse data transfer on the write data bus. Each write strobe signal corresponds to one byte of the write data bus. When asserted HIGH, a write strobe indicates that the corresponding byte lane of the write data bus contains valid information.

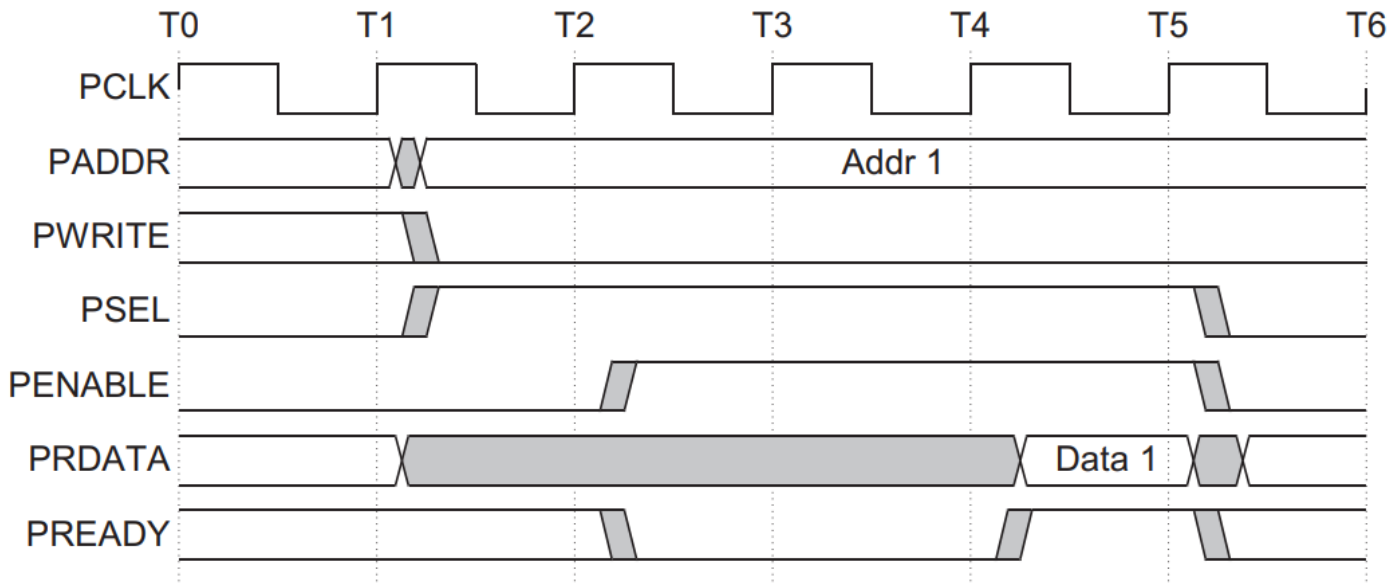
There is one write strobe for each eight bits of the write data bus, so **PSTRB[n]** corresponds to **PWDATA[(8n + 7):(8n)]**. Figure 3-3 shows this relationship on a 32-bit data bus.



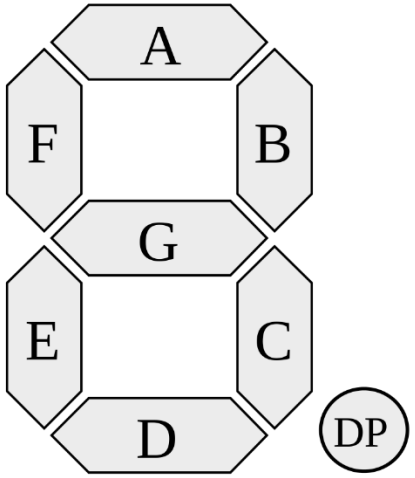
AMBA APB read with no waits

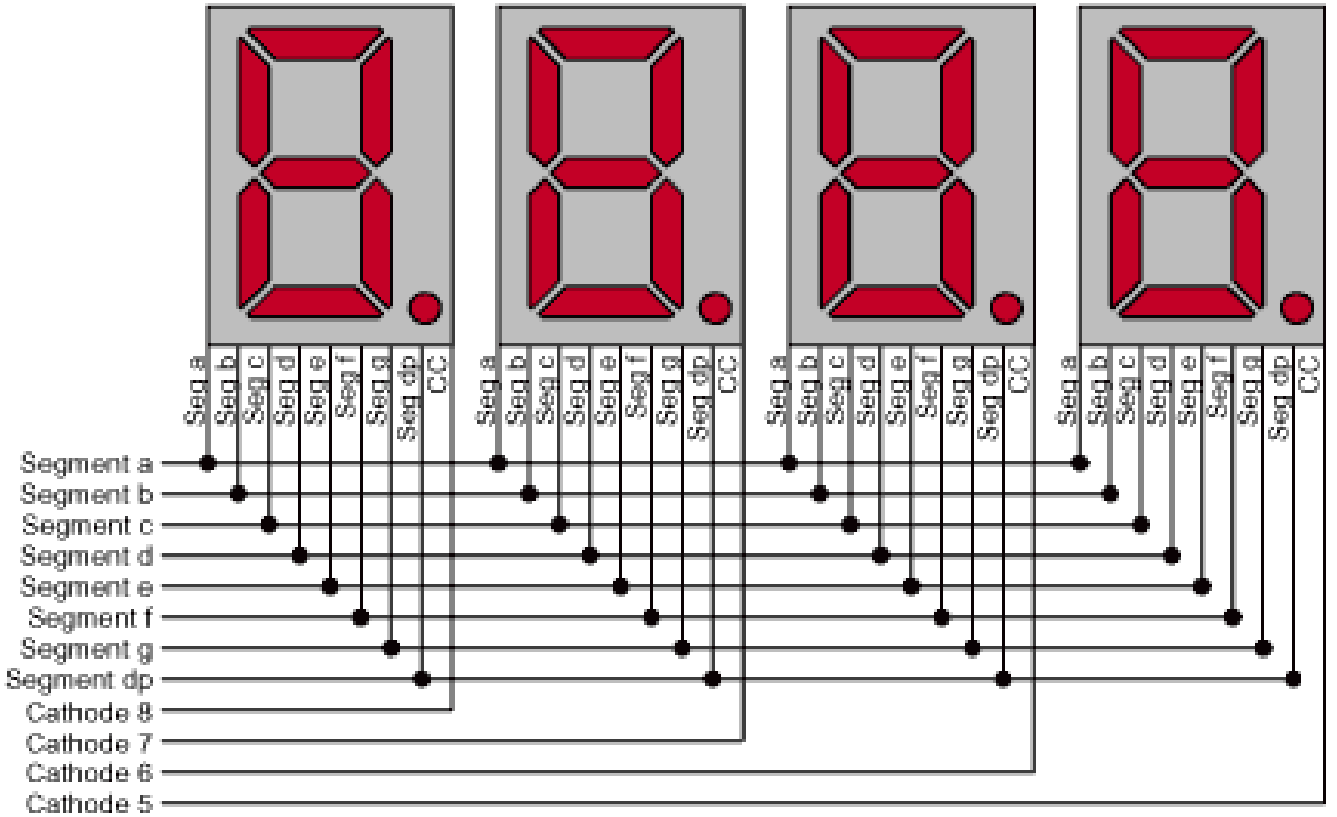


AMBA APB read with waits



7SEG

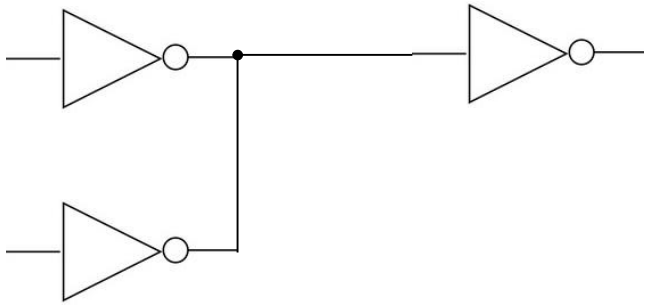

A
F
B
G
E
C
D
DP


Seg a
Seg b
Seg c
Seg d
Seg e
Seg f
Seg g
Seg dp
CC
Segment a
Segment b
Segment c
Segment d
Segment e
Segment f
Segment g
Segment dp
Cathode 8
Cathode 7
Cathode 6
Cathode 5

Verilog

Основные пункты

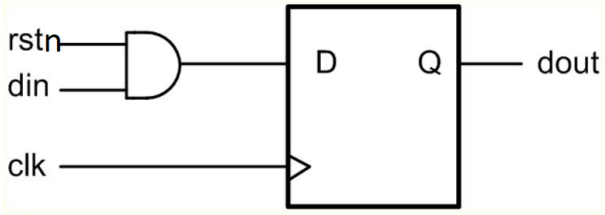
- HDL – hardware description language
- Блокирующее и неблокирующее присваивание
- Синтезируемость
  - Цикл for
  - У каждого сигнала только один драйвер



Сбросы

- Синхронный:

```
always @(posedge clk)
begin
   if( !rstn)
      <reset>
   else
      …
end
```



- Асинхронный:

```
always @(posedge clk or negedge rstn)
begin
   if( !rstn)
      <reset>
   else
      …
end
```

Верификация

- Тестовое окружение есть модуль без выводов, в котором подключен тестируемый блок
- Последовательность тестов в initial блоке
- timescale
- $display
- $finish
- Синхросигнал:

```
always #(T_half_period) clk <= !clk;
```