GATE CSE 2024 SET 1: Question Number 30

- **Master Paper: Question 30**

Q.30 Consider a 5-stage pipelined processor with Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Register Writeback (WB) stages. Which of the following statements about *forwarding* is/are CORRECT?

(A) In a pipelined execution, forwarding means the result from a source stage of an earlier instruction is passed on to the destination stage of a later instruction

(B) In forwarding, data from the output of the MEM stage can be passed on to the input of the EX stage of the next instruction

(C) Forwarding cannot prevent all pipeline stalls

(D) Forwarding does not require any extra hardware to retrieve the data from the pipeline stages

Answer Given By Gate: A, C

My Humble Challenge: Answer should be A,B,C

1)Digital Design and Computer Architecture By David Harris and Sarah Harris

Second Edition, Page No -419

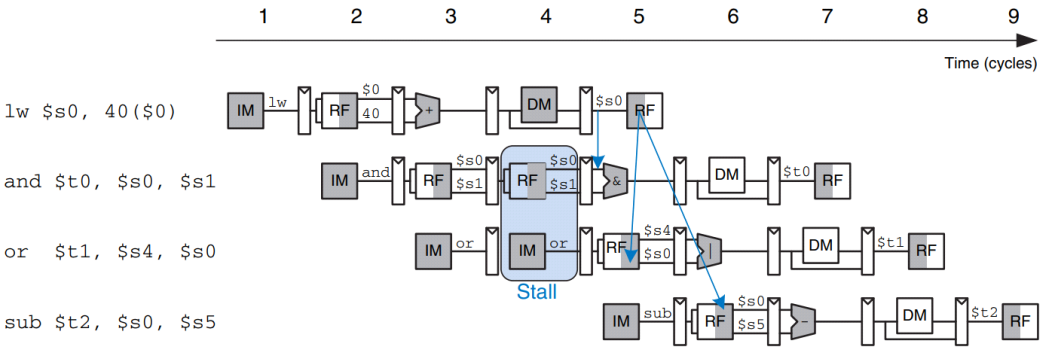

Figure 7.52 **Abstract pipeline diagram illustrating stall to solve hazards**

As is clearly conspicuous from the above diagram the author shows that operand forwarding from the DM(memory access) stage of LD(current) instruction, to the EX stage of ADD (next) instruction is possible.

Also, an important point to notice is that, as there is “can” in option B of master paper question no. 30, so, in my opinion, all the possibilities, i.e., with stalls, and without stalls, should be taken into consideration while answering the question.

Final Remark

Thus, in support of the above mentioned resource, and the argument presented therein ,I would like to claim that option B should also be considered to be correct, since we can do operand forwarding from MEM stage of an instruction to the EX stage of the next instruction, if we are willing to use an intermediary stall cycle. Therefore, I kindly request the gate officials to kindly change the answer to this question to option A, B, and C.