Aluna: Iasmim Maria Freire da Silva Torres. **Matrícula:** 121110942

Roteiro 08

1.
Programa 1:

```
addi s2, zero, 4
addi s3, zero, 3
addi s4, zero, 7
addi s5, zero, 5
addi s6, zero, 6
add s7, s2, s3
```

a) Conteúdo da Memória de Instruções (“Instruction Memory”) e dos Registradores(“Registers”), no início e no final da execução do programa.

Instruction Memory | Data Memory | Registers

Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4

00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3

00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19
000000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10)
I-type Instruction:

addi s6, x0, 6

00000000011000000000101100010011

6	0	0	22	19
000000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 20 (0x14)
R-type Instruction:

add s7, s2, s3

00000001001110010000101110110011

0	19	18	0	23	51
0000000	10011	10010	000	10111	0110011
FUNCT7	RS2	RS1	FUNCT3	RD	OP

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000

8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

1° Step

Instruction Memory | Data Memory | Registers

INSTRUCTION IN IF STAGE

Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4

00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3

00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19
000000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10)
I-type Instruction:

addi s6, x0, 6

00000000011000000000101100010011

6	0	0	22	19
000000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 20 (0x14)
R-type Instruction:

add s7, s2, s3

00000001001110010000101110110011

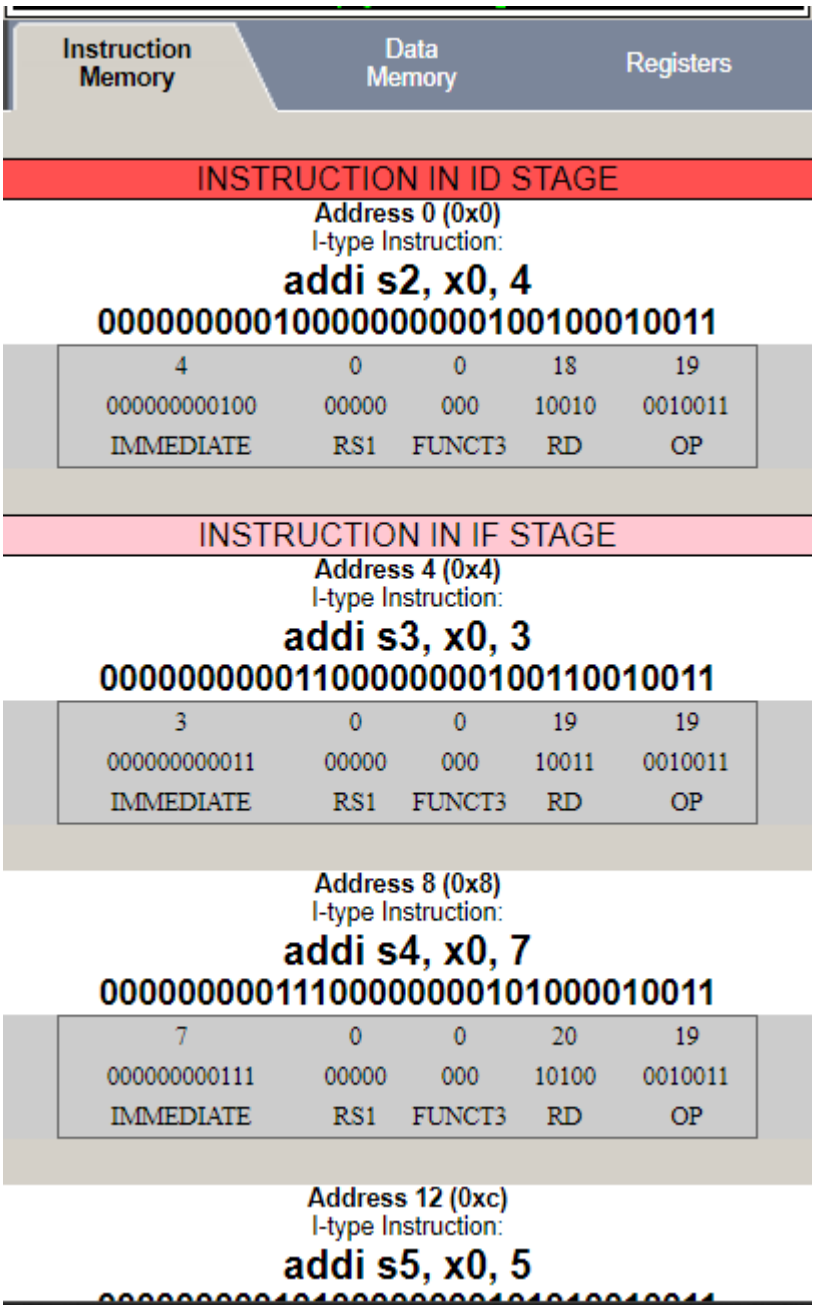
0	19	18	0	23	51
0000000	10011	10010	000	10111	0110011
FUNCT7	RS2	RS1	FUNCT3	RD	OP

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000

7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

2° Step

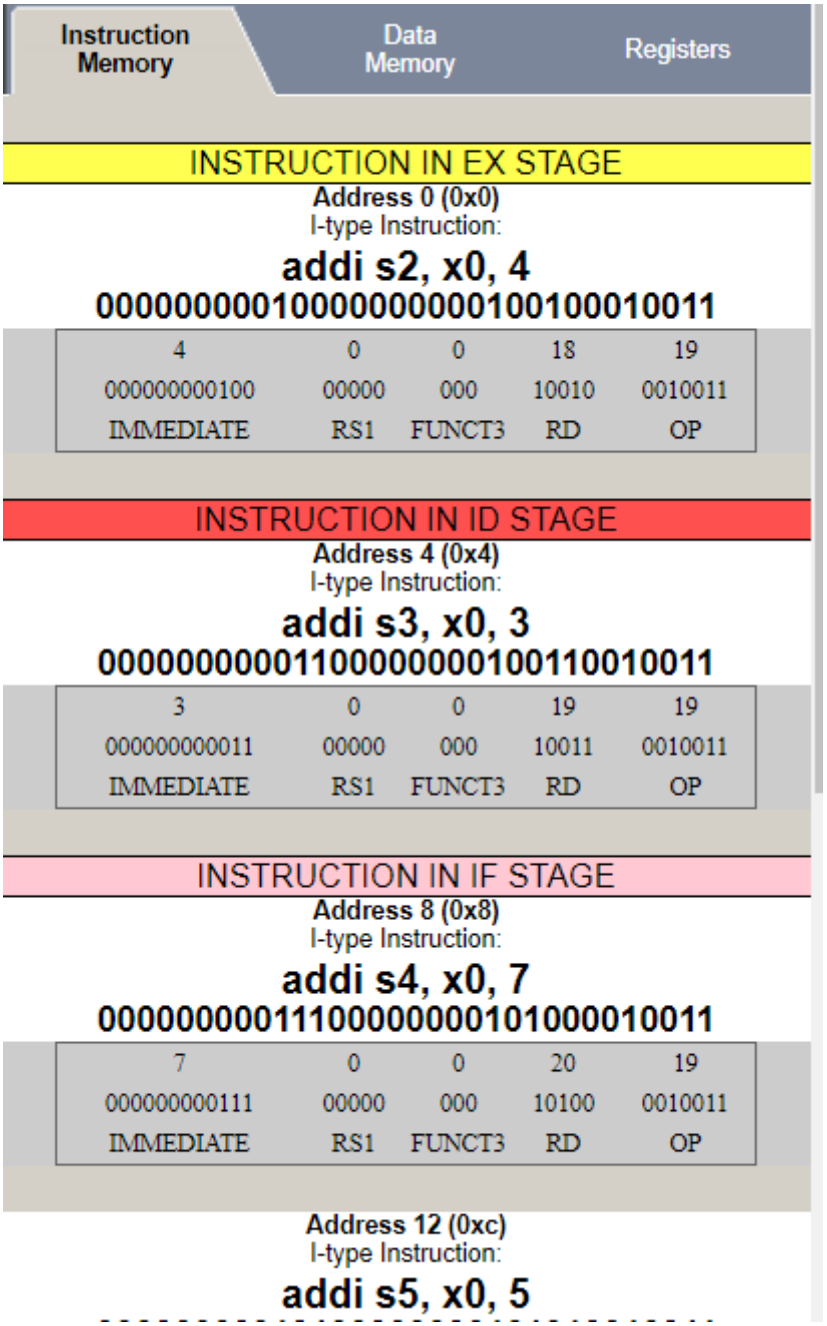

Instruction Memory
Data Memory
Registers
INSTRUCTION IN ID STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN IF STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000

6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

3° Step

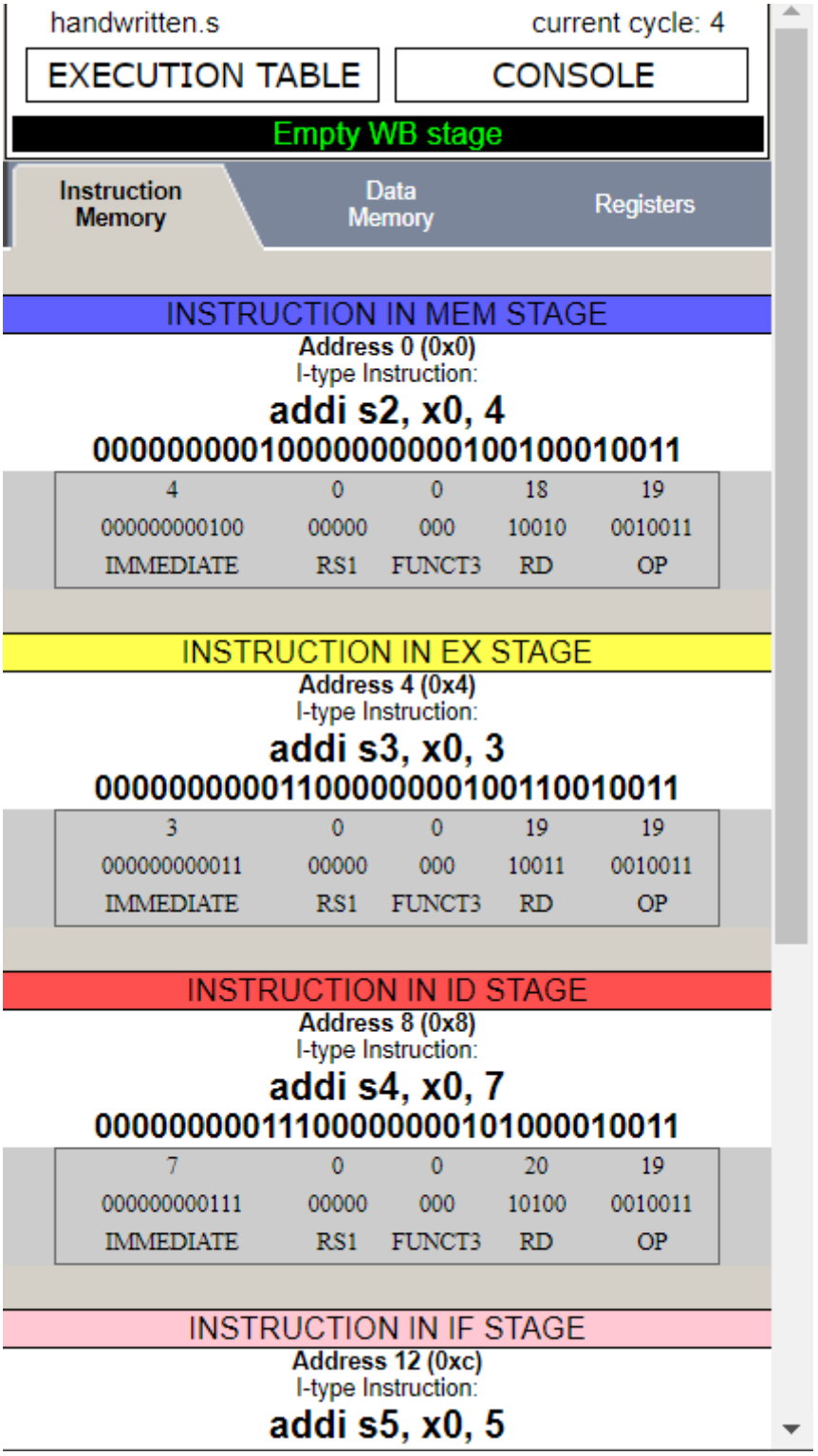

Instruction Memory
Data Memory
Registers
INSTRUCTION IN EX STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN ID STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN IF STAGE
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5

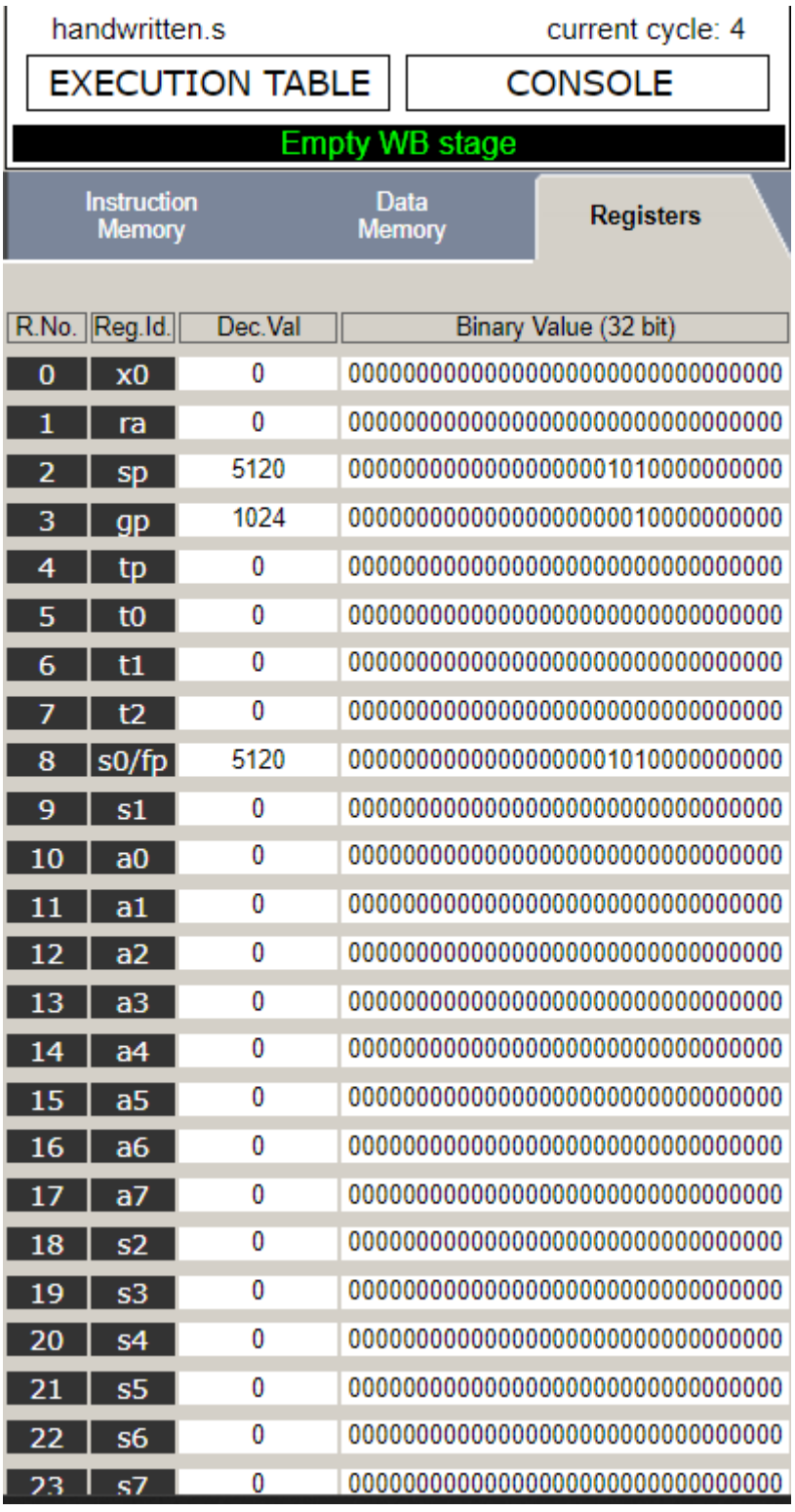
Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000

5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

4° Step

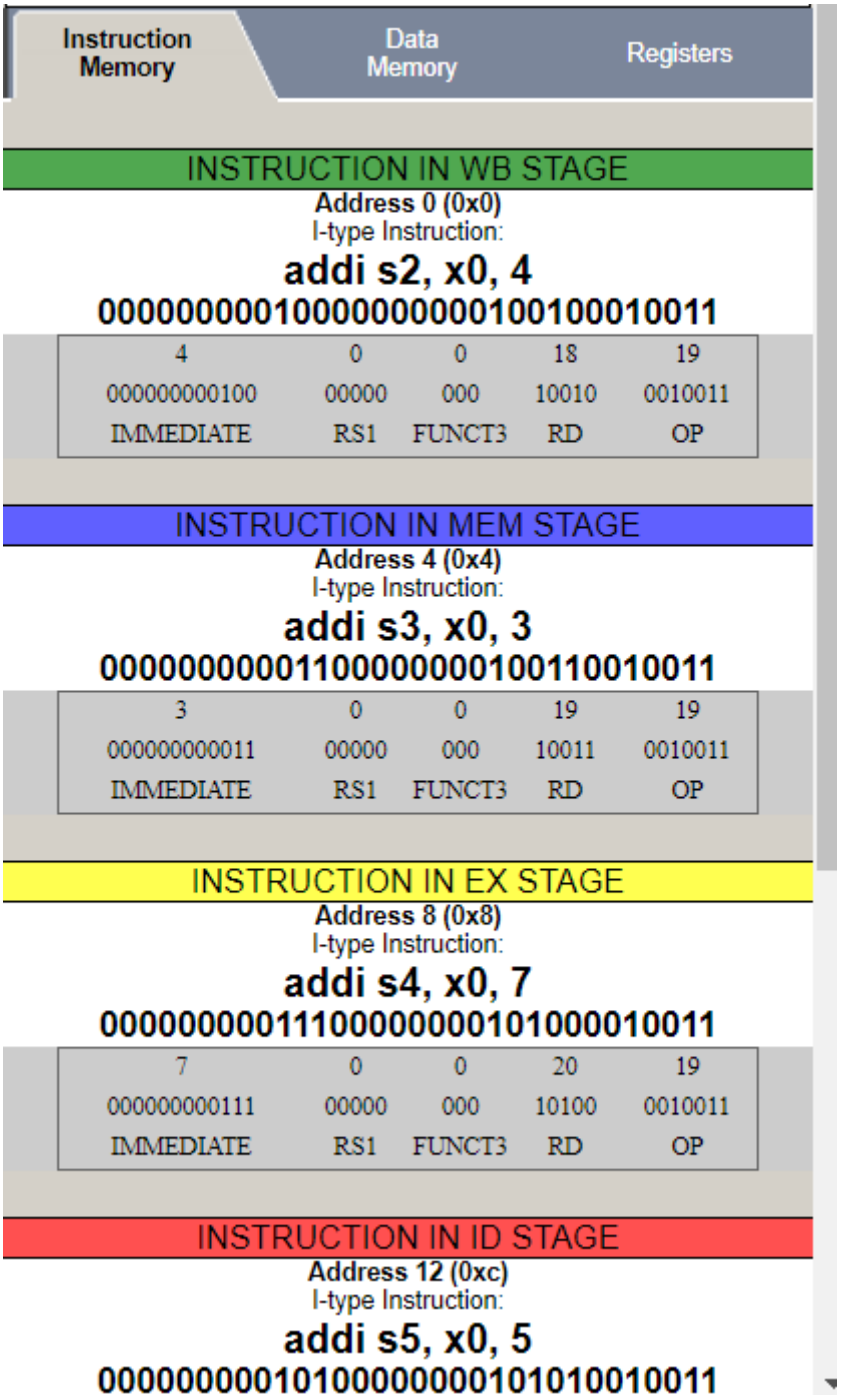

handwritten.s
current cycle: 4
EXECUTION TABLE
CONSOLE
Empty WB stage
Instruction Memory
Data Memory
Registers
INSTRUCTION IN MEM STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN EX STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN ID STAGE
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN IF STAGE
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5

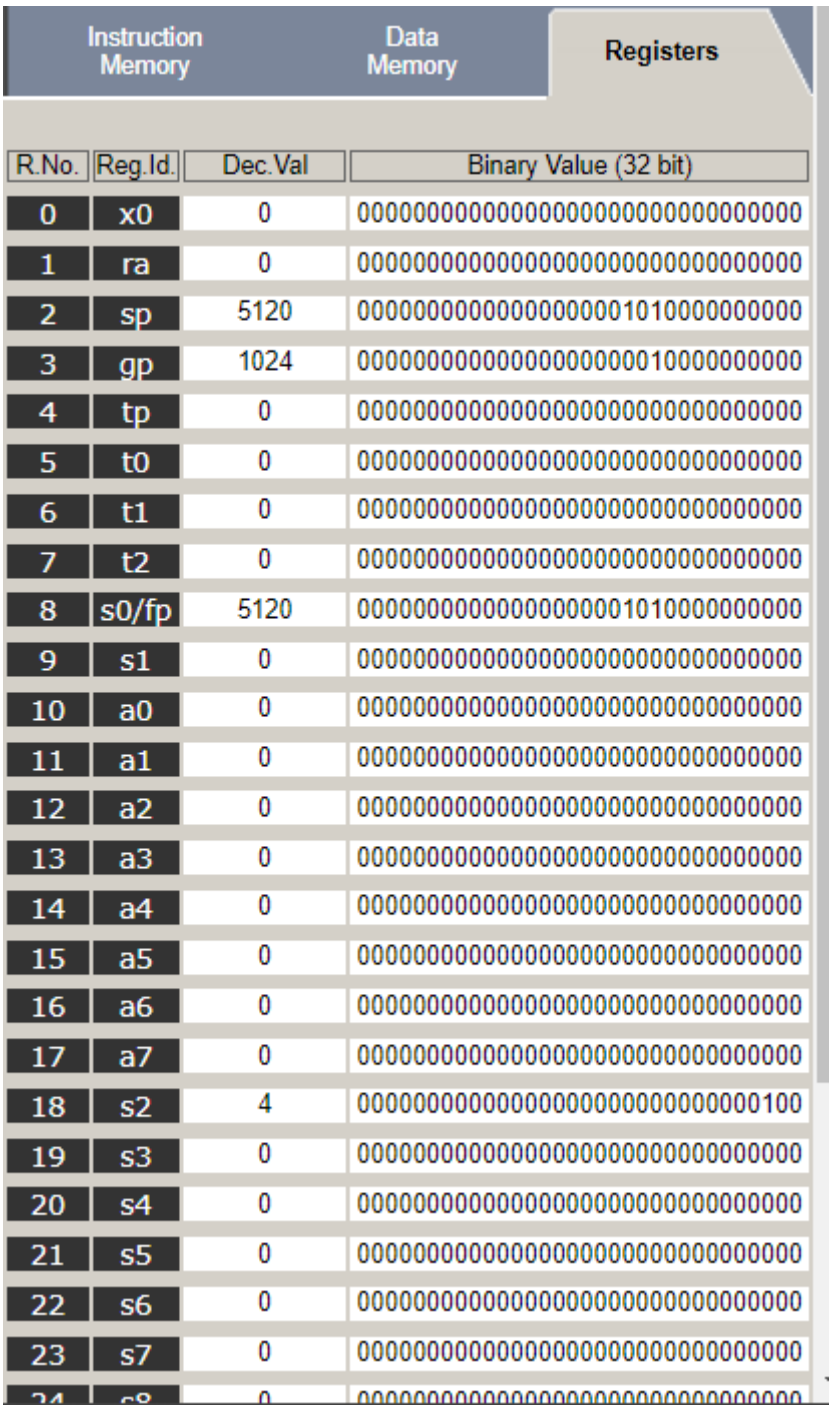


R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000

4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

5° Step


Instruction Memory
Data Memory
Registers
INSTRUCTION IN WB STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN MEM STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN EX STAGE
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN ID STAGE
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011

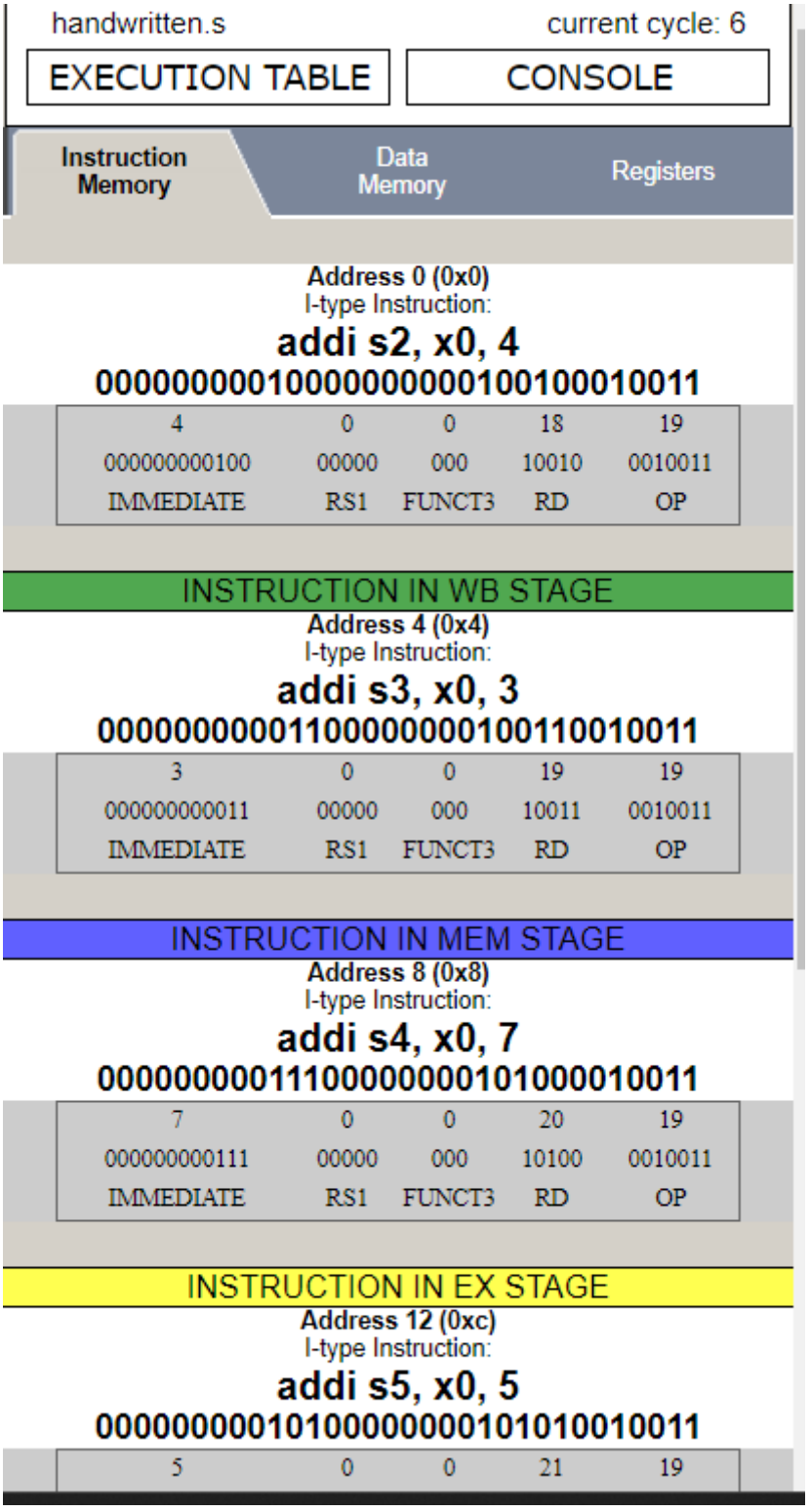


Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000

4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

6° Step


handwritten.s
current cycle: 6
EXECUTION TABLE
CONSOLE
Instruction Memory
Data Memory
Registers
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN WB STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN MEM STAGE
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN EX STAGE
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011
5 0 0 21 19

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000

handwritten.s current cycle: 6

EXECUTION TABLE | CONSOLE

4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

7° Step

EXECUTION STATUS

handwritten.s current cycle: 7

EXECUTION TABLE | CONSOLE

Empty IF stage

Instruction Memory | Data Memory | Registers

Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4

00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3

00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN WB STAGE

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN MEM STAGE

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19

Empty IF stage

INSTRUCTION IN WB STAGE

Address 8 (0x8)

I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN MEM STAGE

Address 12 (0xc)

I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19
000000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN EX STAGE

Address 16 (0x10)

I-type Instruction:

addi s6, x0, 6

00000000011000000000101100010011

6	0	0	22	19
000000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN ID STAGE

Address 20 (0x14)

R-type Instruction:

add s7, s2, s3

00000001001110010000101110110011

0	19	18	0	23	51
0000000	10011	10010	000	10111	0110011
FUNCT7	RS2	RS1	FUNCT3	RD	OP

handwritten.s current cycle: 7

EXECUTION TABLE | CONSOLE

Empty IF stage

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000

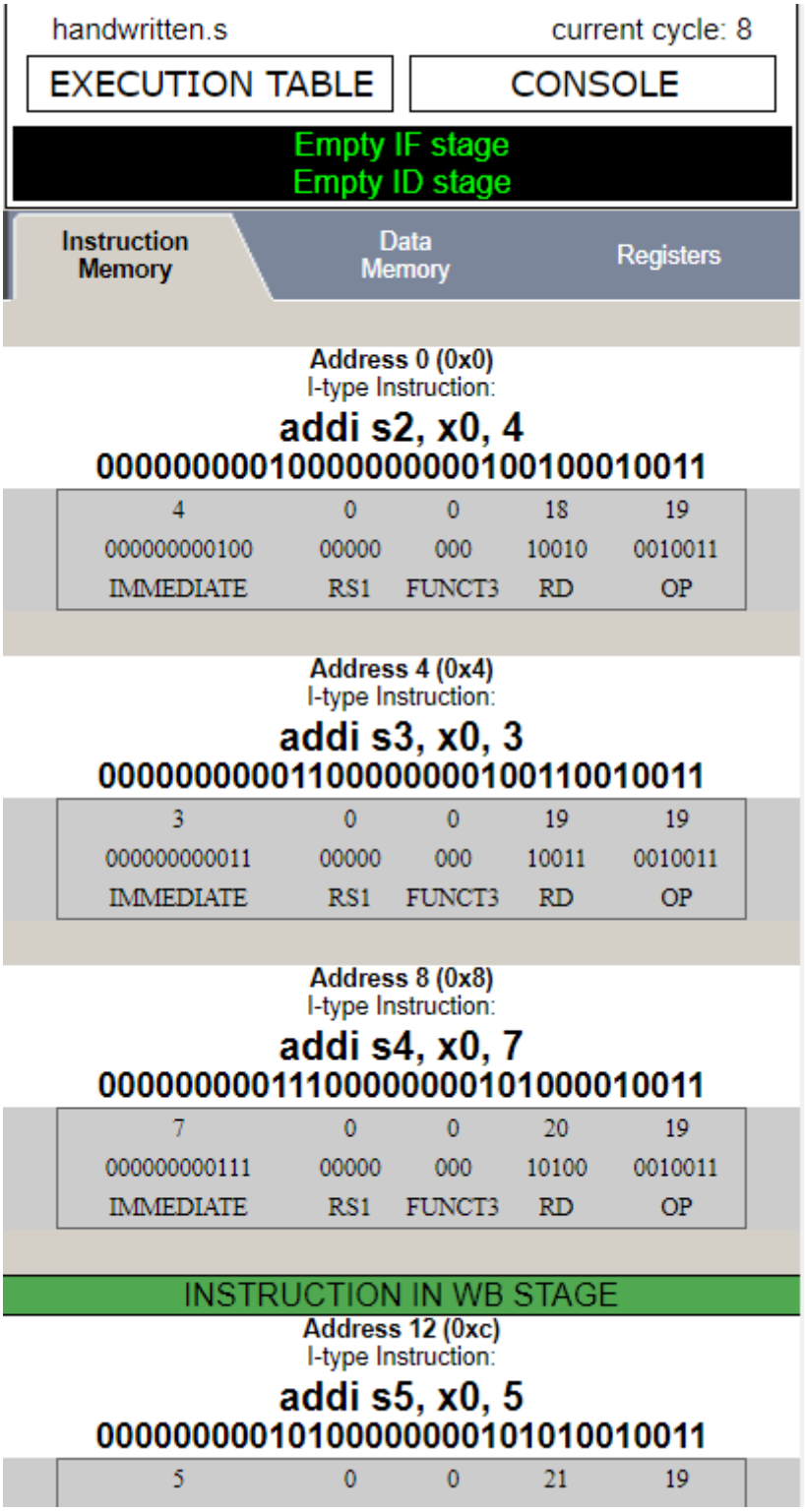
handwritten.s current cycle: 7

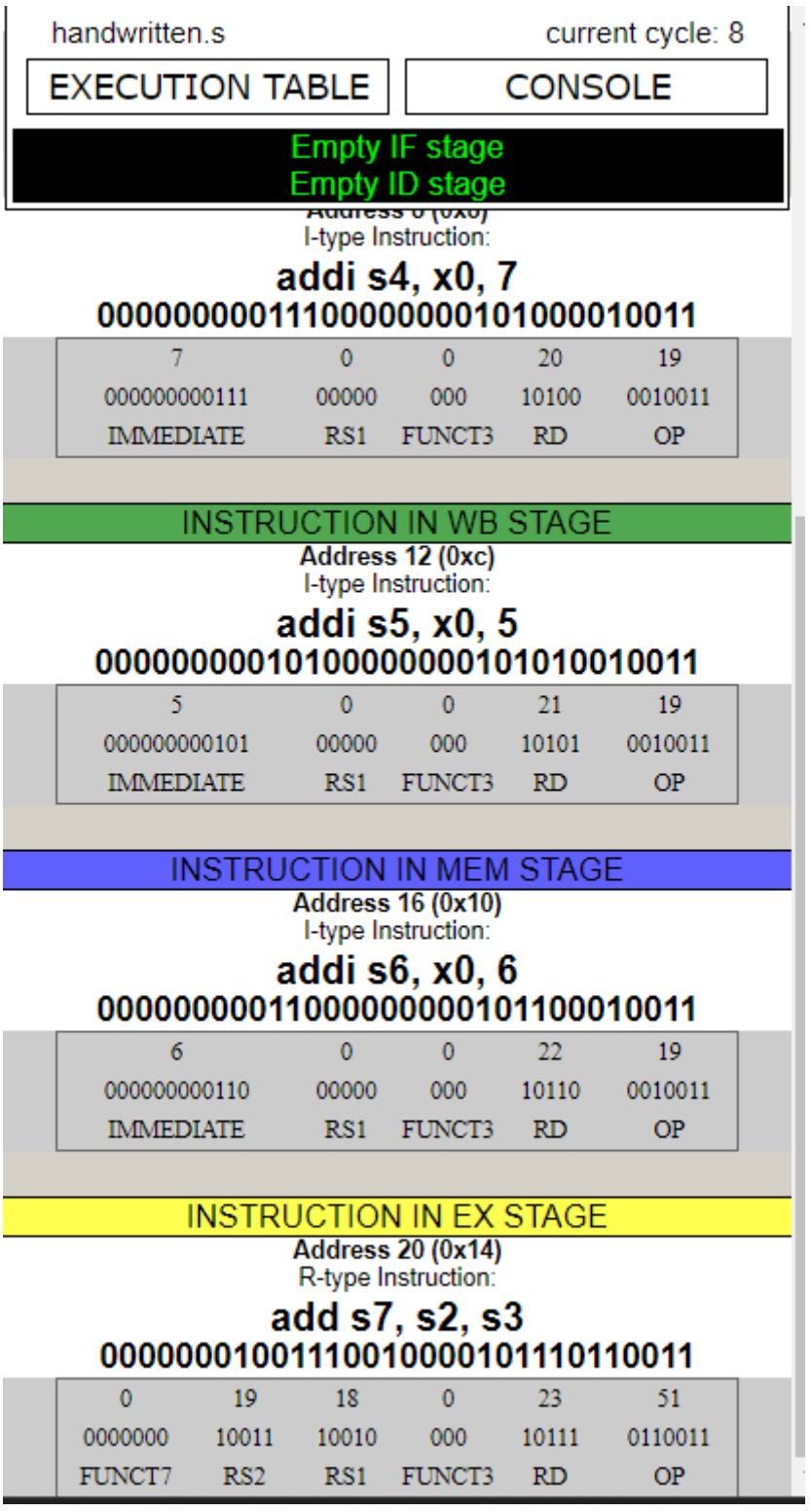
EXECUTION TABLE | CONSOLE

Empty IF stage

4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

8° Step


handwritten.s
current cycle: 8
EXECUTION TABLE
CONSOLE
Empty IF stage
Empty ID stage
Instruction Memory
Data Memory
Registers
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN WB STAGE
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011
5 0 0 21 19


handwritten.s
current cycle: 8
EXECUTION TABLE
CONSOLE
Empty IF stage
Empty ID stage
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN WB STAGE
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011
5 0 0 21 19
000000000101 00000 000 10101 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN MEM STAGE
Address 16 (0x10)
I-type Instruction:
addi s6, x0, 6
00000000011000000000101100010011
6 0 0 22 19
000000000110 00000 000 10110 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN EX STAGE
Address 20 (0x14)
R-type Instruction:
add s7, s2, s3
00000001001110010000101110110011
0 19 18 0 23 51
0000000 10011 10010 000 10111 0110011
FUNCT7 RS2 RS1 FUNCT3 RD OP

Empty IF stage
Empty ID stage

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	00000000000000000000000000000101
22	s6	0	00000000000000000000000000000000

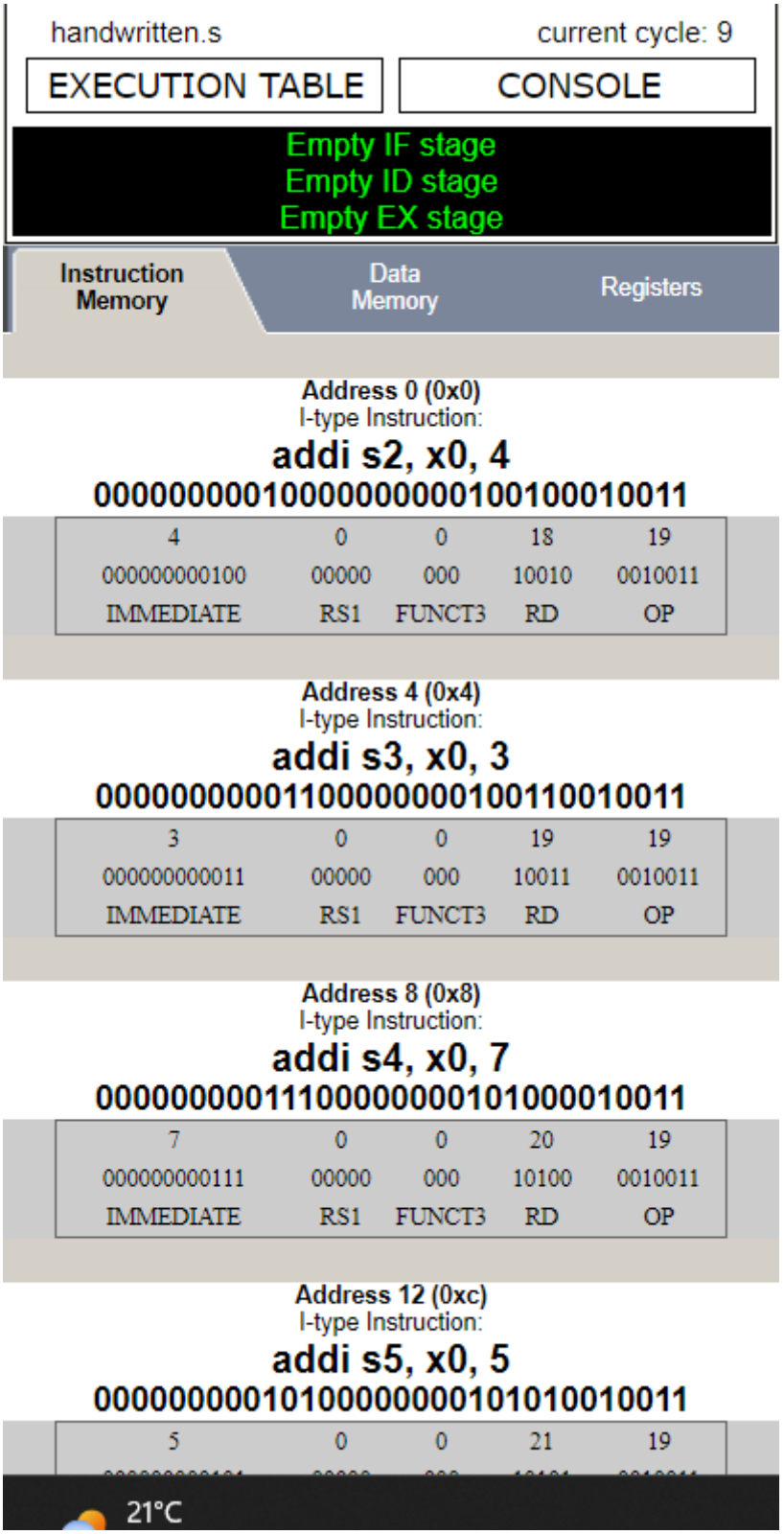
handwritten.s current cycle: 8

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage

5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	00000000000000000000000000000101
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

9° Step


handwritten.s
current cycle: 9
EXECUTION TABLE
CONSOLE
Empty IF stage
Empty ID stage
Empty EX stage
Instruction Memory
Data Memory
Registers
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011
5 0 0 21 19
21°C

handwritten.s current cycle: 9

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19
000000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN WB STAGE

Address 16 (0x10)
I-type Instruction:

addi s6, x0, 6

00000000011000000000101100010011

6	0	0	22	19
000000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN MEM STAGE

Address 20 (0x14)
R-type Instruction:

add s7, s2, s3

00000001001110010000101110110011

0	19	18	0	23	51
0000000	10011	10010	000	10111	0110011
FUNCT7	RS2	RS1	FUNCT3	RD	OP

handwritten.s current cycle: 9

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	00000000000000000000000000000101

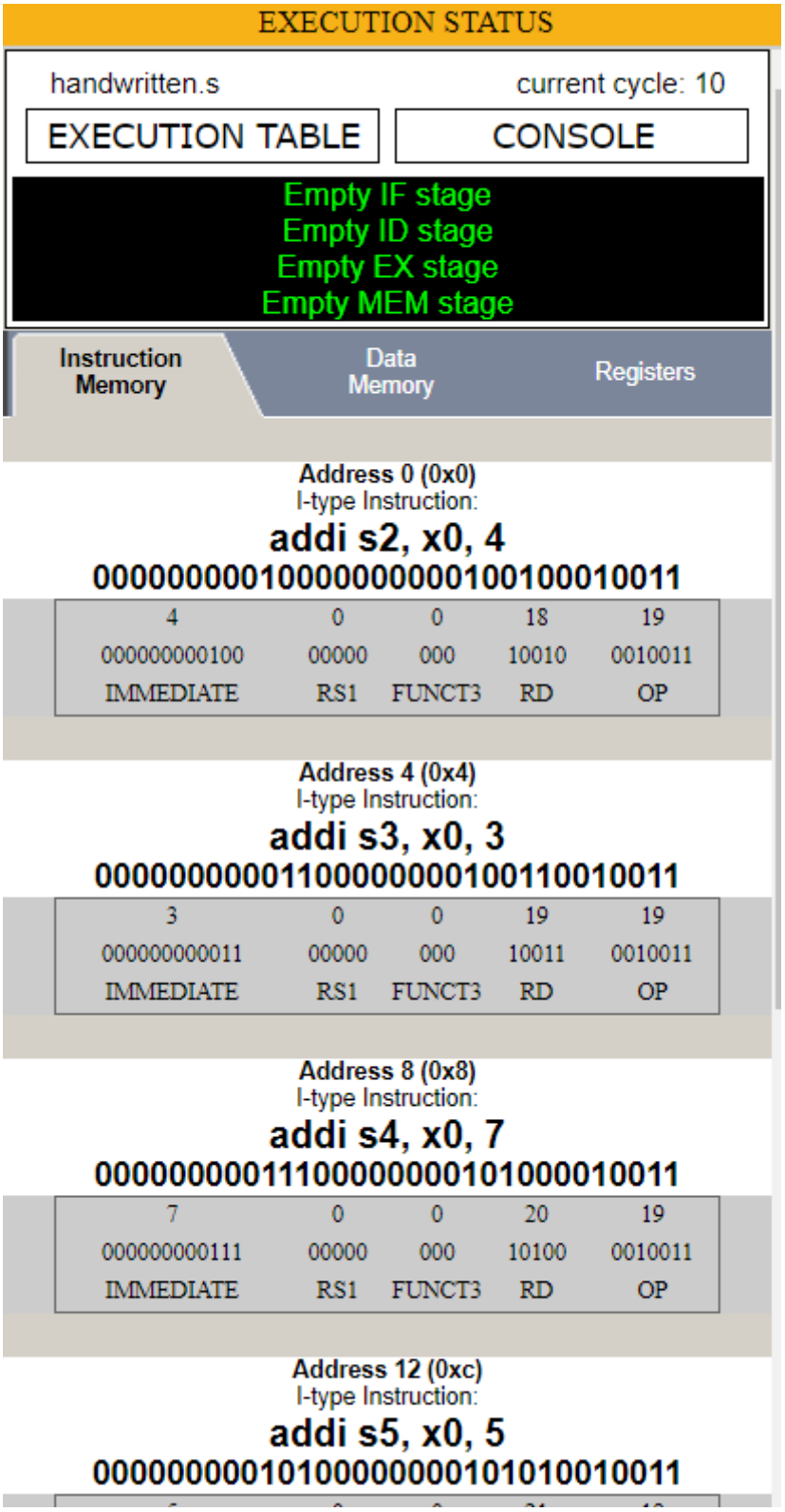
handwritten.s current cycle: 9

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage

6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	00000000000000000000000000000101
22	s6	6	00000000000000000000000000000110
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

10° Step


EXECUTION STATUS
handwritten.s
current cycle: 10
EXECUTION TABLE
CONSOLE
Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Instruction Memory
Data Memory
Registers
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011

EXECUTION STATUS

handwritten.s current cycle: 10

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19
000000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10)
I-type Instruction:

addi s6, x0, 6

00000000011000000000101100010011

6	0	0	22	19
000000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN WB STAGE

Address 20 (0x14)
R-type Instruction:

add s7, s2, s3

00000001001110010000101110110011

0	19	18	0	23	51
0000000	10011	10010	000	10111	0110011
FUNCT7	RS2	RS1	FUNCT3	RD	OP

EXECUTION STATUS

handwritten.s current cycle: 10

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111

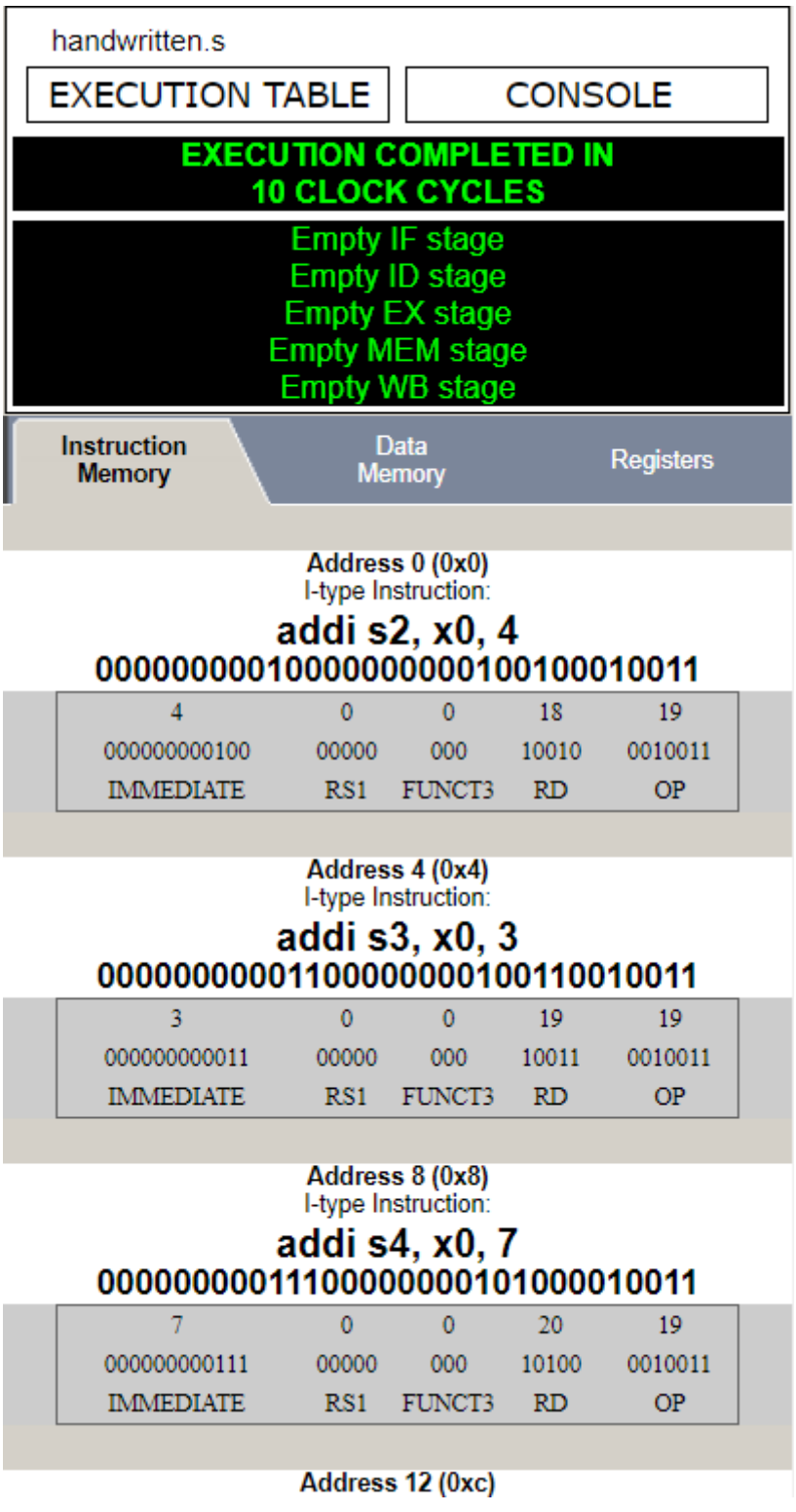
handwritten.s current cycle: 10

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage

7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	00000000000000000000000000000101
22	s6	6	00000000000000000000000000000110
23	s7	7	00000000000000000000000000000111
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

11° Step


handwritten.s
EXECUTION TABLE
CONSOLE
EXECUTION COMPLETED IN
10 CLOCK CYCLES
Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage
Instruction Memory
Data Memory
Registers
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 12 (0xc)

EXECUTION STATUS

handwritten.s

EXECUTION TABLE | CONSOLE

EXECUTION COMPLETED IN 10 CLOCK CYCLES

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19
000000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10)
I-type Instruction:

addi s6, x0, 6

00000000011000000000101100010011

6	0	0	22	19
000000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 20 (0x14)
R-type Instruction:

add s7, s2, s3

00000001001110010000101110110011

0	19	18	0	23	51
0000000	10011	10010	000	10111	0110011
FUNCT7	RS2	RS1	FUNCT3	RD	OP

EXECUTION STATUS

handwritten.s

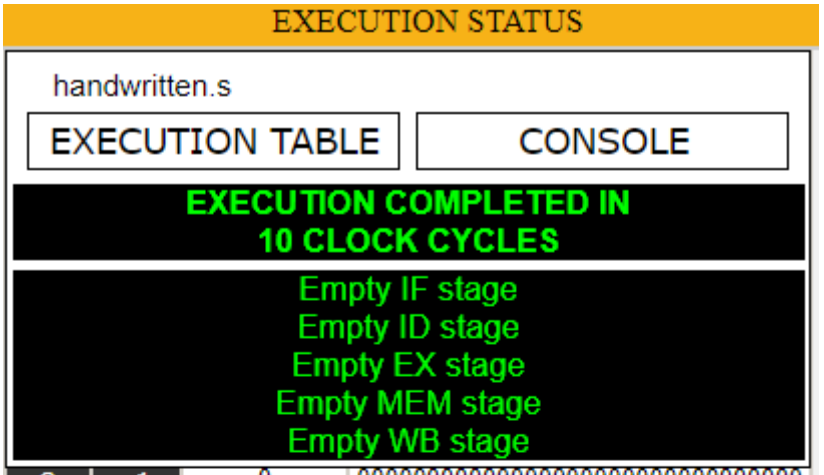
EXECUTION TABLE | CONSOLE

EXECUTION COMPLETED IN 10 CLOCK CYCLES

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100

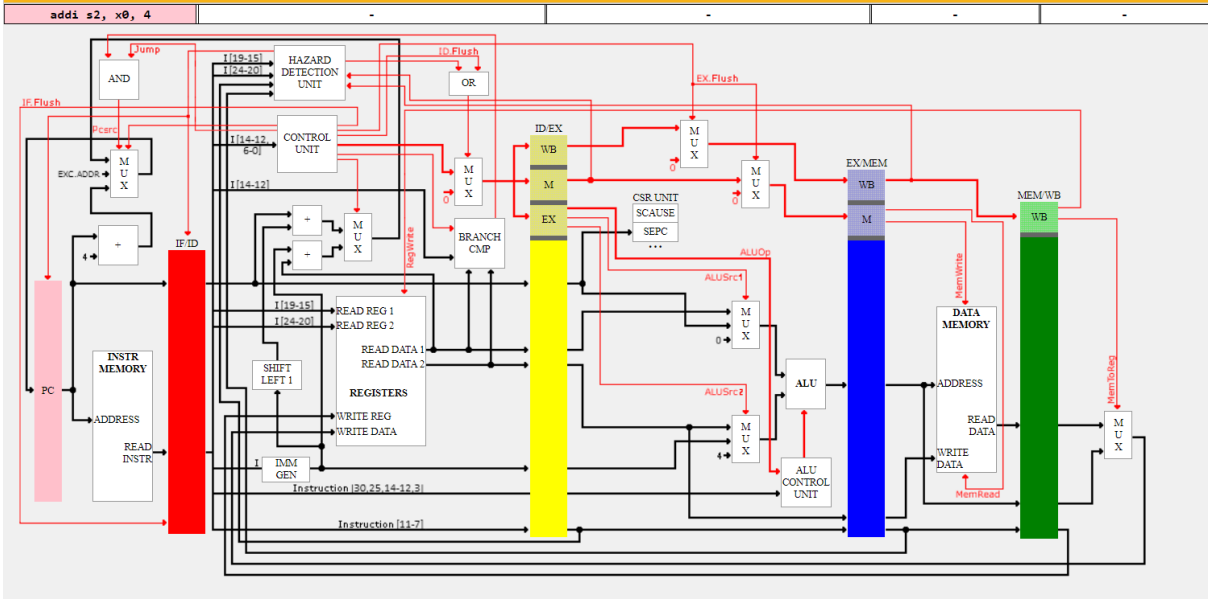


9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	00000000000000000000000000000101
22	s6	6	00000000000000000000000000000110
23	s7	7	00000000000000000000000000000111
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

b)Passagem em três estágios representativos do Pipeline (“SCHEMA LAYOUT”)

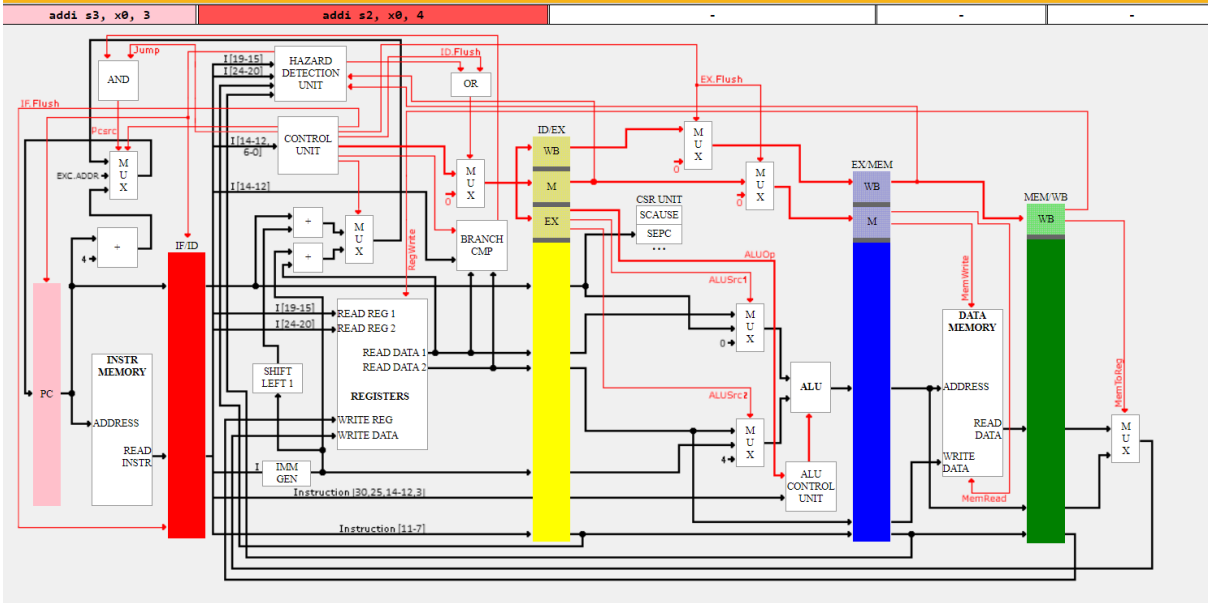
SCHEMA LAYOUT

addi s2, x0, 4	-	-	-	-



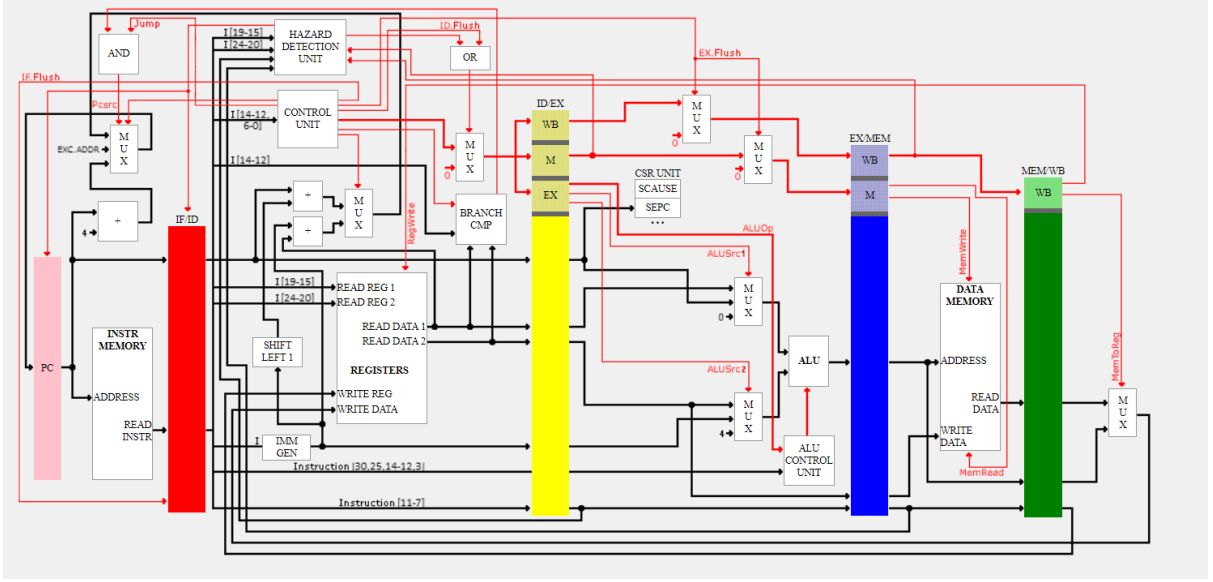
SCHEMA LAYOUT

addi s3, x0, 3	addi s2, x0, 4	-	-	-



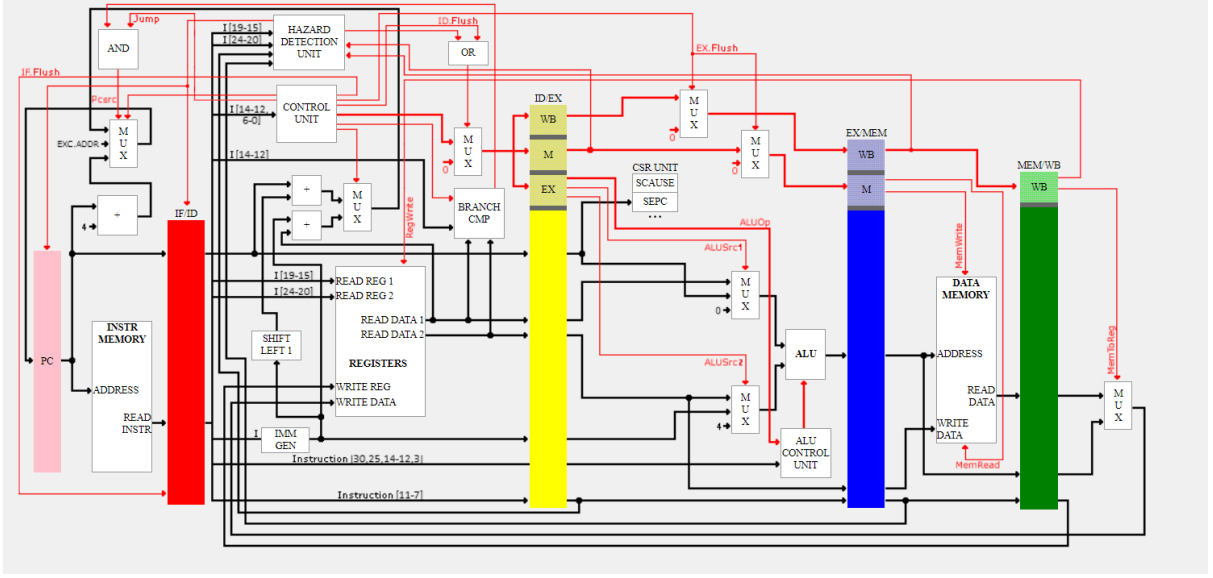
SCHEMA LAYOUT

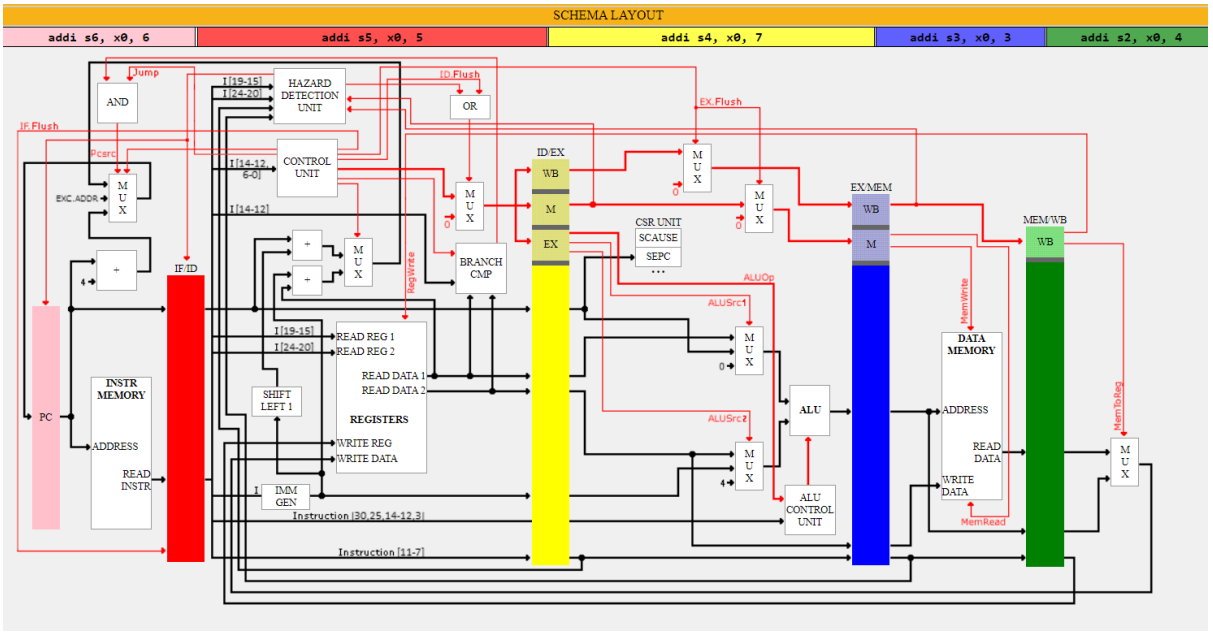
addi s4, x0, 7	addi s3, x0, 3	addi s2, x0, 4	-	-



SCHEMA LAYOUT

addi s5, x0, 5	addi s4, x0, 7	addi s3, x0, 3	addi s2, x0, 4	-





c) Resultado final da execução em Pipeline, por meio da Tabela da Execução do Programa (“EXECUTION TABLE”).

EXECUTION TABLE

FULL LOOPS	CPU Cycles									
Instruction	1	2	3	4	5	6	7	8	9	10
addi s2, x0, 4	F	D	X	M	W					
addi s3, x0, 3		F	D	X	M	W				
addi s4, x0, 7			F	D	X	M	W			
addi s5, x0, 5				F	D	X	M	W		
addi s6, x0, 6					F	D	X	M	W	
add s7, s2, s3						F	D	X	M	W

d) Ciclos de CPU necessários para executar esse programa.
Foram necessários 10 ciclos.

2.

EXECUTION STATUS

handwritten.s current cycle: -

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

Instruction Memory | Data Memory | Registers

Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4

00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3

00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

EXECUTION STATUS

handwritten.s current cycle: -

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19
000000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10)
I-type Instruction:

addi s6, x0, 6

00000000011000000000101100010011

6	0	0	22	19
000000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 20 (0x14)
R-type Instruction:

add s7, s2, s3

00000001001110010000101110110011

0	19	18	0	23	51
0000000	10011	10010	000	10111	0110011
FUNCT7	RS2	RS1	FUNCT3	RD	OP

EXECUTION STATUS

handwritten.s current cycle: -

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000

EXECUTION STATUS

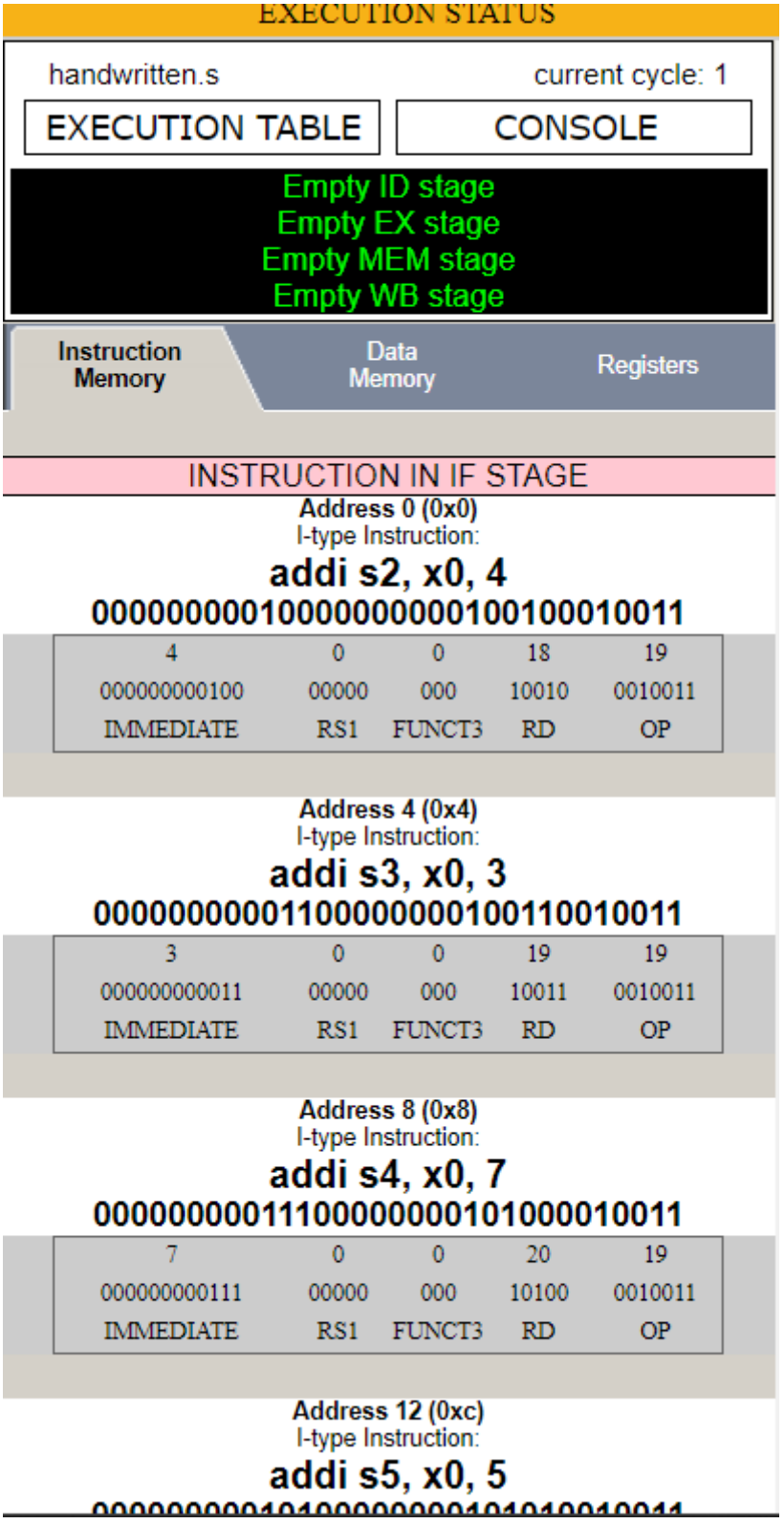
handwritten.s current cycle: -

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

1° Step


EXECUTION STATUS
handwritten.s
current cycle: 1
EXECUTION TABLE
CONSOLE
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage
Instruction Memory
Data Memory
Registers
INSTRUCTION IN IF STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5

EXECUTION STATUS

handwritten.s current cycle: 1

EXECUTION TABLE | CONSOLE

Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000

EXECUTION STATUS

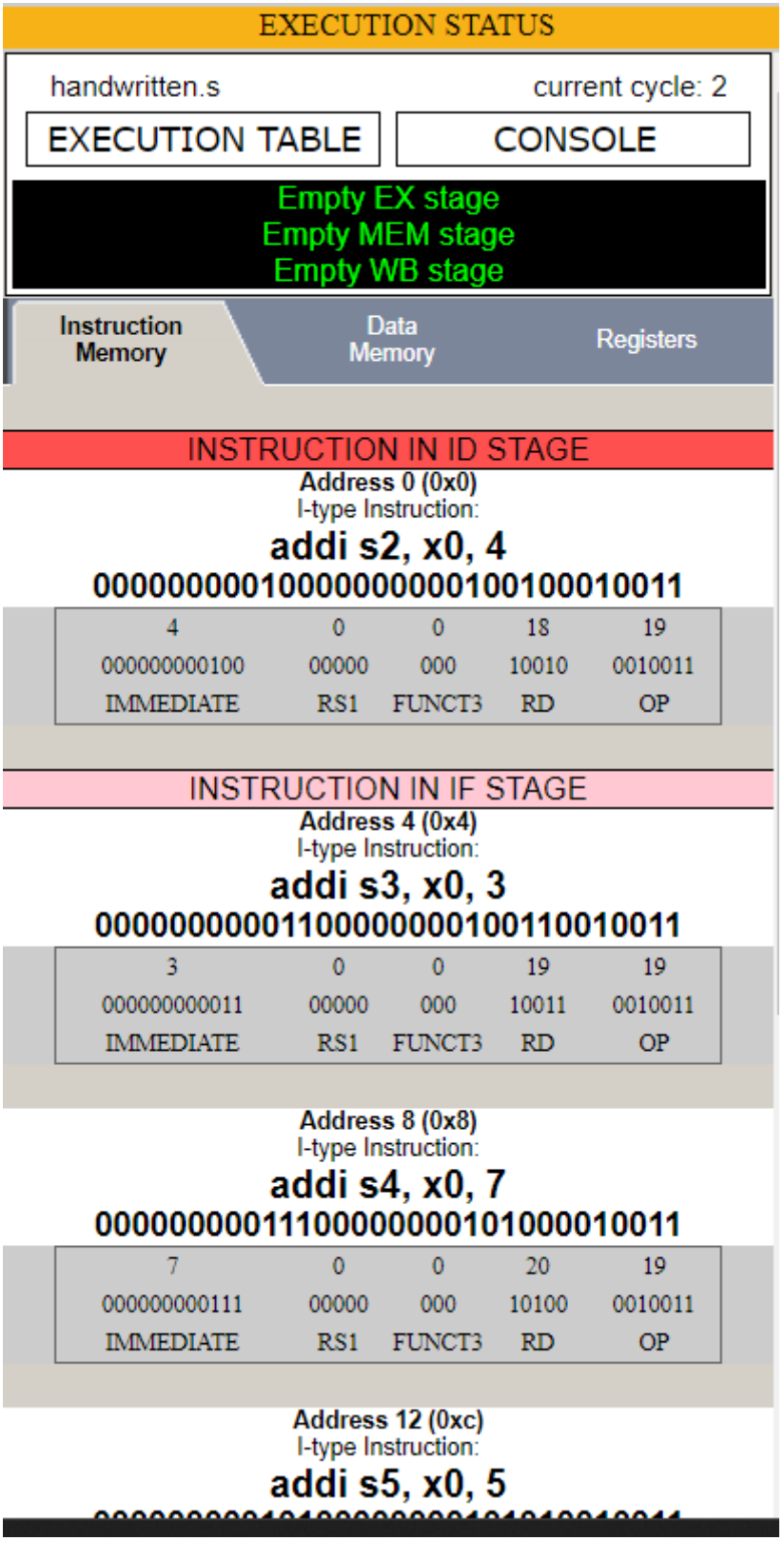
handwritten.s current cycle: 1

EXECUTION TABLE | CONSOLE

Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

2° Step


EXECUTION STATUS
handwritten.s
current cycle: 2
EXECUTION TABLE
CONSOLE
Empty EX stage
Empty MEM stage
Empty WB stage
Instruction Memory
Data Memory
Registers
INSTRUCTION IN ID STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN IF STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5

EXECUTION STATUS

handwritten.s current cycle: 2

EXECUTION TABLE | CONSOLE

Empty EX stage
Empty MEM stage
Empty WB stage

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000

EXECUTION STATUS

handwritten.s current cycle: 2

EXECUTION TABLE | CONSOLE

Empty EX stage
Empty MEM stage
Empty WB stage

6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000
25	s9	0	00000000000000000000000000000000
26	s10	0	00000000000000000000000000000000
27	s11	0	00000000000000000000000000000000
28	t3	0	00000000000000000000000000000000
29	t4	0	00000000000000000000000000000000
30	t5	0	00000000000000000000000000000000
31	t6	0	00000000000000000000000000000000

3° Step

EXECUTION STATUS

handwritten.s current cycle: 3

EXECUTION TABLE | CONSOLE

Empty MEM stage
Empty WB stage

Instruction Memory | Data Memory | Registers

INSTRUCTION IN EX STAGE

Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4
00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN ID STAGE

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3
00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN IF STAGE

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7
00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

EXECUTION STATUS

handwritten.s current cycle: 3

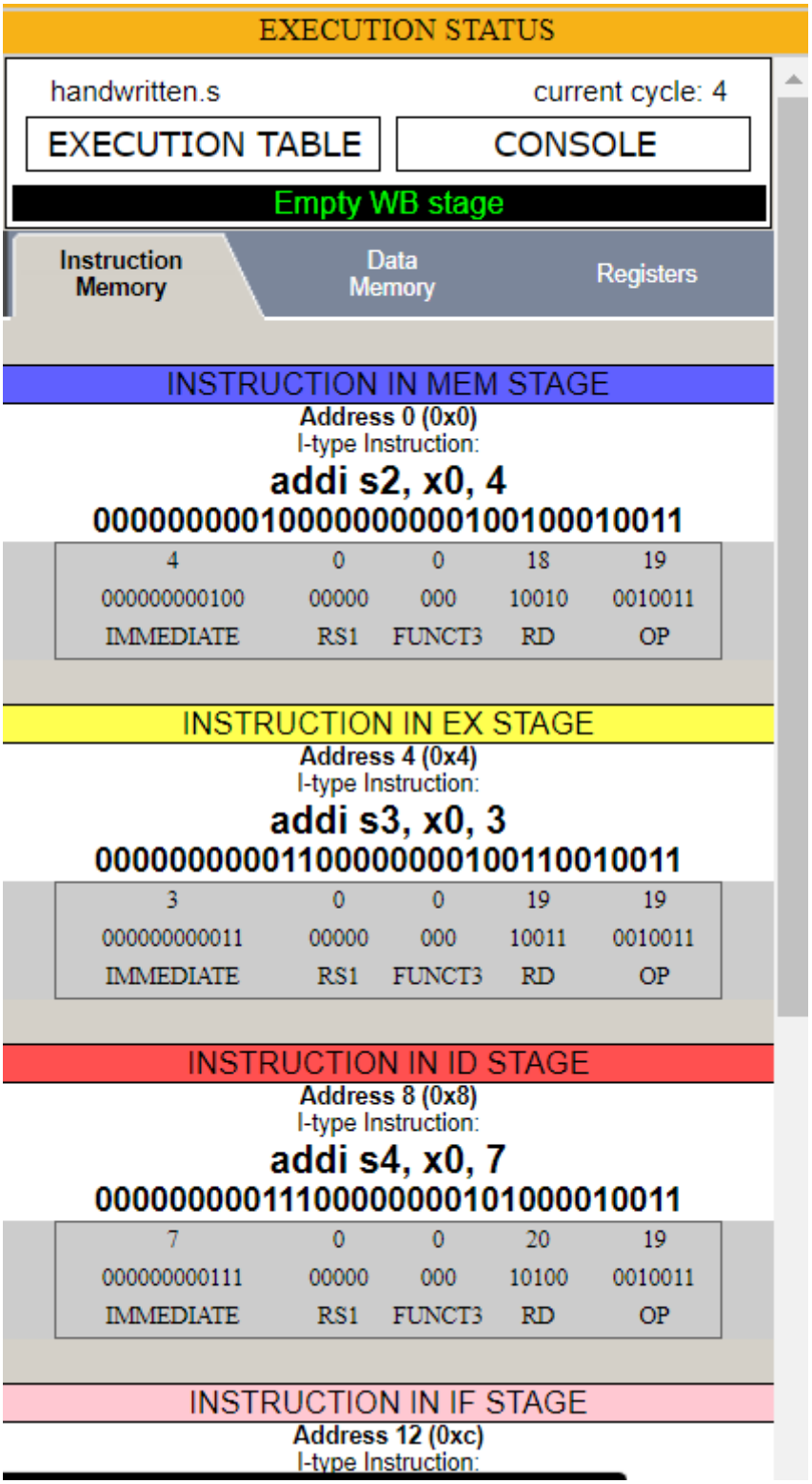
EXECUTION TABLE | CONSOLE

Empty MEM stage
Empty WB stage

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000

4° Step


EXECUTION STATUS
handwritten.s
current cycle: 4
EXECUTION TABLE
CONSOLE
Empty WB stage
Instruction Memory
Data Memory
Registers
INSTRUCTION IN MEM STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN EX STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN ID STAGE
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN IF STAGE
Address 12 (0xc)
I-type Instruction:

EXECUTION STATUS

handwritten.s current cycle: 4

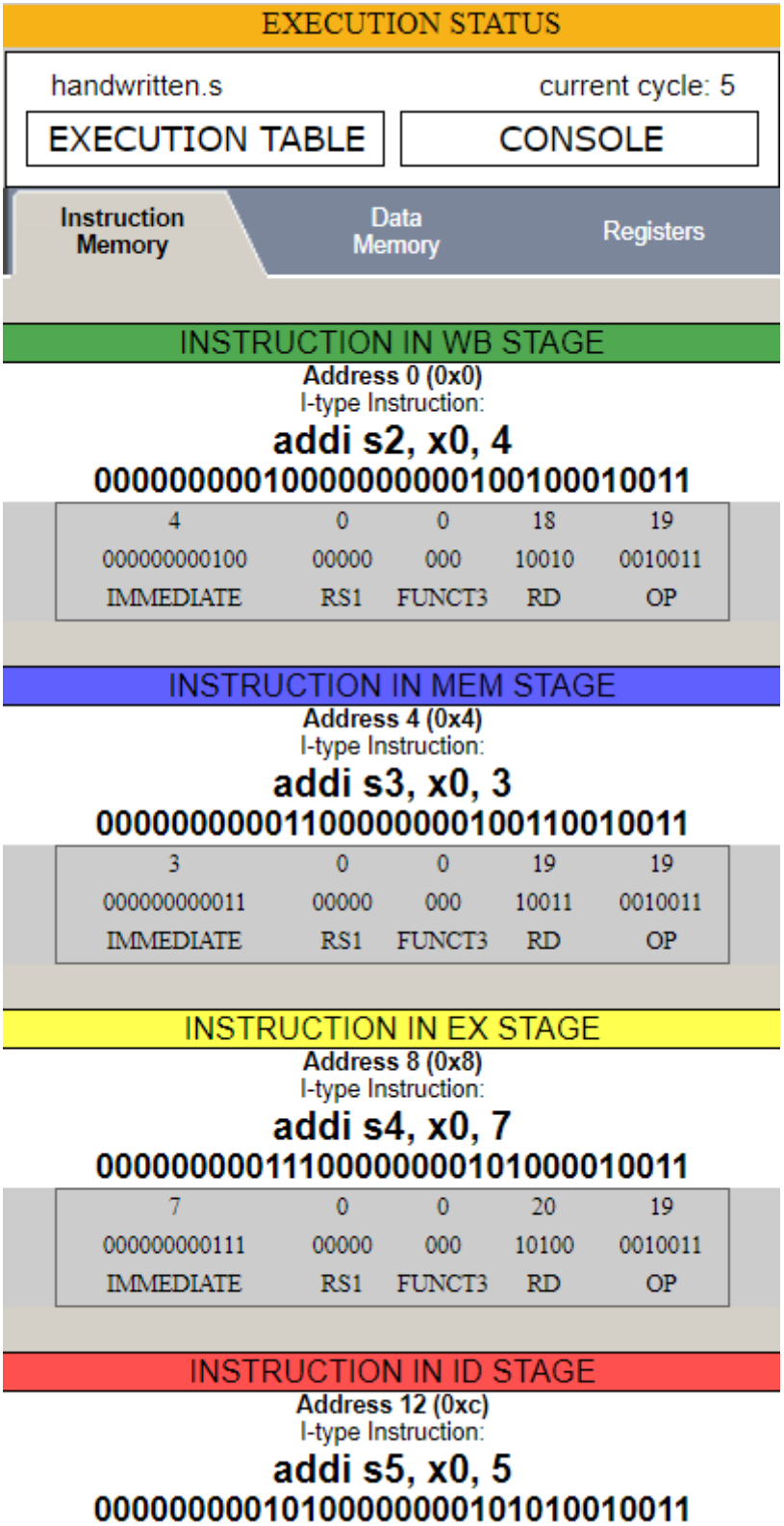
EXECUTION TABLE | CONSOLE

Empty WB stage

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	0	00000000000000000000000000000000
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000

5° Step


EXECUTION STATUS
handwritten.s
current cycle: 5
EXECUTION TABLE
CONSOLE
Instruction Memory
Data Memory
Registers
INSTRUCTION IN WB STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN MEM STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN EX STAGE
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN ID STAGE
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011

EXECUTION STATUS

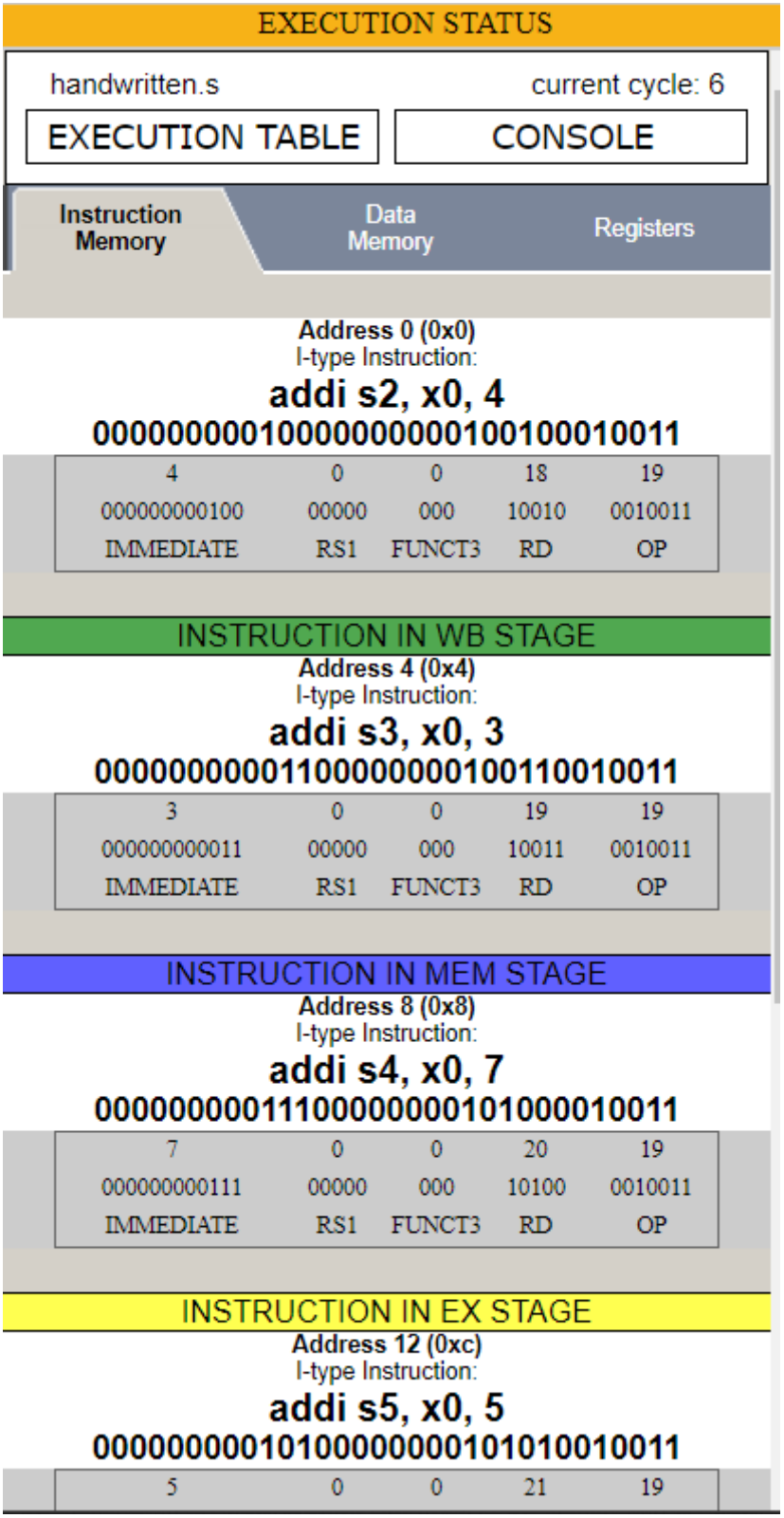
handwritten.s current cycle: 5

EXECUTION TABLE | CONSOLE

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	0	00000000000000000000000000000000
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000

6° Step


EXECUTION STATUS
handwritten.s
current cycle: 6
EXECUTION TABLE
CONSOLE
Instruction Memory
Data Memory
Registers
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN WB STAGE
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN MEM STAGE
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN EX STAGE
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011
5 0 0 21 19

EXECUTION STATUS

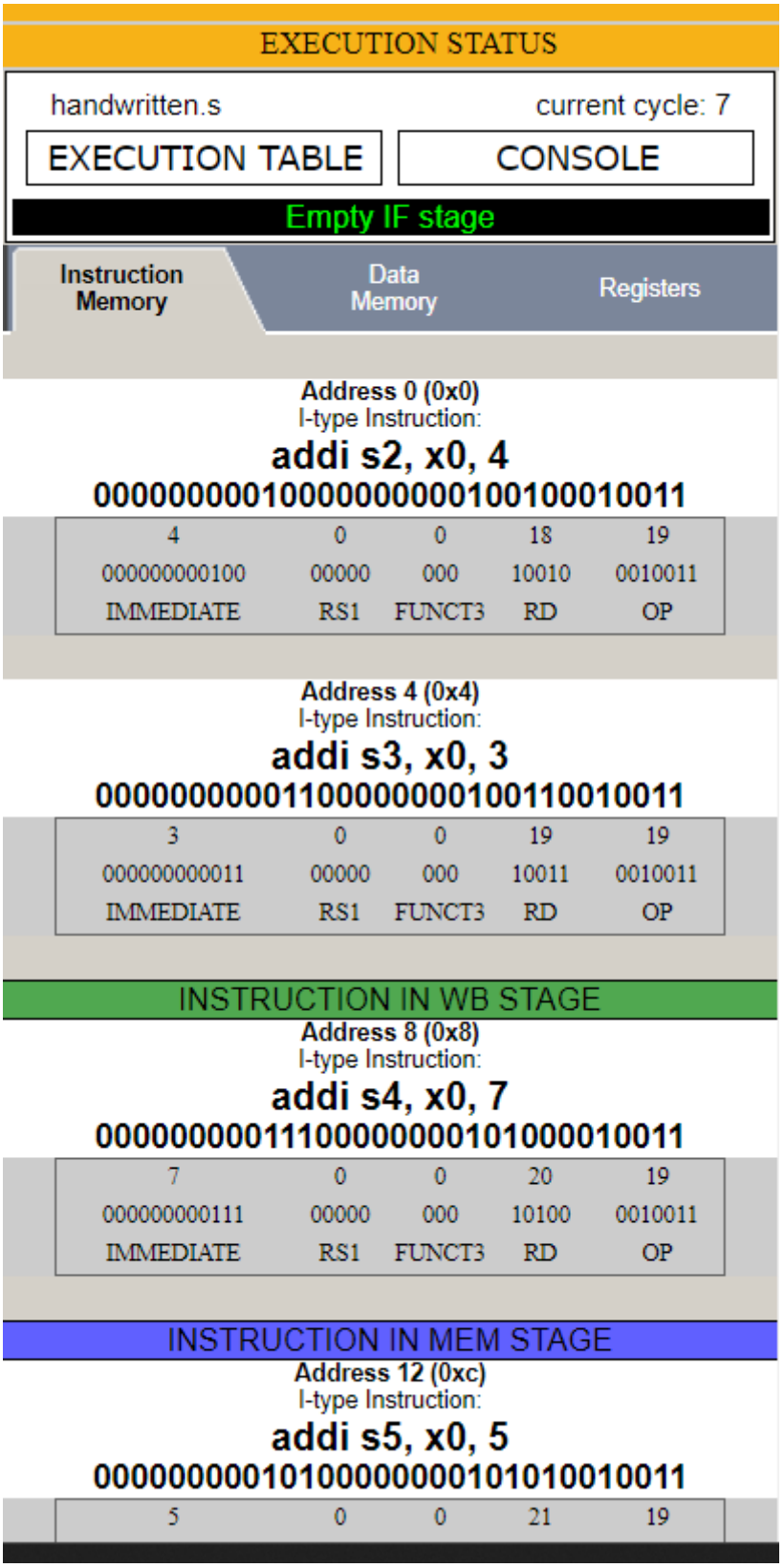
handwritten.s current cycle: 6

EXECUTION TABLE | CONSOLE

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	0	00000000000000000000000000000000
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000
24	s8	0	00000000000000000000000000000000

7° Step


EXECUTION STATUS
handwritten.s
current cycle: 7
EXECUTION TABLE
CONSOLE
Empty IF stage
Instruction Memory
Data Memory
Registers
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100010011
4 0 0 18 19
000000000100 00000 000 10010 0010011
IMMEDIATE RS1 FUNCT3 RD OP
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
3 0 0 19 19
000000000011 00000 000 10011 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN WB STAGE
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000010011
7 0 0 20 19
000000000111 00000 000 10100 0010011
IMMEDIATE RS1 FUNCT3 RD OP
INSTRUCTION IN MEM STAGE
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
00000000010100000000101010010011
5 0 0 21 19

EXECUTION STATUS

handwritten.s current cycle: 7

EXECUTION TABLE | CONSOLE

Empty IF stage

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	0	00000000000000000000000000000000
22	s6	0	00000000000000000000000000000000
23	s7	0	00000000000000000000000000000000

8° Step

EXECUTION STATUS

handwritten.s current cycle: 8

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage

Instruction Memory | Data Memory | Registers

Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4

00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3

00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

INSTRUCTION IN WB STAGE

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

5	0	0	21	19

EXECUTION STATUS

handwritten.s current cycle: 8

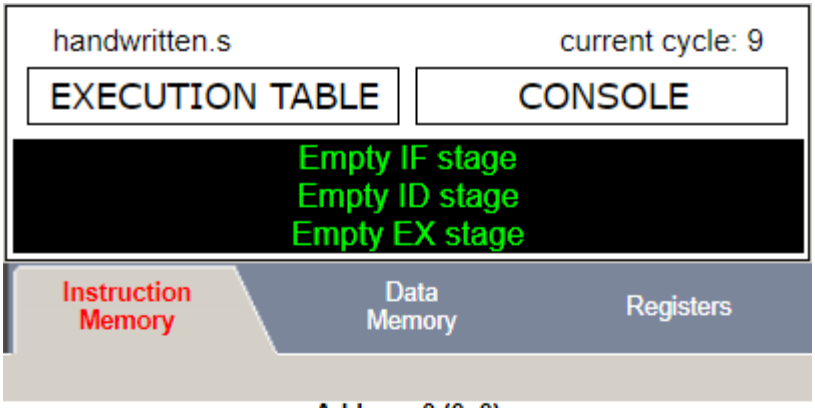
EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	00000000000000000000000000000101
22	s6	0	00000000000000000000000000000000

9° Step



Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4

00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3

00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

handwritten.s current cycle: 9

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage

Instruction Memory | Data Memory | **Registers**

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	00000000000000000000000000000101

10° Step

EXECUTION STATUS

handwritten.s current cycle: 10

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage

Instruction Memory | Data Memory | Registers

Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4

00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3

00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8)
I-type Instruction:

addi s4, x0, 7

00000000011100000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc)
I-type Instruction:

addi s5, x0, 5

00000000010100000000101010010011

EXECUTION STATUS

handwritten.s current cycle: 10

EXECUTION TABLE | CONSOLE

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage

Instruction Memory | Data Memory | Registers

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	00000000000000000000000000000000
1	ra	0	00000000000000000000000000000000
2	sp	5120	00000000000000000001010000000000
3	gp	1024	00000000000000000000010000000000
4	tp	0	00000000000000000000000000000000
5	t0	0	00000000000000000000000000000000
6	t1	0	00000000000000000000000000000000
7	t2	0	00000000000000000000000000000000
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	00000000000000000000000000000000
10	a0	0	00000000000000000000000000000000
11	a1	0	00000000000000000000000000000000
12	a2	0	00000000000000000000000000000000
13	a3	0	00000000000000000000000000000000
14	a4	0	00000000000000000000000000000000
15	a5	0	00000000000000000000000000000000
16	a6	0	00000000000000000000000000000000
17	a7	0	00000000000000000000000000000000
18	s2	4	00000000000000000000000000000100
19	s3	3	00000000000000000000000000000011
20	s4	7	00000000000000000000000000000111

11° Step

EXECUTION STATUS

handwritten.s

EXECUTION TABLE | CONSOLE

EXECUTION COMPLETED IN 10 CLOCK CYCLES

Empty IF stage
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage

Instruction Memory | Data Memory | Registers

Address 0 (0x0)
I-type Instruction:

addi s2, x0, 4

00000000010000000000100100010011

4	0	0	18	19
000000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4)
I-type Instruction:

addi s3, x0, 3

00000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8)
I-type Instruction:

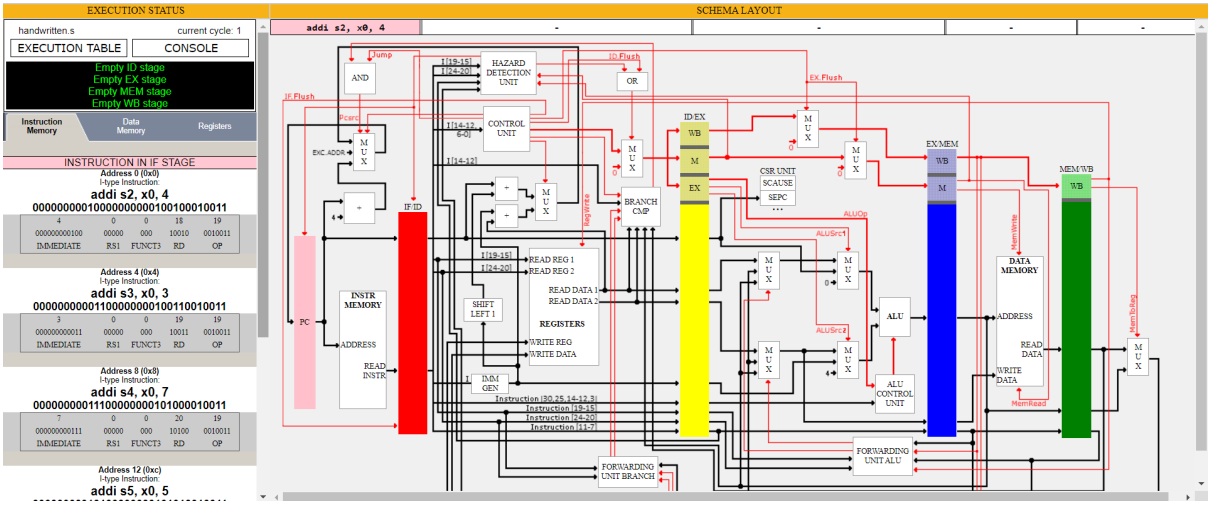
addi s4, x0, 7

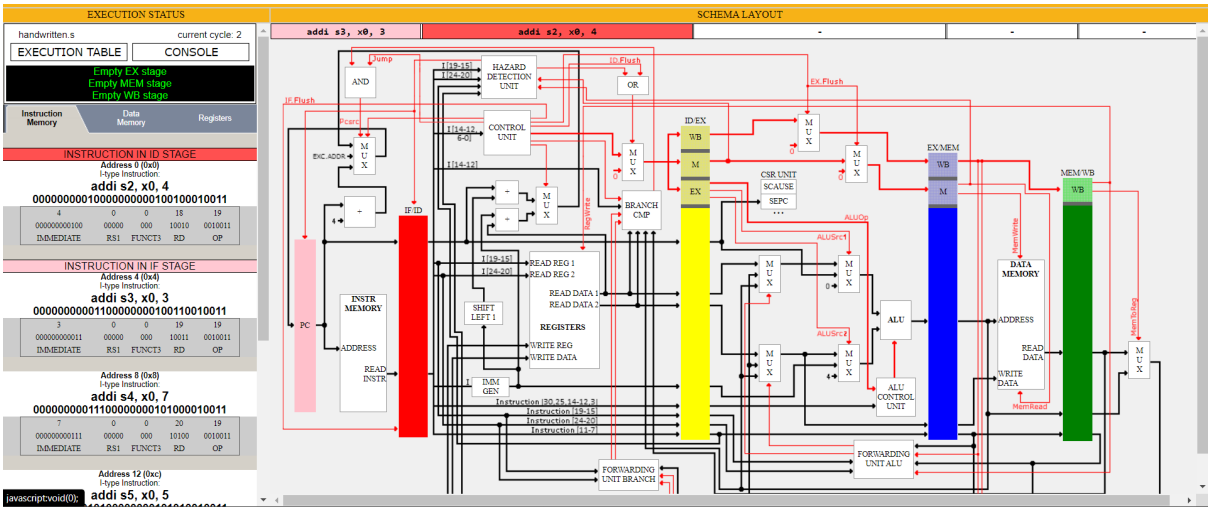
00000000011100000000101000010011

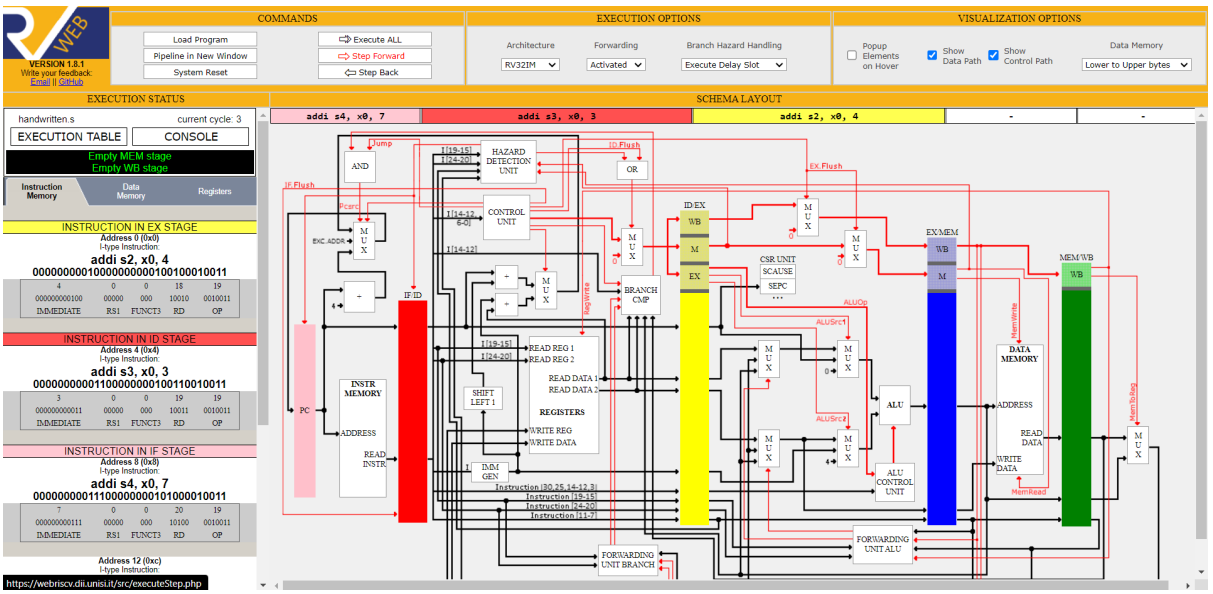
7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

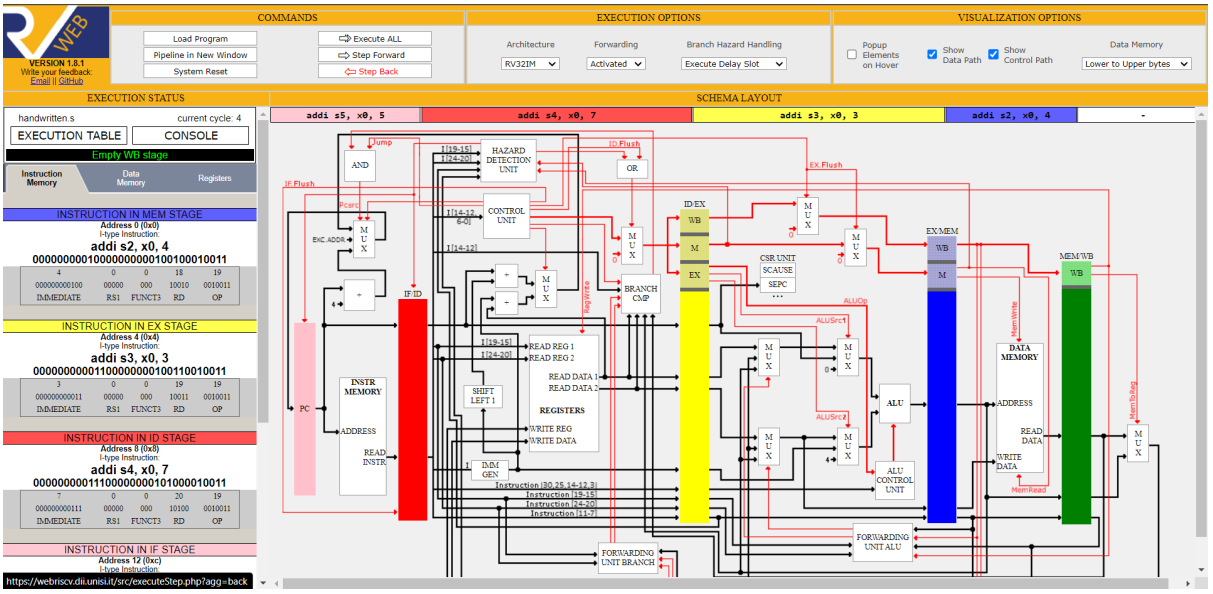
Address 12 (0xc)

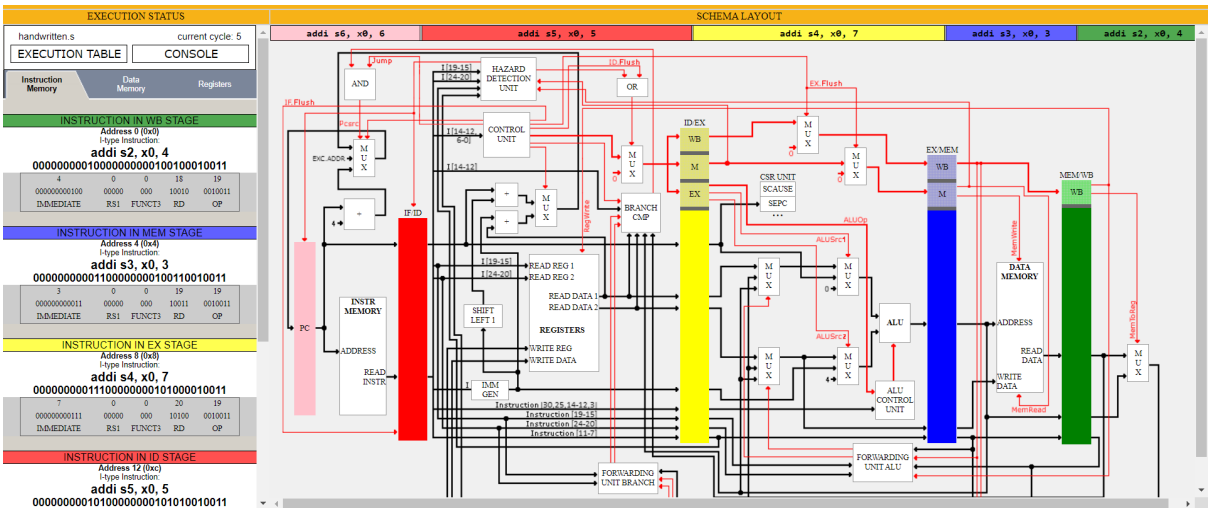
b)


EXECUTION STATUS
handwritten.s
current cycle: 1
EXECUTION TABLE
CONSOLE
Empty ID stage
Empty EX stage
Empty MEM stage
Empty WB stage
Instruction Memory
Data Memory
Registers
INSTRUCTION IN IF STAGE
Address 0 (0x0)
I-type Instruction:
addi s2, x0, 4
00000000010000000000100100011
Address 4 (0x4)
I-type Instruction:
addi s3, x0, 3
00000000001100000000100110010011
Address 8 (0x8)
I-type Instruction:
addi s4, x0, 7
00000000011100000000101000011
Address 12 (0xc)
I-type Instruction:
addi s5, x0, 5
SCHEMA LAYOUT
addi s2, x0, 4
HAZARD DETECTION UNIT
CONTROL UNIT
BRANCH CMP
CSR UNIT
REGISTERS
ALU
ALU CONTROL UNIT
DATA MEMORY
INSTR MEMORY
IMM GEN
FORWARDING UNIT ALU
FORWARDING UNIT BRANCH


EXECUTION STATUS
handwritten.s
current cycle: 2
EXECUTION TABLE
CONSOLE
Empty EX stage
Empty MEM stage
Empty WB stage
INSTRUCTION IN ID STAGE
INSTRUCTION IN IF STAGE
addi s2, x0, 4
addi s3, x0, 3
addi s4, x0, 7
addi s5, x0, 5
javascript:void(0);
SCHEMA LAYOUT
addi s3, x0, 3
addi s2, x0, 4


VERSION 1.8.1
COMMANDS
Load Program
Pipeline in New Window
System Reset
Execute ALL
Step Forward
Step Back
EXECUTION OPTIONS
Architecture
RV32IM
Forwarding
Activated
Branch Hazard Handling
Execute Delay Slot
VISUALIZATION OPTIONS
Popup Elements on Hover
Show Data Path
Show Control Path
Data Memory
Lower to Upper bytes
EXECUTION STATUS
handwritten.s
current cycle: 3
EXECUTION TABLE
CONSOLE
Empty MEM stage
Empty WB stage
INSTRUCTION IN EX STAGE
INSTRUCTION IN ID STAGE
INSTRUCTION IN IF STAGE
addi s2, x0, 4
addi s3, x0, 3
addi s4, x0, 7
https://webriscv.dii.unisi.it/src/executeStep.php
SCHEMA LAYOUT
addi s4, x0, 7
addi s3, x0, 3
addi s2, x0, 4





c)

EXECUTION TABLE

FULL LOOPS	CPU Cycles									
Instruction	1	2	3	4	5	6	7	8	9	10
addi s2, x0, 4	F	D	X	M	W					
addi s3, x0, 3		F	D	X	M	W				
addi s4, x0, 7			F	D	X	M	W			
addi s5, x0, 5				F	D	X	M	W		
addi s6, x0, 6					F	D	X	M	W	
add s7, s2, s3						F	D	X	M	W

d) Foram necessários 10 ciclos.