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#### Roteiro 08

1. Programa 1: addi s2, zero, 4 addi s3, zero, 3 addi s4, zero, 7 addi s5, zero, 5 addi s6, zero, 6 add s7, s2, s3

a) Conteúdo da Memória de Instruções ("Instruction Memory") e dos Registradores ("Registers"), no início e no final da execução do programa.

Instruction Memory	Data Memory	Registers
	Address 0 (0x0) I-type Instruction:	

#### addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4) I-type Instruction:

# addi s3, x0, 3 0000000001100000000100110010011

3	0	0	19	19
00000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8) I-type Instruction:

# addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

#### Address 8 (0x8)

I-type Instruction:

# addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

# Address 12 (0xc) I-type Instruction:

# addi s5, x0, 5 0000000010100000000101010010011

5	0	0	21	19
00000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

# Address 16 (0x10) I-type Instruction:

# addi s6, x0, 6 000000001100000000101100010011

6	0	0	22	19
00000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

# Address 20 (0x14)

R-type Instruction:

0	19	18	0	23	51	
0000000	10011	10010	000	10111	0110011	
FUNCT7	RS2	RS1	FUNCT3	RD	OP	

	Instruction Memory		Data Memory	Registers
		5		,
R.No.	Reg.Id.	Dec.Val	Binary \	Value (32 bit)
0	x0	0	000000000000000	000000000000000000000000000000000000000
1	ra	0	000000000000000	000000000000000000000000000000000000000
2	sp	5120	000000000000000	000001010000000000
3	gp	1024	00000000000000	00000010000000000
4	tp	0	000000000000000	000000000000000000000000000000000000000
5	t0	0	000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000	000000000000000000000000000000000000000
7	t2	0	000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000	000001010000000000
9	s1	0	000000000000000	000000000000000000000000000000000000000
10	a0	0	00000000000000	000000000000000000000000000000000000000
11	a1	0	00000000000000	000000000000000000000000000000000000000
12	a2	0	00000000000000	000000000000000000000000000000000000000
13	<b>a</b> 3	0	00000000000000	000000000000000000000000000000000000000
14	a4	0	00000000000000	000000000000000000000000000000000000000
15	a5	0	00000000000000	000000000000000000000000000000000000000
16	a6	0	00000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000	000000000000000000000000000000000000000
18	s2	0	000000000000000	000000000000000000000000000000000000000
19	s3	0	000000000000000	000000000000000000000000000000000000000
20	s4	0	000000000000000	000000000000000000000000000000000000000

/	LZ	v	000000000000000000000000000000000000000
8	s0/fp	5120	0000000000000000001010000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5	0	000000000000000000000000000000000000000
31	t6	0	000000000000000000000000000000000000000

Instruction
Memory

Data Memory

Registers

# INSTRUCTION IN IF STAGE

Address 0 (0x0) I-type Instruction:

# addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4) I-type Instruction:

#### addi s3, x0, 3 0000000001100000000100110010011

3	0	0	19	19
00000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8) I-type Instruction:

# addi s4, x0, 7 0000000011100000000101000010011

,	U	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

addi s5, x0, 5

000000004040400000004040404004004

Address 8 (0x8) I-type Instruction:

# addi s4, x0, 7 000000001110000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

# addi s5, x0, 5 0000000010100000000101010010011

5	0	0	21	19
00000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10) I-type Instruction:

# addi s6, x0, 6 0000000011000000000101100010011

6	0	0	22	19
00000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 20 (0x14) R-type Instruction:

0	19	18	0	23	51	
0000000	10011	10010	000	10111	0110011	
FUNCT7	RS2	RS1	FUNCT3	RD	OP	

	Instruction Memory		Data Memory	Registers
R.No.	Reg.Id.	Dec.Val	Binary	Value (32 bit)
0	x0	0		000000000000000000000000000000000000000
1	ra	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
2	sp	5120	000000000000000000000000000000000000000	0000001010000000000
3	gp	1024	000000000000000000000000000000000000000	000000010000000000
4	tp	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000000000000000000000000000	0000001010000000000
9	s1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
13	a3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
21		۸	000000000000000000000000000000000000000	

7	t2	0	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000000101000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5	0	000000000000000000000000000000000000000
31	t6	0	000000000000000000000000000000000000000

2° Step

Instruction Memory Data Memory

Registers

#### INSTRUCTION IN ID STAGE

Address 0 (0x0) I-type Instruction:

# addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN IF STAGE

Address 4 (0x4) I-type Instruction:

# addi s3, x0, 3 0000000001100000000100110010011

3	0	0	19	19
00000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8) I-type Instruction:

#### addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

addi s5, x0, 5

00000000040400000000404040040044

	Instruction Memory		Data Memory	Registers
R.No.	Reg.Id.	Dec.Val	Binary '	Value (32 bit)
0	x0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
1	ra	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
2	sp	5120	000000000000000000000000000000000000000	00000010100000000000
3	gp	1024	000000000000000000000000000000000000000	000000010000000000
4	tp	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000000000000000000000000000	00000010100000000000
9	s1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
13	a3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000

6	t1	0	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000
8	s0/fp	5120	0000000000000000001010000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5	0	000000000000000000000000000000000000000
31	t6	0	000000000000000000000000000000000000000

Instruction Memory Data Memory

Registers

#### INSTRUCTION IN EX STAGE

Address 0 (0x0) I-type Instruction:

#### addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN ID STAGE

Address 4 (0x4) I-type Instruction:

#### addi s3, x0, 3 0000000001100000000100110010011

3	0	0	19	19
00000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN IF STAGE

Address 8 (0x8) I-type Instruction:

# addi s4, x0, 7 0000000011100000000101000010011

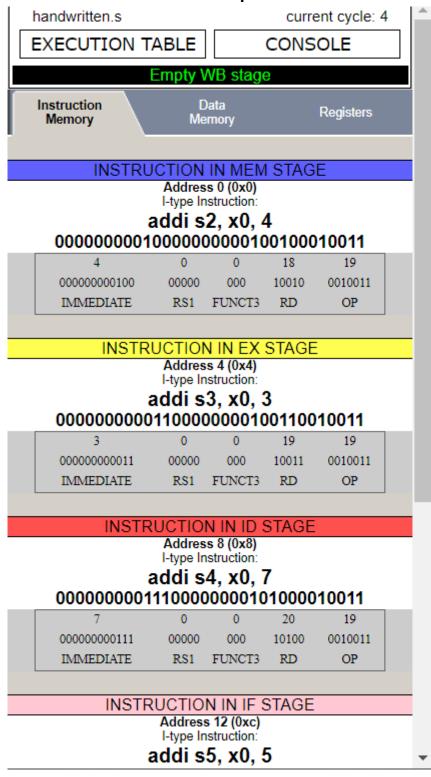
7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

	Instruction Memory	1	Data Memory	Registers
R.No.	Reg.Id.	Dec.Val	Binary '	Value (32 bit)
0	x0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
1	ra	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
2	sp	5120	000000000000000000000000000000000000000	0000001010000000000
3	gp	1024	000000000000000000000000000000000000000	000000010000000000
4	tp	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000000000000000000000000000	00000010100000000000
9	s1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
20	<b>s4</b>	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000

П

5	t0	0	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000
8	s0/fp	5120	0000000000000000001010000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	a3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5	0	000000000000000000000000000000000000000
31	t6	0	000000000000000000000000000000000000000



I	handwritten.s				current cycle: 4		
EX	EXECUTION TABLE			С	ONSOLE		
		Em	pty W	/B stage			
	Instruction Memory			ata nory	Registers		
R.No.	Reg.Id.	Dec.Val		Binary	Value (32 bit)		
0	x0	0	0000	000000000	000000000000000000000000000000000000000		
1	ra	0	0000	000000000	000000000000000000000000000000000000000		
2	sp	5120	0000	000000000	0000001010000000000		
3	gp	1024	0000	000000000	0000000010000000000		
4	tp	0	0000	000000000	000000000000000000000000000000000000000		
5	t0	0	0000	000000000	000000000000000000000000000000000000000		
6	t1	0	0000	000000000	000000000000000000000000000000000000000		
7	t2	0	0000	000000000	000000000000000000000000000000000000000		
8	s0/fp	5120	0000	000000000	0000001010000000000		
9	s1	0	0000	000000000	000000000000000000000000000000000000000		
10	a0	0	0000	000000000	000000000000000000000		
11	a1	0	0000	000000000	000000000000000000000		
12	a2	0	0000	000000000	000000000000000000000		
13	<b>a</b> 3	0	0000	000000000	000000000000000000000		
14	a4	0	0000	000000000	000000000000000000000		
15	a5	0	0000	000000000	000000000000000000000		
16	a6	0	0000	000000000	000000000000000000000		
17	a7	0	0000	000000000	000000000000000000000		
18	s2	0	0000	000000000	000000000000000000000000000000000000000		
19	s3	0			000000000000000000000		
20	s4	0			000000000000000000000		
21	s5	0			000000000000000000000		
22	s6	0			000000000000000000000		
23	s7	0	0000	000000000	000000000000000000000000000000000000000		

4	Ψ	v	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000
8	s0/fp	5120	0000000000000000001010000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5	0	000000000000000000000000000000000000000
31	t6	0	000000000000000000000000000000000000000

5° Step

Instruction Memory Data Memory

Registers

#### INSTRUCTION IN WB STAGE

Address 0 (0x0) I-type Instruction:

# addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN MEM STAGE

Address 4 (0x4) I-type Instruction:

# addi s3, x0, 3 0000000001100000000100110010011

3	0	0	19	19
00000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN EX STAGE

Address 8 (0x8) I-type Instruction:

#### addi s4, x0, 7 00000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN ID STAGE

Address 12 (0xc) I-type Instruction:

	Instruction Memory		Data Memory	Registers
R.No.	Reg.Id.	Dec.Val	Binary \	Value (32 bit)
0	x0	0		000000000000000000000000000000000000000
1	ra	0	000000000000000	0000000000000000000
2	sp	5120	000000000000000	000001010000000000
3	gp	1024	000000000000000	000000010000000000
4	tp	0	000000000000000	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000	0000010100000000000
9	s1	0	000000000000000	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
13	a3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000	000000000000000000000000000000000000000
18	s2	4	000000000000000000000000000000000000000	0000000000000000100
19	s3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
24	c0	n	000000000000000000000000000000000000000	000000000000000000000000000000000000000

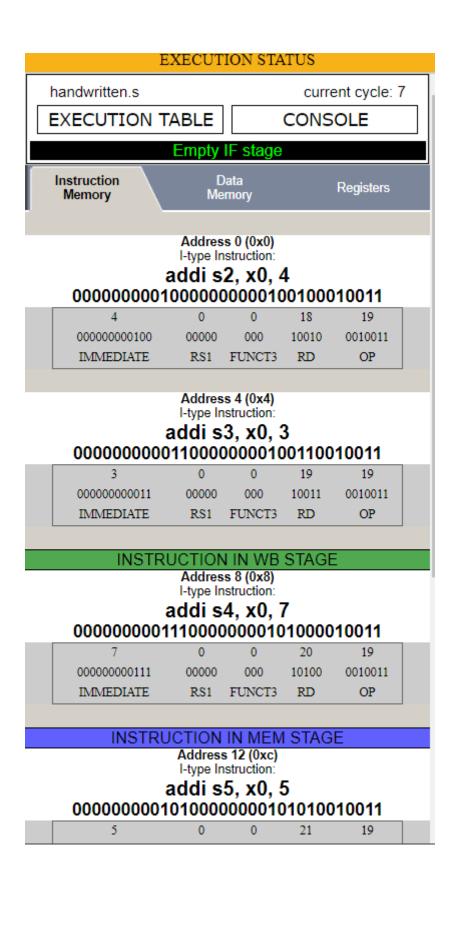
4	tp	0	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000
8	s0/fp	5120	0000000000000000001010000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	4	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5	0	000000000000000000000000000000000000000
31	t6	0	000000000000000000000000000000000000000

		0	Step			
han	ndwritten.s			curre	ent cycle: 6	
EX	EXECUTION TABLE			CONSOLE		
	truction lemory		ata mory		Registers	
	000000000	I-type In addi s			10011	
	4	0	0	18	19	
	00000000100	00000	000	10010	0010011	
	IMMEDIATE	RS1	FUNCT3	RD	OP	
	INSTR	LICTION	I IN WB	STAGE	=	
	1110111	Addres	s 4 (0x4)	01/102	-	
			struction:			
		addi s				
	000000000	0110000	0000010	01100	10011	
	3	0	0	19	19	
	000000000011	00000	000	10011	0010011	
	IMMEDIATE	RS1	FUNCT3	RD	OP	
	INSTRI	JCTION	IN MEM	STAG	F	
	INSTIC	Addres	s 8 (0x8)	JIAO	_	
			struction:	_		
		addi s				
	000000000	1110000	0000010	10000	10011	
					40	
	7	0	0	20	19	
	7 00000000111	00000	000	20 10100	0010011	
	7 00000000111 IMMEDIATE	•				
	IMMEDIATE	00000 RS1	000 FUNCT3	10100 RD	0010011 OP	
	IMMEDIATE	00000 RS1	000 FUNCT3	10100 RD	0010011 OP	
	IMMEDIATE	00000 RS1 RUCTION Address	000 FUNCT3	10100 RD	0010011 OP	
	IMMEDIATE	00000 RS1  RUCTION Address I-type In	NIN EX s 12 (0xc) struction:	10100 RD STAGE	0010011 OP	
	IMMEDIATE	00000 RS1  RUCTION Address I-type In	NIN EX s 12 (0xc) struction:	10100 RD STAGE	0010011 OP	

	Instructio Memory		Data Memory	Registers
R.No.	Reg.Id.	Dec.Val	Binary \	Value (32 bit)
0	x0	0	00000000000000	000000000000000000000000000000000000000
1	ra	0	00000000000000	0000000000000000000
2	sp	5120	000000000000000	000001010000000000
3	gp	1024	000000000000000	000000010000000000
4	tp	0	000000000000000	0000000000000000000
5	t0	0	000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000	000000000000000000000000000000000000000
7	t2	0	000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000	000001010000000000
9	s1	0	000000000000000	000000000000000000000000000000000000000
10	a0	0	000000000000000	000000000000000000000000000000000000000
11	a1	0	000000000000000	000000000000000000000000000000000000000
12	a2	0	000000000000000	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000	000000000000000000000000000000000000000
14	a4	0	000000000000000	000000000000000000000000000000000000000
15	a5	0	000000000000000	000000000000000000000000000000000000000
16	a6	0	000000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000	000000000000000000000000000000000000000
18	s2	4	000000000000000	0000000000000000100
19	s3	3	000000000000000000000000000000000000000	000000000000000011
20	s4	0	000000000000000	000000000000000000000000000000000000000
21	s5	0	000000000000000	000000000000000000000000000000000000000
22	s6	0	000000000000000	000000000000000000000000000000000000000
23	<b>s</b> 7	0	000000000000000	000000000000000000000000000000000000000
24	c0	۸	000000000000000000000000000000000000000	000000000000000000000000000000000000000

handwritten.s			current cycle: 6		
EX	ECUT	ION TABI	LE CONSOLE		
	3F				
4	tp	0	000000000000000000000000000000000000000		
5	t0	0	000000000000000000000000000000000000000		
6	t1	0	000000000000000000000000000000000000000		
7	t2	0	000000000000000000000000000000000000000		
8	s0/fp	5120	000000000000000000101000000000		
9	s1	0	000000000000000000000000000000000000000		
10	a0	0	000000000000000000000000000000000000000		
11	a1	0	000000000000000000000000000000000000000		
12	a2	0	000000000000000000000000000000000000000		
13	<b>a</b> 3	0	000000000000000000000000000000000000000		
14	a4	0	000000000000000000000000000000000000000		
15	a5	0	000000000000000000000000000000000000000		
16	a6	0	000000000000000000000000000000000000000		
17	a7	0	000000000000000000000000000000000000000		
18	s2	4	000000000000000000000000000000000000000		
19	s3	3	00000000000000000000000000000011		
20	s4	0	000000000000000000000000000000000000000		
21	s5	0	000000000000000000000000000000000000000		
22	s6	0	000000000000000000000000000000000000000		
23	s7	0	000000000000000000000000000000000000000		
24	s8	0	000000000000000000000000000000000000000		
25	s9	0	000000000000000000000000000000000000000		
26	s10	0	000000000000000000000000000000000000000		
27	s11	0	000000000000000000000000000000000000000		
28	t3	0	000000000000000000000000000000000000000		
29	t4	0	000000000000000000000000000000000000000		
30	t5	0	000000000000000000000000000000000000000		
31	t6	0	000000000000000000000000000000000000000		

7° Step



#### Empty IF stage

#### INSTRUCTION IN WESTAGE

Address 8 (0x8) I-type Instruction:

# addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19	
00000000111	00000	000	10100	0010011	ı
IMMEDIATE	RS1	FUNCT3	RD	OP	

#### INSTRUCTION IN MEM STAGE

Address 12 (0xc) I-type Instruction:

# addi s5, x0, 5 0000000010100000000101010010011

5	0	0	21	19
00000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN EX STAGE

Address 16 (0x10) I-type Instruction:

#### addi s6, x0, 6 0000000011000000000101100010011

6	0	0	22	19
00000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN ID STAGE

Address 20 (0x14) R-type Instruction:

0	19	18	0	23	51	
0000000	10011	10010	000	10111	0110011	
FUNCT7	RS2	RS1	FUNCT3	RD	OP	

handwritten.s  EXECUTION TABLE				current cycle: 7		
EX	ECUI	ION IAB	LE		ONSOLE	ᆜ
		En	npty II	F stage		
	Instruction Memory		Da Men		Registers	
R.No.	Reg.ld.	Dec.Val		Binary '	Value (32 bit)	
0	x0	0	0000	0000000000	000000000000000000000000000000000000000	0000
1	ra	0	0000	0000000000	000000000000000000000000000000000000000	0000
2	sp	5120	0000	000000000	000000101000000	0000
3	gp	1024	0000	000000000	000000001000000	0000
4	tp	0	0000	0000000000	000000000000000000000000000000000000000	0000
5	t0	0	0000	0000000000	000000000000000000000000000000000000000	0000
6	t1	0	0000	0000000000	000000000000000000000000000000000000000	0000
7	t2	0	0000	0000000000	000000000000000000000000000000000000000	0000
8	s0/fp	5120	0000	0000000000	00000101000000	0000
9	s1	0	0000	0000000000	000000000000000000000000000000000000000	0000
10	a0	0	0000	0000000000	000000000000000000000000000000000000000	0000
11	a1	0	0000	0000000000	000000000000000000000000000000000000000	0000
12	a2	0	0000	0000000000	000000000000000000000000000000000000000	0000
13	a3	0	0000	0000000000	000000000000000000000000000000000000000	0000
14	a4	0	0000	0000000000	000000000000000000000000000000000000000	0000
15	a5	0	0000	0000000000	000000000000000000000000000000000000000	0000
16	a6	0	0000	0000000000	000000000000000000000000000000000000000	0000
17	a7	0	0000	0000000000	000000000000000000000000000000000000000	0000
18	s2	4	0000	0000000000	000000000000000000000000000000000000000	0100
19	s3	3	0000	0000000000	000000000000000000000000000000000000000	0011
20	s4	7	0000	0000000000	000000000000000000000000000000000000000	0111
21	s5	0	0000	0000000000	000000000000000000000000000000000000000	0000
22	s6	0	0000	0000000000	000000000000000000000000000000000000000	0000
23	s7	0	0000	0000000000	000000000000000000000000000000000000000	0000

handwritten.s current cycle: 7 **EXECUTION TABLE** CONSOLE Empty IF stage 4 | W | U t0 0 0 t1 0 s0/fp 5120 000000000000000000101000000000 s1 0 0 a0 0 a1 0 a2 a3 0 0 a4 0 a5 0 a6 a7 0 4 00000000000000000000000000000011 3 **s**3 s4 7 0000000000000000000000000000111 20 0 0 s6 0 **s**7 **s8** 0 s9 0 0 s10 0 0 t4 0 0 t5 0 t6

		•		
nandwritten.s			curre	ent cycle:
XECUTION T	ABLE		CONS	OLE
		IF stage		
	Empty	ID stage		
Instruction Memory		)ata emory		Registers
	Addres	s 0 (0x0)		
		struction:	4	
0000000001		2, x0, 4		10011
4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP
	Addres	s 4 (0x4)		
	2.	struction:		
0000000000		3, x0, 3 0000010		10011
3	0	0	19	19
00000000011	00000	000	10011	0010011
00000000011 IMMEDIATE	00000 RS1	000 FUNCT3	10011 RD	0010011 OP
	RS1	FUNCT3		
IMMEDIATE	RS1 Addres	FUNCT3	RD	
IMMEDIATE	Addres I-type Ir	FUNCT3  8s 8 (0x8) estruction: 4, x0,	RD	OP
IMMEDIATE	Addres I-type Ir addi s	FUNCT3  ss 8 (0x8) astruction: 4, x0, 7 0000010	RD 7 010000	OP 110011
000000001	Addres I-type Ir addi s 110000	FUNCT3  ss 8 (0x8) astruction: 4, x0, 7 0000010	7 010000	OP 110011
IMMEDIATE	Addres I-type Ir addi s	FUNCT3  ss 8 (0x8) astruction: 4, x0, 7 0000010	RD 7 010000	OP 110011
000000000111	Addres    -type   r     addi	FUNCT3  8s 8 (0x8) estruction: 4, x0, 7 0000010 0 0000	7 010000 20 10100	OP 010011 19 0010011
0000000001 7 000000000111 IMMEDIATE	Addres I-type Ir addi s 110000 0 00000 RS1	FUNCT3  8s 8 (0x8) estruction: 4, x0, 7 0000010 0 0000	7 010000 20 10100 RD	OP 010011 19 0010011 OP
0000000001 7 000000000111 IMMEDIATE	Address I-type Ir addi so I 110000 0 00000 RS1	FUNCT3  ss 8 (0x8) astruction: 4, x0, 7 0000010 0 000 FUNCT3	7 010000 20 10100 RD	OP 010011 19 0010011 OP
0000000001 7 000000000111 IMMEDIATE	Address I-type Ir O 0 00000 RS1	FUNCT3  ss 8 (0x8) astruction: 4, x0, 7 0000010 0 000 FUNCT3  VIN WB ss 12 (0xc) astruction:	7 010000 20 10100 RD	OP 010011 19 0010011 OP
0000000001 7 000000000111 IMMEDIATE	Address I-type Ir Address I-type Ir Address I-type Ir addi s	FUNCT3  ss 8 (0x8) estruction: 4, x0, 7 0000010 0 000 FUNCT3  N IN WB s 12 (0xc) estruction: 5, x0, 8	7 010000 20 10100 RD	OP 110011 19 0010011 OP

handwritten.s current cycle: 8

EXECUTION TABLE CONSOLE

#### Empty IF stage Empty ID stage

I-type Instruction:

#### addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN WB STAGE

Address 12 (0xc) I-type Instruction:

#### addi s5, x0, 5 0000000010100000000101010010011

5	0	0	21	19
00000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN MEM STAGE

Address 16 (0x10) I-type Instruction:

#### addi s6, x0, 6 0000000011000000000101100010011

6	0	0	22	19
00000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN EX STAGE

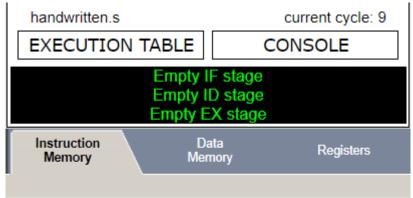
Address 20 (0x14) R-type Instruction:

0	19	18	0	23	51	
0000000	10011	10010	000	10111	0110011	
FUNCT7	RS2	RS1	FUNCT3	RD	OP	

# Empty IF stage Empty ID stage

	Instruction Memory		Data Memory	Registers
R.No.	Reg.Id.	Dec.Val	Binary '	Value (32 bit)
0	x0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
1	ra	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
2	SD	5120	000000000000000000000000000000000000000	000001010000000000
3	gp	1024	000000000000000000000000000000000000000	000000010000000000
4	tp	0	000000000000000	000000000000000000000000000000000000000
5	t0	0	0000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000	000000000000000000000000000000000000000
7	t2	0	0000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	0000000000000000	000001010000000000
9	s1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
10	a0	0	000000000000000	000000000000000000000000000000000000000
11	a1	0	000000000000000	000000000000000000000000000000000000000
12	a2	0	000000000000000	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
18	s2	4	000000000000000000000000000000000000000	000000000000000000000000000000000000000
19	s3	3	000000000000000000000000000000000000000	0000000000000000011
20	s4	7	000000000000000000000000000000000000000	0000000000000000111
21	s5	5	000000000000000000000000000000000000000	0000000000000000101
22	s6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000

handwritten.s				current cycle: 8
EX	EXECUTION TABLE			CONSOLE
				F stage
5	l to	0		O stage 000000000000000000000000000000000000
6	t1	0	0000	000000000000000000000000000000000000000
7	t2	0	0000	000000000000000000000000000000000000000
8	s0/fp	5120	0000	000000000000000101000000000
9	s1	0	0000	000000000000000000000000000000000000000
10	a0	0	0000	000000000000000000000000000000000000000
11	a1	0	0000	000000000000000000000000000000000000000
12	a2	0	0000	000000000000000000000000000000000000000
13	<b>a</b> 3	0	0000	000000000000000000000000000000000000000
14	a4	0	0000	000000000000000000000000000000000000000
15	a5	0	0000	000000000000000000000000000000000000000
16	a6	0	0000	000000000000000000000000000000000000000
17	a7	0	0000	000000000000000000000000000000000000000
18	s2	4	0000	000000000000000000000000000000000000000
19	s3	3	0000	000000000000000000000000000011
20	s4	7	0000	00000000000000000000000000111
21	s5	5	0000	000000000000000000000000000000000000000
22	s6	0	0000	000000000000000000000000000000000000000
23	s7	0		000000000000000000000000000000000000000
24	s8	0		000000000000000000000000000000000000000
25	s9	0		000000000000000000000000000000000000000
26	s10	0		000000000000000000000000000000000000000
27	s11	0		000000000000000000000000000000000000000
28	t3	0		000000000000000000000000000000000000000
29	t4	0		000000000000000000000000000000000000000
30	t5	0		000000000000000000000000000000000000000
31	t6	0	0000	000000000000000000000000000000000000000



Address 0 (0x0) I-type Instruction:

#### addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4) I-type Instruction:

#### addi s3, x0, 3 0000000001100000000100110010011

3	0	0	19	19
00000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8) I-type Instruction:

# addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

•	21	17
	40404	0040044
	****	

handwritten.s current cycle: 9

EXECUTION TABLE CONSOLE

Empty IF stage Empty ID stage Empty EX stage

Address o (UXO)
I-type Instruction:

# addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

#### addi s5, x0, 5 0000000010100000000101010010011

5	0	0	21	19
00000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

#### INSTRUCTION IN WB STAGE

Address 16 (0x10) I-type Instruction:

# addi s6, x0, 6 0000000011000000000101100010011

6	0	0	22	19	
00000000110	00000	000	10110	0010011	ı
IMMEDIATE	RS1	FUNCT3	RD	OP	

#### INSTRUCTION IN MEM STAGE

Address 20 (0x14) R-type Instruction:

0	19	18	0	23	51	]
0000000	10011	10010	000	10111	0110011	l
FUNCT7	RS2	RS1	FUNCT3	RD	OP	l

ha	ndwritte	en.s		current cycle: 9						
EXECUTION TABLE				CONSOLE						
Empty IF stage										
Empty ID stage Empty EX stage										
	Instruction Memory	n	Da Men	ıta	Registers					
R.No.	Reg.ld.	Dec.Val		Binary '	Value (32 bit)					
0	x0	0	0000	000000000000000000000000000000000000000						
1	ra	0	0000	0000000000	000000000000000000000000000000000000000					
2	sp	5120	0000	0000000000	000001010000000000					
3	gp	1024	0000	0000000000	000000010000000000					
4	tp	0	0000	0000000000	000000000000000000000000000000000000000					
5	t0	0	0000	0000000000	000000000000000000000000000000000000000					
6	t1	0	0000	0000000000	000000000000000000000000000000000000000					
7	t2	0	0000	0000000000	000000000000000000000000000000000000000					
8	s0/fp	5120	0000	0000000000	0000001010000000000					
9	s1	0	0000	0000000000	000000000000000000000000000000000000000					
10	a0	0	0000	0000000000	000000000000000000000000000000000000000					
11	a1	0	0000	0000000000	000000000000000000000000000000000000000					
12	a2	0	0000	0000000000	000000000000000000000000000000000000000					
13	<b>a</b> 3	0	0000	0000000000	000000000000000000000000000000000000000					
14	a4	0	0000	0000000000	000000000000000000000000000000000000000					
15	a5	0	0000	0000000000	000000000000000000000000000000000000000					
16	a6	0			000000000000000000000000000000000000000					
17	a7	0			000000000000000000000000000000000000000					
18	s2	4			000000000000000000000000000000000000000					
19	s3	3			00000000000000000011					
20	s4	7			0000000000000000111					
21	s5	5	0000	0000000000	00000000000000000101					

hai	ndwritte	en.s		current cycle: 9		
EX	ECUT	ION TAE	BLE	CONSOLE		
Empty IF stage Empty ID stage Empty EX stage						
6	t1	0	0000	000000000000000000000000000000000000000		
7	t2	0	0000	000000000000000000000000000000000000000		
8	s0/fp	5120	0000	000000000000000101000000000		
9	s1	0	0000	000000000000000000000000000000000000000		
10	a0	0	0000	000000000000000000000000000000000000000		
11	a1	0	0000	000000000000000000000000000000000000000		
12	a2	0	0000	000000000000000000000000000000000000000		
13	<b>a</b> 3	0	0000	000000000000000000000000000000000000000		
14	a4	0	0000	000000000000000000000000000000000000000		
15	a5	0	0000	000000000000000000000000000000000000000		
16	a6	0	0000	000000000000000000000000000000000000000		
17	a7	0	0000	000000000000000000000000000000000000000		
18	s2	4	0000	000000000000000000000000000000000000000		
19	s3	3	0000	000000000000000000000000000000001		
20	s4	7	0000	000000000000000000000000011		
21	s5	5	0000	000000000000000000000000000000000000000		
22	s6	6	0000	0000000000000000000000000110		
23	s7	0	0000	000000000000000000000000000000000000000		
24	s8	0	0000	000000000000000000000000000000000000000		
25	s9	0	0000	000000000000000000000000000000000000000		
26	s10	0	0000	000000000000000000000000000000000000000		
27	s11	0	0000	000000000000000000000000000000000000000		
28	t3	0	0000	000000000000000000000000000000000000000		
29	t4	0	0000	000000000000000000000000000000000000000		
30	t5	0	0000	000000000000000000000000000000000000000		
31	t6	0	0000	000000000000000000000000000000000000000		

### 10° Step

### EXECUTION STATUS handwritten.s current cycle: 10 **EXECUTION TABLE** CONSOLE Empty IF stage Empty ID stage Empty EX stage Empty MEM stage Data Memory Instruction Registers Memory Address 0 (0x0) I-type Instruction: addi s2, x0, 4 00000000100000000010010010011 0 0 18 19 000000000100 000 10010 0010011 00000 IMMEDIATE RS1 FUNCT3 RD OP Address 4 (0x4) I-type Instruction: addi s3, x0, 3 0000000001100000000100110010011 3 0 0 19 19 000000000011 00000 000 10011 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 8 (0x8) I-type Instruction: addi s4, x0, 7 00000000011100000000101000010011 0 20 19 0 000000000111 00000 000 10100 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 12 (0xc) I-type Instruction:

handwritten.s

current cycle: 10

**EXECUTION TABLE** 

CONSOLE

Empty IF stage Empty ID stage Empty EX stage Empty MEM stage

Address 8 (0x8) I-type Instruction:

### addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

### addi s5, x0, 5 0000000010100000000101010010011

5	0	0	21	19
00000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10) I-type Instruction:

### addi s6, x0, 6 0000000011000000000101100010011

6	0	0	22	19
00000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

### INSTRUCTION IN WB STAGE

Address 20 (0x14) R-type Instruction:

### add s7, s2, s3 00000001001110010000101110110011

0	19	18	0	23	51	
0000000	10011	10010	000	10111	0110011	
FUNCT7	RS2	RS1	FUNCT3	RD	OP	

### **EXECUTION STATUS** handwritten.s current cycle: 10 **EXECUTION TABLE** CONSOLE Empty IF stage **Empty ID stage** Empty EX stage Empty MEM stage Instruction Memory Data Registers Memory R.No. Reg.Id. Dec.Val Binary Value (32 bit) 0 x0 0 ra 5120 000000000000000000101000000000 sp 1024 000000000000000000001000000000 gp 0 tp 0 0 t1 t2 0 5120 000000000000000000101000000000 s0/fp 0 s1 a0 0 0 0 a2 a3 0 0 a4 0 a5 0 a6 0 a7 4 3 0000000000000000000000000000011 7 00000000000000000000000000000111

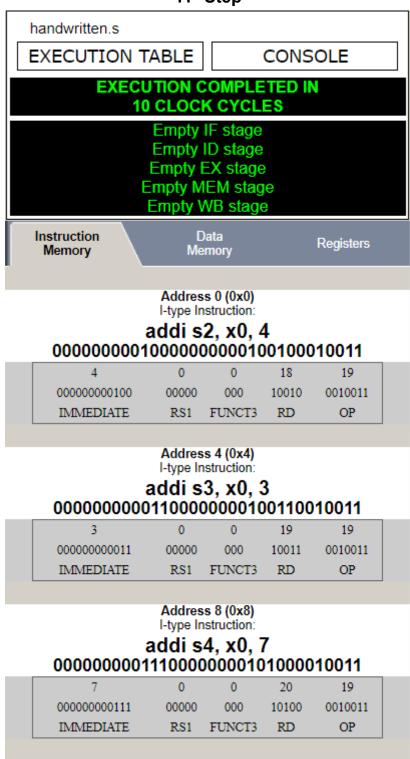
handwritten.s current cycle: 10 **EXECUTION TABLE** CONSOLE Empty IF stage Empty ID stage Empty EX stage Empty MEM stage 7 | t2 0 5120 000000000000000000101000000000 8 s0/fp s1 0 0 a0 0 a1 0 a2 a3 0 0 a4 0 a5 0 a6 0 a7 s2 4 3 0000000000000000000000000000011 s3 0000000000000000000000000000111 7 0000000000000000000000000000000101 s5 5 s6 6 00000000000000000000000000000110 7 00000000000000000000000000000111 0 **s**8 0 s9 s10 0 0 s11 0 t4 0

0

0

t6

### 11° Step



Address 12 (0xc)

handwritten.s

**EXECUTION TABLE** 

CONSOLE

### EXECUTION COMPLETED IN 10 CLOCK CYCLES

Empty IF stage Empty ID stage Empty EX stage **Empty MEM stage** Empty WB stage

### 000000001110000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

### addi s5, x0, 5 0000000010100000000101010010011

5	0	0	21	19
00000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10) I-type Instruction:

### addi s6, x0, 6 000000001100000000101100010011

6	0	0	22	19
00000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 20 (0x14) R-type Instruction:

### add s7, s2, s3 0000001001110010000101110110011

0	19	18	0	23	51	
0000000	10011	10010	000	10111	0110011	
FUNCT7	RS2	RS1	FUNCT3	RD	OP	

# handwritten.s EXECUTION TABLE CONSOLE EXECUTION COMPLETED IN

# 10 CLOCK CYCLES

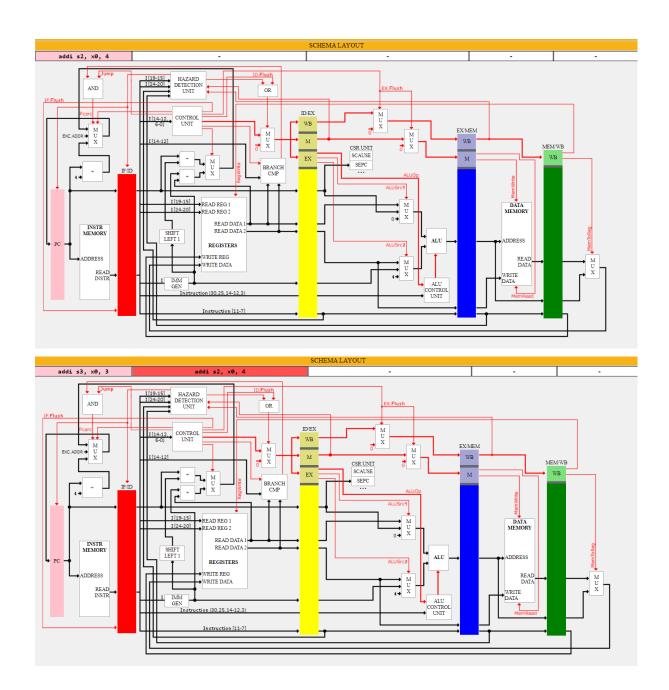
Empty IF stage Empty ID stage Empty EX stage Empty MEM stage Empty WB stage

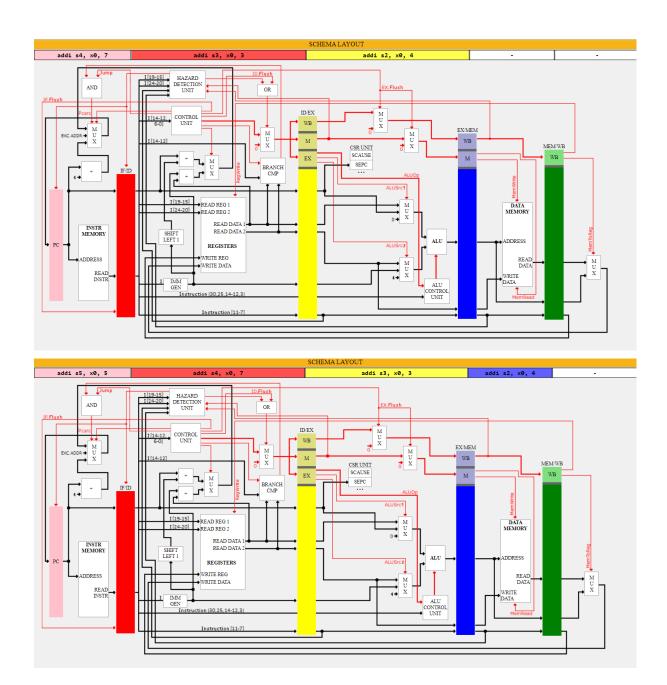
Instruction	Data	Registers
Memory	Memory	Registers

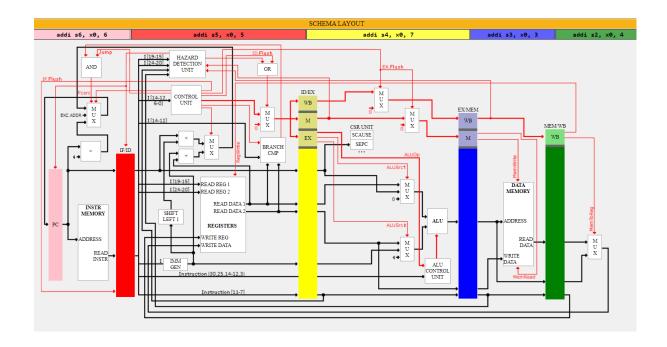
R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	000000000000000000000000000000000000000
1	ra	0	000000000000000000000000000000000000000
2	sp	5120	0000000000000000001010000000000
3	gp	1024	0000000000000000000010000000000
4	tp	0	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000
8	s0/fp	5120	0000000000000000001010000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	a3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	4	000000000000000000000000000000000000000

		EXEC	CUTION STATUS
ha	ndwritte	en.s	
EX	ECUT	TON TABI	LE CONSOLE
		EXECUTIO	ON COMPLETED IN
			OCK CYCLES
			pty IF stage
			pty ID stage pty EX stage
		Emp	ty MEM stage
0	c1	Emp 0	pty WB stage
9	s1 a0	0	000000000000000000000000000000000000000
11	a0 a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	a3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	4	000000000000000000000000000000000000000
19	s3	3	000000000000000000000000000000011
20	s4	7	00000000000000000000000000000111
21	s5	5	000000000000000000000000000000000000000
22	s6	6	000000000000000000000000000000110
23	s7	7	000000000000000000000000000000111
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5 t6	0	000000000000000000000000000000000000000
21	LO	U	

b)Passagem em três estágios representativos do Pipeline ("SCHEMA LAYOUT")



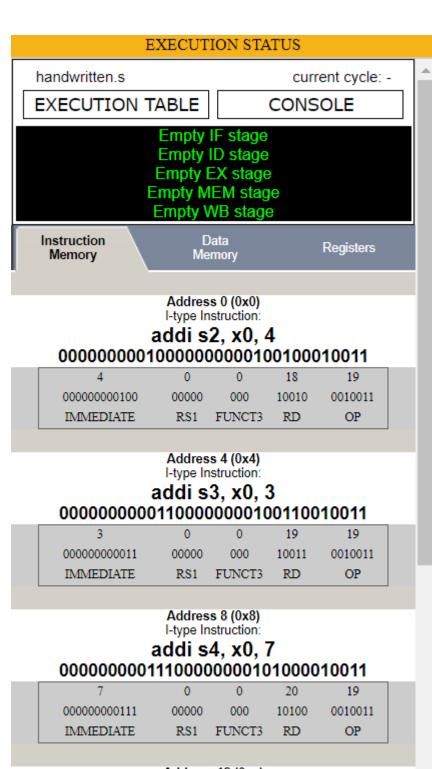




c) Resultado final da execução em Pipeline, por meio da Tabela da Execução do Programa ("EXECUTION TABLE").

EXE	CU	TIO	ON	TA	BL	E				
FULL LOOPS 🗸		CPU Cycles								
Instruction		2	3	4	5	6	7	8	9	10
addi s2, x0, 4		D	X	M	W					
addi s3, x0, 3		F	D	X	M	W				
addi s4, x0, 7			F	D	X	M	W			
addi s5, x0, 5				F	D	X	M	W		
addi s6, x0, 6					F	D	X	M	W	
add s7, s2, s3						F	D	X	M	W

d) Ciclos de CPU necessários para executar esse programa. Foram necessários 10 ciclos.



Address 12 (0xc) I-type Instruction:

handwritten.s

current cycle: -

**EXECUTION TABLE** 

CONSOLE

Empty IF stage Empty ID stage Empty EX stage Empty MEM stage Empty WB stage

Address 8 (0x8) I-type Instruction:

### addi s4, x0, 7 00000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

### addi s5, x0, 5 0000000010100000000101010010011

5	0	0	21	19
00000000101	00000	000	10101	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 16 (0x10) I-type Instruction:

### addi s6, x0, 6 0000000011000000000101100010011

6	0	0	22	19
00000000110	00000	000	10110	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 20 (0x14) R-type Instruction:

### add s7, s2, s3 00000001001110010000101110110011

0	19	18	0	23	51
0000000	10011	10010	000	10111	0110011
FUNCT7	RS2	RS1	FUNCT3	RD	OP

### **EXECUTION STATUS** handwritten.s current cycle: -EXECUTION TABLE CONSOLE Empty IF stage Empty ID stage **Empty EX stage** Empty MEM stage Empty WB stage Instruction Data Registers Memory Memory R.No. Reg.Id. Dec.Val Binary Value (32 bit) x0 0 0 ra 5120 000000000000000000101000000000 sp 000000000000000000001000000000 1024 gp 0 tp 0 0 0 t2 5120 000000000000000000101000000000 s0/fp 0 s1 0 a0 0 0 a2 a3 0 0 0 a5 a6 0 0 0 s2 0 s30

handwritten.s

current cycle: -

EXECUTION TABLE

CONSOLE

Empty IF stage Empty ID stage Empty EX stage Empty MEM stage Empty WB stage

/	LZ	U	***************************************
8	s0/fp	5120	00000000000000000001010000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5	0	000000000000000000000000000000000000000
31	t6	0	000000000000000000000000000000000000000

1° Step

### EXECUTION STATUS handwritten.s current cycle: 1 **EXECUTION TABLE** CONSOLE Empty ID stage Empty EX stage Empty MEM stage Empty WB stage Data Instruction Registers Memory Memory INSTRUCTION IN IF STAGE Address 0 (0x0) I-type Instruction: addi s2, x0, 4 00000000100000000010010010011 4 0 0 18 19 000000000100 00000 000 10010 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 4 (0x4) I-type Instruction: addi s3, x0, 3 000000000110000000100110010011 19 0 0 19 000000000011 00000 000 10011 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 8 (0x8) I-type Instruction: addi s4, x0, 7 000000001110000000101000010011 0 0 20 19 000000000111 00000 000 10100 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 12 (0xc) I-type Instruction:

### **EXECUTION STATUS** handwritten.s current cycle: 1 **EXECUTION TABLE** CONSOLE Empty ID stage **Empty EX stage Empty MEM stage Empty WB stage** Instruction Data Registers Memory Memory R.No. Reg.Id. Dec.Val Binary Value (32 bit) 0 x0 0 ra 5120 00000000000000000001010000000000 sp 1024 000000000000000000001000000000 gp 0 tp to 0 0 0 5120 000000000000000000101000000000 s0/fp 0 s1 a0 0 0 a1 0 a2 0 0 a4 0 a5 0 a6 0 a7 s2 0 0 0 **s4**

handwritten.s

current cycle: 1

**EXECUTION TABLE** 

CONSOLE

Empty ID stage Empty EX stage Empty MEM stage Empty WB stage

7	t2	0	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000000101000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000
24	s8	0	000000000000000000000000000000000000000
25	s9	0	000000000000000000000000000000000000000
26	s10	0	000000000000000000000000000000000000000
27	s11	0	000000000000000000000000000000000000000
28	t3	0	000000000000000000000000000000000000000
29	t4	0	000000000000000000000000000000000000000
30	t5	0	000000000000000000000000000000000000000
31	t6	0	000000000000000000000000000000000000000

### 2° Step

### **EXECUTION STATUS**

handwritten.s

current cycle: 2

**EXECUTION TABLE** 

CONSOLE

Empty EX stage Empty MEM stage Empty WB stage

Instruction Memory Data Memory

Registers

### INSTRUCTION IN ID STAGE

Address 0 (0x0) I-type Instruction:

### addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

### INSTRUCTION IN IF STAGE

Address 4 (0x4) I-type Instruction:

### addi s3, x0, 3 0000000001100000000100110010011

3	0	0	19	19
00000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8) I-type Instruction:

### addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

addi s5, x0, 5

00000000404000000004040404004004

### **EXECUTION STATUS** handwritten.s current cycle: 2 **EXECUTION TABLE** CONSOLE Empty EX stage **Empty MEM stage** Empty WB stage Instruction Data Registers Memory Memory Binary Value (32 bit) R.No. Reg.Id. Dec.Val 0 x0 0 ra 5120 000000000000000000101000000000 sp 1024 000000000000000000001000000000 gp 0 tp 0 t0 0 t1 0 5120 000000000000000000101000000000 s0/fp 0 s1 0 a0

0

0

0

0

0

0

0

0

0

0

0

a1

a2

a4

a5

a6

a7

s2

s3

s4

s5

### **EXECUTION STATUS** handwritten.s current cycle: 2 **EXECUTION TABLE** CONSOLE Empty EX stage **Empty MEM stage** Empty WB stage 6 t1 0 t2 0 5120 000000000000000000101000000000 s0/fp s1 0 a0 0 a1 0 0 a2 0 a3 0 a4 a5 0 0 a6 0 a7 0 s2 s3 0 0 0 s5 s6 0 0 0 **s8** s9 0 s10 0 s11 0 0 0 0 t6 0

### EXECUTION STATUS handwritten.s current cycle: 3 **EXECUTION TABLE** CONSOLE Empty MEM stage Empty WB stage Data Instruction Registers Memory Memory INSTRUCTION IN EX STAGE Address 0 (0x0) I-type Instruction: addi s2, x0, 4 00000000100000000010010010011 0 18 19 000000000100 00000 000 10010 0010011 IMMEDIATE RS1 FUNCT3 RD OP INSTRUCTION IN ID STAGE Address 4 (0x4) I-type Instruction: addi s3, x0, 3 000000000110000000100110010011 19 19 000000000011 00000 000 10011 0010011 OP RS1 FUNCT3 IMMEDIATE RD INSTRUCTION IN IF STAGE Address 8 (0x8) I-type Instruction: addi s4, x0, 7 000000001110000000010100001011 0 0 20 19 0010011 000000000111 00000 000 10100 IMMEDIATE FUNCT3 OP RS1 RD Address 12 (0xc) I-type Instruction: addi s5, x0, 5

handwritten.s

**EXECUTION TABLE** 

Instruction Memory CONSOLE

current cycle: 3

Registers

### Empty MEM stage Empty WB stage

Data Memory

R.No.	Reg.Id.	Dec.Val	Binary Value (32 bit)
0	x0	0	000000000000000000000000000000000000000
1	ra	0	000000000000000000000000000000000000000
2	sp	5120	000000000000000000101000000000
3	gp	1024	000000000000000000001000000000
4	tp	0	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000000101000000000
9	s1	0	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000
13	<b>a</b> 3	0	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000
18	s2	0	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000
		Charles Minds Villes	

### 4° Step

### **EXECUTION STATUS** handwritten.s current cycle: 4 **EXECUTION TABLE** CONSOLE Empty WB stage Instruction Data Registers Memory Memory INSTRUCTION IN MEM STAGE Address 0 (0x0) I-type Instruction: addi s2, x0, 4 00000000100000000010010010011 000000000100 00000 000 10010 0010011 IMMEDIATE RS1 FUNCT3 RD OP INSTRUCTION IN EX STAGE Address 4 (0x4) I-type Instruction: addi s3, x0, 3 000000000110000000100110010011 0 19 19 000000000011 00000 000 10011 0010011 IMMEDIATE RS1 FUNCT3 RD OP INSTRUCTION IN ID STAGE Address 8 (0x8) I-type Instruction: addi s4, x0, 7 00000000111000000010100001011 0 20 19 000000000111 00000 000 10100 0010011 IMMEDIATE RS1 FUNCT3 RD OP

INSTRUCTION IN IF STAGE Address 12 (0xc) I-type Instruction:

### **EXECUTION STATUS** handwritten.s current cycle: 4 **EXECUTION TABLE** CONSOLE Empty WB stage Instruction Memory Data Registers Memory R.No. Reg.Id. Dec.Val Binary Value (32 bit) 0 x0 ra 0 5120 000000000000000000101000000000 sp 1024 0000000000000000000001000000000 gp 0 tp t0 0 0 0 s0/fp 5120 000000000000000000101000000000 0 0 a0 0 a1 0 a3 0 0 a4 0 a5 0 a6 0 a7 0 s2 0 s3 **s4** 0 s50 0 0

### 5° Step

# handwritten.s current cycle: 5 EXECUTION TABLE CONSOLE Instruction Memory Data Memory Registers

### INSTRUCTION IN WB STAGE

Address 0 (0x0) I-type Instruction:

### addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

### INSTRUCTION IN MEM STAGE

Address 4 (0x4) I-type Instruction:

### addi s3, x0, 3 0000000001100000000100110010011

3	0	0	19	19
000000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

### INSTRUCTION IN EX STAGE

Address 8 (0x8) I-type Instruction:

### addi s4, x0, 7 00000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

### INSTRUCTION IN ID STAGE

Address 12 (0xc) I-type Instruction:

handwritten.s

current cycle: 5

EXECUTION TABLE

CONSOLE

	Instruction Memory		Data Memory	Registers
D.N.		D \/-I	Dia	\/-h (22 hh)
R.No.	Reg.Id.	Dec.Val	-	Value (32 bit)
0	x0	0		000000000000000000000000000000000000000
1	ra	0		000000000000000000000000000000000000000
2	sp	5120	000000000000000000000000000000000000000	000001010000000000
3	gp	1024	000000000000000000000000000000000000000	000000010000000000
4	tp	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
5	t0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
7	t2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000000000000000000000000000	000001010000000000
9	s1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
10	a0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
11	a1	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
12	a2	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
13	a3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
14	a4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
15	a5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
16	a6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
18	s2	4	000000000000000000000000000000000000000	000000000000000000000000000000000000000
19	s3	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
20	s4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
21	s5	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
74	c0	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000

### 6° Step **EXECUTION STATUS** handwritten.s current cycle: 6 **EXECUTION TABLE** CONSOLE Data Memory Instruction Registers Memory Address 0 (0x0) I-type Instruction:

### addi s2, x0, 4 00000000100000000010010010011

4	0	0	18	19	
00000000100	00000	000	10010	0010011	
IMMEDIATE	RS1	FUNCT3	RD	OP	

### CTION IN WB STAGE

Address 4 (0x4) I-type Instruction:

### addi s3, x0, 3 000000000110000000100110010011

3	0	0	19	19
00000000011	00000	000	10011	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

### INSTRUCTION IN MEM STAGE

Address 8 (0x8) I-type Instruction:

### addi s4, x0, 7 000000001110000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

### INSTRUCTION IN EX STAGE

Address 12 (0xc) I-type Instruction:

5	0	0	21	19	
---	---	---	----	----	--

handwritten.s

current cycle: 6

EXECUTION TABLE

CONSOLE

	Instruction Memory		Data Memory	Registers
			,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	)
R.No.	Reg.Id.	Dec.Val	Binary '	Value (32 bit)
0	x0	0	000000000000000	000000000000000000000000000000000000000
1	ra	0	000000000000000	000000000000000000000000000000000000000
2	sp	5120	000000000000000	000001010000000000
3	gp	1024	000000000000000	000000010000000000
4	tp	0	000000000000000	000000000000000000000000000000000000000
5	t0	0	000000000000000	000000000000000000000000000000000000000
6	t1	0	000000000000000	000000000000000000000000000000000000000
7	t2	0	000000000000000	000000000000000000000000000000000000000
8	s0/fp	5120	000000000000000	000001010000000000
9	s1	0	000000000000000	000000000000000000000000000000000000000
10	a0	0	000000000000000	000000000000000000000000000000000000000
11	a1	0	000000000000000	000000000000000000000000000000000000000
12	a2	0	000000000000000	000000000000000000000000000000000000000
13	a3	0	000000000000000	000000000000000000000000000000000000000
14	a4	0	000000000000000	000000000000000000000000000000000000000
15	a5	0	000000000000000	000000000000000000000000000000000000000
16	a6	0	000000000000000	000000000000000000000000000000000000000
17	a7	0	000000000000000	000000000000000000000000000000000000000
18	s2	4	000000000000000000000000000000000000000	000000000000000000000000000000000000000
19	s3	3	000000000000000000000000000000000000000	0000000000000000011
20	s4	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
21	s5	0	000000000000000	000000000000000000000000000000000000000
22	s6	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
23	s7	0	000000000000000000000000000000000000000	000000000000000000000000000000000000000
24	cQ.	n	000000000000000000000000000000000000000	000000000000000000000000000000000000000

### 7° Step EXECUTION STATUS handwritten.s current cycle: 7 **EXECUTION TABLE** CONSOLE Empty IF stage Data Memory Instruction Registers Memory Address 0 (0x0) I-type Instruction: addi s2, x0, 4 00000000100000000010010010011 4 0 18 19 0 000000000100 00000 000 10010 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 4 (0x4) I-type Instruction: addi s3, x0, 3 000000000110000000100110010011 3 0 0 19 19 000000000011 00000 000 10011 0010011 IMMEDIATE RS1 FUNCT3 RD OP INSTRU CTION IN WB STAGE Address 8 (0x8) I-type Instruction: addi s4, x0, 7 00000000111000000010100001011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

### INSTRUCTION IN MEM STAGE

Address 12 (0xc) I-type Instruction:

5	0	0	21	19	

### EXECUTION STATUS handwritten.s current cycle: 7 **EXECUTION TABLE** CONSOLE Empty IF stage Instruction Memory Data Registers R.No. Reg.Id. Binary Value (32 bit) Dec.Val 0 x0 0 ra 000000000000000000101000000000 5120 1024 000000000000000000001000000000 qp 0 tp 0 t<sub>0</sub> 0 0 s0/fp 5120 00000000000000000001010000000000 s1 0 a0 0 0 a1 0 0 a3 a4 0 0 a6 0 a7 0 4 s2 3 0000000000000000000000000000011 7 0000000000000000000000000000111 **s4** 0 **s**5 0 **s6** 0

### 8° Step EXECUTION STATUS handwritten.s current cycle: 8 EXECUTION TABLE CONSOLE Empty IF stage Empty ID stage Instruction Data Registers Memory Memory Address 0 (0x0) I-type Instruction: addi s2, x0, 4 00000000100000000010010010011 0 18 19 000000000100 00000 000 10010 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 4 (0x4) I-type Instruction: addi s3, x0, 3 000000000110000000100110010011 3 0 19 0 19 000000000011 00000 000 10011 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 8 (0x8) I-type Instruction: addi s4, x0, 7

## 000000001110000000101000010011

7	0	0	20	19
000000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

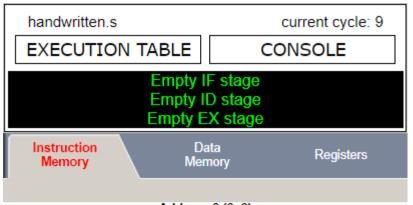
### INSTRUCTION IN WB STAGE

Address 12 (0xc) I-type Instruction:

5	0	0	21	19	

		EXE	CUTION	STAT	US
handwritten.s				current cycle: 8	
E	(ECUT	ION TAB	LE	С	ONSOLE
		Em	pty IF sta	age	
			pty ID sta		
	Instruction Memory		Data Memory		Registers
	Wiemory		Wellioly		\
R.No.	Reg.Id.	Dec.Val		Binary '	Value (32 bit)
0	x0	0	00000000	000000	000000000000000000000000000000000000000
1	ra	0	00000000	000000	000000000000000000000000000000000000000
2	sp	5120	00000000	000000	0000001010000000000
3	gp	1024	00000000	000000	000000010000000000
4	tp	0	00000000	000000	000000000000000000000000000000000000000
5	t0	0	00000000	000000	000000000000000000000000000000000000000
6	t1	0	00000000	000000	000000000000000000000000000000000000000
7	t2	0	00000000	000000	000000000000000000000000000000000000000
8	s0/fp	5120	00000000	000000	00000010100000000000
9	s1	0	00000000	000000	000000000000000000000000000000000000000
10	a0	0	00000000	000000	000000000000000000000000000000000000000
11	a1	0	00000000	000000	000000000000000000000000000000000000000
12	a2	0	00000000	000000	000000000000000000000000000000000000000
13	<b>a</b> 3	0	00000000	000000	000000000000000000000000000000000000000
14	a4	0			000000000000000000000000000000000000000
15	a5	0			000000000000000000000000000000000000000
16	a6	0			000000000000000000000000000000000000000
17	a7	0			000000000000000000000000000000000000000
18	s2	4			00000000000000000100
19	s3	3			00000000000000000011
20	s4	7			0000000000000000111
21	s5	5			0000000000000000101
22	s6	0	00000000	000000	000000000000000000000000000000000000000

9° Step



Address 0 (0x0) I-type Instruction:

### addi s2, x0, 4 000000001000000000010010011

4	0	0	18	19
00000000100	00000	000	10010	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 4 (0x4) I-type Instruction:

### addi s3, x0, 3 0000000001100000000100110010011

	3	0	0	19	19
000	000000011	00000	000	10011	0010011
IM	MEDIATE	RS1	FUNCT3	RD	OP

Address 8 (0x8) I-type Instruction:

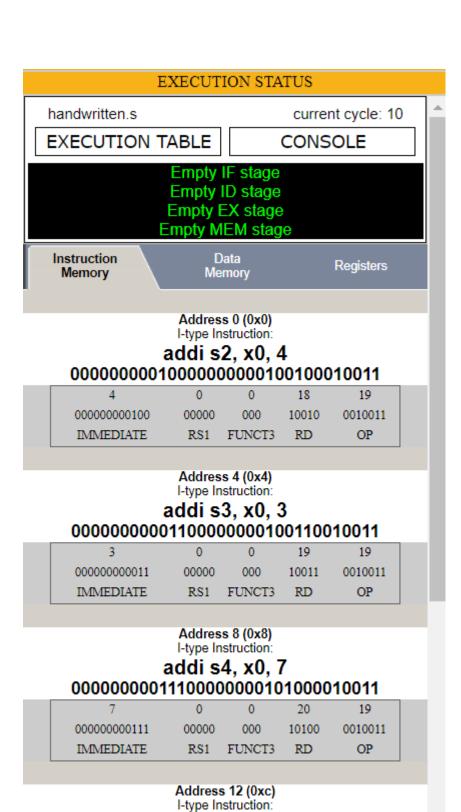
### addi s4, x0, 7 0000000011100000000101000010011

7	0	0	20	19
00000000111	00000	000	10100	0010011
IMMEDIATE	RS1	FUNCT3	RD	OP

Address 12 (0xc) I-type Instruction:

	ndwritter			current cycle: 9						
EX	(ECUT	ON TAB	LE	С	ONSOLE					
				F stage						
				D stage X stage						
	Instructior Memory		Da Men	ıta	Registers					
R.No.	Reg.Id.	Dec.Val		Rinary	Value (32 bit)					
		0	الممم		000000000000000000000000000000000000000					
0	x0	0			000000000000000000000000000000000000000					
1	ra									
2	sp	5120			0000001010000000000					
3	gp	1024			0000000010000000000					
4	tp	0			000000000000000000000000000000000000000					
5	t0	0			000000000000000000000000000000000000000					
6	t1	0			000000000000000000000000000000000000000					
7	t2	0			000000000000000000000000000000000000000					
8	s0/fp	5120			0000001010000000000					
9	s1	0			000000000000000000000000000000000000000					
10	a0	0			000000000000000000000000000000000000000					
11	a1	0			000000000000000000000000000000000000000					
12	a2	0	0000	0000000000	000000000000000000000000000000000000000					
13	a3	0	0000	0000000000	000000000000000000000000000000000000000					
14	a4	0	0000	0000000000	000000000000000000000000000000000000000					
15	a5	0	0000	0000000000	000000000000000000000000000000000000000					
16	a6	0	0000	0000000000	000000000000000000000000000000000000000					
17	a7	0	0000	0000000000	000000000000000000000000000000000000000					
18	s2	4	0000	0000000000	000000000000000000000000000000000000000					
19	s3	3	0000	000000000	00000000000000000011					
20	s4	7	0000	0000000000	00000000000000000111					
21	s5	5	0000	0000000000	00000000000000000101					

10° Step

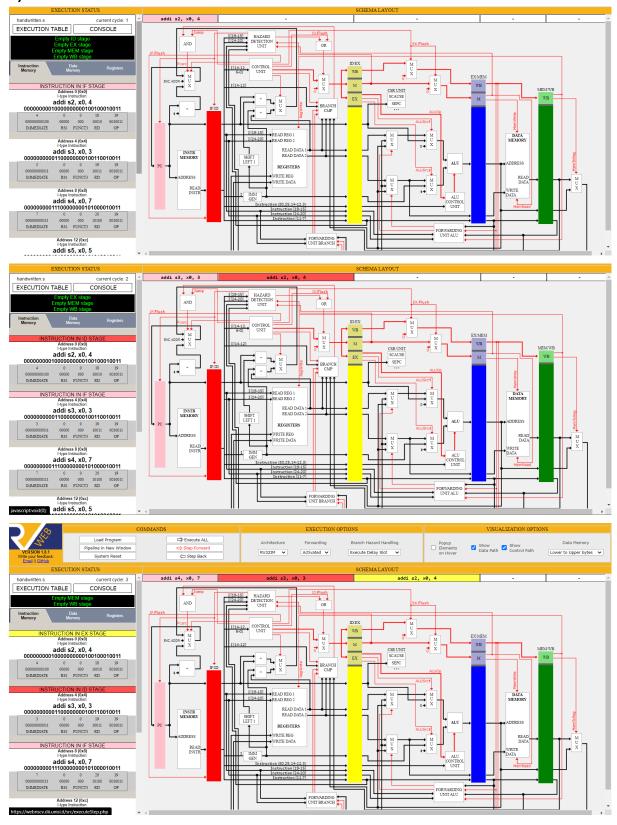


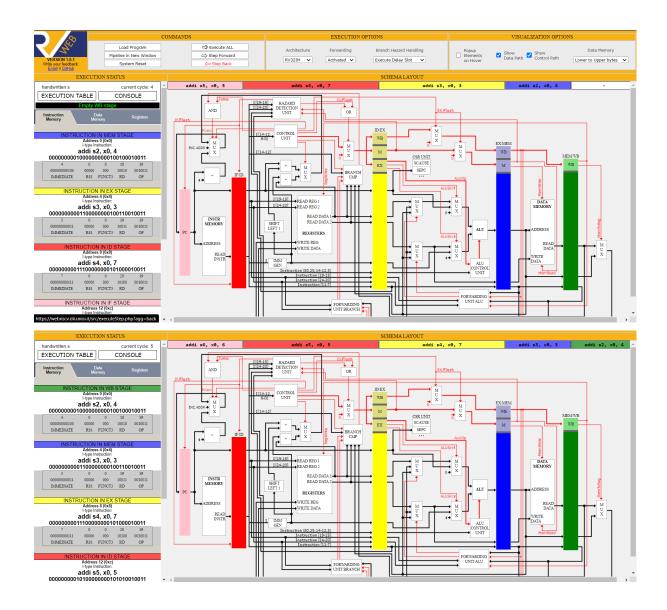
		EXE	CUTI	ON STAT	US						
hai	ndwritte	en.s		current cycle: 10							
		ION TAB	IF		ONSOLE						
	LCOI				ONSOLL						
				F stage D stage							
				X stage EM stage							
	Instructio Memory	n	Da Men		Registers						
					\						
R.No.	Reg.Id.	Dec.Val			Value (32 bit)						
0	x0	0			000000000000000000000000000000000000000						
1	ra	0			000000000000000000000000000000000000000						
2	sp	5120			00000010100000000000						
3	gp	1024			0000000010000000000						
4	tp	0			000000000000000000000000000000000000000						
5	t0	0			000000000000000000000000000000000000000						
6	t1	0			000000000000000000000000000000000000000						
7	t2	0			000000000000000000000000000000000000000						
8	s0/fp	5120			00000010100000000000						
9	s1	0			000000000000000000000000000000000000000						
10	a0	0			000000000000000000000000000000000000000						
11	a1	0			000000000000000000000000000000000000000						
12	a2	0			000000000000000000000000000000000000000						
13	a3	0			000000000000000000000000000000000000000						
14	a4	0			000000000000000000000000000000000000000						
15	a5	0			000000000000000000000000000000000000000						
16	a6	0			000000000000000000000000000000000000000						
17	a7	0			000000000000000000000000000000000000000						
18	s2	4			000000000000000000000000000000000000000						
19	s3	3			0000000000000000011						
20	s4	7	0000	0000000000	0000000000000000111						

11° Step

### EXECUTION STATUS handwritten.s **EXECUTION TABLE** CONSOLE EXECUTION COMPLETED IN **10 CLOCK CYCLES** Empty IF stage Empty ID stage Empty EX stage Empty MEM stage Empty WB stage Instruction Data Registers Memory Memory Address 0 (0x0) I-type Instruction: addi s2, x0, 4 00000000100000000010010010011 4 0 18 19 000000000100 10010 0010011 00000 000 IMMEDIATE RS1 FUNCT3 RD OP Address 4 (0x4) I-type Instruction: addi s3, x0, 3 000000000110000000100110010011 19 19 000000000011 00000 000 10011 0010011 IMMEDIATE RS1 FUNCT3 RD OP Address 8 (0x8) I-type Instruction: addi s4, x0, 7 00000000011100000000101000010011 0 0 20 19 000000000111 00000 000 10100 0010011 IMMEDIATE RS1 FUNCT3 RD OP

Address 12 (0xc)





c)

FULL LOOPS V	CPU Cycles									
Instruction	1	2	3	4	5	6	7	8	9	10
addi s2, x0, 4	F	D	X	M	W					
addi s3, x0, 3		F	D	X	M	W				
addi s4, x0, 7			F	D	X	M	W			
addi s5, x0, 5				F	D	X	M	W		
addi s6, x0, 6					F	D	X	M	W	
add s7, s2, s3						F	D	X	M	W

d) Foram necessários 10 ciclos.